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(54) **Title:** RECONFIGURABLE INTELLIGENT SURFACES WITH INTEGRATED CHALCOGENIDE PHASE-DELAY ELEMENTS

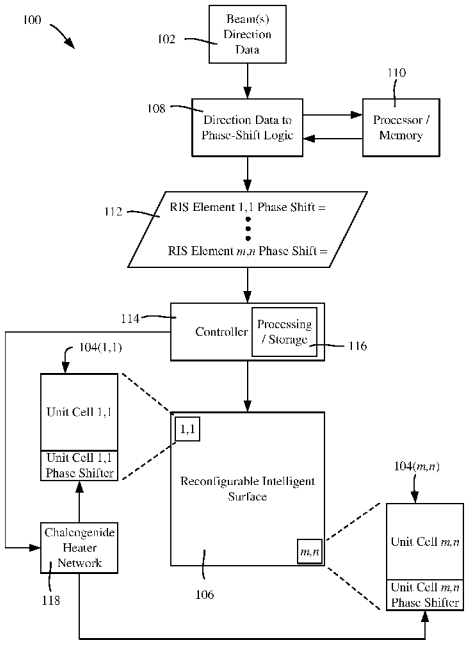


FIG. 1

(57) **Abstract:** The technology described herein is directed towards a design and implementation of a unit cell for a reconfigurable intelligent surface / reflectarray by incorporating reconfigurability within a phase-delay element of the unit cell. Reconfigurability is directly incorporated into the unit cell via a variable length phase delay line element and PCM-based (e.g., mmWave) phase shifter that determines the unit cell's phase shift by changing the length of the phase delay line element. One implementation is directed to a monolithic integration of the element using chalcogenide materials as switch elements with pulsed actuation to switch among different available lengths that determine the length of the phase delay line element, resulting in a significant reduction in power consumption, area saving, and digital reconfigurability.

WO 2025/147276 A1

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RECONFIGURABLE INTELLIGENT SURFACES WITH INTEGRATED CHALCOGENIDE PHASE-DELAY ELEMENTS

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RELATED APPLICATION

[0001] This application claims priority to U.S. Non-Provisional Patent Application No. 18/403,434, filed January 3, 2024, and entitled "RECONFIGURABLE INTELLIGENT SURFACES WITH INTEGRATED CHALCOGENIDE PHASE-DELAY ELEMENTS", the entirety of which priority application is hereby incorporated by reference herein.

BACKGROUND

[0002] Reconfigurable intelligent surfaces (alternatively referred to as intelligent reflective surfaces, or metasurfaces) are man-made thin reflective surfaces whose electromagnetic response can be electronically controlled. Intelligent reflective surfaces thus have the ability to boost the spectral energy and spectral efficiency of redirected electromagnetic waves. Because an intelligent reflective surface can change the phase shifts of signals reflected at the surface, intelligent reflective surfaces are being evaluated for use in beyond fifth generation (B5G) and sixth generation (6G) wireless communication and wireless sensing networks.

[0003] Traditionally, the elements, or unit cells, of a reconfigurable intelligent surface have a variable conductive patch size, wherein the size of the conductive patch determines the phase shift of the unit cell. By controlling the phase shifts among the unit cells of a reconfigurable intelligent surfaces, the reflections of the unit cells with respect to an impinging electromagnetic wave can be combined into a beam steered in a specified direction, or into multiple beams split into multiple directions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The technology described herein is illustrated by way of example and not limited in the accompanying figures in which like reference numerals indicate similar elements and in which:

[0005] FIG. 1 is an example block diagram showing a system for controlling phase shifts of unit cells based on varying transmission line path lengths that determine lengths of phase-delay lines of the unit cells, in accordance with various example embodiments and implementations of the subject disclosure.

[0006] FIG. 2A and 2B are representations of example unit cells conceptually showing different phase shifts corresponding to different lengths of a phase-delay line element of a unit cell, in accordance with various example embodiments and implementations of the subject disclosure.

[0007] FIG. 3 is a representation of an example part of a phase shifter of a unit cell conceptually showing selection of different phase shifts by selecting among different length candidate paths for a phase-delay line of a unit cell, in accordance with various example embodiments and implementations of the subject disclosure.

[0008] FIG. 4 is a representation of an example part of a phase shifter of a unit cell conceptually showing selection of different phase shifts by selecting among different first candidate sub-paths and selecting among different second candidate sub-paths, for a phase-delay line of a unit cell, in accordance with various example embodiments and implementations of the subject disclosure.

[0009] FIG. 5 is an exploded view representation of a unit cell in which the length of a variable length phase-delay line element is determined by a chalcogenide-based phase shifter that is part of the unit cell, in accordance with various example embodiments and implementations of the subject disclosure.

[0010] FIG. 6 is a representation of an example chalcogenide-based phase shifter that is part of a unit cell and is controlled by a pulse-code modulation-based (PCM-based) controller, in accordance with various example embodiments and implementations of the subject disclosure.

[0011] FIG. 7 is a graphical representation of the reflection phase of a unit cell with a variable length phase-delay line element, showing a substantially linear phase profile with a

larger range in contrast to the non-linear phase profile of a variable patch size unit cell, in accordance with various example embodiments and implementations of the subject disclosure.

[0012] FIG. 8 is a graphical representation of the reflection magnitude of a unit cell with a variable length phase-delay line element, showing reduced magnitude variation in contrast to the magnitude variation of a variable patch size unit cell, in accordance with various example embodiments and implementations of the subject disclosure.

[0013] FIG. 9A and 9B are graphical representations of simulated relative phase shift (FIG. 9A) and group delay (FIG. 9B) of the chalcogenide-based phase shifter in different phase shift states over a range of frequencies with a 25 - 34 GHz band, in accordance with various example embodiments and implementations of the subject disclosure.

[0014] FIG. 10 is a flow diagram showing example operations related to controlling a phase shifter to change a phase shift of the variable phase-shift unit cell by switching among conductive and non-conductive states of chalcogenide material elements, in accordance with various example embodiments and implementations of the subject disclosure.

[0015] FIG. 11 is a flow diagram showing example operations related to changing a phase shift of a unit cell by determining respective states of respective individual chalcogenide components of respective switches of the unit cell, to vary a transmission line path length of a variable phase-delay line element, in accordance with various example embodiments and implementations of the subject disclosure.

DETAILED DESCRIPTION

[0016] The technology described herein is generally directed towards a design and implementation of a reconfigurable intelligent surfaces (RIS) realized by incorporating reconfigurability within a phase-delay element of the unit cells that form the reconfigurable intelligent surfaces, as an alternative to the commonly used variable size element patch. The technology described herein overcomes many known problems with reconfigurable intelligent surfaces that have unit cells with variable patch sizes, including non-linearity of an element's phase profile caused by using a variable of resonating frequency for phase profile. Such non-linearity resulting from the variable patch sizes limits the achievable bandwidth of the reflectarray surface, because non-linearity leads to distorted radiation patterns, and further, the restricted operational bandwidth due to the non-linearity cannot effectively

support wideband applications such as satellite and automotive radar systems. Another problem is fabricating reflectarrays with variable-sized elements, which requires high manufacturing precision due to its aggressive variation near its resonating frequency; imprecise element sizes result in performance degradation and reduced overall efficiency, which limits their use in high-frequency applications. Variable-sized elements also can introduce high insertion / reflection loss due to increased material usage, impedance mismatches and their usage in resonating frequency, which reduces the overall efficiency of a reflectarray, resulting in decreased signal strength, a lower signal-to-noise ratio and degraded system performance. Non-uniform loss distribution from variable patch sizes results in uneven power distribution and compromises the performance of a reflectarray, causing high sidelobes and a lower signal-to-noise ratio. Further, the irregularities introduced by the use of variable-sized elements violate the assumption of an infinite array, especially on the area where phase wrapping occurs; such a violation of the infinite array approximation can lead to deviations in the radiation pattern and degradation of the beam-steering capabilities of a reflectarray.

[0017] Instead, described herein introduces reconfigurability directly into a phase-delay element (via a variable length phase delay line element), which overcomes the various challenges associated with typically-used variable size conductive patches, including as improved bandwidth and reduced fabrication costs with lower precision requirements that result technology described herein. One implementation of the technology described herein is directed to a monolithic integration of the element using chalcogenide materials, such as germanium antimony telluride (GST) alloys. Usage of this material offers advantages such as negligible power consumption through pulsed actuation and reduced design and external wiring.

[0018] It should be understood that any of the examples and/or descriptions herein are non-limiting. Thus, any of the embodiments, example embodiments, concepts, structures, functionalities or examples described herein are non-limiting, and the technology may be used in various ways that provide benefits and advantages in communications and computing in general. It also should be noted that terms used herein, such as “maximize” “optimize” or “optimal” and the like only represent objectives to move towards a more maximal or optimal state, rather than necessarily obtaining ideal results.

[0019] Reference throughout this specification to “one embodiment,” “an embodiment,” “one implementation,” “an implementation,” etc. means that a particular feature, structure,

characteristic and/or attribute described in connection with the embodiment / implementation can be included in at least one embodiment / implementation. Thus, the appearances of such a phrase "in one embodiment," "in an implementation," etc. in various places throughout this specification are not necessarily all referring to the same embodiment / implementation. Furthermore, the particular features, structures, characteristics and/or attributes may be combined in any suitable manner in one or more embodiments / implementations. Repetitive description of like elements employed in respective embodiments may be omitted for sake of brevity.

[0020] The detailed description is merely illustrative and is not intended to limit embodiments and/or application or uses of embodiments. Furthermore, there is no intention to be bound by any expressed or implied information presented in the preceding sections, or in the Detailed Description section.

[0021] One or more embodiments are now described with reference to the drawings, wherein like referenced numerals are used to refer to like elements throughout. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a more thorough understanding of the one or more embodiments. It is evident, however, in various cases, that the one or more embodiments can be practiced without these specific details.

[0022] Further, it is to be understood that the present disclosure will be described in terms of a given illustrative architecture; however, other architectures, structures, materials and process features, and steps can be varied within the scope of the present disclosure.

[0023] Example embodiments of the subject disclosure will now be described more fully hereinafter with reference to the accompanying drawings in which example components, graphs and/or operations are shown. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the various embodiments. However, the subject disclosure may be embodied in many different forms and should not be construed as limited to the examples set forth herein.

[0024] FIG. 1 shows a system 100 in which beam direction data 102 is used to determine the phase shifts of unit cells 104(1,1) – 104(m,n) of a reconfigurable intelligent surface 106 (typically $m = n$ to provide a square reconfigurable intelligent surface). In general, the beam direction data 102, which can refer to a single beam direction or multiple directions of a split

beam, is determined by the unit cells' individually controllable phase shifts with respect to an electromagnetic wave impinging on the reconfigurable intelligent surface 106. Direction data-to-phase-shift logic 108, e.g., coupled to or incorporating a suitable processor and memory 110, converts the desired beam direction data to the respective individual phase shift data (values) 112 needed for each of the respective unit cells 104(1,1) – 104(m,n) that will result in the desired beam direction data being achieved. As can be readily appreciated, the phase-shift logic 108 can be remote with respect to the location of the reconfigurable intelligent surface 106, as the individual phase shift data 112 can be determined at and communicated from a remote location to the reconfigurable intelligent surface location. Alternatively the requested beam direction data 102 can be communicated to the location of the reconfigurable intelligent surface 106, which can decide the phase shifts based thereon.

[0025] A controller 114, e.g., having some processing and storage capabilities (block 116) located at the reconfigurable intelligent surface 106 obtains or determines the individual phase shift values 112. Each of the unit cells 104(1,1) – 104(m,n) includes a phase shifter as described herein, e.g., on the back surface of each unit cell. The phase shifters each comprise a number of single-pole, multiple-throw switches that are based on phase change material (chalcogenide) elements (component parts of the switches).

[0026] One or more intended uses of the technology described herein is for millimeter wave (mmWave) applications. With mmWave phase shifters, size and power consumption are significant criteria. For these reasons, a chalcogenide material-based phase shifter is designed and implemented with the advantages of monolithic integration and reduction in power consumption.

[0027] In general, a voltage or current pulse changes the resistance of the chalcogenide material from a low-resistance (conductive) state to a high-resistance (non-conductive) state or vice-versa, depending on the energy level and duration of the pulse. Significantly, once the chalcogenide material is in one of the states, the chalcogenide material remains in that state, without needing further power to maintain or refresh the state, that is, there is no power consumption after reconfiguration. Such an ability to latch chalcogenide elements in a state is facilitated via a pulse code modulation-based phase shifter, which is employed in one example implementation described herein. Thus, it is straightforward to construct a single-pole, multi-throw switch with individually controllable chalcogenide material elements with "open" position(s) corresponding to the high-resistance state(s) and a closed position

corresponding to the low-resistance state, with only power consumed for changing the switch position.

[0028] Based on the individual phase shift values 112, the controller 114 controls a heater network 118 to change the resistances states of the chalcogenide elements, which in this implementation results in basically changing the "throw positions" of the switches formed with those chalcogenide elements. Note that only the chalcogenide elements that need changing need to be pulsed, e.g., if a switch is already in the correct position as a result of a previous phase shift scenario, which the controller 114 can evaluate with respect to the needed states corresponding to the just-received phase shift values, there is no need to pulse the chalcogenide elements that make up that particular switch.

[0029] FIGS. 2A and 2B shows the concept of a variable phase delay line element, in which the phase delay / corresponding phase shift (X° or Y°) is based on the length of the phase delay line element coupled to the conductive portion. Note however that FIGS. 2A and 2B are only conceptual representations for purposes of explanation, as the depicted example physical geometries do not actually change as might be suggested by the different line element lengths of FIGS. 2A and 2B; rather, the length of the variable phase delay line is determined by controlling the resultant "throw positions" of the chalcogenide-based switches by controlling the states of the chalcogenide material elements that are the components of those switches. Significantly, the sizes of the conductive portion need not change to obtain the desired phase shift.

[0030] Described herein is incorporating reconfigurability into the phase-delay elements, which is unlike prior solutions that avoid phase-delay elements because of prior lack of reconfigurability, (and instead use elements with variable size patches, despite their many drawbacks). Reconfigurability is accomplished as described herein by selecting among different lengths of phase delay elements using chalcogenide-based switches.

[0031] FIG. 3 shows a general concept related to the reconfigurability of a phase delay element, in which one selected path among different candidate paths with different transmission line lengths from a radio frequency (RF) input terminal to an RF output terminal is selected based on the desired phase shift, which corresponds to one of the transmission line path lengths and the phase delay resulting therefrom. As shown in FIG. 3, two switches 330 and 332 based on chalcogenide elements in controllable states (controlled via the heater network 118) are coupled to the RF input and to the RF output, respectively through one of the paths (Path1- Path*j*). In this example, the chalcogenide elements of the switches 330 and

332 (single-pole, *j*-throw, or SP*j*T where *j* represents the number of candidate paths from which to select) are in a low-resistance states with respect to coupling the RF input and RF output to Path2, and in high-resistance states with respect to the other candidate paths. Note that two such chalcogenide-based switches 330 and 332 are used at the start and end of any of the selectable paths, respectively, with respective matching counterpart chalcogenide element states, because in RF / microwave designs, the second switch 332 prevents the RF signal from flowing backwards, which would otherwise create standing waves and thus an impedance mismatch. Further, note that a single pole switch is employed at each end, because dividing the signal into two or more lines would cause an impedance mismatch as at the output, as part of the signal will arrive with intermodulation products (as an unwanted signal).

[0032] FIG. 4 generally shows a schematic of a loss-compensated 3-bit switched, two-stage phase shifter. In general, this example implementation provides a more practical implementation of switches and transmission lines (relative to FIG. 3), in which instead of selecting among each path individually, the lengths of two transmission line sub-path sections A and B can be additively combined to provide more phase shift candidate paths with fewer transmission lines. Further, although more chalcogenide-based switches are present than in FIG. 3, they have fewer chalcogenide elements, e.g., four single-pole triple-throw switches (SP3T) 441 - 444 are used in the example implementation of FIG. 4.

[0033] As can be seen in FIG. 4, the SP3T switches 441 - 444 are connected back-to-back, such that there are four switches and one common signal path port t_{0c}. The signal coming from the RF input is fed to the switch 441. If no delay is needed for this first sub-path A, the signal can be routed to the middle path section (the t_0 transmission line), otherwise the t_1 transmission line can be selected, which has a length / delay corresponding to 20 degrees of phase shift, or the t_2 transmission line can be selected which has a length / delay corresponding to 40 degrees of phase shift. Similarly, the next SP3T switch 442 is connected in reverse, such that the signal from any path / port (the second half of sub-path A) goes to the common signal path port t_{0c}.

[0034] The components of the second sub-path B are somewhat similar to those of sub-path A, except that the third switch 443 is connected to the common port t_{0c} and the fourth switch 444 is connected to the RF output terminal. Moreover, the available transmission line lengths include t_3 and t_4 (along with another instance of a reference / no delay t_0 transmission line), in

which the t_3 transmission line corresponds to 60 degrees of phase shift and the t_4 transmission line corresponds to 120 degrees of phase shift.

[0035] As can be seen, changing the four switches' chalcogenide element states to select among (e.g., "mix and match") the candidate path lengths / transmission lines results in a phase delay of one of: of 0, 20, 40, 60, 80, 100, 120, 140 or 160 degrees. For example, to configure 80 degrees of phase shift, the chalcogenide elements' states are changed (if necessary) such that the path from the RF input to the RF output is via transmission paths t_1 and t_3.

[0036] Note that for loss compensation, in one implementation the widths of the transmission lines increase with the length of the transmission line. This reduces the variation of the loss that would otherwise occur without different widths.

[0037] As can be readily appreciated, FIG. 4 shows only one example implementation. In a different implementation, if more fine-grained phase delay selections are needed, for example, more than two sub-path sections (e.g., with smaller differences in degree selections per path) can be present, and/or other than SP3T switches can be used, e.g., SP4T, SP5T and so on. The number of throw positions for the switch pairs of one sub-path section can be different from the number of throw positions for the switch pairs in a different sub-path section.

[0038] FIG. 5 shows how one implementation of a unit cell 550 can be constructed in accordance with the technology described herein, including with a first layer 552 containing the conductive portion (patch) 553 and a variable-length conductive phase-delay transmission line element 554. A ground layer 556 is a second layer, which is above a third layer that (on its underside) contains the PCM-based circuitry of the phase shifter 558. Vias 559 facilitate coupling of the RF input and output terminals (through the third layer 558, through the second (ground layer 556) and through the first layer 552) to complete a circuit in the variable-length conductive phase-delay transmission line element 554. In this way, the selected transmission lines of the phase shifter 558 conductively complete the circuit with the selected path length that determines the desired phase shift of the unit cell 550.

[0039] FIG. 6 shows additional details of one example phase shifter implementation 558. As can be seen, the longer transmission path lengths correspond to larger amounts of phase shift. As also can be seen, the longer the transmission path length, the wider the path width, for loss compensation mitigation. The control pads C1 – C12 couple the phase shifter to the

various other components described herein, including the heater network so that the PCM SPT3 switches (in this example) can be switched. Note that the chalcogenide elements of pairs of switches in each sub-path section can be controlled together using a shared pulse, and thus do not need individual control pads, although if shared in this way, the pulse energy (e.g., voltage) needs to be increased because such a shared pulse shares a path to two chalcogenide elements.

[0040] Numerical experiments were conducted to evaluate the performance between elements with variable size (as typically used), and elements with variable phase-delay line elements as described herein. FIG. 7 shows results of a variable element size simulation of the reflection magnitude with variable size element patches (graph plot 770) compared to the reflection magnitude of unit-cells embedded with phase-delay elements (graph plot 772). As demonstrated by the non-linear resulting curve in graph plot 770 versus the generally linear results in the graph plot 772, the phase profile of the elements with variable phase / time delay is significantly more linear that the prior variable patch size approach, with a larger range. This near-linearity means a reduction in phase range error and phase truncation error, and hence an increase in the reflective intelligent surface bandwidth.

[0041] FIG. 8 shows a comparison between magnitude plots 880 and 882, showing how the magnitude variation is reduced with the variable phase / time delay unit cells compared to variable patch size approaches. This means when applying phase-only synthesis during design, the surface with a uniform magnitude is better approximated, hence a reduction in design error. A comparison between geometry plots also demonstrates that geometry variation is less aggressive with variable phase / time delay unit cells compared to those with variable patch size, which means an improvement on the infinite array approximation, and therefore less design errors.

[0042] FIG. 9A and 9B show finite element method (FEM) simulated relative phase shifts and group delays, respectively, of a chalcogenide-based phase shifter over 25 - 34GHz band. The lines 771*p* – 779*p* of FIG. 9A and 771*d* – 779*d* represent different phase shifter states for the relative phase shifts and group delays, respectively.

[0043] In sum, described herein in general is providing reconfigurability to reflectarrays with phase-delay elements by the utilization of PCM-based mmWave phase shifters, instead of using elements with variable size. This phase-delay-based element technology brings several advantages, including that the use of phase-delay elements offers reduced phase truncation errors, reduced deviation from infinite array approximation, and reduced phase

range errors. At the same time, the use of PCM-based phase shifts offers the elimination of soldered components, fast switching, significant reduction in power consumption, area saving, and digital reconfigurability. By incorporating chalcogenide materials, the design process is simplified, reconfigurability is achieved, and the inherent benefits of using phase-delay lines are maintained.

[0044] One or more example embodiments can be embodied in a system, such as represented in the example operations of FIG. 10, and for example can include a memory that stores computer executable components and/or operations, and a processor that executes computer executable components and/or operations stored in the memory. Example operations can include operation 1002, which represents implementing a variable phase-shift unit cell, the variable phase-shift unit cell comprising a conductive metal portion electrically coupled to a variable-length conductive phase-delay transmission line element. Example operation 1004 represents controlling a phase shifter to change a phase shift of the variable phase-shift unit cell by switching among conductive and non-conductive states of chalcogenide material elements to vary a path length of the variable-length conductive phase-delay transmission line element, wherein the path length between a radio frequency (RF) input terminal and an RF output terminal determines the phase shift of the variable phase-shift unit cell.

[0045] At least two of the chalcogenide material elements can form a chalcogenide material-based single-pole, multiple throw switch.

[0046] The path length of the variable-length conductive phase-delay transmission line element can correspond to a selected conductive path, selected by the phase shifter from among a group of candidate conductive paths, by determining respective conductive or non-conductive states of respective chalcogenide material elements of the chalcogenide material elements. Respective candidate conductive paths can correspond to respective different phase shift amounts, and the respective candidate conductive paths can have respective different conductive path widths that correspond to the respective different phase shifts.

[0047] The phase shifter can include a pulse code modulation-based controller coupled to a heater network to individually determine the respective conductive or non-conductive states of the respective chalcogenide material elements. The phase shift can be a first phase shift, and the pulse code modulation-based controller phase can apply pulsed energy to latch the respective conductive or non-conductive states of the respective chalcogenide material

elements without applying further energy until the variable phase-shift unit cell is changed from the first phase shift to a second phase shift that is different from the first phase shift.

[0048] A subgroup of the chalcogenide material elements can be configured as a single-pole, multiple-throw switch, and controlling the phase shifter to change the phase shift can include switching among conductive and non-conductive states of the subgroup of the chalcogenide material elements to select the path length between the RF input terminal and the RF output terminal from among multiple different candidate path lengths corresponding to multiple switch positions of the multiple-throw switch. The subgroup can be a first subgroup configured as a first single-pole, multiple-throw switch at a beginning of the path length, a second subgroup of the chalcogenide material elements can be configured as a second single-pole, multiple-throw switch, and controlling the phase shifter to change the phase shift can include switching among conductive and non-conductive states of the second subgroup of the chalcogenide material elements to determine an end of the path length.

[0049] The candidate path lengths can include a first candidate path length that corresponds to a first amount of phase delay, a second candidate path length that corresponds to a second amount of phase delay, and a third candidate path length that corresponds to a reference phase delay; the first candidate path length, the second candidate path length, and the third candidate path length can be different from one another.

[0050] A first subgroup of the chalcogenide material elements can be configured as a first single-pole, multiple-throw switch, a second subgroup of the chalcogenide material elements can be configured as a second single-pole, multiple-throw switch, a third subgroup of the chalcogenide material elements can be configured as a third single-pole, multiple-throw switch, and a fourth subgroup of the chalcogenide material elements can be configured as a fourth single-pole, multiple-throw switch. Controlling of the phase shifter to change the phase shift can include switching among conductive and non-conductive states of the first subgroup and among conductive and non-conductive states of the second subgroup to select a first sub-path length from among multiple different candidate first sub-path lengths that correspond to multiple throw positions of the first single-pole, multiple-throw switch and multiple throw positions of the second single-pole, multiple-throw switch. Controlling of the phase shifter to change the phase shift can include switching among conductive and non-conductive states of the third subgroup and among conductive and non-conductive states of the fourth subgroup to select a second sub-path length from among multiple different candidate second sub-path lengths that correspond to multiple throw positions of the third

single-pole, multiple-throw switch, and multiple throw positions of the second single-pole, multiple-throw switch. An output terminal of the second single-pole, multiple-throw switch can be coupled to an input terminal of the third single-pole, multiple-throw switch to add the first sub-path length to the second sub-path length to determine the path length between the RF input terminal and the RF output terminal.

[0051] The variable phase-shift unit cell can be one unit cell of a group of unit cells that form a reconfigurable intelligent surface, and the phase shift of the unit cell can determine part of a beam reflected as a beam by the reconfigurable intelligent surface from an electromagnetic wave impinging on the reconfigurable intelligent surface. The group of unit cells can include respective unit cells comprising respective conductive metal portions; the respective conductive metal portions can be matching or substantially matching in size.

[0052] One or more example embodiments, such as corresponding to example operations of a method, are represented in FIG. 11. Example operation 1102 represents obtaining, by a system comprising a processor, a phase shift value for a unit cell. Example operation 1102 represents changing, by the system, a phase shift of the unit cell to match the phase shift value, comprising determining respective states of respective individual chalcogenide components of respective switches of the unit cell to vary a transmission line path length of a variable phase-delay line element, corresponding to a phase delay, from a first path length to a second path length.

[0053] Changing the respective states of the respective individual chalcogenide components can include controlling a controllable heater network that selectively transfers heat to at least some of the respective individual chalcogenide components.

[0054] The transmission line path length can correspond to a first sub-path length of the phase-delay line corresponding to a first amount of phase shift, and a second sub-path length of the phase-delay line corresponding to a second amount of phase shift. Changing the respective states of the respective chalcogenide components can include controlling at least some of the respective states to add the first sub-path length of the phase-delay line to the second sub-path length of the phase-delay line to vary the transmission line path length of the variable phase-delay line element.

[0055] The transmission line path length can include a first sub-path length plus a second sub-path length, and changing the respective states of the respective chalcogenide

components can include controlling at least some of the respective states to change the first sub-path length to a different first sub-path length.

[0056] One or more example embodiments can be embodied in a unit cell, such as described and represented herein. The unit cell can include a conductive patch, a phase delay element coupled to the conductive patch, and a phase shifter, the phase shifter including respective switches comprising respective chalcogenide material parts in respective low-resistance or high-resistance states, the phase shifter changing at least some of the respective low-resistance or high-resistance states of the respective chalcogenide material parts to select among available transmission paths that determine a length of the phase delay element, resulting in a phase shift of the unit cell with respect to redirecting an electromagnetic wave impinging on the unit cell.

[0057] The phase shifter can include a pulse code modulation-based controller that controls a heater network for changing the at least some of the respective low-resistance or high-resistance states of the respective chalcogenide material parts.

[0058] The length of the phase delay element can include a first sub-path length determined by the phase shifter, and a second sub-path length determined by the phase shifter.

[0059] The unit cell can be one unit cell of a group of unit cells that form a reconfigurable intelligent surface, and the phase shift of the unit cell can determine part of a beam reflected by the reconfigurable intelligent surface based on an electromagnetic wave impinging on the unit cell.

[0060] As can be seen, the technology described herein provides a unit cell with a variable phase change element that overcomes many of the issues with variable element patch size solutions. The phase-delay unit-cells described herein enable a linear phase profile across the array, which is highly desirable as it allows for precise control and manipulation of the electromagnetic wavefront across the array, leading to improved beamforming and beam-steering capabilities. The phase-delay unit-cells described herein offer improved bandwidth compared to variable-size unit-cells, because the linearity of the phase profile enables a wider range of phase shifts, allowing for broader frequency coverage and enhanced performance across a larger bandwidth. The use of phase-delay unit-cells reduces the sensitivity to fabrication imperfections, which reduces the error and fabrication cost; phase-delay unit-cells rely on accurate phase control, which is typically easier to achieve in fabrication. Phase-delay unit-cells can achieve better impedance matching, resulting in reduced power losses

and improved overall efficiency of the reconfigurable intelligent surface. Phase-delay unit-cells offer a more uniform distribution of losses throughout the reconfigurable intelligent surface; (in contrast, with variable-size unit-cells, the non-uniformity of element sizes leads to non-uniform power distribution and uneven losses across the array, causing performance degradation). With phase-delay unit-cells as described herein, the power distribution is more balanced, resulting in improved performance consistency.

[0061] Further, phase-delay unit-cells help mitigate the infinite array approximation violation by maintaining a more consistent and regular array structure, improving the applicability of theoretical models and simplifying system design. This is due to less geometrical structure being changed across unit-cells. As a result, the technology described herein provides significant prospects in enhancing the performance and efficiency of reconfigurable intelligent surface technology in mmWave/6G applications.

[0062] The above description of illustrated embodiments of the subject disclosure, comprising what is described in the Abstract, is not intended to be exhaustive or to limit the disclosed embodiments to the precise forms disclosed. While specific embodiments and examples are described herein for illustrative purposes, various modifications are possible that are considered within the scope of such embodiments and examples, as those skilled in the relevant art can recognize.

[0063] In this regard, while the disclosed subject matter has been described in connection with various embodiments and corresponding Figures, where applicable, it is to be understood that other similar embodiments can be used or modifications and additions can be made to the described embodiments for performing the same, similar, alternative, or substitute function of the disclosed subject matter without deviating therefrom. Therefore, the disclosed subject matter should not be limited to any single embodiment described herein, but rather should be construed in breadth and scope in accordance with the appended claims below.

[0064] As it employed in the subject specification, the term “processor” can refer to substantially any computing processing unit or device comprising, but not limited to comprising, single-core processors; single-processors with software multithread execution capability; multi-core processors; multi-core processors with software multithread execution capability; multi-core processors with hardware multithread technology; parallel platforms; and parallel platforms with distributed shared memory. Additionally, a processor can refer to an integrated circuit, an application specific integrated circuit, a digital signal processor, a

field programmable gate array, a programmable logic controller, a complex programmable logic device, a discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. Processors can exploit nano-scale architectures such as, but not limited to, molecular and quantum-dot based transistors, switches and gates, in order to optimize space usage or enhance performance of user equipment. A processor may also be implemented as a combination of computing processing units.

[0065] As used in this application, the terms "component," "system," "platform," "layer," "selector," "interface," and the like are intended to refer to a computer-related resource or an entity related to an operational apparatus with one or more specific functionalities, wherein the entity can be either hardware, a combination of hardware and software, software, or software in execution. As an example, a component may be, but is not limited to being, a process running on a processor, a processor, an object, an executable, a thread of execution, a program, and/or a computer. By way of illustration and not limitation, both an application running on a server and the server can be a component. One or more components may reside within a process and/or thread of execution and a component may be localized on one computer and/or distributed between two or more computers. In addition, these components can execute from various computer readable media having various data structures stored thereon. The components may communicate via local and/or remote processes such as in accordance with a signal having one or more data packets (e.g., data from one component interacting with another component in a local system, distributed system, and/or across a network such as the Internet with other systems via the signal). As another example, a component can be an apparatus with specific functionality provided by mechanical parts operated by electric or electronic circuitry, which is operated by a software or a firmware application executed by a processor, wherein the processor can be internal or external to the apparatus and executes at least a part of the software or firmware application. As yet another example, a component can be an apparatus that provides specific functionality through electronic components without mechanical parts, the electronic components can comprise a processor therein to execute software or firmware that confers at least in part the functionality of the electronic components.

[0066] In addition, the term "or" is intended to mean an inclusive "or" rather than an exclusive "or." That is, unless specified otherwise, or clear from context, "X employs A or B" is intended to mean any of the natural inclusive permutations. That is, if X employs A; X

employs B; or X employs both A and B, then "X employs A or B" is satisfied under any of the foregoing instances.

[0067] While the embodiments are susceptible to various modifications and alternative constructions, certain illustrated implementations thereof are shown in the drawings and have been described above in detail. It should be understood, however, that there is no intention to limit the various embodiments to the specific forms disclosed, but on the contrary, the intention is to cover all modifications, alternative constructions, and equivalents falling within the spirit and scope.

[0068] In addition to the various implementations described herein, it is to be understood that other similar implementations can be used or modifications and additions can be made to the described implementation(s) for performing the same or equivalent function of the corresponding implementation(s) without deviating therefrom. Still further, multiple processing chips or multiple devices can share the performance of one or more functions described herein, and similarly, storage can be effected across a plurality of devices. Accordingly, the various embodiments are not to be limited to any single implementation, but rather are to be construed in breadth, spirit and scope in accordance with the appended claims.

WHAT IS CLAIMED IS:

1. A system, comprising:

a processor; and

a memory that stores executable instructions that, when executed by the processor, facilitate performance of operations, the operations comprising:

implementing a variable phase-shift unit cell, the variable phase-shift unit cell comprising a conductive metal portion electrically coupled to a variable-length conductive phase-delay transmission line element; and

controlling a phase shifter to change a phase shift of the variable phase-shift unit cell by switching among conductive and non-conductive states of chalcogenide material elements to vary a path length of the variable-length conductive phase-delay transmission line element, wherein the path length between a radio frequency (RF) input terminal and an RF output terminal determines the phase shift of the variable phase-shift unit cell.

2. The system of claim 1, wherein at least two of the chalcogenide material elements comprise a chalcogenide material-based single-pole, multiple throw switch.

3. The system of claim 1, wherein the path length of the variable-length conductive phase-delay transmission line element corresponds to a selected conductive path, selected by the phase shifter from among a group of candidate conductive paths, by determining respective conductive or non-conductive states of respective chalcogenide material elements of the chalcogenide material elements.

4. The system of claim 3, wherein respective candidate conductive paths correspond to respective different phase shift amounts, and wherein the respective candidate conductive paths have respective different conductive path widths that correspond to the respective different phase shifts.

5. The system of claim 3, wherein the phase shifter comprises a pulse code modulation-based controller coupled to a heater network to individually determine the respective conductive or non-conductive states of the respective chalcogenide material elements.

6. The system of claim 5, wherein the phase shift is a first phase shift, and wherein the pulse code modulation-based controller phase applies pulsed energy to latch the respective conductive or non-conductive states of the respective chalcogenide material elements without applying further energy until the variable phase-shift unit cell is changed from the first phase shift to a second phase shift that is different from the first phase shift.

7. The system of claim 1, wherein a subgroup of the chalcogenide material elements is configured as a single-pole, multiple-throw switch, and wherein the controlling of the phase shifter to change the phase shift comprises switching among conductive and non-conductive states of the subgroup of the chalcogenide material elements to select the path length between the RF input terminal and the RF output terminal from among multiple different candidate path lengths corresponding to multiple switch positions of the multiple-throw switch.

8. The system of claim 7, wherein the subgroup is a first subgroup configured as a first single-pole, multiple-throw switch at a beginning of the path length, wherein a second subgroup of the chalcogenide material elements is configured as a second single-pole, multiple-throw switch, and wherein the controlling of the phase shifter to change the phase shift comprises switching among conductive and non-conductive states of the second subgroup of the chalcogenide material elements to determine an end of the path length.

9. The system of claim 7, wherein the candidate path lengths comprise a first candidate path length that corresponds to a first amount of phase delay, a second candidate path length that corresponds to a second amount of phase delay, and a third candidate path length that corresponds to a reference phase delay, and wherein the first candidate path length, the second candidate path length, and the third candidate path length are different from one another.

10. The system of claim 1, wherein a first subgroup of the chalcogenide material elements is configured as a first single-pole, multiple-throw switch, wherein a second subgroup of the chalcogenide material elements is configured as a second single-pole, multiple-throw switch, wherein a third subgroup of the chalcogenide material elements is configured as a third single-pole, multiple-throw switch, and wherein a fourth subgroup of the chalcogenide material elements is configured as a fourth single-pole, multiple-throw switch,

wherein the controlling of the phase shifter to change the phase shift comprises:

switching among conductive and non-conductive states of the first subgroup and among conductive and non-conductive states of the second subgroup to select a first sub-path length from among multiple different candidate first sub-path lengths that correspond to multiple throw positions of the first single-pole, multiple-throw switch and multiple throw positions of the second single-pole, multiple-throw switch; and

switching among conductive and non-conductive states of the third subgroup and among conductive and non-conductive states of the fourth subgroup to select a second sub-path length from among multiple different candidate second sub-path lengths that correspond to multiple throw positions of the third single-pole, multiple-throw switch, and multiple throw positions of the second single-pole, multiple-throw switch, and

wherein an output terminal of the second single-pole, multiple-throw switch is coupled to an input terminal of the third single-pole, multiple-throw switch to add the first sub-path length to the second sub-path length to determine the path length between the RF input terminal and the RF output terminal.

11. The system of claim 1, wherein the variable phase-shift unit cell is one unit cell of a group of unit cells that form a reconfigurable intelligent surface, and wherein the phase shift of the unit cell determines part of a beam reflected as a beam by the reconfigurable intelligent surface from an electromagnetic wave impinging on the reconfigurable intelligent surface.

12. The system of claim 11, wherein the group of unit cells comprise respective unit cells comprising respective conductive metal portions, and wherein the respective conductive metal portions are matching or substantially matching in size.

13. A method, comprising:

obtaining, by a system comprising a processor, a phase shift value for a unit cell; and

changing, by the system, a phase shift of the unit cell to match the phase shift value, comprising determining respective states of respective individual chalcogenide components of respective switches of the unit cell to vary a transmission line path length of a variable phase-delay line element, corresponding to a phase delay, from a first path length to a second path length.

14. The method of claim 13, wherein the changing of the respective states of the respective individual chalcogenide components comprises controlling a controllable heater network that selectively transfers heat to at least some of the respective individual chalcogenide components.

15. The method of claim 13, wherein the transmission line path length corresponds to a first sub-path length of the phase-delay line corresponding to a first amount of phase shift, and a second sub-path length of the phase-delay line corresponding to a second amount of phase shift, and wherein the changing of the respective states of the respective chalcogenide components comprises controlling at least some of the respective states to add the first sub-path length of the phase-delay line to the second sub-path length of the phase-delay line to vary the transmission line path length of the variable phase-delay line element.

16. The method of claim 13, wherein the transmission line path length comprises a first sub-path length plus a second sub-path length, and wherein the changing of the respective states of the respective chalcogenide components comprises controlling at least some of the respective states to change the first sub-path length to a different first sub-path length.

17. A unit cell, comprising:

a conductive patch;

a phase delay element coupled to the conductive patch; and

a phase shifter, the phase shifter comprising respective switches comprising respective chalcogenide material parts in respective low-resistance or high-resistance states, the phase shifter changing at least some of the respective low-resistance or high-resistance states of the respective chalcogenide material parts to select among available transmission paths that determine a length of the phase delay element, resulting in a phase shift of the unit cell with respect to redirecting an electromagnetic wave impinging on the unit cell.

18. The unit cell of claim 17, wherein the phase shifter comprises a pulse code modulation-based controller that controls a heater network for changing the at least some of the respective low-resistance or high-resistance states of the respective chalcogenide material parts.

19. The unit cell of claim 17, wherein the length of the phase delay element comprises a first sub-path length determined by the phase shifter, and a second sub-path length determined by the phase shifter.

20. The unit cell of claim 17, wherein the unit cell is one unit cell of a group of unit cells that form a reconfigurable intelligent surface, and wherein the phase shift of the unit cell determines part of a beam reflected by the reconfigurable intelligent surface based on an electromagnetic wave impinging on the unit cell.

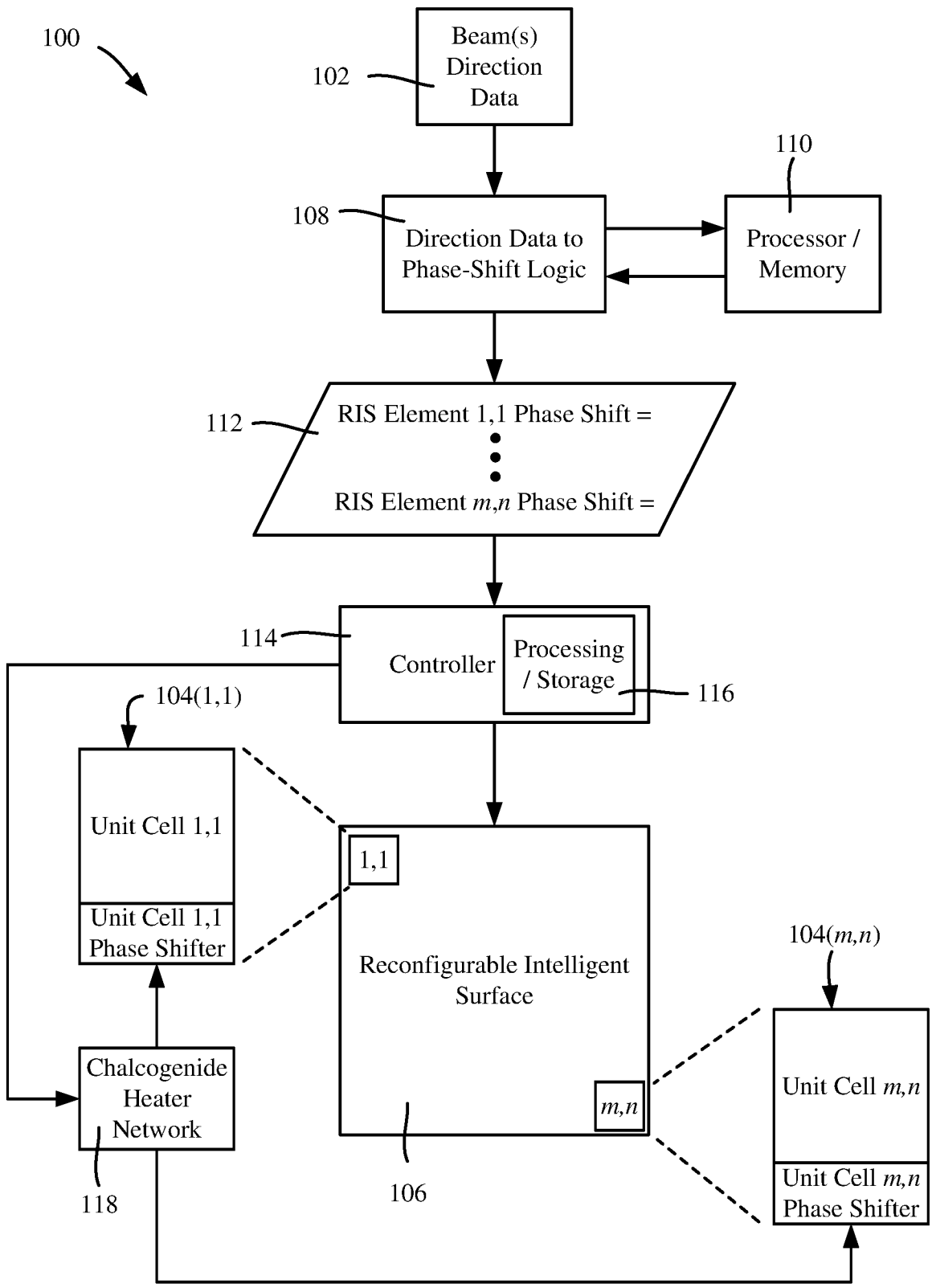

100
Beam(s) Direction Data
102
110
108
Direction Data to Phase-Shift Logic
Processor / Memory
112
RIS Element 1,1 Phase Shift =
RIS Element m,n Phase Shift =
114
Controller
Processing / Storage
116
104(1,1)
Unit Cell 1,1
Unit Cell 1,1 Phase Shifter
1,1
Reconfigurable Intelligent Surface
104(m,n)
Unit Cell m,n
Unit Cell m,n Phase Shifter
m,n
Chalcogenide Heater Network
118
106

FIG. 1

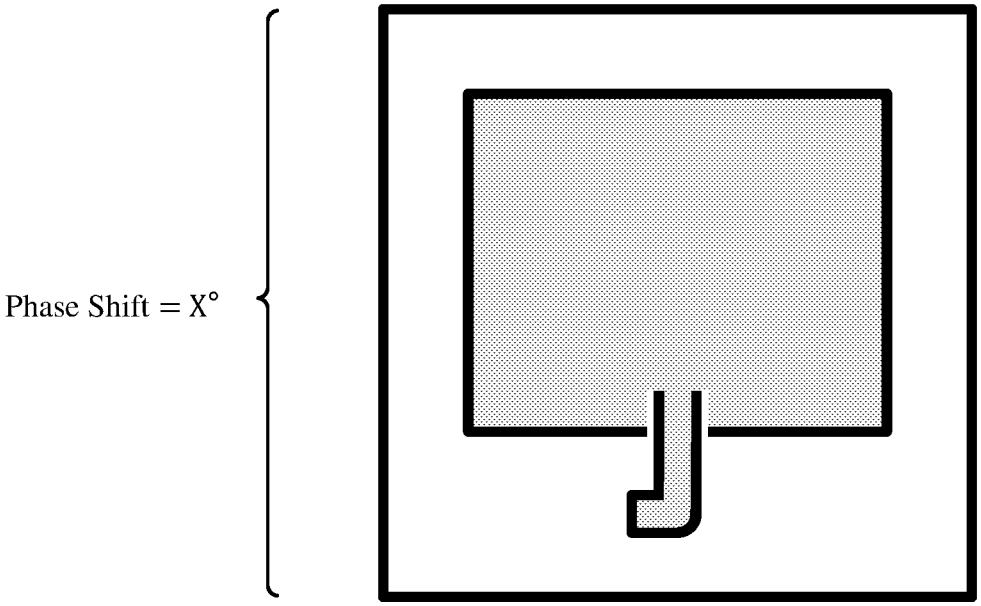


FIG. 2A

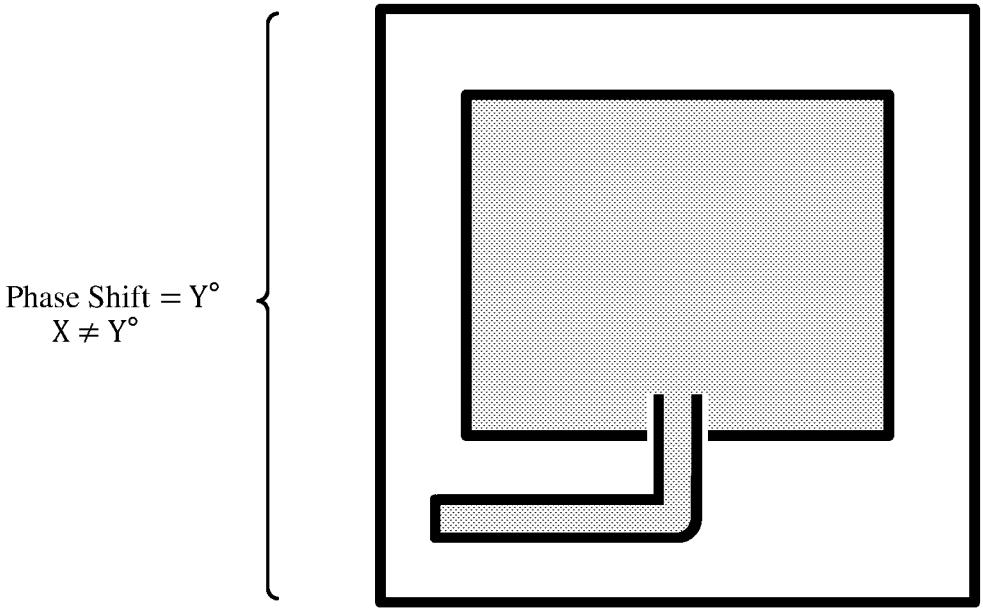


FIG. 2B

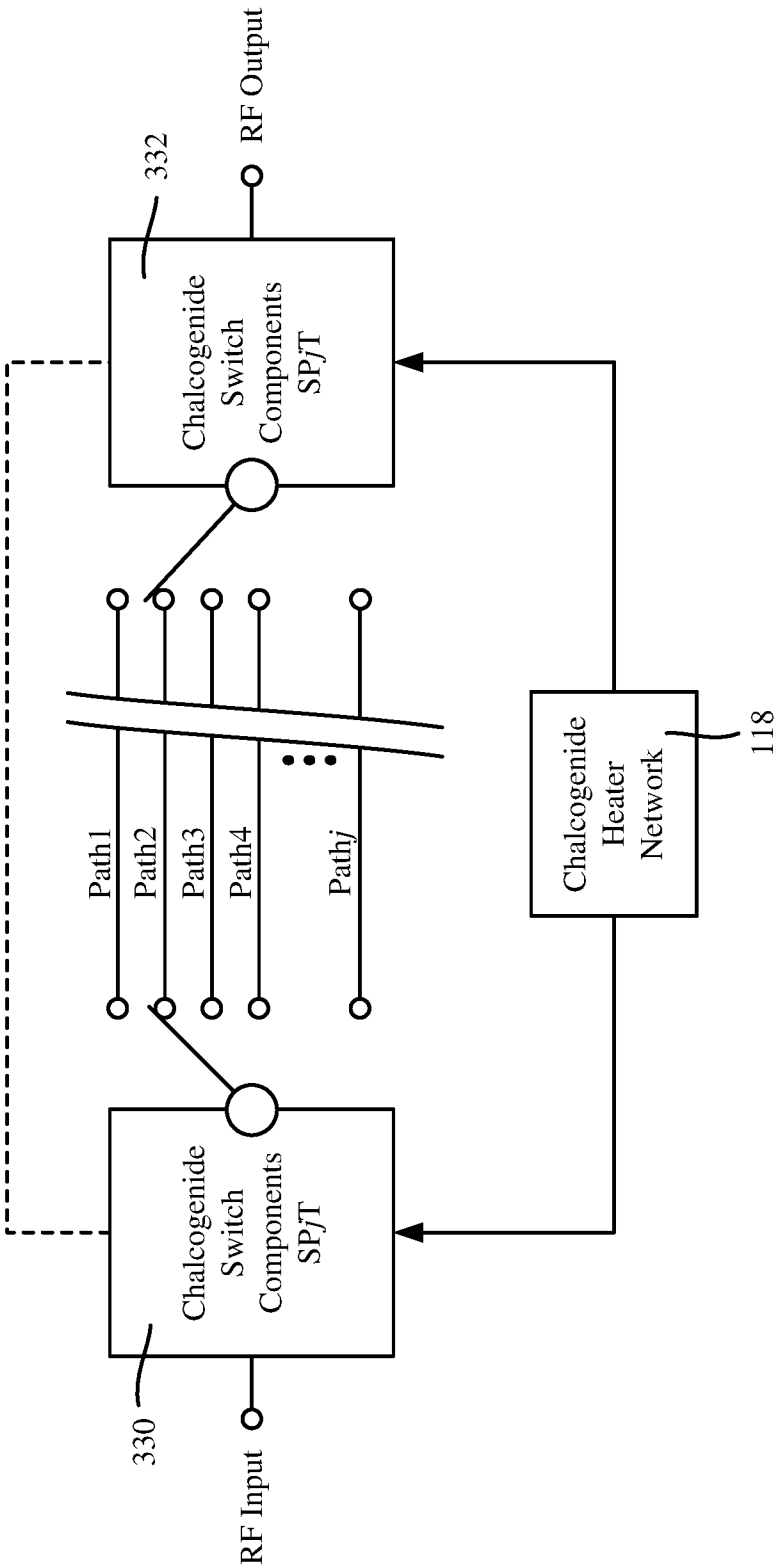

RF Output
332
Chalcogenide Switch Components SPjT
Path1
Path2
Path3
Path4
Pathj
Chalcogenide Heater Network
118
Chalcogenide Switch Components SPjT
330
RF Input

FIG. 3

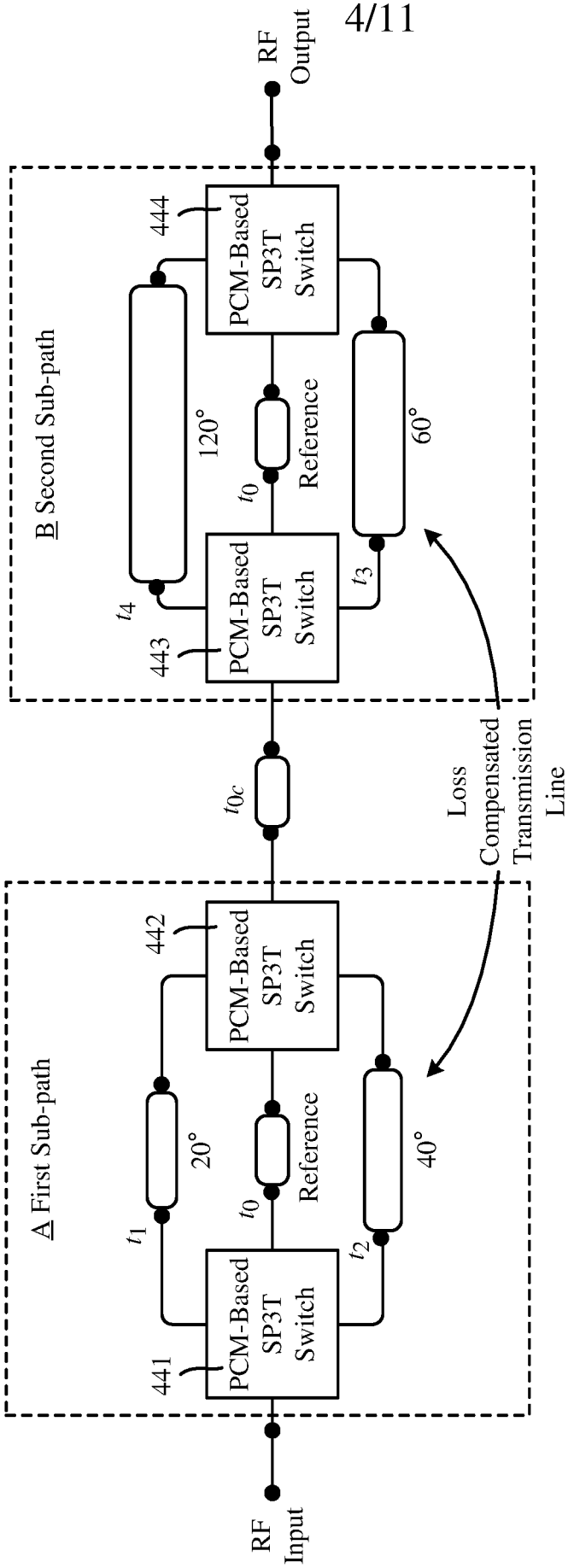

RF Output
B Second Sub-path
444
PCM-Based SP3T Switch
120°
t_0
Reference
60°
t_4
443
PCM-Based SP3T Switch
t_3
t_{0c}
Loss Compensated Transmission Line
A First Sub-path
442
PCM-Based SP3T Switch
20°
t_1
t_0
Reference
40°
t_2
441
PCM-Based SP3T Switch
RF Input

FIG. 4

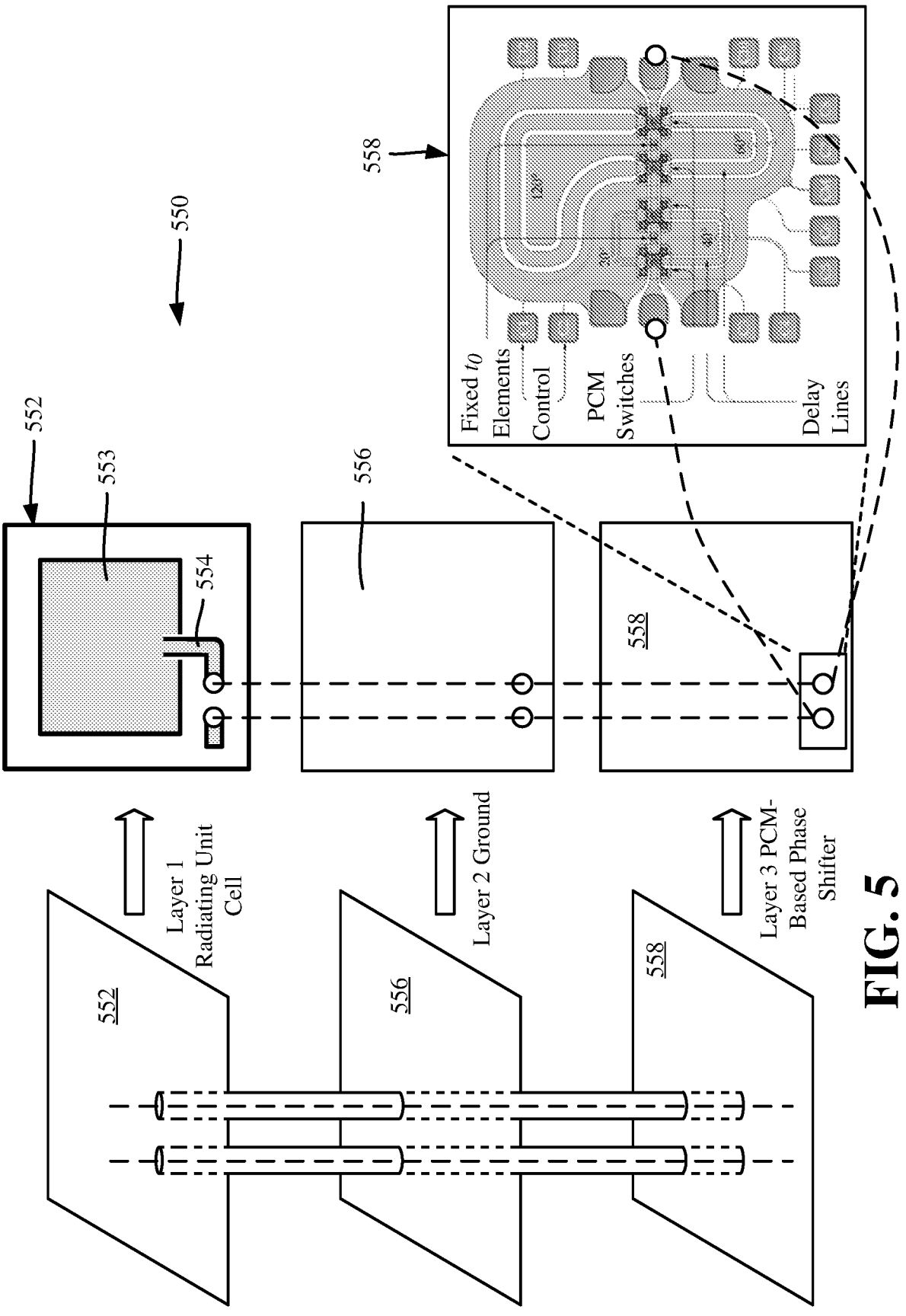

550
552
553
554
556
558
Fixed t_0 Elements
Control
PCM Switches
Delay Lines
Layer 1 Radiating Unit Cell
Layer 2 Ground
Layer 3 PCM-Based Phase Shifter

FIG. 5

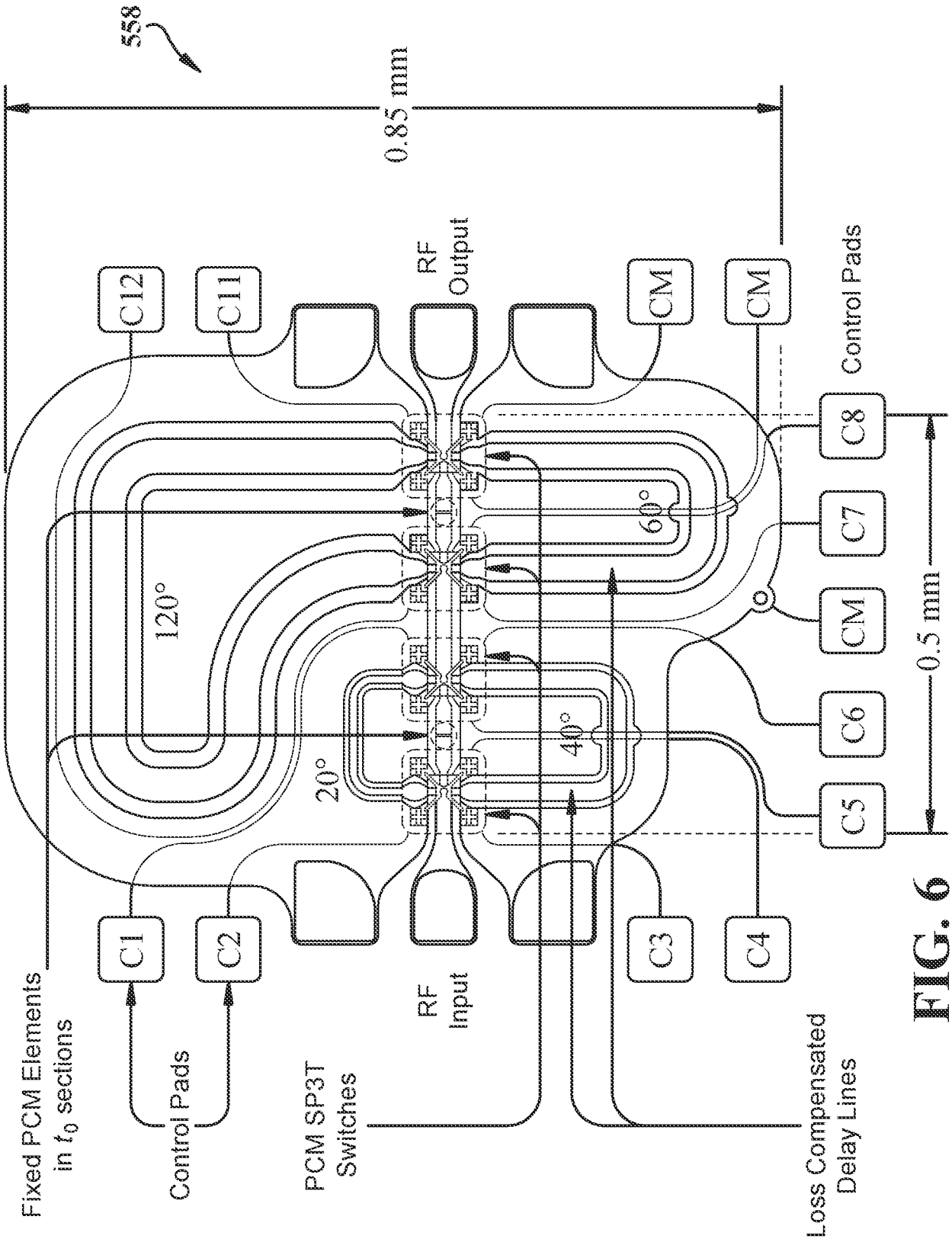

558
0.85 mm
C12
C11
RF Output
CM
CM
Control Pads
C8
C7
CM
C6
C5
0.5 mm
60°
120°
40°
20°
C1
C2
C3
C4
RF Input
Fixed PCM Elements in t_0 sections
Control Pads
PCM SP3T Switches
Loss Compensated Delay Lines

FIG. 6

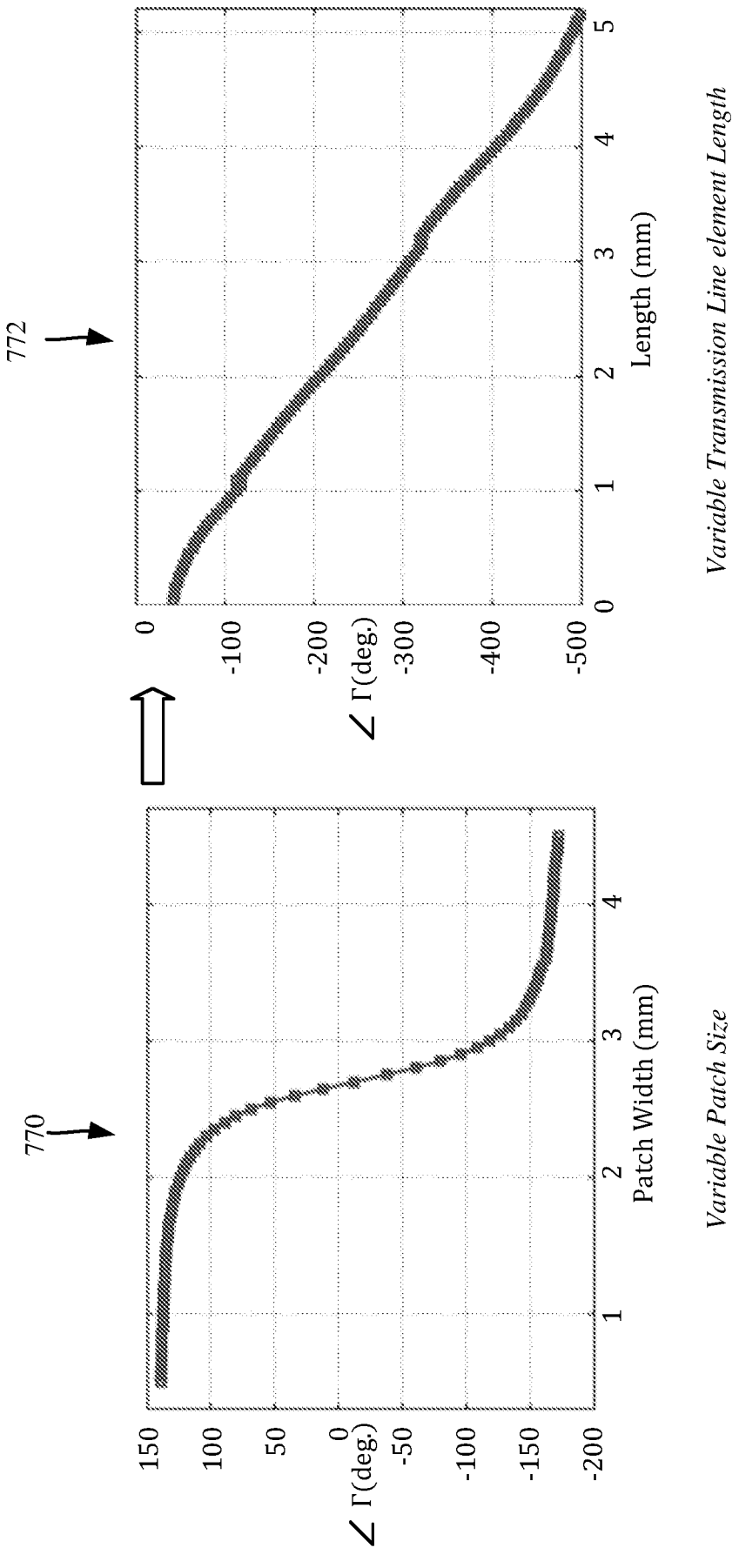

772
0
-100
-200
-300
-400
-500
∠ Γ(deg.)
0
1
2
3
4
5
Length (mm)
Variable Transmission Line element Length
770
150
100
50
0
-50
-100
-150
-200
∠ Γ(deg.)
1
2
3
4
Patch Width (mm)
Variable Patch Size

FIG. 7

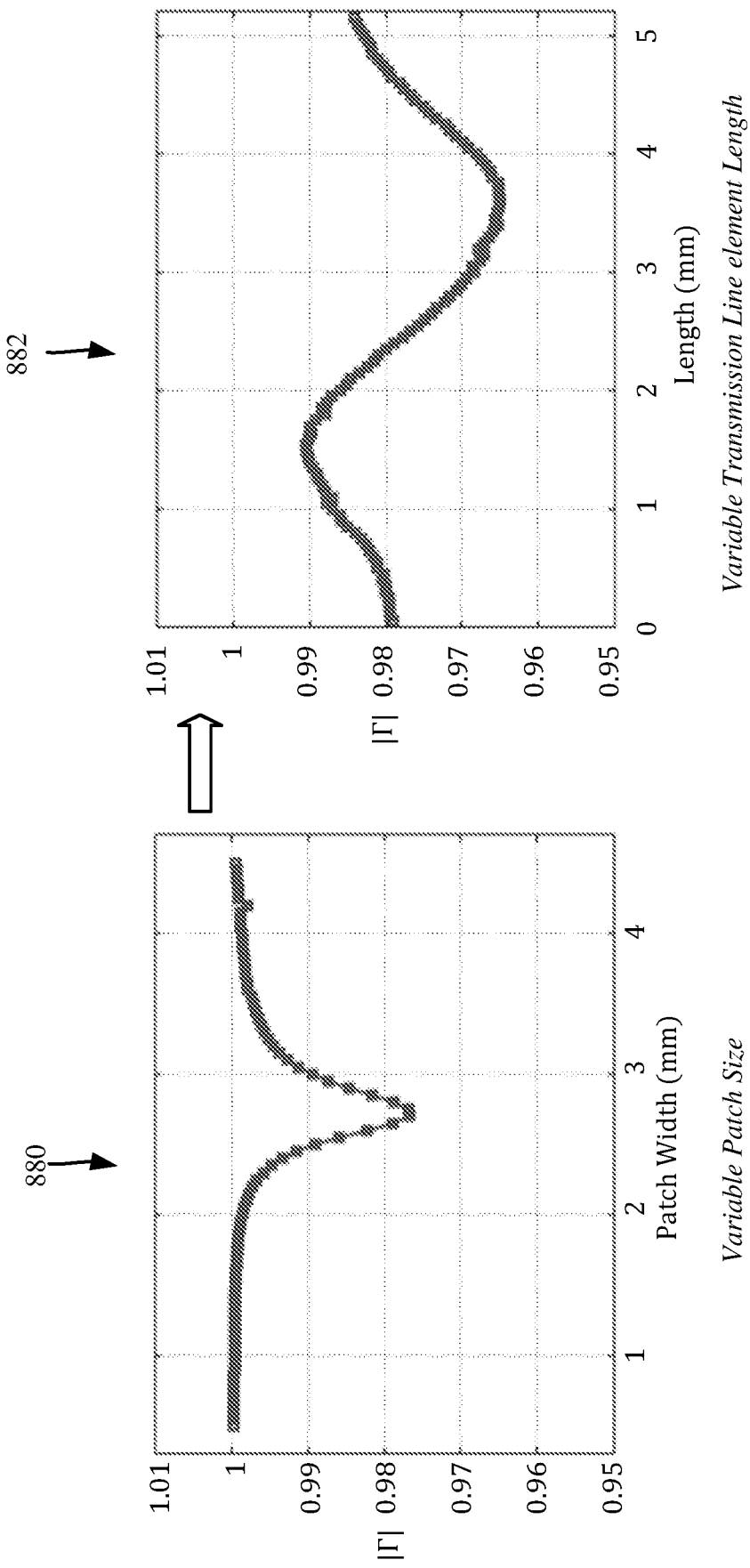

880
882
|Γ|
1.01
1
0.99
0.98
0.97
0.96
0.95
1
2
3
4
Patch Width (mm)
Variable Patch Size
0
1
2
3
4
5
Length (mm)
Variable Transmission Line element Length

FIG. 8

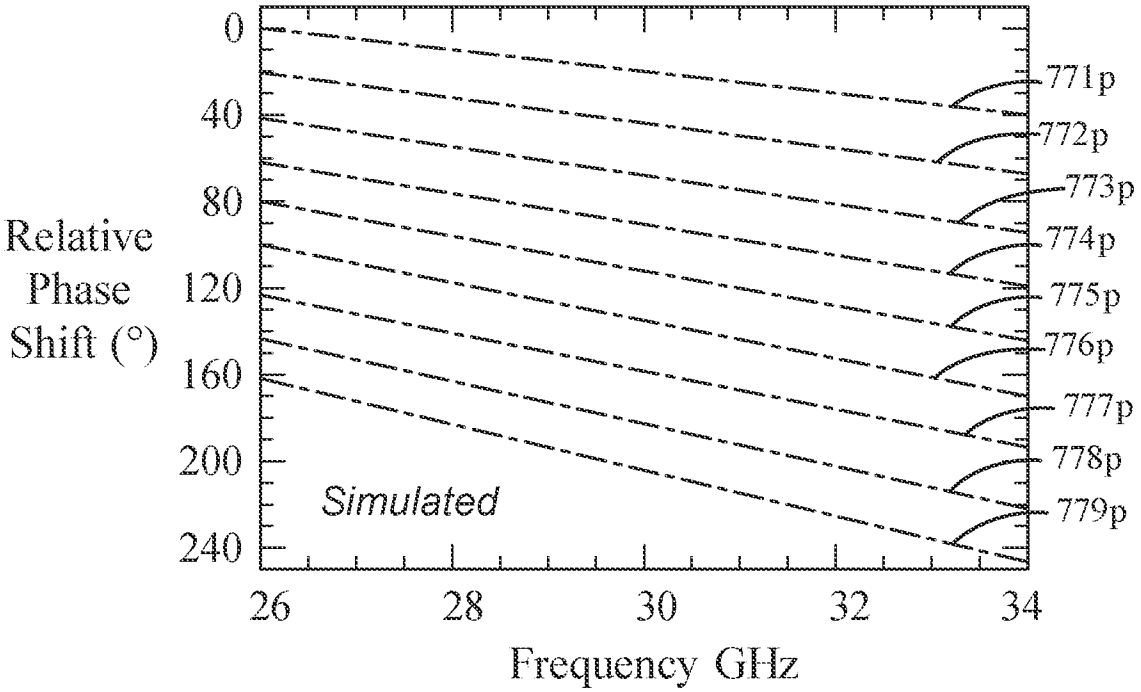

Relative Phase Shift (°)
0
40
80
120
160
200
240
Simulated
771p
772p
773p
774p
775p
776p
777p
778p
779p
26
28
30
32
34
Frequency GHz

FIG. 9A

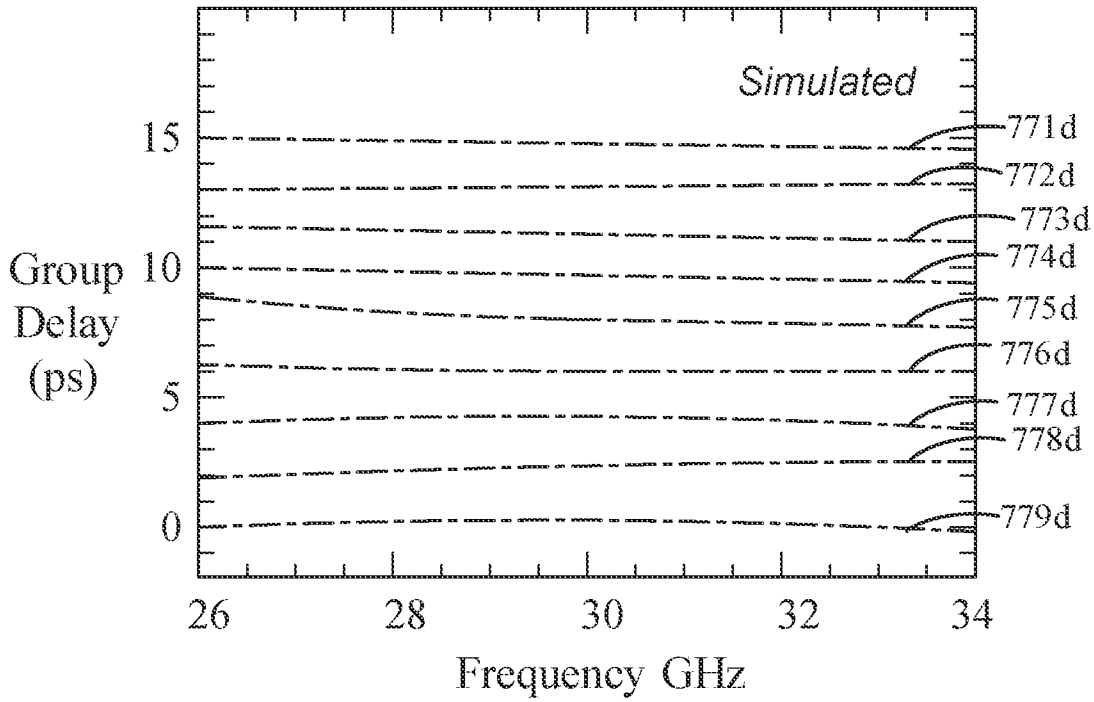

Group Delay (ps)
15
10
5
0
Simulated
771d
772d
773d
774d
775d
776d
777d
778d
779d
26
28
30
32
34
Frequency GHz

FIG. 9B

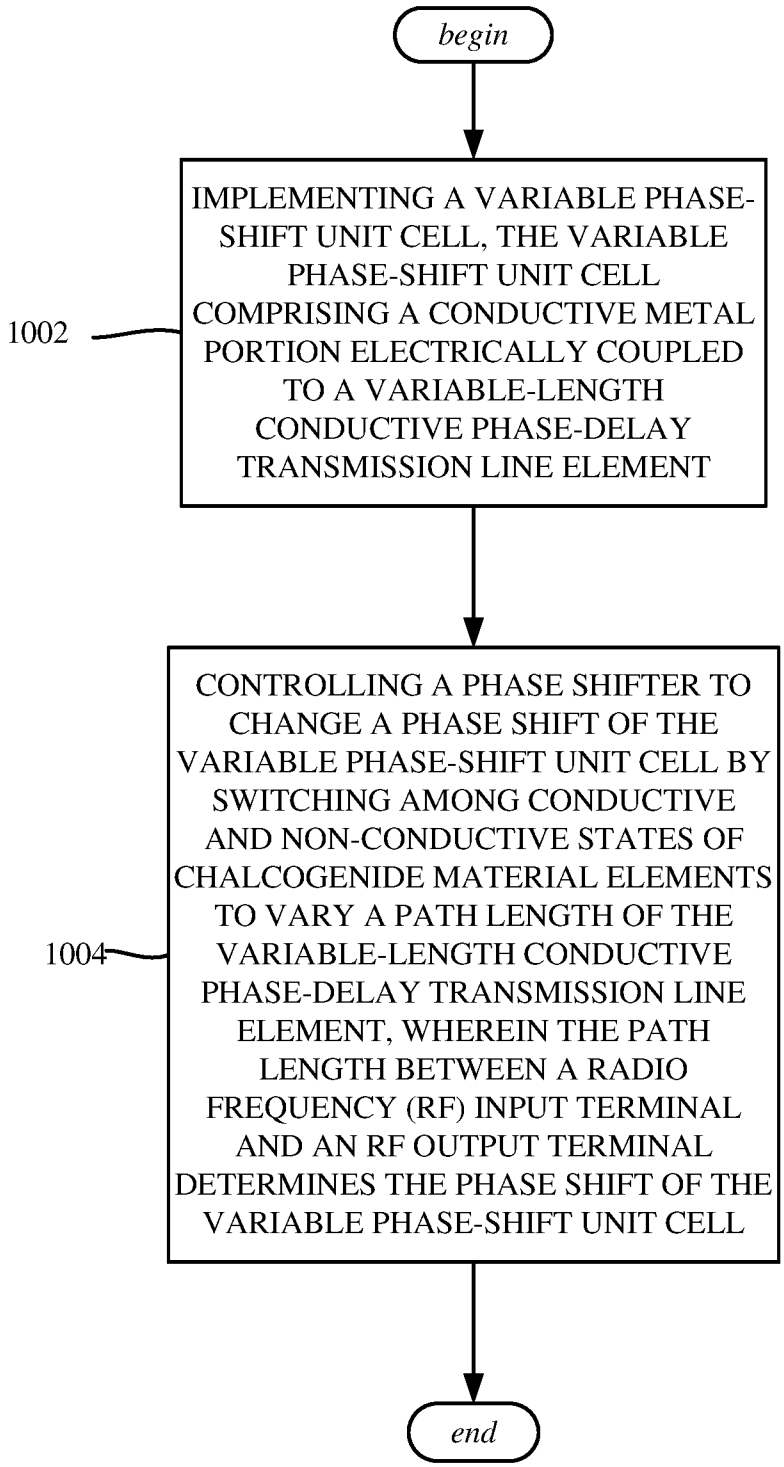

begin
IMPLEMENTING A VARIABLE PHASE-SHIFT UNIT CELL, THE VARIABLE PHASE-SHIFT UNIT CELL COMPRISING A CONDUCTIVE METAL PORTION ELECTRICALLY COUPLED TO A VARIABLE-LENGTH CONDUCTIVE PHASE-DELAY TRANSMISSION LINE ELEMENT
1002
CONTROLLING A PHASE SHIFTER TO CHANGE A PHASE SHIFT OF THE VARIABLE PHASE-SHIFT UNIT CELL BY SWITCHING AMONG CONDUCTIVE AND NON-CONDUCTIVE STATES OF CHALCOGENIDE MATERIAL ELEMENTS TO VARY A PATH LENGTH OF THE VARIABLE-LENGTH CONDUCTIVE PHASE-DELAY TRANSMISSION LINE ELEMENT, WHEREIN THE PATH LENGTH BETWEEN A RADIO FREQUENCY (RF) INPUT TERMINAL AND AN RF OUTPUT TERMINAL DETERMINES THE PHASE SHIFT OF THE VARIABLE PHASE-SHIFT UNIT CELL
1004
end

FIG. 10

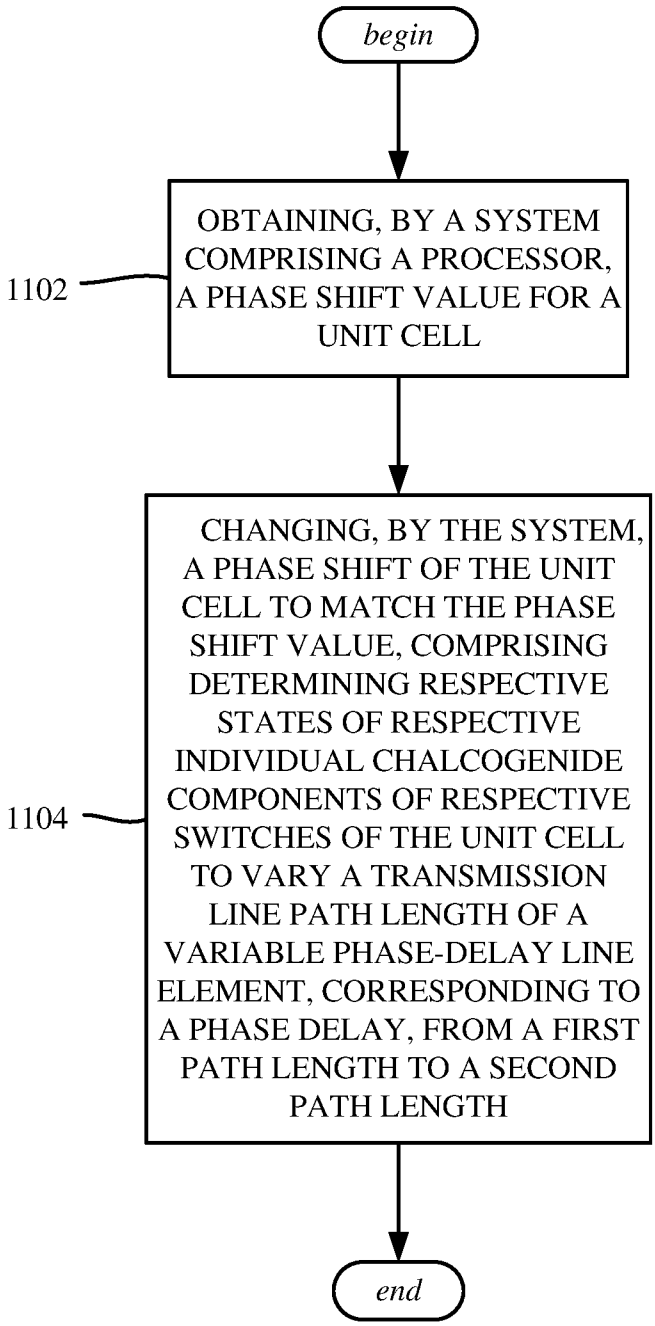

begin
OBTAINING, BY A SYSTEM COMPRISING A PROCESSOR, A PHASE SHIFT VALUE FOR A UNIT CELL
1102
CHANGING, BY THE SYSTEM, A PHASE SHIFT OF THE UNIT CELL TO MATCH THE PHASE SHIFT VALUE, COMPRISING DETERMINING RESPECTIVE STATES OF RESPECTIVE INDIVIDUAL CHALCOGENIDE COMPONENTS OF RESPECTIVE SWITCHES OF THE UNIT CELL TO VARY A TRANSMISSION LINE PATH LENGTH OF A VARIABLE PHASE-DELAY LINE ELEMENT, CORRESPONDING TO A PHASE DELAY, FROM A FIRST PATH LENGTH TO A SECOND PATH LENGTH
1104
end

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2024/013725

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01P1/18 H01Q3/46 H01Q15/00 H01P1/15
ADD. H10N79/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01P H01Q H10N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	RODRIGUES DAVI V Q ET AL: "Optimized phase shifts in intelligent reflective surfaces for robust radar-based indoor coverage enhancement", 20230614, vol. 12535, 14 June 2023 (2023-06-14), pages 1253508-1253508, XP060183796, ISSN: 0277-786X, DOI: 10.1117/12.2662926 ISBN: 978-1-5106-6184-4 chapters 1-3; figures 1, 4, 6 -----	1-7,9, 11-15, 17-20
Y	WO 2023/147891 A1 (NEC LABORATORIES EUROPE GMBH [DE]) 10 August 2023 (2023-08-10) pages 1, 7 - page 11; figure 4 ----- -/--	1-7,9, 11-15, 17-20

[x] Further documents are listed in the continuation of Box C.

[x] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 September 2024	27/09/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hueso González, J

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2024/013725

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SINGH TEJINDER ET AL: "Recent Advancements in Reconfigurable mmWave Devices Based on Phase-Change and Metal Insulator Transition Materials", IEEE JOURNAL OF MICROWAVES, [Online] vol. 3, no. 2, 7 April 2023 (2023-04-07), pages 827-851, XP093204773, ISSN: 2692-8388, DOI: 10.1109/JMW.2023.3247360 Retrieved from the Internet: URL:https://ieeexplore.ieee.org/ielx7/9171629/10091703/10075653.pdf?tp=&arnumber=10075653&isnumber=10091703&ref=aHR0cHM6Ly9pZWVleHBsb3JlLmllZWUub3JnL2RvY3VtZW50LzEwMDc1NjUz> [retrieved on 2024-09-16] chapters I, III and III.G.2; figures 2, 24	1-10, 13-19

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