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(54) Title: NON-VOLATILE OPTO-ELECTRONIC DEVICE

(57) Abstract: The present invention relates to an opto-electronic switch/memory device utilizing thin layer of exfoliated graphene laid upon monolayer or multilayer of MoS₂, forming a hetero-hybrid structure. The specific architecture of the device is planar, which can be made by laying a continuous sheet of graphene on a continuous sheet of MoS₂ (graphene-on-MoS₂) and electrode contacts are placed only on graphene layer forming an in-plane geometry.



WO 2014/178016 A2

NON-VOLATILE OPTO-ELECTRONIC DEVICE

FIELD OF THE INVENTION

[0001] Present disclosure relates to fabrication and development in non-volatile memory devices based on hybrid inorganic/organic nano-composites and also switching and carrier transport mechanisms in the hybrid non-volatile memory devices. More preferably, the present disclosure relates to an opto-electronic device and implementation of a method to induce optoelectronic functionality into graphene by hybridizing it with light sensitive membranes of MoS₂.

BACKGROUND OF THE INVENTION

[0002] Implementation of atomically thin membranes for new functionality is a rapidly developing field. Among the emerging class of materials, graphene is one of the most common and extensively researched for a variety of electrical applications. Unfortunately, graphene responds very weakly to light, being nearly 98% transparent to visible spectrum of radiation. There have been reports of semiconductor nano particle-graphene hybrids that enhance photo-conductivity of graphene by eight orders of magnitude, approaching the level of single photon detection. There are however many technical challenges such as gate tunability, speed of operation, among others that need to be met.

[0003] Graphene is an attractive material for optoelectronics and photo-detection applications as it offers a broad spectral bandwidth and fast response times. At the same time, disadvantages such as weak light absorption, and absence of a gain mechanism that can generate multiple charge carriers from one incident photon, have limited the sensitivity of graphene-based photo-detectors. However, even in view of the above disadvantages, devices with specific pulse detection need to be developed, which devices can then benefit from gate-tunable sensitivity and speed, spectral selectivity from short-wavelength infrared to visible range, and which devices can be compatible with current circuit technologies. In this respect, graphene has unexpectedly led to a new world of unique opto-electronic properties that are not encountered in standard electronic materials owing to properties such as high optical transparency, high quality (large mobility) electrical characteristics with gate tunability, thinness, and flexibility.

[0004] Hybrid heterostructures of atomically thin membranes from layered materials promise devices that combine advantages of ultimate miniaturization and multiple

functionalities in modern electronic and photonic devices such as high mobility transistors, solid state lasers, light emitting devices, and solar cells. For instance, paper titled “Graphene and boron nitride lateral heterostructures for atomically thin circuitry” by Mark P Lavendorf et. al, discloses high mobility field-effect transistors that are realized by transferring graphene onto lattice-matched boron nitride (BN) substrates. A major drawback with the graphene-BN device is that the growth process is not self-limiting i.e. graphene film thickness is governed by the time of exposure to the carbon precursor as well as thickness of BN film. Another disadvantage with the BN catalyzed growth is that a large number of wrinkles and folds are observed in the films which disrupt the flow of electrons, thereby obstructing the need of current electronic device.

[0005] Molybdenum disulphide (MoS_2) is another semiconductor layered material with a thickness dependent band gap in the optical range. MoS_2 offers properties such as layered structure, light absorbing property, and gate tunable transport property. Although standalone ultra-thin membranes of MoS_2 have been extensively investigated for energy-efficient electronic devices, no experimental studies exist for optoelectronic properties of graphene- MoS_2 composites.

[0006] Existing hybrid heterostructures based devices have not shown significant activity in memory and/or switching devices, particularly when it comes to switching based on light pulses as well as gate voltage pulses. Existing devices also have lower stability and are not responsive to light and gate intensities and therefore do not possess a wide-band photo-detection. Furthermore, existing hybrid architectures always follow a cross-plane architecture.

[0007] There is therefore a need for a hybrid heterostructure that has applications in multiple opto-electronic devices, preferably, memory and/or switching devices that have capability to induce optoelectronic functionality into graphene, allows controlled photoconduction, can work efficiently at extremely high frequencies, among many other advantages.

OBJECTS OF PRESENT INVENTION

[0008] It is an object of the present invention to provide an opto-electronic sensor that is free of above mentioned disadvantages.

[0009] It is another object of the present invention to combine gate controllable superior electrical property of graphene with light sensitivity of MoS₂ to develop opto-electronic illumination.

[00010] It is another object of the present invention to provide an opto-electronic device that can use graphene and MoS₂ to design high quality ultrathin (< 10 nm) optoelectronic memory/switching devices whose sensitivity can be controlled by using both light and gate voltage.

[00011] It is still another object of the invention to provide an electro-optical device that can work on technology based on SET and RESET functions using light pulses as well as gate voltage pulses.

[00012] It is yet another object of the present invention to provide such architecture for opto-electronic device in which current can flow perpendicular to the layers of the insulating material due to light pulse and can be controlled with an external electric field.

[00013] It is yet another object of the present invention to provide an electro-optical device that meets and provides solutions for current technical challenges such as gate tunability, speed of operation.

[00014] Other objects of the present invention will be apparent from the description of the invention herein below.

SUMMARY OF THE INVENTION

[00015] The present disclosure relates to a non-volatile opto-electronic device made from atomically thin binary hybrids of Graphene and Molybdenum di-Sulphide (MoS₂), wherein superior gate controllable property of graphene is combined with high light sensitivity of MoS₂ in order to enhance opto-electronic illumination of the opto-electronic device. In an embodiment of the present invention, opto-electronic device of the present disclosure includes a memory device, a sensor device, or a switching device, where in hybrids of Graphene and Molybdenum di-Sulphide (MoS₂) are arranged in a planar stacking geometry by laying a continuous sheet of graphene on a continuous sheet of MoS₂.

[00016] According to one embodiment, opto-electronic device of the present disclosure can be set in ON-state (high-resistance state for enabling writing function) with light pulse and can be reset (low-resistance state for enabling erase function) by an electrical voltage pulse.

Light pulse utilizes the illumination property of MoS₂ along its localization property of electron states to enable an avalanche-mediated electron-hole pair generation, thereby allowing writing function on the opto-electronic device whereas the gate controllable electrical property of graphene allows reset function when electrical voltage pulse is applied.

[00017] In one embodiment, architecture of an opto-electronic device of the present disclosure comprises:

- a) at least one layer of graphene;
- b) at least one layer of MoS₂ film deposited over SiO₂ and/or Si substrate, wherein the graphene layer is laid on the MoS₂ layer forming an hetero-hybrid structure, and wherein the graphene is transferred on top of the MoS₂ in a continuous sheet with an electrical conductance in the graphene layer and light pulse conductance in MoS₂ layer forming an in-plane geometry.

[00018] It is a primary objective of the present invention to provide other objects and features of the present invention, which will become apparent from the following detailed description considered in conjunction with the accompanying drawings. It is to be understood, however, that the drawings are designed solely for purposes of illustration and not as a definition of the limits of the invention, for which reference should be made to the appended claims. It should be further understood that the drawings are not necessarily drawn to scale and that, unless otherwise indicated, they are merely intended to conceptually illustrate the structures and procedures described herein.

BRIEF DESCRIPTION OF DRAWINGS

[00019] Figures 1(a) and (b) illustrates an exemplary 3-Dimensional and 2-Dimensional architecture of opto-electronic device respectively in accordance with an embodiment of the present invention.

[00020] Figure 2 illustrates an exemplary method of development of opto-electronic device in accordance with an embodiment of the present invention.

[00021] Figure 3 illustrates a solid black line in the R-V_g characteristics of graphene-MoS₂ hybrids in absence of light in accordance with an embodiment of the present invention.

[00022] Figure 4 illustrates an exemplary switching operation of the device in accordance with an embodiment of the present invention.

[00023] **Figure 5** depicts device operation over many cycles in accordance with an embodiment of the present invention.

[00024] **Figure 6** illustrates influence of illumination intensity on device response in accordance with an embodiment of the present invention.

[00025] **Figure 7(a)** represents a near relaxation free nature of high resistance state for low intensity light pulse at different gate voltages in accordance with an embodiment of the present invention.

[00026] **Figure 7(b)** illustrates R-V_g response of opto-electronic device in accordance with an embodiment of the present invention.

[00027] **Figure 8(a)** illustrates switching operation of an opto-electronic device in accordance with an embodiment of the present invention.

[00028] **Figure 8(b)** illustrates R-V_g response of an opto-electronic device in accordance with an embodiment of the present invention.

[00029] **Figure 9(a)** illustrates switching operation of an opto-electronic device in repeatable mode in accordance with an embodiment of the present invention.

[00030] **Figure 9(b)** illustrates operation of an opto-electronic device at room temperature with respect to exfoliated sample in accordance with an embodiment of the present invention.

[00031] **Figure 9(c)** illustrates operation of an opto-electronic device at room temperature with respect to CVD sample in accordance with an embodiment of the present invention.

[00032] **Figure 10** illustrates 'ON' and 'OFF' states of an opto-electronic switch over several hours for many cycles in accordance with an embodiment of the present invention.

[00033] **Figure 11** illustrates switching characteristics as a inherent nature of the graphene-MoS₂ hybrid in accordance with an embodiment of the present invention.

DETAIL DESCRIPTION OF THE INVENTION

[00034] Embodiments described herein and various features and advantageous details thereof are explained more fully with reference to the non-limiting embodiments that are illustrated in the accompanying figures and detailed in the following description. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the embodiments herein. Examples used herein are intended merely to facilitate an understanding of ways in which the embodiments herein may be practiced and to further enable those of skill in the art to practice the embodiments herein. Accordingly, the examples should not be construed as limiting the scope of the embodiments herein.

[00035] Embodiments of a device as a sensor/switch/memory and methods of implementation of a device are provided with exemplary embodiments being discussed below in detail.

[00036] Embodiments of present invention relate to fabrication and developments in non-volatile memory devices based on hybrid inorganic/organic nano-composites and also switching and carrier transport mechanisms in the hybrid non-volatile memory devices. More preferably, present invention relates to a device and implementation of method to induce optoelectronic functionality into graphene by physically hybridizing it to light sensitive membranes of MoS₂.

[00037] Graphene refers to a two-dimensional planar sheet of carbon atoms arranged in a hexagonal benzene-ring structure. A free standing graphene is theoretically stable only in a two dimensional space, from which it can be implied that a truly planar structure of graphene does not exist in a three dimensional space, being unstable with respect to formation of curved structures such as soot, fullerenes, nanotubes etc.

[00038] MoS₂(molybdenum disulphide) is another inorganic graphene analogue which can exhibit excellent electrical and illumination performance. MoS₂ belongs to layered transition metal dichalcogenides (LTMDs) materials, which are traditionally used as solid-state lubricants and as catalysts for hydrodesulfurization and hydrogen evolution. Similar to graphene and h-BN, MoS₂ has a hexagonal crystal structure. Each Mo atom is six-fold coordinated, hexagonally packed between two three-fold coordinated sulfur atoms. Each S–Mo–S quintuple-layer is weakly bonded to other S–Mo–S layers by van der Waals forces. Because of the relatively weak interaction between the S-Mo-S layers, physical or chemical exfoliation methods can be used to cleave MoS₂ flakes down to ultrathin crystals. Properties such as electrical properties of MoS₂ change dramatically from bulk MoS₂ to monolayer due

to interlayer interaction. Bulk MoS₂ is a semiconducting material with an indirect band gap of ~1.2 eV, while monolayer MoS₂ is a direct band-gap material with a band-gap of ~1.8 eV. Also, its charge neutrality level is in the vicinity of the conduction band (Ec), thus n-type contacts can be more easily made for MoS₂ transistors behave as depletion-mode with large negative threshold voltages.

[00039] MoS₂ can be synthesized using top down exfoliation methods and different bottom up approaches such as transition metal sulfurization, thermal decomposition of thiosalts, vapour transportation, and solvo thermalization. In one embodiment chemical vapour deposition (CVD) can be used to give better control over the number of layers if growth occurs via surface mediated synthesis where band-gap of MoS₂ varies from bulk down to monolayer.

[00040] According to one embodiment, a method can be implemented to synthesize high quality MoS₂ single crystal flakes (with lateral sizes up to several micrometers) more preferably to 1 nm on a CVD grown graphene (CVD-G) surface. MoS₂ nanoflakes can be epitaxially synthesized on the surface of graphene at relatively room temperature. Relatively large lattice mismatch between MoS₂ and graphene (~28%) is expected to be relaxed through the weak van der Waals force.

[00041] Resulting hybrid layer can lead to an unprecedented controllability in photoconduction and can be said to have a potential to operate at extremely high frequencies. In one embodiment of present invention, architecture of the proposed opto-electronic device can be said to have combined carbon nanotubes, more preferably graphene field effect transistor devices, with a photosensitive polymer such as MoS₂ in order to fabricate the optoelectronic device. Electric charges are created upon illumination by the polymer-nanotube element of the structure, wherein charge storage occurs in a nanotube transducer. Read and erase functions are performed by a voltage applied across the nanotube channel. Spectral response of the device can be adjusted by utilizing different polymers with different absorption characteristics.

[00042] Figure 1(a) illustrates an exemplary architecture of an opto-electronic device in a three dimensional (3D) view and Figure 1(b) illustrates an exemplary architecture of an opto-electronic device in a two dimensional (2D) view. According to one embodiment, architecture of opto-electronic device 100 of the present invention comprises:

- a) at least one layer of graphene 102;

- b) at least one layer of MoS₂ film 104 deposited over SiO₂ 106 and/or Si 108 substrate, wherein the graphene layer 102 is laid on the MoS₂ film 104 forming a hetero-hybrid structure, wherein the graphene 102 is transferred on top of the MoS₂ film 104 in a continuous sheet with an electrical conductance in the graphene layer 102 and light pulse conductance in MoS₂ layer 104 forming an in-plane geometry.

[00043] According to one embodiment, graphene layer 102 may be formed separately and then transferred on the MoS₂ film 104. Graphene layer 102 may be formed by any appropriate method, including but not limited to chemical vapor deposition (CVD), mechanical exfoliation, adhesion, chemical exfoliation, and thermal decomposition silicon carbide (SiC). Graphene layer 102 may include a network or a film of graphene flakes in some embodiments. For a graphene based sensor that is used in transmission mode, substrate may be a material such as quartz, glass, or sapphire, which are transparent in the approximate frequency range of absorption peak of the graphene layer 102.

[00044] According to one embodiment, exfoliation is a process in which a required product can be formed by peeling away very thin sheets from its existing natural form. For instance, SiO₂ is ideal as a graphene substrate because it allows a single atom-layer of graphene to be visible with the naked eye under white light, unlike pure silicon's mirror-like surface. The contrast between a graphene flake and a substrate has to be relatively high for the flake to be visible to a naked eye, which, in the case of a SiO₂ on Si substrate, relies on the relative indices of refraction of SiO₂, Si, and graphene. According to *Blake et. al*, any thickness of SiO₂ will do when the right filters are used. A fresh piece can be removed and pressed firmly with the adhesive side down to the shiny side of the substrate for about ten seconds. A tape can then be gently peeled away with thick, shiny layers of graphite stuck to it. Resulting graphite is known as exfoliated graphite/graphene.

[00045] According to another embodiment, MoS₂ flakes can be mechanically exfoliated from bulk ingot and then can be transferred to a heavily p-doped silicon substrate 108 (0.01-0.02 Ω cm) with a 300nm SiO₂ capping layer 106. Silicon substrate 108 can serve as a global back gate, while the 300nm SiO₂ 106 can serve as a gate dielectric. After the step of flake transfer, electron beam lithography technique can be used to pattern the flake, followed by plasma dry etching. Since graphene 102 can include a single atomic layer or a double atomic layer and thickness of MoS₂ films 104 can also be restricted to a very few atomic layers (< 10) (~1nm), thickness of the device can be less than 10 nm in thickness and can be operated up to 350 K. In

some embodiments, substrate may comprise any other appropriate material, depending upon the mode in which sensor/memory/switch is used. In an embodiment, n-channel switches can also be created by sandwiching few layers of MoS₂ 104 between a monolayer graphene sheet 102 and a metal thin film. Molybdenum disulphide (MoS₂) can act as barriers for electrons tunnelling from one layer of graphene to another. An advantage of this type of structure is that the current which flows perpendicular to the layers of the insulating material, also referred to as “tunnelling current”, which can be controlled with an external electric field. Technically, this is because the electrons induced in graphene by the external field have a higher probability for tunnelling and the number of such electrons increases with the field. Although any insulator can be considered as a tunnelling barrier, it is only when the barrier is a few atoms thick that the tunnelling current can be easily measured. MoS₂ is ideal for use in this respect because extremely thin flakes of the materials can be produced using the method as described in the present disclosure.

[00046] According to another embodiment, exfoliated graphene 102 can be placed on MoS₂ film 104 with electrical lead contacts 110 configured on the graphene layer 102. Exfoliation of graphene 102 can be done in a similar way as exfoliation of MoS₂ is performed, but on a polymer coated transparent tape present on a substrate, more preferably on glass slide. Graphene layer 102 may be a single layer, double layer, or multilayer, which, post exfoliation, can be transferred on top of MoS₂ film 104 by utilizing e-beam lithography technique and thermal evaporation technique, or any other suitable set of techniques, so as to make metal contacts on graphene-on-MoS₂ hybrids. Specific structure of the device 100 is planar, which can be made by laying a continuous sheet of graphene 102 on a continuous sheet of MoS₂ 104 (graphene-on-MoS₂).

[00047] In an implementation, an operation of the device 100 involves electrical conductance that is only limited to graphene layer 102 whereas MoS₂ layer 104 is photosensitive layer with no electrical conductance forming an in-plane geometry. Electrical conductivity of graphene can result into measurable persistent photoconductivity and switching/memory actions under appropriate sequence of light pulses through a light source 112 and gate pulses as may be pertinent in figures described below. The device 100 can be less than 10 nm in thickness and comprise a single atomic layer of graphene laid on a (~ 5 to 10) molecular layer thick crystalline film of MoS₂. Switching action of the device can be controlled externally by applying appropriate light and gate voltage pulses. Light pulse can be applied to set the device in ‘ON’ state, also referred to as high resistance state, for enabling the writing action

to happen by utilization of the optical illumination property of the MoS₂ film 104. Voltage pulses can be applied across the electrode on graphene layer 102 to bring the device 100 in low resistance state 'OFF' state, for enabling erase function to happen by use of electrical conductivity property of graphene layer 102. The 'writing' action can be achieved with a pulse of white light while the 'resetting' of the memory can be carried out with a gate voltage pulse on a global back gate on the highly doped Si substrate 108. Sensitivity of the device 100 can be controlled independent of the gate voltage and the light pulse intensity. Under appropriate conditions, 'ON' state of the memory can be found to be extremely long and well beyond the experimental time scales.

[00048] Figure 2 illustrates an exemplary method to develop an opto-electronic device 200 comprising the steps of:

- a) Transferring exfoliated graphene 201 layer onto a polymer coated transparent tape 202 on a substrate such as a glass slide 203;
- b) transferring MoS₂ flakes 204 onto a (SiO₂/Si) substrate (205/206); and
- c) laying the exfoliated graphene layer 201 on the MoS₂ layer 204 forming an in-plane geometry; wherein the opto-electronic device 200 is set into a high resistance state with a light pulse and reset into low resistance state with an electrical voltage pulse through the graphene layer 201.

[00049] According to another embodiment, in order to make an optoelectronic switch or memory, MoS₂ flakes 204 can be transferred by mechanical exfoliation onto Si 206 and/or SiO₂ 205 substrate. Exfoliation of graphene 201 can be performed similarly on polymer coated transparent tape 202 on a glass slide 203. After exfoliated graphene 201 and exfoliated MoS₂ 204 are prepared in individual layers, a hybrid structure as in step (c) can be formed by laying single or double layer of exfoliated graphene on monolayer or multilayer of MoS₂ to form an in-plane geometry.

[00050] In an embodiment, all measurements relating to light and electrical pulse can be performed using Stanford lock-in amplifier (SR830). Gate voltage (V_g) can be applied across the graphene layer 201 and Si substrate 206 using Keithley-2400 source meter. In case of graphene and graphene-MOS₂ hybrid, measurements can be established using 4-probe technique. For measuring only-MoS₂ devices, 2-probe measurements technique can be used.

[00051] According to another embodiment of present invention, operation of opto-electronic sensor/switch/memory device can rely upon the voltage tunability of the tunneling density of states in graphene and on the effective height of tunnel barrier adjacent to graphene electrode.

Operation of the device involves electrical current only in the graphene layer²⁰¹, and not in MoS₂²⁰⁴. This can be referred to "in-plane" geometry. The device can be configured to measure the tunnel current-voltage curves (I-V) and to characterize the response of electrodes on the graphene layer²⁰¹. A gate voltage (V_g) can be applied across the back gate at Si layer²⁰⁶ and graphene layer²⁰¹, which induces electrical conductance through its surface and can induce erase in memory, leading it to OFF state and resulting into substantial enhancement in the tunnel current and a strong change can be seen at low bias. Both graphene²⁰¹ and MoS₂²⁰⁴ can be flexible because of the layered ultra-thin structure and hence these hybrid devices can be easily exploited in flexible opto-electronic applications. 'ON' state of the opto-electronic memory/switches can be persistent state, which may follow a short light pulse and can be extremely long. The 'ON' state can show nearly no relaxation within experimental time scales (upto 12 hours) and can exceed upto few years. The persistent state and memory operations can be achieved at room temperature and with large area CVD graphene. The two-dimensional nature of the hybrids can allow versatile patterning possibilities with suitable lithographic techniques and can also allow large-scale manufacturing. Since band gap of MoS₂ is known to vary with layer numbers, it is possible to tune the device for a range of wavelengths by simply choosing appropriate thickness (hence the layer numbers) of MoS₂ fortuning the device response for different frequency of light.

[00052] Figure 3 illustrates a solid black line in the R-V_g characteristics of graphene-MoS₂ hybrids in absence of light. Because of the conducting nature of MoS₂ (MoS₂ conductance curve) as depicted on the right side of the 'dirac point', MoS₂ screens the gate voltage and hence resistance (R) becomes insensitive to the gate voltage increment and thus is different from conventional R-V_g characteristics of graphene. Device response can be found to be very sensitive to the light (white LED) as depicted towards the left side of the threshold voltage of MoS₂ and can be shown by the red trace. All the measurements were done at ~110K temperature unless otherwise specified.

[00053] Figure 4 illustrates a typical switching operation of opto-electronic device in accordance with an exemplary embodiment of the present invention. At some negative gate-voltage background (depending on the threshold voltage of MoS₂), application of a light pulse such as avalanche-mediated electron-hole pair generation can SET a device resistance to different value, which is very stable over time and is persistent in nature. Application of a suitable gate pulse can, on the other hand, RESET the device resistance to its original value before light pulse is applied. Therefore, by using suitable light and gate pulses, opto-

electronic device of present invention can be operated as a rewritable optoelectronic switch/memory device. In the graph illustrated in Figure 4, R vs t plot is shown illustrating 'set' and 'reset' operations achieved by light and gate pulses, respectively. For both curves shown in graph value of $I_{LED} = 5$ mA. The vertical red (dashed) and green (dotted) lines are used to indicate the light and gate pulses, respectively. Measurements were done at 110K.

[00054] **Figure 5** depicts device operation over many cycles. Gate controllable sensitivity can also be depicted in the graph. It is clear from the figure that sensitivity of the device decreases with decreasing negative gate voltage. Evolution of the switching effect can be depicted as a function of V_g . For all traces, the value of I_{LED} is taken to be 10 μ A. The vertical red (dashed) and green (dotted) lines are used to indicate the light and gate pulses, respectively.

[00055] **Figure 6** illustrates the influence of illumination intensity on the device response, and depicts that 'ON' state becomes more prominent with higher intensity (corresponds to higher LED current), whereas at low or moderate intensity of illumination, the ON state shows virtually no relaxation. Figure illustrates evolution of the switching action as a function of light intensity. Transient effect dies with lowering light intensity thus showing a flat response at value 20 μ A and 2 μ A of current.

[00056] **Figure 7(a)** represents a near relaxation free nature of the 'ON' state for low intensity light pulse at different gate voltages. For higher intensity pulse, opto-electrical device shows some initial relaxation and then slowly stabilizes. From the figure it can be concluded that nearly relaxation free nature of persistent states are found at three different gate voltages i.e. -40V, -35V and -30V. Also $I_{LED} = 2$ μ A has been used for 0.1 s to 'excite' the opto-electronic device.

[00057] **Figure 7(b)** illustrates R - V_g response of opto-electronic device. From the graph, it is clear that transition from logarithmic decay to nearly relaxation free state after photo excitation with LED current 200 μ A is for 0.1s. Solid lines are guide to eye. Inset shows the trace of 'ON' state over long time scale (~ 12 hrs).

[00058] **Figure 8(a)** illustrates switching operation of an opto-electronic device. Image of a graphene-on-MoS₂ device is shown in which white dashed line is the guide to the graphene outline. To carry out an experiment for this invention, CVD graphene was used in making this device.

[00059] **Figure 8(b)** illustrates R - V_g response of an opto-electronic device.

[00060] Figure 9(a) illustrates switching operation of an opto-electronic device in repeatable mode. Switching action of opto-electronic device can be seen at 110 K. For experimental embodiment, value of $V_g = -30$ V and I_{LED} is 5 mA.

[00061] Figure 9(b) illustrates operation of an opto-electronic device at room temperature with respect to exfoliated sample. For an experimental embodiment, data from an exfoliated device is taken at room temperature as $V_g = -80$ V and $I_{LED} = 5$ mA.

[00062] Figure 9(c) illustrates operation of an opto-electronic device at room temperature with respect to CVD sample. This can directly address the issue of scalability for large area manufacture, patterning and operation. For an experimental embodiment, data from a CVD device is taken at room temperature as $V_g = -40$ V and $I_{LED} = 5$ mA.

[00063] Figure 10 illustrates 'ON' and 'OFF' states of an opto-electronic switch over several hours for many cycles which can be concluded for long time retention response. Data in the graph shows stability of the system in a timescale of hours. In the graph, $V_g = -40$ V and $I_{LED} = 5$ μ A. The vertical red (dashed) and green (dotted) lines are used to indicate the light and gate pulses, respectively.

[00064] Figure 11 illustrates switching characteristics as an inherent nature of the graphene-MoS₂ hybrid. Controlled experiments were performed with only graphene and only MoS₂. No obvious switching action was observed in both cases. In the graph, response of (a) thin layer MoS₂ on Si/SiO₂ and (b) single layer graphene on Si/SiO₂ to light and gate pulses can be depicted at different gate voltages. The vertical red (dashed) and green (dotted) lines are used to indicate the light and gate pulses, respectively. Note that a few points representing the transient response to gate pulse have been removed for clarity.

[00065] It is understood that the specific order or hierarchy of steps in the methodology disclosed is an illustration of exemplary approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the processes may be rearranged. Some of the steps may be performed simultaneously. The accompanying method claims present elements of various steps in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

[00066] There may be many other ways to implement the invention. Various functions and elements described herein may be portioned differently from those shown without departing from the spirit and scope of the invention. Various modifications of these embodiments will readily apparent to those skilled in the art in view of present disclosure, and generic method defined herein may be applied to other embodiments.

[00067] All structural and functional equivalents to the elements of the various embodiments of the invention described throughout the disclosure that are known or later come to be known to those ordinary skills in the art are expressly incorporated herein by reference and intended to be encompassed by the invention.

[00068] The above description and drawings are only illustrative of preferred embodiments which achieve the objects, features and advantages of the present invention, and it is not intended that present invention be limited thereto. Any modification of the present invention which comes within the spirit and scope of following claims is considered part of the present invention. Furthermore, to extent that the term “include”, “have” or like is used in the description or the claims, such term is intended to be inclusive in manner similar to the term “comprise” is interpreted when employed as a transitional word in claim.

ADVANTAGES OF PRESENT INVENTION

[00069] The present invention provides for combination of gate controllable superior electrical property of graphene and light sensitivity of MoS₂ to provide opto-electronic illumination.

[00070] The present invention provides an electro-optical device that can work on technology based on SET and RESET functions using light pulses as well as gate voltage pulses.

[00071] The present invention provides an opto-electronic device that can use graphene and MoS₂ to design high quality ultrathin (< 10 nm) optoelectronic memory/ switching devices whose sensitivity can be controlled by using both light and gate voltage.

[00072] The present invention provides an architecture for opto-electronic device in which current can flow perpendicular to the layers of the insulating material due to light pulse and can be controlled with an external electric field due to applied voltage pulse.

[00073] The present invention provides an electro-optical device that meets and provides solution for current technical challenges such as gate tunability, speed of operation.

[00074] Other advantages of the present invention are apparent from the description of the invention presented herein.

CLAIMS

We claim

1. An opto-electronic device comprising:
 - a) at least one layer of graphene;
 - b) at least one layer of MoS₂ film deposited over a substrate, wherein said graphene layer is laid on said MoS₂ film forming an hetero-hybrid structure, and wherein said graphene is transferred on top of said MoS₂ in a continuous sheet forming an in-plane geometry.
2. The device according to claim 1, wherein said device is selected from one or more of a switch device, a sensor device, and a memory device.
3. The device according to claim 1, wherein said graphene is positioned onto a polymer coated tape, wherein said polymer coated tape is positioned onto a second substrate.
4. The device according to claim 3, wherein said second substrate is made of quartz, glass, or sapphire.
5. The device according to claim 1, wherein said device is SET based on a light pulse and is RESET based on a gate voltage pulse.
6. The device according to claim 1, wherein said graphene is exfoliated, and wherein said exfoliated graphene is in single layer or double layer.
7. The device according to claim 1, wherein the MoS₂ layer is a single layer or a double layer or a monolayer.
8. The device according to claim 1, wherein the substrate is selected from one or more of SiO₂, Si, or a combination thereof.

9. The device according to claim 7, wherein the Si substrate is highly doped.
10. The device according to claim 1, wherein the graphene is transferred on the MoS₂ film based on one or more of electron beam lithography technique, thermal evaporation technique, or a combination thereof to make a metal contact between said hetero-hybrid structure.
11. The device according to claim 1, wherein said device can be operated at room temperature.
12. An opto-electronic device comprising:
 - a) at least one graphene layer with electrical leads;
 - b) at least one MoS₂ layer with a light pulse conducting property configured on said graphene layer, wherein said opto-electronic device is set into a high resistance state with a light pulse through, and wherein said device is reset into low resistance state with an electrical voltage pulse through the graphene layer.
13. The device according to claim 12, wherein the high resistance state is ON state and low resistance state is OFF state.
14. The device according to claim 12, wherein said electrical leads connect said graphene with a substrate, wherein said MoS₂ layer is configured on said substrate.
15. A method for developing an opto-electronic device comprising steps of:
 - a) Transferring at least one layer of exfoliated graphene onto a polymer coated transparent tape; and
 - b) Transferring at least one layer of MoS₂ flakes onto a substrate, wherein said exfoliated graphene layer is laid on said MoS₂ layer forming a hetero-hybrid structure, wherein said exfoliated graphene is transferred on top of said MoS₂ in a continuous sheet with an electrical conductance in the graphene layer and light pulse conductance in MoS₂ layer forming an in-plane geometry.

16. The method according to claim 15, wherein the exfoliated graphene is in single layer or double layer.
17. The method according to claim 14, wherein the MoS₂ layer is a single layer or a double layer or a monolayer.
18. The method according to claim 14, wherein the substrate is selected from one or more of SiO₂, Si, or a combination thereof.

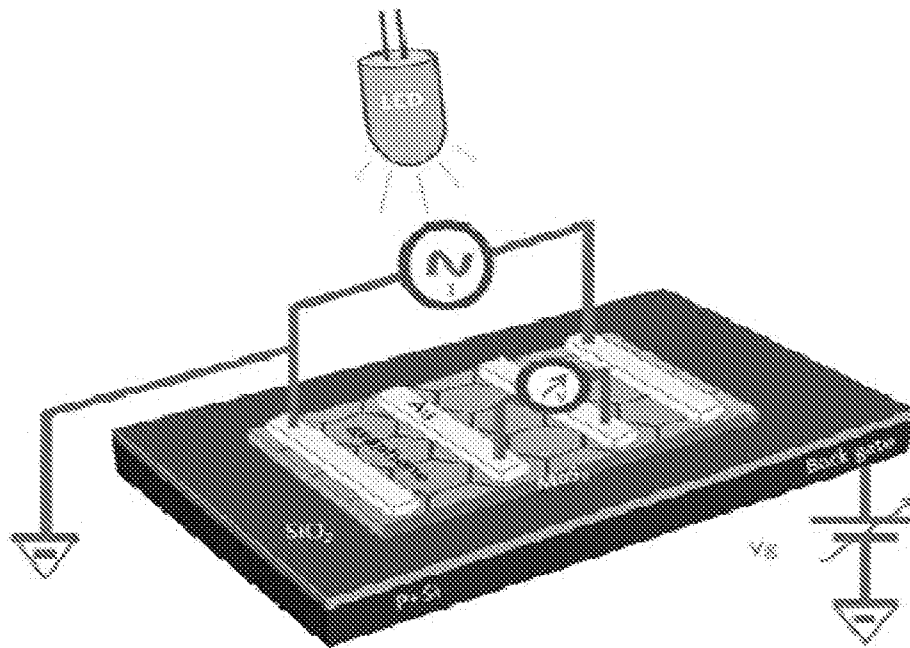


FIGURE 1 (a)

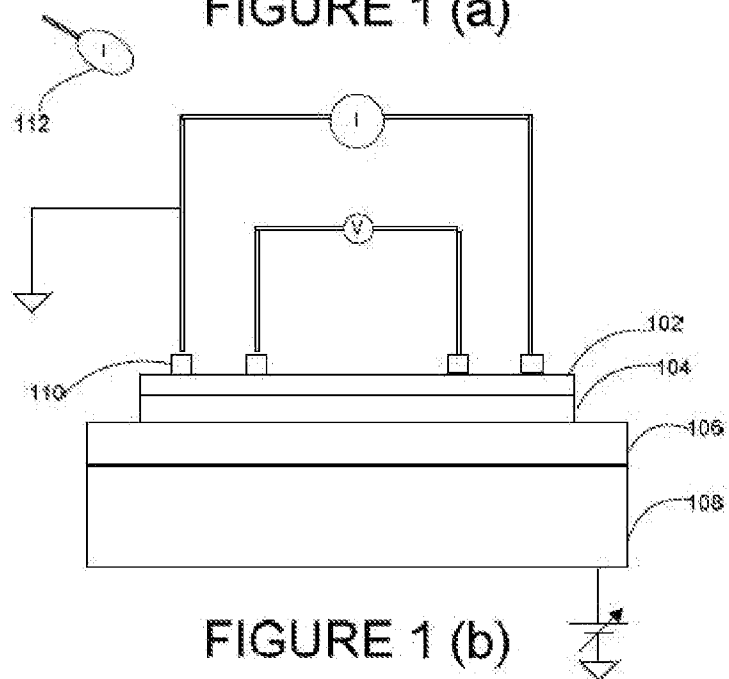
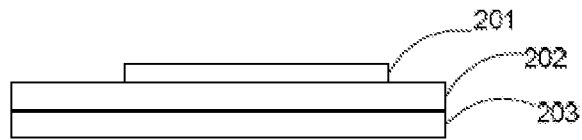
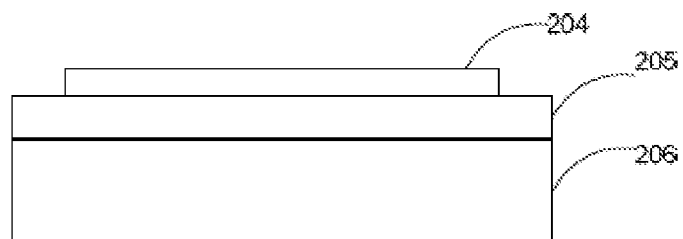


FIGURE 1 (b)

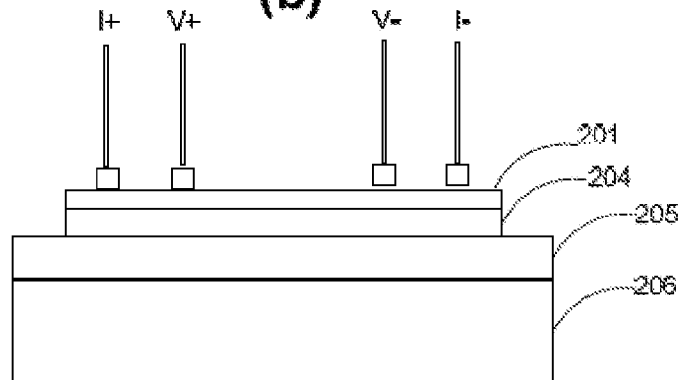
200



(a)



(b)



(c)

FIGURE 2

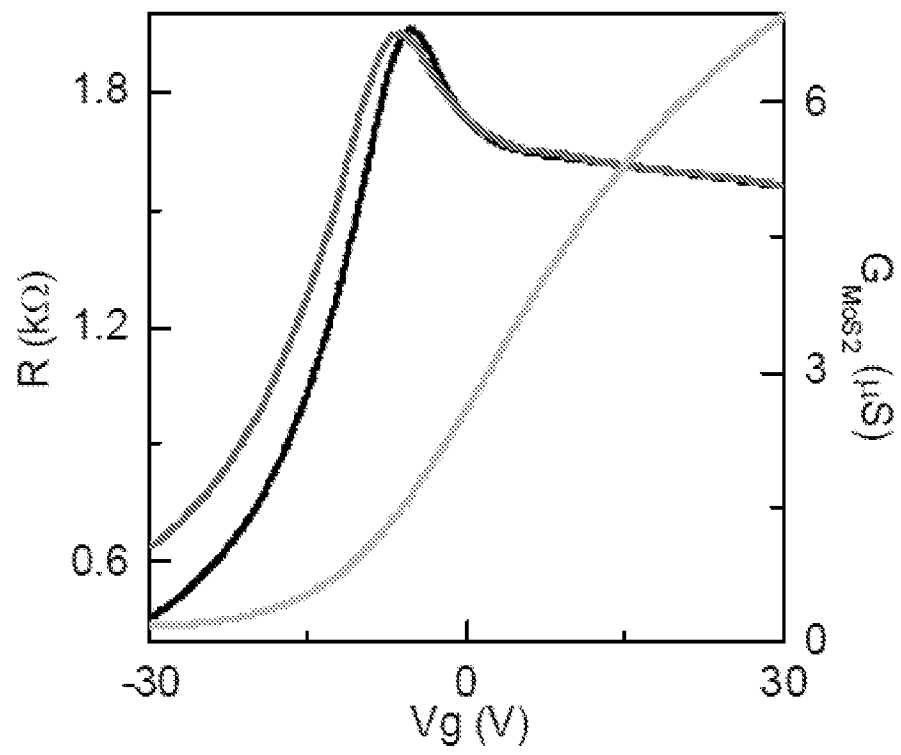


FIGURE 3

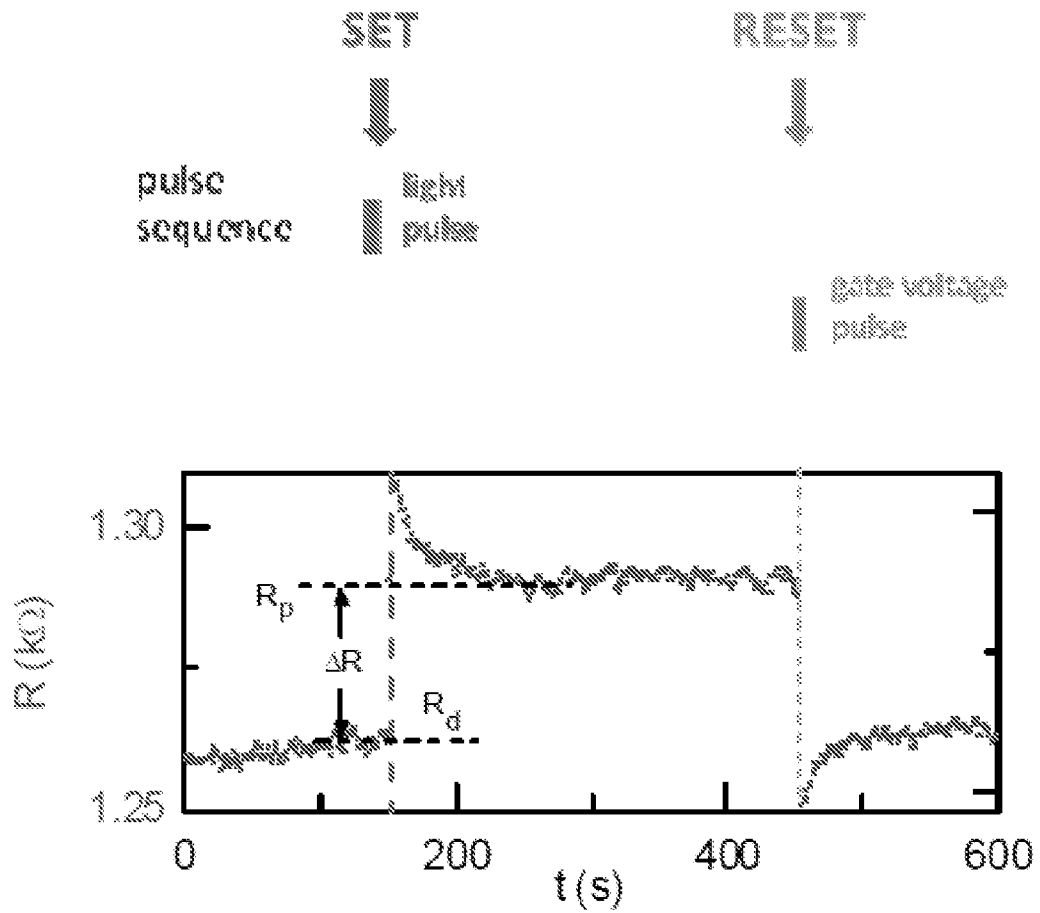


FIGURE 4

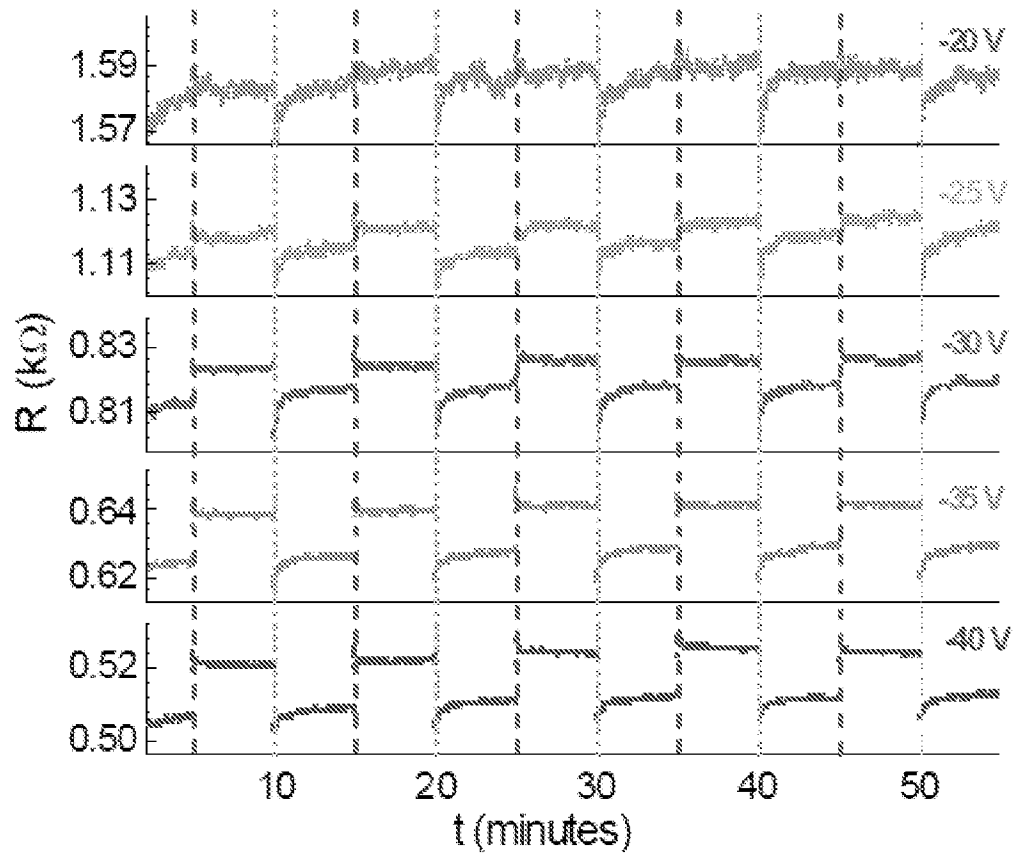


FIGURE 5

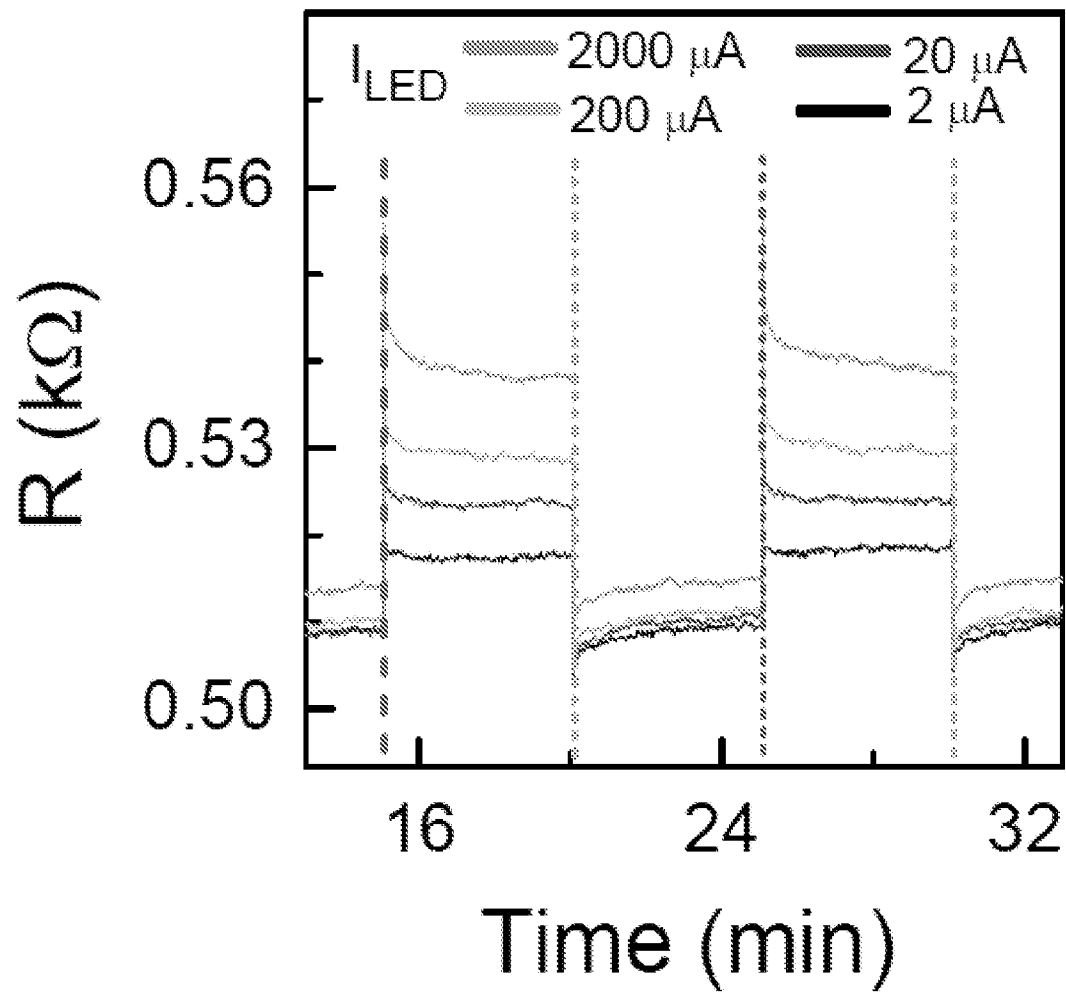


FIGURE 6

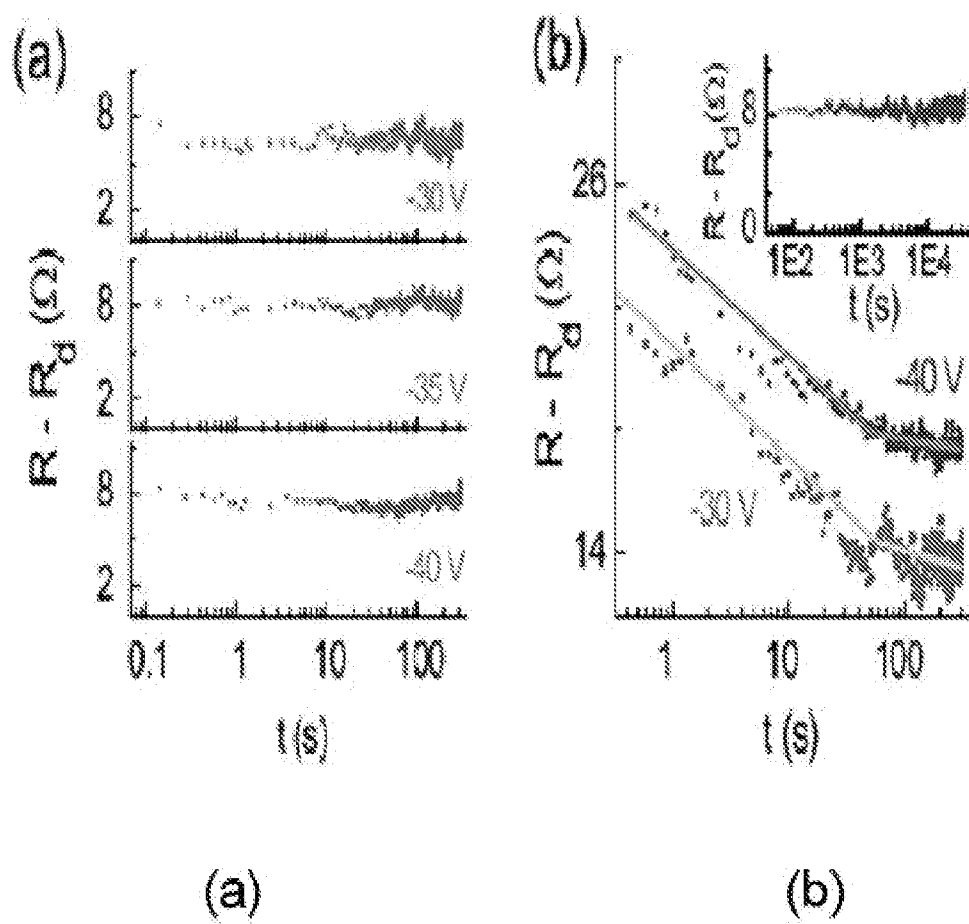


FIGURE 7

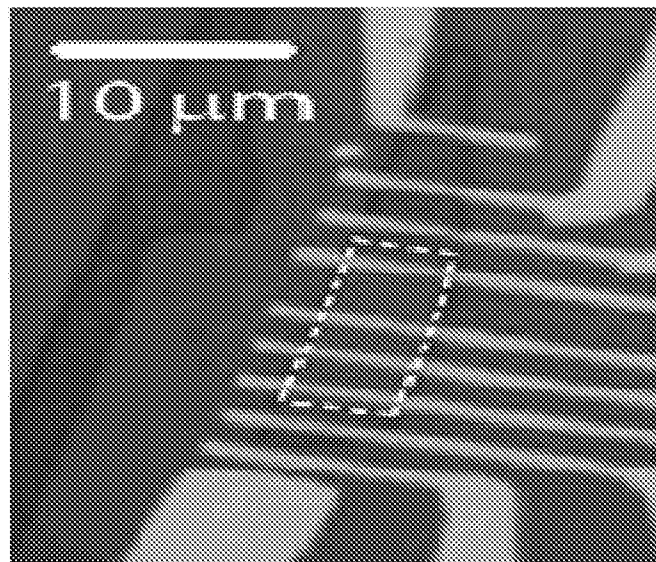


FIGURE 8 (a)

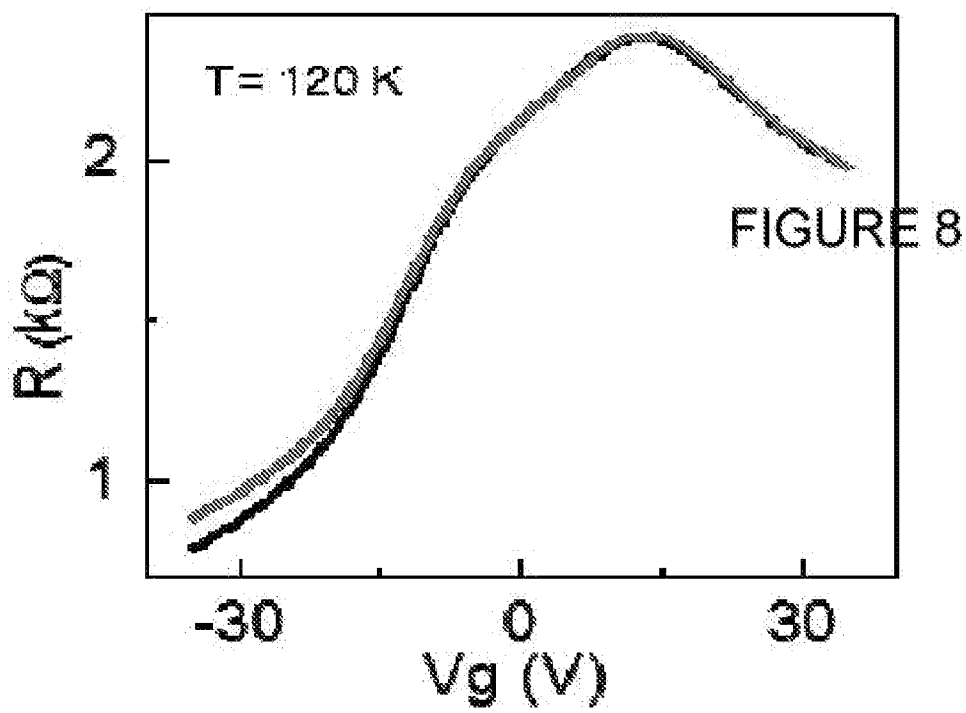


FIGURE 8 (b)

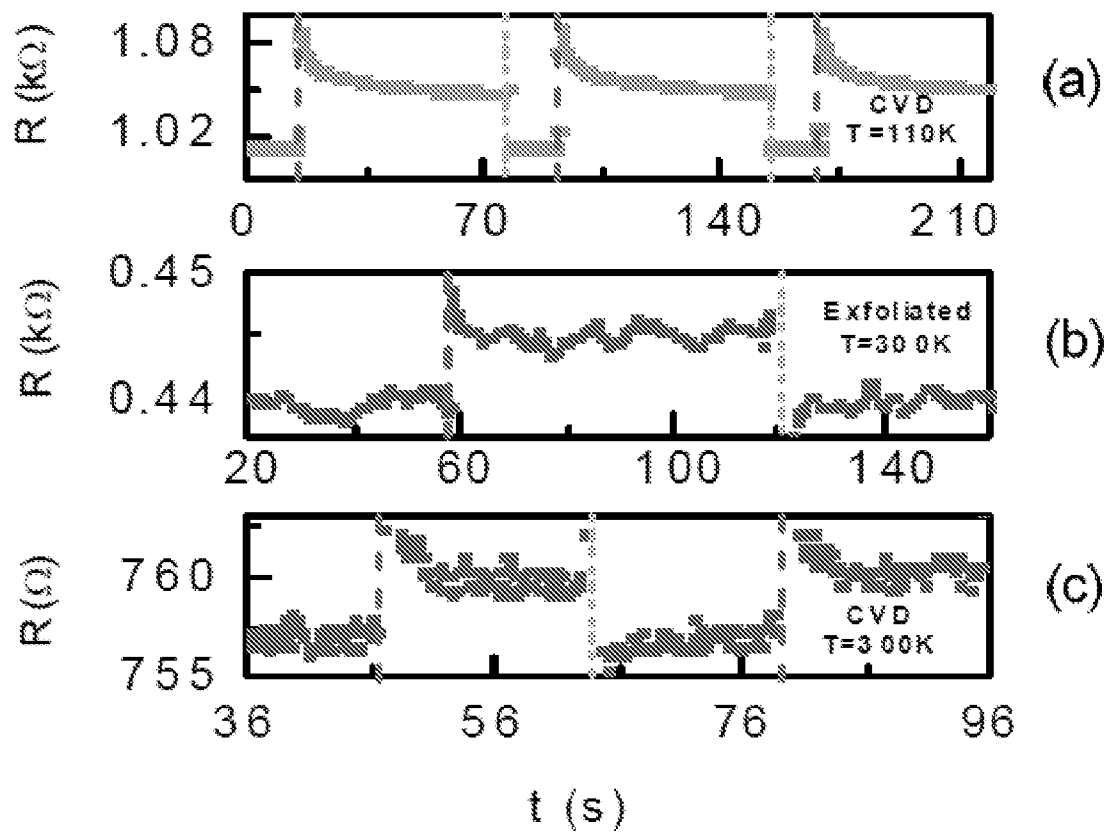


FIGURE 9

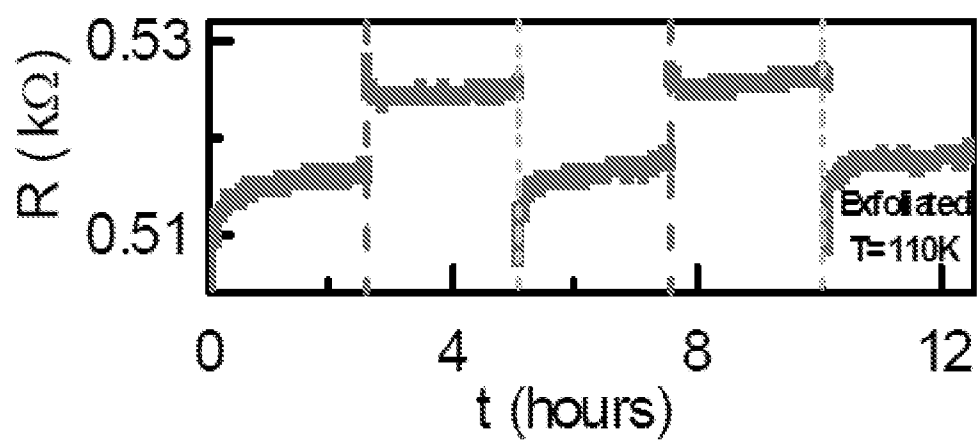


FIGURE 10

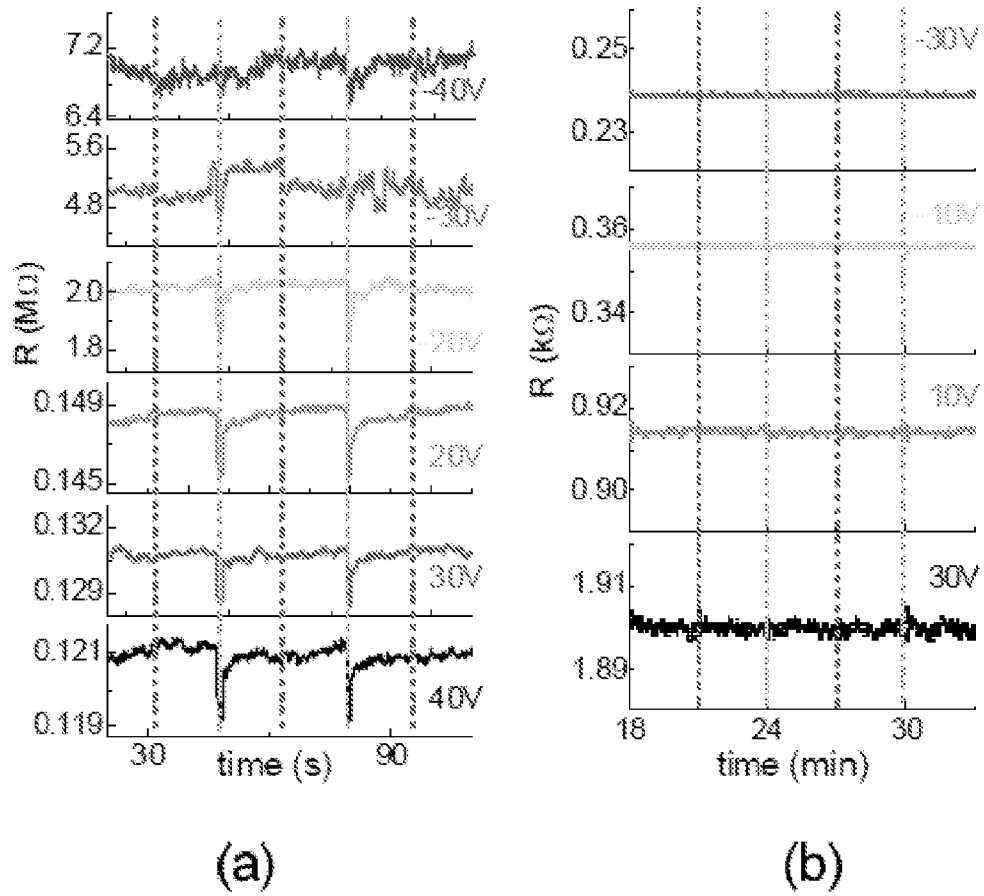


FIGURE 11