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1 [0001] **METAL GATE STRUCTURES FOR FIELD EFFECT**
2 **TRANSISTORS AND METHOD OF FABRICATION**

3 [0002] **BACKGROUND**

4 [0003] 1. Field

5 [0004] Field effect transistor technology which may be in the form of a 3D gate
6 (FinFET) or a planar gate MOSFET.

7 [0005] 2. Description of the Background Art

8 [0006] This section describes background subject matter related to the disclosed
9 embodiments of the present invention. There is no intention, either express or implied,
10 that the background art discussed in this section legally constitutes prior art.

11 [0007] The semiconductor industry is poised to make general use of 3D FinFET
12 gate structures and various planar MOSFET gate structures during the coming years.
13 There is a need to develop FET gate structures which can meet the new size node in
14 semiconductor manufacturing, which will be in the range of 10 - 15 nm. Because FET
15 structures generates significant electrical effects on neighboring structures, and the
16 spacing between the structures is decreasing, there is a need to improve the metal gate
17 structures in a manner which better controls electrical effects while maintaining good
18 conductivity. To provide a starting background against which the present, inventive
19 technology may be better understood, applicants want to describe at least a portion of the
20 published art which is related to applicants' improved metal-comprising gate structures,
21 and a fabrication method which is useful in making the improved metal-comprising gate
22 structures.

23 [0008] U.S. Patent No. 7,105,934 to Anderson et al., issued September 12 2006,
24 entitled: "FinFET With Low Gate Capacitance And Low Extrinsic Resistance" describes
25 a Fin FET device designed to lower gate capacitance and extrinsic resistance in a field
26 effect transistor. The method of forming the structure comprises forming an isolation

1 layer comprising a BOX layer over a substrate, configuring source/drain regions above
2 the isolation layer, forming a fin electrode adjacent to the fin structure, disposing a gate
3 insulator between the first gate electrode and the fin structure, positioning a second gate
4 electrode transverse to the first gate electrode, and depositing a third gate electrode on
5 the fin structure, the first gate electrode and the second gate electrode. (Abstract)

6 [0009] U.S. Patent No. 7,396,710 to Okuno, issued July 8, 2008, entitled: "Fin-
7 type Semiconductor Device With Low Contact Resistance And Its Manufacture Method"
8 describes a fin-type semiconductor device which is said to have low contact resistance.
9 The semiconductor device comprises a fin-type semiconductor region (fin) on a support
10 substrate, where the fin has a pair of generally vertical side walls and an upper surface
11 coupling the side walls. An insulated gate electrode structure traverses an intermediate
12 portion of the fin, and has side walls in conformity with the side walls of the fin.
13 (Abstract)

14 [0010] A U.S. Patent Application Publication of Baumgartner et al., Pub. No.: US
15 2009/0309162, published December 17, 2009, and entitled: "Semiconductor Device
16 Having Different Fin Widths", describes a similar structure. The device includes at least
17 one source region and at least one drain region. A plurality of fins extend between a
18 source region and a drain region, wherein at least one fin has a different width than
19 another fin. At least one gate is provided to control current flow through such fins. Fin
20 spacing may be varied in addition to, or alternative to utilizing different fin widths.
21 (Abstract)

22 [0011] A U.S. Patent Application Publication of Jagannathan et al., Pub. No.
23 2011/0260257, published October 27, 2011, and entitled: "High Performance Non-Planar
24 Semiconductor Devices With Metal Filled Inter-Fin Gaps" describes a non-planar
25 semiconductor transistor device which includes a substrate layer. Conductive channels
26 extend between corresponding source and drain electrodes. A gate stack extending in a
27 direction perpendicular to the conductive channels crosses over the plurality of
28 conductive channels. The gate stack includes a dielectric layer running along the

1 substrate and the plurality of conductive channels and arranged with a substantially
2 uniform layer thickness. A metal layer, distinct from the work-function electrode layer,
3 covers the work function electrode layer and is arranged with a substantially uniform
4 height with respect to the substrate, such that the metal layer fills a gap between
5 proximate conductive channels of the plurality of conductive channels. (Abstract)

6 [0012] U.S. Patent Application Publication of Chang et al., Pub. No.
7 2012/0319178, published December 20, 2012, and entitled: "Double Gate Planar Field
8 Effect Transistors" describes a stacked planar device and a method of forming the same.
9 The method includes forming, on a substrate a stack of layers having alternating
10 sacrificial and channel layers, patterning the stack such that sides of the stack include
11 exposed surfaces of the sacrificial and channel layers, forming a dummy gate structure
12 over a region of the stack to establish a planar area, forming a dielectric layer around the
13 dummy gate structure to cover areas adjacent to the planar area, removing the dummy
14 gate structure to expose the stack, selectively etching the stack to remove the sacrificial
15 layers from the channel layers in the planar area, and forming a gate conductor over and
16 in between the channel layers to form a transistor device. (Abstract)

17 [0013] U.S. Patent Application Publication of Wahl et al., Pub. No.
18 2013/0049136, published February 28, 2013, and entitled: "Combined Planar FET and
19 FIN-FET Devices and Methods" describes electronic devices having advantageous
20 design flexibility that avoid channel-width quantization effects common with prior art
21 fin-type (FIN) field effect transistors (FIN-FETS). The devices are said to be obtained
22 by providing multiple FIN-FETs and at least one planar FET on a common substrate.
23 (Abstract)

24 [0014] In a paper titled: "A 22 nm High Performance and Low-Power CMOS
25 Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts &
26 High Density MIM Capacitors", presented in the 2012 Symposium on VLSI Technology
27 Digest of Technical Papers, 978-1-4673-0847-2/12 IEEE, there is a description of
28 upcoming 22 nm logic technology. (Abstract).

[0015] While the technology discussed above has been established to work for the 22 nm node process, the next progression to a 15 nm node and further to the 11 nm node requires a change in materials and fabrication processes to accommodate the smaller size requirements while still meeting performance requirements. Requirements which must be met include trench opening size of less than 10 nm. Fin plus gate height for fill needs to be about 100 nm. This means the metal-comprising gate fill materials and processes must be applicable to a high aspect ratio trench which has an opening size in the range of 10 nm. Further, the conductivity of the gate must be maintained at a feature size of less than 10 nm. Finally, the new materials and processes must have a minimal impact on device variability. Applicants developed a significant amount of data related to resistivity of various materials as the critical dimension of a trench to be metal filled decreases from 22 nm, approaching zero. The data indicates that as the critical dimension of the metal-filled trench becomes smaller, the resistivity of a filled metal-comprising gate tends to increase exponentially. This is a serious problem which needs to be solved by a combination of specialty materials and particular fabrication techniques. The present invention relates to the solution of this problem for filled metal-comprising gates needed for the 15 nm or lower semiconductor device manufacturing node.

[0016] **SUMMARY**

[0017] Embodiments of the present invention relate to combinations of materials and fabrication techniques which permit the fabrication of filled, metal-comprising gates for use in planar and 3D MOSFET gate structures. A first portion of the embodiments relate to gate structures of the kind needed for improved performance in functioning semiconductor structures at the 15 - 10 nm semiconductor manufacturing node, for example. A second portion of the embodiments relate to larger gate structures where there are more options available for modification of the overall structure.

[0018] The embodiments provide several variations in structure and materials.

1 Typically a change in the overall features of the structure, or in the materials used to
2 form the structures, requires that a different series of process steps be used to apply the
3 materials. The differences in crystalline structure and physical properties of the various
4 materials, as well as the spacial requirements for formation of structural features of filled
5 metal-comprising gates must be considered. The processing techniques discussed for
6 application and removal of materials during fabrication of semiconductor structures, such
7 as ALD, CVD, PVD, reflow, and RIE are generally known in the art. The present
8 invention lies in the use of a particular combination of processing steps performed in a
9 specific order; and, the selection of particular combinations of materials which are
10 applied within the processing steps, so that the resulting semiconductor structure formed
11 is as required to provide the performance advantages described herein.

12 [0019] Determination of the combination of materials and processing steps which
13 will perform at a manufacturing node of 15 nm or less has required the development of
14 empirical data on a large scale. We have developed some very advantageous
15 combinations of materials and processes which provide filled, metal-comprising gate
16 structures for field effect transistors (FETs) at the 15 nm or lower semiconductor
17 manufacturing node.

18 [0020] As the MOSFET gate scaling continues, metal gate conductivity is
19 continuously decreasing. Some of the metal-based materials previously used cannot
20 provide adequate conductivity at the 15 nm or lower gate trench width. We have
21 developed new metal and metal alloy compositions which improve conductivity. Our
22 supporting data illustrating various metal and metal alloy conductive line materials is
23 shown in the form of conductivity versus metal line trench width in Figures 9A through
24 9C.

25 [0021] A number of gate structures are described below, to illustrate the most
26 advantageous combination of materials and processes which provide particular filled,
27 metal-comprising FET gate structures. A portion of the structures illustrated have been
28 established to be obtainable for a 15 nm manufacturing node using structure mimicking

1 device data. Each of the gate structures is described with reference to representative
2 figures, since this enables a better understanding of the combination of materials and
3 processes which are required for formation of the structure. While many of the structures
4 are similar, the combination of alternative materials and varying processing conditions
5 produces a new performance result. The fabrication processes described are for use in
6 scaled MOSFET structures including both planar and 3D FET, and provide improved
7 performance and processing compatibility for various channel lengths.

8 [0022] In one embodiment related to smaller gate structures, a portion of a
9 conformal diffusion barrier/work function (DB/WF) layer is etched back to create an area
10 near the upper surface of the filled, metal-comprising gate structure which is then filled
11 with a more conductive metal, so that the overall conductivity of the gate structure is
12 improved. In another embodiment related to larger gate structures, a portion of a
13 conformal metal-comprising conductive layer, which is formed from a diffusion
14 barrier/work function (DB/WF) metal, is selectively etched back without affecting an
15 adjacent, highly conductive gap fill metal portion of the filled, metal-comprising gate
16 structure. The etched back portion of the DB/WF metal layer provides a space which is
17 then filled with a higher conductivity metal, improving the overall conductivity of the
18 gate structure.

19 [0023] We have developed a filled, metal-comprising gate formation process in
20 which gate trench sections are lined with a high k dielectric layer, followed by at least
21 one metal layer deposition. Typically, the metal layer deposition(s) are followed by a
22 chemical mechanical polishing (CMP) step, to remove metal extending above the
23 maximum height of the dielectric liner layer. Subsequently, an etch back process is used
24 to selectively or non-selectively remove an upper portion of the metal fill which
25 comprises a lower conductivity DB/WF metal, for example. The space created by the
26 etch back process is filled with a metal or metal alloy of a higher conductivity. In some
27 instances multiple layers of conductive metals are deposited and a reflow is carried out
28 which converts a portion adjacent metal layers into an alloy.

[0024] In another embodiment, where the overall gate conductivity is acceptable, and a main concern is a possibility of contact misalignment, the etched back sections described above may be filled with a dielectric film which acts as a self-aligned contact etch stop layer.

[0025] The series of process steps used work well for different channel lengths (short and long). Long channel and short channel conductivity for FETs may be maximized for an entire substrate, containing multiples of varying chips. Previously known technology is not applicable for simultaneous processing of a wide range of channel lengths.

[0026] **BRIEF DESCRIPTION OF THE DRAWINGS**

[0027] Figure 1A shows an exemplary FinFET structure comprising a gate 101. The gate is a filled, metal-comprising gate. Variations on the filled, metal-comprising FinFET gate structure, are described for a number of different embodiments herein. With reference to Figure 1A, the filled, metal-comprising gate 101 includes a horizontal section 109 which is in direct communication with the upper surface 103 of conductive Fin 102, and vertical sections 108 which are in direct contact with sidewalls 105 of Fin 102. The exterior surfaces of Fin 102 are typically covered by a thin film of a high k dielectric (not shown).

[0028] Figure 1B shows an exemplary planar FET structure comprising a first metal gate section 111, and a second metal gate section 112, with a contact 113 between the first and second metal gates. A layer of oxide 104 overlies the upper surface 115 of first metal gate 111 and the upper surface 117 of second metal gate 112.

[0029] Figures 2A through 2D illustrate a first series of process steps for fabrication of a first embodiment gate structure where the gate size is designed for a

1 manufacturing node of 15 nm or lower, and where there are multiple sized gates
2 processed simultaneously on a common substrate.

3 [0030] Figures 2E through 2H illustrate the fabrication of a larger gate structure,
4 having a gate size designed for a manufacturing node of larger than 15 nm. The larger
5 gate structure is present on the same substrate as the gate structure illustrated in Figures
6 2A through 2D. The processing is simultaneous and the same process steps are discussed
7 with reference to Figures 2E through 2H.

8 [0031] Figures 3A through 3D illustrate a second series of process steps for
9 fabrication of a second embodiment gate structure where the gate size is designed for a
10 manufacturing node of 15 nm or lower, and where there are multiple sized gates
11 processed simultaneously on a common substrate.

12 [0032] Figures 3E through 3H illustrate the fabrication of the larger gate structure
13 designed for a manufacturing node of larger than 15 nm. The larger gate structure is
14 present on the same substrate as the gate structure illustrated in Figures 3A through 3D.
15 The processing is simultaneous and the same process steps are discussed with reference
16 to Figures 3E through 3H.

17 [0033] Figure 4 shows an enlargement 362 of the second embodiment gate
18 structure shown in Figure 3H, where rather than a conductive layer 312, a dielectric layer
19 415 is applied in the space created by the etchback of layer 308. Deposition of such a
20 dielectric layer is helpful when there is a possibility, due to the electronic device design,
21 that a contact 314 formed as part of the device structure might not land at the correct
22 location on substrate 302.

23 [0034] Figures 5A through 5C illustrate a third series of process steps for

1 fabrication of a third embodiment gate structure where the gate size is designed for a
2 manufacturing node of 15 nm or lower, and where there are multiple sized gates
3 processed simultaneously on a common substrate.

4 [0035]] Figures 5D through 5F illustrate the fabrication of the larger gate
5 structure designed for a manufacturing node of larger than 15 nm. The larger gate
6 structure is present on the same substrate as the gate structure illustrated in Figures 5A
7 through 5C. The processing is simultaneous and the same process steps are discussed
8 with reference to Figures 5D through 5F.

9 [0036] Figures 6A through 6D illustrate a fourth series of process steps for
10 fabrication of a fourth embodiment gate structure where the gate size is designed for a
11 manufacturing node of 15 nm or lower, and where there are multiple sized gates
12 processed simultaneously on a common substrate.

13 [0037] Figures 6E through 6H illustrate the fabrication of the larger gate structure
14 designed for a manufacturing node of larger than 15 nm. The larger gate structure is
15 present on the same substrate as the gate structure illustrated in Figures 6A through 6D.
16 The processing is simultaneous and the same process steps are discussed with reference
17 to Figures 6E through 6H.

18 [0038] Figures 7A through 7D illustrate a fifth series of process steps for
19 fabrication of a fifth embodiment gate structure where the gate size is designed for a
20 manufacturing node of 15 nm or lower, and where there are multiple sized gates
21 processed simultaneously on a common substrate.

22 [0039] Figures 7E through 7H illustrate the fabrication of the larger gate structure
23 designed for a manufacturing node of larger than 15 nm. The larger gate structure is

1 present on the same substrate as the gate structure illustrated in Figures 7A through 7D.
2 The processing is simultaneous and the same process steps are discussed with reference
3 to Figures 7E through 7H.

4 [0040] Figures 8A through 8C illustrate a sixth series of process steps for
5 fabrication of a sixth embodiment gate structure where the gate size is designed for a
6 manufacturing node of 15 nm or lower, and where there are multiple sized gates
7 processed simultaneously on a common substrate.

8 [0041] Figures 8D through 8F illustrate the fabrication of the larger gate structure
9 designed for a manufacturing node of larger than 15 nm. The larger gate structure is
10 present on the same substrate as the gate structure illustrated in Figures 8A through 8C.
11 The processing is simultaneous and the process steps are discussed with reference to
12 Figures 8A through 8F.

13 [0042] Figure 9A shows a graph 900 with conductance on scale 902 versus trench
14 width shown on scale 904 for three metal or metal-comprising materials which are known
15 in the art.

16 [0043] Figure 9B shows a graph 920 with conductance on scale 922 versus trench
17 FICD shown on scale 924, for various metal fill materials deposited using various means
18 of deposition.

19 [0044] Figure 9C shows a graph 940 with conductance on scale 942 versus gate
20 length on scale 944, for various metals and metal alloys. The materials which were
21 reflowed were deposited by atomic layer deposition.

1 [0045] **DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS**

2 [0046] As a preface to the detailed description, it should be noted that, as used in
3 this specification and the appended claims, the singular forms "a", "an", and "the" include
4 plural referents, unless the context clearly dictates otherwise.

5 [0047] When the word "about" is used herein, this is intended to mean that the
6 nominal value presented is precise within $\pm 10\%$.

7 [0048] Embodiments of the present invention relate to combinations of materials
8 and fabrication techniques which permit the fabrication of filled, metal-comprising gates
9 for use in planar and 3D MOSFET gate structures. A first portion of the embodiments
10 relate to gate structures of the kind needed for improved performance in functioning
11 semiconductor structures at the 15 - 10 nm semiconductor manufacturing node, for
12 example. A second portion of the embodiments relate to larger gate structures where
13 there are more options available for modification of the overall structure.

14 [0049] The embodiments provide several variations in structure and materials.
15 Typically a change in the overall features of the structure, or in the materials used to form
16 the structures, requires that a different series of process steps be used to apply the
17 materials. The processing techniques discussed for application and removal of materials
18 during fabrication of semiconductor structures, such as ALD, CVD, PVD, reflow, and
19 RIE are generally known in the art. The present invention lies in the use of a particular
20 combination of processing steps performed in a specific order; and, the selection of
21 particular combinations of materials which are applied within the processing steps, so that
22 the resulting semiconductor structure formed is as required to provide the performance
23 advantages described.

24 [0050] A number of gate structures are described below, to illustrate the most
25 advantageous combination of materials and processes which provide particular filled,
26 metal-comprising FET gate structures. A portion of the structures illustrated have been
27 established to be obtainable for a 15 nm manufacturing node using structure mimicking
28 device data. Each of the gate structures is described with reference to representative

1 figures, since this enables a better understanding of the combination of materials and
2 processes which are required for formation of the structure. While many of the structures
3 are similar, the combination of alternative materials and varying processing conditions
4 produces a new performance result. The fabrication processes described are for use in
5 scaled MOSFET structures including both planar and 3D FET, and provide improved
6 performance and processing compatibility for various channel lengths.

7 [0051] Described below is a filled, metal-comprising gate formation process in
8 which gate trench sections are lined with a high k dielectric layer, followed by at least
9 one metal layer deposition. Typically, the metal layer deposition(s) are followed by a
10 chemical mechanical polishing (CMP) step, to remove metal extending above the
11 maximum height of the dielectric liner layer. Subsequently, an etch back process is used
12 to selectively or non-selectively remove an upper portion of the metal fill which
13 comprises a lower conductivity DB/WF metal, for example. The space created by the
14 etch back process is filled with a metal or metal alloy of a higher conductivity. In some
15 instances multiple layers of conductive metals are deposited and a reflow is carried out
16 which converts a portion adjacent metal layers into an alloy.

17 [0052] Also described below is another embodiment, where the overall gate
18 conductivity is acceptable, and a main concern is a possibility of contact misalignment,
19 the etched back sections described above may be filled with a dielectric film which acts
20 as a self-aligned contact etch stop layer.

21 [0053] Figure 1A shows a FinFET structure 100 which includes a filled metal-
22 comprising gate structure 101 of the kind which may be fabricated using any one of the
23 combination of materials and process steps which are described and claimed herein. The
24 semiconductor Fin 102 and the STI oxide 104 are generally known in the art.

25 [0054] With reference to Figure 1A, a FinFET gate structure, the horizontal
26 section 109 of gate structure 101 and the vertical sections 108 of the gate structure 101
27 are formed so that they are in direct contact with the surfaces of the conductive Fin
28 structure 102. The first layer of the gate structure, which is formed in direct contact with

surfaces of the Fin structure 102 and in direct contact with an STI oxide layer 104 is referred to as a liner layer 106. The liner layer 106, a common feature of all of the filled, metal-comprising gate structures is described herein. The liner layer is illustrated in the cross-sectional view of a planar FET which is shown in Figure 1B. The liner layer is also shown in Figure sets 2 - 8. The liner layer 106 typically comprises a high-k dielectric fabricated using an ALD or CVD deposition process which forms a conformal layer having a thickness in the range of about 1nm to about 3 nm. High-k liner layer 106 comprises a material selected from the group consisting of hafnium oxide, hafnium oxide silicate, hafnium nitride, Zr-doped hafnium oxide, and combinations thereof, by way of example and not by way of limitation. The liner layer is deposited over the surface of Fin 102 (where there is typically an oxide layer on the surface of the Fin) and over STI oxide layer 104 in Figure 1A.

[0055] Following deposition of the liner layer 106, a metal-comprising layer which acts as a diffusion barrier layer and a work function metal-containing combined layer combined (DB/WF layer) 208, which has an electrical conductivity selected based on desired device function, is applied over liner layer 106. DB/WF layer 208 is typically applied using a method which applies a conformal layer, such as atomic layer deposition (ALD) or chemical vapor deposition (CVD), where the material deposited is selected from the group consisting of TiN, TiAl, TaAl, TiAlC, WSi, WN, and combinations thereof.

[0056] After deposition of liner layer 106 and DB/WF layer 208, the materials and processing which are subsequently applied are varied depending on the filled, metal-comprising gate structure which is most beneficial to a particular application. Figure sets 2 through 8 represent embodiment gate structures which may be fabricated. It is understood that with respect to gate fill applications, when it is desired to control the thickness of an individual layer which has been applied, and that surface rises above the surface of DB/WF layer 208, chemical mechanical polishing (CMP) may be used for this purpose.

[0057] Figure 1B represents a planar FET transistor structure of a kind known in the semiconductor industry. (The structure includes a silicon substrate 102, two gate sections, 111 and 112, each of which is adjacent to, but electrically separated from contact 113.) Filled metal-comprising gate sections 111 and 112 each include a high k dielectric layer 106, and a metal fill layer 208 with an overlying more conductive metal fill 212. The higher conductivity metal fill 212 is present at the upper surface 115 of gate section 111 and the upper surface 117 of gate section 112. An overlying insulating dielectric layer 104 is in contact with both the electrical contact 113 and both gate sections 111 and 112. The materials used to form the filled, metal-comprising gate sections are the same as those described with respect to Figure 1A.

[0058] Figures 2A - 2H show a set of processing steps which make up a first embodiment fabrication process. Figures 2A - 2D represent process steps used to fabricate a small CD filled, metal comprising gate structures (typically having a CD of 15 nm or smaller). A MOSFET gate trench 203 having a liner layer 206 of a high-k dielectric layer is typically formed from hafnium oxide. A conformal metal-comprising layer 208 (which becomes a metal fill when the CD is as small as 15 nm or less) is applied over the liner layer 206. The conformal metal comprising layer material is typically applied by ALD or CVD, and is selected from the group consisting of TiN, TiSiN, TaN, TiAl, TiAlC, TaAlC, WSi, WN, TaAlSi, TaN, TaC, HfC and combinations thereof, depending on the desired performance characteristics for the functional device which will make use of the gate structure.

[0059] Figures 2E - 2H show a set of processing steps which are used for fabrication of larger CD filled, metal-comprising gate structure, for example a CD which is larger than 15 nm and may be 60 nm or larger, by way of example and not by way of limitation. The processing steps for this gate structure are the same as those described above for Figures 2A - 2D, followed by additional steps, where a layer 210, referred to herein as a gap fill metal is applied over the conformal metal comprising layer 208 using an application such as CVD or PVD, depending on the surfaces which are to be covered.

1 In Figure 2E, the gap fill metal 210 is typically applied using a CVD or PVD process.
2 The gap fill metal is typically selected from a Ti liner with Al fill, a Co liner with Al fill,
3 Al, Ti-Al, Co-Al, W, or combinations thereof, by way of example and not by way of
4 limitation. After application, the metal(s) deposited are typically reflowed.

5 [0060] As indicated in Figure 2F, CMP is generally used to remove excess
6 material from the surface of the structure illustrated in Figure 2E. This provides for a
7 cleaner process and a more uniform upper surface after the etch back process, the result
8 of which is shown in Figure 2G. The etch back process is a non-selective etch back
9 process which removes both the conformal layer of metal 208, and the CVD or PVD
10 reflow deposited layer of gap fill metal present as fill, as illustrated in Figure 2F. The
11 depth of etch is typically about 20 % to 30 % of the gate height, depending on the
12 application. When there are both small gate features (15 nm or less CD) as shown in Fig.
13 2B and large gate features (larger than 15 nm CD) as shown in Fig. 2F on the substrate
14 surface which is being processed, both features are etched to approximately the same
15 depth, depending on the composition of the DB/WF layer 208 and the composition of the
16 gap fill layer 210, as well as the performance characteristics desired for the gate
17 structures. The small and large gate structures after the etch back process are shown in
18 Figures 2C and 2G, respectively. The RIE etchant chemistry used for the etch back
19 process is Cl_2 or BCl_3 , by way of example to etch TiAl or TiN; and SF_6 or NF_3 to etch Wn
20 or WSi, by way of example.

21 [0061] Subsequently, to improve the conductivity of the gate, for either the small
22 gate feature illustrated in Figure 2D or for the large gate feature illustrated in Figure 2H, a
23 highly conductive metal selected from the group consisting of Al, W, Co, or
24 combinations thereof is deposited by CVD or PVD, depending on the gate feature size.

25 [0062] Figures 3A - 3H show a set of processing steps which make up a second
26 embodiment fabrication process. Figures 3A - 3D show a set of processing steps which
27 are used for fabrication of small CD filled, metal comprising gate structures (typically
28 having a CD of 15 nm or smaller). A MOSFET gate trench 303 is formed, having a liner

layer 306 of a high-k dielectric layer selected from the group consisting of HfO_2 , HfSiO , Hf SiON , Hf(M)Ox and combinations thereof, by way of example. A conformal metal-comprising layer 308 (which becomes a metal fill when the CD is as small as 15 nm or less) is applied over the liner layer 306. The conformal metal comprising layer material is typically applied by ALD or CVD, and is selected from the group consisting of TiN , TiAl , TaAl , TiAlC , TaAlC , WSi , WN , TaAlSi , TaN , TaC , HfC , and combinations thereof, depending on the desired performance characteristics for the functional device which will make use of the gate structure.

[0063] Figures 3E - 3H represent the fabrication of the larger CD filled, metal-comprising gate structures, which are formed simultaneously on the same substrate as the smaller CD gate structures. The gap fill metal which does not deposit on the interior of the smaller CD gate structures (which are filled with the conformal metal described above) does deposit on the interior of the larger CD structures. The gap fill metal is typically selected from W , Co , Ti-Al , Co-Al , and combinations thereof, by way of example and not by way of limitation, and is applied using CVD or PVD, depending on the surfaces which are to be covered. In Figure 3E, the gap fill metal 310 is applied using a CVD process. After application, the metal(s) deposited are typically reflowed to provide for a good fill.

[0064] As indicated in Figure 3F, CMP is generally used to remove excess material from the surface of the structure illustrated in Figure 3E. This provides a cleaner etch back process and a more uniform upper surface after the etch back process. In this embodiment, the etch back process is a selective etch back process which removes the conformal layer of metal 308, without affecting the gap fill metal 310. This is illustrated in Figure 3G which represents the large feature CD where the exterior layer of conformal metal 308 is removed, but the gap fill metal layer 310 is not removed. Further, since the conformal layer of metal 308 is present in the central portion of the small feature CD, this metal is removed in the etch back process to form the structure shown in Figure 3C. The depth of etch within both the large and small feature CDs is about 20 % to about 30 % of

the trench depth (or gate height), as previously discussed, depending on the application for the gate structure. The RIE etch back process is as follows. Cl_2 or BCl_3 , by way of example, is typically used to etch TiN without disturbing W; SF_6 or NF_3 , by way of example, is typically used to etch WN without disturbing Al. Cl or F based RIE, by way of example, is typically used to etch TiN, TiAl, or W without disturbing Co. It is also possible to use a wet etch, such as an Ammonia Peroxide Mixture ($\text{NH}_4 + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$), also referred to as "SCF", to etch TiN, Ti, Al and W without disturbing Co.

[0065] Subsequently, the space created by the partial depth removal of conformal layer 308 is filled with a highly conductive metal using CVD or PVD of Al, W, Co, and combinations thereof with reflow, to provide the structures shown in Figure 3D (small gate feature) and 3H (large gate feature).

[0066] Figure 4 illustrates an alternative embodiment to the metal fill of the etched back space created using the process described with respect to Figures 3A - 3D and 3E - 3H. This alternative provides a third embodiment fabrication process. For substrates which contain planar FETs of the kind shown in Figure 1B, whether the gate channel size is the large or small, there is a danger that the contact structure 113 may not be landed in the desired position between the gates 111 and 112 (due to contact size, shape, or registration difficulties during processing). To protect against short circuiting between a contact 414 which has been improperly landed, the space created by the partial depth removal of conformal layer 308 (not shown) may be filled with a dielectric film 415 which operates as a self-aligned contact etch stop layer around the outer edge of the highly conductive metal fill layer. Examples of dielectric film materials are SiN, SiON, SiCN, and combinations thereof, by way of example. Since the gap fill metal 310 area is sufficiently large for the large gate channel, as illustrated in Figure 4, the overall conductance of the gate will not be adversely affected.

[0067] A second CMP is used to polish either the last metal fill (e.g. Al or W) or to polish the etch stop dielectric film (eg. SiN, SiON, SiCN).

[0068] The above described structure and process for making it provide a number

1 of benefits for the gate structures produced. The process works well for different channel
2 lengths. Long channel conductivity is retained even while enabling self-aligned contact
3 etch stop (typically SiN) along the edge of the large gate structure.

4 [0069] Figures 5A - 5F illustrate a set of processing steps which make up a fourth
5 embodiment fabrication process. Steps 5A - 5C are used for fabrication of small CD
6 filled, metal comprising gate structures (typically having a CD of 15 nm or smaller). A
7 MOSFET gate trench 503 having a layer 506 of a high-k dielectric layer of the kind
8 previously described herein is formed. A conformal metal-comprising layer 508 (which
9 becomes a metal fill when the CD is as small as 15 nm or less) is applied over the liner
10 layer 506. The conformal metal comprising layer material is typically applied by ALD or
11 CVD, and is selected from the group consisting of TiN, TiSiN, TaN, TiAl, TiAlC, TaAlC,
12 WSi, WN TaN, TaC, HfC, and combinations thereof, depending on the desired
13 performance characteristics for the functional device which will make use of the gate
14 structure.

15 [0070] Figures 5D - 5F show a set of processing steps which are used for
16 fabrication of larger CD filled, metal-comprising gate structure, for example a CD which
17 is larger than 15 nm and may larger than 60 nm, by way of example and not by way of
18 limitation. The fabrication steps for this gate structure are the same as those described
19 above for Figures 5A - 5C, followed by additional steps which provide a thicker layer of
20 a DB/WF material at the bottom of trench 503, which helps protect underlying layers
21 during an etch back process.

22 [0071] A second layer of the same material as that which was applied as layer 508
23 is applied using PVD to form an additional layer 510 at the bottom of trench 503. This is
24 a targeted PVD deposition, as the ALD or CVD conformal layer 508 filled the small gate
25 feature, as shown in Figure 5A. Subsequently, an optional CVD may be used to remove
26 excess metal-containing material which is present on surfaces above the liner layer 506
27 (not shown). This provides a cleaner process and a more uniform upper surface after the
28 etch back process, the result of which is shown in Figures 5B and 5E.

[0072] The etch back process is carried out using RIE processing which makes use of Cl_2 or BCl_3 , by way of example to etch TiAl or TiN; and SF_6 or NF_3 to etch Wn or WSi, by way of example. The etch back process is anisotropic and etches back a portion of the conformal fill layer 508 present in the upper area of the small gate feature as shown in Figure 5B, and a portion of the PVD deposited layer 510 present at the bottom of the trench, as illustrated in Figure 5E.

[0073] Subsequently, a highly conductive metal 512 is applied by CVD or PVD to the etched back areas to form a more conductive gate structure which is illustrated in Figures 5C and 5F. The highly conductive metal is typically Al, W, Co or combinations thereof.

[0074] Figures 6A - 6H illustrate a set of processing steps where all metal fill materials which are applied after the first conformal layer of DB/WF material are applied using PVD. The PVD is targeted toward the long channel gates only, as the short channel gates are completely filled by the first conformal layer. For example, PVD of TiAl as a WF layer, or a PVD Ti liner with Al fill, reflowed, or Ti Al /Ti liner/Al all work well to form a protective layers at the bottom of a trench during an etch back step.

[0075] Figures 6A - 6H show a set of processing steps which are used for simultaneous fabrication of short channel and long channel gates on a single substrate. The small channel gate structures typically have a trench CD of 15 nm or smaller. The large channel gate structures typically have a trench CD ranging from larger than 15 nm up to about 60 nm.

[0076] The trench liner of high k dielectric previously described herein is present as a liner layer in all of the gate trenches. The thickness of the high k dielectric layer 606 is about 2 nm. A layer of a DB/WF material 608, selected from TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN and combinations thereof is applied conformally using ALD or CVD to produce a DB/WF layer which is about 4 nm thick. The DB/WF layer 608 completely fills the short channel gate trench, as shown in Figure 6A, due to the CD of the trench.

[0077] A liner layer 610 of Ti, DB/WF material, is then applied by PVD, to

1 rapidly cover the conformal layer 608 which was previously deposited in the long
2 channel gate trench, as shown in Figure 6E. The thickness of this Ti layer is about 5 nm.
3 Subsequently, a layer of aluminum fill 612 is applied using PVD over the conformal layer
4 608. The thickness of the Al layer is about 200 nm. The metal in the filled, metal
5 comprising trenches is then reflowed.

6 [0078] After deposition of the layers described above, an optional CMP is typically
7 carried out, to provide a uniform, level surface prior to the etch step which follows. The
8 structure of the small channel gate is then as shown in Figure 6B and the large channel
9 gate in Figure 6F.

10 [0079] An anisotropic, non-selective etch back is then performed to create a space
11 in the top of each gate trench. The etch back RIE is performed using Cl_2 , or BCl_3 source
12 gas, for example to etch TiAl or TiN, for example; or using SF_6 , or NF_3 source gas, for
13 example, to etch WN or WSi. The etch back produces the small channel gate structure
14 shown in Figure 6C and the large channel gate structure shown in Figure 6G.

15 [0080] The open spaces 614 created at the top of the gate structures, as shown in
16 Figures 6C and 6G are then filled with a highly conductive metal such as Al, W, Co, and
17 combinations thereof, by way of example, as shown in Figure 6D for the short channel
18 gate and in Figure 6H for the long channel gate. The installation of the highly conductive
19 metal into the top portion of both of the filled metal-comprising gate structures increases
20 the overall performance speed of the gates, while the stability of the overall gate
21 structures is maintained.

22 [0081] Figures 7A - 7H show a set of processing steps which are used for
23 simultaneous fabrication of short channel and long channel gates on a single substrate.
24 The short (small channel) gate structures typically have a trench CD of 20 nm or smaller.
25 The large channel gate structures typically have a trench CD ranging from larger than 15
26 nm up to about 60 nm.

27 [0082] The trench liner of high k dielectric previously described herein is present
28 as a liner layer in all of the gate trenches. The thickness of the high k dielectric layer 706

1 is about 2 nm. A layer of a DB/WF material 708, selected from TiN, TiAl, TaAl, TiAlC,
2 TaAlC, WSi, WN TaSi, TaSiAl, TaN, TaC, HfC, and combinations thereof is applied
3 conformally using ALD or CVD to produce a DB/WF layer which is about 8 nm thick.
4 The DB/WF layer 708 completely fills the short channel gate trench, as shown in Figure
5 7A, due to the CD of the trench.

6 [0083] Subsequently, a layer of Ti-Al or W fill, or a combination thereof, for
7 example, 710 is applied using CVD or PVD, followed by reflow. The resultant structures
8 are illustrated in Figure 7A for the short channel gate and in Figure 7E for the long
9 channel gate.

10 [0084] After deposition of the layers described above, an optional CMP is typically
11 carried out, to provide a uniform, level surface prior to the etch step which follows. The
12 structure of the small channel gate is then as shown in Figure 7B and the large channel
13 gate is as shown in Figure 7F.

14 [0085] An anisotropic, non-selective etch back is then performed to create a space
15 in the top of each channel trench. The etch back RIE is performed using Cl_2 or BCl_3
16 source gas, for example to etch TiAl or TiN; or using SF_6 or NF_3 source gas, for example,
17 to etch WN or WSi. The etch back produces the small channel gate structure shown in
18 Figure 7C and the large channel gate structure shown in Figure 7G.

19 [0086] The open spaces 713 created at the top of the small channel and large
20 channel gate structures, as shown in Figures 7C and 7N, respectively, are then filled using
21 a selective metal on metal deposition of a highly conductive metal such as Co using
22 CVD, as described in U.S. Patent Publication 2009/0269507, or Co applied using electro
23 less plating. The selective metal on metal deposition is carried out using a process such
24 as electro less plating. The final gate structures produced are illustrated in Figure 7D for
25 the small channel gate and in Figure 7H for the large channel gate. The advantage of this
26 process is that it is possible to avoid the need for a second CMP step after the deposition
27 of the top layer 712 of the highly conductive metal, thus reducing cost and complication
28 of the semiconductor substrate processing.

[0087] Figures 8A - 8F show a set of processing steps which are used for simultaneous fabrication of short channel and long channel gates on a single substrate. The small channel gate structures typically have a trench CD of 15 nm or smaller. The large channel gate structures typically have a trench CD ranging from larger than 15 nm up to about 60 nm.

[0088] The trench liner of high k dielectric previously described herein is present as a liner layer in all of the gate trenches. The thickness of the high k dielectric layer 806 is about 2 nm. A layer of a DB/WF material 808, selected from TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN TaSi, TaSiAl, TaN, TaC, HfC, and combinations thereof is applied conformally using ALD or CVD to produce a DB/WF layer which is about 8 nm thick. The DB/WF layer 808 completely fills the short channel gate trench, as shown in Figure 8A, due to the CD of the trench.

[0089] Subsequently, a layer of Ti-Al, W, or Co-Al fill, or a combination thereof, for example, 810 is applied using CVD or PVD, followed by reflow. The resultant structures are illustrated in Figure 8A for the short channel gate and in Figure 8D for the long channel gate.

[0090] After deposition of the layers described above, a CMP is carried out, to provide a uniform, level surface prior to the selective metal deposition step which follows. The structure of the small channel gate is then as shown in Figure 8B and the large channel gate in Figure 8E.

[0091] A selective metal on metal deposition is then carried out using CVD of Co, or electro less plating of CoWP, for example. The final gate structures produced are illustrated in Figure 8C for the small channel gate and in Figure 8F for the large channel gate. The advantage of this process is that it is possible to increase the gate speed by use of a more conductive metal on the surface of the filled metal-comprising gate. However the improvement in gate speed is not expected to be as high as that achieved using an etch back process, where the amount of DB/WF fill in the trenches of the gates is reduced and the amount of a more conductive metal present is more substantially increased. The main

1 advantage of this fabrication method is the simplicity and reduction in production costs.

2 [0092] Figures 9A through 9C show graphs which relate gate channel size (trench
3 width) to conductivity of the gate (trench) for various metal trench fill materials. Figure
4 9A presents data known in the industry, where scale 902 represents the conductivity of a
5 metal fill in a gate trench, and scale 904 represents the trench width in nm. It is readily
6 apparent that as the manufacturing node which requires a 15 nm trench size causes a
7 substantial reduction in conductivity of metal filled gate structures, thereby reducing the
8 gate speed. Cobalt appears to be the best metal fill for gates in terms of operating speed,
9 however this metal is difficult to work.

10 [0093] Figure 9B shows data developed for combinations of materials of the kind
11 described above for use in the filled, metal-comprising gate structures. Scale 922
12 represents the conductivity of the metal fill within a gate trench, and scale 924 represents
13 the trench width in nm. Figure 9C represents data for metal gate fills which are created
14 using a reflow process, and for CVD tungsten. Scale 942 represents the conductivity of
15 the metal fill within a gate trench, and scale 944 represents the gate length (trench width)
16 in nm. Clearly the Co-Al reflowed materials provide better conductivity than previously-
17 known materials.

18 [0094] The above described exemplary embodiments are not intended to limit the
19 scope of the present invention, as one skilled in the art can, in view of the present
20 disclosure, expand such embodiments to correspond with the subject matter of the
21 invention claimed below.

[0095]**CLAIMS****[0096]** We claim:

1. A filled, metal-comprising gate structure useful for FinFet and planar FET structures, wherein said gate structure comprises a trench which is filled with a combination of layers including at least one lower layer of a diffusion barrier/work function metal-containing material, and at least one upper layer of a metal or metal alloy having a high conductivity, so that the speed of the gate is increased by the presence of the upper layer of high conductivity material.

2. A filled, metal-comprising gate structure in accordance with Claim 1, wherein said lower layer of diffusion barrier/work function metal-comprising material is selected from the group consisting of TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN, and combinations thereof.

3. A filled metal-comprising gate structure in accordance with Claim 1, wherein said metal or metal alloy having high conductivity is selected from the group consisting of Al, W, Co, Co-Al alloy, Ti-Al alloy, and combinations thereof.

4. A filled metal-comprising gate structure in accordance with Claim 1, or Claim 2, or Claim 3, wherein said at least one upper layer of a metal or metal alloy having high conductivity is present between a high k dielectric trench liner and a central trench fill metal of a different conductivity.

5. A filled metal-comprising gate structure in accordance with Claim 1 or Claim 2, or Claim 3, wherein a dielectric layer is present adjacent the top surface of said gate,

3 between a high k dielectric trench liner and a central trench fill metal, to act as a short
4 prevention layer with respect to contact structures of a gate which are not properly
5 landed.

1 6. A method of forming a filled metal-comprising gate structure for use in field
2 effect transistors such as a planar FET or a Fin-FET, said method comprising:
3 forming FETs having more than one channel length simultaneously on a single
4 substrate, wherein a first channel length is 15 nm or less, and at least one additional
5 channel length ranges between more than 15 nm to about 60 nm.

1 7. A method in accordance with Claim 6, wherein a high k dielectric liner layer is
2 applied to a trench interior surface within a semiconductor substrate, followed by
3 deposition of a DB/WF layer of material selected from the group consisting of
4 TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN or combinations thereof, wherein said layer is
5 deposited using ALD or CVD; followed by

6 deposition of a more conductive fill layer of Ti-Al, W, or a combination
7 thereof, wherein said fill is applied using CVD or PVD and a reflow is conducted after
8 deposition of said fill; followed by

9 chemical mechanical polishing (CMP) of an upper surface of said trench area to
10 provide removal of excess metal extending above said dielectric liner layer; followed by

11 a non selective etch back of both said DB/WF layer and said metal fill using an
12 RIE where a gas used to create the RIE is selected from Cl_2 , BCl_3 , or a combination
13 thereof when a metal-comprising material being etched is TiAl, TiN, or a combination
14 thereof, and a gas used to create the RIE is selected from SF_6 , NF_3 , or a combination
15 thereof when a metal-comprising material being etched is SN, WSi, or a combination
16 thereof; followed by

17 filling the space created by the etch back with a highly conductive metal
18 selected from the group consisting of Al, W, Co, and combinations thereof using a CVD

19 or PVD process followed by reflow.

1 8. A method in accordance with Claim 6, wherein a high k dielectric liner layer is
2 applied to a trench interior surface within a semiconductor substrate, followed by
3 deposition of a DB/WF layer of material selected from the group consisting of
4 TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN or combinations thereof, wherein said layer is
5 deposited using ALD or CVD;

6 chemical mechanical polishing of an upper surface of said trench area to
7 provide removal of excess metal extending above said dielectric liner layer; followed by

8 deposition of a fill of a more conductive fill layer of Ti-Al, Co-Al, Al, W, Co,
9 or a combination thereof, wherein said fill is applied using CVD or PVD and a reflow is
10 conducted after deposition of said fill; followed by

11 a selective etch back of the DB/WF layer of material which does not affect said
12 more conductive fill layer, wherein said selective etch back is conducted by RIE or a wet
13 etch, where a gas used to create said RIE is selected from Cl_2 , BCl_3 , or a combination
14 thereof when a metal-comprising material being etched is TiAl, TaAl, TiN, or a
15 combination thereof, and a gas used to create the RIE is selected from SF_6 , NF_3 , or a
16 combination thereof when a metal-comprising material being etched is SN, WSi, or a
17 combination thereof, and wherein a wet etch is APM when TiN or Tial is being etched;
18 followed by

19 filling the space created by the etch back with a highly conductive metal
20 selected from the group consisting of Al, W, Co, and combinations thereof using a CVD
21 or PVD process followed by reflow, to increase the speed of said gate.

1 9. A method in accordance with Claim 6, wherein a high k dielectric liner layer is
2 applied to a trench interior surface within a semiconductor substrate, followed by
3 deposition of a DB/WF layer of material selected from the group consisting of
4 TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN or combinations thereof, wherein said layer is

5 deposited using ALD or CVD;

6 chemical mechanical polishing of an upper surface of said trench area to
7 provide removal of excess metal extending above said dielectric liner layer; followed by
8 deposition of a fill of a more conductive fill layer of Ti-Al, Co-Al, Al, W, Co,
9 or a combination thereof, wherein said fill is applied using CVD or PVD and a reflow is
10 conducted after deposition of said fill; followed by

11 a selective etch back of the DB/WF layer of material which does not affect said
12 more conductive fill layer, wherein said selective etch back is conducted by RIE or a wet
13 etch, where a gas used to create said RIE is selected from Cl_2 , BCl_3 , or a combination
14 thereof when a metal-comprising material being etched is TiAl, TaAl, TiN, or a
15 combination thereof, and a gas used to create the RIE is selected from SF_6 , NF_3 , or a
16 combination thereof when a metal-comprising material being etched is SiN, WSi, or a
17 combination thereof, and wherein a wet etch is APM when TiN or TiAl is being etched;
18 followed by

19 filling the space created by the etch back with a dielectric film selected from the
20 group consisting of SiN, SiON, SiCN and combinations thereof using a CVD or PVD, to
21 produce a self aligned exterior layer around said high conductivity fill layer at the surface
22 of said FET, to protect against short circuiting between an electrical contact which may
23 be improperly landed.

1 10. A method in accordance with Claim 6, wherein a high k dielectric liner layer is
2 applied to a trench interior surface within a semiconductor substrate; followed by

3 deposition of a DB/WF layer of material selected from the group consisting of
4 TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN and combinations thereof, wherein said layer
5 is deposited using ALD or CVD; followed by

6 deposition of a second DB/WF layer of material selected from the group
7 consisting of TiN, TiAl, TaAl, WSi, WN, TiN, Ti and combinations thereof, wherein said
8 layer is deposited using PVD; followed by

9 anisotropically etching back deposited layers in a manner such that at least a
10 portion of said DB/WF layer deposited by PVD remains near the bottom of a trench
11 interior surface within a gate having a channel length which ranges between more than 15
12 nm to about 60 nm, wherein said etching is RIE etching and wherein RIE is produced
13 from gases selected from Cl_2 , BCl_3 and combinations thereof when TiAl, TiN, or
14 combinations thereof is etched, or from gases selected from SF_6 , NF_3 , and combinations
15 thereof when WN, WSi, and combinations thereof is etched ; followed by
16 depositing a filling layer of highly conductive metal selected from the group
17 consisting of Al, W, Co, and combinations thereof using CVD, PVD, or a combination
18 thereof.

1 11. A method in accordance with Claim 6, wherein a high k dielectric liner layer is
2 applied to a trench interior surface within a semiconductor substrate, followed by
3 deposition of a DB/WF layer of material selected from the group consisting of
4 TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN or combinations thereof, wherein said layer is
5 deposited using ALD or CVD; followed by
6 deposition of a layer of Ti over said layer of DB/WF material, wherein said Ti
7 layer is deposited using PVD; followed by
8 deposition of a layer of Al by PVD, followed by reflow, to create a fill over
9 said DB/WF layer, wherein said fill has a composition Ti/TiAl/Al , where Ti is adjacent
10 said DB/WF layer and TiAl overlies Ti, and Al overlies TiAl; followed by
11 chemical mechanical polishing (CMP) of an upper surface of said trench area to provide
12 removal of excess metal extending above said dielectric liner layer; followed by
13 a non selective etch back of both said DB/WF layer and said metal fill using
14 an RIE where a gas used to create the RIE is selected from Cl_2 , BCl_3 , or a combination
15 thereof when a metal-comprising material being etched is TiAl, TiN, or a combination
16 thereof, and a gas used to create the RIE is selected from SF_6 , NF_3 , or a combination
17 thereof when a metal-comprising material being etched is SN, WSi, or a combination

thereof; followed by

filling the space created by said etch back with a highly conductive metal selected from the group consisting of Al, W, Co, and combinations thereof using a CVD or PVD process followed by reflow.

12. A method in accordance with Claim 6, wherein a high k dielectric liner layer is applied to a trench interior surface within a semiconductor substrate, followed by

deposition of a DB/WF layer of material selected from the group consisting of TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN or combinations thereof, wherein said layer is deposited using ALD or CVD; followed by

deposition of a more conductive fill layer of Ti-Al, W, or a combination thereof, wherein said fill is applied using CVD or PVD and a reflow is conducted after deposition of said fill; followed by

chemical mechanical polishing (CMP) of an upper surface of said trench area to provide removal of excess metal extending above said dielectric liner layer; followed by

a non selective etch back of both said DB/WF layer and said metal fill using an RIE where a gas used to create the RIE is selected from Cl_2 , BCl_3 , or a combination thereof when a metal-comprising material being etched is TiAl, TiN, or a combination thereof, and a gas used to create the RIE is selected from SF_6 , NF_3 , or a combination thereof when a metal-comprising material being etched is SN, WSi, or a combination thereof; followed by

selective deposition of a conductive metal upon metal, with said conductive metal depositing on metal surfaces contained within a high k dielectric liner, said selective deposition filling a space created by the etch back with a highly conductive metal selected from the group consisting of Co applied by CVD, electro less plating with CoWP.

13. A method in accordance with Claim 6, wherein a high k electric liner layer is

2 applied to a trench interior surface within a semiconductor substrate, followed by
3 deposition of a DB/WF layer of material selected from the group consisting of
4 TiN, TiAl, TaAl, TiAlC, TaAlC, WSi, WN or combinations thereof, wherein said layer is
5 deposited using ALD or CVD; followed by
6 deposition of a more conductive fill layer of Ti-Al, W, or a combination
7 thereof, wherein said fill is applied using CVD or PVD and a reflow is conducted after
8 deposition of said fill; followed by
9 chemical mechanical polishing (CMP) of an upper surface of said trench area to
10 provide removal of excess metal extending above said dielectric liner layer; followed by
11 selective deposition of a conductive metal upon metal, with said conductive
12 metal depositing on metal gate surfaces which are surrounded said by high k dielectric
13 liner layer, wherein said conductive metal deposited is selected from the group consisting
14 of Co applied by CVD, electro less plating with CoWP.

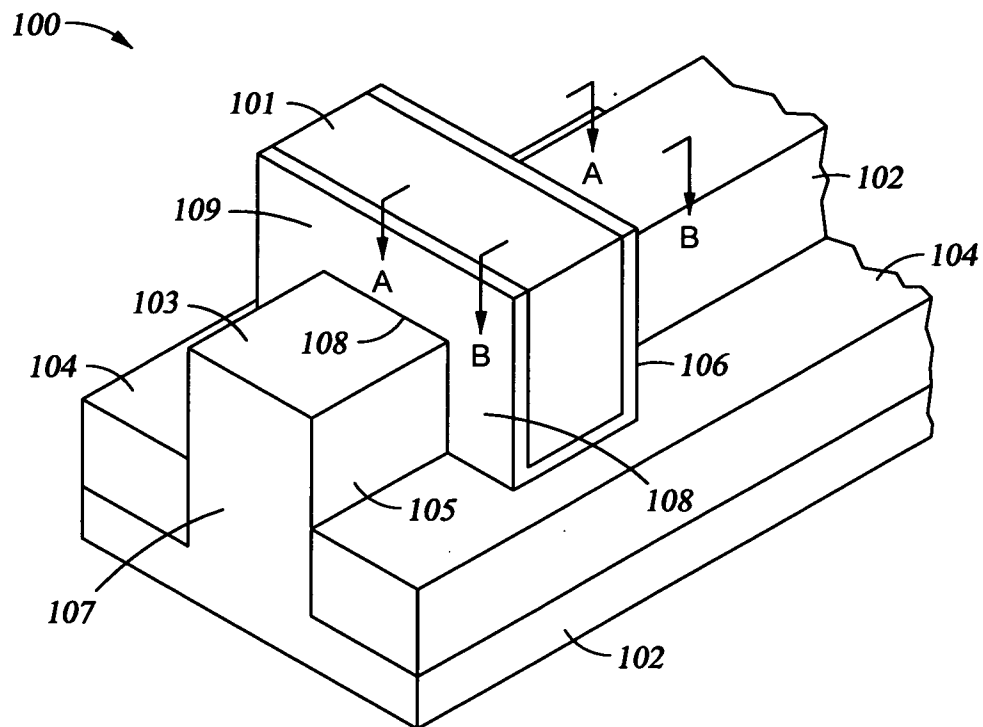


Fig. 1A

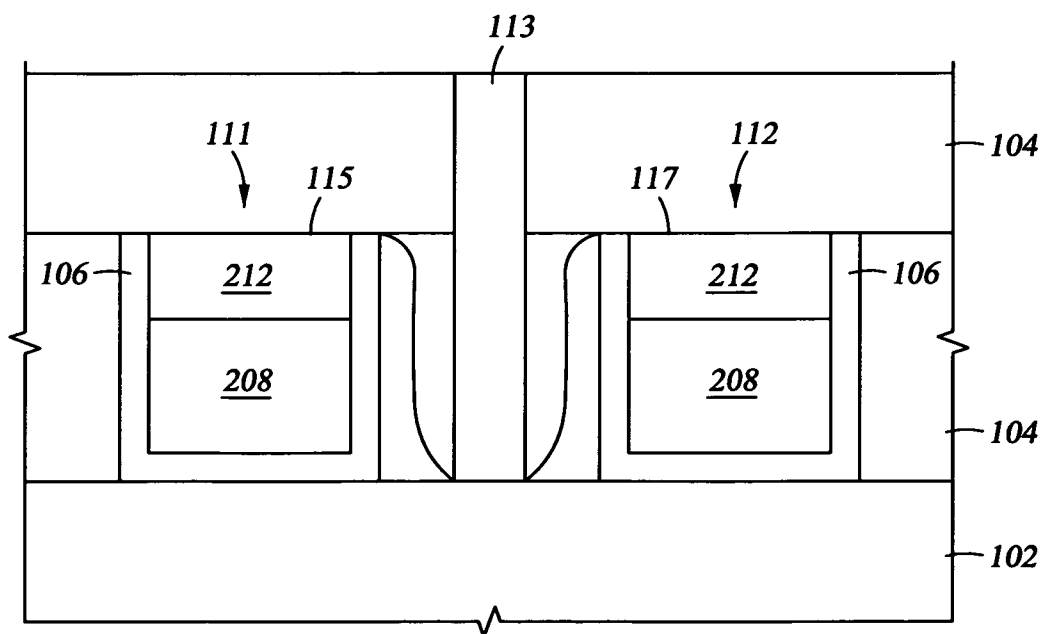


Fig. 1B

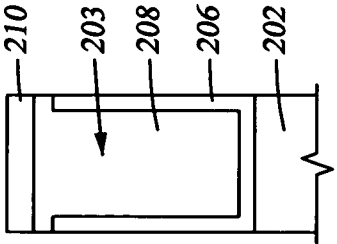


Fig. 2A

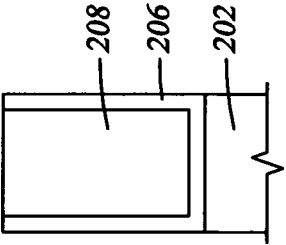


Fig. 2B

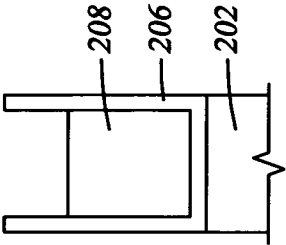


Fig. 2C

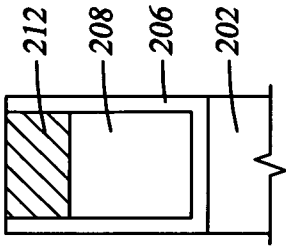


Fig. 2D

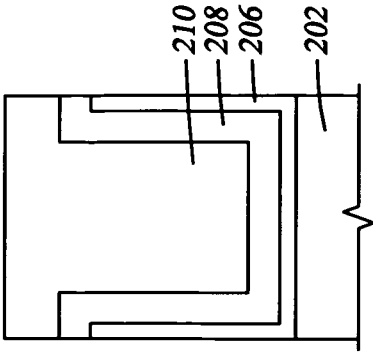


Fig. 2E

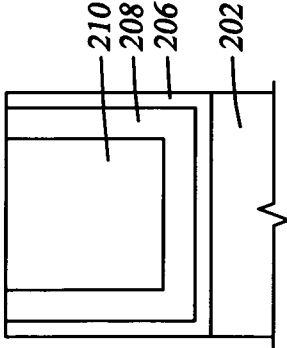


Fig. 2F

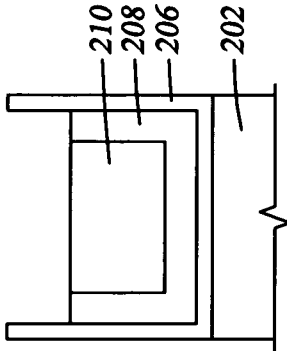


Fig. 2G

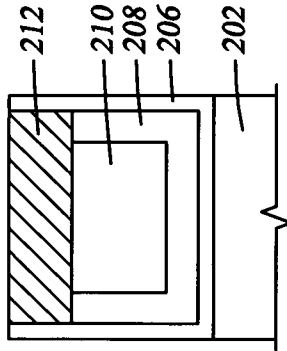


Fig. 2H

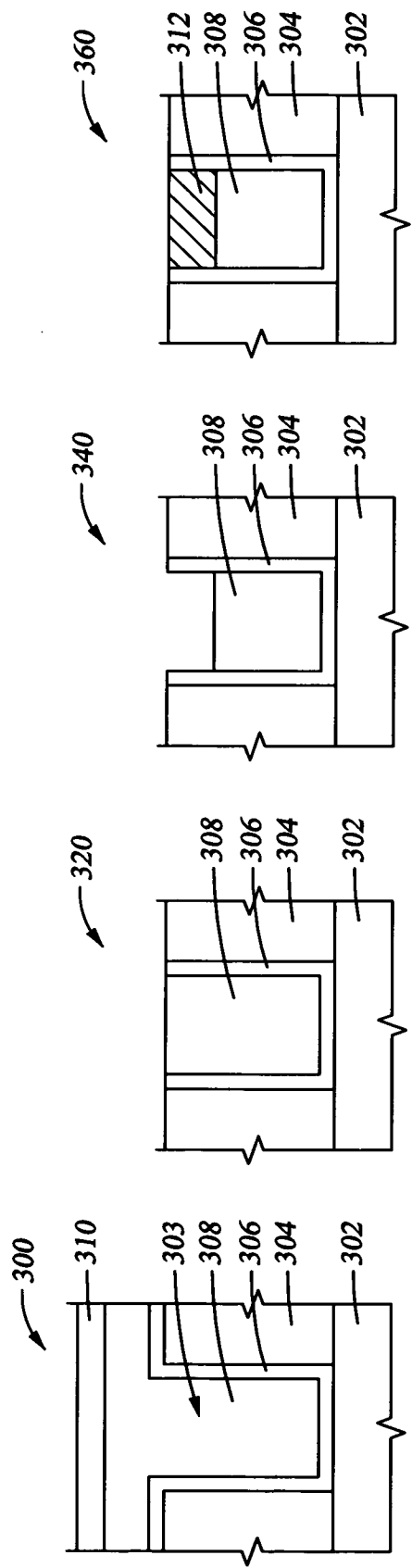


Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

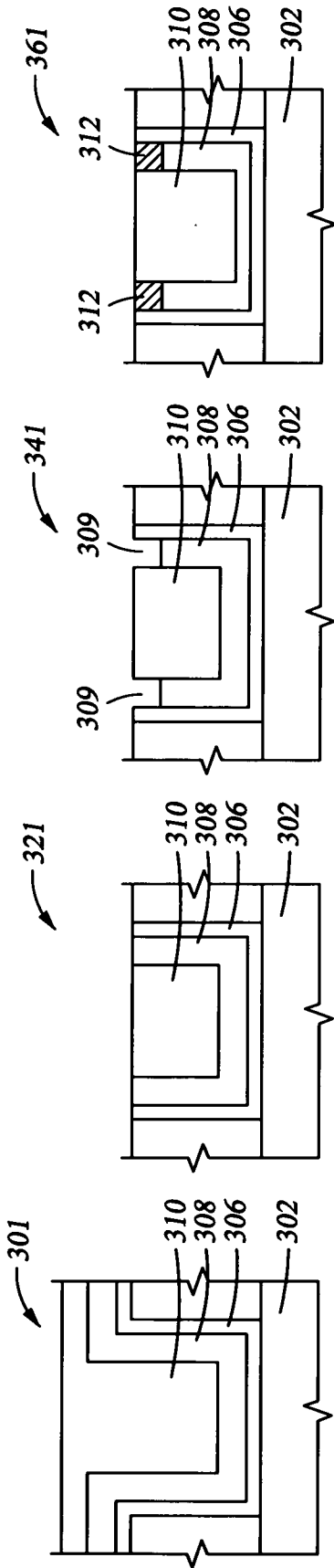
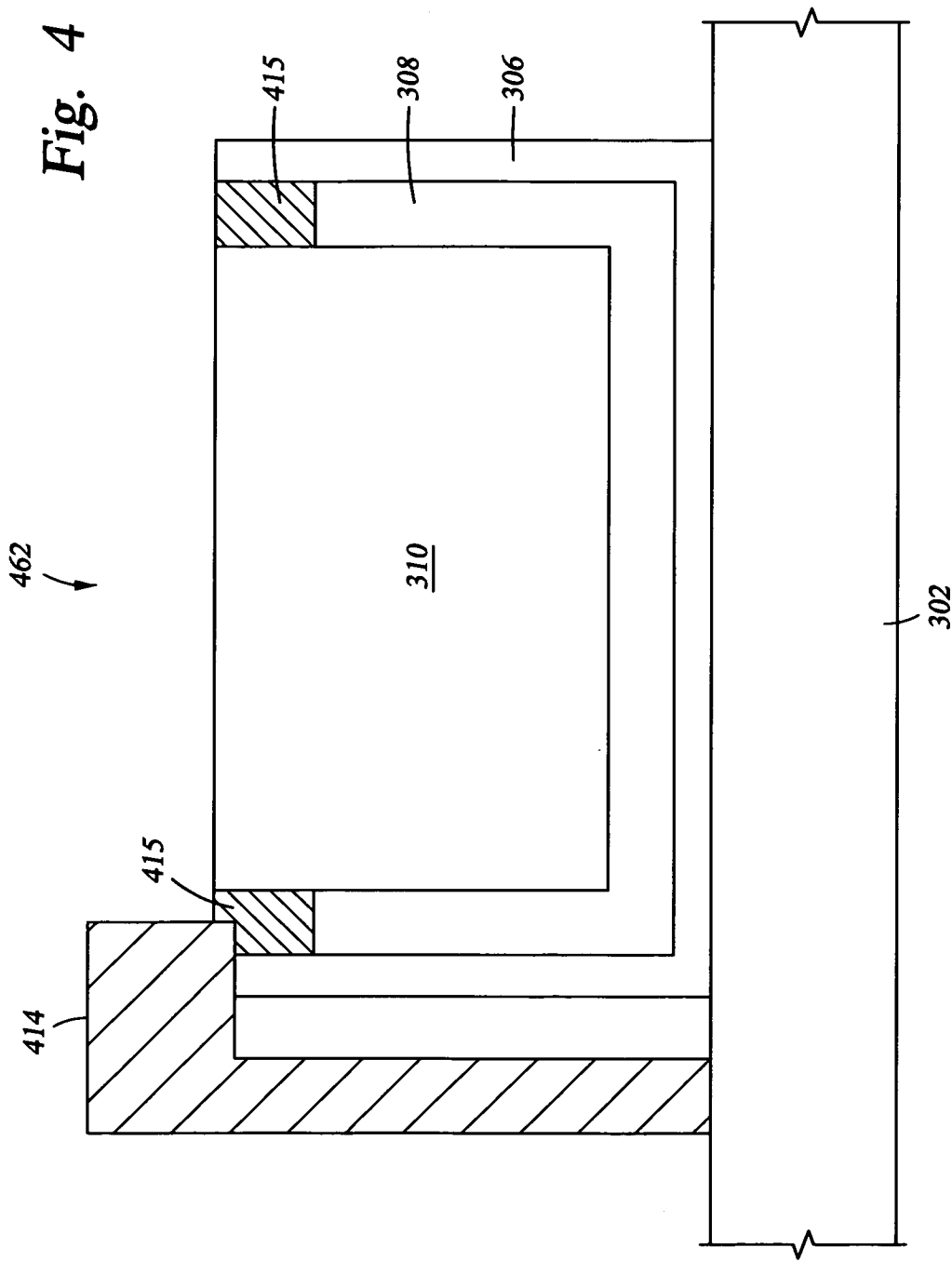


Fig. 3E

Fig. 3F

Fig. 3G

Fig. 3H



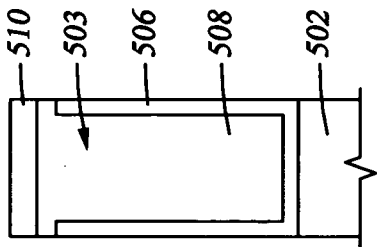


Fig. 5A

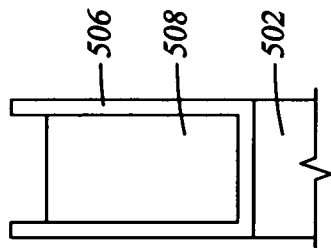


Fig. 5B

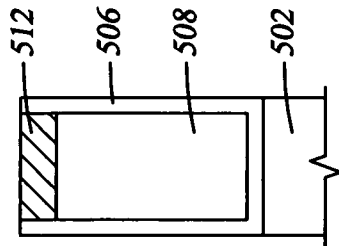


Fig. 5C

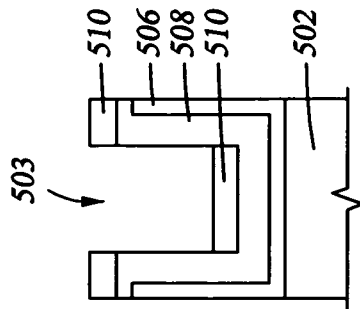


Fig. 5D

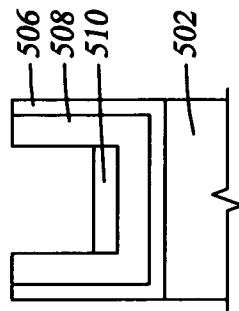


Fig. 5E

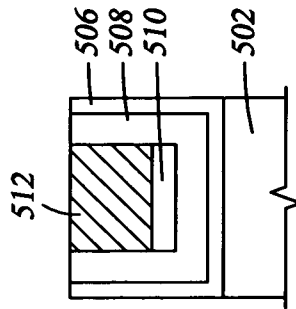


Fig. 5F

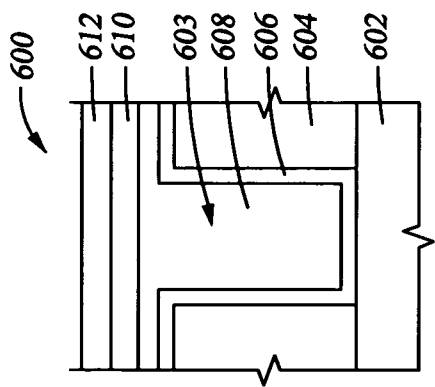


Fig. 6A

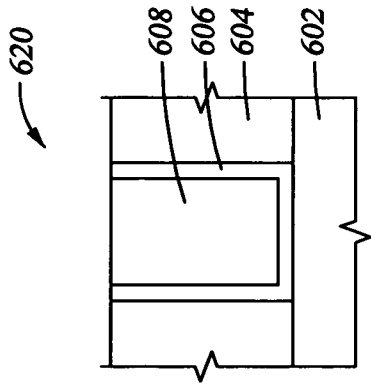


Fig. 6B

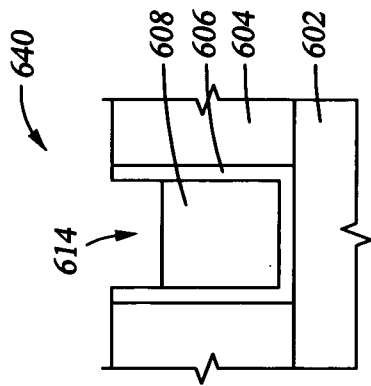


Fig. 6C

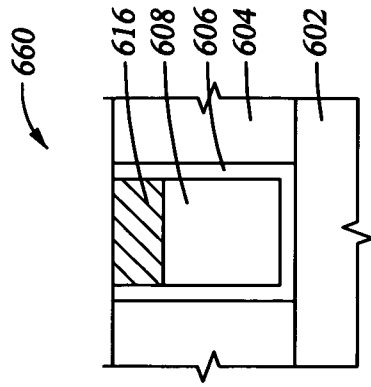


Fig. 6D

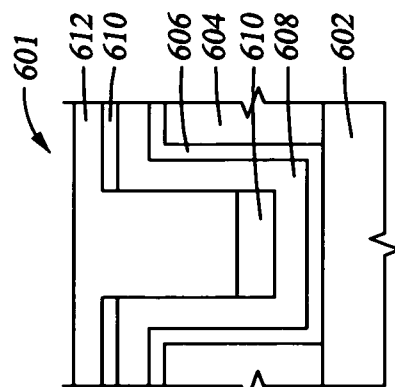


Fig. 6E

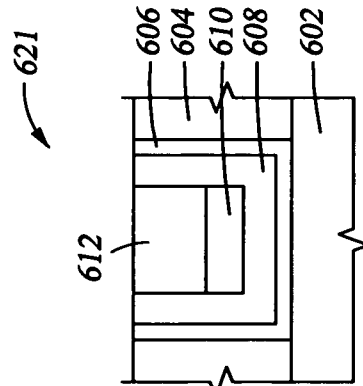


Fig. 6F

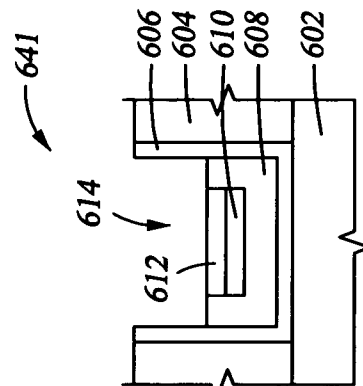


Fig. 6G

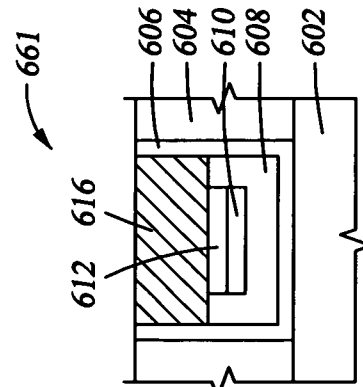


Fig. 6H

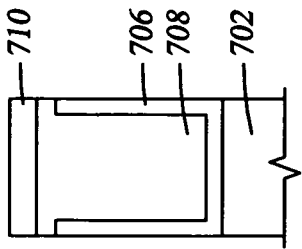


Fig. 7A

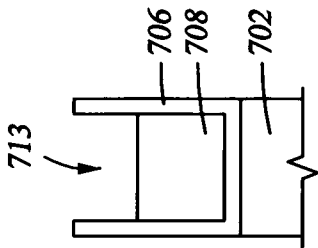


Fig. 7C

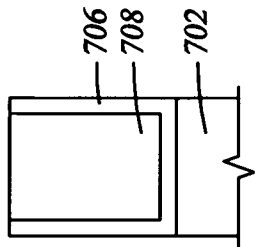


Fig. 7B

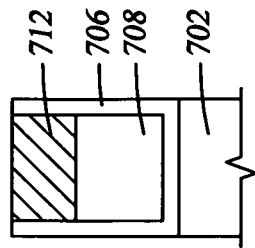


Fig. 7D

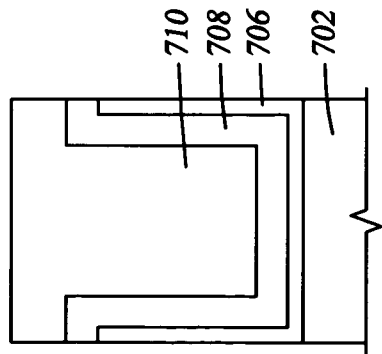


Fig. 7E

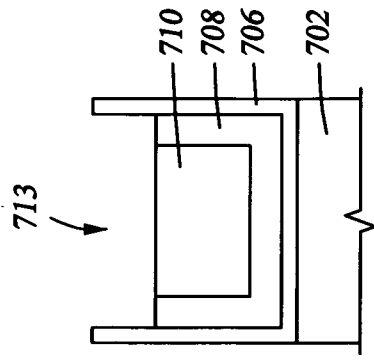


Fig. 7G

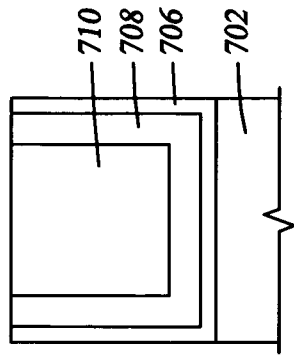


Fig. 7F

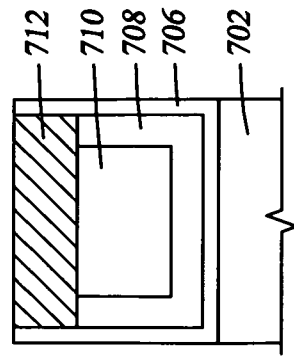


Fig. 7H

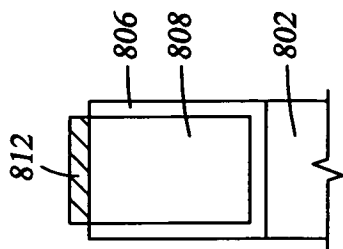


Fig. 8C

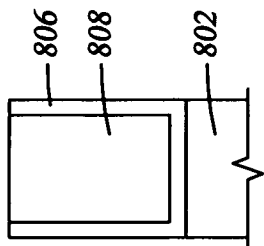


Fig. 8B

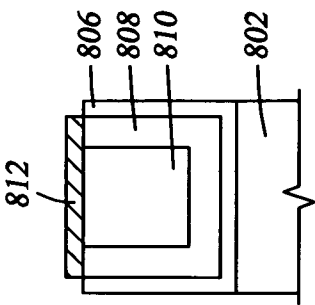


Fig. 8F

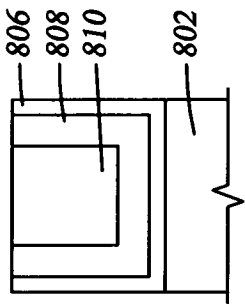


Fig. 8E

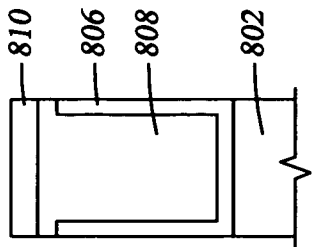


Fig. 8A

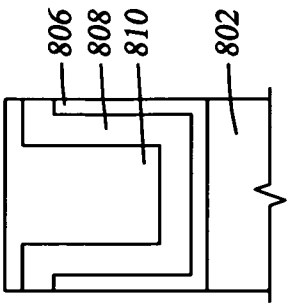


Fig. 8D

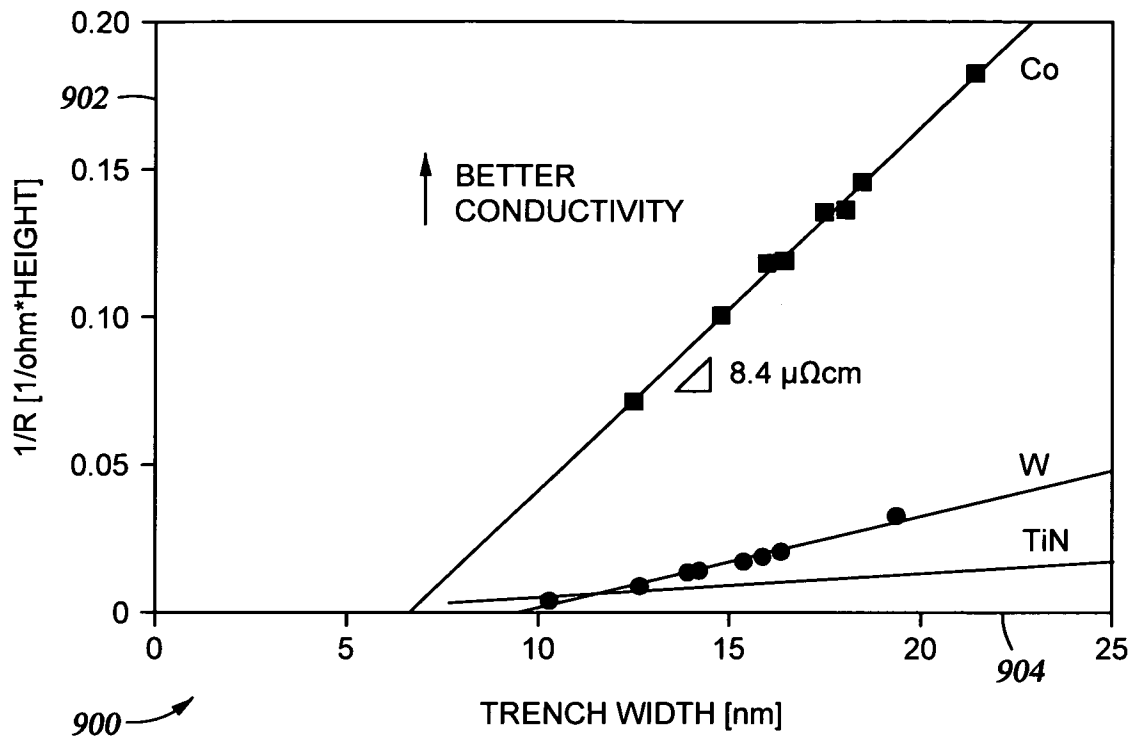


Fig. 9A
(PRIOR ART)

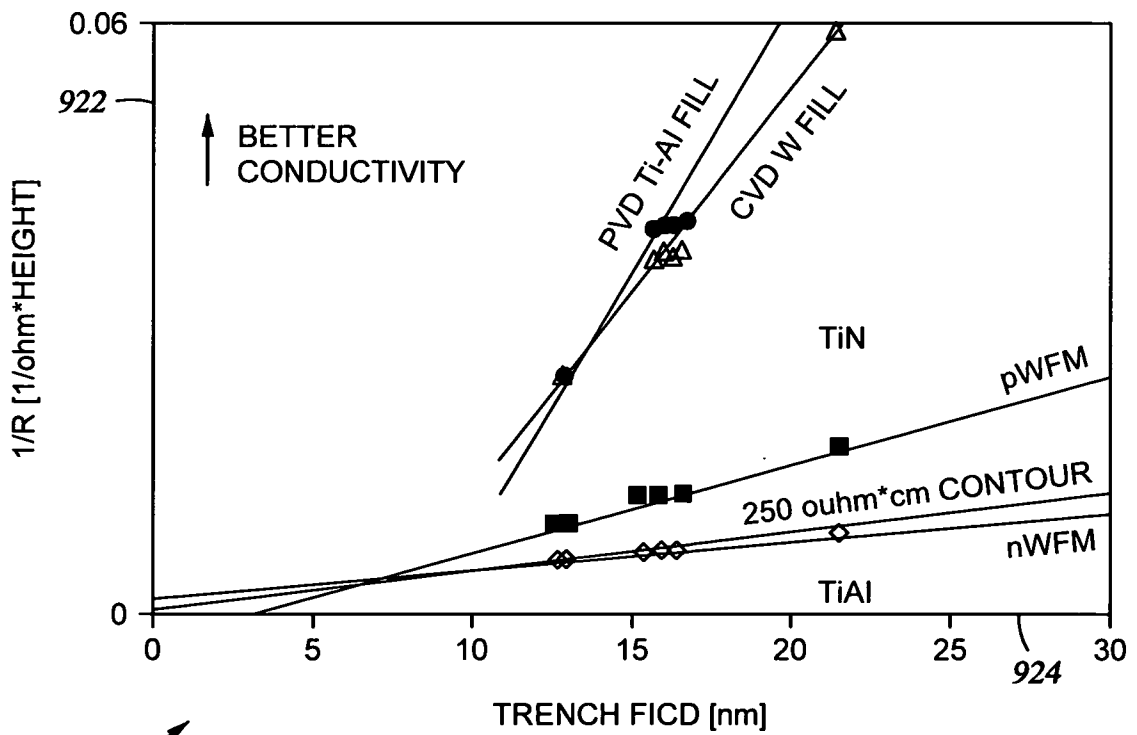


Fig. 9B

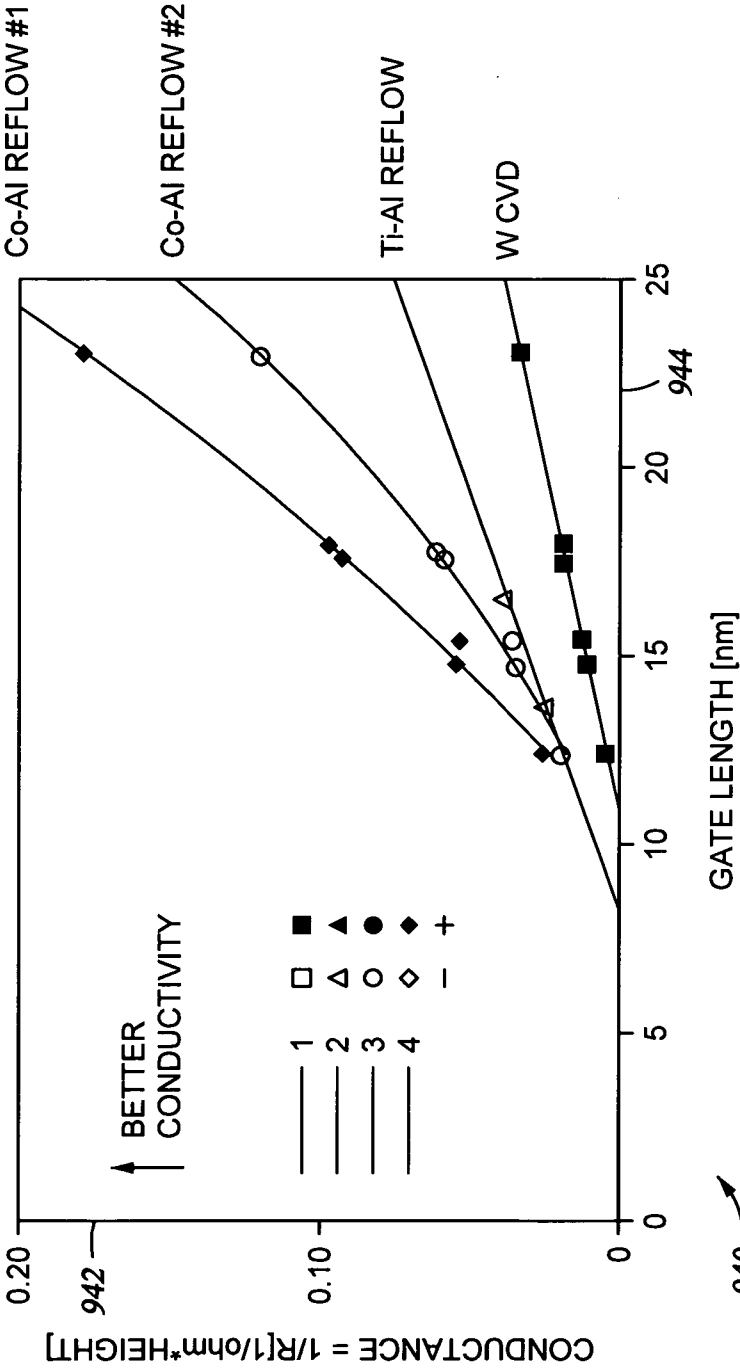


Fig. 9C

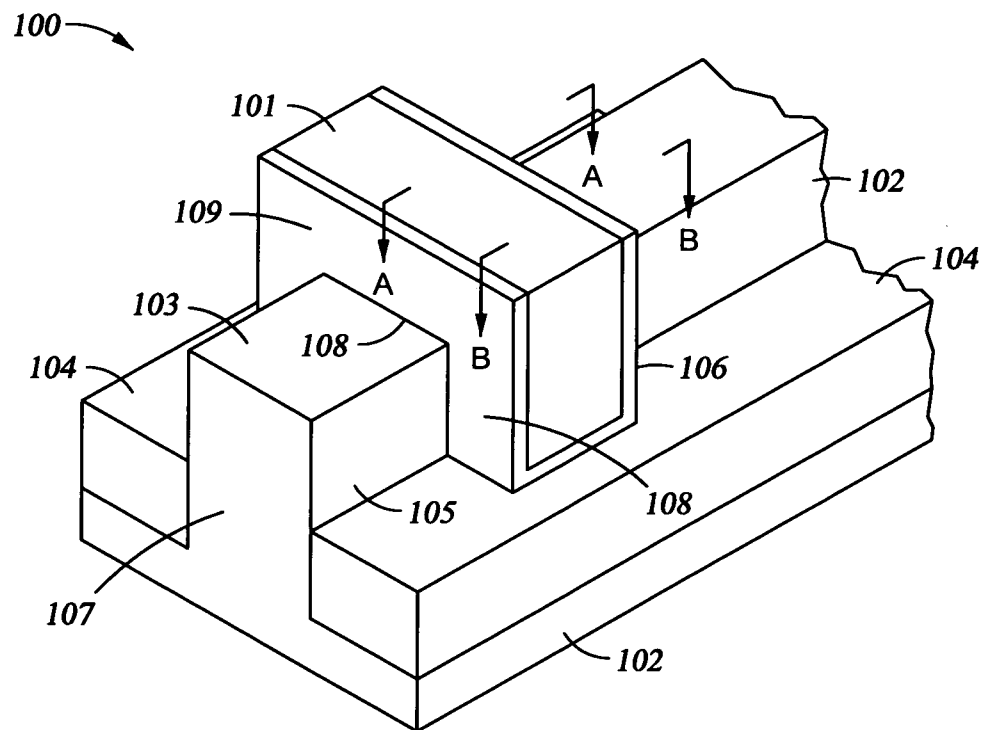


Fig. 1A

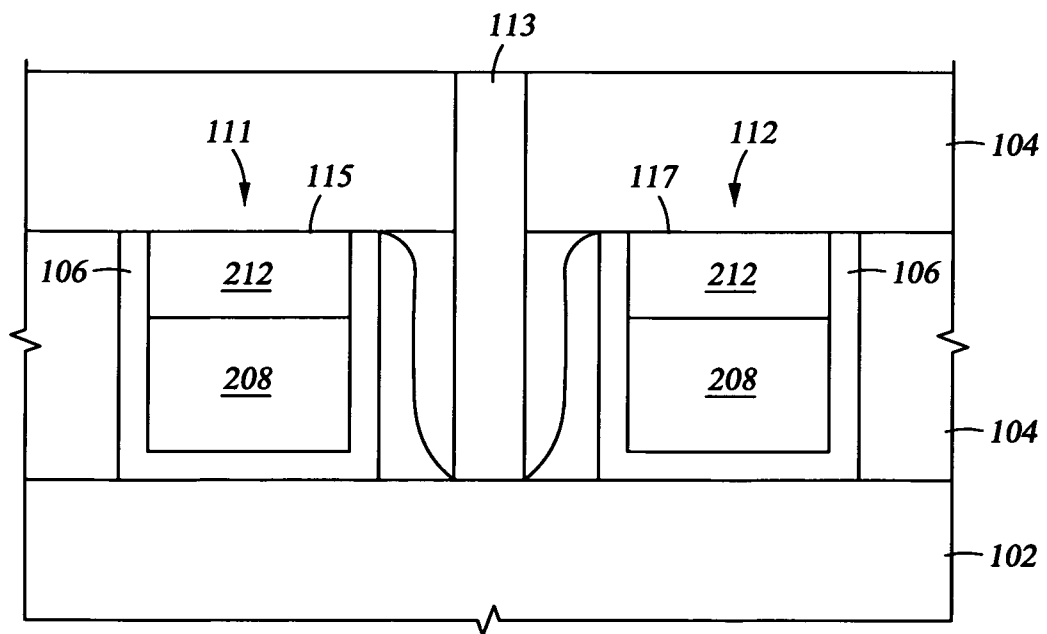


Fig. 1B

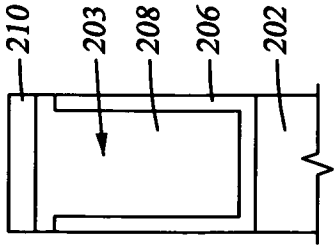


Fig. 2A

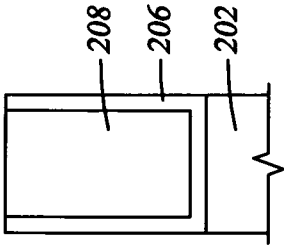


Fig. 2B

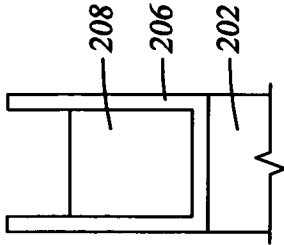


Fig. 2C

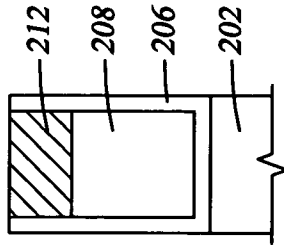


Fig. 2D

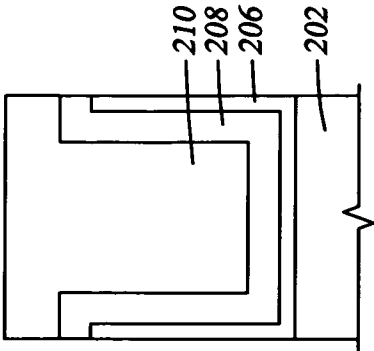


Fig. 2E

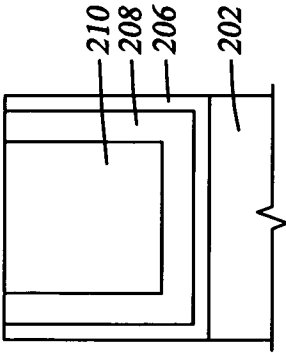


Fig. 2F

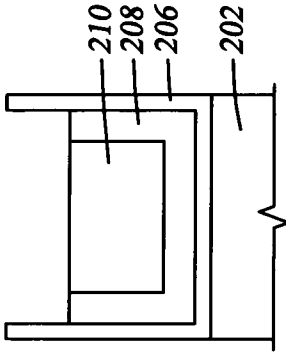


Fig. 2G

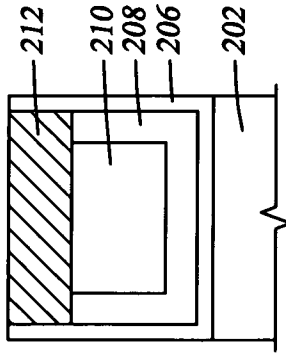


Fig. 2H

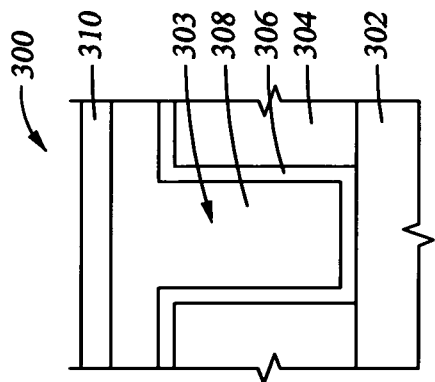


Fig. 3A

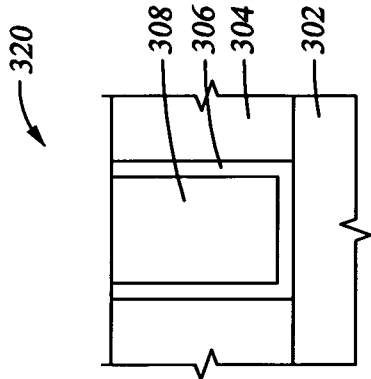


Fig. 3B

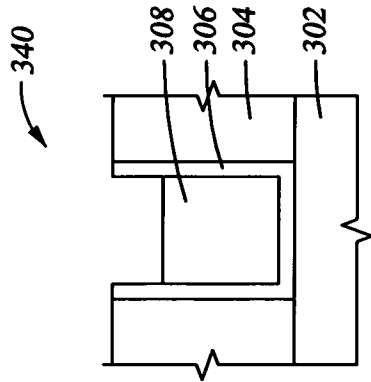


Fig. 3C

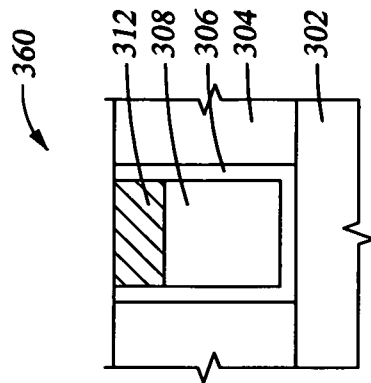


Fig. 3D

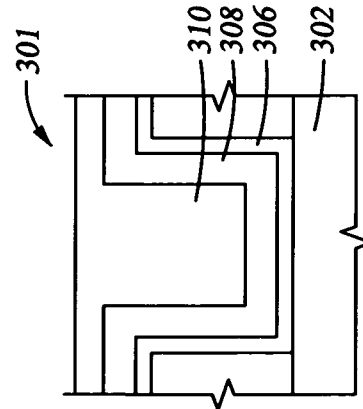


Fig. 3E

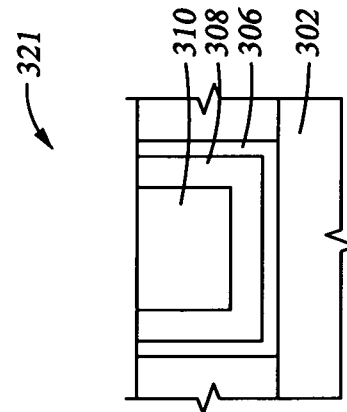


Fig. 3F

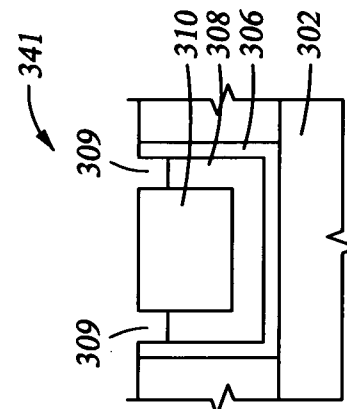


Fig. 3G

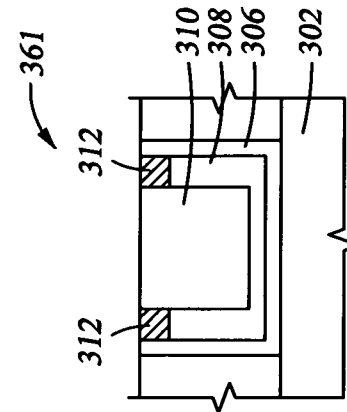
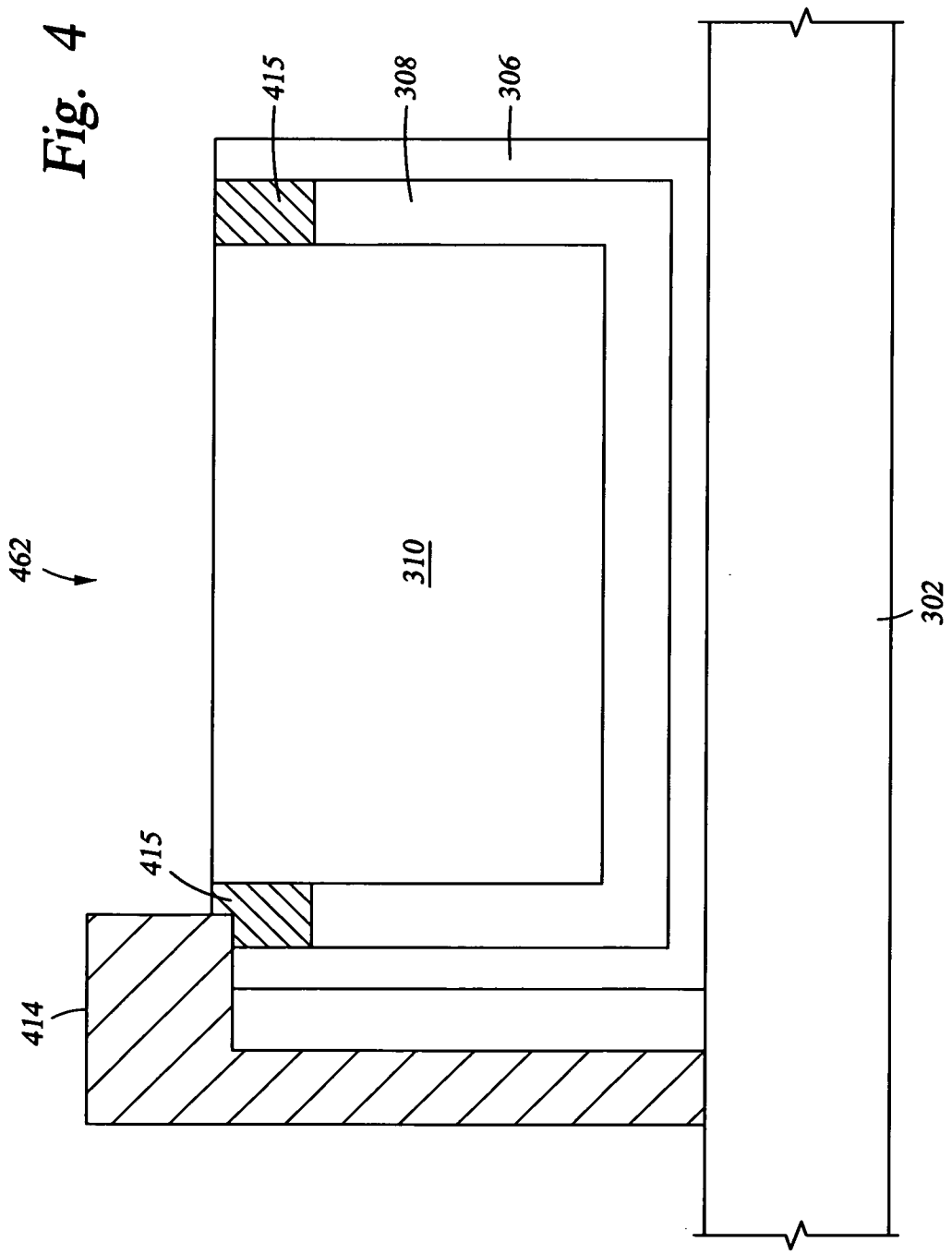


Fig. 3H



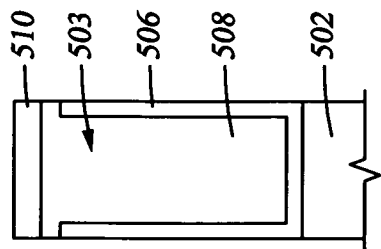


Fig. 5A

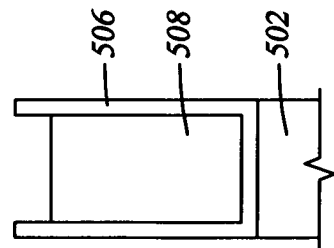


Fig. 5B

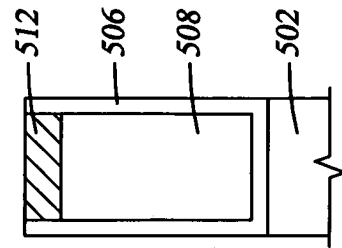


Fig. 5C

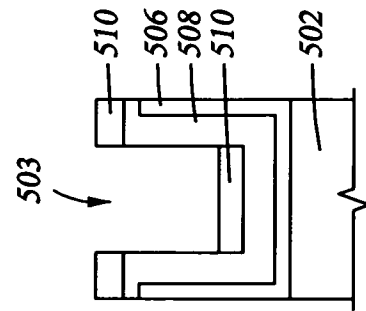


Fig. 5D

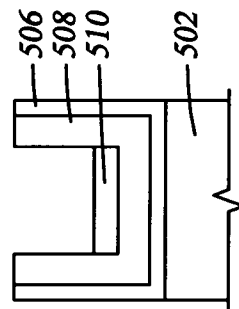


Fig. 5E

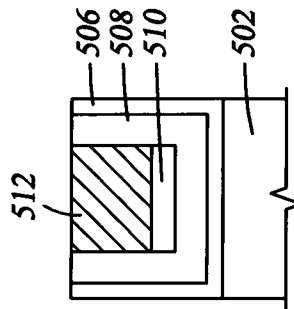


Fig. 5F

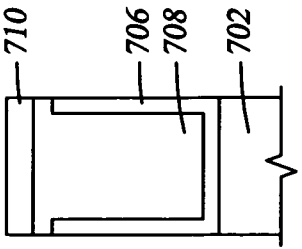


Fig. 7A

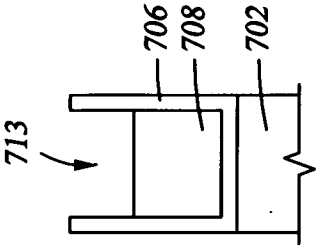


Fig. 7C

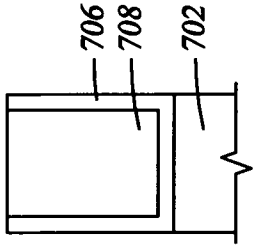


Fig. 7B

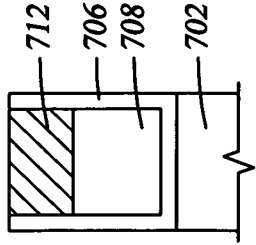


Fig. 7D

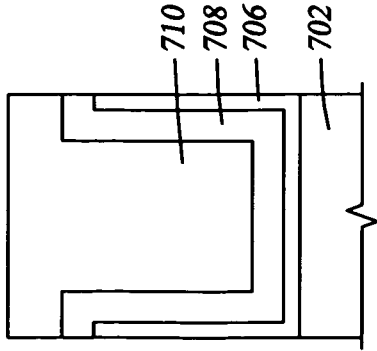


Fig. 7E

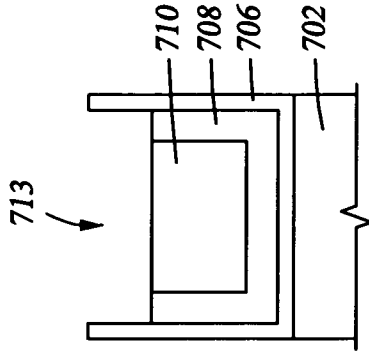


Fig. 7G

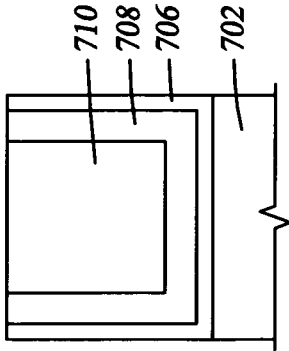


Fig. 7F

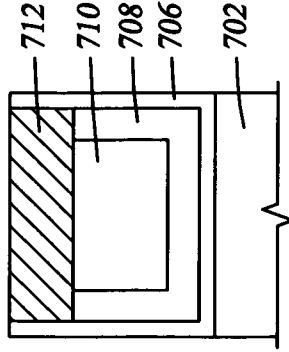


Fig. 7H

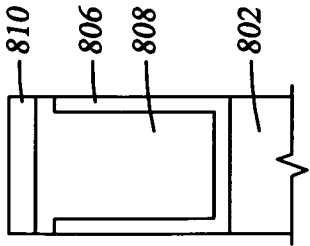


Fig. 8A

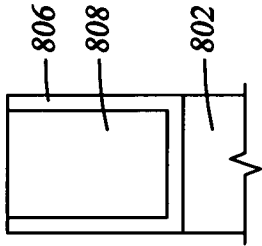


Fig. 8B

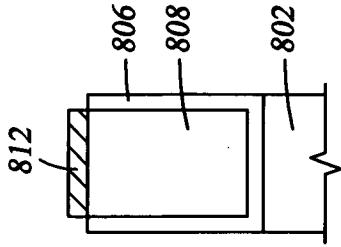


Fig. 8C

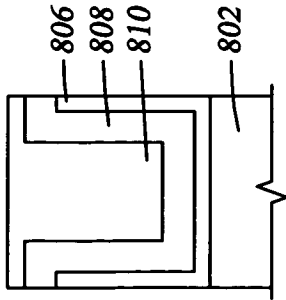


Fig. 8D

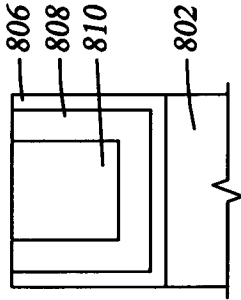


Fig. 8E

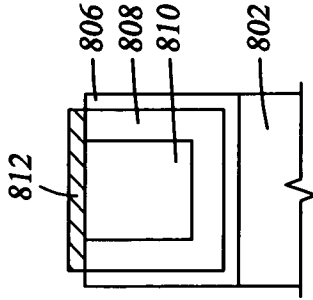


Fig. 8F

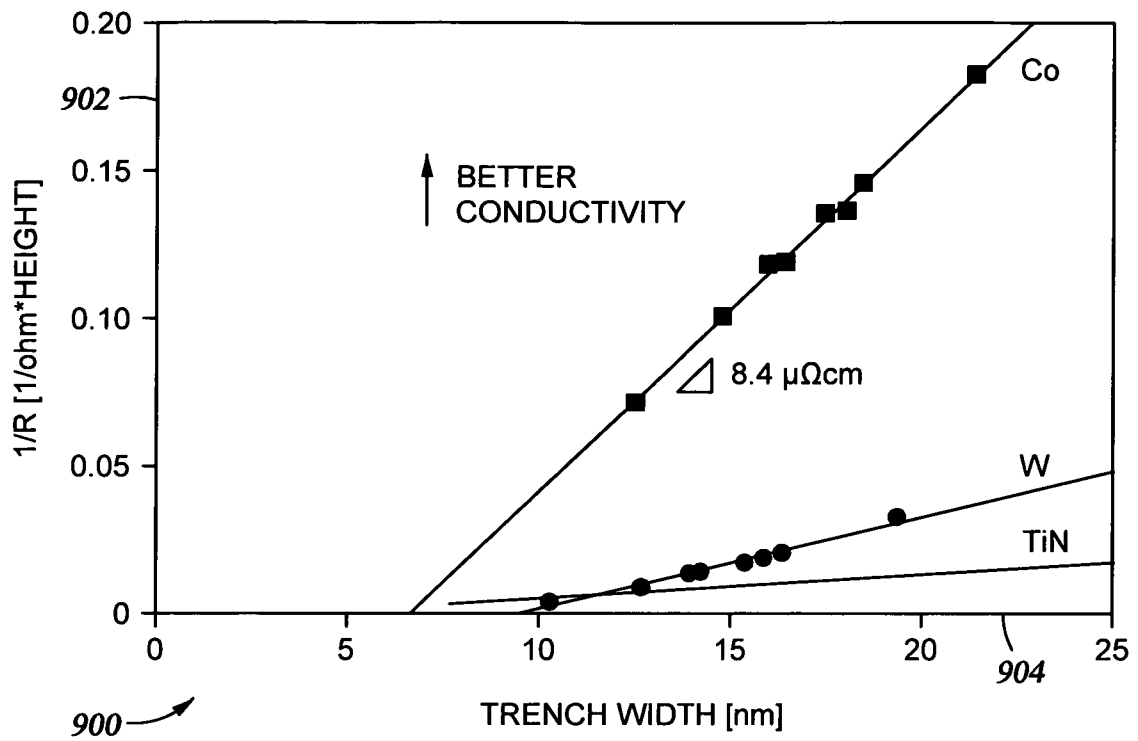


Fig. 9A

(PRIOR ART)

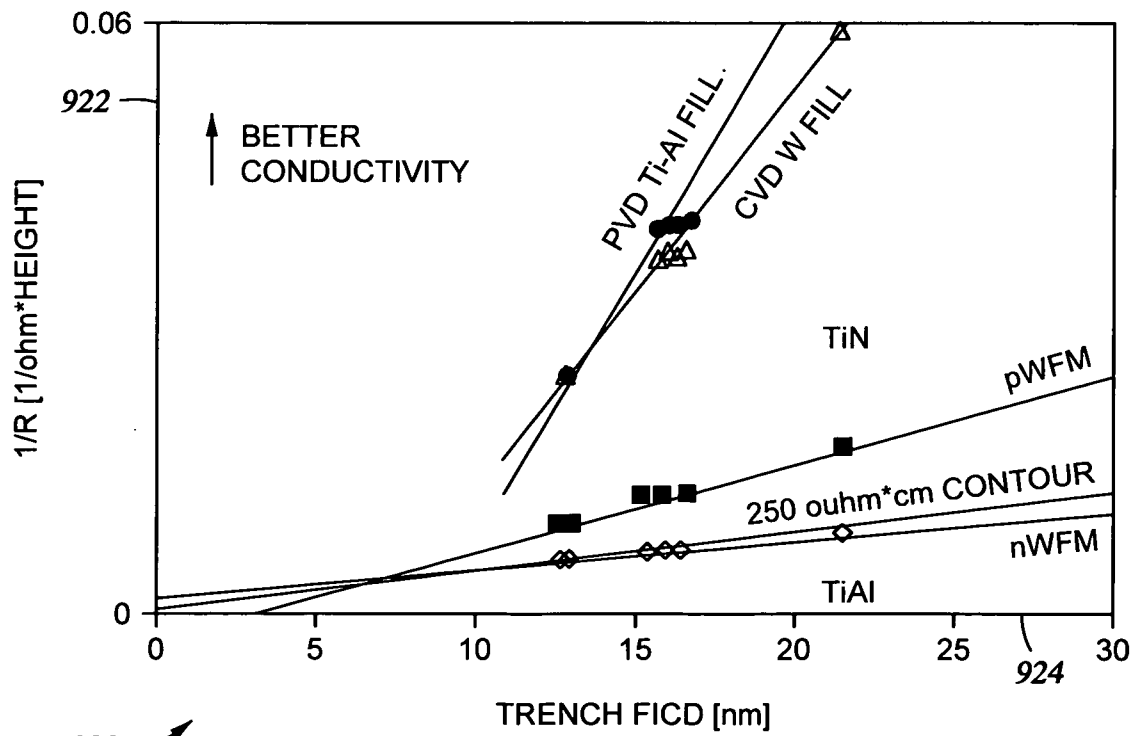
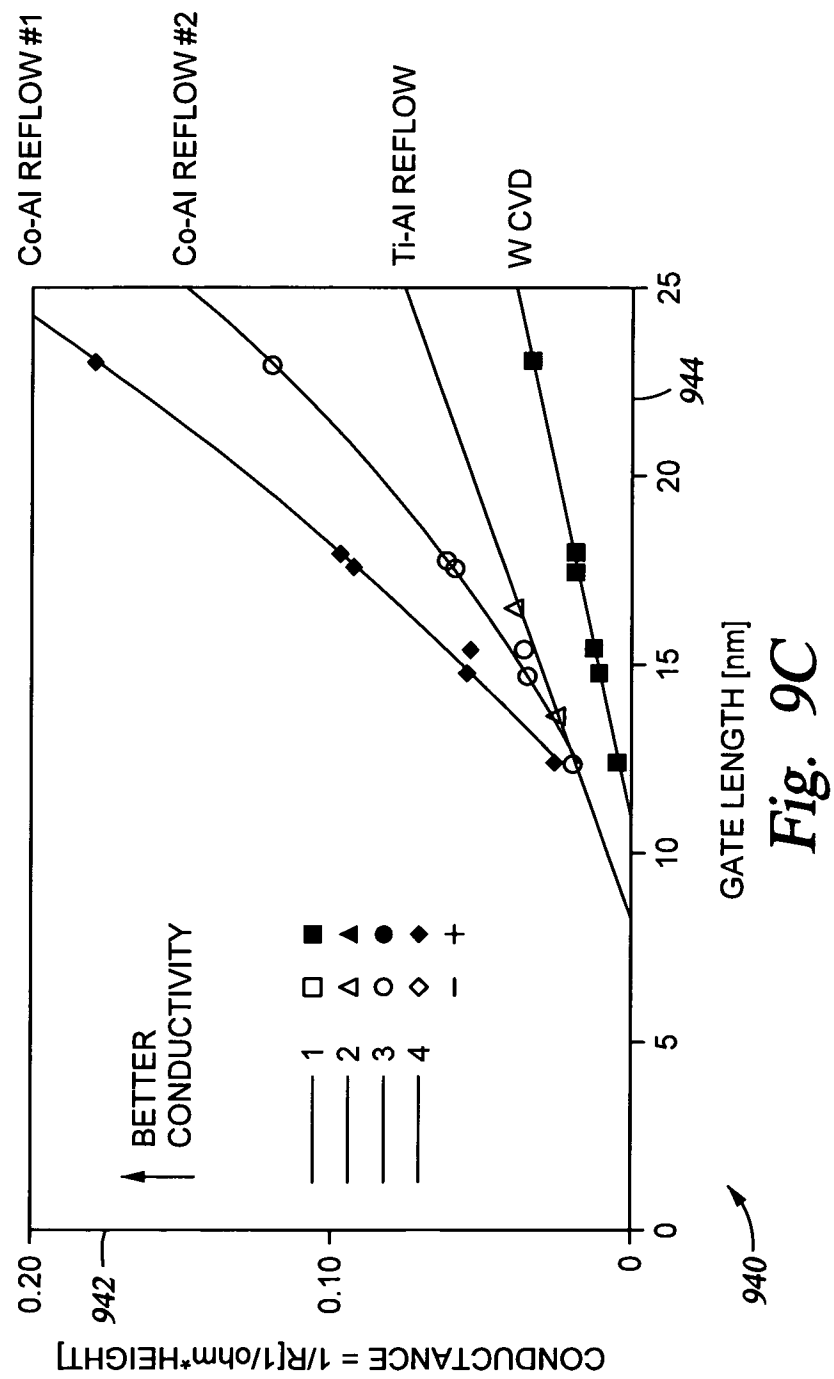


Fig. 9B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/000024**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/336(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/336; H01L 21/302; H01L 27/115; G05F 3/02; H01L 21/20; H01L 27/088; H01L 21/28; H01L 29/78; H01L 21/8247; H01L 29/423

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: gate, trench, lower, upper, layer, diffusion, barrier, metal, high, conductivity, second, channel, length

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0240204 A1 (MATT YEH et al.) 23 September 2010 See abstract, paragraphs [0016]-[0045] and figures 1-21.	1-3
Y	US 2009-0212854 A1 (BAUMGARTNER PETER) 27 August 2009 See abstract, paragraphs [0046]-[0053] and figures 8a-8e.	6
Y	US 2013-0015580 A1 (SAMEER H JAIN et al.) 17 January 2013 See abstract, paragraphs [0020]-[0035] and figures 2-15.	6
A	US 2005-0051854 A1 (CYRIL CABRAL JR. et al.) 10 March 2005 See abstract, paragraphs [0040]-[0054] and figures 7-10.	1-5
A	KR 10-2013-0007178 A (SK HYNIX INC.) 18 January 2013 See abstract, paragraphs [0017]-[0041] and figures 2a-4.	6-13
A	US 2012-0292715 A1 (HYUNG-SEOK HONG et al.) 22 November 2012 See abstract, paragraphs [0110]-[0137] and figures 24-31.	6-13



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

25 July 2014 (25.07.2014)

Date of mailing of the international search report

25 July 2014 (25.07.2014)

Name and mailing address of the ISA/KR

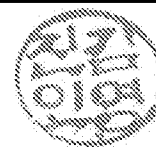
International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

KIM, Young Jin

Telephone No. +042 481 5771



INTERNATIONAL SEARCH REPORTInternational application No.
PCT/US2014/000024**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Group 1, claims 1-5 are directed to a filled gate structure comprising a trench filled with a combination of layers including at least one lower layer of a diffusion barrier/work function metal-containing material and at least one upper layer of a metal or metal alloy having a high conductivity.

Group 2, claims 6-13 are directed to a method of forming a filled gate structure, the method comprising: forming FETs having more than one channel length simultaneously on a single substrate, wherein a first channel length is 15 nm or less, and at least one additional channel length ranges between more than 15 nm to about 60 nm..

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/000024

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0240204 A1	23/09/2010	CN 101901762 A CN 101901762 B US 8268085 B2	01/12/2010 04/04/2012 18/09/2012
US 2009-0212854 A1	27/08/2009	DE 102009000624 A1 US 08067287 B2 US 08377778 B2 US 08432004 B2 US 08597999 B2 US 2012-025325 A1 US 2012-042296 A1 US 2013-167097 A1	05/11/2009 29/11/2011 19/02/2013 30/04/2013 03/12/2013 02/02/2012 16/02/2012 27/06/2013
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KR 10-2013-0007178 A	18/01/2013	None	
US 2012-0292715 A1	22/11/2012	KR 10-2012-0128531 A	27/11/2012