

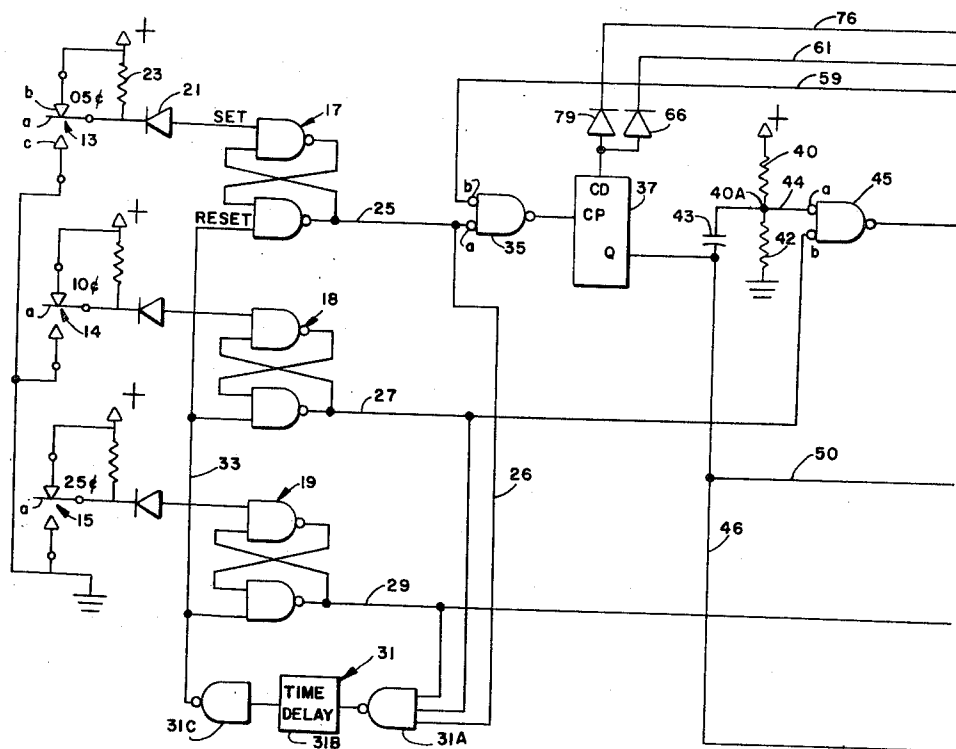
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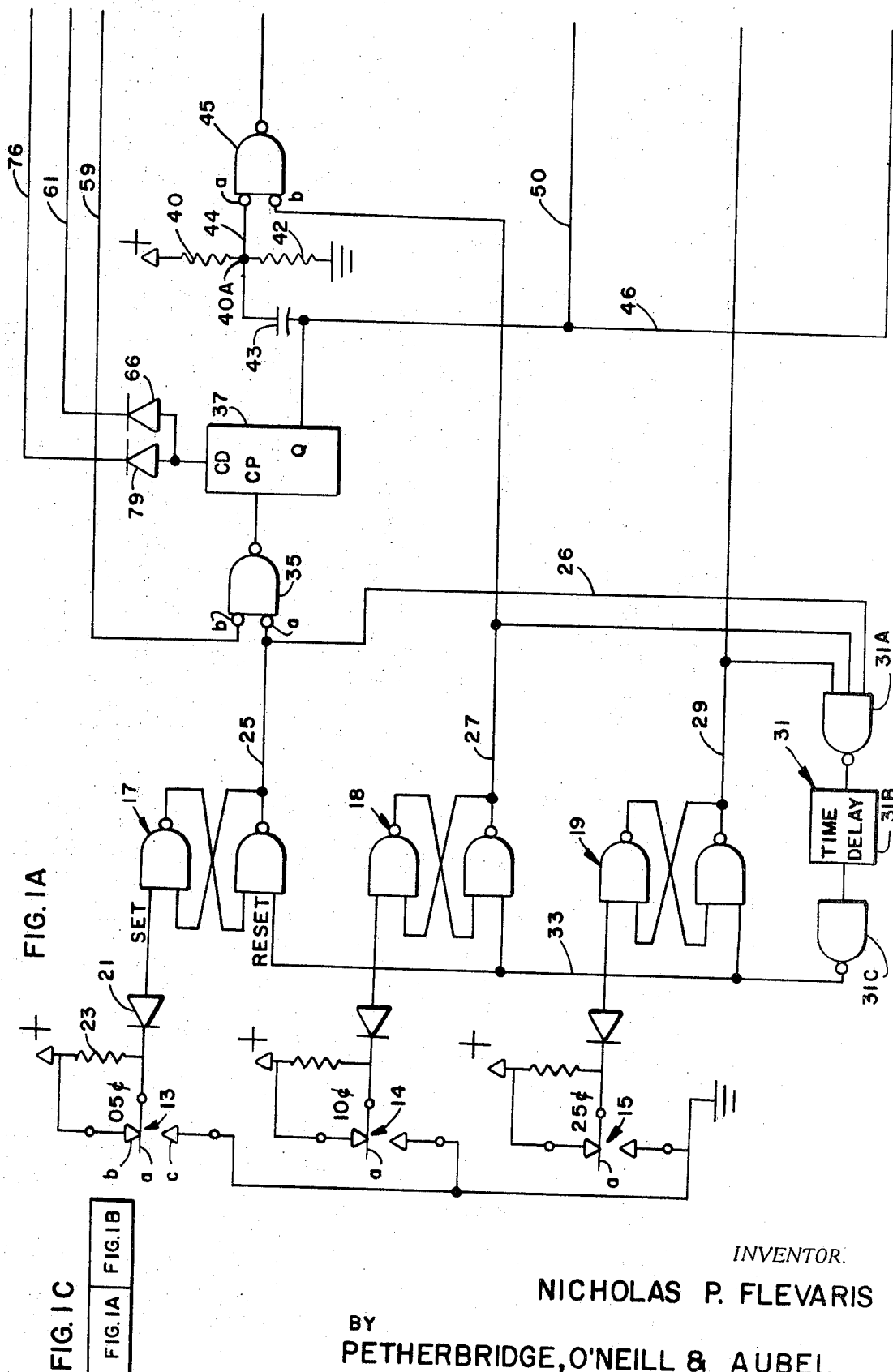
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[54] **COIN COUNTING AND REGISTERING CIRCUIT**
10 Claims, 3 Drawing Figs.

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ABSTRACT: A coin counting and registering circuit is disclosed which accumulates inputs representing the insertion or introduction of coins of different denominations to indicate that a selected total has been accumulated.





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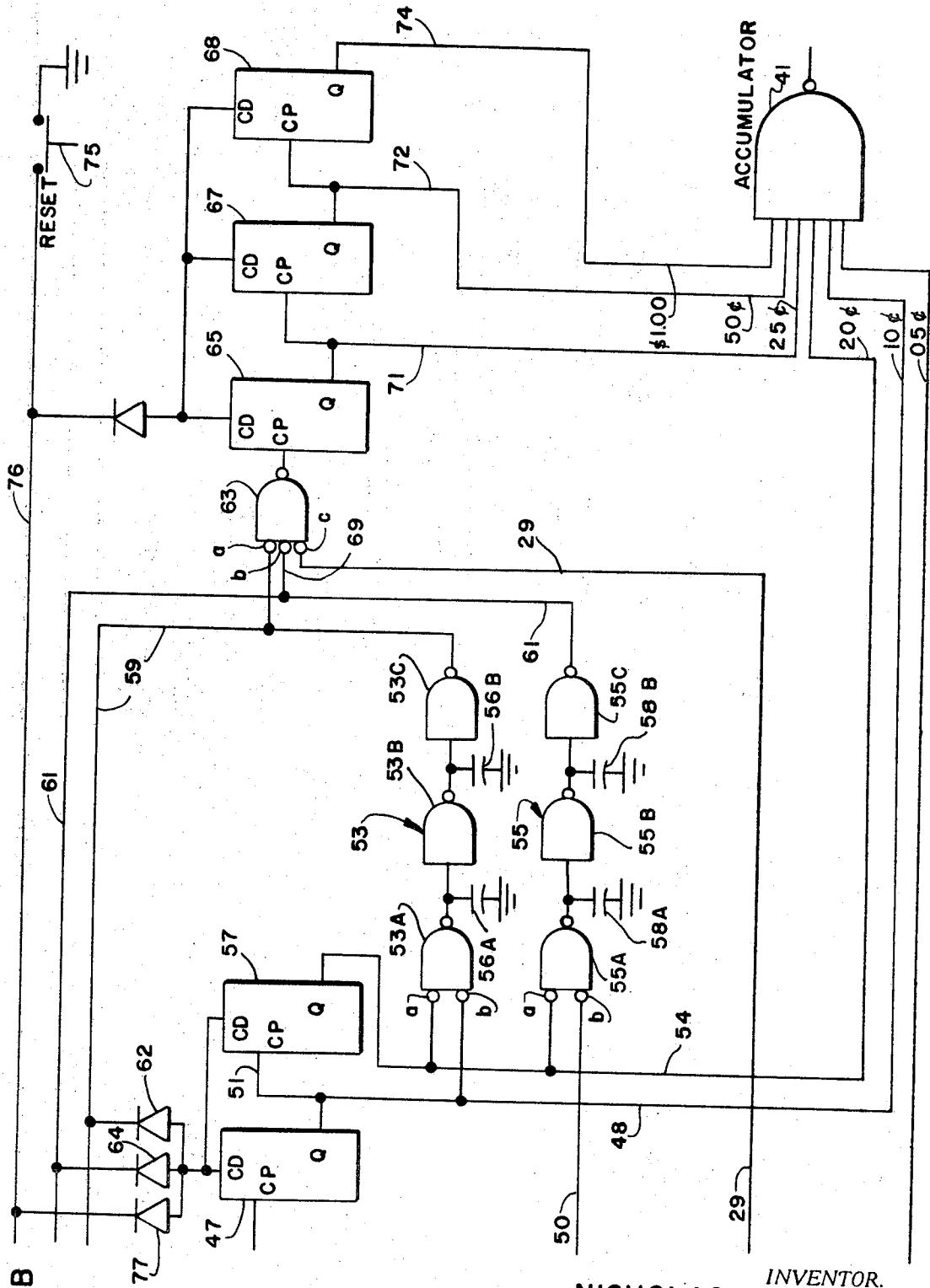


FIG. 1B

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COIN COUNTING AND REGISTERING CIRCUIT

Prior art coin registering circuits utilize mechanical switches which have the disadvantage that when the switches are operated by the insertion of a coin, the system often registers an erroneous count. More specifically, such mechanical switches utilize a contact arm movable between an "OFF" terminal and an "ON" terminal. This movable arm is actuated away from its "OFF" terminal in response to the insertion of a coin in the associated slot and moves across a gap to make contact with the "ON" terminal. Due to its momentum, the arm may bounce or vibrate. The bounce of the contact arm is often sufficient to momentarily break the electrical connection and then to again momentarily reestablish the connection. Such a make-break-make action may be repeated several times. Consequently, if such a mechanical switch is used as input to the electronic circuit, each mechanical operation of the switch may be erroneously interpreted by the associated electronic circuitry to be several operations, thereby indicating that several coins have been inserted into the system.

As is obvious, the insertion of one coin should result in a given mechanical operation which in turn provides only one electrical pulse to the electronic circuitry.

The present invention solves the foregoing problem and assures each given mechanical operation always results in the production of only one electric pulse to thereby provide a correct count of registration of the coins inserted into the associated slot.

Further, prior art coin registering circuits are complex, complicated, unreliable and generally do not meet the requirements of the industry. The present invention provides a relatively simplified coin counting and registering circuit which has been found to be reliable and to meet present industry requirements.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings wherein:

FIGS. 1A and 1B show the coin counting and registering circuit according to the invention; and

FIG. 1C shows the relative orientation of FIGS. 1A and 1B.

Referring to FIGS. 1A and 1B, the invention comprises suitable known mechanical switches 13, 14 and 15 which are operatively connected to a suitable receptacle or slot, not shown, to indicate the insertion of the proper coin therein. Switches 13, 14 and 15 are essentially identical, with switch 13 being operated by the insertion of a coin of a selected denomination, say 5 cents, in the associated slot, switch 14 being operated by the insertion of a coin of a second selected denomination, say 10 cents, therein, and switch 15 being operated by the insertion of a coin of a third selected denomination, say 25 cents, in the slot.

For purposes of illustration, switches 13, 14 and 15 are each shown as a two-position switch having a movable arm *a*. Since the operation of each of the switches 13, 14 and 15 is essentially identical, only the operation of switch 13 need be described in detail.

The movable arm *a* of switch 13 is connected through a resistor 23 to the positive terminal of a suitable source of potential. Stationary contact *b* of switch 13 is connected to the positive terminal of the source, and stationary contact *c* is connected to ground reference. The contact arm *a* is also connected through a diode 21 to a latch circuit 17, of any suitable known type. Diode 21 has its cathode connected through resistor 23 to the positive potential and its anode connected to latch 17.

As is known, latch circuit or latch 17, as well as each of latch circuits 18 and 19 which are essentially identical thereto, is a binary storage device settable in either of two stable states. Each latch has a set and a reset input conductor. When a signal is applied to the set input conductor, the latch is set in one of its bistable states. Further signals applied to the set input conductor will not change the state of the latch. However, a signal applied to the reset input conductor will cause the latch to shift to its original bistable state.

In the initial or "normal" condition of the circuit, the movable arm *a* of switch 13 rests against contact *b*. When a coin is inserted in the associated slot, the movable arm *a* is caused to move across the gap and engage contact *c*, thereby connecting ground reference to the set input lead of latch circuit 17. When the set input lead of latch 17 is connected to ground reference, the voltage on the output lead 25 of latch 17 goes relatively lower. This lower voltage on the output lead 25 is coupled as an input to terminal *a* of gate 35 for a flip-flop circuit 27, as will be described.

Note that in the following description the terms high voltage or signal and low voltage or signal refer herein to relative voltage signal levels as is conventional when describing circuits operating in binary or at "two-voltage" levels.

The low voltage on lead 25 is also coupled, essentially as a feedback control, through lead 26 to a time delay circuit generally labeled 31, of any suitable known type, and which includes gates 31A and 31C and an adjustable time delay circuit 31B. The time delay of the delay circuit 31 is adjusted to be longer than the time required for mechanical switches 13, 14 and 15 to terminate any bouncing action. Moreover, the time delay of delay circuit 31 is shorter than the time required to initiate a succeeding operation of the same switch, such as by the insertion of two similar coins one right after the other, into the associated slot. Thus, the movement of the arm *a* to stationary contact *c* provides electrical pulses to set latch 17, and latch 17 once set remains in its set position until it is reset by the time delay circuit 31. Thus, latch 17 provides only one electrical pulse output as a result of a coin being inserted to activate switch 13. Any bouncing action by the movable arm *a* of switch 13 is isolated by latch 17 and is prevented from affecting the operation of the remaining circuitry of FIGS. 1A and 1B.

After the adjusted period of time delay established by the time delay circuit 31, a feedback pulse is provided through lead 33 to reset latch 17 to its initial condition. Latch 17 will now be responsive to the insertion of a succeeding coin and the actuation of switch 13.

As mentioned above, the output of latch circuit 17 is connected through lead 25 to terminal *a* of electronic gate 35 of any suitable known design. Gate 35 drives the clock of a suitable known type flip-flop 37 which is connected and biased such that the input voltage at its terminal CD is normally low, and the voltage at its output terminal Q is normally low.

When latch 17 is shifted to a set condition, a low voltage is provided to terminal *a* of gate 35 which gate inverts the signal and provides a high voltage to terminal CP of flip-flop 37. When latch 17 is reset, the signal on lead 25 goes high causing the output from gate 35 to return to a low voltage. This high to low voltage excursion at the output of gate 35 is coupled to flip-flop 37 to reverse the flip-flop 37. Thus, when a coin actuates switch 13, flip-flop 37 will reverse states, and its output terminal Q will go high and provide a signal through lead 46 to the accumulator 41 which provides an accumulation or indication that a 5 cent coin has been inserted in the slot.

For purposes to be explained herein below, the output from terminal Q of flip-flop 37 is also coupled through lead 50 to terminal *b* of a gate 55A.

Now assume that a second 5 cent coin is inserted in the slot, and actuates switch 13. Latch 17 will again shift states and couple a voltage through lead 25 and gate 35 to cause flip-flop 37 to change its conducting state thereby causing the output from terminal Q of flip-flop 37 to return to a low level.

Terminal Q of flip-flop 37 is connected through a series capacitor 43 (and lead 44) to terminal *a* of a gate 45. The junction of capacitor 43 and terminal *a* of gate 45 is also connected to the junction point 40A of resistors 40 and 42 which resistors are connected between ground and a positive potential. In the quiescent state the junction point 40A is arranged to be at a normally high voltage level. Gate 45 also functions to invert the input thereto.

In operation, when terminal Q of flip-flop 37 goes from a low to a high level, an instantaneous positive pulse will be coupled through capacitor 43 to terminal *a* of gate 45 which will,

however, not affect the operation of the circuit. On the other hand, the transition of terminal Q of flip-flop 37 from a high to a low level causes a negative pulse to be developed at point 40A. This negative pulse is coupled to terminal a of gate 45 thereby causing a positive pulse to be provided to terminal CP of a second flip-flop 47 which causes flip-flop 47 to shift states and provide a high voltage at its terminal Q. Thus, a pulse is coupled from terminal Q of flip-flop 37 to cause flip-flop 47 to change conducting states to indicate two 5 cent coins, that is, to indicate that a total of 10 cent has been inserted in the associated slot. When terminal Q of flip-flop 37 goes low, the input from lead 46 to accumulator 41 is low, that is, effectively canceled; hence, the accumulator records a total of 10 cents.

Note that a positive going excursion of a pulse primes the flip-flops 37, 47, 57, etc., and the negative going excursion of the pulse triggers the flip-flops to change conducting states. Thus, a positive voltage on terminal Q of flip-flop 47 will prime flip-flop 57, but will not change its conducting state and hence will not change the voltage at terminal Q of flip-flop 57. At this point, and as mentioned above, the voltage on terminal Q of flip-flops 37 and 57 is low and only the voltage on terminal Q of flip-flop 47 is high thereby providing a high voltage through lead 48 to the accumulator 41 which accumulates or indicates a total of 10 cents.

Assuming a third 5 cent coin is then inserted to actuate switch 13, flip-flop 37 will again shift states to provide a high output through its terminal Q and lead 46 to accumulator 41 to indicate a 5 cent coin. Thus, a high output on terminal Q of 37 and a high output from terminal Q of flip-flop 47 causes accumulator 41 to indicate a total of 15 cents.

Assume next, as an example, that a 10 cent coin is deposited to actuate switch 14, providing a positive going output pulse through latch 18, lead 27, terminal b of gate 45, and gate 45 to terminal CP of flip-flop 47. This pulse from latch 18 will cause flip-flop 47 to shift states and its terminal Q will go low. Note that flip-flop 57 was already primed since terminal Q of flip-flop 47 was previously high; and, when terminal Q of flip-flop 47 goes low, flip-flop 57 will shift states and its output terminal Q will go high.

The output from terminal Q of flip-flop 57 is coupled in parallel to suitable gate circuits generally labeled 53 and 55. The gate circuit 53 includes a two-input AND gate 53A and series connected signal shaping and inverting circuits 53B and 53C. A capacitor 56A is connected from the junction of AND gate 53A and circuit 53B to ground reference. Likewise, a capacitor 56B is connected from the junction of circuits 53B and 53C to ground reference. Capacitors 56A and 56B function to shape and extend the pulse inputs to AND gate 53A to thereby provide a pulse of sufficient length or duration from gate 53 through feedback lead 59 to assure that both flip-flops 37 and 47 are reset to an initial state in response to a pulse output from terminals Q of flip-flops 47 and 57.

Gate 53 also provides an input pulse through lead 59 to terminal a of NAND gate 63 to actuate the gate and couple a pulse to flip-flop 65, for purposes to be explained.

Gate circuit 55 is similar to gate circuit 53 and includes capacitor 58A and 58B which are connected the same as and function the same as capacitors 56A and 56B. Gate 55 provides a pulse of lead 61 when the terminal Q of both flip-flops 37 and 57 are high to reset flip-flops 37, 47 and 57. The pulse on lead 61 is also coupled through lead 69 to terminal b of gate 63 to actuate gate 63 and couple a pulse to terminal CP of flip-flop 65.

As mentioned above, when the 10 cent coin is deposited, switch 14 will actuate latch 18, flip-flop 47 will shift states and its terminal Q will go low thereby causing terminal Q of flip-flop 57 to go high. At this point, a high voltage will be coupled from terminal Q of flip-flop 57 to terminal a of AND gate 53A; however, a low voltage will be coupled from terminal Q of flip-flop 47 to terminal b of AND gate 53A; thus gate 53A will not pass a signal.

However, a high voltage will be coupled from terminal Q of flip-flop 57 to terminal a of AND gate 55A, and a high voltage

will be coupled from terminal Q of flip-flop 37 to terminal b of gate 55A. Thus, gate 55A will couple a signal pulse therethrough which pulse is extended and inverted by gate circuit 55. The output from gate circuit 55 is coupled through lead 61 to terminal b of a NAND gate 63 to cause gate 63 to couple a signal to change the state of flip-flop 65. Flip-flop 65 will now provide a high voltage from its terminal Q to lead 71 to accumulator 41 to indicate a 25 cent total.

As indicated above, the low signal on lead 61 is also coupled back through diode 64 to terminals CD of flip-flops 47 and 57 to reset these flip-flops to their initial condition with their output terminals Q at a low voltage. Likewise, the signal on lead 61 is coupled through lead 61 and diode 66 to terminal CP of flip-flop 37 to reset it to its initial condition with its terminal Q at a low voltage. Thus, at this point, leads 46, 48 and 54 are low and lead 71 is high, hence the accumulator 41 is indicating a total of 25 cents.

Assume now, as another example, that the accumulator total is 20 cents with terminals Q of flip-flops 37 and 47 being low and terminal Q of flip-flop 57 being high. Consider now that another 10 cent coin is inserted in the associated slot. This causes terminal Q of flip-flop 47 to go high. The terminals Q of flip-flops 47 and 57 are now high, and terminal Q of flip-flop 37 is low. Accordingly, a high signal will be coupled from terminal Q of flip-flop 47 through a terminal b of AND gate 53A and a high signal will be coupled from terminal Q of flip-flop 57 to terminal a of AND gate 53A. Gate 53A will thus pass a signal pulse which is extended and inverted by gate circuit 53 and coupled as a low signal through lead 59 to terminal a of gate 63 to actuate gate 63 to change the state of flip-flop 65. Thus, terminal Q of flip-flop 65 goes high to provide a signal on lead 71 to accumulator 41 to indicate the entry of 25 cents.

Note also that the signal on lead 59 is coupled back through diode 62 to terminals CD of flip-flops 47 and 57, respectively, causing the flip-flops 47 and 57 to reset to their initial state with their terminal Q at a low level.

Also, the signal on lead 59 is concurrently coupled back to terminal b of gate 35 to cause flip-flop 37 to shift conducting states and provide a high output from its terminal Q through lead 46 to accumulator 41. Thus, at this point, lead 46 from flip-flop 37 and lead 71 from flip-flop 65 are high thereby indicating 5' and 25 cents, respectively, which is accumulated as a 30 cent total by the accumulator 41.

Other examples of operation, in response to the insertion of different coin combinations, can be understood from the foregoing description.

Note also that the mechanical switch 15 is connected directly through latch circuit 19, lead 29 and gate 63 to flip-flop 65. Accordingly, when a 25 cent coin is deposited, switch 15 is actuated to provide a pulse through the circuit just traced causing flip-flop 65 to change states and provide a high output voltage at terminal Q of flip-flop 65, which output is coupled through lead 71 to indicate a 25 cent registration in accumulator 41.

Flip-flops 65, 67 and 78 of any suitable known type are connected in a known manner to operate in a binary fashion. More explicitly, flip-flop 67 is connected to change states once for every two operations of flip-flop 65 etc. Accordingly, a high output at terminal Q of flip-flop 67 indicates a 50 cent credit and a high output on flip-flop 68 indicates a \$1.00 credit.

As many flip-flops as required can be added similarly as flip-flops 65, 67 and 68 to operate in a binary fashion to increase the total amount that can be accumulated.

The circuit of FIGS. 1A and 1B can be reset to its initial condition by manually actuating the reset button 75 causing all the flip-flops to be reset through lead 76 and the respective diodes. Suitable automatic reset means as are well-known in the art such as, for example, means for resetting the circuit when a desired item has been dispensed, may also be provided.

It should, of course, be understood that coins of other denominations may be utilized to provide different accumulated totals as desired. Further, while the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood that by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

I claim:

1. A coin counting and registering or summing means comprising, in combination, means for receiving coins of various denominations and selectively providing electrical pulses in response thereto, a plurality of bistable means adapted to be set and reset to second and first stable operating states respectively in response to selective electrical pulses to provide binary output voltages and thereby give an indication of the reception of selected coins, network means including a capacitor and resistors for coupling an output voltage from the first bistable means to the second bistable means to set said second bistable means to its second stable state when said first bistable means is reset, said second bistable means having its output connected to the third bistable means, said third bistable means being set when said second bistable means is reset, first gate means for selectively receiving an output voltage from a first and a third of said bistable means to provide feedback voltages to reset said bistable means, second gate means for selectively receiving output voltages from said second and said third bistable means for providing feedback voltages to said first bistable means and to reset said second and third bistable means, and third gate means for receiving output voltages from said first and second gate means to actuate succeeding bistable means to thereby provide an accumulated total indication.

2. A coin counting and summing circuit as in claim 1 wherein said plurality of bistable means comprises three flip-flop units connected to operate in a bistable manner wherein each flip-flop is actuated to indicate a sum of twice the sum indicated by operation of the preceding flip-flop.

3. A coin counting and summing circuit as in claim 1 further including mechanical switch means actuatable to provide electrical pulses in response to the insertion of a coin in an associated slot, latch means coupled to said switch means and shiftable from a set to a reset operating condition to provide

output signals in response to electrical pulses received from said switch means, delay means coupled to receive output signals from said latch means and provide a time delayed pulse in response thereto, means to couple the output pulse from said delay means to reset said latch means to its initial condition, whereby said latch is shifted from a set to a reset condition in response to an electrical pulse received from said switch and remains in said condition until it is reset by a pulse from said delay means such that only one signal effective electrical pulse representative of the actuation of said mechanical switch means is provided in response to the insertion of a coin in the associated slot and any electrical pulses caused by bouncing of said mechanical switch are prevented from effecting the operation of the coin counting and summing circuit.

4. A coin counting and summing circuit as in claim 3 wherein three mechanical switches are provided each actuable respectively by a 5 cent, 10 cent and 25 cent coin, and wherein a pulse developed by each mechanical switch is directly coupled to a respective bistable means.

5. A coin counting and summing circuit as in claim 1 wherein said network means comprises a capacitor connected in series between said first and second bistable means, and resistor means connected across a source of potential and having an intermediate point of said resistor means connected to said capacitor.

6. A coin counting and summing circuit as in claim 1 wherein said gate means each comprise an AND gate and include capacitor means connected to said AND gate to shape and extend the output voltage pulse from said AND gate.

7. A coin counting and summing circuit as in claim 1 further including an accumulator for accumulating and recording the total sum of said coins.

8. A coin counting and summing circuit as in claim 7 wherein the output of each of said bistable means are also connected directly to said accumulator to thereby provide an indication of the reception of a coin directly to said accumulator.

9. A coin counting and summing circuit as in claim 1 further including a plurality of bistable means each connected to indicate a sum of twice that indicated by the preceding bistable means.

10. A coin counting and summing circuit as in claim 1 wherein means are provided to reset all of said bistable means concurrently.