



- (51) **International Patent Classification:**
H01L 31/0224 (2006.01) *H01L 31/18* (2006.01)
- (21) **International Application Number:**
PCT/US2014/071320
- (22) **International Filing Date:**
18 December 2014 (18.12.2014)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
14/137,610 20 December 2013 (20.12.2013) US
- (71) **Applicant:** SUNPOWER CORPORATION [US/US]; 77
Rio Robles, San Jose, California 95134 (US).
- (72) **Inventors:** AGRAWAL, Mukul; 4399 Peralta Boulevard,
Fremont, California 94536 (US). RIM, Seung; 1618 Sand
Hill Road, Apt. 319, Palo Alto, California 94304 (US).
CUDZINOVIC, Michael; 378 Balsam Avenue,
Sunnyvale, California 94085 (US).
- (74) **Agents:** VINCENT, Lester J. et al.; Blakely Sokoloff
Taylor & Zafman LLP, 1279 Oakmead Parkway,
Sunnyvale, California 94085 (US).

- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) **Title:** BARRIER-LESS METAL SEED STACK AND CONTACT

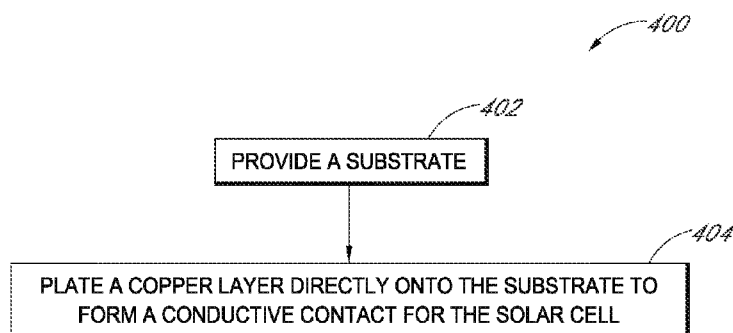


FIG. 4

(57) **Abstract:** Approaches for forming barrier-less seed stacks and contacts are described. In an example, a solar cell includes a substrate and a conductive contact disposed on the substrate. The conductive contact includes a copper layer directly contacting the substrate. In another example, a solar cell includes a substrate and a seed layer disposed directly on the substrate. The seed layer consists essentially of one or more non-diffusion-barrier metal layers. A conductive contact includes a copper layer disposed directly on the seed layer. An exemplary method of fabricating a solar cell involves providing a substrate, and forming a seed layer over the substrate. The seed layer includes one or more non-diffusion-barrier metal layers. The method further involves forming a conductive contact for the solar cell from the seed layer.

BARRIER-LESS METAL SEED STACK AND CONTACT

TECHNICAL FIELD

[0001] Embodiments of the present disclosure are in the field of renewable energy and, in particular, include approaches for forming barrier-less metal seed stacks and contacts.

BACKGROUND

[0002] Photovoltaic cells, commonly known as solar cells, are well known devices for direct conversion of solar radiation into electrical energy. Generally, solar cells are fabricated on a semiconductor wafer or substrate using semiconductor processing techniques to form a p-n junction near a surface of the substrate. Solar radiation impinging on the surface of, and entering into, the substrate creates electron and hole pairs in the bulk of the substrate. The electron and hole pairs migrate to p-doped and n-doped regions in the substrate, thereby generating a voltage differential between the doped regions. The doped regions are connected to conductive regions on the solar cell to direct an electrical current from the cell to an external circuit coupled thereto.

[0003] Techniques for increasing the efficiency in the manufacture of solar cells are generally desirable. Some embodiments of the present disclosure allow for increased solar cell manufacturing efficiency by providing novel processes for fabricating solar cell structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figures 1A, 1B, and 1C illustrate cross-sectional views of a portion of a solar cell with conductive contacts including a copper layer directly contacting a substrate, in accordance with an embodiment of the present disclosure.

[0005] Figure 2 illustrates a cross-sectional view of a portion of a solar cell with conductive contacts including a metal seed layer disposed on a substrate, in accordance with an embodiment of the present disclosure.

[0006] Figure 3 illustrates a cross-sectional view of a portion of a solar cell with conductive contacts including multiple metal seed layers disposed on a substrate, in accordance with an embodiment of the present disclosure.

[0007] Figure 4 is a flowchart illustrating operations in a method of fabricating a solar cell, in accordance with an embodiment of the present disclosure.

[0008] Figures 5A and 5B illustrate cross-sectional views of processing operations in a method of fabricating solar cells corresponding to operations of the flowchart of Figure 4, and in accordance with an embodiment of the present disclosure.

[0009] Figure 6 is a flowchart illustrating operations in a method of fabricating a solar cell, in accordance with an embodiment of the present disclosure.

[0010] Figures 7A, 7B, 7C, and 7D illustrate cross-sectional views of processing operations in a method of fabricating solar cells corresponding to operations of the flowchart of Figure 6, and in accordance with an embodiment of the present disclosure.

[0011] Figure 8A illustrates a graph of the change in leakage current density after annealing an exemplary substrate with a copper seed layer, in accordance with an embodiment of the present disclosure.

[0012] Figure 8B illustrates a graph of the change in bulk recombination rate after annealing an exemplary substrate with a copper seed layer, in accordance with an embodiment of the present disclosure.

[0013] Figure 8C illustrates a graph of the change in leakage current density after annealing an exemplary substrate with a copper seed layer, in accordance with an embodiment of the present disclosure.

[0014] Figure 8D illustrates a graph of the change in bulk recombination rate after annealing an exemplary substrate with a copper seed layer, in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0015] The following detailed description is merely illustrative in nature and is not intended to limit the embodiments of the subject matter or the application and uses of such embodiments. As used herein, the word “exemplary” means “serving as an example, instance, or illustration.” Any implementation described herein as exemplary is not necessarily to be construed as preferred or advantageous over other implementations. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary, or the following detailed description.

[0016] This specification includes references to “one embodiment” or “an embodiment.” The appearances of the phrases “in one embodiment” or “in an embodiment” do not necessarily refer to the same embodiment. Particular features, structures, or characteristics may be combined in any suitable manner consistent with this disclosure.

[0017] Terminology. The following paragraphs provide definitions and/or context for terms found in this disclosure (including the appended claims):

[0018] “Comprising.” This term is open-ended. As used in the appended claims, this term does not foreclose additional structure or steps.

[0019] “Configured To.” Various units or components may be described or claimed as

“configured to” perform a task or tasks. In such contexts, “configured to” is used to connote structure by indicating that the units/components include structure that performs those task or tasks during operation. As such, the unit/component can be said to be configured to perform the task even when the specified unit/component is not currently operational (e.g., is not on/active). Reciting that a unit/circuit/component is “configured to” perform one or more tasks is expressly intended not to invoke 35 U.S.C. §112, sixth paragraph, for that unit/component.

[0020] “First,” “Second,” etc. As used herein, these terms are used as labels for nouns that they precede, and do not imply any type of ordering (e.g., spatial, temporal, logical, etc.). For example, reference to a “first” solar cell does not necessarily imply that this solar cell is the first solar cell in a sequence; instead the term “first” is used to differentiate this solar cell from another solar cell (e.g., a “second” solar cell).

[0021] “Coupled.” The following description refers to elements or nodes or features being “coupled” together. As used herein, unless expressly stated otherwise, “coupled” means that one element/node/feature is directly or indirectly joined to (or directly or indirectly communicates with) another element/node/feature, and not necessarily mechanically.

[0022] In addition, certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, and “below” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, “side”, “outboard”, and “inboard” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

[0023] Approaches for forming barrier-less metal seed stacks and contacts for solar cells and the resulting solar cells are described herein. In the following description, numerous specific details are set forth, such as specific process flow operations, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known fabrication techniques, such as copper plating techniques, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

[0024] Disclosed herein are methods of fabricating solar cells. In an embodiment, a method of fabricating a solar cell involves providing a substrate, and plating a copper layer directly onto the substrate to form a conductive contact.

[0025] In another embodiment, a method of fabricating a solar cell involves providing a substrate, and forming a seed layer over the substrate. The seed layer consists essentially of one or more non-diffusion-barrier metal layers. The method further involves forming a conductive contact for the solar cell from the seed layer.

[0026] Also disclosed herein are solar cells. In an embodiment, a solar cell includes a substrate. A conductive conduct is disposed on the substrate and includes a copper layer directly contacting the substrate.

[0027] In another embodiment, a solar cell includes a substrate. A seed layer is disposed directly on the substrate, and consists essentially of one or more non-diffusion-barrier metal layers. A conductive contact includes a copper layer disposed directly on the seed layer.

[0028] Thus, embodiments of the present disclosure include solar cells with diffusion-barrier-less conductive contacts. Existing methods of forming contacts generally involve deposition of multiple seed layers, including a diffusion barrier layer between a copper layer and the silicon. Copper diffusion into the silicon can damage devices, and therefore existing contacts include a diffusion barrier metal layer to prevent unwanted diffusion of the copper into the silicon. An example of a diffusion barrier material is a Titanium-Tungsten alloy (TiW). One example of a seed stack for forming a contact with a diffusion barrier layer includes an aluminum (Al) seed layer disposed on a silicon substrate, a TiW barrier layer disposed on the aluminum seed layer, and a copper (Cu) seed layer disposed on the TiW barrier layer. The TiW barrier layer thus limits copper diffusion into the silicon substrate.

[0029] Methods involving deposition of a barrier layer may involve additional processing steps and require complex processing tools. For example, deposition of multiple metal layers including a TiW barrier layer may necessitate a separate substrate edge coating operation to prevent metal from being deposited on the edges of the solar cell substrate. The additional processing steps involved in depositing a barrier layer can decrease throughput. In contrast to existing methods, embodiments of the disclosure include solar cell contacts without a diffusion barrier layer but that limit copper diffusion into the silicon.

[0030] Figures 1A-1C, Figure 2, and Figure 3 illustrate cross-sectional views of solar cells in accordance with embodiments of the present disclosure.

[0031] Figure 1A illustrates a cross-sectional view of a portion of a solar cell with conductive contacts including a copper layer directly contacting a substrate, in accordance with an embodiment of the present disclosure. A portion of the solar cell 100A includes a substrate 102. Conductive contacts 104 are disposed on the substrate 102. According to embodiments, the conductive contacts 104 include a copper layer directly contacting the substrate 102. Figure 1A illustrates a portion of the solar cell 100A with a patterned dielectric layer 114 disposed over the

substrate 102. In the illustrated embodiment, the conductive contacts 104 contact the substrate 102 through gaps or contact openings in the dielectric layer 114. The substrate 102 can include one or more semiconducting and/or dielectric layers. For example, Figures 1B and 1C illustrate exemplary substrates upon which the conductive contacts 104 may be disposed.

[0032] Figure 1B illustrates a cross-sectional view of a portion of a solar cell having conductive contacts formed on emitter regions formed above a substrate, in accordance with an embodiment of the present disclosure.

[0033] Referring to Figure 1B, a portion of a solar cell 100B includes a patterned dielectric layer 224 disposed above a plurality of n-type doped polycrystalline silicon (polysilicon) regions 220, a plurality of p-type doped polysilicon regions 222, and on portions of a substrate 200 exposed by trenches 216. The polysilicon regions 220 and 222 are formed from a polysilicon layer disposed in or above the substrate 200. According to one such embodiment, the polysilicon layer has a doping concentration in a range of at least 10^{18} per cm^3 . In one such embodiment, the doping concentration is in the range of 10^{19} to 10^{20} per cm^3 . In one embodiment, the substrate 200 includes a monocrystalline silicon substrate. Although described as a polycrystalline silicon regions 220 and 222, in an alternative embodiment, the regions 220 and 222 are formed from an amorphous silicon layer.

[0034] The conductive contacts 104 include a copper layer that directly contacts the polycrystalline regions 220 and 222. In the illustrated embodiment, conductive contacts 104 are directly disposed in a plurality of contact openings disposed in the dielectric layer 224 and are coupled to the plurality of n-type doped polysilicon regions 220 and to the plurality of p-type doped polysilicon regions 222. The plurality of n-type doped polysilicon regions 220 and the plurality of p-type doped polysilicon regions 222 can, in one embodiment, provide emitter regions for the solar cell 100B. Thus, in an embodiment, the conductive contacts 104 are disposed on the emitter regions. In an embodiment, the conductive contacts 104 are back contacts for a back-contact solar cell and are situated on a surface of the solar cell opposing a light receiving surface (direction provided as 201 in Figure 1B) of the solar cell 100B. Furthermore, in one embodiment, the emitter regions are formed on a thin or tunnel dielectric layer 202. In one embodiment in which the emitter regions are formed from an amorphous silicon layer, the amorphous silicon emitters are disposed on an intrinsic amorphous silicon layer.

[0035] Figure 1B illustrates a portion of the solar cell 100B having one dielectric layer 224 disposed over the polysilicon regions 220 and 222, but other embodiments may not include dielectric layers, or may include more than one dielectric layer. In an embodiment with one or more dielectric layers disposed over the polysilicon regions 220 and 222, a copper layer of the

conductive contacts directly contacts the polycrystalline silicon layer through the gaps or contact openings in the one or more dielectric layers.

[0036] Thus, Figure 1B illustrates a solar cell having conductive contacts formed on emitter regions formed above a substrate. In another embodiment, a solar cell includes conductive contacts disposed directly on emitter regions formed in a substrate of the solar cell. For example, Figure 1C illustrates a cross-sectional view of a portion of a solar cell having conductive contacts formed on emitter regions formed in a substrate, in accordance with an embodiment of the present disclosure.

[0037] Referring to Figure 1C, a portion of a solar cell 100C includes a patterned dielectric layer 124 disposed above a plurality of n-type doped diffusion regions 120, a plurality of p-type doped diffusion regions 122, and on portions of a substrate 100, such as a bulk crystalline (e.g., monocrystalline) silicon substrate. Conductive contacts 104 are disposed in a plurality of contact openings disposed in the dielectric layer 124 and are coupled to the plurality of n-type doped diffusion regions 120 and to the plurality of p-type doped diffusion regions 122.

[0038] In an embodiment, the conductive contacts 104 include a copper layer that directly contacts the substrate of the solar cell 100C. In one embodiment with a monocrystalline silicon substrate, the copper layer of the conductive contacts 104 directly contacts the monocrystalline silicon substrate. For example, in an embodiment, the diffusion regions 120 and 122 are formed by doping regions of a silicon substrate with n-type dopants and p-type dopants, respectively. Furthermore, the plurality of n-type doped diffusion regions 120 and the plurality of p-type doped diffusion regions 122 can, in one embodiment, provide emitter regions for the solar cell 100C. Thus, in an embodiment, the conductive contacts 104 are disposed on the emitter regions. In an embodiment, the conductive contacts 104 are back contacts for a back-contact solar cell and are situated on a surface of the solar cell opposing a light receiving surface, such as opposing a texturized light receiving surface 101, as depicted in Figure 1C. In an embodiment, referring again to Figure 1C, each of the conductive contacts 104 includes a copper layer disposed on the emitter regions (i.e., diffusion regions) in direct contact with the substrate of the solar cell 100C. The conductive contacts 104 may be similar to or the same as the conductive contacts 104 described above in association with Figures 1A and 1B.

[0039] Although certain materials are described specifically above with reference to Figures 1A and 1B, some materials may be readily substituted with others with other such embodiments remaining within the spirit and scope of embodiments of the present disclosure. For example, in an embodiment, a different material substrate, such as a group III-V material substrate, can be used instead of a silicon substrate.

[0040] Furthermore, the formed contacts need not be formed directly on a bulk

substrate, as was described in Figure 1C. For example, in one embodiment, conductive contacts such as those described above are formed on semiconducting regions formed above (e.g., on a back side of) as bulk substrate, as was described for Figure 1B.

[0041] Like Figure 1B, Figure 1C illustrates a portion of the solar cell 100C having one dielectric layer 124, but other embodiments may not include dielectric layers, or may include more than one dielectric layer disposed over the substrate 100. In one embodiment with one or more dielectric layers disposed over the substrate 100, a copper layer of the conductive contacts directly contacts the monocrystalline silicon substrate through gaps or contact openings in the one or more dielectric layers.

[0042] Figures 1A-1C illustrate portions of solar cells with conductive contacts disposed directly on a substrate, without metal seed layers, according to embodiments of the disclosure. An exemplary fabrication process for forming solar cells such as the solar cells illustrated in Figures 1A-1C is described below with reference to Figures 4, 5A, and 5B.

[0043] Figures 2 and 3 illustrate example solar cells with conductive contacts including one or more metal seed layers disposed on a substrate, according to embodiments of the disclosure. For example, Figure 2 illustrates a cross-sectional view of a portion of a solar cell having conductive contacts including a metal seed layer disposed on a substrate, in accordance with an embodiment of the present disclosure.

[0044] A portion of the solar cell 250 includes a substrate 252. A seed layer 256 is disposed directly on the substrate 252. In one embodiment, the seed layer 256 consists essentially of one or more non-diffusion-barrier metal layers. Thus, in one such embodiment, the seed layer 256 includes one or more metal layers without an intervening diffusion-barrier metal layer. Conductive contacts 254 include a copper layer disposed directly on the seed layer 256.

[0045] In one embodiment, the substrate includes a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate. For example, the conductive contacts 254 may be formed on emitter regions formed above a substrate, such as described above with respect to Figure 1B. In one such embodiment, the seed layer 256 directly contacts the polycrystalline silicon layer. The substrate 252 may further include one or more dielectric layers disposed over the polycrystalline silicon layer, such as the patterned dielectric layer 214. In one such embodiment, the seed layer 256 directly contacts the polycrystalline silicon layer through gaps or contact openings in the dielectric layer 214.

[0046] In another embodiment, the substrate 252 includes a monocrystalline silicon substrate, and the seed layer 256 directly contacts the monocrystalline silicon substrate. For example, the conductive contacts 254 can be formed on emitter regions formed in a substrate

such as described above with respect to Figure 1C. The substrate 252 may further include one or more dielectric layers disposed over the monocrystalline silicon layer, such as the patterned dielectric layer 214. In one such embodiment, the seed layer directly contacts the monocrystalline silicon substrate through gaps or contact openings in the dielectric layer 214. Thus, in embodiments, the substrate over which the seed layer 256 is disposed may include various semiconductor and/or dielectric layers.

[0047] The metal seed layer 256 can include, for example, a copper seed layer, an aluminum seed layer, a silver seed layer, a nickel seed layer, or any other non-diffusion-barrier metal layer. A “non-diffusion-barrier metal” is a metal that does not have low copper diffusivity, such as copper, aluminum, silver, or any other non-diffusion-barrier metal. In one embodiment, a copper seed layer is disposed on and directly contacts the substrate 302, and the conductive contacts 304 include a copper layer disposed directly on the copper seed layer.

[0048] According to an embodiment, the seed layer 256 includes multiple metal seed layers such as, as illustrated in Figure 3. Figure 3 illustrates a cross-sectional view of a portion of a solar cell having conductive contacts including multiple metal seed layers disposed on a substrate, in accordance with an embodiment of the present disclosure. A portion of a solar cell 300 includes a substrate 302. The substrate 302 can be similar to, or the same, as the substrates discussed above (e.g., the substrate 102 of Figure 1A). As illustrated in Figure 3, a dielectric layer 314 is disposed over the substrate 302, and the seed layer 306 contacts the substrate 302 through gaps or contact openings in the dielectric layer 314.

[0049] Metal seed layers 306 and 308 are disposed over the substrate 302. As illustrated in Figure 3, a first metal seed layer 306 is directly contacting the substrate 302. A second metal seed layer 308 is directly contacting the first metal seed layer 306 and the conductive contact 304. The metal seed layers 306 and 308 may include, for example, one or more of a copper seed layer, an aluminum seed layer, and a silver seed layer, or any other non-diffusion-barrier metal layer.

[0050] In one embodiment, the first seed layer 306 is an aluminum or silver seed layer disposed on and directly contacting the substrate 302. Aluminum enables forming a good electrical contact with both p-type and n-type silicon. Additionally, an aluminum seed layer can have the benefit of increasing reflection of light back into the solar cell. In one such embodiment, the second metal seed layer 308 that directly contacts the first metal seed layer 306 is a copper seed layer. In one such embodiment, the copper seed layer also directly contacts a copper layer of the conductive contacts 304. A copper seed layer can enable ease of plating the copper layer of the conductive contacts 304. In other embodiments, the metal seed layers 306 and 308 may include other non-diffusion-barrier metal layers.

[0051] Although Figure 3 illustrates conductive contacts 304 formed from two metal seed layers, other embodiment may include more than two metal seed layers. For example, in one embodiment, an aluminum seed layer is disposed directly on the substrate 302, a nickel seed layer is disposed directly on the aluminum seed layer, and a copper seed layer is disposed directly on the nickel seed layer. Other embodiments can include no metal seed layers (as described above with respect to Figures 1A-1C), or a single metal seed layer (as described with respect to Figure 2).

[0052] Figure 4 is a flowchart illustrating operations in a method of fabricating a solar cell, in accordance with an embodiment of the present disclosure. Figures 5A and 5B illustrate cross-sectional views of the operations of the flowchart 400 of Figure 4, in accordance with an embodiment of the present disclosure.

[0053] Referring to Figure 5A, and to corresponding operation 402 of the flowchart 400, a method of fabricating a solar cell involves providing a substrate 502. As explained above, providing the substrate can involve providing one or more semiconducting and/or dielectric layers. For example, providing the substrate can involve providing a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate. In another example, providing the substrate can involve providing a monocrystalline silicon substrate. Providing the substrate may further involve providing one or more patterned dielectric layers disposed over the monocrystalline silicon substrate and/or the polysilicon layer. As illustrated in Figures 5A and 5B, a patterned dielectric layer 514 is disposed over the substrate 502.

[0054] Referring to Figure 5B, and to corresponding operation 404 of the flowchart 400, the method further involves plating a copper layer 504 directly onto the substrate 502 to form a conductive contact. Other embodiments may involve techniques other than plating to form the copper layer 504 directly onto the substrate 502 to form the conductive contact. In an embodiment with a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate, plating the copper layer may involve plating the copper layer directly onto the polycrystalline silicon layer. In an embodiment with a monocrystalline silicon substrate, plating the copper layer may involve electroplating the copper layer directly onto the monocrystalline silicon substrate. In other embodiments, plating the copper layer may involve any other suitable method of forming the conductive contacts. In an embodiment with one or more dielectric layers disposed over the polycrystalline silicon layer and/or monocrystalline substrate, such as the dielectric layer 514, the plated copper layer may contact underlying silicon through gaps or contact openings in the dielectric layer 514.

[0055] The method may further involve annealing the copper layer. Annealing the

copper layer enables formation of a good contact between the copper layer and the substrate. In one embodiment, annealing the copper layer may involve heating the copper layer to a temperature that is greater than 50 °C and less than 500 °C. In one such embodiment, the copper layer is heated to a temperature in a range of 50 to 450 °C. According to embodiments, heating the copper layer to a temperature in a range of 50 to 450 °C can enable formation of a good contact without causing significant copper migration into the silicon. Annealing at temperatures higher than 500 °C may result in migration of sufficient copper into the silicon to short contacts on the solar cells or cause other device defects. Figures 8A-8D illustrate graphs showing the effects of annealing at different temperatures for different lengths of time, according to an embodiment. In one embodiment, the amount of time the copper layer is annealed depends on the annealing temperature. A higher temperature (e.g., 500 °C) may involve annealing the copper layer for 10-30 minutes. A lower temperature (e.g., 300 °C) may involve annealing the copper layer for greater than 30 minutes (e.g., an hour). Other embodiments may involve other temperatures and annealing times. Annealing the copper layer at lower temperatures and/or for shorter periods of time may prevent substantial diffusion of copper into the substrate, and therefore prevent or limit damage to devices formed in the substrate.

[0056] According to an embodiment, copper atoms that diffuse into the underlying substrate tend to segregate on crystalline defects, on the surface of the substrate, or form complexes with dopant atoms. In an embodiment with a polycrystalline silicon layer disposed in or above a monocrystalline silicon substrate (e.g., such as in the portion of the solar cell 100B of Figure 1B), the copper atoms may precipitate within the polycrystalline silicon layer, therefore preventing substantial copper contamination of the monocrystalline silicon substrate. However, other embodiments without such a polycrystalline silicon layer (e.g., the portion of the solar cell 100C of Figure 1C) may also include conductive contacts directly on the substrate.

[0057] Thus, one embodiment includes directly plating a copper layer onto the substrate to form a conductive conduct for a solar cell. Directly plating the copper layer onto the substrate enables solar cell fabrication with fewer processing operations than existing fabrication methods. For example, embodiments may eliminate deposition and etching operations for formation of metal seed layers, and/or eliminate edge coating operations. A simpler process flow may in turn enable higher manufacturing throughput. Furthermore, directly plating the copper layer on the substrate without metal seed layers can enable a reduction of materials used to form solar cell contacts.

[0058] Figure 6 is a flowchart illustrating operations in a method of fabricating a solar cell, in accordance with an embodiment of the present disclosure. Figures 7A, 7B, 7C, and 7D illustrate cross-sectional views of the operations of the flowchart 600 of Figure 6, in accordance

with an embodiment of the present disclosure.

[0059] Referring to Figure 7A, and to corresponding operation 602 of the flowchart 600, a method of fabricating a solar cell involves providing a substrate 702. As explained above with respect to operation 402 of Figure 4, providing the substrate 702 can involve providing one or more semiconducting and/or dielectric layers. As illustrated in Figures 7A-7D, a patterned dielectric layer 714 is disposed over the substrate 702. The substrate 702 can be similar to or the same as the substrates described above (e.g., the substrate 102 of Figure 1A).

[0060] The method further involves forming a seed layer over the substrate, at operation 604. In an embodiment with one or more dielectric layers disposed over the polycrystalline silicon layer and/or monocrystalline substrate, such as the dielectric layer 714, the seed layer may contact underlying silicon through gaps or contact openings in the dielectric layer 714. In one embodiment, the seed layer consists essentially of one or more non-diffusion-barrier metal layers. Figure 7B illustrates a single non-diffusion-barrier metal seed layer 704. Figure 7C illustrates two non-diffusion-barrier metal seed layers 704 and 706. In one embodiment, forming the seed layer over the substrate may involve depositing an aluminum layer directly on the substrate to form the metal seed layer 704, and depositing a copper layer directly on the aluminum layer to form the metal seed layer 706. Deposition of the metal seed layers 704 and 706 may involve, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or any other deposition method capable of depositing metal seed layers. Although Figures 7C and 7D illustrate two metal seed layers, other embodiments may involve deposition of a single metal seed layer, or more than two metal seed layers.

[0061] The method further involves forming a conductive contact 708 for the solar cell from the seed layer, at operation 606. Forming the conductive contact 708 can involve annealing the non-diffusion-barrier metal layers 704 and 706. Annealing the seed layer can involve heating the seed layer to a temperature that is greater than 50 °C and less than 500 °C. In one such embodiment, the copper layer is heated to a temperature in a range of 50 to 450 °C. As discussed above with respect to Figure 4, according to embodiments, the amount of time the seed layer is annealed depends on the annealing temperature. For example, the method may involve annealing the seed layer at a temperature in a range of 50 to 450 °C for less than an hour. In one such embodiment, the method involves annealing the seed layer at a temperature in a range of 50 to 450 °C for less than ten minutes. In one embodiment, the method may further involve applying a patterned plating resist to the seed layer. The method may further involve plating a metal onto the patterned seed layer to form a plurality of metal contacts on the seed layer.

[0062] According to an embodiment, the method may further involve etching portions

of the seed layers 704 and 706 between the plurality of metal contacts, to obtain the portion of the solar cell as illustrated in Figure 7D. Etching portions of the seed layers 704 and 706 may involve wet etching, or any other method of etching the metal seed layers. In an embodiment with a seed layer that includes multiple different metal seed layers, etching may involve multiple etching operations with different chemistries. The absence of a diffusion barrier layer between the two metal seed layers may result in mixing of the metal seed layers 704 and 706 during annealing of the seed layer. Therefore, etching portions of the seed layer may involve chemistries appropriate for etching metal alloys. For example, where the metal seed layer 704 is an aluminum layer, and the metal seed layer 706 is a copper layer, etching the seed layer may involve etching using a chemistry for a copper-aluminum alloy.

[0063] Figures 8A-8D illustrate graphs for exemplary substrates with copper seed layers after annealing, in accordance with embodiments of the present disclosure. The graphs in Figures 8A-8D illustrate data from tests performed on test wafers with copper seed layers disposed directly on a substrate, similar to the portion of the solar cell illustrated in Figure 2. The data in Figures 8A-8D are from measurements made on symmetrical test devices using a transient photo conductive decay (PCD) measurement setup on a well calibrated tool. Calibration of the tool was confirmed prior to making the measurements illustrated in Figures 8A-8D in part by testing different lots of several types of control devices, including some types of control devices having Cu diffusion barriers with well-known expected results, and some devices that were not subject to thermal stress. Figures 8A and 8B illustrate graphs from tests performed on test wafers having copper seed layers disposed on n-type doped polysilicon regions (e.g., the n-type doped polysilicon regions 220 of Figure 1B). Figures 8C and 8D illustrate graphs from tests performed on test wafers having copper seed layers disposed on p-type doped polysilicon regions (e.g., the p-type doped polysilicon regions 222 of Figure 1B).

[0064] Figure 8A illustrates a graph 800A of the change in leakage current density (ΔJ_0) after annealing at different temperatures for different periods of time. The graph 800A includes data for test wafers kept at approximately room temperature (25 °C) and data for test wafers annealed at temperatures of 200 °C, 300 °C, 400 °C, and 500 °C. The legend 802 shows the symbols representing the length of time a test wafer was annealed for at a given temperature. The test wafers kept at 25 °C were measured after 50 hours. Test wafers annealed at 200 °C were measured after 10 hours, 17 hours, and 25 hours. Test wafers annealed at 300 °C, 400 °C, and 500 °C were measured after 2 hours, 4 hours, and 6 hours. As can be seen in the graph 800A, the test wafers held at 25 °C and the test wafers annealed at 200 °C, 300 °C, and 400 °C experienced little change in leakage current density. However, annealing the test wafers at 500 °C resulted in an increase in the leakage current density, which may be indicative of a reduction

in quality or defective devices.

[0065] Figure 8B illustrates a graph 800B of the change in bulk recombination rate (ΔBRR) of the test wafers annealed at the temperatures and times described above with respect to Figure 8A. Similar to the graph 800A of Figure 8A, the graph 800B shows that the test wafers did not experience a significant change in bulk recombination rate when held at 25 °C or annealed at 200 °C, 300 °C, and 400 °C. However, the test wafers annealed at 500 °C experienced an increase in bulk recombination rate, also indicative of a reduction in quality or defective devices.

[0066] Figures 8C and 8D illustrate graphs comparable to those in Figures 8A and 8B, but for test wafers having copper seed layers disposed on p-type doped polysilicon regions. The graphs 800C and 800D include data for test wafers kept at approximately room temperature (25 °C) and data for test wafers annealed at temperatures of 200 °C, 300 °C, 400 °C, and 500 °C. The graph 800C illustrates the change in leakage current density (ΔJ_0) after annealing at different temperatures, and the graph 800D illustrates the change in bulk recombination rate (ΔBRR) of test wafers annealed at the temperatures and times shown in Figure 8C. Like the graphs in Figures 8A and 8B, the graph 800C of Figure 8C and the graph 800D of Figure 8D show relatively insignificant changes to the test wafers held at 25 °C or annealed at 200 °C, 300 °C, and 400 °C, but show greater changes when annealed at 500 °C. However, even when annealed at 500 °C for shorter periods of time (e.g., two hours or four hours), graphs 800C and 800D show relatively little change in leakage current density and bulk recombination rate.

[0067] Thus, the graphs in Figures 8A-8D illustrate that an embodiment with a copper seed layer, but no barrier layer between the copper seed layer and the substrate, may be annealed without significantly changing the leakage current density or bulk recombination rate. For example, annealing at low temperatures (e.g., less than 500 °C), or at higher temperatures (e.g., 500 °C) but for shorter periods of time, may enable forming good contacts without significantly increasing the leakage current density or bulk recombination rate. The small changes in leakage current density and bulk recombination rate illustrated in Figures 8A-8D indicate that embodiments with barrier-less copper seed layers may be annealed to make solar cells contacts without causing device defects.

[0068] According to embodiments, forming a seed layer without a diffusion barrier layer enables solar cell fabrication with fewer processing operations than existing fabrication methods. For example, embodiments may eliminate deposition and etching operations for the barrier layer, and/or eliminate edge coating operations. A simpler process flow may in turn enable higher manufacturing throughput. Furthermore, forming a seed layer without a barrier layer can enable a reduction of materials used to form solar cell contacts.

[0069] Thus, approaches for forming barrier-less metal seed stacks and contacts for solar cells and the resulting solar cells have been disclosed.

[0070] Although specific embodiments have been described above, these embodiments are not intended to limit the scope of the present disclosure, even where only a single embodiment is described with respect to a particular feature. Examples of features provided in the disclosure are intended to be illustrative rather than restrictive unless stated otherwise. The above description is intended to cover such alternatives, modifications, and equivalents as would be apparent to a person skilled in the art having the benefit of this disclosure.

[0071] The scope of the present disclosure includes any feature or combination of features disclosed herein (either explicitly or implicitly), or any generalization thereof, whether or not it mitigates any or all of the problems addressed herein. Accordingly, new claims may be formulated during prosecution of this application (or an application claiming priority thereto) to any such combination of features. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the appended claims.

[0072] In an embodiment, a solar cell includes a substrate and a conductive contact disposed on the substrate and comprising a copper layer directly contacting the substrate.

[0073] In one embodiment, the substrate comprises a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate, and the copper layer directly contacts the polycrystalline silicon layer.

[0074] In one embodiment, the substrate further includes one or more dielectric layers disposed over the polycrystalline silicon layer, wherein the copper layer directly contacts the polycrystalline silicon layer through gaps in the one or more dielectric layers.

[0075] In one embodiment, the substrate comprises a monocrystalline silicon substrate, and the copper layer directly contacts the monocrystalline silicon substrate.

[0076] In one embodiment, the substrate further comprises one or more dielectric layers disposed over the monocrystalline silicon substrate, wherein the copper layer directly contacts the monocrystalline silicon substrate through gaps in the one or more dielectric layers.

[0077] In one embodiment, the substrate comprises a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate, and the polycrystalline silicon layer has a doping concentration of at least 10^{18} per cm^3 . In an embodiment, a solar cell includes a substrate, a seed layer disposed directly on the substrate, the seed layer consisting essentially of one or more non-diffusion-barrier metal layers, and a conductive contact comprising a copper layer disposed directly on the seed layer.

[0078] In one embodiment, the substrate comprises a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate, and the seed layer directly contacts the polycrystalline silicon layer.

[0079] In one embodiment, the substrate further comprises one or more dielectric layers disposed over the polycrystalline silicon layer, wherein the seed layer directly contacts the polycrystalline silicon layer through gaps in the one or more dielectric layers.

[0080] In one embodiment, the substrate comprises a monocrystalline silicon substrate, and the seed layer directly contacts the monocrystalline silicon substrate.

[0081] In one embodiment, the substrate further comprises one or more dielectric layers disposed over the monocrystalline silicon substrate, wherein the seed layer directly contacts the monocrystalline silicon substrate through gaps in the one or more dielectric layers.

[0082] In one embodiment, the one or more non-diffusion-barrier metal layers comprise an aluminum or silver seed layer directly contacting the substrate, and a copper seed layer directly contacting the aluminum or silver seed layer.

[0083] In an embodiment, a method of fabricating a solar cell providing a substrate, forming a seed layer over the substrate, the seed layer consisting essentially of one or more non-diffusion-barrier metal layers. The method also involves forming a conductive contact for the solar cell from the seed layer.

[0084] In one embodiment, providing the substrate comprises providing a monocrystalline silicon substrate, and forming a polycrystalline silicon layer in or above the monocrystalline silicon substrate and forming the seed layer over the substrate comprises forming the seed layer directly on the polycrystalline silicon layer.

[0085] In one embodiment, providing the substrate further comprises providing one or more patterned dielectric layers disposed over the polycrystalline silicon layer, and forming the seed layer comprises directly forming the seed layer on the polycrystalline silicon layer through gaps in the one or more patterned dielectric layers.

[0086] In one embodiment, providing the substrate comprises providing a monocrystalline silicon substrate, and forming the seed layer comprises forming the seed layer directly on the monocrystalline silicon substrate.

[0087] In one embodiment, providing the substrate further comprises providing one or more patterned dielectric layers disposed over the monocrystalline silicon substrate, and forming the seed layer comprises forming the seed layer directly on the monocrystalline silicon substrate through gaps in the one or more patterned dielectric layers.

[0088] In one embodiment, forming the conductive contact for the solar cell from the seed layer comprises annealing the seed layer at a temperature in a range of 50 to 450 °C.

[0089] In one embodiment, providing the substrate comprises providing a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate, wherein the polycrystalline silicon layer has a doping concentration of at least 10^{18} per cm^3 .

[0090] In one embodiment, forming the conductive contact for the solar cell from the seed layer comprises annealing the seed layer, applying a patterned plating resist to the seed layer, plating a metal onto the patterned seed layer to form a plurality of metal contacts on the seed layer, and etching portions of the seed layer between the plurality of metal contacts.

CLAIMS

What is claimed is:

1. A solar cell comprising:
a substrate; and
a conductive contact disposed on the substrate and comprising a copper layer directly contacting the substrate.
2. The solar cell of claim 1, wherein:
the substrate comprises a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate; and
the copper layer directly contacts the polycrystalline silicon layer.
3. The solar cell of claim 2, wherein:
the substrate further comprises one or more dielectric layers disposed over the polycrystalline silicon layer, wherein the copper layer directly contacts the polycrystalline silicon layer through gaps in the one or more dielectric layers.
4. The solar cell of claim 1, wherein:
the substrate comprises a monocrystalline silicon substrate; and
the copper layer directly contacts the monocrystalline silicon substrate.
5. The solar cell of claim 4, wherein:
the substrate further comprises one or more dielectric layers disposed over the monocrystalline silicon substrate, wherein the copper layer directly contacts the monocrystalline silicon substrate through gaps in the one or more dielectric layers.
6. The solar cell of claim 1, wherein:
the substrate comprises a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate, and wherein the polycrystalline silicon layer has a doping concentration of at least 10^{18} per cm^3 .
7. A solar cell comprising:
a substrate;
a seed layer disposed directly on the substrate, the seed layer consisting essentially of one or more non-diffusion-barrier metal layers; and

a conductive contact comprising a copper layer disposed directly on the seed layer.

8. The solar cell of claim 7, wherein:
the substrate comprises a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate; and
the seed layer directly contacts the polycrystalline silicon layer.
9. The solar cell of claim 8, wherein the substrate further comprises one or more dielectric layers disposed over the polycrystalline silicon layer, wherein the seed layer directly contacts the polycrystalline silicon layer through gaps in the one or more dielectric layers.
10. The solar cell of claim 7, wherein:
the substrate comprises a monocrystalline silicon substrate;
the seed layer directly contacts the monocrystalline silicon substrate.
11. The solar cell of claim 10, wherein:
the substrate further comprises one or more dielectric layers disposed over the monocrystalline silicon substrate, wherein the seed layer directly contacts the monocrystalline silicon substrate through gaps in the one or more dielectric layers.
12. The solar cell of claim 7, wherein the one or more non-diffusion-barrier metal layers comprise an aluminum or silver seed layer directly contacting the substrate, and a copper seed layer directly contacting the aluminum or silver seed layer.
13. A method of fabricating a solar cell, the method comprising:
providing a substrate;
forming a seed layer over the substrate, the seed layer consisting essentially of one or more non-diffusion-barrier metal layers; and
forming a conductive contact for the solar cell from the seed layer.
14. The method of claim 13, wherein:
providing the substrate comprises providing a monocrystalline silicon substrate, and
forming a polycrystalline silicon layer in or above the monocrystalline silicon substrate; and

forming the seed layer over the substrate comprises forming the seed layer directly on the polycrystalline silicon layer.

15. The method of claim 14, wherein:

providing the substrate further comprises providing one or more patterned dielectric layers disposed over the polycrystalline silicon layer; and

forming the seed layer comprises directly forming the seed layer on the polycrystalline silicon layer through gaps in the one or more patterned dielectric layers.

16. The method of claim 13, wherein:

providing the substrate comprises providing a monocrystalline silicon substrate; and

forming the seed layer comprises forming the seed layer directly on the monocrystalline silicon substrate.

17. The method of claim 16, wherein:

providing the substrate further comprises providing one or more patterned dielectric layers disposed over the monocrystalline silicon substrate; and

forming the seed layer comprises forming the seed layer directly on the monocrystalline silicon substrate through gaps in the one or more patterned dielectric layers.

18. The method of claim 13, wherein forming the conductive contact for the solar cell from the seed layer comprises annealing the seed layer at a temperature in a range of 50 to 450 °C.

19. The method of claim 13, wherein:

providing the substrate comprises providing a monocrystalline silicon substrate with a polycrystalline silicon layer disposed in or above the monocrystalline silicon substrate, wherein the polycrystalline silicon layer has a doping concentration of at least 10^{18} per cm^3 .

20. The method of claim 13, wherein forming the conductive contact for the solar cell from the seed layer comprises:

annealing the seed layer;

applying a patterned plating resist to the seed layer;

plating a metal onto the patterned seed layer to form a plurality of metal contacts on the seed layer; and

etching portions of the seed layer between the plurality of metal contacts.

1/11

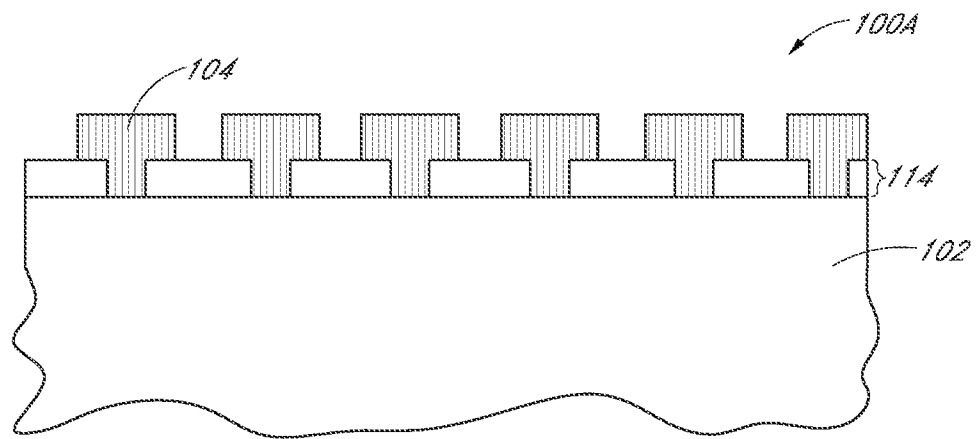


FIG. 1A

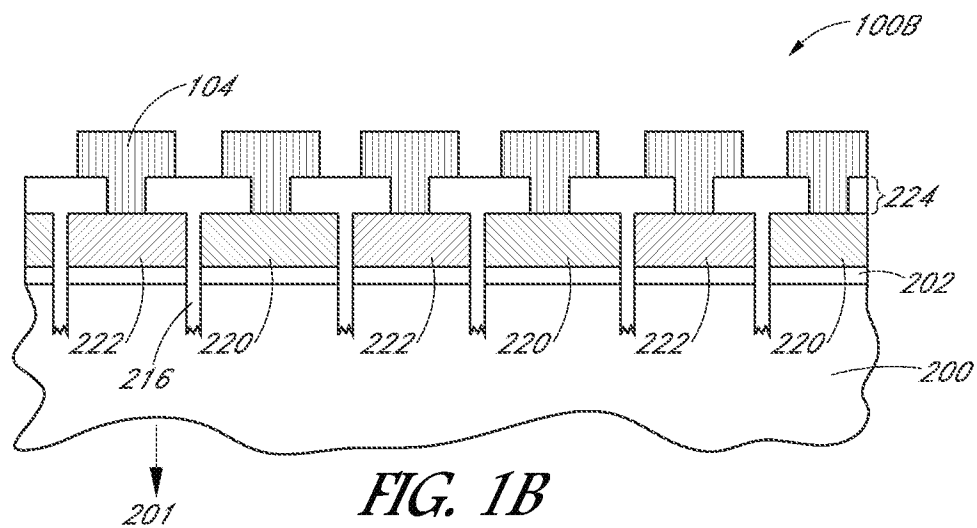


FIG. 1B

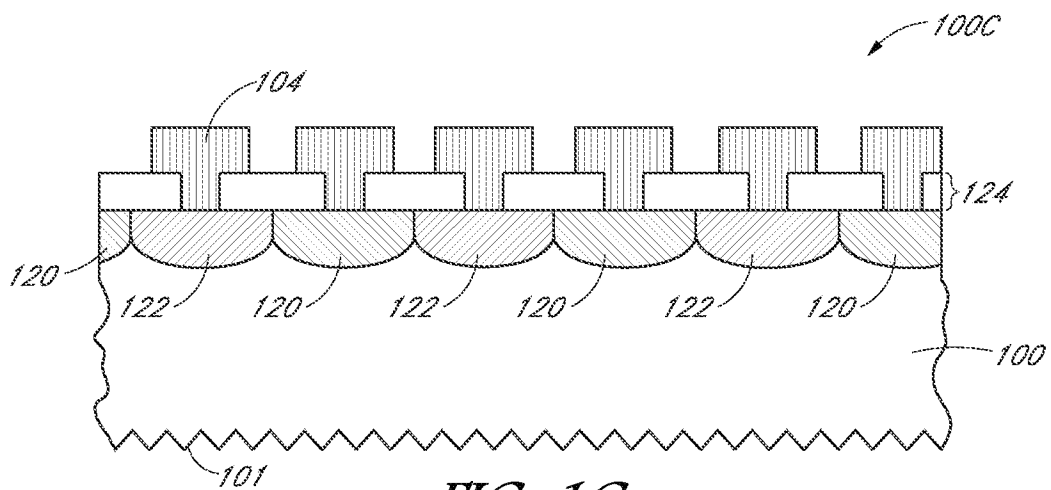


FIG. 1C

2/11

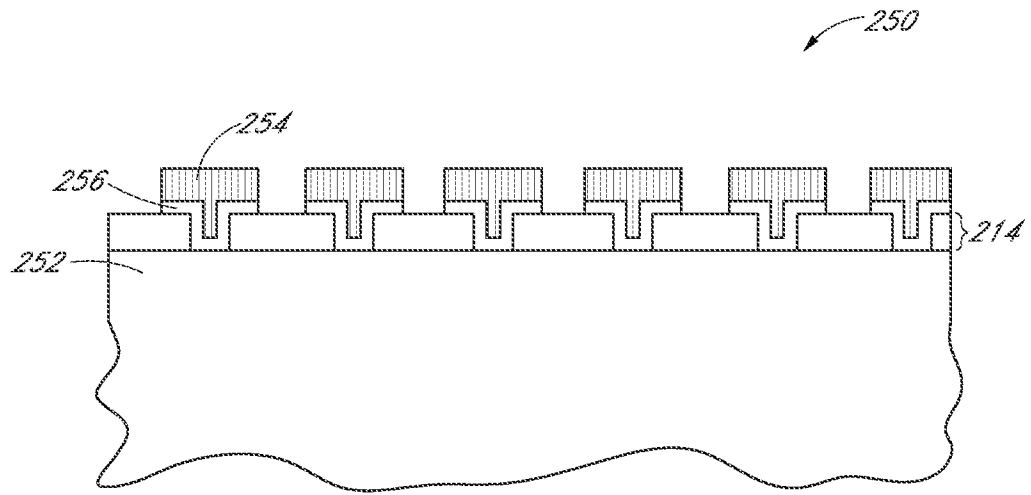


FIG. 2

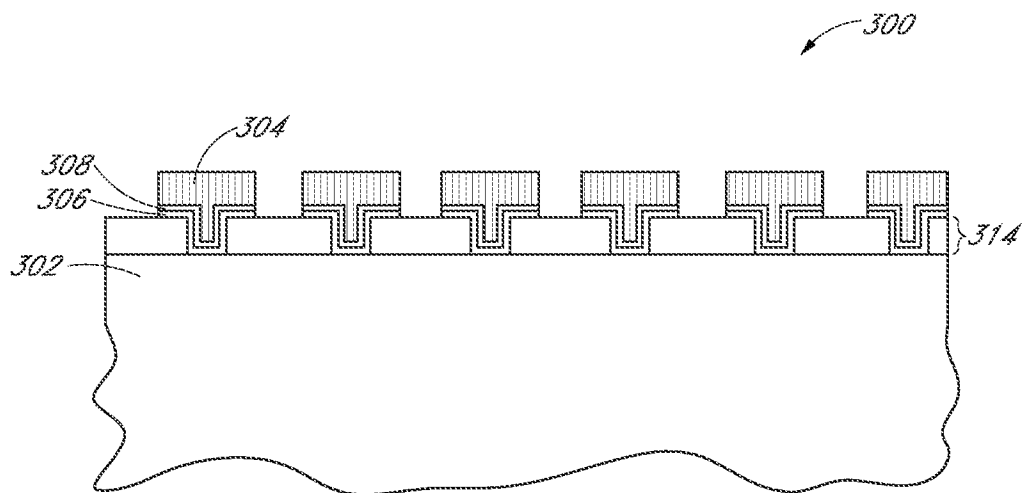
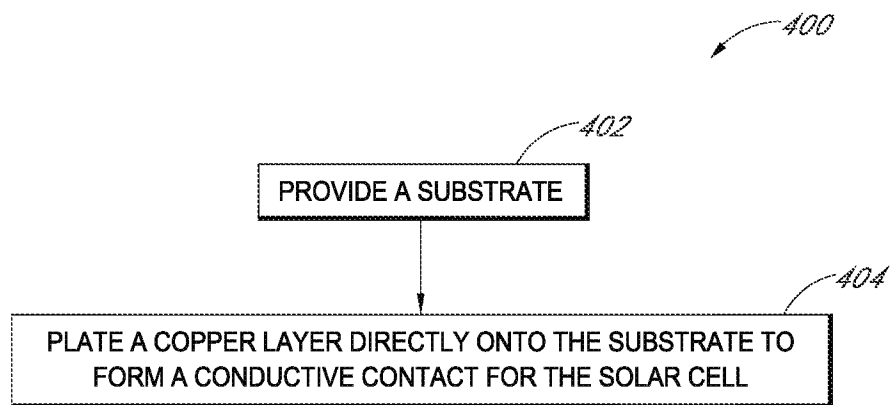


FIG. 3

3/11

*FIG. 4*

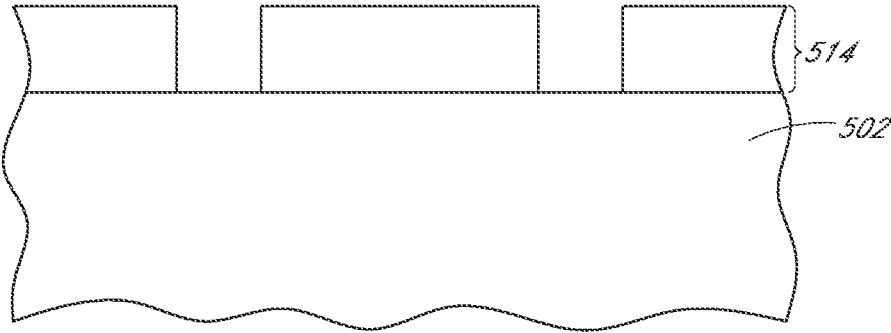


FIG. 5A

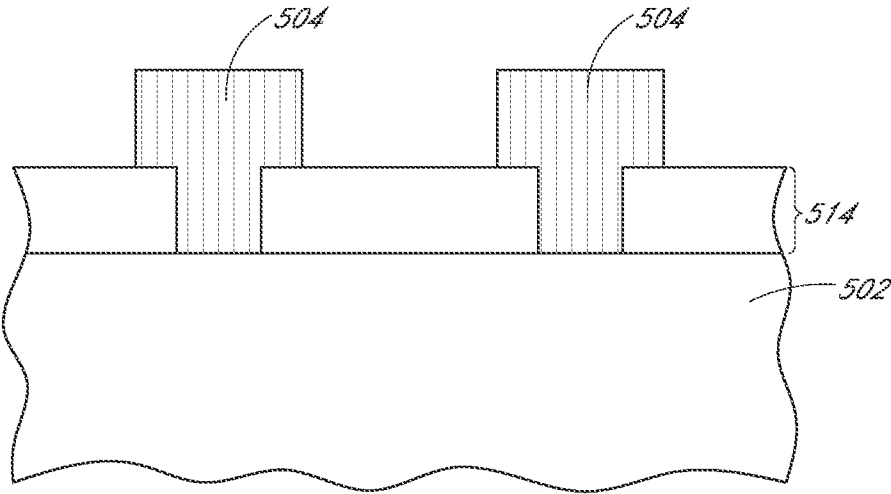
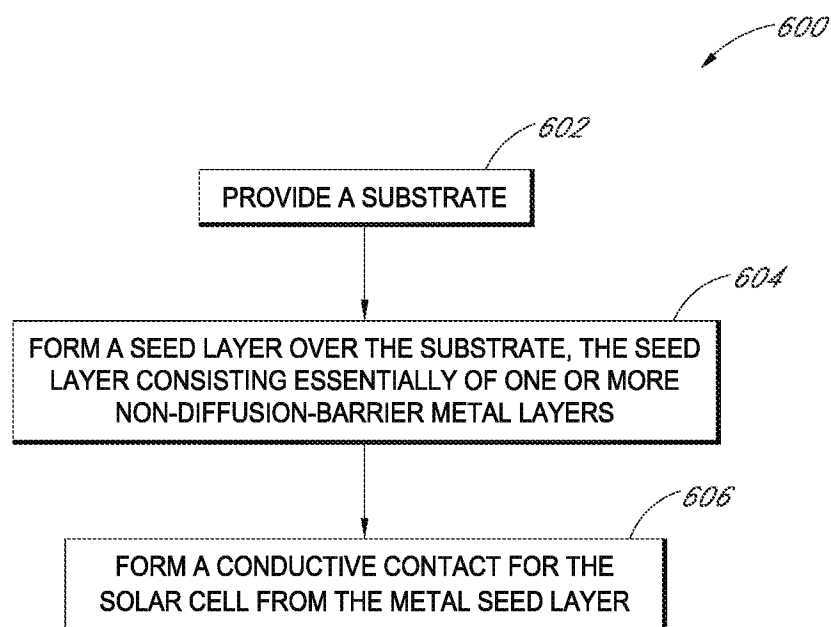


FIG. 5B

5/11

*FIG. 6*

6/11

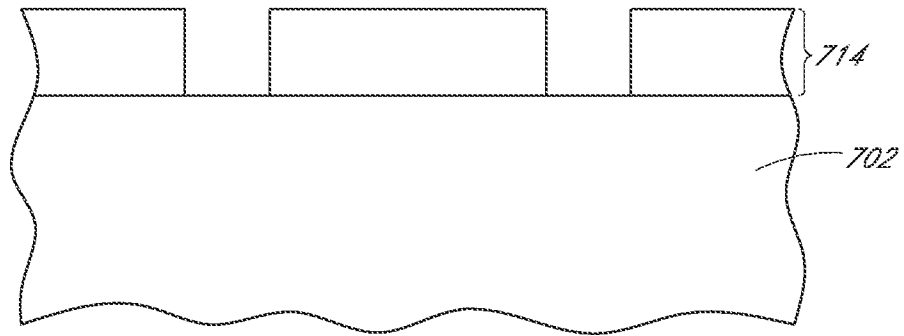


FIG. 7A

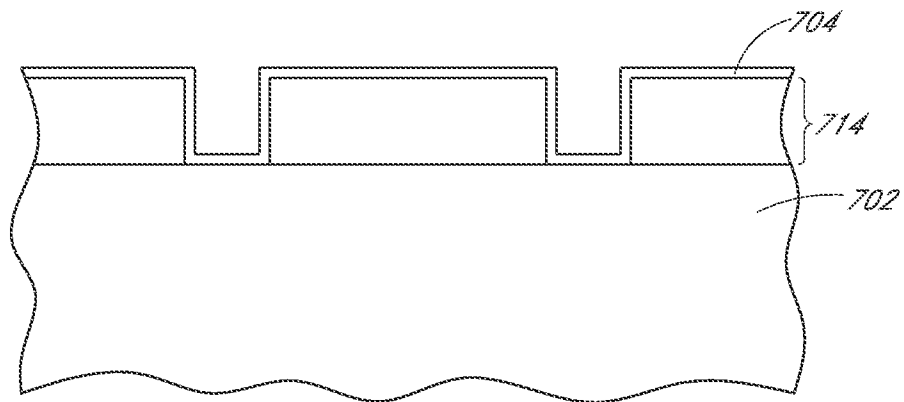


FIG. 7B

7/11

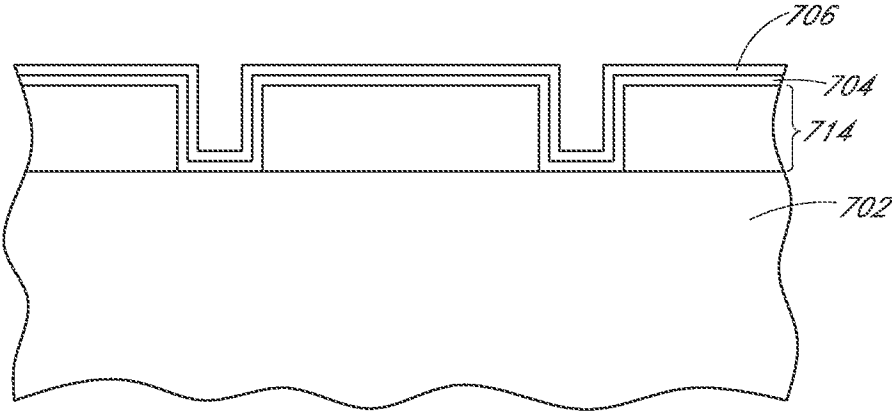


FIG. 7C

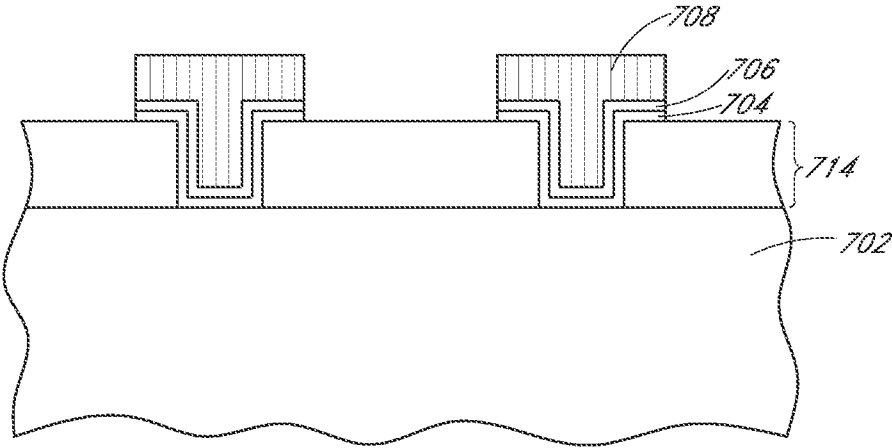


FIG. 7D

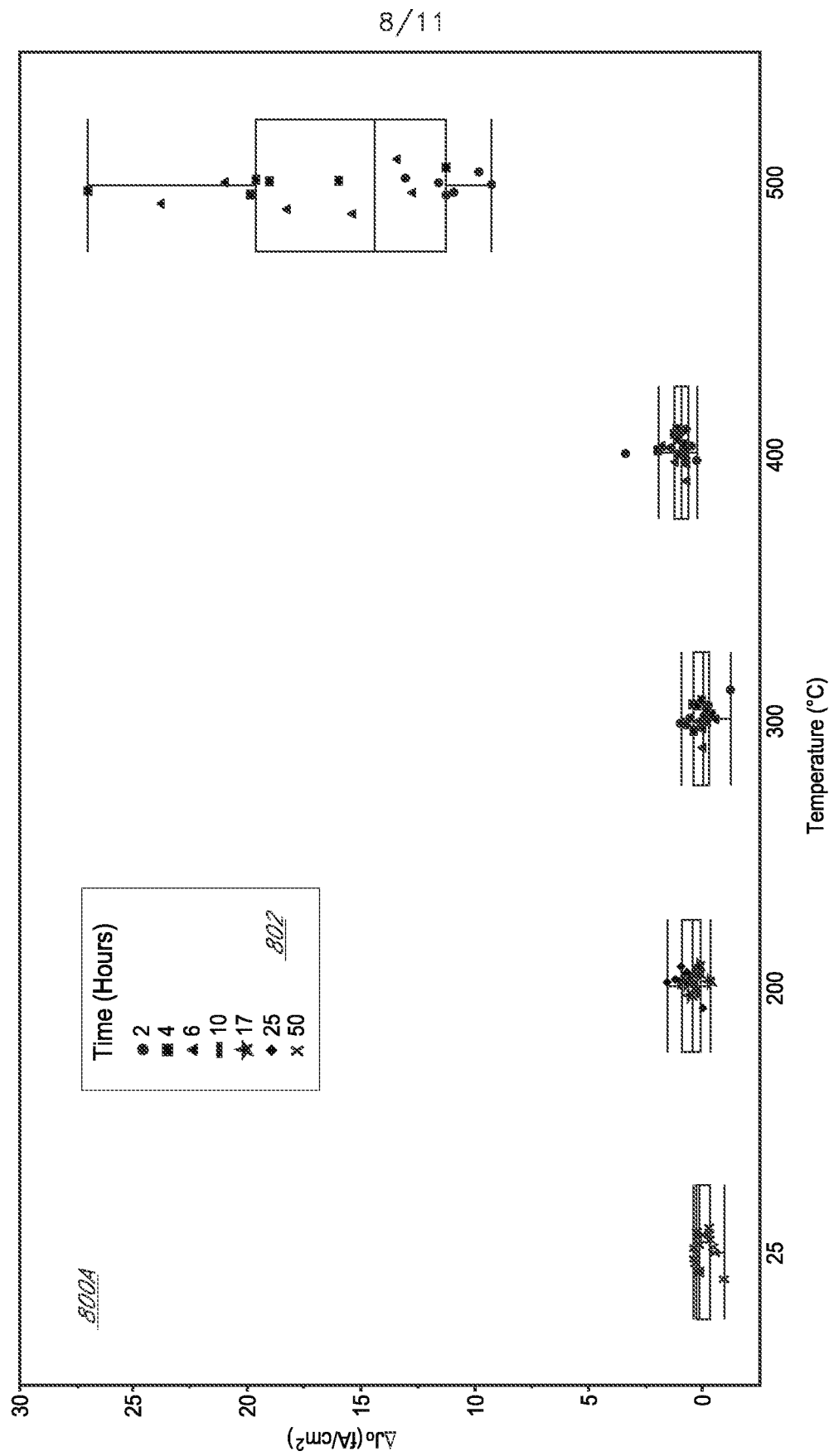


FIG. 8A

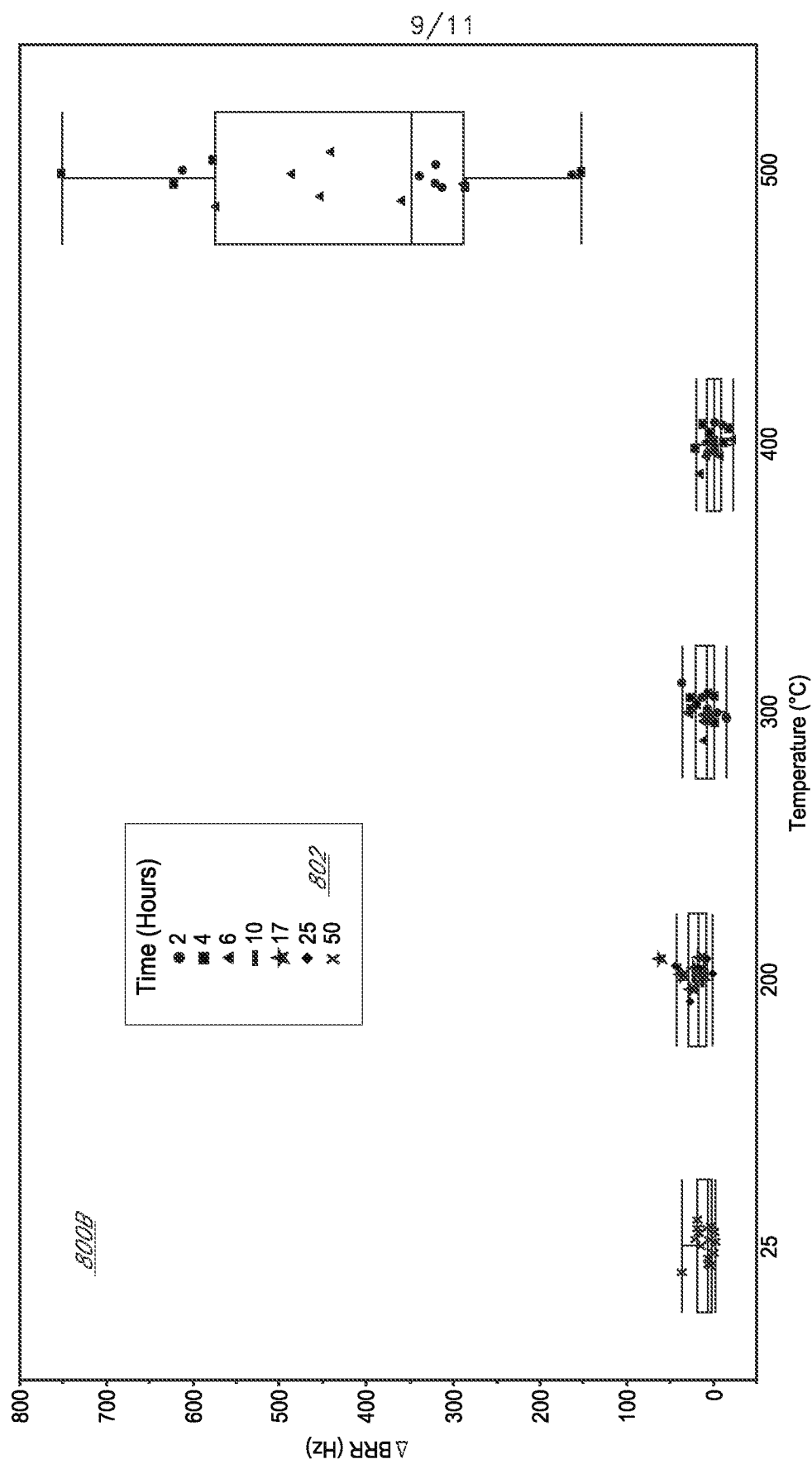


FIG. 8B

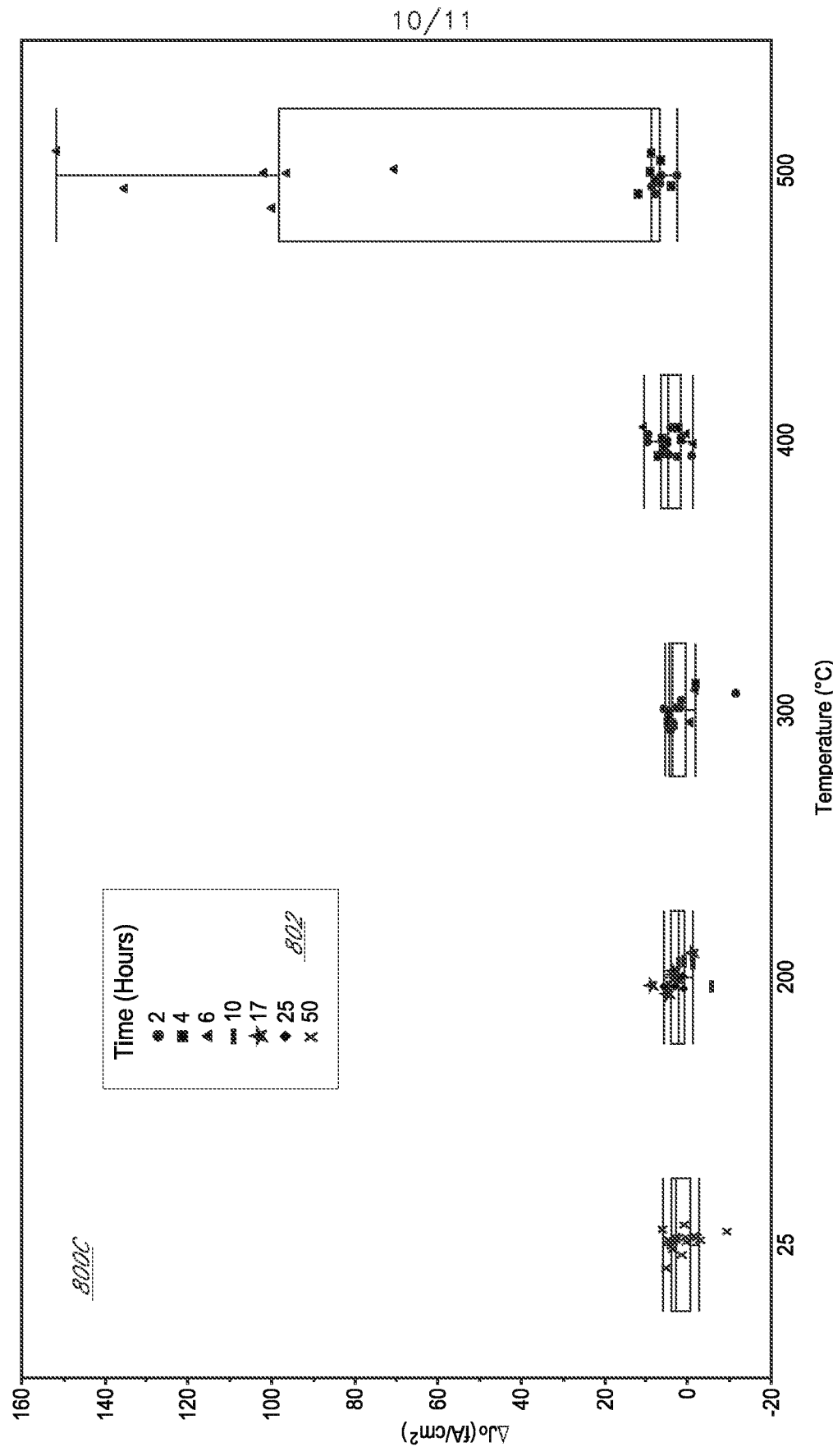


FIG. 8C

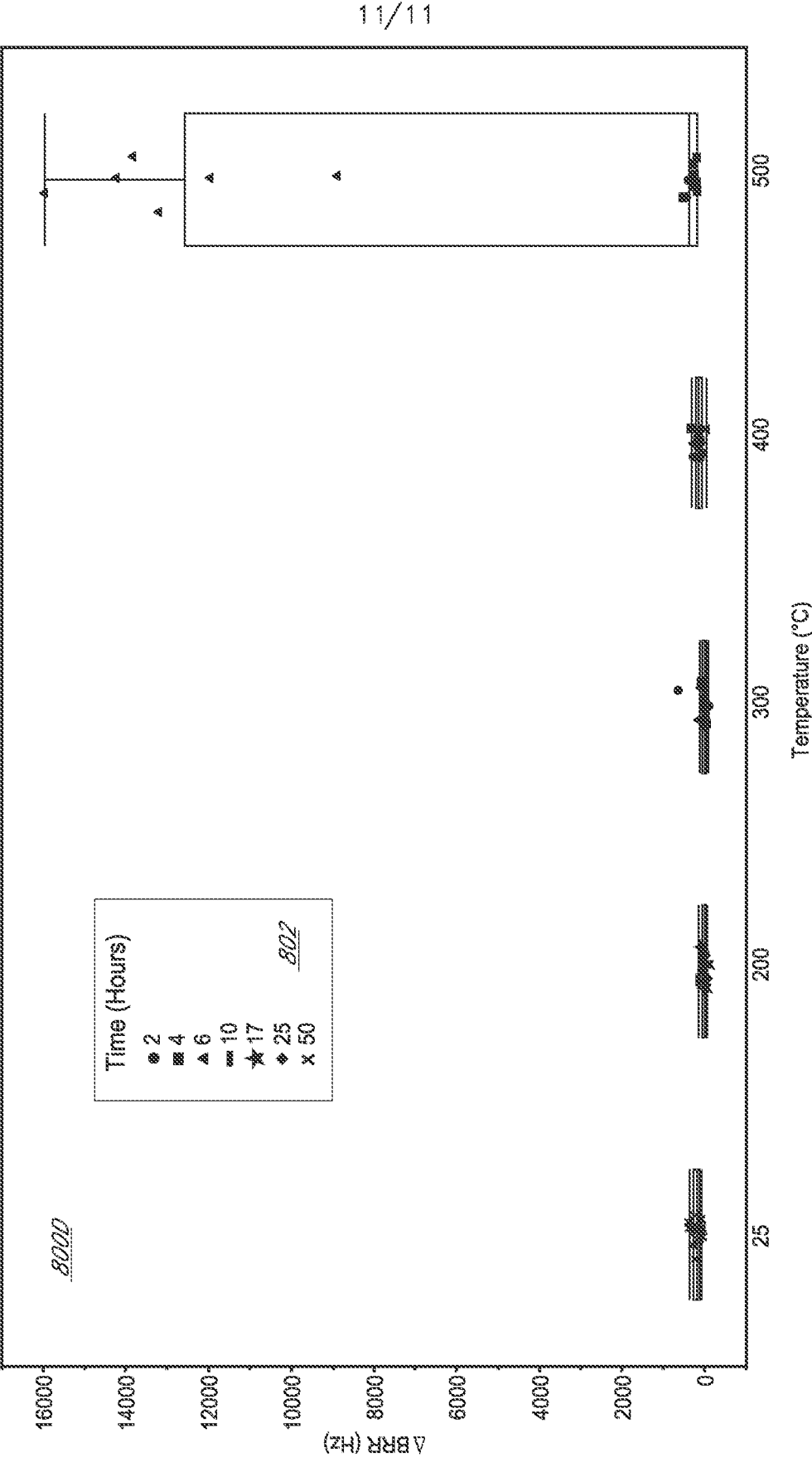


FIG. 8D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/071320**A. CLASSIFICATION OF SUBJECT MATTER****H01L 31/0224(2006.01)i, H01L 31/18(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
H01L 31/0224; H01L 31/0216; H01L 31/0236; H01L 31/04; H01L 31/18; H01L 31/0232Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: solar cell, conductive contact, seed layer, copper**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0147003 A1 (YOUNG-SU KIM et al.) 13 June 2013 See paragraphs [0036]–[0110]; and figures 2–12.	1, 4, 5, 7, 10–13 , 16–18, 20
Y		2, 3, 6, 8, 9, 14, 15, 19
Y	US 2012-0266951 A1 (BO LI et al.) 25 October 2012 See paragraphs [0028]–[0068]; and figures 1–4E.	2, 3, 6, 8, 9, 14, 15, 19
A	US 2011-0162703 A1 (BABAK ADIBI et al.) 07 July 2011 See paragraphs [0043]–[0098]; and figures 1–24.	1–20
A	US 2012-0167977 A1 (JINHYUNG LEE et al.) 05 July 2012 See paragraphs [0029]–[0087]; and figures 1–4.	1–20
A	WO 2012-132854 A1 (SANYO ELECTRIC CO., LTD.) 04 October 2012 See paragraphs [0010]–[0081]; and figures 1–17.	1–20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 March 2015 (23.03.2015)

Date of mailing of the international search report

25 March 2015 (25.03.2015)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea

Facsimile No. ++82 42 472 7140

Authorized officer

KIM, Do Weon

Telephone No. +82-42-481-5560



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/071320

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013-0147003 A1	13/06/2013	CN 103165691 A	19/06/2013
		EP 2605285 A2	19/06/2013
		JP 2013-125963 A	24/06/2013
		KR 10-2013-0067207 A	21/06/2013
US 2012-0266951 A1	25/10/2012	CN 103493216 A	01/01/2014
		EP 2702614 A1	05/03/2014
		EP 2702614 A4	24/09/2014
		JP 2014-512701 A	22/05/2014
		KR 10-2014-0041494 A	04/04/2014
		TW 201304160 A	16/01/2013
		US 2014-295608 A1	02/10/2014
		US 8802486 B2	12/08/2014
		US 8912038 B2	16/12/2014
		WO 2012-148523 A1	01/11/2012
US 2011-0162703 A1	07/07/2011	CN 102099870 A	15/06/2011
		CN 102099923 A	15/06/2011
		CN 102150277 A	10/08/2011
		CN 102150278 A	10/08/2011
		CN 102396068 A	28/03/2012
		EP 2304803 A1	06/04/2011
		EP 2308060 A1	13/04/2011
		EP 2319087 A1	11/05/2011
		EP 2319088 A1	11/05/2011
		EP 2409331 A1	25/01/2012
		JP 05520290 B2	11/06/2014
		JP 2011-524638 A	01/09/2011
		JP 2011-524639 A	01/09/2011
		JP 2011-524640 A	01/09/2011
		JP 2011-525301 A	15/09/2011
		JP 2012-521642 A	13/09/2012
		KR 10-2011-0042051 A	22/04/2011
		KR 10-2011-0042052 A	22/04/2011
		KR 10-2011-0042053 A	22/04/2011
		KR 10-2011-0050423 A	13/05/2011
		KR 10-2012-0027149 A	21/03/2012
		SG 174289 A1	28/10/2011
		SG 186005 A1	28/12/2012
		US 2009-0308439 A1	17/12/2009
		US 2009-0308440 A1	17/12/2009
		US 2009-0308450 A1	17/12/2009
		US 2009-0309039 A1	17/12/2009
		US 8697553 B2	15/04/2014
		US 8871619 B2	28/10/2014
		WO 2009-152365 A1	17/12/2009
		WO 2009-152368 A1	17/12/2009
		WO 2009-152375 A1	17/12/2009
		WO 2009-152378 A1	17/12/2009

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/071320

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		WO 2010-108151 A1	23/09/2010
US 2012-0167977 A1	05/07/2012	KR 10-2012-0079591 A	13/07/2012
WO 2012-132854 A1	04/10/2012	US 2014-0020753 A1	23/01/2014