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(54) Title: BINARY WEIGHTED CAPACITOR ARRAY WITH SPLIT CAPACITOR LAYOUT

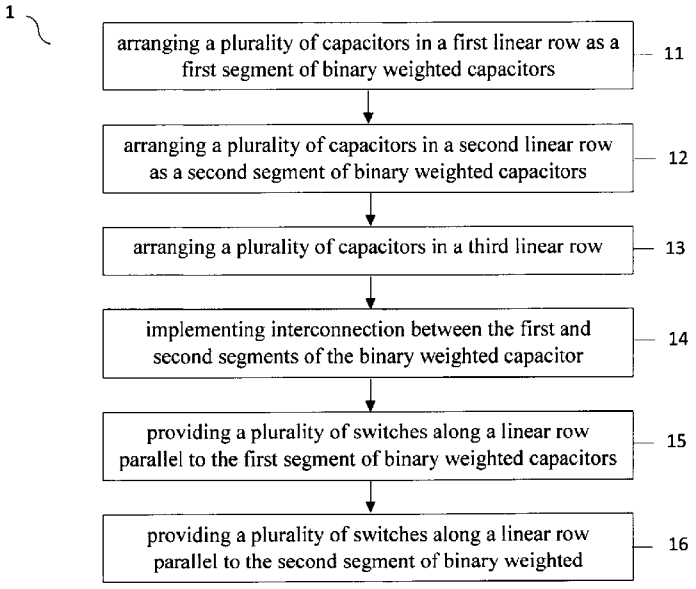

Figure 15

(57) Abstract: The present invention discloses a method of building a binary weighted split capacitor array (1) for minimizing routing induced parasitic mismatch. Specifically, the binary weighted split capacitor array is built with a plurality of unit capacitors with three-dimensional structures having a top plate comprising a plurality of stacked metal plates (M2, M3, M4, M5) and a bottom plate enclosing the top plate with side walls, a floor layer and a ceiling layer to minimize top plate parasitic capacitance to the substrate, and to achieve overall equal parasitic capacitance to the substrate.

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Binary Weighted Capacitor Array with Split Capacitor Layout

Technical Field

The present invention relates to a capacitor array for converting analog to digital signals or digital to analog signals. More specifically, the present invention discloses a binary weighted capacity array with split capacitor layout and a method of building the layout.

Background Art

Our world today is powered by electricals and electronics, and people are heading towards the world of automation, eliminating the need of human labour in the future. Generally, these electrical and electronics are made of different sets of electric circuits where they provide and transport electric energy to drive different applications in the electricals and electronics such as lighting up a space, heating up and cooling down temperatures, driving electric vehicles or motors, storing data and many more.

However, technology advances in a pace quicker than it has been expected. Huge demands from the world seem to be leading the pace, with industries developing more and more advance electricals and electronics to provide better solutions that improves the qualities of human lives. With this in mind, electricals and electronics require more developed and advanced electric circuits to run in a more efficient manner. To achieve such performance, systems within the electric circuits have to run efficiently. By running efficiently, electric circuits have to ensure components and their layouts have the capacity to provide such efficient results.

In electric circuits, the speed of conversions from analog to digital signals and digital to analog signals is one of the elements that determines the efficiency. A number of technologies and techniques have been known to be focusing on the efficiency of the conversions, including direct conversion or flash type analog to digital converter, ADC, successive approximation type ADC, ramp-compare ADC, and R-2R or binary weighted techniques in digital to analog converter, DAC. However, these layouts often provide capacity formations resulting in non-linearity in circuit operations.

US Patent Publication no. 8,149,152 B2 discloses a method and system for capacitor based digital to analog converter design layout for high speed analog to digital converter. Specifically, the patent document aims to eliminate parasitic capacitance in a capacitor based digital to analog converter, DAC by arranging a plurality of metal plates having a driven plate and a common plate, providing a plurality of interconnections in the common plate, extending the plate over the plurality of interconnects and shielding the common plate by the driven plate. However, the patent document has not mentioned that the routing of the binary or split weighted capacitor array includes switches.

US Patent Publication no. 5,952,952 A discloses a binary-weighted capacitor array that is applicable for use in analog-to-digital or digital-to-analog converters, switched-capacitor filters, etc. The patent document aims to eliminate top-plate parasitic error due to metal interconnections and metal overlap, ratio error due to oxide thickness gradients, and edge-definition errors. To achieve such effect, the patent document explains that it provides a plurality of unit capacitors arranged in a lateral row, where it is laid out in parallel to a switch array so that each metal interconnect between a unit capacitor and a corresponding switch is of a uniform length. However, the unit capacitor used is a 2D metal-oxide-metal, MOM type, and that the routing of the binary weighted capacitor array including switches are arranged in a single row.

In view of the deficiencies of the prior arts, there is therefore a need to provide a capacitor unit for building binary weighted split capacitor array with physical structures that are capable of promoting regularity and achieving linearity, thereby minimizing the routing induced parasitic mismatch.

Summary of Invention

The present invention relates to the building of a capacitor array for minimizing routing induced parasitic mismatch, and particularly, a method of building a binary weighted split capacitor array. More specifically, the binary weighted split capacitor array is built with unit capacitor with three-dimensional structures having a top plate

comprising a plurality of stacked metal plates and a bottom plate enclosing the top plate with side walls, a floor layer and a ceiling layer to minimize top plate parasitic capacitance to a substrate, and to achieve overall equal parasitic capacitance to the substrate.

It is an object of the present invention to provide a method of building a binary weighted split capacitor array with two different unit capacitors, one for use in the binary weighted part of the capacitor array and another one for use in bridging or attenuation part connecting two binary weighted sub-arrays in split array topology.

It is another object of the present invention to provide a method of building a binary weighted split capacitor array based on three-dimensional structures of the unit capacitor that promotes regularity.

It is a further object of the present invention to provide a method of building a binary weighted split capacitor array where the array is capable of minimizing routing induced parasitic mismatch.

Brief Description of the Drawings

Figure 1 illustrates a typical structure of successive approximation analog-to-digital converter, SAR ADC.

Figure 2 illustrates a typical capacitive digital-to-analog converter, CDAC block topology in a charge redistribution SAR ADC.

Figure 3 illustrates a CDAC block topology in a high resolution, in 10 bits or above, charge redistribution SAR ADC.

Figure 4 illustrates a model of a typical capacitor implemented in complementary metal-oxide semiconductor, CMOS technology.

Figure 5 illustrates a graphical example of large differential non-linearity, DNL error due to sudden jump when transiting from a low gain side, LSB to high gain side, MSB.

Figure 6 illustrates a graphical example of large differential non-linearity, DNL error resulting in missing codes at the vicinity of transition from low gain side, LSB to high gain side, MSB and vice versa.

Figure 7 illustrates a top plan view of the cross section of the unit capacitor.

Figure 8 illustrates a bottom plan view of the cross section of the unit capacitor, particularly cut from the second metal plate (M2).

Figure 9 illustrates a side plan view of the cross section of the unit capacitor.

Figure 10 illustrates a top plan view of the cross section of the attenuation capacitor, particularly cut from the fifth metal plate (M5).

Figure 11 illustrates a side plan view of the cross section of the attenuation capacitor.

Figure 12 illustrates an example of a conventional CDAC layout.

Figure 13 illustrates a proposed embodiment of the CDAC layout.

Figure 14 illustrates a layout of the binary weighted split capacitor array of the present invention.

Figure 15 illustrates a flow chart of the method of building a binary weighted split capacitor array.

Detailed Description of the Present Invention

The above mentioned and other features and objects of this invention will become more apparent and better understood by reference to the following detailed description.

It should be understood that the detailed description made known below is not intended to be exhaustive or limit the invention to the precise form disclosed as the invention may assume various alternative forms. On the contrary, the detailed description covers all the relevant modifications and alterations made to the present invention, unless the claims expressly state otherwise.

It is understood that typical structures and architectures of successive approximation analog-to-digital converter, SAR ADC comprises of a comparator, a capacitive digital-to-analog converter, CDAC with an embedded sample-and-hold, S/H circuit, and an SAR control logic circuit, as shown in Figure 1. In common practice, the CDAC block is implemented with topology shown in Figure 2 for most of the low resolution, 8-bits or below conversions. To achieve higher resolutions, topologies shown in Figure 3 are typically implemented. The reason for implementing such topology is the reduction of the total capacitor array size in terms of both area and capacitive value. Such topologies are known as binary weighted split capacitor array, where the capacitive array is split into several parts connected together by bridge or attenuation capacitors.

For medium to high resolution and high-speed applications, instead of using a binary weighted capacitor array structure for the CDAC sub-block, a binary weighted split capacitor array is usually adopted to achieve small total capacitance. Conventionally, only metal–insulator–metal, MIM capacitors are provided in foundry process design kit, PDK, which has a number of disadvantages such as being area-consuming and unfit for application in SAR ADCs. MIM capacitors feature a high capacitance density and a strict design rule checking, resulting in a both power hungry and big-area capacitive tank. In contrast to MIM capacitors, Metal-Oxide-Metal, MOM capacitors use oxide between metals as a dielectric to build a capacitor. To satisfy the operation of SAR ADCs, not only the capacitance, but its parasitic also need to be accounted. A general model of a MOM capacitor is illustrated in Figure 3. Generally, 'C_{pB}' stands for bottom plate parasitic while 'C_{pT}' stands for top plate parasitic of the MOM capacitor. 'C_U' is an expected unit capacitor, and 'DeltaC' represents an extra coupling factor between bottom and top plates. This is caused mostly by the extra coupling between routing wire and a certain capacitor plate, where usually the C_{pB} is much

larger than C_{pT}. The binary weighted split capacitor array structure suffers from high sensitivity to parasitic capacitor, especially the C_{pT} of the Least Significant Bit side, LSB. C_{pT}'s effect on the two separate sides can be regarded as gain errors. This is shown in Figure 4, where the topology illustrates a model of a typical capacitor implemented in complementary metal-oxide semiconductor, CMOS technology, which C_{pB} acts as the bottom plate parasitic, C_{pT} acts as the top plate parasitic, and DeltaC acts as the extra coupling capacitor between the top and bottom plates. Different gains at the two separate sides, MSB-side, LSB-side results in differential non-linearity, DNL errors. In the example of a 10-bit ADC, the gain difference leads to a large DNL error between every *"xxxxx11111"* and *"xxxxx00000"* transitions. Figure 5 illustrates in a more detailed manner on how different gains at the two separate sides result in DNL error graphically while Figure 6 shows that such errors can result in missing codes around the vicinity of transition when the errors are too large.

In order to minimize routing induced parasitic mismatch in a binary weighted split capacitor array, the present invention discloses a method for building a capacitor array (1). The method (1), as disclosed in the present invention, comprises the steps of arranging a plurality of capacitors in a first linear row, with symmetry to the center of the row, as a first segment of binary weighted capacitor (11); arranging a plurality of capacitors in a second linear row, with symmetry to the center of the row, as a second segment of binary weighted capacitor (12); arranging a plurality of capacitors in a third linear row, with symmetry to the center of the row (13); implementing interconnection between the first and second segments of the binary weighted capacitor through a custom attenuation capacitor (14); providing a plurality of switches along a linear row parallel to the first segment of binary weighted capacitor (15); providing a plurality of switches along a linear row parallel to the second segment of binary weighted capacitor (16); characterized in that the steps of arranging the plurality of capacitors in the first and second linear rows form a binary weighted split capacitor and the plurality of capacitors in the third linear row forms an attenuation capacitor, and that the capacitors are arranged with a top plate comprising a plurality of stacked metal plates (M1, M2, M3, M4, M5, M6) and a bottom plate enclosing the top plate with side walls, a floor layer and a ceiling layer to minimize top plate parasitic capacitance to the

substrate. With the customized three-dimensional MOM unit capacitors constructed from layers of metal inherent with the CMOS process that promotes regularity, the aforementioned problems faced commonly in split capacitor arrays are alleviated.

To achieve linearity, the method (1) provided by the invention produces three-dimensional unit capacitor where the top plate is enclosed entirely by the bottom plate metals with systematic layouts and arrangements that minimizes the routing induced parasitic mismatches. The physical structures with the binary weighted unit capacitor's top view, bottom view and side view are illustrated respectively in Figure 7, Figure 8 and Figure 9. As previously mentioned, the top plate of the unit capacitor is composed of a plurality of stacked metal plates, specifically from second metal plate (M2) to fifth metal plate (M5). Routing path for the top plate is formed by the fifth metal plate's (M5) layer extension in a two-directional manner. The bottom plate comprises the side walls represented by a plurality of metal plates from first to sixth metal plates (M1, M2, M3, M4, M5, M6), a floor represented by the first metal plate (M1) and a ceiling represented by the sixth metal plate (M6). The configuration of the top and bottom plates is best represented in Figure 9. Such a configuration also minimizes the top plate parasitic capacitance to the substrate, as the routing path of the bottom plate uses the floor layer for interconnection with the substrate. The routing is extended in two-directional directions that are perpendicular to the top plate to ensure parasitic capacitance is evenly distributed to each capacitor. In one embodiment of the present invention, the interconnection extends its lines in a transverse direction, or 90° from the first and third linear rows.

In one of the preferred embodiment of the present invention, the first segment of the binary weighted capacitor and the second segment of the binary weighted capacitor are interconnected, where the interconnection is implemented through a custom attenuation capacitor having equal parasitic on both top and bottom plates at the center of the row. The custom attenuation capacitor, or more particularly the unit capacitor arranged on the third linear row, comprises a top plate and a bottom plate where the parasitic are to be equal. This is to prevent a jump in gain error when codes transits from one segment of the binary weighted capacitor array to the next segment. Similar

to the binary weighted capacitor, the structure of the custom attenuation capacitor is also three-dimensional. The physical structure of the custom attenuation capacitor, specifically its top, bottom and side views are illustrated in Figure 10 and Figure 11. The top plate comprises a plurality of stacked metal plates from second to fifth metal plates (M2, M3, M4, M5), which are positioned at the center of the structure of the capacitor. Further, the second to fifth metal plates (M2, M3, M4, M5) are structured in a manner that they extend to the sides of the structure so that the parasitic equal to the bottom plate. However, the interconnection layer with other capacitors is still the fifth metal plate (M5). Similarly, the bottom plate comprises the side walls represented by a plurality of metal plates from first to sixth metal plates (M1, M2, M3, M4, M5, M6), a floor represented by the first metal plate (M1) and a ceiling represented by the sixth metal plate (M6). The configuration of the top and bottom plates is best represented in Figure 11. The routing path of the custom attenuation capacitor is also formed at the fifth metal plate (M5) that extends in four directions. Also, the routing path of the custom attenuation capacitor is formed at the bottom plate by the floor layer, extending in four directions.

Also described in the present invention is the provisions of a plurality of switches along the linear rows parallel to the first and second segments of the binary weighted capacitors. More specifically, the plurality of switches comprises equal and regular connections between gates of transistors in the switches with the first and second segments of binary weighted capacitors.

In another embodiment of the present invention, the binary weighted split capacitor array is also built based on the steps depicted hereunder, and they include defining the split capacitor architecture to be used, defining the number of binary weighted capacitor to be used at each capacitor array segment, laying out the binary weighted capacitor array by arranging customized unit capacitor in a symmetrical order where both sides have equal number of the customized unit capacitor, connecting the binary weighted capacitor array segments through the customized attenuation capacitor, characterizing the parasitic of the entire split capacitor array to ensure that the parasitic within the array is equal, laying out the interconnection between the unit capacitors in

binary weighted array segment and switches to make sure that the parasitic is equal and regular, and laying out shielding wires between the layout of the binary weighted array segment and layout of the switches. Further to the steps mentioned above, the definition of the architecture is important as it determines whether the capacitor is a single, dual or triple attenuation capacitor. The customized unit capacitor mentioned above is referring to the unit capacitors disclosed in the preferred embodiment of the present invention. Particularly, they are capacitors with three-dimensional structures with top and bottom plates having multiple stacked metal plates that provides equal parasitic to the overall structure of the capacitor array.

To provide a better understanding of the present invention, Figure 12 is provided to illustrate an example of a conventional CDAC layout, Figure 13 is to illustrate a proposed embodiment of the CDAC layout and Figure 14 is to illustrate a layout of the preferred embodiment of the present invention. The layout in Figure 12 illustrates placement implementation in conventional binary weighted split capacitor array comprising unit capacitors of 16C, 8C, 4C, 2C, 1C, including both LSB binary weighted array and MSB binary weighted array, and an attenuation capacitor connecting the LSB and MSB arrays. The top plates of all unit capacitors are connected to each other to build a common top node. However, this type of routing contributes to non-linearity due to the non-regular and un-equal parasitic for each individual binary weight capacitor, i.e. especially 16C, 8C, 4C, 2C, 1C when routing to the CDAC switches are taken into account. It is believed that such conventional common-centroid layout is not suitable for binary weighted capacitor array split structure, because common top plate connection is so complex that its parasitic capacitance to ground, $C_{parasitic}$ is so large that it deteriorates the static and dynamic performance.

Further, in Figure 13, the bottom-plate routing of each unit capacitor is extended to the directions of the top and bottom plates in a regular and equal manner to the CDAC switches. This minimizes systematic non-linearity by ensuring the routing itself is binary weighted and hence it is parasitic. The use of custom attenuation capacitor in this layout also ensures that no jump in gain error will happen for the layout of binary

weighted split capacitor array. Figure 14 best represents the embodiment of the binary weighted split capacitor array of the present invention. Effective capacitance of each unit capacitor, C_{UNIT_EFF} is thus composed of C_U, by the pillar-shape top plate with enclosing bottom plate, C_{pR} and C_{pB}, where [$C_{UNIT\_EFF} = C_U + C_{pR} + C_{pB}$]. Thus, if C_{pR} and C_{pB} are also binary weighted, then it is believed that the ratio of capacitances in such a layout is binary weighted even taking into account the routing to the switches and the parasitic contributed by routing from the bottom plate.

Although specific embodiments of the present invention have been described, it will be understood by those of skill in the art they are not intended to be exhaustive or to limit the invention to the precise forms disclosed and obviously many modifications and variations are possible in view of the above teachings, including equivalents. Accordingly, it is to be understood that the invention is not to be limited by the specific illustrated embodiments, but only by the scope of the appended claims.

Claims

1. A method of building a capacitor array (1) for minimizing routing induced parasitic mismatch, the method (1) comprising the steps of:

arranging a plurality of capacitors in a first linear row, with symmetry to the center of the row, as a first segment of binary weighted capacitor (11);

arranging a plurality of capacitors in a second linear row, with symmetry to the center of the row, as a second segment of binary weighted capacitor (12);

arranging a plurality of capacitors in a third linear row, with symmetry to the center of the row (13);

implementing interconnection between the first and second segments of the binary weighted capacitor through a custom attenuation capacitor (14);

providing a plurality of switches along a linear row parallel to the first segment of binary weighted capacitor (15);

providing a plurality of switches along a linear row parallel to the second segment of binary weighted capacitor (16);

characterized in that the steps of arranging the plurality of capacitors in the first and second linear rows form a binary weighted split capacitor and the step of arranging the plurality of capacitors in the third linear row forms an attenuation capacitor, and that the capacitors are arranged with a top plate comprising a plurality of stacked metal plates (M1, M2, M3, M4, M5, M6) and a bottom plate enclosing the top plate with side walls, a floor layer and a ceiling layer to minimize top plate parasitic capacitance to the substrate.

2. The method (1) according to claim 1, wherein the interconnection between the first and second segments of the binary weighted capacitor is implemented through the custom attenuation capacitor to provide equal parasitic on both top and bottom plates at the center of the row.

3. The method (1) according to claim 1, wherein the plurality of switches along the linear row parallel to the first segment of binary weighted capacitor comprises

equal and regular connection between gates of transistors in the switches with the first segment of binary weighted capacitor.

4. The method (1) according to claim 1, wherein the plurality of switches along the linear row parallel to the second segment of binary weighted capacitor comprise equal and regular connection between gates of transistors in the switches with the second segment of binary weighted capacitor.

5. The method (1) according to claim 1, wherein the plurality of stacked metals in the top plate of the capacitors in the first and second linear rows comprises second (M2), third (M3), fourth (M4) and fifth (M5) metal plates, with a two-directional routing path formed by the fifth metal plate (M5).

6. The method (1) according to claim 1, wherein a routing path of the capacitors in the first and second linear rows is formed at the bottom plate by the floor layer, extending in two directions that are perpendicular to top plate routing to ensure parasitic capacitance is evenly distributed to each capacitor.

7. The method (1) according to claim 1, wherein the plurality of stacked metals in the top plate of the capacitors in the third linear row comprises second (M2), third (M3), fourth (M4) and fifth (M5) metal plates that are positioned at the center of the structure of the capacitors, and structured in a manner that they extend to the side of the structure of the capacitors.

8. The method (1) according to claim 1, wherein the top plate of the capacitors in the third linear row comprises routing path formed by the fifth metal plate (M5) that extends to four directions.

9. The method (1) according to claim 1, wherein a routing path of the capacitors in the third linear row is formed at the bottom plate by the floor layer, extending in four directions.

10. A binary weighted split capacitor array obtained from the method (1) as claimed in claim 1.

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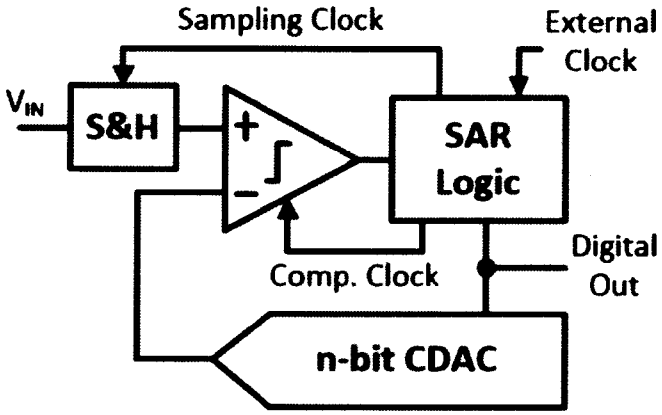
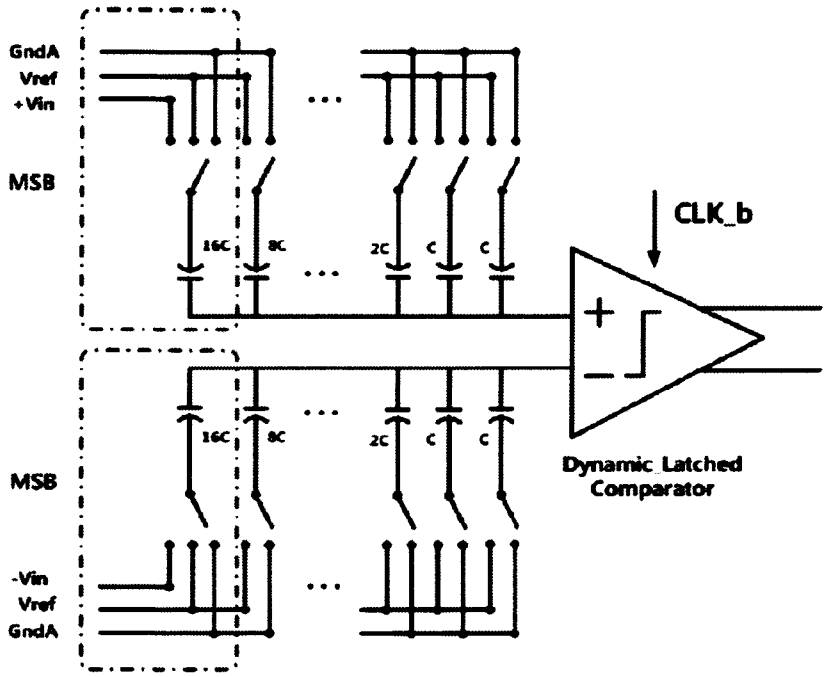


Figure 1



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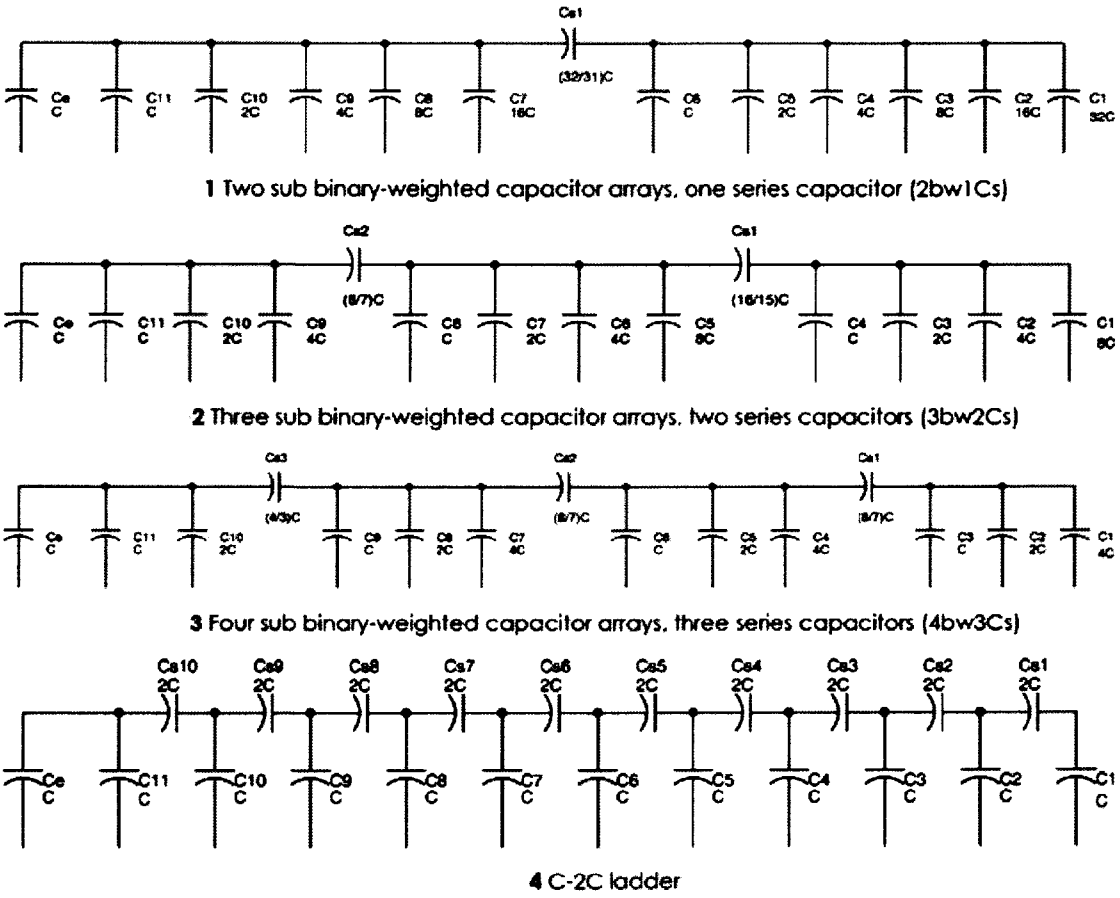

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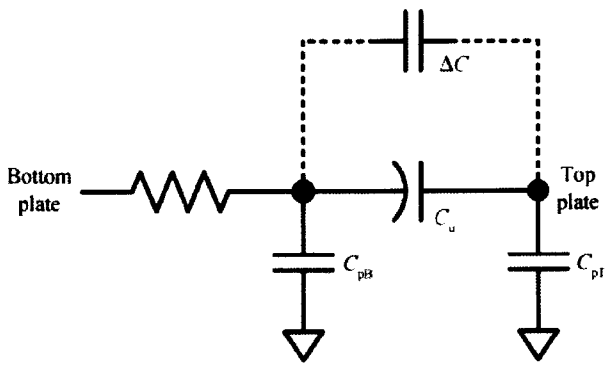

Figure 4

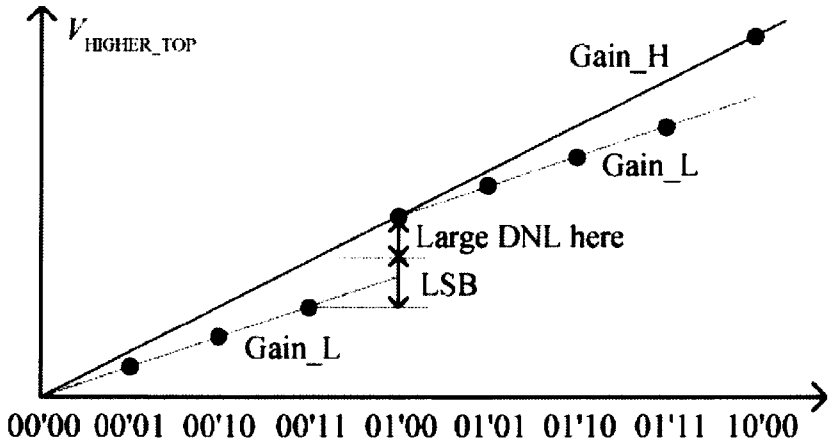

Figure 5

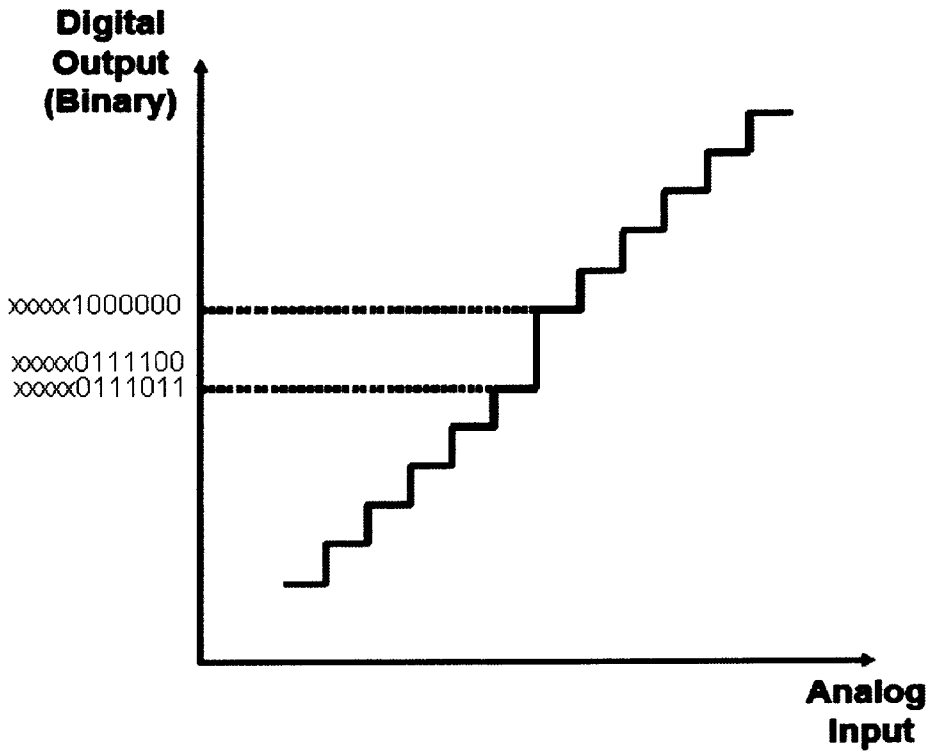

Figure 6

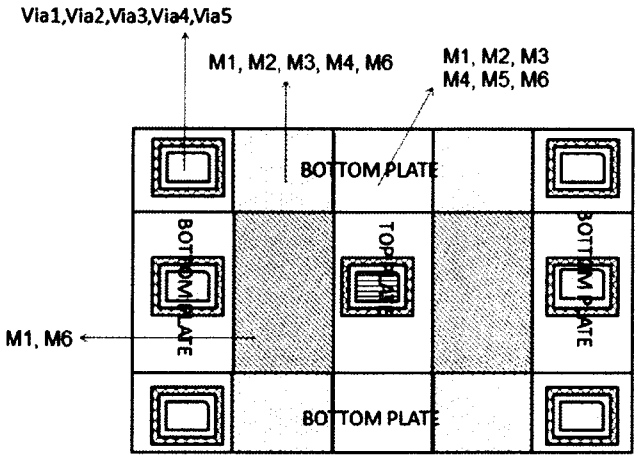

Figure 7

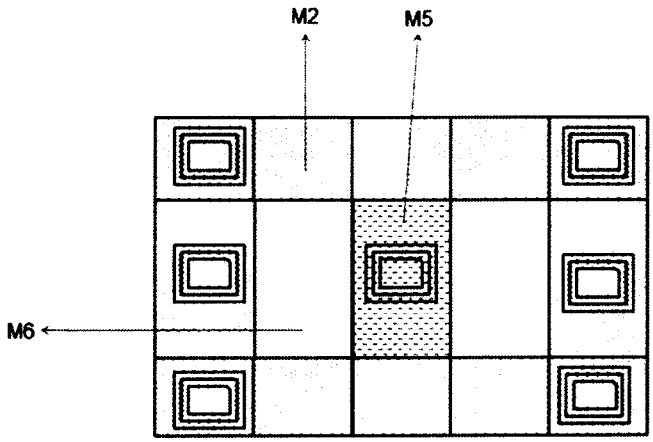

Figure 8

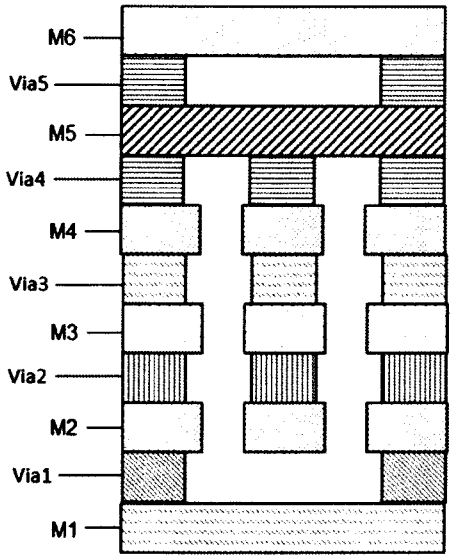

Figure 9

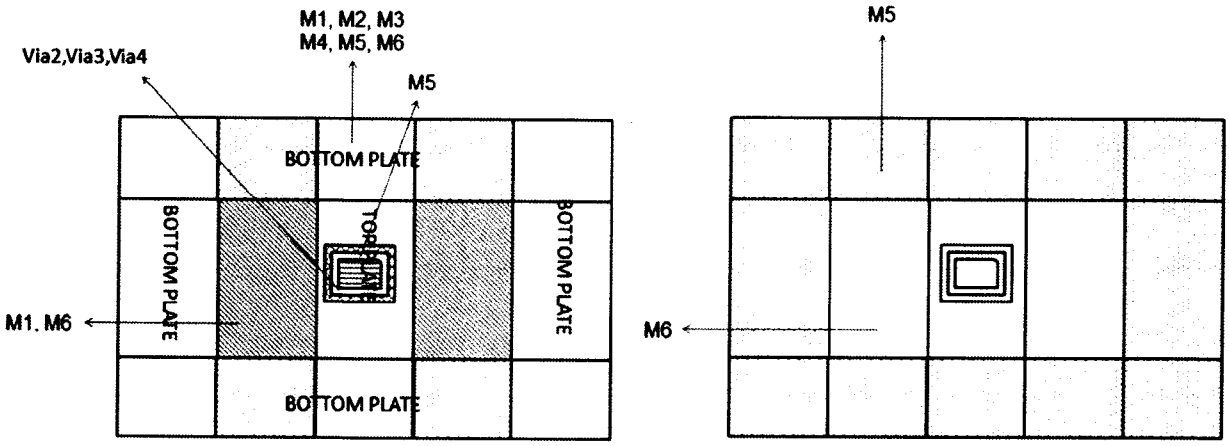

Figure 10

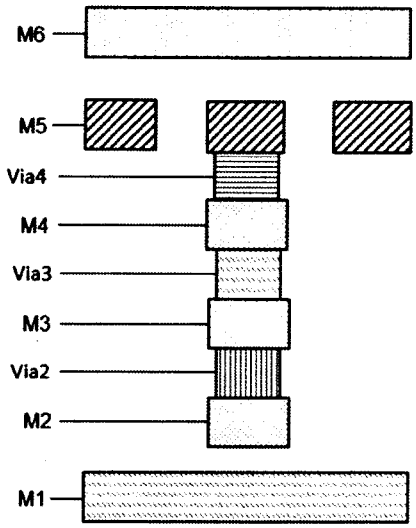

Figure 11

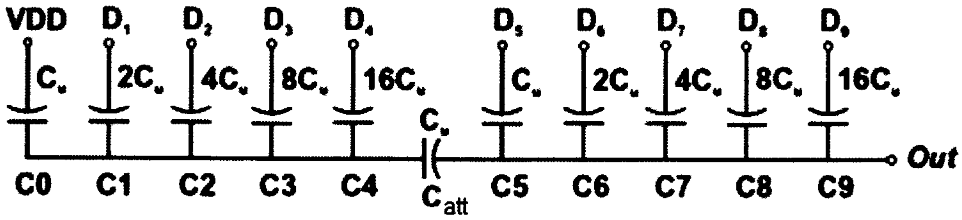

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Figure 12

D	D	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	D	D

D	D	C9	C8	C9	C7	C9	C8	C9	C6	C9	C8	C9	C7	C9	C8	C9	C5	C9	C8	C9	C7	C9	C8	C9	C6	C9	C8	C9	C7	C9	C8	C9	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Catt	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	C4	C3	C4	C2	C4	C3	C4	C1	C4	C3	C4	C2	C4	C3	C4	C0	C4	C3	C4	C2	C4	C3	C4	C1	C4	C3	C4	C2	C4	C3	C4	D	D

D	D	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	SW	D	D

Figure 13

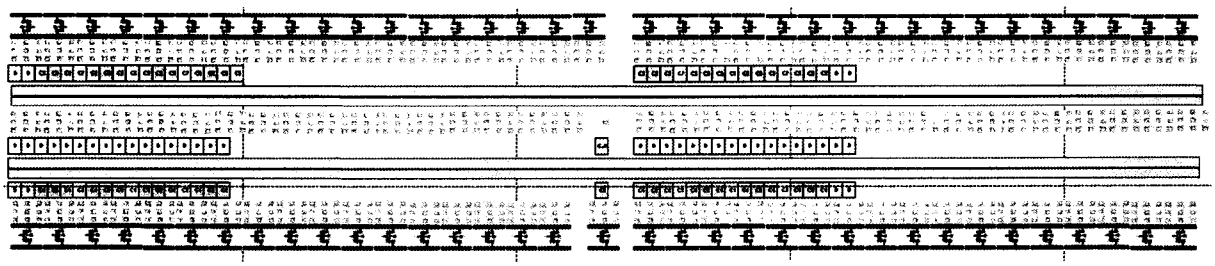

Figure 14

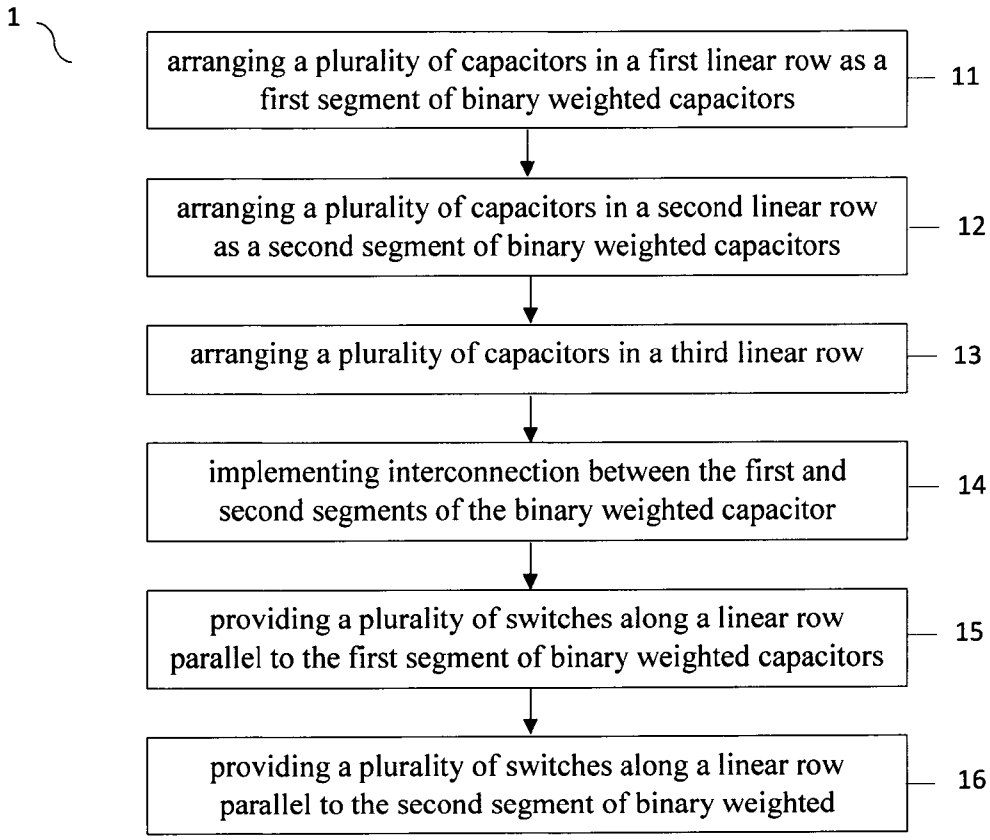

Figure 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2019/000031

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L21/822(2006.01)i, H01L21/82(2006.01)i, H01L27/04(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L21/822, H01L21/82, H01L27/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2019
Registered utility model specifications of Japan 1996-2019
Published registered utility model applications of Japan 1994-2019

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 104143982 A (SHANGHAI LINGWOBO INTELLIGENT TECHNOLOGY CO., LTD.) 2014.11.12, (No Family)	1-10
A	US 2014/0049872 A1 (HIMAX TECHNOLOGIES LIMITED) 2014.02.20, (No Family)	1-10
A	US 7473955 B1 (ALVAND TECHNOLOGIES, INC.) 2009.01.06, (No Family)	1-10
A	US 7456462 B1 (ALVAND TECHNOLOGIES, INC.) 2008.11.25, (No Family)	1-10
A	WO 2017/168521 A1 (OLYMPUS CORPORATION) 2017.10.05, & US 2018/0351568 A1	1-10

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17.10.2019	29.10.2019

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