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(54) METHOD TO PREVENT STATIC DESTRUCTION OF AN ACTIVE ELEMENT COMPRISED IN A LIQUID CRYSTAL DISPLAY DEVICE

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(22) Filed: **Dec. 8, 2004**

Related U.S. Application Data

(62) Division of application No. 10/458,198, filed on Jun. 11, 2003, which is a division of application No. 09/903,639, filed on Jul. 13, 2001, now Pat. No. R,E38,292.

(30) **Foreign Application Priority Data**

Oct. 3, 1995 (JP) 7-279587

Publication Classification

(51) **Int. Cl.**[7] **H01L 31/036**; H01L 21/84

(52) **U.S. Cl.** **257/72**; 257/59; 438/149; 438/151; 257/350; 257/351

(57) ABSTRACT

A liquid crystal display device which utilizes an active matrix substrate and its substrate, and which is provided with a novel method of manufacture which can reduce the manufacturing process of amorphous silicon thin film transistors of reverse stagger construction, and an electrostatic protection means which is created using this method of manufacture. In a thin film transistor manufacturing process, along with forming an aperture for connecting the contact hole and the external terminal in a manufacturing process for a thin film transistor, utilization is made of ITO film as the wiring. The electrostatic protection means is formed from a bidirectional diode (electrostatic protection element) which is composed utilizing an MOS transistor connected between the electrode (PAD) for connecting the external terminal, and the joint electric potential line. The electrostatic protection element is substantially a transistor, with great current capacity, and utilizing the TFT formation process of pixel components in their existent state, the process can be formed without any complications.

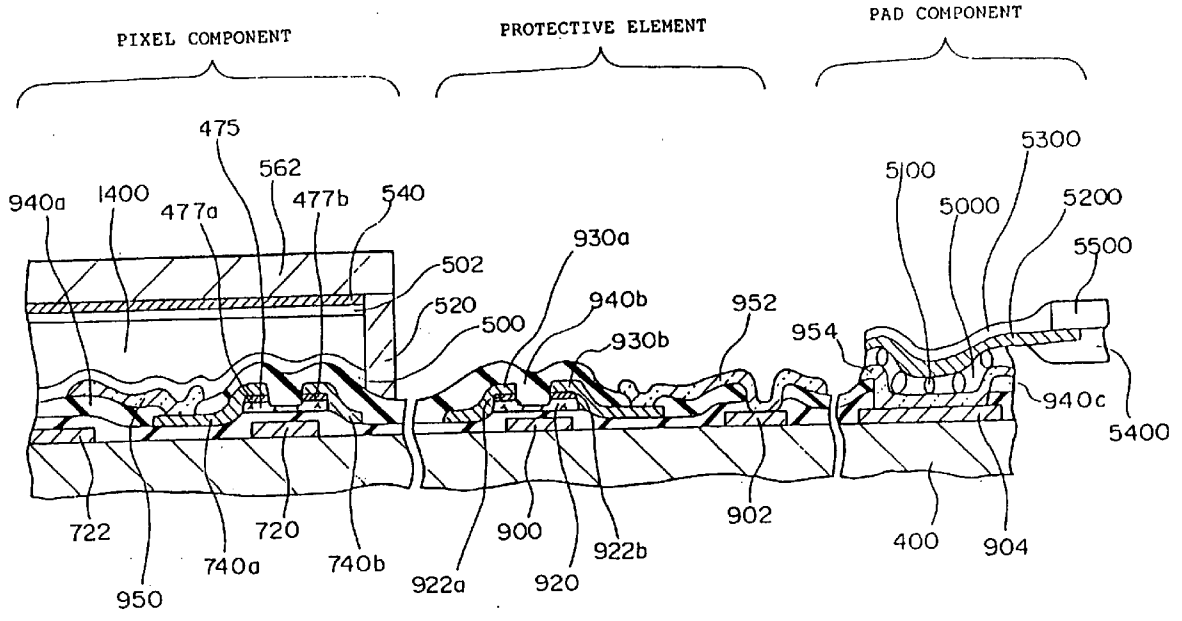


FIG. 1

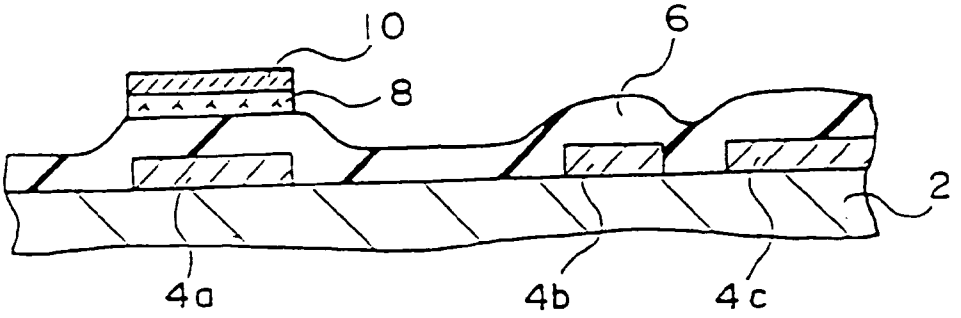


FIG. 2

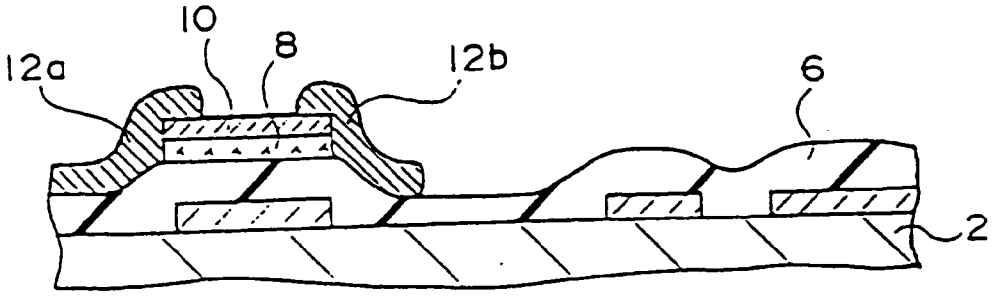


FIG. 3

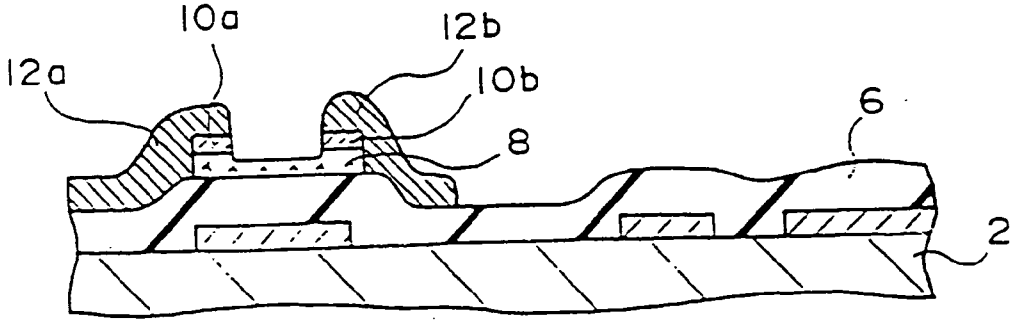


FIG.4

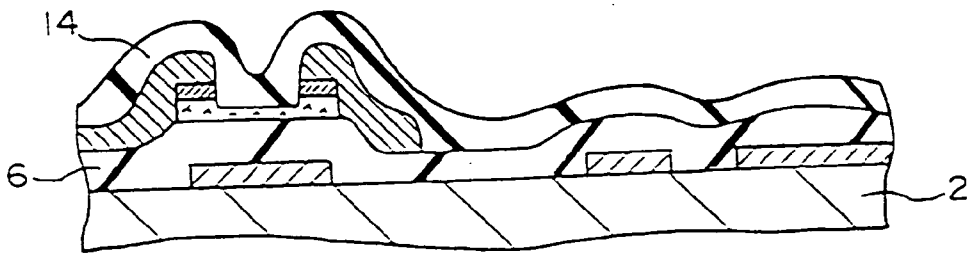


FIG.5

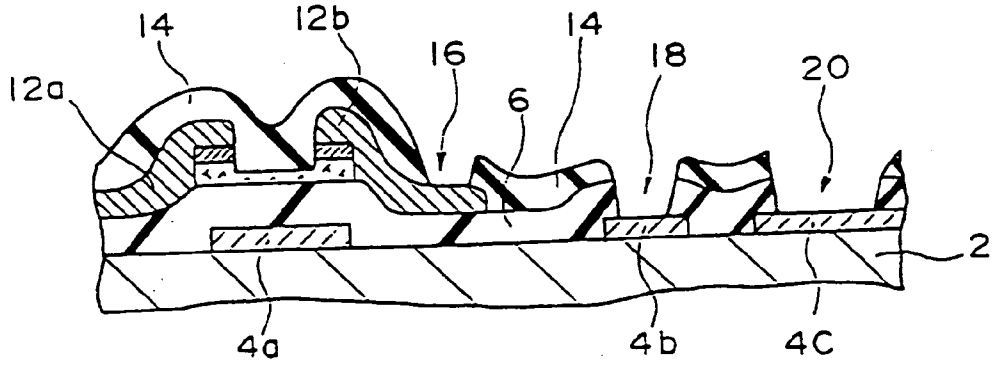


FIG.6

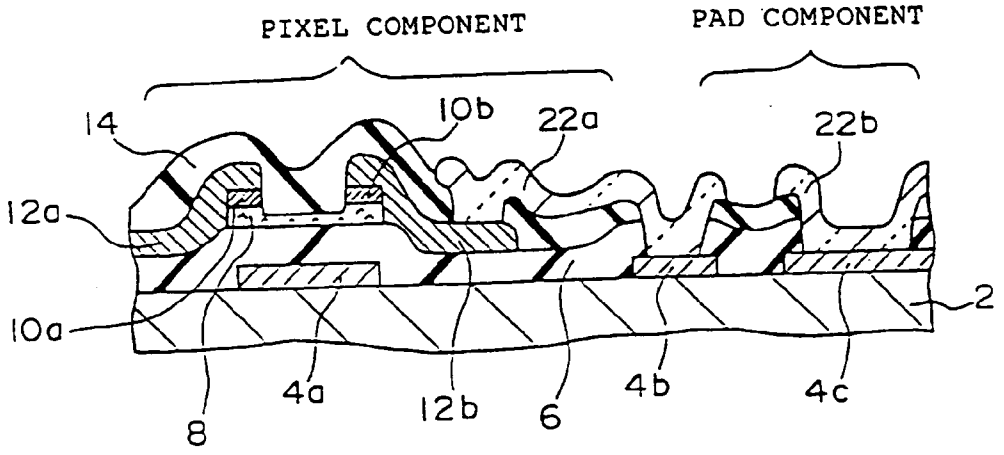


FIG. 7A

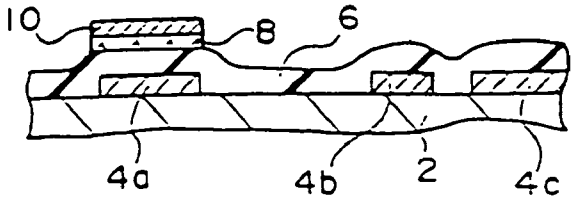


FIG. 7B

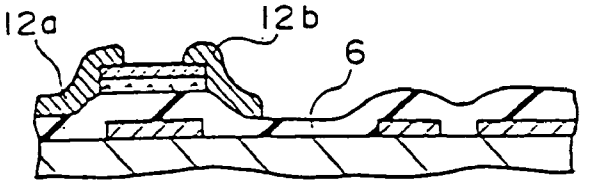


FIG. 7C

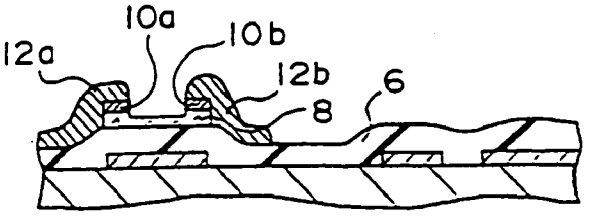


FIG. 7D

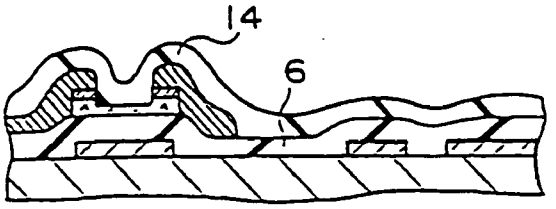


FIG. 7E

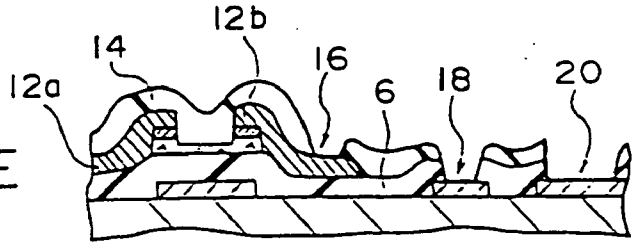


FIG. 7F

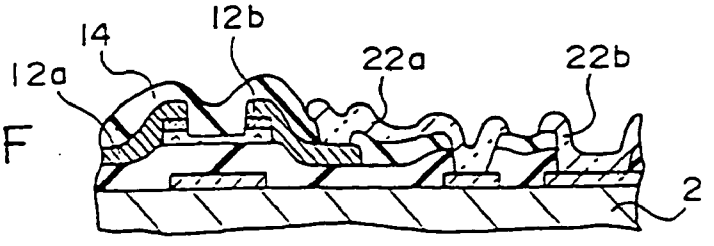


FIG. 8A

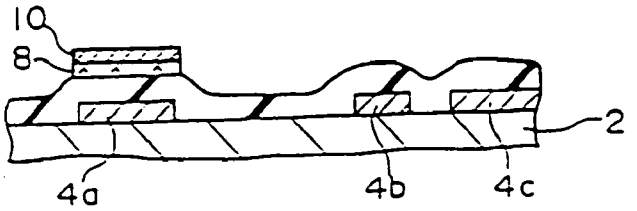


FIG. 8B

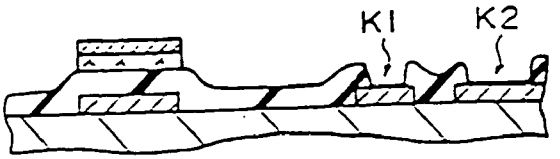


FIG. 8C

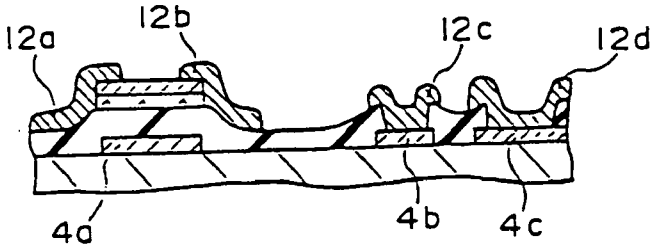


FIG. 8D

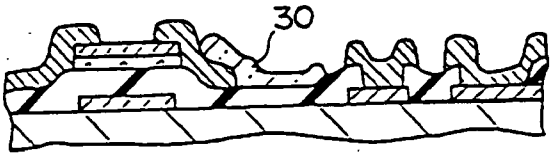


FIG. 8E

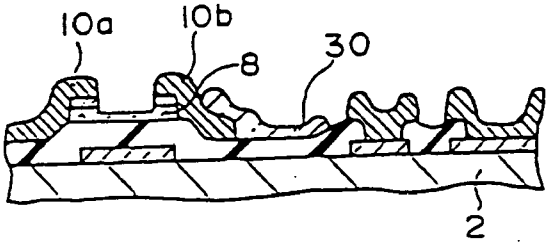


FIG. 8F

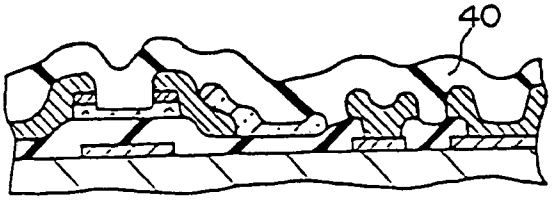


FIG. 8G

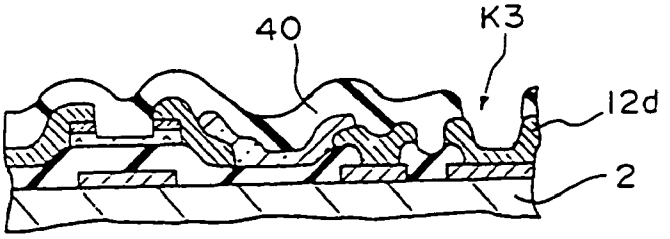


FIG.9

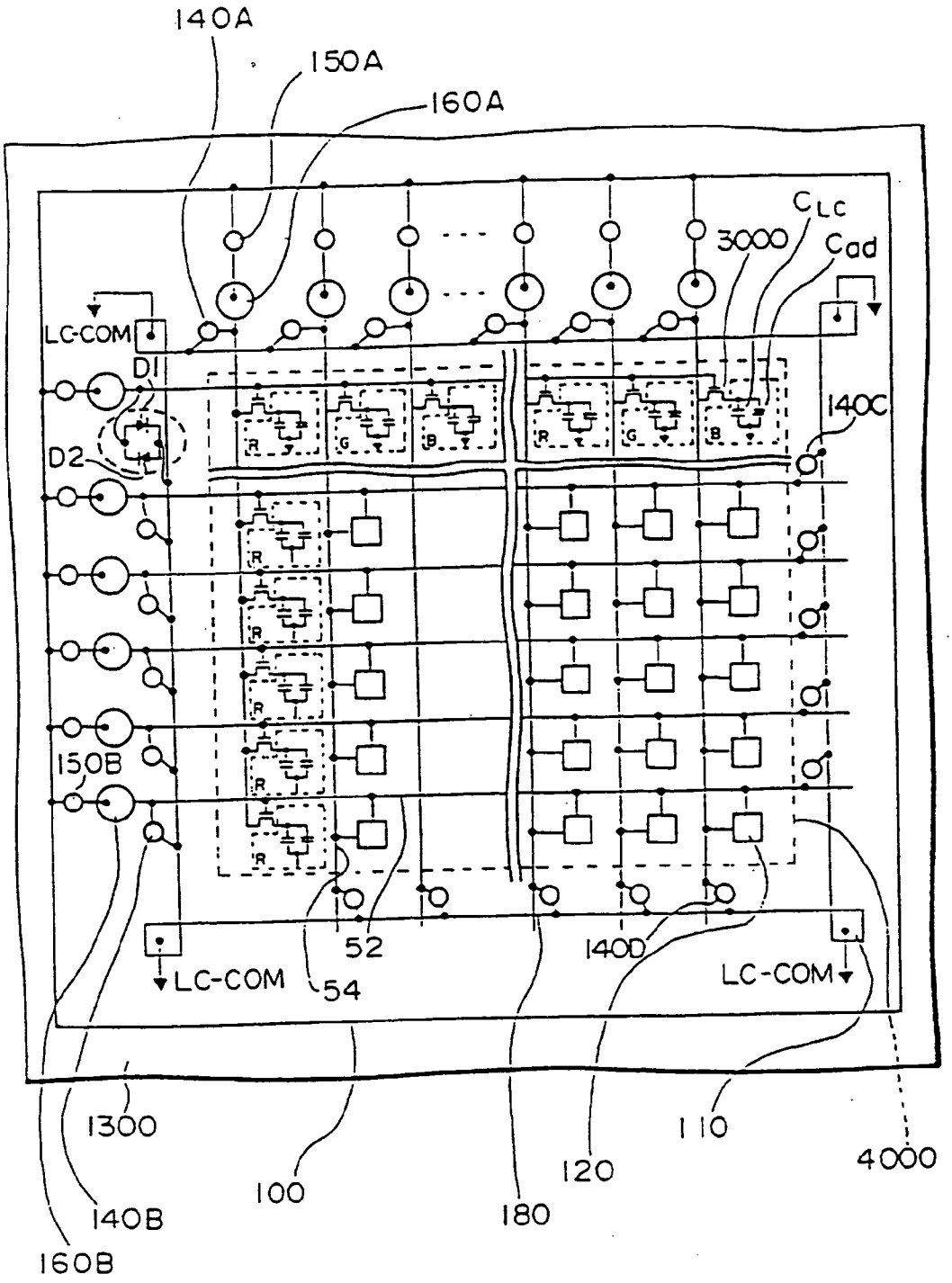

140A
150A
160A
C_{LC}
3000
C_{ad}
LC-COM
D1
D2
140C
R
G
B
150B
52
54
LC-COM
1400
LC-COM
1300
100
180
120
110
4000
140B
160B

FIG. 10

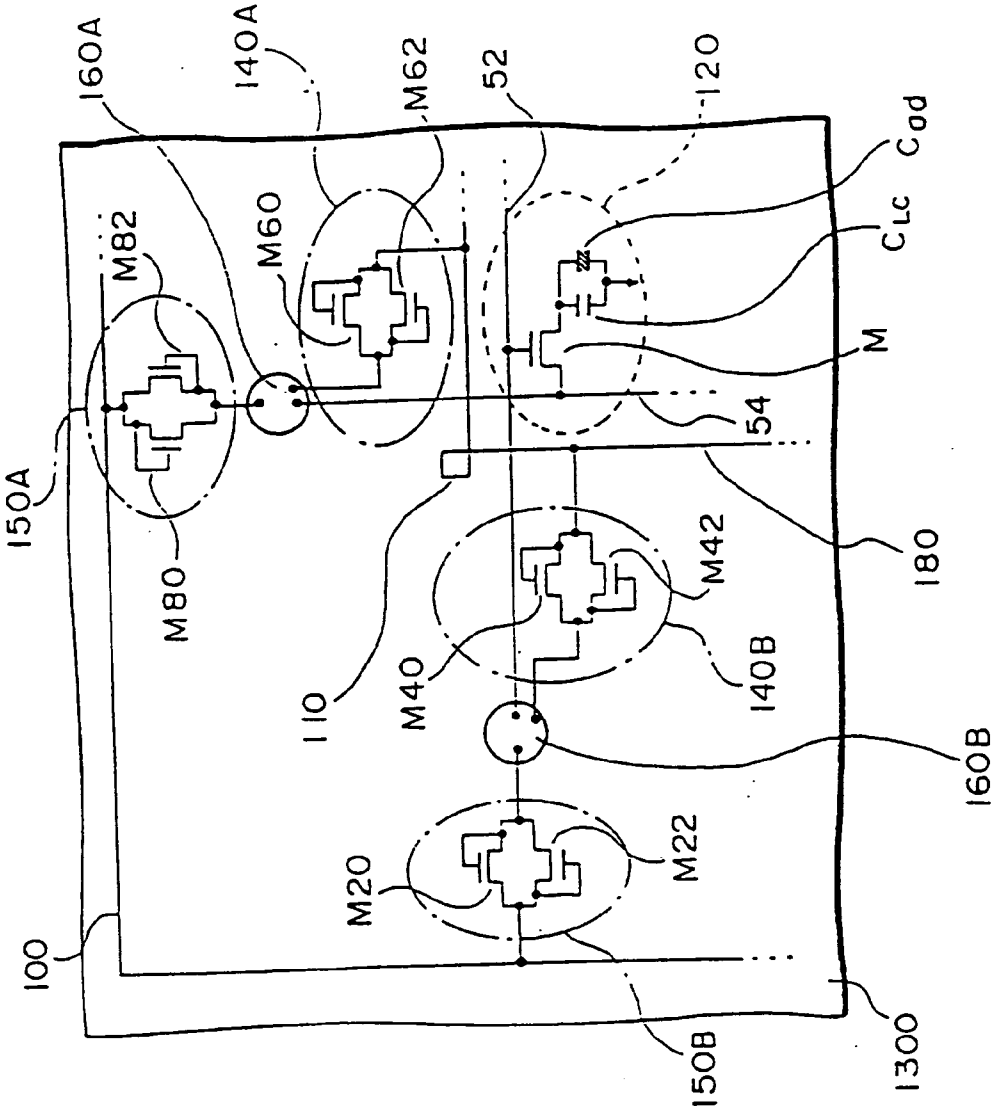

160A
140A
M62
52
120
Cod
CLC
M82
M60
M
54
150A
M80
180
M42
M40
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110
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M22
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100
150B
1300

FIG.11A

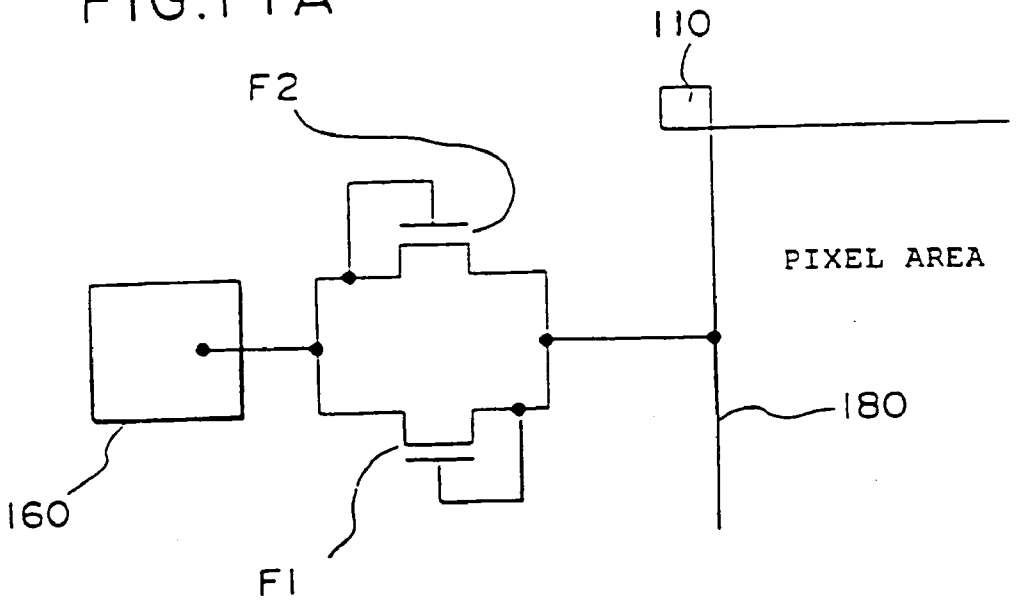


FIG.11B

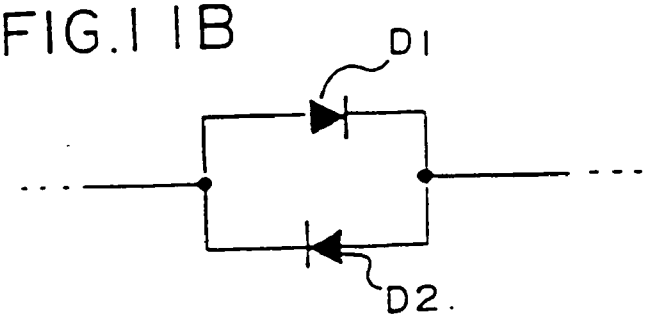


FIG.11C

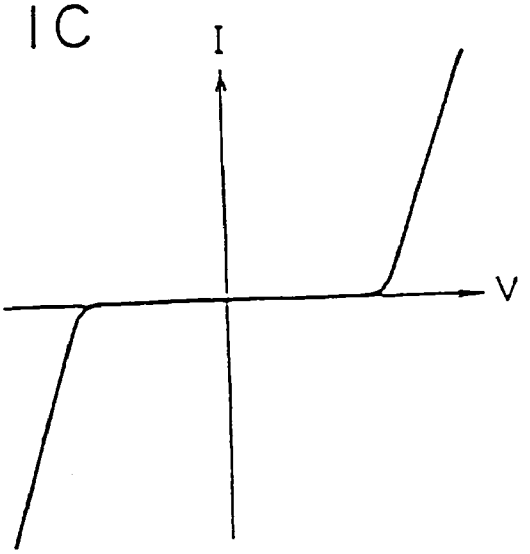
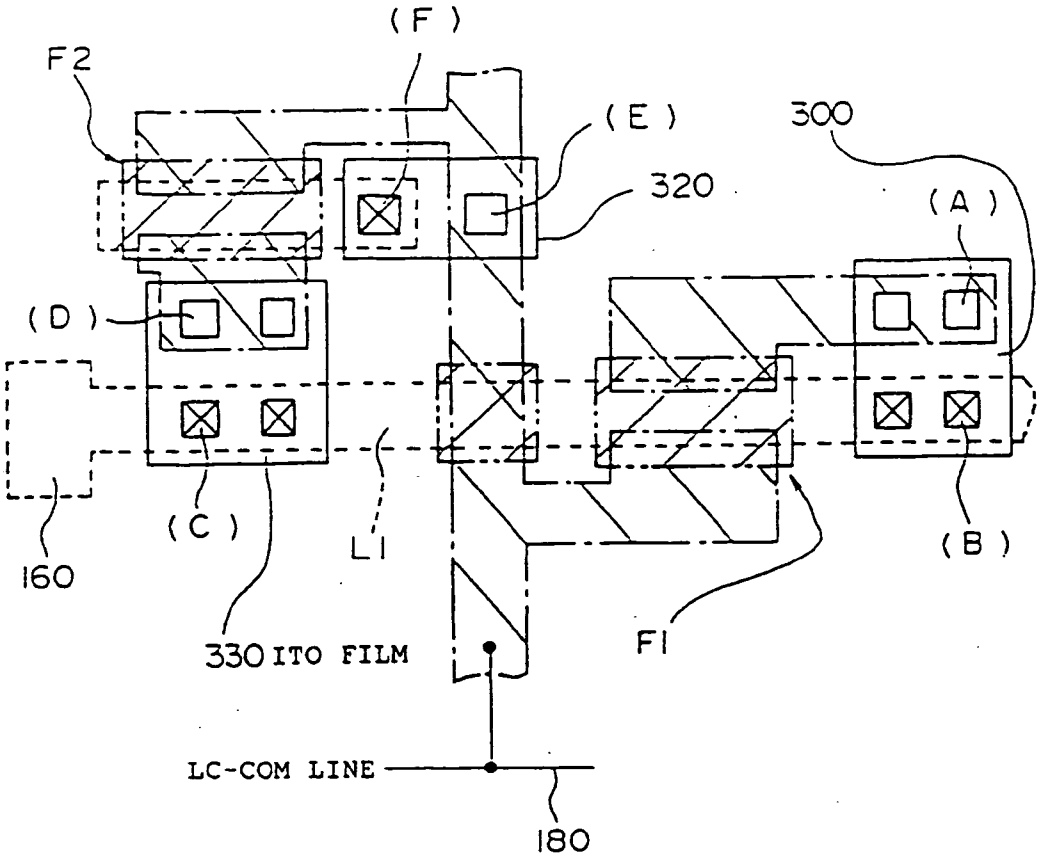


FIG.12



------ ; GATE ELECTRODE (FIRST LAYER)

—·—·— ; AMORPHOUS SILICON (SECOND LAYER)

—·— ; SOURCE ELECTRODE, DRAIN ELECTRODE, JOINT ELECTRIC POTENTIAL (LC-COM) ELECTRODE AND THE LIKE (THIRD LAYER)

——— ; ELECTRODE FORMED FROM ITO (LAYER 4)

□ ; CONTACT HOLE FOR CONNECTING LAYER 3 AND LAYER 4

⊠ ; CONTACT HOLE FOR CONNECTING LAYER 1 AND LAYER 4

▨ ; TFT FORMATION REGION

▧ ; ELECTRODE AND WIRING UTILIZING LAYER 3

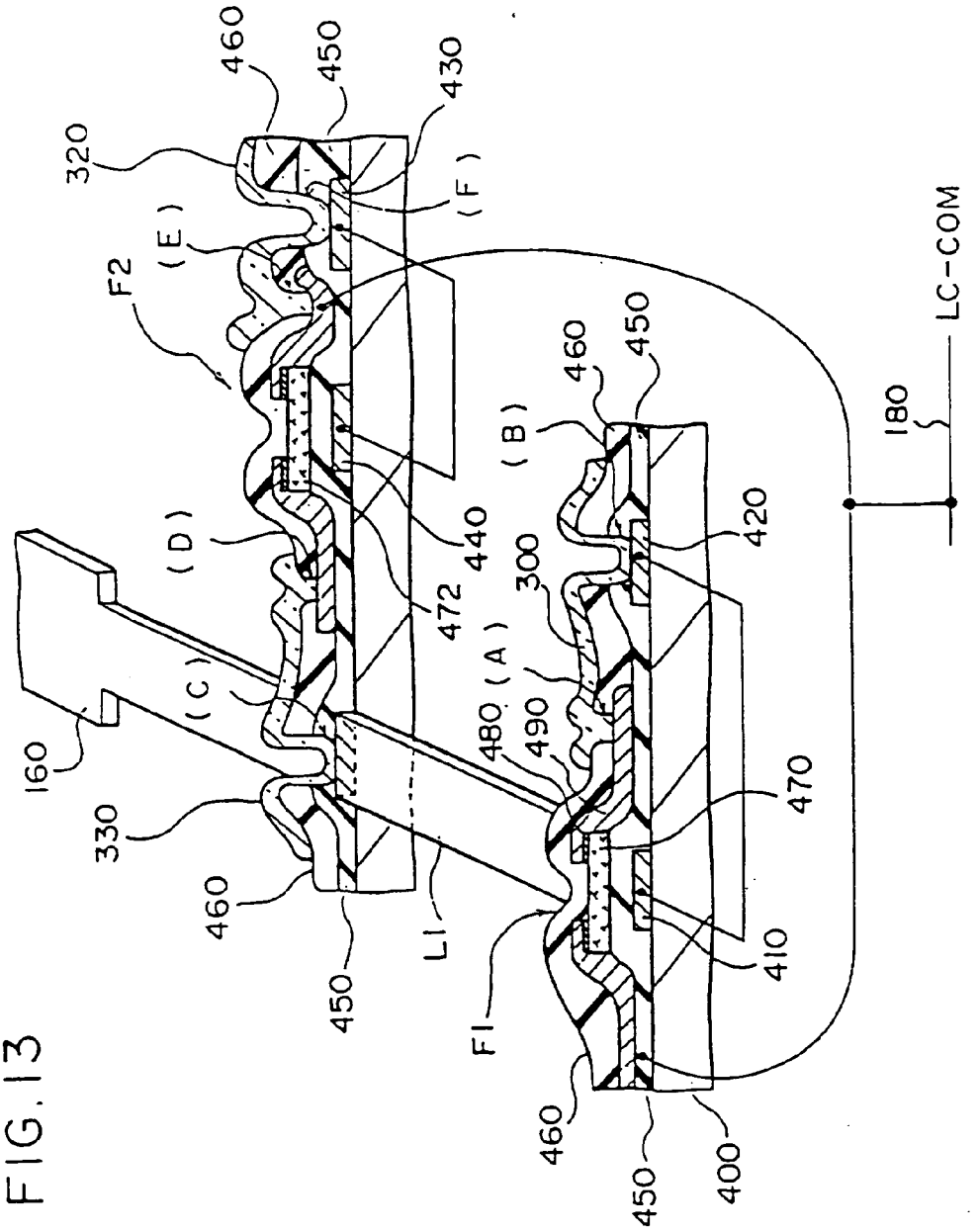

460
450
430
320
(F)
(E)
F2
LC-COM
180
460
450
(B)
(D)
440
420
300
472
(A)
(C)
480
490
160
470
330
460
L1
410
450
F1
460
450
400

FIG. 13

FIG. 14

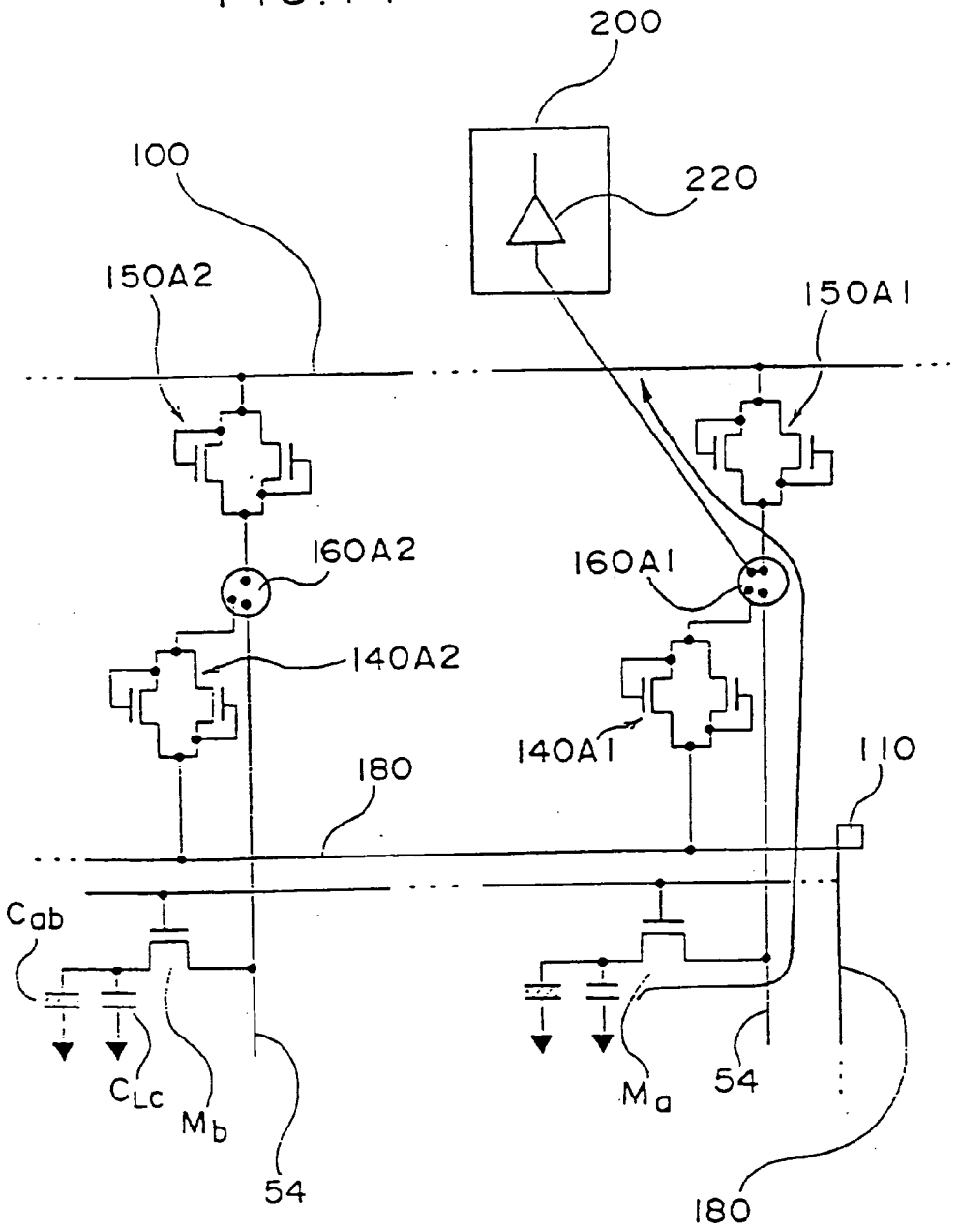
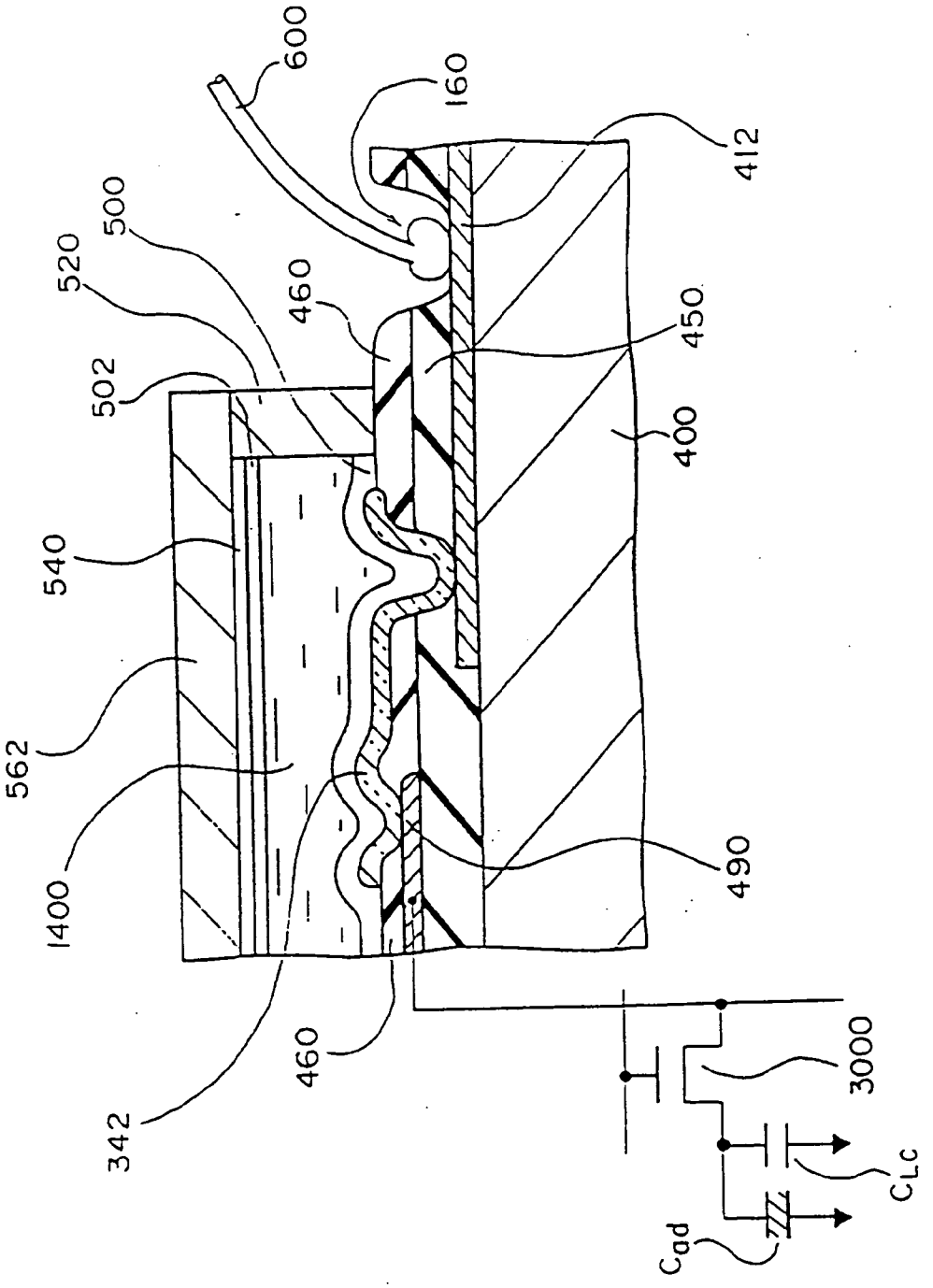

200
220
100
150A2
150A1
160A2
160A1
140A2
140A1
180
110
Cab
CLC
Mb
54
Ma
54
180

FIG. 15


600
160
412
500
520
460
450
502
400
540
562
1400
490
342
460
3000
C_{LC}
C_{ad}

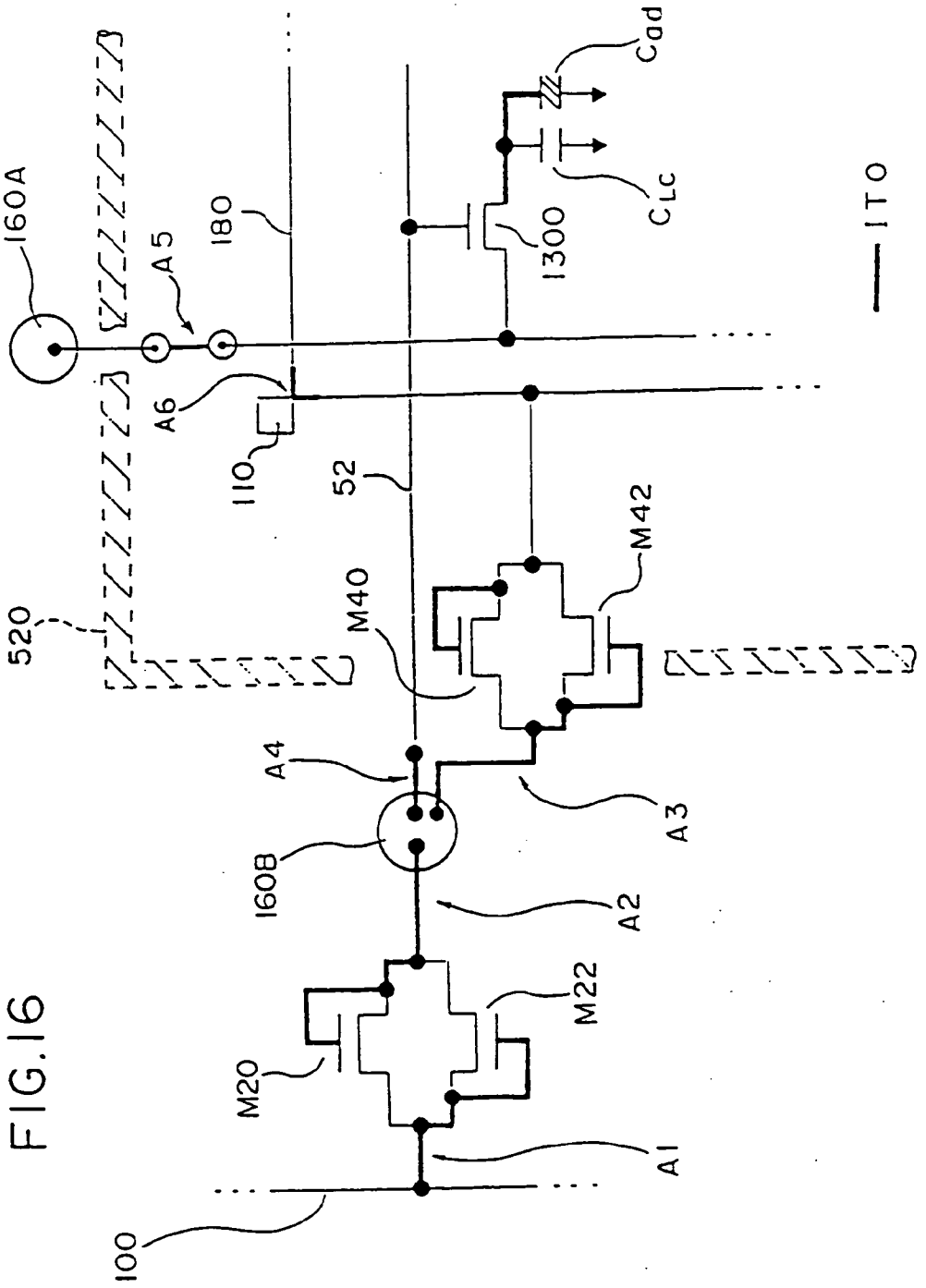

160A
A5
180
Cad
CLC
1300
ITO
A6
110
52
M42
M40
520
A4
A3
160B
A2
M22
M20
A1
100

FIG. 16

FIG.17

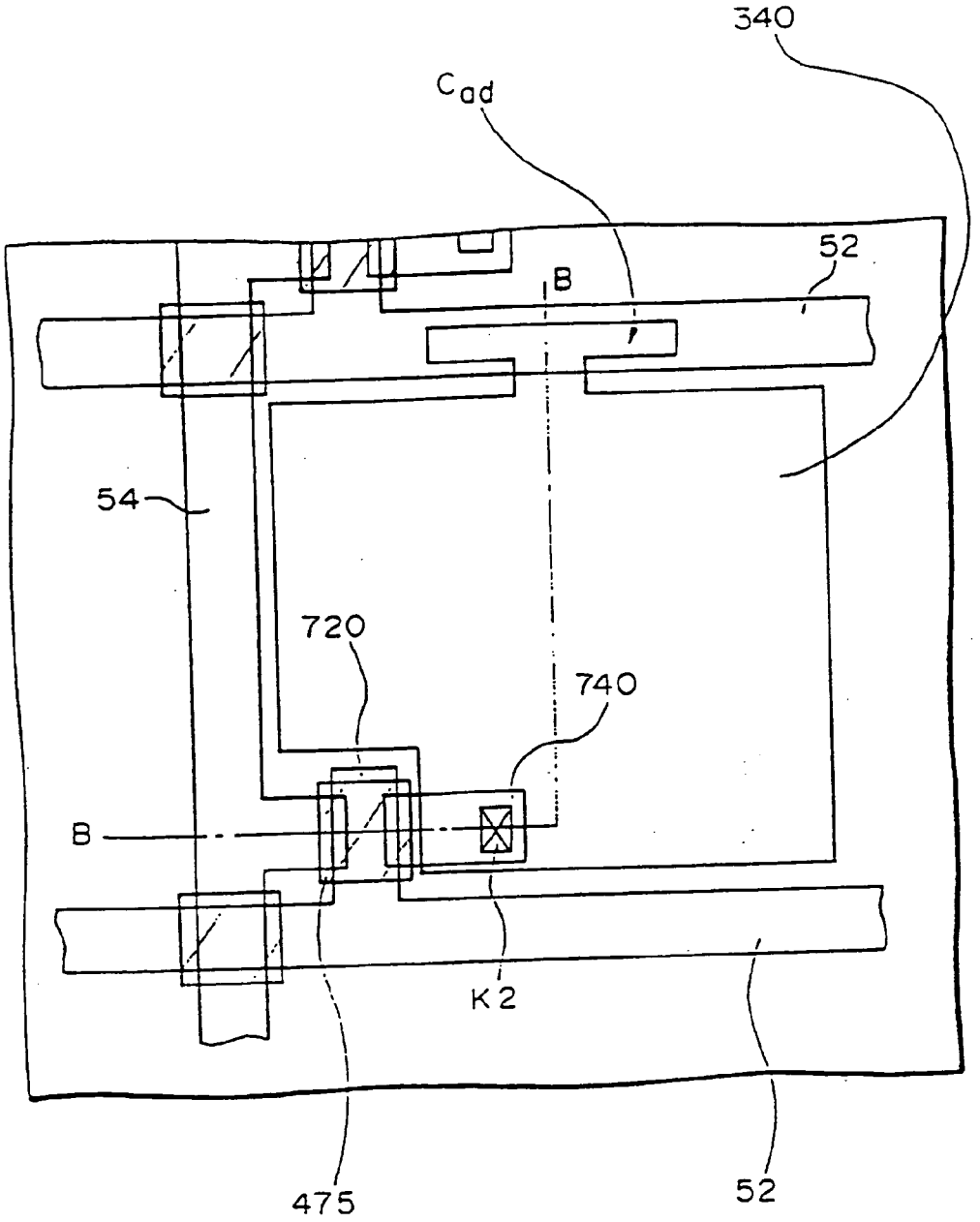


FIG. 18

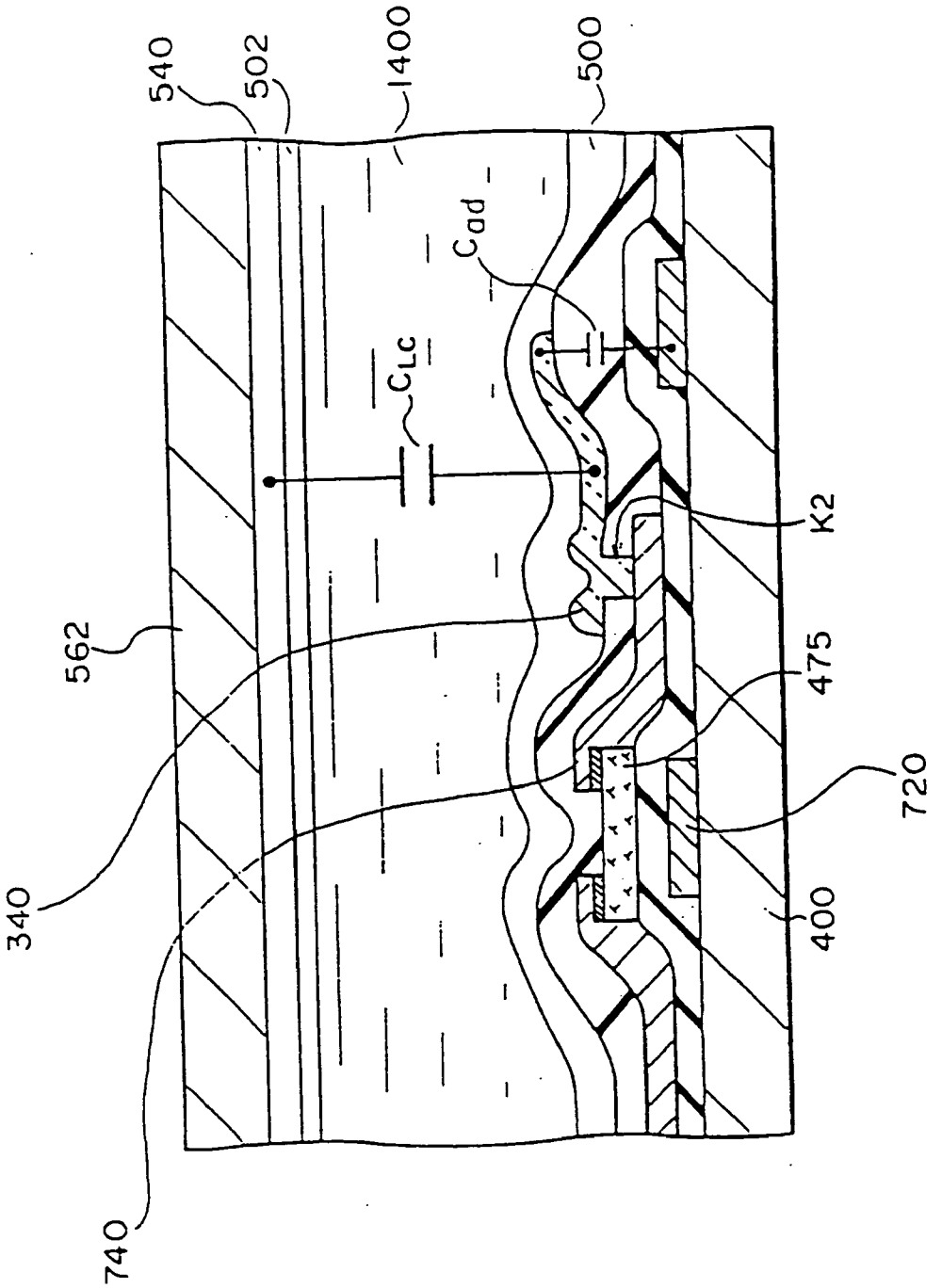


FIG. 19

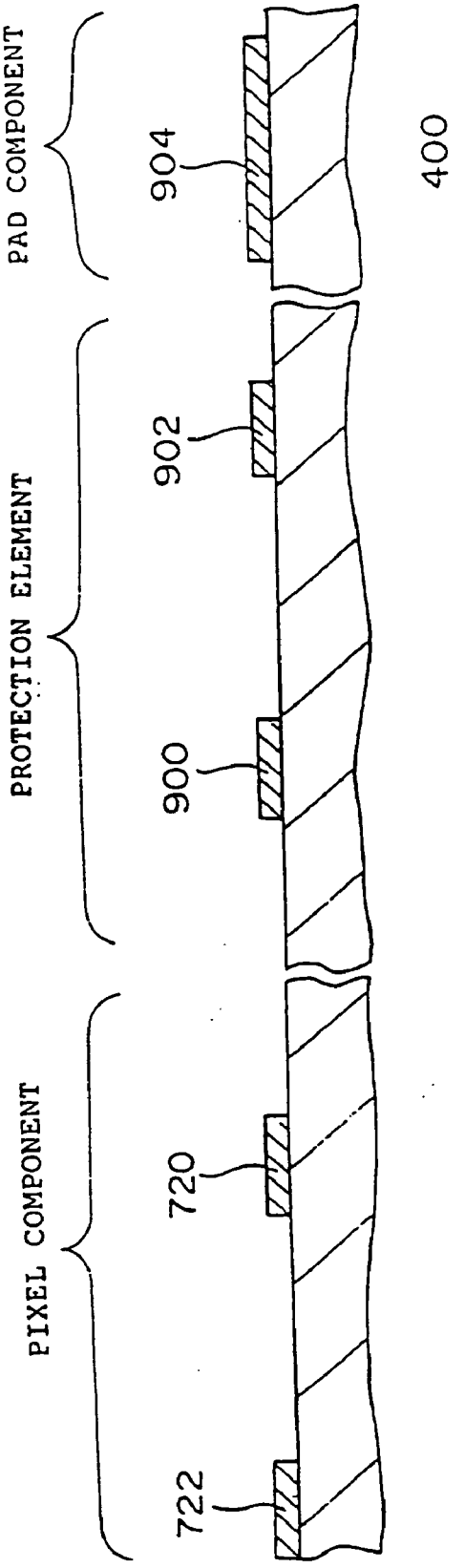

PAD COMPONENT
PROTECTION ELEMENT
PIXEL COMPONENT
904
902
900
720
722
400

FIG. 20

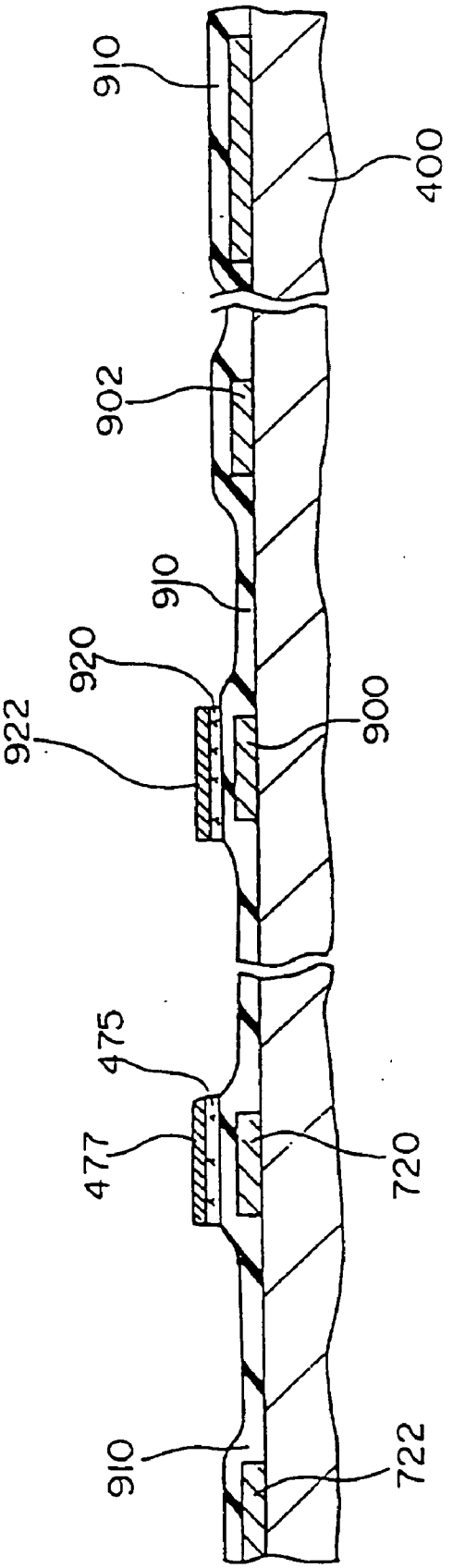


FIG. 21

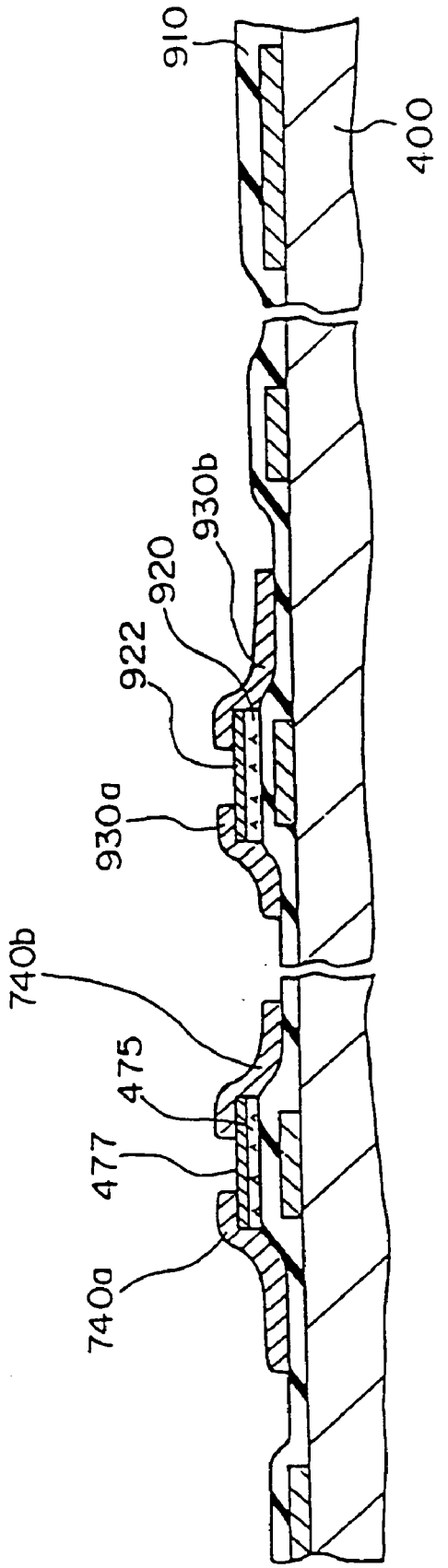


FIG. 22

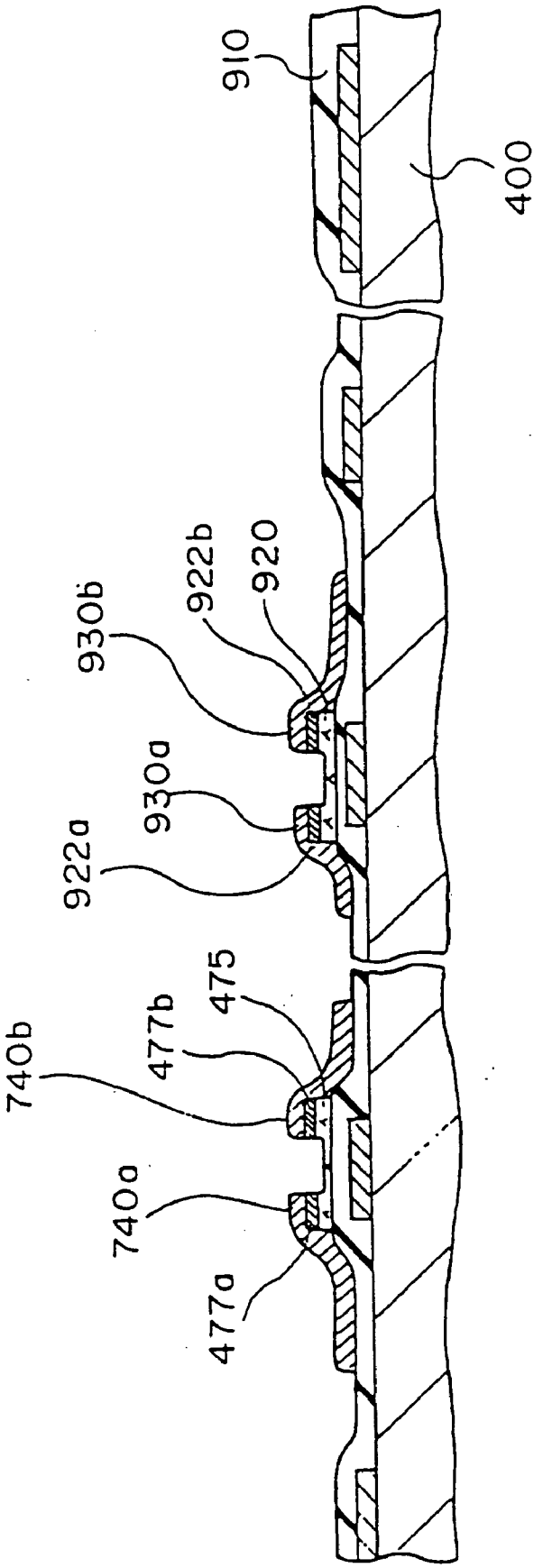


FIG. 23

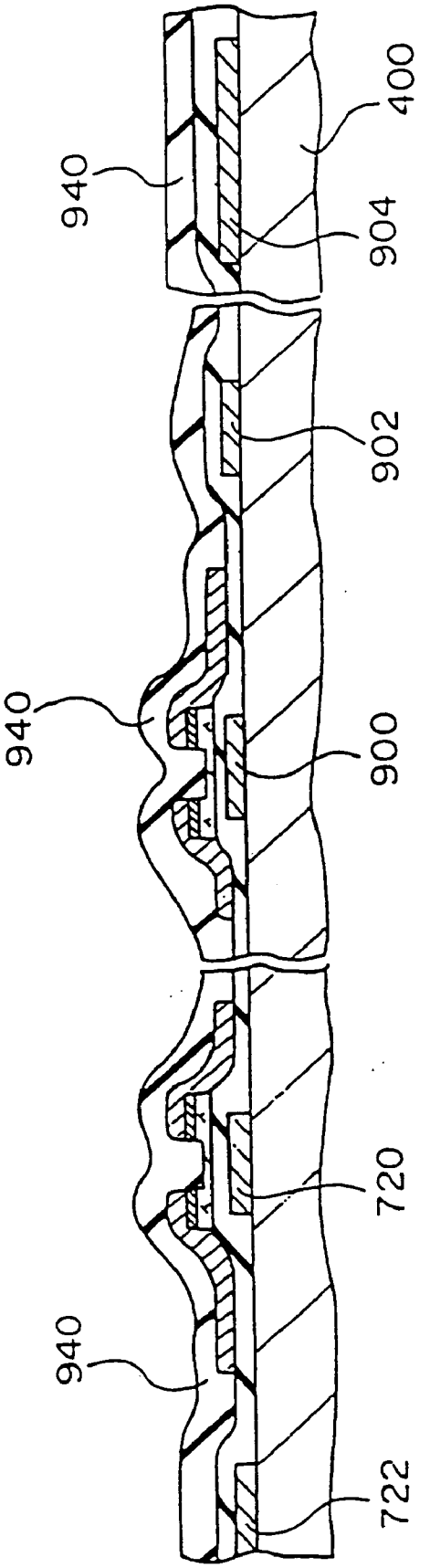
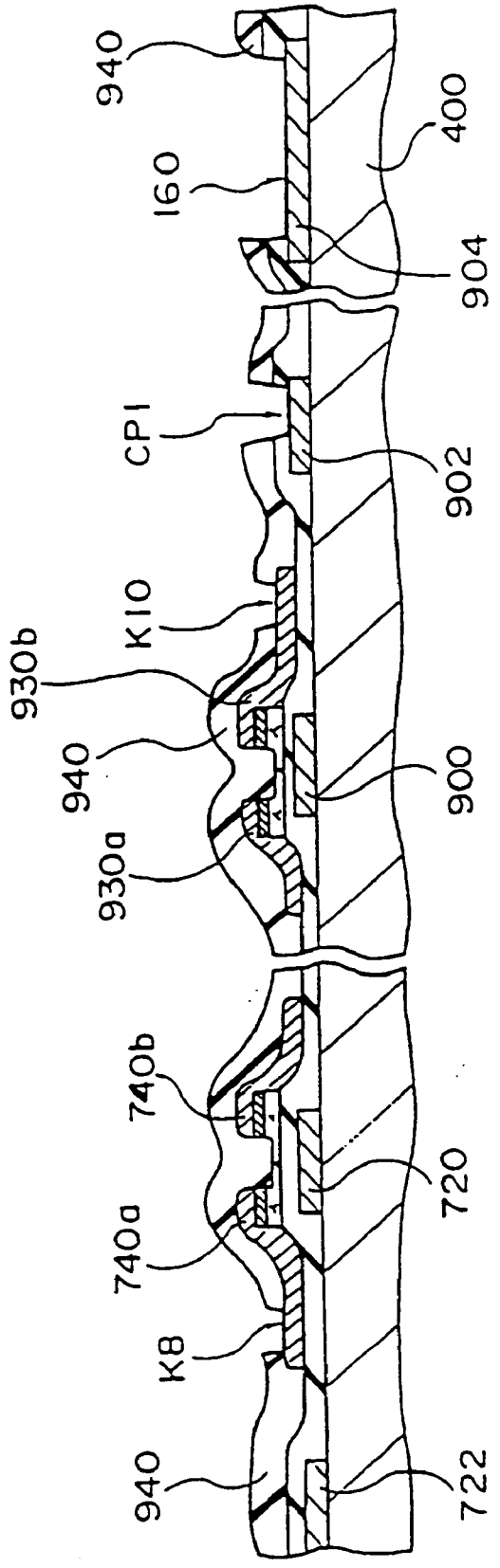


FIG. 24


940
160
400
904
CP1
902
K10
930b
940
900
930a
740b
720
740a
K8
940
722

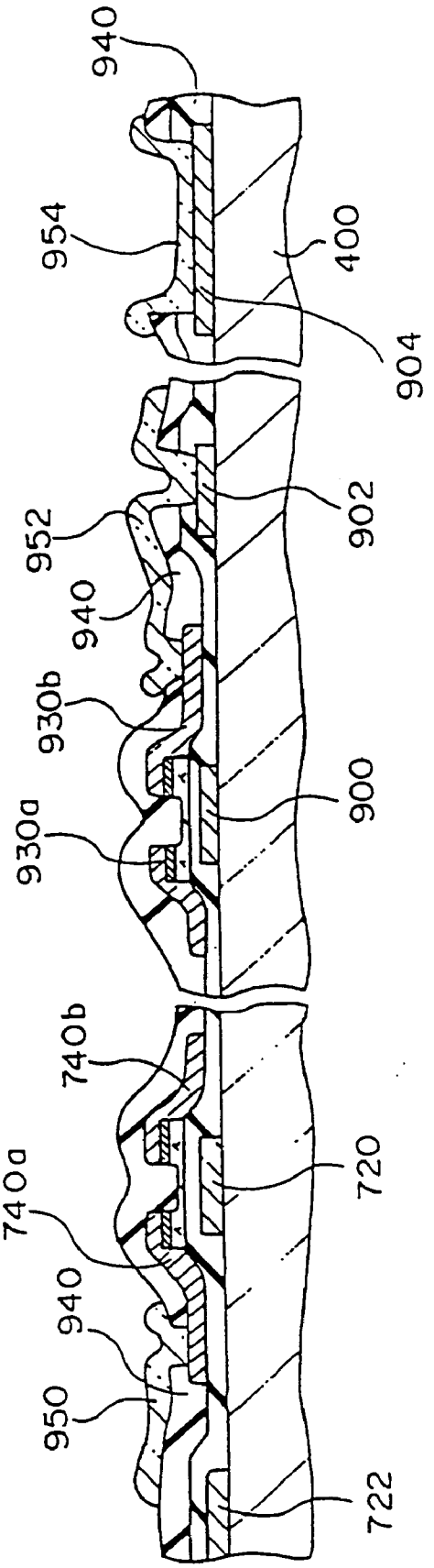

940
954
400
904
952
902
940
930b
900
930a
740b
720
740a
940
950
722

FIG. 25

FIG. 26

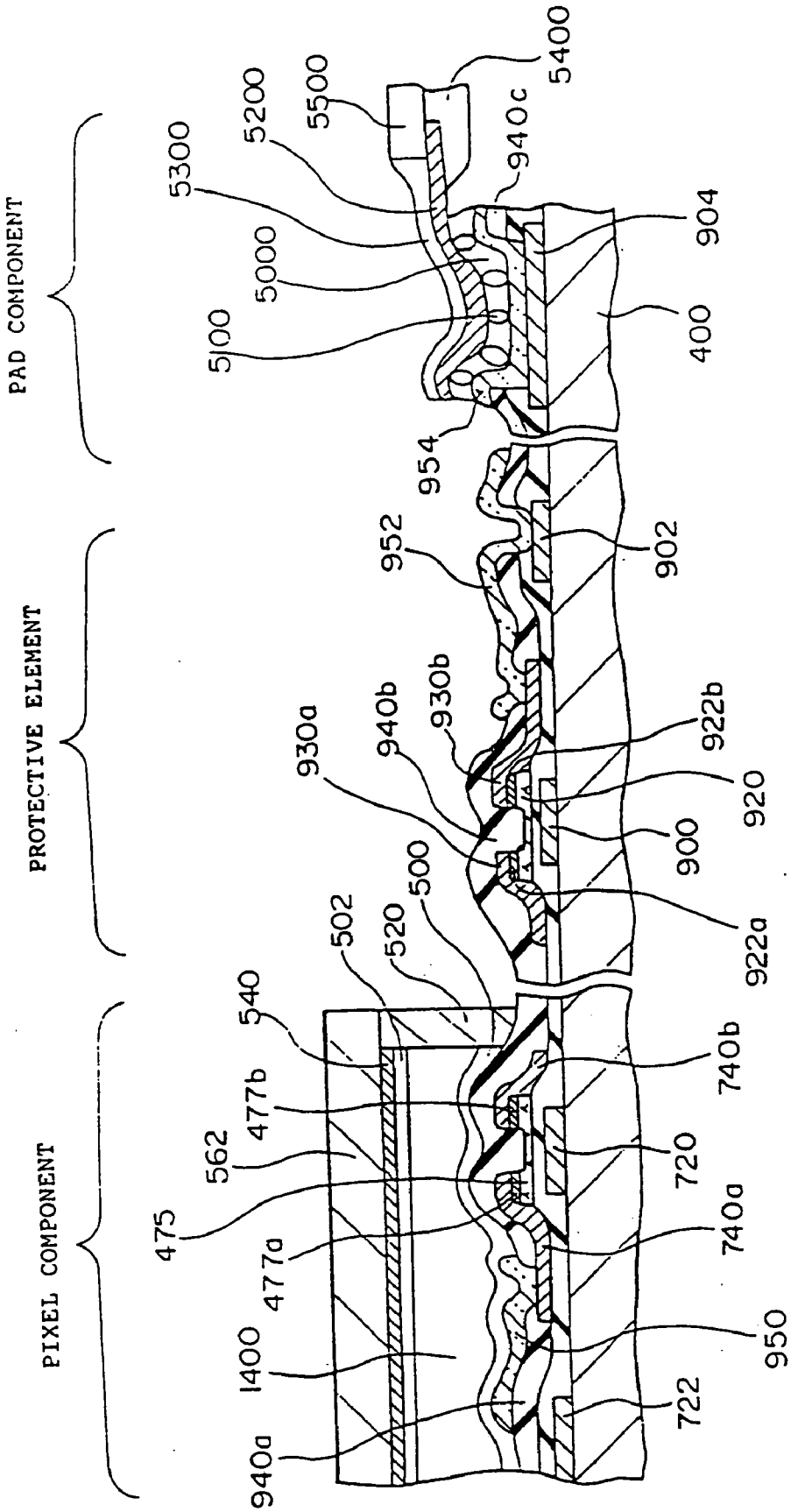

PAD COMPONENT
PROTECTIVE ELEMENT
PIXEL COMPONENT
5400
5500
5200
5300
5000
5100
940c
904
400
954
952
902
930a
940b
930b
922b
920
900
922a
500
502
520
540
740b
720
740a
950
722
562
477b
475
477a
1400
940a

FIG. 27

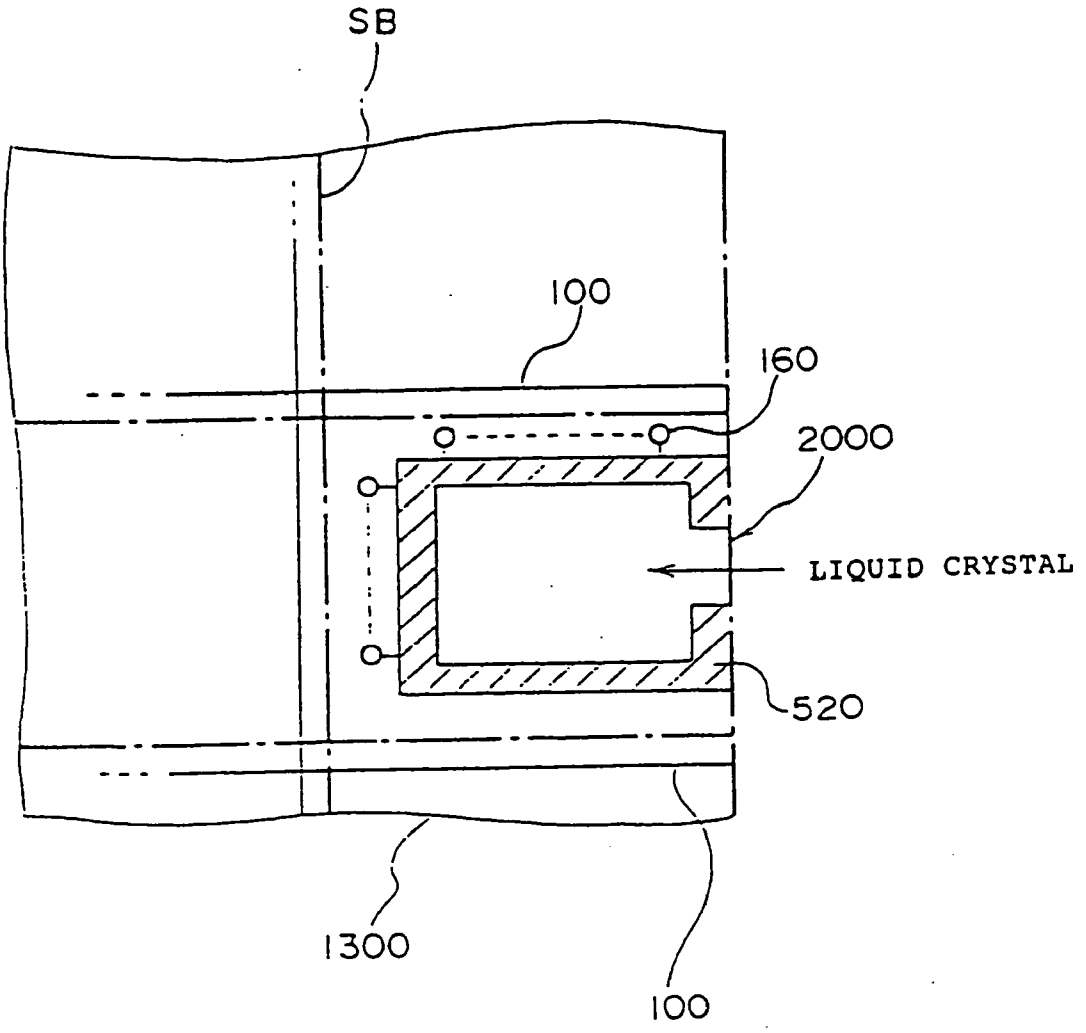


FIG. 28

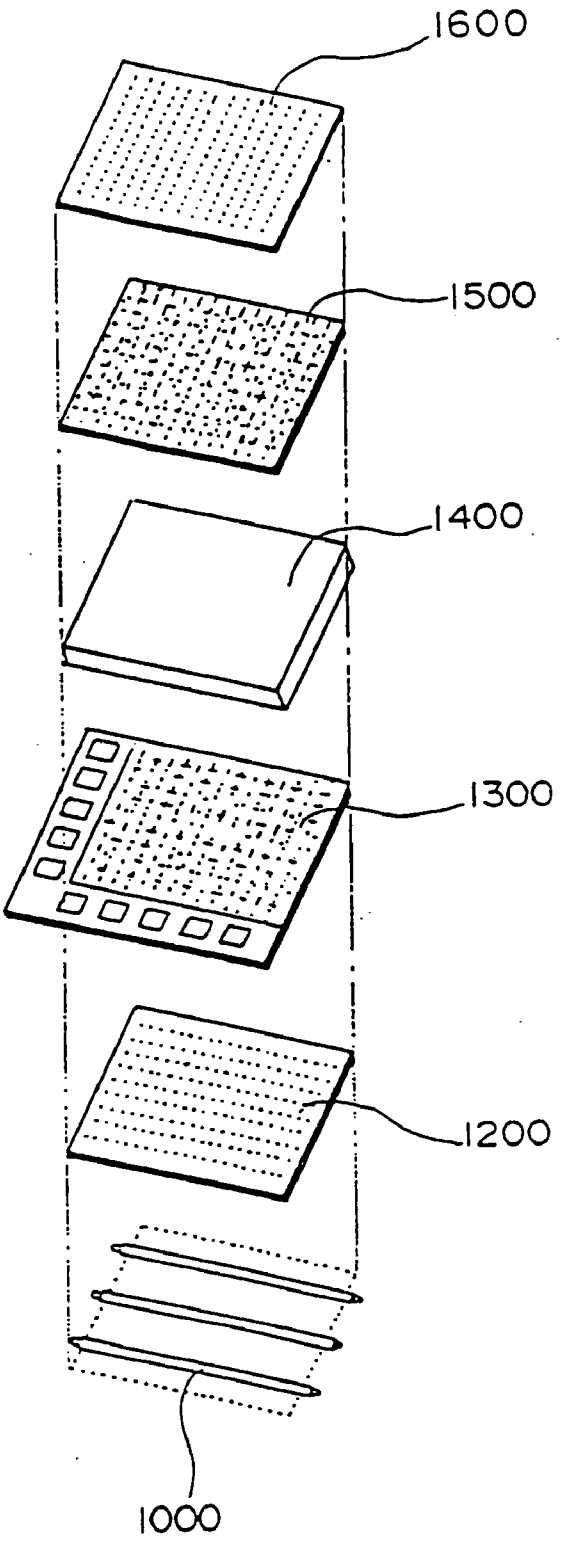


FIG. 29

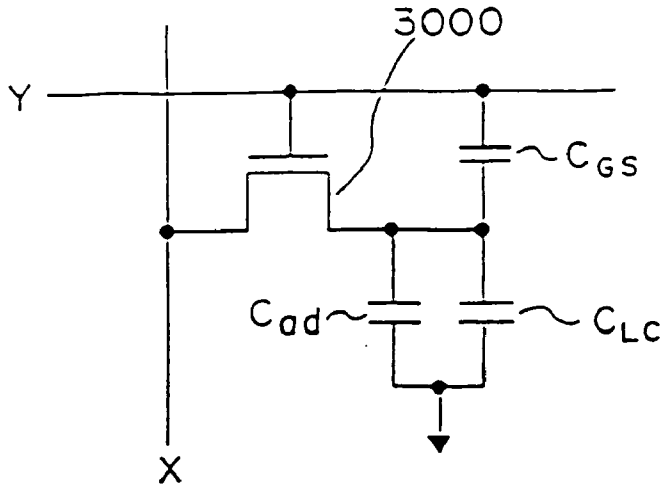
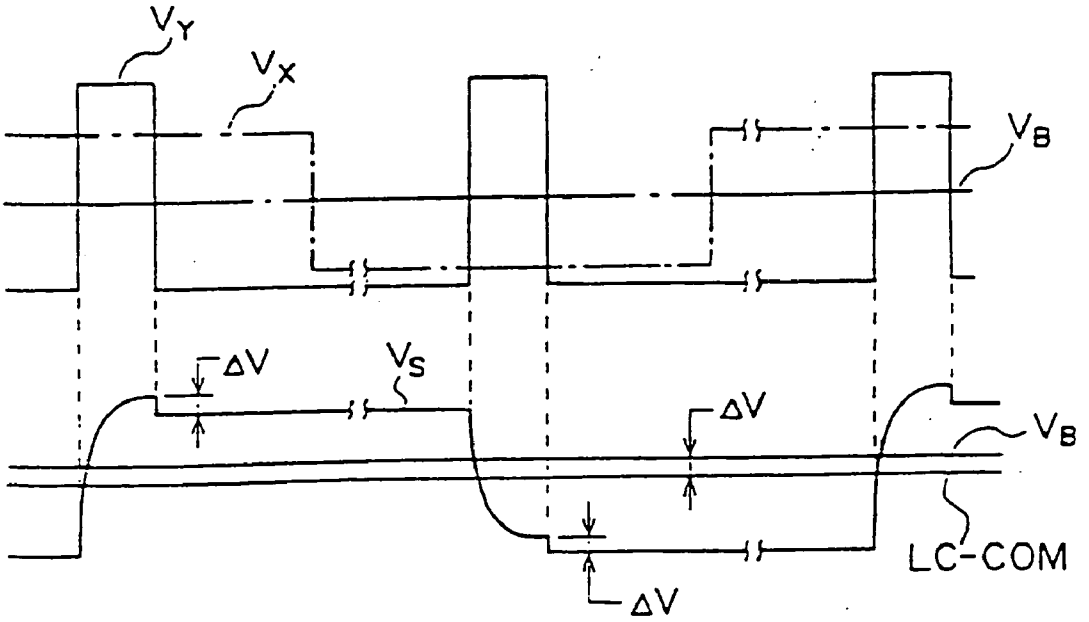


FIG. 30



METHOD TO PREVENT STATIC DESTRUCTION OF AN ACTIVE ELEMENT COMPRISED IN A LIQUID CRYSTAL DISPLAY DEVICE

[0001] This is a Division of Application Ser. No. 10/458,198, filed on Jun. 11, 2003, which is a Division of U.S. Pat. No. RE 38,292 (application Ser. No. 09/903,639, filed Jul. 13, 2001), which is a Reissue of U.S. Pat. No. 5,930,607, issued Jul. 27, 1999 (Application Ser. No. 08/849,288, filed May 30, 1997), which is a U.S. National Stage of PCT/JP96/02858, filed Oct. 2, 1996. The entire disclosure of the prior applications is hereby incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of Invention

[0003] The present invention relates to a method for manufacturing a thin film element, an active matrix substrate, a liquid crystal display device and an active matrix substrate, as well as a method for preventing the electrostatic destruction of an active element included in a liquid crystal display device.

[0004] 2. Description of Related Art

[0005] With the liquid crystal display device having an active matrix format, the switching element in each pixel electrode is connected, and each pixel electrode is switched through the switching element. As the switching element, utilization may be made, for example, of a thin film transistor (TFT).

[0006] The construction and operation of the thin film transistor is fundamentally the same as the single crystal silicon MOS transistor.

[0007] As the structure of the thin film transistor which utilizes amorphous silicon (α-Si) there are a number of well known types of construction. However, bottom gate structure (reverse stagger structure) wherein the gate electrode is at the bottom of the amorphous silicon film is generally used.

[0008] In the structure of a thin film transistor, it is important to reduce the number of construction processes and to assure a high yield.

[0009] In addition, in the production process of an active matrix substrate, it is important to effectively protect the thin film transistor from the destruction caused by the generated static electricity. The technology for protecting the thin film transistor from electrostatic destruction is disclosed, for example, in Japanese laid open utility model **63-33130** which is recorded on microfilm, or in laid open patent publication 62-187885.

SUMMARY OF THE INVENTION

[0010] One of the objects of the present invention is to provide a novel thin film element production process technology which enables the reduction of the number of thin film transistor manufacturing processes, with a high degree of reliability.

[0011] In addition, another object of the present invention is to provide an active matrix substrate and a liquid crystal display device in which the production process is formed utilizing production process technology which is not complicated, and which has adequate electrostatic prevention capacity for the protection elements. In addition, another object of the present invention is to provide an electrostatic destruction prevention method which can prevent the electrostatic destruction of the active elements (TFT) included in the TFT substrate.

[0012] One of the desirable situations for the production method of thin film elements according to the present invention is that, at the time of producing the thin film elements having a bottom gate construction, it includes a process for forming a protective film which covers the source electrode, the drain electrode, and the gate electrode material layer. Subsequently a process for forming a first aperture component having a part of a built up film comprising a gate electrode layer is selectively etched. A gate insulation film which is present on a gate electrode material layer, and a protective film are also formed so that a portion of the surface of the gate electrode layer and the gate electrode material layer is exposed. At the same time, a second aperture component is formed wherein selected etching of a portion of the source electrode layer and the protective film on the drain electrode layer is accomplished, so as to expose a part of the source electrode layer and the surface of the drain electrode layer; and a process which subsequently connects at least one of the gate electrode layer, the gate electrode material layer, the source electrode layer, or the drain electrode layer with the electrically conductive material layer through the first and second aperture.

[0013] According to the described thin film element manufacturing method, selective etching of the insulation film is accomplished all at once. Hence, the formation process of an aperture to connect the external connection terminal to the electrode (pad open process), and the formation process of an aperture for connecting the internal wiring to the electrode (contact hole formation process) can be jointly accomplished, and the number of processes can be reduced.

[0014] As the "electrically conductive material layer", ITO (indium tin oxide) film is desirably utilized. As described above, the first aperture is formed so that it passes through the overlapped films comprising the first insulation film over the gate electrode material layer and the second insulation film over the first insulation film, a deep contact hole is created so as to correspond in depth of the two insulation films.

[0015] However, since ITO has a high melting point, ITO has good step coverage in comparison with alumiinum, and the like, therefore the connection is not poor even if it is accomplished through a deep contact hole.

[0016] In addition to the ITO film, other transparent electrode materials which have a high melting point, such as metallic oxides can also be utilized as the "electrically conductive material layer". For example, metallic oxides such as SnOx and ZnOx may be utilized. In this case as well, the step coverage is able to withstand actual use.

[0017] In addition, with one desirable situation for an active matrix substrate according to the present invention, a protective means used to prevent the electrostatic destruction used with thin film transistors is connected between at least one line between the scanning line and the signal line, or between an electrically equivalent region to said line and a joint electric potential line.

[0018] The protective means used to prevent electrostatic destruction is composed to include a diode which is constructed so as to connect the gate electrode layer in the thin film transistor and the drain electrode layer, and by selectively removing the insulation layer from the gate electrode layer to electrically connect the drain electrode and the gate electrode, and by selectively removing the resultant first aperture component and the insulation from the drained electrode layer. The resultant second aperture component is formed by the same manufacturing process; and furthermore, the gate electrode layer and the drain electrode layer are connected by the electrically conducted layer formed from the same material as the pixel electrodes, through the first and second apertures.

[0019] Short circuiting the TFT gate and drain, the formed MOS diode (MIS diode) comprises a substantive transistor, in which there is a high capacity for the flow of electric current, and the static electricity can be quickly absorbed, with high static electricity protection capacity. In addition, since it is substantially a transistor, the control of the electric current/voltage characteristic threshold value voltage (V_{th}) can be easily accomplished. Furthermore, it is possible to reduce the unnecessary leakage of electric current. In addition, the number of manufacturing processes of the thin film element is reduced, and construction is simplified. As the "pixel electrode" and the "electrically conductive layer formed from the same material as the pixel electrode", desirable utilization is made of ITO (indium tin oxide) film. Other than the ITO film, utilization may also be made of other transparent electrode materials having a high melting point, such as metallic oxides. For example, use may be made of such metallic oxides as SnOx, and ZnOx and the like.

[0020] With one desirable situation for the active matrix substrate according to the present invention, the described "line which has at least one of either a scanning line or a signal line, and electrically equivalent regions" comprises an electrode (pad) for connecting an external connection element, and the "joint electric potential line" with a line (LC-COM line) to which is applied a standard electric potential which becomes the standard at the time of the alternating current driving of the liquid crystals, or with the manufacturing stage of the liquid crystal display device, it comprises a line (guard ring) for jointly connecting the electrode (pad) for connecting the external connection element and making it the same electric potential.

[0021] The guard ring is a line connected to the exterior of the pad, and serves as a counter measure for static electricity in the manufacturing stage of the liquid crystal display device. Both the LC-COM line and the guard ring are joint electric potential lines. Furthermore, by connecting a protective diode between the pad and these lines, static electricity can be avoided in the lines.

[0022] In addition, one of the desirable situations for an active matrix substrate according to the present invention is that the "protection means used to prevent static electricity destruction" is attached both between the electrode (pad) for connecting an outside terminal and the line (LC-COM line) to which has been applied the standard electric potential which became the standard at the time of alternate current driving of the liquid crystal; as well as between the electrode (pad) for connecting the external terminal and the line (guard ring) for jointly connecting the electrode (pad) for connecting the external terminal and making it the same electric potential.

[0023] The guard ring, following the emulation between the TFT substrate and the facing substrate (color filter substrate) is completely cut off prior to the connection of the IC used for the drive, and the LC-COM line is the line which remains in the final product. Furthermore, even after the substrate cutoff prior to the connection of the IC, according to the construction described above, the pixel TFT is protected from electrostatic destruction, and continuing, there is an improvement in the reliability of the product.

[0024] In addition, since the protective diode remains even in the final product, there is also an improvement in the strength of the protection against electrostatic destruction at the time of the product's actual use.

[0025] Furthermore, since it is a protective diode which uses the TFT, control of the threshold value voltage (V_{th}) can be easily accomplished, and since the current leakage can also be reduced, there is no negative influence even if the diode remains in the final product.

[0026] In addition, with one desirable situation for a method of manufacturing an active matrix substrate according to the present invention, the electrostatic destruction prevention protection means provides a bi-directional diode which jointly connects the first diode anode and the second diode cathode, and jointly connects the first diode cathode and the second diode anode.

[0027] Since it is a bi-direction protective diode, the TFT can be protected from both the positive electrode surge and negative electrode surge.

[0028] In addition, the liquid crystal display device is constructed using the active matrix substrate of the present invention. By assuredly preventing electrostatic destruction of the active element (TFT) of the pixels in the active matrix substrate, the reliability of the liquid crystal display device is also improved. In addition, with one desirable situation of a method of manufacturing an active matrix substrate according to the present invention at the time of forming the TFT of the bottom gate construction, in a specified region on the insulation film, at the same time as forming a source/drain electrode layer from the same materials, it includes a process for forming the source/drain electrode material layer from the same material as the source/drain electrode layer; and a process for creating a protective film which covers the source/drain electrode layer, and the source/drain electrode layer material; and a process for forming a second aperture so as to expose a part of the surface of the source/drain electrode layer or the source/drain electrode material layer, selectively etching the protective film on the source/drain electrode layer or the source/drain electrode material layer, at the same time as forming a first aperture so as to expose a part of the surface of the gate electrode layer and the gate electrode material layer, selectively etching the film buildup of the gate insulation film which exists on the gate electrode layer and the gate electrode material layer, as well as the protective film; and a process for connecting the electrically conductive material layer to the gate electrode layer, the gate electrode material layer, the source/drain electrode layer, or the source/drain electrode material layer, through the first and second apertures.

[0029] According to the described method of manufacture of the thin film element, selective etching of the insulation film is accomplished all at once. Hence, the formation process (pad open process) of the aperture for connecting the external terminal to the pad, and the formation process (contact hole formation process) of the aperture for connecting the wiring to the electrodes are jointly accomplished, thereby reducing the number of processes.

[0030] This method of manufacturing can also be used in the formation of the MOS diode as the static electricity protection element. In addition, utilization may also be made in the formation of the crossunder wiring in the vicinity of the pad. The "crossunder wiring" at the time of leading the internal wiring of the liquid crystal display device to the outside of the seal material achieves the protection of the wiring by means of a thick layer of insulating film between them connecting the wiring in the upper layer to the wiring of the lower layer with the wiring being used to lead to the outside in a round about manner.

[0031] The "conducted material layer" is desirably the same material as the pixel electrode. By this means, the wiring which is formed of the electrically conductive material is capable of being formed at the same time as the process for forming the pixel electrodes.

[0032] Furthermore, desirable use is made of ITO (indium tin oxide) film as the "electrically conductive material layer". Other than ITO film, use may also be made of other transparent electrode materials, having a high melting point such as metallic oxides.

[0033] In addition, as a preferable situation for an electrostatic destruction prevention method in the active matrix liquid crystal display device according to the present invention, a protective means used for electrostatic destruction prevention formed from a bi-directional diode is attached between at least one of either the scanning line or the signal line, or a region which is electrically equivalent to the line and a joint electric potential line, by which means prevention can be accomplished of electrostatic destruction of an active element included in the liquid crystal display device.

[0034] The electrostatic destruction of the active element (TFT) included in the active matrix substrate can be assuredly prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] **FIGS. 1-6** are cross sectional diagrams of the device following each process, and show the construction method of the thin film element according to the present invention.

[0036] FIGS. **7A-FIG. 7F** are drawings which explain the characteristics of the manufacturing process technology shown in **FIGS. 1-6**.

[0037] **FIGS. 8A-8G** are cross-sectional diagrams of the device following each process of a contrasting example.

[0038] **FIG. 9** is a diagram which shows a compositional example of the TFT substrate according to the present invention.

[0039] **FIG. 10** is a diagram which shows the composition in the pad periphery of the TFT substrate of **FIG. 9**.

[0040] **FIG. 11A** shows the composition of the electrostatic protection circuit; **FIG. 11B** shows the equivalent circuit of an electrostatic protection circuit; and **FIG. 11C** is a diagram which shows the electric voltage/electric current characteristics of an electrostatic protection circuit.

[0041] **FIG. 12** is a diagram which shows the plane surface layout of an electrostatic protection circuit.

[0042] **FIG. 13** is a diagram for explaining the composition of an electrostatic protection circuit of **FIG. 12**, using cross-sectional construction of the device.

[0043] **FIG. 14** is a diagram for explaining the function of the electrostatic protection circuit.

[0044] **FIG. 15** is a diagram which shows a sample structure when the wiring of the liquid crystal panel is led to the bonding pad.

[0045] **FIG. 16** is a diagram which shows an example of the location for ITO use in a region which excludes the pixels in an active matrix substrate according to the present invention.

[0046] **FIG. 17** is a diagram which shows the plane surface layout form of the pixels in the liquid crystal display device according to the present invention.

[0047] **FIG. 18** is a diagram which shows a cross-section of the liquid crystal display device along the line B—B of **FIG. 17**.

[0048] **FIGS. 19-25** are respective cross-sectional diagrams of the device following each process which shows the method of construction of an active matrix substrate according to the present invention.

[0049] **FIG. 26** is a diagram which shows the cross-sectional structure of the essential components of the liquid crystal display device in its assembled form utilizing the active matrix substrate of **FIG. 25**.

[0050] **FIG. 27** is a diagram for explaining the dividing process of the substrate by means of a cell division device.

[0051] **FIG. 28** is a diagram for explaining a summary of the entire construction of the liquid crystal display device of an active matrix type.

[0052] **FIG. 29** is a circuit diagram which shows the composition of the pixel components of the liquid crystal display device of an active matrix type.

[0053] **FIG. 30** is a diagram which shows the voltage wave form for driving the liquid crystal in the pixel component of **FIG. 29**.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0054] An explanation is provided hereafter of the form of the execution of the present invention, with reference to the drawings.

First Embodiment

[0055] **FIGS. 1-6** are cross-sectional diagrams of the device following each process which show an example of the construction method of the thin film element (bottom gate construction TFT) of the present invention.

[0056] Contents of Each Manufacturing Process

[0057] Process 1

[0058] As shown in **FIG. 1**, using photolithography technology on the glass substrate (non-alkali substrate) **2**, formation can be accomplished for example of gate electrode **4***a* formed from Cr (chrome) which has a thickness of 1,300 Å approximately, and gate electrode material layers **4***b* and **4***c*. The gate electrode **4**a is a gate electrode of the TFT of a bottom gate construction formed in a matrix shape on the pixel. In addition, the gate electrode material **4***b* becomes the region formed by the protective element used to prevent electrostatic destruction, described hereafter. In addition, the gate electrode material layer **4***c* becomes the region formed for use in connections with external components, or for the elements used for scanning.

[0059] Next, by means of a plasma CVD method, continuous formation is accomplished of amorphous silicon film **8** in which there are no doped impurities, as well as the n type silicon film ((ohmic-phonetic) contact layer) **10**; and next, by means of photo-etching, islands can be created of amorphous silicon film **8** and n type silicon film (ohmic contact layer) **10**.

[0060] In this instance, the thickness of the gate insulation film **6** is for example 3000 Å approximately, and the thickness of the genuine silicon film **8** is for example approximately 3000 Å, and the thickness of the ohmic contact layer **10** is for example approximately 500 Å.

[0061] With this process, characteristically there is no formation of a contact hole relative to the gate insulation film.

[0062] Process 2

[0063] Next, as shown in **FIG. 2** for example, formation is accomplished by means of sputtering and photo-etching the source/drain electrodes **12***a* and **12***b* of approximately 1300 Å formed from Cr (chrome).

[0064] Process 3

[0065] Next, as shown in **FIG. 3**, utilization is made of the source/drain electrodes **12***a* and **12***b* as the mask, and the central portion of the ohmic contact layer **10** is removed by etching, and separation (separation etching) is accomplished on the source/drain. In this instance, etching is accomplished for the purpose of patterning the source/drain electrodes and separation etching can be continuously accomplished within the same chamber of the same etching device.

[0066] In other words, first of all etching of the source/drain electrodes **12***a*, **12***b* is accomplished using etching gas of the Cl_2 type. Continuing, etching of the center portion of the ohmic contact layer **10** can be accomplished by switching to gas of the SF_6 type for the etching gas.

[0067] Process 4

[0068] Next, as shown in **FIG. 4**, formation of the protective film **14** is accomplished, for example, by means of the plasma CVD method. The protective film **14** is for example a silicon nitride film (SiN_x) of approximately 2,000 Å.

[0069] Process 5

[0070] Next, as shown in **FIG. 5**, contact holes **16**, and **18** are formed on a portion of the protective film **14**, at the same time as aperture **20** is formed for connecting to the outside terminal (bonding wire or IC outer lead).

[0071] The aperture **20** and contact hole **18** are formed so as to pass through the built up film comprising the gate insulation film **6** and the protective film **14**. The contact hole **16** is formed so as to only pass through the protective film **14**.

[0072] When forming the aperture **20** and the contact hole **18**, the gate electrode material layer **4***b* and **4***c* respectively function as etching stoppers. In addition, when forming the contact hole **16**, the source/drain electrode **12***b* functions as an etching stopper.

[0073] Process 6

[0074] Next, as shown in **FIG. 6**, ITO (indium tin oxide) film is deposited with a thickness of approximately 500 Å, accomplishing selective etching, and forming wiring **22***a* and the electrode **22***b* from the ITO. The etching of the ITO is accomplished by means of wet etching in which utilization is made of a compound liquid of $HCVHNO_3/H_2O$. As explained, the aperture **20** and the contact hole **18** are formed to pass through the built up film composed of the gate insulation film **6** and the protective film **14**. Furthermore, this becomes a contact hole with a depth corresponding to the thickness of the two layer insulation film.

[0075] However, since the ITO has a high melting point, the step coverage is good in comparison to aluminum and the like. Furthermore, there is not a poor connection even though the contact hole may be deep. Moreover, other than ITO, utilization may also be made of other transparent electrode materials having a high melting point such as metallic oxide. For example, utilization may be made of metallic oxides such as SnOx and ZnOx. In this case as well, the step coverage is able to also withstand actual application.

[0076] The TFT having bottom gate construction which is produced in this manner is used as a pixel switching element in an active matrix substrate. In addition, the electrode **22***b* formed from the ITO becomes a pad for connecting the external terminal (IC outer lead and the like).

[0077] Characteristics of the Present Manufacturing Method

[0078] **FIGS. 7A-7F** show the manufacturing process of the TFT applied to the state of the present embodiment recorded in **FIG. 1**through **FIG. 6**. On the other hand, **FIGS. 8A-8G** show the manufacturing process of the TFT in a contrast example. This contrast example was considered by the present inventors to clarify the characteristics of the manufacturing process of the TFT applied to the shape of the present embodiment, and is not a prior art example.

[0079] **FIG. 8A** of the contrast example is the same as **FIG. 7A**. In **FIGS. 8A-8G**, the same reference numbers are applied to the same components as in FIGS. 7A-F.

[0080] In the case of the contrast example, as shown in **FIG. 8B**, prior to the creation of the drain electrode layer, the contact holes K1, and K2 are formed.

[0081] Also, as shown in **FIG. 8C**, formation is accomplished of the source/drain electrode layers **12***a* and **12***b*, as well as the source/drain electrode material layers **12***c*, and

12*d* formed from the same materials. Next, formation of the ITO film **30** is accomplished as shown in **FIG. 8D**. Subsequently, etching (separation etching) is accomplished of the center portion of the ohmic layer **10** as shown in **FIG. 8E**. Subsequently, formation of the protective film **40** is accomplished as shown in **FIG. 8F**.

[**0082**] Finally, formation of the aperture K**3** is accomplished as shown in **FIG. 8G**. By this means, the surface of the source/drain electrode material layer **12***d* is exposed, and the electrode (pad) is formed for the purpose of connecting the external connection terminal.

[**0083**] According to the manufacturing method of this type of contrast example, in the formation process of the contact hole in **FIG. 8B**, a process is added to form the aperture K**3** in **FIG. 8G**, with the necessity of a total of two aperture formation processes.

[**0084**] In this regard, according to the manufacturing method of the present embodiment, as shown in **FIG. 7E**, formation is accomplished of apertures **16**, **18**, and **20** all at once. In other words, at the same time as forming the aperture passing through the built up film comprising the protective film **14** and the gate insulation film **6**, through the simultaneous patterning also of the protective film **14** on the source/drain electrode layer **12***b,* the aperture formation process may be accomplished at one time. Furthermore, the light exposure process can be reduced by one process. In accompaniment with this, the process of depositing the photo resist film, and its etching process becomes unnecessary. Furthermore, altogether there is a reduction of three processes. In other words, the manufacturing process is simplified.

[**0085**] In addition, according to the manufacturing method of the present embodiment, patterning (dry etching) of the source/drain electrode **12***a* and **12***b* are continued as shown in **FIG. 7b** and the etching (dry etching) of the center part of the ohmic contact layer **10** shown in **FIG. 7C** is continued, and is accomplished within the same chamber. In other words, by chronologically switching the etching gas within the same chamber, it is possible for etching to be continued.

[**0086**] In this regard, in the case of the contrast example, following the patterning (dry etching) of the source/drain electrode layers **12***a* and **12***b* of **FIG. 8C**, wet quenching is accomplished of the ITO film **30** of **FIG. 8D**, and subsequently, the etching (dry etching) is accomplished of the center portion of the ohmic layer **10** of **FIG. 8E**. The ITO film cannot be processed by means of dry etching, and since there is no accomplishment of processing by means of wet etching, each of the etching processes shown in **FIGS. 8C, 8D**, and 8E, cannot be continuously accomplished within a single chamber. Hence, it becomes necessary for the substrate to be handled following each process, making the operation inconvenient.

[**0087**] In addition, in the case of the shape of the present embodiment, the protective film **14** is necessarily present between the ITO films **22***a* and **22***b,* and the source/drain electrodes **12***a,* **12***b.* This being the case, in the other regions (not shown in the drawing) of the substrate, it means that the wiring formed from the ITO film, and the wiring or electrodes formed from the same material as the source/drain electrodes are assuredly and electrically separated.

[**0088**] However, in the case of the contrast example, the ITO film **30** and the source/drain electrodes **10***a,* **10***b* belong in the same layer. In other words, both are laminated, and no protective layer is present between the two. Hence, in other regions (not shown in the diagram) of the substrate, if foreign matter is present, then notwithstanding the fact that they must be insulated thereafter, there is the concern that wiring formed from the ITO film, and wiring or electrodes formed from the same material as the source/drain electrodes will become completely shorted. In other words, the device formed by the method of manufacture of the present embodiment has high reliability.

[**0089**] In addition, with the contrast example, in order to form (in **FIG. 8D**) the ITO film **30** by means of a relatively fast step, in the subsequent processes, there is some concern of staining by means of indium (In) or tin (Sn) comprising the ITO composite product.

[**0090**] In this regard, with the method of manufacture according to the present embodiment, since the ITO film **22***a* and **22***b* is formed in the final process, there is little concern of staining being caused by the tin (Sn) comprising the ITO composite.

[**0091**] In this manner, according to the method of manufacture of the present embodiment, the manufacturing process can be shortened, and a device can be manufactured having high reliability.

Second Embodiment

[**0092**] Next, an explanation of the second embodiment of the present invention is provided hereafter with reference to **FIGS. 9 through 18**.

[**0093**] **FIG. 9** is a diagram which shows the plane surface layout of an active matrix substrate in which application is made of the second embodiment of the present invention.

[**0094**] The active matrix substrate of **FIG. 9** is utilized in a liquid crystal display device. As the protective elements used as switching elements for the pixels, and used to prevent electrostatic destruction, utilization is made of TFT manufactured by the manufacturing method explained in the first embodiment.

[**0095**] The pixel parts **4000** (in the diagram shown by the dotted line) are formed from multiple pixels **120**, and each pixel is composed to include TFT (switching element) **3000**. The TFT **3000** is attached to the intersecting points of the scanning line **52** and the signal line **54**.

[**0096**] To each end of the signal line **54** and the scanning line **52** is respectively attached a pad **160**A, and **160**B, with the first protective element **140**A and **140**B being connected between the pad and the LC-COM line **180**, with a second protective element **150**A, and **150**B being formed between the pad and the guard ring **100**. Furthermore, the LC-COM line **180** is also connected to the facing electrode through the silver point pad **110**.

[**0097**] "Pads **160**A and **160**B" are electrodes for connecting the bonding wire or the (bump-phonetic) electrode or for connecting electrodes (external terminals) which use polyimide tape.

[**0098**] In addition, the "LC-COM line **180**" is a line to which an electric potential is applied which becomes the standard liquid crystal drive. The common electric potential LC-COM, for example, as shown in **FIG. 30** is established

to the electric potential which is reduced only DV by means of the midpoint electric potential V_B of the display signal voltage V_x. In other words, as shown in the example in **FIG. 29**, in the pixel TFT **3000**, a capacity CGS is present between the gate/source, and with its influence, between the display signal voltage V_X and the final maintained voltage V_s is produced the voltage potential difference DV. In order to compensate for the electric potential difference DV, the electric potential reduced by only DV becomes the joint standard electric potential by means of the midpoint electric potential V_B of the display signal voltage V_X.

[**0099**] Furthermore, in **FIG. 29**, X represents the signal line, and Y represents the scanning line, C_{LC} shows the equivalent capacity of the liquid crystal, and the C_{ad} shows the maintenance capacity. In addition, in **FIG. 30**, V_X represents the displayed signal voltage which is supplied to the signal line X, and V_y is the scanning signal voltage supplied to the scanning line Y.

[**0100**] In addition, the guard ring **100** is a line which is attached to the outside of the pads **160**A and **160**B as an electrostatic countermeasure to the manufacturing stage of the liquid crystal display device.

[**0101**] Both the LC-COM line **180** and the guard ring **100** are joint electric potential lines, and continuing, the electrostatic electricity avoids these lines by the connection of a protective diode between the pad and these lines.

[**0102**] In addition, the guard ring **100**, as shown in **FIG. 27**, following the emulation of the TFT substrate **1300** and the opposing substrate (color filter substrate), completely cuts off along the scribe line (SB) prior to the connection of the IC for drive use, however, the LC-COM line **180** is a line which remains in the final product. Furthermore, following the substrate cutoff, even prior to the connection of the IC, the TFT of the pixel components are protected from electrostatic destruction by means of the first protective element **140**, and continuing, there is improved reliability of the product.

[**0103**] In addition, since the protective diode also remains in the final product, there is also an improvement in the electrostatic destructive protection strength in the actually used final product.

[**0104**] Furthermore, since the protective diode utilizes the TFT, the control of the threshold value voltage (V_{th}) is easy, and since the amount of leaking electric current can also be reduced, there is no negative influence even if the diode remains in the final product.

[**0105**] A practical embodiment of the protection elements is shown in **FIGS. 11A-11C**.

[**0106**] In other words, as shown in **FIG. 11A**, the protective element connects the MOS diode formed from the connection of the gate/drain of the first TFT (F1), and the MOS diode formed by connecting the gate/drain of the second TFT (F2) mutually in the reverse direction, in parallel. The equivalent circuit is such as that which is shown in **FIG. 11B**.

[**0107**] Furthermore, as shown in **FIG. 11C**, the protective element has nonlinear shape characteristics in both directions, in terms of the electric current/electric voltage characteristics. Each diode is given a high impedance at the time of low voltage impression, becoming a low impedance state at the time of high voltage impression. In addition, each diode is substantially a transistor, and the electric current flow capacity is great, and since the static electricity can be quickly absorbed, the static electric protective performance is high.

[**0108**] **FIG. 10** shows a practical arrangement of the static electricity protective elements in the periphery of the pads **160**A and **160**B of **FIG. 9**.

[**0109**] The protective element **140**A of **FIG. 1** is constructed by means of thin film transistors M**60** and M**62** which are connected between the gate/drain, and in the same manner, the protective element **140**B of **FIG. 1** is formed from the thin film transistors M**40** and M**42**.

[**0110**] In the same manner, both the second protective elements **150**A and **150**B are formed from the thin film transistors M**80**, M**82**, M**20**, and M**22**.

[**0111**] These protective elements are turned on when there is the impression of a excessive positive or negative surge, and there is movement so that the LC-COM line **180** or the guard ring **100** avoid the surge. In addition, a second protective element **150** arranged on the other side of the pad is added to the function of the electrostatic protection, and each of the pads **160** are shorted by the guard ring **100**, with the function of preventing a final scan from becoming impossible in the array process. An explanation of this is provided hereafter with reference to **FIG. 14**.

[**0112**] As shown in **FIG. 14**, a case where the probe of the array tester **200** (which has 220 amp) is connected to the pad **160A1** to test the pixel TFT (Ma) is considered.

[**0113**] At this time, the second protective element **150A1** and the second protective element **150A2** maintain a state of high impedance, and furthermore the pixels TFT (Ma) and TFT (Mb) are electrically separated. Hence, crosstalk with other transistors is prevented, and experimentation can be accomplished only relative to the specified TFT (Ma).

[**0114**] In addition, as shown in **FIG. 27**, when the creation of the TFT substrate **1300** is complete, then following the completion of each of the processes comprising the coating of the facing film, the rubbing process, the coating process of the seal material (spacer), the substrate emulation process, the dividing process, and the liquid crystal injection and seal prevention process, then prior to the connection of the IC used for the drive, by cutting off along the scribe line (SB), the guard ring **100** is completely removed.

[**0115**] However, since the first protective element **140** connected between the LC-COM line **180** and the pad **160** is present, then even prior to the connection of the IC used as the drive, electrostatic protection is accomplished.

[**0116**] Furthermore, the first protective element also remains in the final product, however, with the protective element which uses TFT in order to accomplish positive threshold control, there is no concern of reducing the reliability of the product by means of the leakage of electric current and the like.

[**0117**] Next, an explanation is provided of the construction of the device of the first and second transistors (F1, F2) shown in **FIG. 11A**, with reference to **FIG. 12** and **FIG. 13**.

[**0118**] With the present embodiment, as shown in **FIG. 12**, the film (ITO film) **300**, **320**, and **330** formed from the

ITO comprising the pixel electrode material is used as the wiring used to connect the gate/drain.

[0119] The cross-sectional construction corresponding to each component (A)-(F) in the plane layout of **FIG. 4** is shown in **FIG. 13**.

[0120] As shown in the figure, the first thin film transistor F1 and the second thin film transistor F2 which compose the static electricity protection element are both provided with a reverse stagger construction (bottom gate construction).

[0121] In other words, formation of gate electrode layers **410**, **420**, **430**, and **440** is accomplished on the glass substrate **400**, formation of a gate insulation film **450** being accomplished on it, forming genuine amorphous silicon layers **470**, and **472**, and forming a drain electrode (source electrode) layer **492** through the n type ohmic layer **480**, a protective layer **460** being formed so as to cover each of these layers. Also, connections are established between the gate/drain by means of the films (ITO films) **300**, **320**, and **330** formed from the IPO which comprises the pixel electrode material.

[0122] The ITO films **300**, **320**, and **330** connect the gate electrode layer and the drain electrode layer through the contact hole which passes through the two films of the gate insulation film **450** on the gate electrode layer, and the protective film **460**; and through the contact hole which passes through the protective film **460** on the drain electrode layer **490**.

[0123] In this case, the ITO has superior step coverage at high melting points in comparison with those held by aluminum and the like, owing to which good contact is assured even through a deep contact hole passing through the two film layers.

[0124] In addition, as explained in the first embodiment, the contact hole relative to the gate/source is formed at the same time in the process of forming the aperture (pad open) for connecting the external connection terminal, thereby shortening the number of processes.

[0125] Above, an explanation has been provided with respect to an example for forming the protective diode using the ITO film as wiring. However, the use of the ITO film as wiring is not limited to this, and for example it is possible for utilization to also be made of a format such as that shown in **FIG. 15**.

[0126] In other words, in **FIG. 15**, the ITO film **342** is used in the formation of the cross under wiring **342** in the vicinity of the pad **160**.

[0127] The "cross under wiring" at the time of leading the inner wiring of the liquid display device toward the outside of the seal material **520**, in order to achieve protection of the wiring by means of a thick insulation film between the layers, connects the wiring of the upper layer to the wiring of the lower layer, and comprises wiring which is utilized to conduct round about to the outside.

[0128] In other words, the ITO film **342** connects the drain electrode layer **490** and the layer (gate electrode material layer) **412** which is formed from the same material as the gate electrode. By this means, the components led to the outside of the gate electrode material layer **412** are protected in both directions by the gate insulation film **450** and the protective film **460**, improving reliability.

[0129] Furthermore, in **FIG. 15**, the reference numbers **500** and **502** show facing film arrangement, **520** shows the seal material, **540** shows the opposing electrodes, **562** shows the glass substrate, and **140** shows the liquid crystal. In addition, connection of the bonding wire **600** is accomplished, for example, on the pad **160**. In substitution for the bonding wire, there are also cases when connection is accomplished of the electrode layers utilizing the (bump-phonetic) electrode or the polyimide film.

[0130] The ITO film may also be used as wiring in various other locations. **FIG. 16** shows an easily understood example of locations in which utilization of the ITO film may be used as wiring.

[0131] In **FIG. 16**, the ITO film is shown as a fat solid line.

[0132] The ITO film in the locations A1-A3 is utilized as wiring for the formation of the protective element, and in location A4, the ITO film is utilized as wiring for connecting the scanning line **52** and the pad **160**B, and in location AS, the ITO film is used as the cross-under wiring shown in **FIG. 15**.

[0133] In addition, in location A6, the ITO film is used as wiring for connecting the horizontal LC-COM line and the perpendicular LC-COM line. In other words, the horizontal LC-COM line is formed from a gate material, and the perpendicular LC-COM line is formed from a source material, owing to which it is necessary for both to be connected by the ITO.

[0134] Furthermore, in location A6 in **FIG. 16**, the silver point pad **110** may be formed as a unit by means of the same process as one of either the horizontal LC-COM line or the perpendicular LC-COM line, and when thus formed, connection of the silver point pad **110** and the LC-COM line (either the horizontal or perpendicular line) not formed in a unit may be accomplished through the silver pad **110** and the ITO.

[0135] Next, an explanation is provided with regard to the construction of each pixel of the pixel components, with reference to **FIGS. 17 and 18**.

[0136] **FIG. 17** shows a plane surface layout of the pixel component.

[0137] The TFT (constructed so as to include a gate electrode **720**, a drain electrode **740**, and a genuine amorphous silicon layer **475** in which no impurities are doped) is arranged to function as a switching element and is connected to the scanning line **52** and the signal line **54**. The pixel electrode (ITO) **340** is connected to the drain electrode **740**. In the diagram, K2 represents the contact hole, and Cad shows the maintenance capacity. The maintenance capacity *Cad* is composed from a buildup of proximate gate wiring and extended pixel electrodes.

[0138] **FIG. 18** is a diagram which shows the cross-sectional construction along the line B-B in **FIG. 17**. The cross-sectional construction is the same as the structure described in **FIG. 15**.

Third Embodiment

[0139] An explanation is provided hereafter with regard to the method of manufacture of the TFT substrate applied in the second embodiment described above, with reference to **FIGS. 19-26**.

[0140] In each diagram, the left side is a region in which the switching transistor of the pixel element is formed, and the center region is the region in which the protective element is formed, and the right region (pad component) is where the external connection terminal is connected.

[0141] (1) As shown in **FIG. 19**, first of all, utilization is made of photo lithography technology on the glass (non-alkali substrate) substrate **400**. For example, formed are the electrodes **720**, **722**, **900**, **902**, **904** which are formed from Cr (chrome) having a thickness of about 1800 Å.

[0142] The Cr deposit is accomplished with a reduced pressure of 50 mTorr utilizing a magnetron sputter device. In addition, the Cr process is accomplished by means of dry etching in which utilization is made of Cl_2 type gas.

[0143] Reference numbers **720**, **900** are layers (gate electrode layers) which become TFT gate electrodes, wherein reference number **722** is a layer which corresponds to the scanning line **52** shown in **FIG. 17**. In addition, reference numbers **902**, and **904** are layers (gate electrode material layers) which are formed from the same material as the gate electrode layer.

[0144] (2) Next, as shown in **FIG. 20**, continuous formation of the gate insulation film **910** formed from silicon nitride film SiN_x and the like, formed by plasma CVD method, and genuine amorphous silicon film which does not include doped impurities, and the n type silicon film (ohmic layer) is accomplished. Continuing, patterning of the genuine amorphous silicon film and the n type silicon film (ohmic layer) is accomplished by means of dry etching in which utilization is made of SF_6 type etching gas.

[0145] By this means, formation of the genuine amorphous silicon layers **475** into islands, and n type silicon layers (ohmic layer) **477**, and **922** is accomplished.

[0146] The thickness of the gate insulation film **910** is, for example, approximately 4000 Å, and the thickness of the genuine silicon layers **475** and **920** are, for example, approximately 3000 Å, whereas the thickness of the ohmic layers **477** and **922** are, for example, about 900 Å.

[0147] With regard to this process, characteristically, there is no formation of a contact hole relative to the gate insulation film. Furthermore, the coating process of the photo resist, the light exposure process, and the etching removal process comprising three processes become unnecessary, and the number of processes is abbreviated.

[0148] (3) Next, as shown in **FIG. 21**, the source/drain electrode layers **740***a*, **740***b*, **930***a*, and **930***b* which are approximately 1500 Å and which are formed from Cr (chrome) are formed by means of sputtering and photo etching.

[0149] (4) Continuing, separation of the source and drain, removing the ohmic layer **477** and **922** center portions by means of etching is accomplished using the source/drain electrode layers **740***a*, **740***b*, **930***a*, and **930***b* as a mask.

[0150] The source/drain electrode layer patterning shown in **FIG. 21**, and the source/drain separation etching shown in **FIG. 22** are continuously accomplished within the same dry etching device chamber. In other words, initially, processing of the source/drain electrode layers **740***a*, **740***b*, **930***a*, and **930***b* is accomplished by means of Cl_2 type etching gas. Continuing, by switching the etching gas to the SF_6 type gas, etching of the center of the ohmic layers **477**, and **922** is accomplished. In this manner, dry etching is continued in its use, thereby simplifying the manufacturing operation.

[0151] (5) Next, as shown in **FIG. 23**, the protective film **940** is formed using the plasma CVD method. This protective film is, for example, a silicon nitride film SiN_x having a thickness of approximately 2000 Å.

[0152] (6) Next, as shown in **FIG. 24**, the protective film **940** is selectively etched using the SF_6 type etching gas is accomplished. In other words, at the same time as forming the aperture **160** of the pad, formation of the contact hole CP**1** and the contact hole K**8** and K**10** is accomplished.

[0153] The aperture **160** and the contact hole CP**1** are apertures formed through the built up film of the gate insulation film **910** and the protective film **940**, and the contact holes K**8** and K**10** are apertures which only pass through the protective film **940**.

[0154] In this instance, the gate electrode material layers **902** and **904** respectively function as etching stoppers at the time of forming the contact hole CP**1** and the aperture **160**, and the source/drain electrodes **740***a* and **930***b* respectively function as etching stoppers at the time of forming the contact holes K**8** and K**10**.

[0155] (7) Next, as shown in **FIG. 25**, the ITO (indium tin oxide) film is deposited with a thickness of approximately 500 Å utilizing a magnetron sputtering device), wherein etching is accomplished utilizing a compound liquid comprising $HCl/HNO_3/H_2O$, being processed into a specific pattern. By this means, the active matrix substrate is complete. In **FIG. 25**, the reference number **950** is a pixel electrode formed from ITO, the reference number **952** is wiring formed from ITO which composes a part of the protective diode, and reference number **954** is an electrode (pad) formed from an ITO for connecting the external terminal.

[0156] Since ITO having good step coverage is used as wiring, a good electrical connection can be assured. As the pixel electrode material, utilization can be made also of other transparent electrode materials having a high melting point, such as metallic oxides. For example, use may be made of such metallic oxides as SnOx and ZnOx and the like.

[0157] In addition, as is clear from **FIG. 25**, a protective film **940** necessarily passes between the ITO layers **950** and **952**, and the source/drain electrodes **740***a*, **740***b*, **930***a*, and **930***b*. This means that in a wiring region (not shown in the diagram) on the substrate, the wiring layer formed from ITO and the source/drain electrode layer are assuredly electrically separated. Furthermore, there is no concern of shorting of two items being caused by foreign substances.

[0158] In addition, with this manufacturing method, since the ITO film is formed in the final process **(FIG. 25)**, there is little concern relating to staining caused by ITO composites such as tin (Sn) and indium (In). In this manner, according to the manufacturing method of the present embodiment, the manufacturing process of an active matrix substrate can be abbreviated. Furthermore, it is possible to mount a thin film circuit having high reliability as an adequate countermeasure for static electricity.

[0159] Furthermore, in **FIG. 25**, direct connection of ITO film **952** and **954** to the gate electrode layer **902** and to the gate electrode material layer **904** is accomplished. However, it is also possible for connection to be accomplished through other materials through buffer layers such as molybdenum (MO), tantalum (Ta), and titan (Ti) and the like.

[0160] Next, an explanation is provided with regard to the process for assembling a liquid crystal display device using a completed active matrix substrate.

[0161] As shown in **FIG. 28**, emulation of the opposing substrate **1500** and the TFT substrate **1300** is accomplished, and, following the cell division process shown in **FIG. 27**, enclosure of the liquid crystal is accomplished. Next, the IC used for the drive is connected, and furthermore as shown in **FIG. 28**, the assembly process using polarized light plates **1200**, and **1600** and the back light **1000** and the like is accomplished, thereby completing the active matrix liquid crystal display device.

[0162] **FIG. 26** is a cross-sectional diagram of the essential components of an active matrix liquid crystal display device. In **FIG. 26**, the same reference numbers are applied to the same locations as for the drawings shown in **FIGS. 15 and 18**.

[0163] In **FIG. 26**, regions are formed wherein the left side is an active matrix, and the center is a protective element (static electricity protective diode), and the right side is a pad. In the pad, an outer lead **5200** of the driver IC **5500** of the liquid crystal is connected through the anistropic conductive film **5000** on the electrode (pad) **954** formed from the ITO. The reference number **5100** is an electrically conductive granule, the reference **5300** is a film tape, and the reference number **5400** is a resin used for encapsulation.

[0164] In **FIG. 26**, adoption is made of the format (TAB) which uses a tape carrier as the method for connecting the driver-IC. However, other formats such as the COG (chip on glass) format may also be adopted.

[0165] The present invention is not limited to the above embodiment, and it is also possible to use an appropriate changed form as well where adoption is made of a positive stagger method TFT. In addition, as the pixel electrode material, utilization may also be made of other transparent electrode materials having a high melting point, such as metallic oxides, for the ITO. For example, utilization may be made of metallic oxides such as SnOx and ZnOx and the like. In this instance as well, the step coverage can withstand actual use.

[0166] If the liquid crystal display device of the present embodiment is used as a display device in a mechanism such as a personal computer, the value of the product is improved.

What is claimed is:

1. An active matrix substrate, comprising:

a scanning line;

a signal line;

a thin film transistor disposed in correspondence with intersections of the scanning line and the signal line;

a pixel electrode disposed in correspondence with the thin film transistor; and

a protective element to prevent static electricity destruction electrically connected between at least one of the scanning line and the signal line, and a common electric potential line, the protective element at least in part forming a pixel electrode material layer.

2. The active matrix substrate of claim 1, at least one of the scanning line and the signal line being electrically connected to an electrode to connect an external terminal, the protective element being electrically connected between the common electric potential line and the electrode to connect the external terminal.

3. The active matrix substrate of claim 1, the protective element using the thin film transistor.

4. The active matrix substrate of claim 3, one of a source electrode and a drain electrode of the thin film transistor for the protective element being electrically connected to one of the scanning line and the signal line via the pixel electrode material layer.

5. The active matrix substrate of claim 3, the protective element including a diode that is formed from the thin film transistor electrically connected between a gate electrode and one of a source electrode and a drain electrode.

6. The active matrix substrate of claim 5, one of a source electrode and a drain electrode of the thin film transistor for the protective element being electrically connected to one of the scanning line and the signal line via the pixel electrode material layer.

7. The active matrix substrate of claim 5, a gate electrode of the thin film transistor for the protective element being electrically connected to one of the source electrode and the drain electrode of the thin film transistor via the pixel electrode material layer.

8. The active matrix substrate of claim 3, the protective element including a first diode formed from the connection of the gate electrode and a drain electrode of a first thin film transistor, and a second diode formed from the connection of the gate electrode and a drain electrode of a second thin film transistor, the first diode and the second diode being connected mutually in a reverse direction, in parallel.

9. The active matrix substrate of claim 1, the common electric potential line being electrically connected to a facing electrode.

10. The active matrix substrate of claim 9, the common electric potential line being electrically connected to a pad to connect a facing electrode via the pixel electrode material layer.

11. A liquid crystal display device, comprising:

the active matrix substrate of claim 1.

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