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- (21) Application No. 2825/77
- (22) Filed 24 Jan. 1977
- (31) Convention Application No. 656 677
- (32) Filed 9 Feb. 1976 in
- (33) United States of America (US)
- (44) Complete Specification published 14 May 1980
- (51) INT CL³ H03K 17/00
- (52) Index at acceptance H3T 2B2 2T3F MC
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(54) PREAMPLIFIERS

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to sense preamplifiers for memory systems or other small signal or analog circuits, and more particularly to memory sense amplifiers incorporating preamplifiers.

In the recent past there have been several improvements in sensing circuits for memory cells, particularly for the one device memory cell. One significant concept for improving the sensitivity of sensing circuits is the concept of charge transfer as described in United Kingdom Patent No. 1,397,152. Other references related to this concept are United Kingdom Patent No. 1,374,215 and United Kingdom Patent No. 1,371,468, United States Patent No. 3,774,176 entitled "Semiconductor Memory Having Single Transistor Storage Elements and a Flip-Flop Circuit for the Evaluation and Regeneration of Information", and United Kingdom Patent Application No. 26502/75 (Serial No. 1,495,063) and a paper entitled "High Sensitivity Charge-Transfer Sense Amplifier", 1975 IEEE International Solid-State Circuits Conference Digest, pp. 112—113, by L. G. Heller et al.

A preamplifier according to the invention, is responsive to the application of an input signal having either one of two different voltages to either one of a pair of input/output lines, and comprises first and second devices each having first and second current carrying electrodes and a control electrode, said first current carrying electrodes of said first and second devices being connected to respective ones of the

pair of input/output lines, said second current carrying electrode of said first device being coupled to said control electrode of said second device via a first node, said second current carrying electrode of said second device being coupled to said control electrode of said first device via a second node, a first capacitor having a first electrode connected to said second node, a second capacitor having a first electrode connected to said first node, precharge circuit means to apply to a precharge voltage onto said first and second nodes to cause said first and second devices to turn on whereby each of the input/output lines charges up to a predetermined voltage lying between said two different voltages, the subsequent application of such a said input signal to one of the input/output lines increasing the threshold voltage of one of said first and second devices, and means to apply a ramp voltage to the other electrodes of said first and second capacitors whereby said one of said first and second devices turns on more than the other and transfers more charge to the input/output line to which it is connected than is transferred by the other of said first and second devices to the input/output line to which it is connected.

How the invention can be carried into effect will now be described by way of example, with reference to the accompanying drawings, in which:—

FIGURE 1 represents one cross-coupled charge transfer preamplifier circuit embodying the invention;

FIGURE 2 represents another embodiment of a cross-coupled transfer preamplifier circuit;

FIGURE 3 is a timing diagram showing the pulse sequence for the operation of the embodiments of Figures 1 and 2;

FIGURES 4, 6, 8 and 10 are circuit diagrams of cross-coupled charge transfer sense amplifier circuits each of which includes a cross-coupled charge transfer preamplifier;

FIGURES 5, 7, 9 and 11 are timing

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diagrams of the pulsing sequences for operation of the circuits of Figures 4, 6, 8 and 10 respectively.

A preamplifier circuit 10 (Figure 1) includes cross-coupled charge transfer means and is connected between a pair of input/output lines consisting of bit/sense line (B/S) segments 16 and 18 which are operably associated with a row of storage cells in a memory matrix (not shown). Preamplifier circuit 10 includes two actuatable devices 20 and 22 such as MOSFET's, the gate electrodes of which are connected to a phase 1 line. Preamplifier circuit 10 also includes actuatable devices 24 and 26 such as MOSFET's wherein device 24 is connected to B/S line segment 16 and also to actuatable device 20 at a circuit node 28. Device 26 is connected to B/S line segment 18 and also to actuatable device 22 at a circuit node 30. The gate electrode of device 24 is cross-coupled to node 30 and also connected through capacitor 32 to a phase 2 line. The gate electrode of device 26 is cross-coupled to node 28 and also connected through capacitor 34 to the phase 2 line. Capacitors 36 and 38 represent parasitic capacitance which is inherent in the B/S lines. The parasitic capacitances are shown in Figs. 1 and 2 for completeness, but are assumed but not shown in the figures for the remaining embodiments.

The preamplifier 10 of Fig. 1 will be described with reference to the pulsing sequence illustrated in the timing waveform of Fig. 3 wherein the period A—B is the pre-charge period, B—C is the period wherein the signal to be sensed is developed, and C—D is the charge transfer period. The actuatable devices are assumed for purposes of explanation to be N-channel, enhancement type. Initially, the phase 1 line is activated, turning on devices 20 and 22 which are made to operate in the linear region. Thus, nodes 28 and 30 will charge to the power supply potential V_1 which is connected to devices 20 and 22. As nodes 28 and 30 charge up, cross-coupled charge transfer devices 24 and 26 will also turn on. Devices 24 and 26 operate in the saturation region and, therefore, the bit/sense line segments 16 and 18 are caused to charge up until they are at a predetermined cutoff value $V_1 - V_t$ where V_t is the device threshold voltage and is a function of source to substrate voltage. Assuming that the bit/sense line segments 16 and 18 are associated with a row of storage cells which each consist of a capacitor and a single FET for gating charge into and out of the capacitor, the voltage V_1 is selected such that bit/sense line segments 16 and 18 are at a threshold potential midway between a worst case stored "1" and worst case stored "0" voltage level in the storage cell

capacitor, where the "1" and "0" are high and low levels, respectively. Devices 24 and 26 then are at their cutoff state and the phase 1 line is now deactivated turning devices 20 and 22 off, thus ending the pre-charge period. If desired, it is also possible to perform an incomplete precharge, i.e., devices 20, 22 are turned off when charge-transfer devices 24, 26 are in a close-to-cutoff state. As a result, charge-transfer will take place between nodes 28, 30 and bit/sense lines 16, 18. Devices 24 and 26 will cutoff to a high degree since any charge transfer which takes place after devices 20 and 22 are turned off will cause the potential to drop on the gates of devices 24 and 26 (and nodes 28 and 30) thus forcing them to cutoff hard. It is also possible to enhance the gate-to-source capacitance of devices 20, 22 so that when the phase 1 line is deactivated outcoupling takes place at nodes 28, 30 sufficient to turn charge-transfer devices 24, 26 off.

After the precharge period, a word line WL of the memory matrix (not shown) is accessed and, depending on the information stored in the accessed storage cell, the sense signal will be either positive or negative, with the bit/sense lines charged to a midway potential. Assuming that a word line is accessed on the left side of the circuit and that the stored potential is zero volts, a negative signal is, therefore developed on the bit/sense line capacitance. Correspondingly, the source potential of device 24 drops to V_{sense} and its threshold voltage also decreases an incremental amount due to the backgate bias effect. The additive combination of the sense signal and the incremental threshold voltage decrease serve to give device 24 a higher gate drive ($V_{\text{gate}} - V_{\text{sense}} - V_{\text{threshold}}$) than device 26.

After the sense signal is introduced, the phase 2 line is ramped positive causing the potential on nodes 28 and 30 to momentarily increase. A point will be reached where device 24 will turn on initially by an amount to cause significant positive charge to transfer from node 28 to the bit/sense line 16. The bit/sense line capacitance is much larger than the capacitance at node 28. Therefore, the potential at node 28 will decrease and so cause device 26 to be turned off. As the phase 2 ramp continues to rise positively the potential at node 30 rises while the potential at node 28 falls until device 24 is taken out of saturation and driven into the linear region at which point charge transfer ceases. Little or no charge was transferred from node 30 to bit/sense line 18, therefore, node 30 experiences only a voltage rise. Essentially then, a preamplified signal is developed across nodes 28 and 30, which is at least equal to a device threshold voltage and independent of the magnitude of the

sense signal (assumed small in comparison). Therefore, the preamplifier circuit provides charge gain, i.e., the preamplified signal across nodes 28 and 30 may contain more charge than was stored the storage cell capacitor. At this point the preamplification phase is completed. The dashed line in the phase 2 waveform indicates that phase 2 turnoff time is non-critical. The same notation will be used in later embodiments.

If a "1" were stored in the memory cell, a positive signal would have been introduced onto the left bit/sense line. The previously described circuit operation is the same except that charge transfer would have taken place through device 26 and the preamplified signal at nodes 28 and 30 would have been of opposite polarity.

The preamplifier circuit 12 of Fig. 2 operates in much the same manner as the preamplifier circuit 10 of Fig. 1. The operation of the circuit of Fig. 2 is as follows. The $\phi 1$ line is activated turning on devices 20, 22, 40 and 42. Since these devices are made to operate in the linear region nodes 28, 30 charge to $+V_1$ volts and nodes 44, 46 charge to $+V_2$ volts. As nodes 28 and 30 charge up, cross-coupled charge-transfer devices 24 and 26 will also turn on. Devices 24 and 26 operate in the saturation region and, therefore, the bit/sense line segments 16 and 18 are caused to charge up until they are at a predetermined cutoff value $V_1 - V_t$. Nodes 44 and 46 charge to $+V_2$ volts, where V_2 is larger than V_1 . With devices 24 and 26 at their cutoff state the phase 1 is deactivated turning devices 20, 22, 40 and 42 off, thus ending the precharge period.

After the precharge period, a word line is accessed. Assume a sense signal consisting of a negative drop in potential is developed on the left bit/sense line. As previously explained device 24 has a higher gate drive than device 26.

After the sense signal is introduced, the phase 2 line is ramped positive causing the potential on nodes 28 and 30 to momentarily increase. As previously explained a point will be reached where device 24 will turn on initially by an amount to cause significant positive charge to transfer from node 44 to the bit/sense line 16. The bit/sense line capacitance is much larger than the capacitance at node 44. Therefore, the potential at node 44 will decrease. Also as a result of coupling through capacitor 48, node 28 will also drop in potential turning device 26 off. As the phase 2 ramp continues to rise positively the potential at nodes 30 and 46 rises while the potential at nodes 28 and 44 falls until device 24 is taken out of saturation and driven into the linear region at which point charge-transfer ceases. Little or no charge was transferred from node 46 to bit/sense line 18, therefore nodes 30 and 46

experience only a voltage rise. A preamplified signal is developed across nodes 44 and 46 which can be much larger than a device threshold voltage. Again this is possible through charge gain. At this point the preamplification phase is completed. The introduction of a positive signal on B/S line 16 results in a preamplified signal across nodes 44 and 46 of the opposite polarity.

A complete sense amplifier circuit which includes the preamplifier circuit 10 is shown in Fig. 4. The pulsing sequence is shown in Fig. 5. The preamplified signal appears across nodes 28 and 30 as previously described. Therefore, after preamplification, the $\phi 3$ line is activated turning devices 52, 54 on and charging the bit/sense lines to stored "1" level. Devices 52, 54 are then turned off. The $\phi 4$ line is now ramped slowly toward ground potential. Since node 28 is lower in potential relative to node 30, assuming a negative sense signal is being sensed on the left-hand B/S line, device 58 will turn on before device 56. The ramp rate is such as to allow node 28 to follow $\phi 4$ within a threshold voltage of device 56. Device 56 then never turns on. As node 28 discharges, device 24 turns on causing bit/sense line 16 to discharge. The bit/sense line is made to discharge down to ground potential. Since this was the original information in the memory cell its word line is deactivated; the information has been written back. The $\phi 4$ line is returned to $+V_1$ volts and the $\phi 2$ line is returned to 0 volts. The sense cycle is completed with the $\phi 5$ line activated discharging both bit/sense lines to ground potential. If a "1" had been sensed, devices 26 and 56 would turn on and the left B/S line 16 would stay high inserting the "1" level back into the memory cell.

Another sense amplifier circuit which includes preamplifier circuit 10 is shown in Fig. 6. The associated pulsing sequence is shown in Fig. 7. The preamplified signal appears across nodes 28 and 30. The $\phi 3$ and $\phi 4$ lines are activated charging the bit/sense lines to the high level. The $\phi 3$ line is then deactivated. The $\phi 5$ line is ramped toward ground potential with the condition previously stated. Assuming a negative signal on B/S line 16, device 58 will turn on discharging bit/sense line 16 to ground potential. The word line is deactivated. The $\phi 2$ and $\phi 4$ lines are returned to 0 volts and the $\phi 5$ lines is returned to $+V_1$ volts. $\phi 6$ is activated discharging both B/S lines to ground potential and the sense cycle is completed. The sensing of a "1" on B/S 16 results in B/S line 16 remaining high and a "1" being written back into the memory cell.

Another complete sense amplifier circuit is shown in Fig. 8. This embodiment is similar to that of Fig. 4 with preamplifier 10

replaced by preamplifier 12. The associated timing diagrams shown in Fig. 9 are similar to Fig. 5.

5 Similarly the embodiment of another complete sense amplifier circuit shown in Fig. 10 is similar to that shown in Fig. 6 with preamplifier 10 replaced with preamplifier 12. The associated timing diagrams shown in Fig. 11 are equivalent to Fig. 7.

10 What has been described has been preamplifiers and complete sense amplifiers which have been embodied in a memory cell array application. However, it should be evident to one skilled in the art that the described circuits incorporating the cross-coupled charge transfer techniques to provide both voltage and charge gain can be generally used as signal sensors for sensing small signals in comparators, polarity sensors, and other small signal or analog circuit applications.

WHAT WE CLAIM IS:—

1. A preamplifier responsive to the application of an input signal having either one of two different voltages to either one of a pair of input/output lines, the preamplifier comprising first and second devices each having first and second current carrying electrodes and a control electrode, said first current carrying electrodes of said first and second devices being connected to respective ones of the pair of input/output lines, said second current carrying electrode of said first device being coupled to said control electrode of said second device via a first node, said second current carrying electrode of said second device being coupled to said control electrode of said first device via a second node, a first capacitor having a first electrode connected to said second node, a second capacitor having a first electrode connected to said first node, precharge circuit means to apply a precharge voltage onto said first and second nodes to cause said first and second devices to turn on whereby each of the input/output lines charges up to a predetermined voltage lying between said two different voltages, the subsequent application of such a said input signal to one of the input/output lines increasing the threshold voltage of one of said first and second devices, and means to apply a ramp voltage to the other electrodes of said first and second capacitors whereby said one of said first and second devices turns on more than the other and transfers more charge to the input/output line to which it is connected than is transferred by the other of said first and second devices to the input/output line to which it is connected.

2. A preamplifier as claimed in claim 1, in which the precharge circuit means includes third and fourth devices each having first and second current carrying electrodes and

a control electrode, said second electrode of said third device being coupled to said first node, said second electrode of said fourth device being coupled to said second node, and a source of control signal of a given duration connected to said control electrodes of said third and fourth devices to turn them on, to thereby apply said precharge voltage onto said first and second nodes.

3. A preamplifier as claimed in claim 2, further including fifth and sixth devices each having first and second current carrying electrodes and a control electrode, said second electrode of said fifth device being connected to said second electrode of said first device at a third node, and said control electrode of said fifth device being connected to said source of control signal, said second electrode of said sixth device being connected to said second electrode of said second device at a fourth node and said control electrode of said sixth device being connected to said source of control signal, a third capacitor connected between said first and third nodes, a fourth capacitor connected between said second and fourth nodes, the arrangement being such that, in operation, said control signal of a given duration also functions to turn said fifth and sixth devices on to thereby apply a second precharge voltage onto said third and fourth nodes, said second precharge voltage being larger than said first precharge voltage by more than the threshold voltage of said devices and the application of said ramp voltage to said first and second capacitors causes said one of said first and second devices to turn on more than the other and to transfer more charge from one of said third and fourth nodes to the input/output line to which it is connected than is transferred by the other of said first and second devices to the input/output line to which it is connected.

4. A preamplifier as claimed in any preceding claim, which is incorporated in a sense amplifier associated with a memory array, said input/output lines comprising bit/sense line segments of the memory array.

5. A memory sense amplifier including a preamplifier as claimed in claim 1 or claim 2, the input/output lines comprising memory bit/sense line segments, fifth, sixth, seventh and eighth devices, each having first and second current carrying electrodes and a control electrode, said second current carrying electrodes of said fifth and sixth devices being connected to respective ones of the memory bit/sense line segments, said second current carrying electrodes of said seventh and eighth devices being respectively connected to said first and second nodes, a signal source connected to said control electrodes of said fifth and sixth devices for

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- turning said fifth and sixth devices on after said precharge voltage is applied on said first and second nodes for transferring charge to said bit/sense line segments, a signal source connected to said first current carrying electrodes of said seventh and eighth devices for turning on one of said seventh and eighth devices and discharging one of said first and second nodes connected thereto and thereby turning on one of said first and second devices connected to said one of said first and second nodes and thereby discharging one of said bit/sense line segments connected to one of said first and second devices. 55
- 5 6. A memory sense amplifier including a preamplifier as claimed in claim 1 or claim 2, the input/output lines comprising memory bit/sense line segments, fifth, sixth, seventh, eighth, ninth and tenth devices, each having first and second current carrying electrodes and a control electrode, said second current carrying electrodes of said fifth and sixth devices being connected to respective ones of the bit/sense line segments, said control electrodes of said seventh and eighth devices being respectively connected to said first and second nodes, a first signal source connected to said control electrodes of said fifth and sixth devices and a second signal source connected to said control electrodes of said ninth and tenth devices for turning them on after said precharge voltage is applied on said first and second nodes for transferring charge to said bit/sense line segments, and a second signal source connected to said first current carrying electrodes of said seventh and eighth devices for turning one of said seventh and eighth devices and discharging one of said bit/sense line segments. 60
- 10 7. A memory sense amplifier including a preamplifier as claimed in claim 3, the input/output lines comprising memory bit/sense line segments, seventh, eighth, ninth and tenth devices, each having first and second current carrying electrodes and a control electrode, said second current carrying electrodes of said seventh and eighth devices being connected to respective ones of the bit/sense line segments, said second current carrying electrodes of said seventh and eighth devices being connected to said control electrodes of said ninth and tenth devices being respectively connected to said fourth and third nodes, a first signal source connected to said control electrodes of said seventh and eighth devices and a second signal source connected to said control electrodes of said eleventh and twelfth devices for turning said devices on after said precharge voltage is applied on said third and fourth nodes for transferring charge to said bit/sense line segments, a signal source connected to said first current carrying electrodes of said ninth and tenth devices for turning on one of said ninth and tenth devices and discharging one of said bit/sense line segments. 65
- 15 8. A memory sense amplifier including a preamplifier as claimed in claim 3, the input/output lines comprising memory bit/sense line segments, seventh, eighth, ninth, tenth, eleventh and twelfth devices, each having first and second current carrying electrodes and a control electrode, said second current carrying electrodes of said seventh and eighth devices being connected to respective ones of the bit/sense line segments, said control electrodes of said ninth and tenth devices being respectively connected to said fourth and third nodes, a first signal source connected to said control electrodes of said seventh and eighth devices and a second signal source connected to said control electrodes of said eleventh and twelfth devices for turning said devices on after said precharge voltage is applied on said third and fourth nodes for transferring charge to said bit/sense line segments, a signal source connected to said first current carrying electrodes of said ninth and tenth devices for turning on one of said ninth and tenth devices and discharging one of said bit/sense line segments. 70
- 20 9. A preamplifier substantially as described with reference to Figure 1 or Figure 2 of the accompanying drawings. 75
- 25 10. A memory sense amplifier substantially as described with reference to Figure 4, Figure 6, Figure 8 or Figure 10 of the accompanying drawings. 80
- 30 7. A memory sense amplifier including a preamplifier as claimed in claim 3, the input/output lines comprising memory bit/sense line segments, seventh, eighth, ninth and tenth devices, each having first and second current carrying electrodes and a control electrode, said second current carrying electrodes of said seventh and eighth devices being connected to respective ones of the bit/sense line segments, said second current carrying electrodes of said seventh and eighth devices being respectively connected to said ninth and tenth devices being respectively connected to said third and fourth nodes, a signal 85
- 35 9. A preamplifier substantially as described with reference to Figure 1 or Figure 2 of the accompanying drawings. 90
- 40 10. A memory sense amplifier substantially as described with reference to Figure 4, Figure 6, Figure 8 or Figure 10 of the accompanying drawings. 95
- 45 7. A memory sense amplifier including a preamplifier as claimed in claim 3, the input/output lines comprising memory bit/sense line segments, seventh, eighth, ninth and tenth devices, each having first and second current carrying electrodes and a control electrode, said second current carrying electrodes of said seventh and eighth devices being connected to respective ones of the bit/sense line segments, said second current carrying electrodes of said seventh and eighth devices being respectively connected to said ninth and tenth devices being respectively connected to said third and fourth nodes, a signal 100
- 50 9. A preamplifier substantially as described with reference to Figure 1 or Figure 2 of the accompanying drawings. 100
10. A memory sense amplifier substantially as described with reference to Figure 4, Figure 6, Figure 8 or Figure 10 of the accompanying drawings.

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FIG. 1

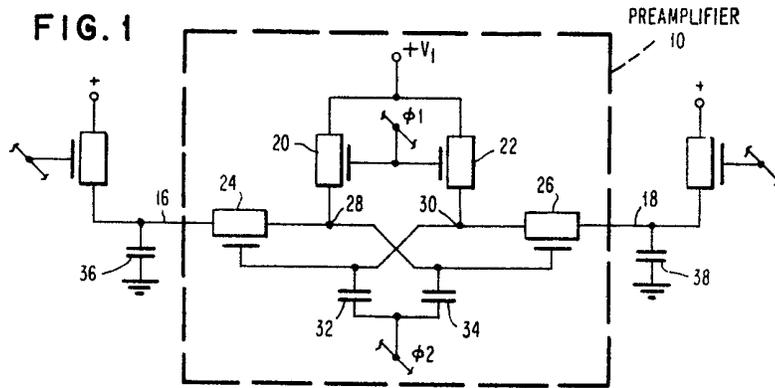


FIG. 2

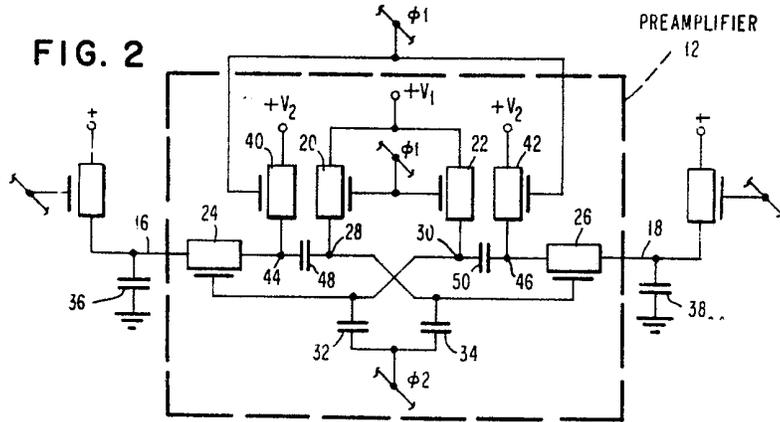


FIG. 3

