Oct. 18, 1966 A. NATHAN 3,280,319

ELECTRONIC MULTIPLIER

Filed Feb. 13, 1963 4 Sheets-Sheet 1

FIG. 1

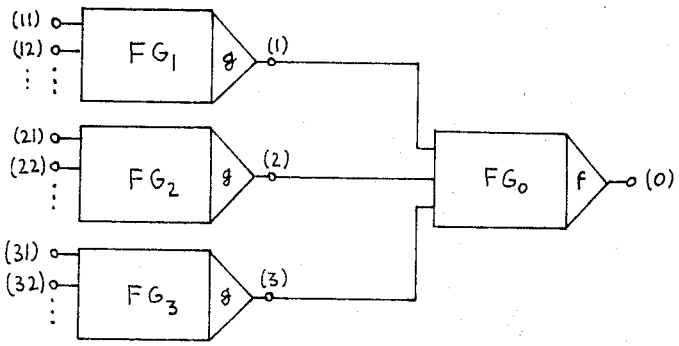


FIG. 2

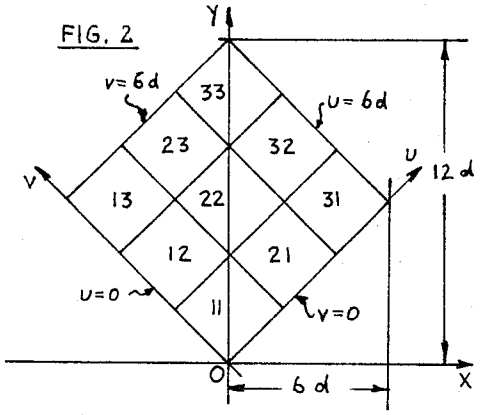


FIG. 3

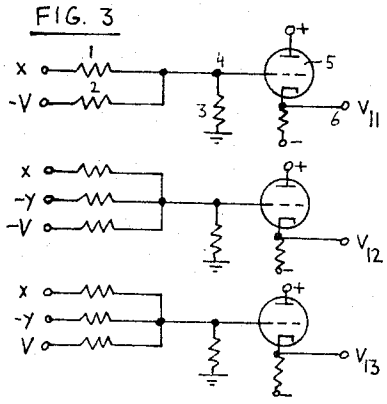
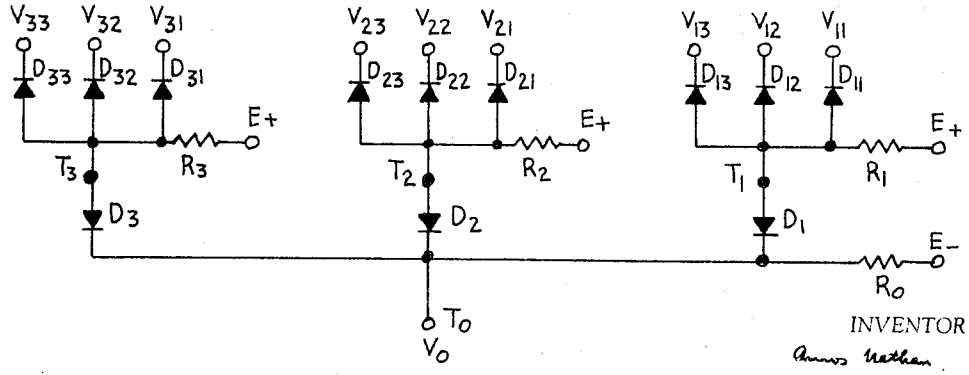


FIG. 4



INVENTOR

Amos Nathan

Oct. 18, 1966 A. NATHAN 3,280,319

ELECTRONIC MULTIPLIER

Filed Feb. 13, 1963 4 Sheets-Sheet 2

FIG. 5

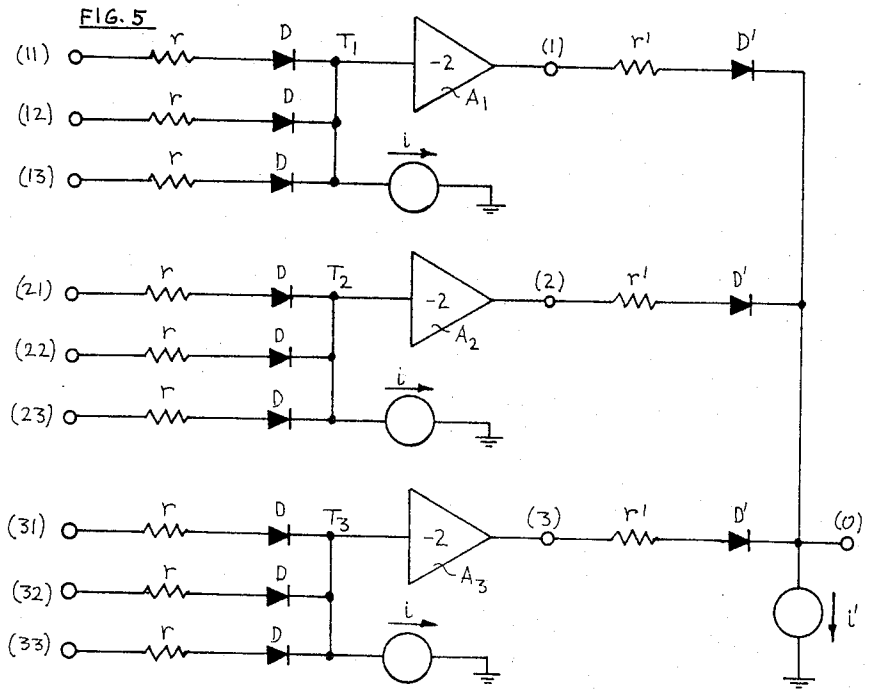
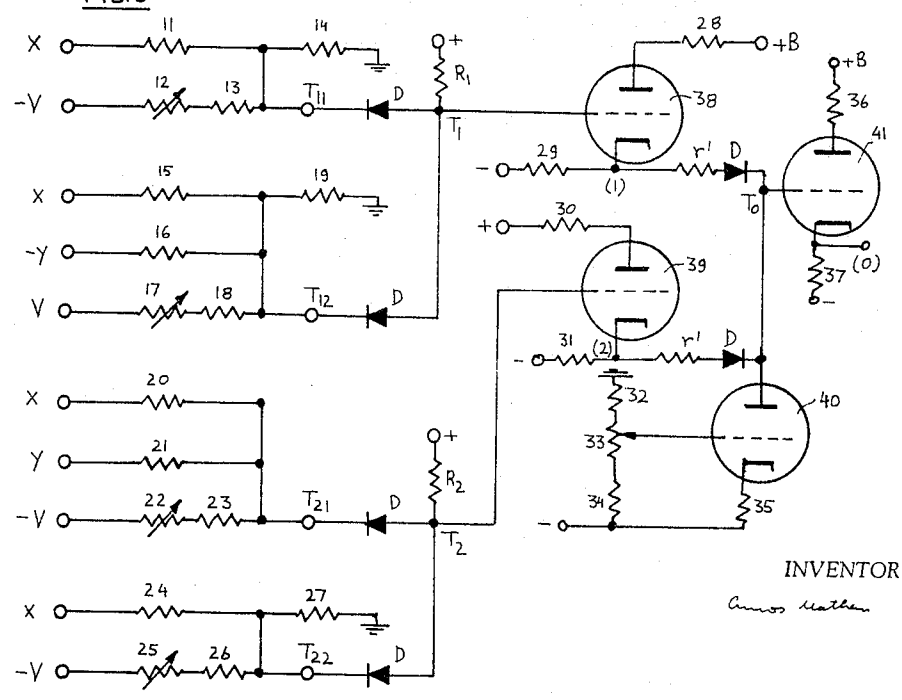


FIG. 6



INVENTOR

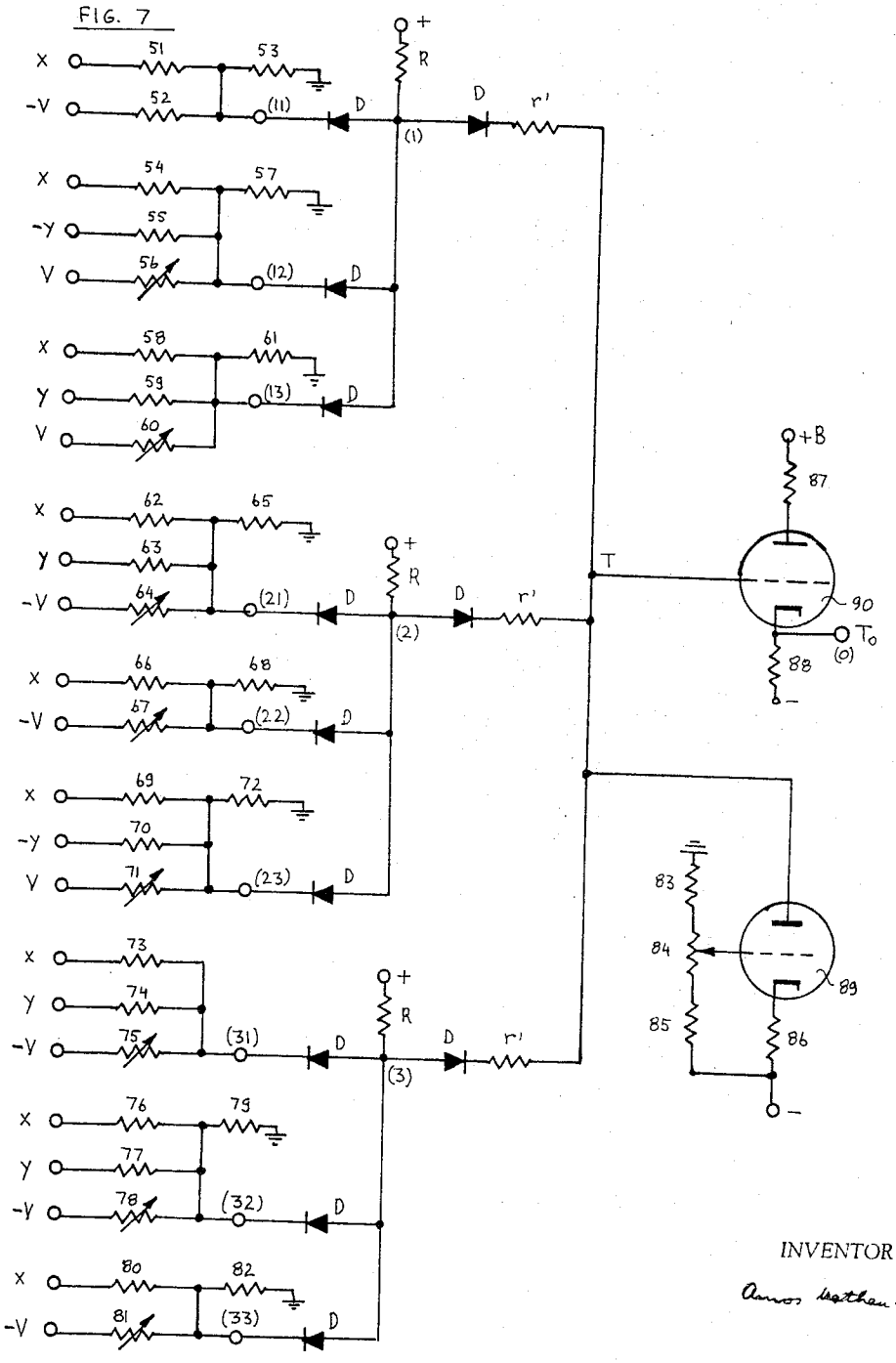
Amos Nathan

Oct. 18, 1966 A. NATHAN 3,280,319

ELECTRONIC MULTIPLIER

Filed Feb. 13, 1963 4 Sheets-Sheet 3

FIG. 7



INVENTOR

Amos Nathan.

Oct. 18, 1966

A. NATHAN

3,280,319

ELECTRONIC MULTIPLIER

Filed Feb. 13, 1963

4 Sheets-Sheet 4

FIG. 8

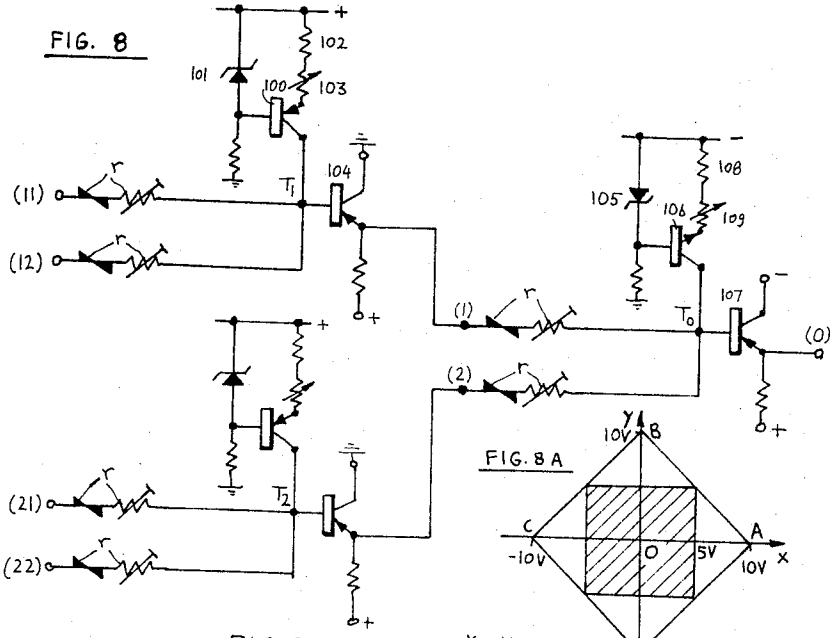


FIG. 8A

FIG. 9

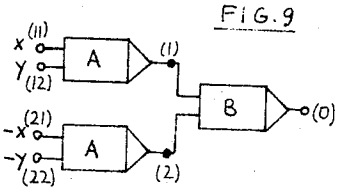


FIG. 10

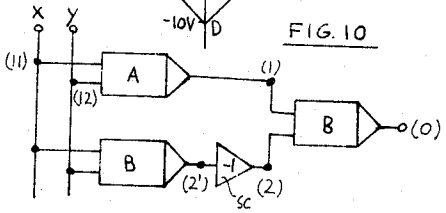


FIG. 11

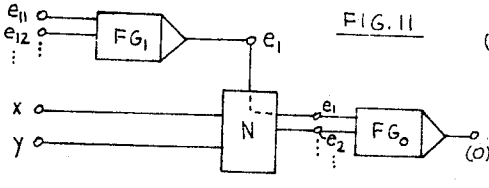


FIG. 13

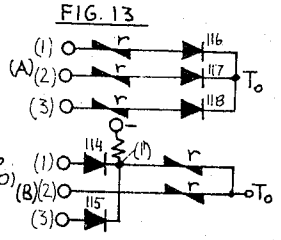
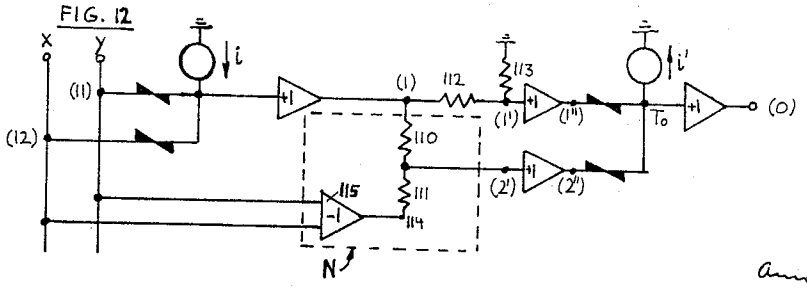


FIG. 12



INVENTOR

Amos Nathan.

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Patented Oct. 18, 1966

3,280,319

ELECTRONIC MULTIPLIER

Amos Nathan, Dept. El Engg., Technion, Haifa, Israel

Filed Feb. 13, 1963, Ser. No. 258,301
18 Claims. (Cl. 235—194)

This invention relates to electronic analog multipliers in which an output signal is produced which represents the product of the instantaneous values of two variables. More specifically, this invention includes a squarer having the transfer property which consists in transferring to its output terminal any signal simultaneously applied to all input terminals thereof.

This application is a continuation in part of my prior copending applications Serial No. 801,468 filed March 24, 1959, and Serial No. 837,616 filed September 2, 1959, both now abandoned.

Electronic multipliers have a great number of applications. Of particular interest is their application in analog computers in which the variables are represented in the form of electric potentials. One prior art embodiment of such multipliers uses the quarter squares system in which the product z of x and y is written as follows:

$$z=x\cdot y=u^2-v^2$$

where u and v are given by the expressions

$$u=(y+x)/2$$
$$v=(y-x)/2$$

A quarter squares multiplier first produces signals corresponding to u and v, subsequently employs two squarers for the production of u^2 and v^2 from u and v, respectively and finally produces z by taking the difference of the square signals. Such a multiplier, while simple in principle, has a number of disadvantages: It usually requires a considerable number of sign changers and/or adders in its implementations; it is liable to introduce errors because of the need of computing x as the difference of two quantities both of which may be large while the required result may be small.

In particular, any quarter squares multiplier employs at least one sign changer or one added for the production of the difference of u^2 and v^2, which are first separately produced.

This invention makes use of one or more squarers having the "transfer' property in a novel circuit configuration which eliminates the need for said one sign changer or said one adder and simultaneously does not produce z as the difference of two separately produced functions, thus eliminating another of the disadvantages of quarter squares multipliers. For this purpose the invention produces in a first stage from x and y as input signals a plurality of secondary input signals which represent the sums of u^2 and third signals, said secondary signals being fed to a second stage consisting of a transferring squarer adapted to produce from said third signals a signal representing $-v^2$ and simultaneously transferring u^2 to its output terminal, whereat a signal representing z for the instantaneous values of x and y is thereby produced.

Function generators having the transfer property and being thus suitable for use in the present invention are described in my copending application, Serial Number 837,617 filed September 2, 1959, entitled "Electronic Function Generator with Interpolating Resistors," now Patent No. 3,106,639. Another type of function generator suitable for use in the present invention consists of simple diode selection circuits comprising a plurality of input terminals, one diode each connected to a corresponding one of said input terminals, said diodes having a common output connection, their polarity being such

that either all anodes or all cathodes are connected at said common connection.

The invention will now be more particularly described in connection with the accompanying drawings in which

FIGURE 1 is a block diagram illustrating the use of transferring function generators for the production of functions of two variables;

FIGURE 2 is a plot of the x, y plane and of its subdivision into regions which are of interest in some embodiments of this invention;

FIGURE 3 is a schematic diagram of circuits for the production of input voltages for the multiplier of FIGURE 4;

FIGURE 4 is a schematic diagram of one embodiment of the invention using diode selection circuits as basic squarers;

FIGURE 5 is a schematic diagram of one embodiment of the invention, using piecewise-linear interpolators as basic squarers;

FIGURE 6 is a schematic diagram of another embodiment of the invention that uses piecewise-linear interpolators as basic squarers;

FIGURE 7 is a schematic diagram of a direct coupled embodiment of the invention;

FIGURE 8 is one embodiment of a four-quadrant multiplier of the invention using non-linear interpolating squarers as basic elements;

FIGURE 8A is a plot of the x, y plane relating to the embodiment of FIGURE 8;

FIGURE 9 is a block diagram corresponding to the multiplier of FIGURE 8;

FIGURE 10 is a block diagram of a four-quadrant multiplier of the invention using only one sign-changer;

FIGURE 11 is a block diagram of bilinear function generators;

FIGURE 12 is a schematic diagram of one embodiment of a bilinear multiplier of this invention;

FIGURES 13A and B are scrap circuit diagrams relating to multipliers of the invention.

Let it be required to produce the function

$$F(x,y)=f(s)+g(t)$$

where s and t are both functions of x and y. FIGURE 1 is a block diagram of a function generator producing F. In FIGURE 1, FG_1, FG_2 and FG_3 are similar function generators having a plurality of input terminals at **11**, **12**, . . . ; **21**, **22**, . . . ; and **31**, **32**, . . . ; **21**, **22**, . . . ; and **31**, **32**, . . . , respectively, and possessing the transfer property. FG_1 produces at terminal **1** the function $g(t)$ when input terminals **11**, **12**, . . . are fed with voltages e_{g1}, e_{g2}, . . . , which are each suitable functions of x and y or suitable constants. FG_2 similarly produces at terminal **2** the function $g(t)$ when the same input voltages are fed to terminals **21**, **22**, . . . , respectively. FG_3 is similarly adaptable to produce $g(t)$ at terminal **3**. FG_0 is a transferring function generator which produces $f(s)$ at output terminal **0** if voltages e_{f1}, e_{f2}, e_{f3} are applied at terminals **1**, **2**, **3**, respectively.

In order to produce $F(x,y)$ the function generator corresponding to FIGURE 1 proceeds as follows:

FG_1 is fed with voltages:

$e_{11}=e_{f1}+e_{g1}$ at **11**
$e_{12}=e_{f1}+e_{g2}$ at **12**

etc.

FG_2 is fed with voltages:

$e_{21}=e_{f2}+e_{g1}$ at **21**
$e_{22}=e_{f2}+e_{g2}$ at **22**

etc.

FG_3 is fed with voltages:

$e_{31}=e_{f3}+e_{g1}$ at **31**

$e_{32}=e_{f3}+e_{g2}$ at **32**

etc.

FG_1 thereby produce at terminal (**1**) the voltage

$$e_1=e_{f1}+g(t)$$

because e_{f1}, being simultaneously applied to all input terminals is transferred to terminal **1**, whereas e_{g1}, e_{g2}, etc. produce $g(t)$ at terminal **1** irrespective of the signal which is simultaneously transferred through FG_1.

FG_2 similarly produces at terminal **2** the signal

$$e_2=e_{f2}+g(t)$$

and FG_3 produces at terminal **3** the signal

$$e_3=e_{f3}+g(t)$$

The signals e_1, e_2, e_3 are the input signals to FG_0 which therefore transfers $g(t)$ to output terminal **0** and simultaneously produces thereat the signal $f(s)$. The total signal thus produced at output terminal **0** is therefore equal to $F(x,y)$, as required. The circuit for the production of e_1, e_2, . . . , will be called the first stage of the function generator while FG_0 constitutes its second stage. In the above example FG_0 has three input terminals this being purely illustrative. In general the second stage has two or more input terminals.

In order to apply these considerations to multipliers we write $s=u$ and $t=v$, u and v being defined above, and

$$F(x,y)=xy=f(u)+g(v)=u^2-v^2$$

The function $f(u)=u^2$ thus requires a squarer for its production and the function $g(v)=-v^2$ requires another squarer which simultaneously changes the sign and produces $-v^2$ from suitable input signals. Another way of applying the scheme of FIGURE 1 to multipliers is by taking $s=v$ and $t=u$ and thus

$$F(x,y)=f(v)+g(u)=-v^2+u^2$$

In this case the second stage must be a squarer and the first stage a sign reversing squarer. Both schemes are clearly equivalent and it will be sufficient to describe one of them.

As an example of a multiplier of the invention let it be required to design a multiplier operative for values of x and y within the square area defined in the plot of FIGURE 2 by u and v between **0** and $6d$, where $d=(50/12)$ volt in this example. A multiplier of this invention which produces an approximation to an output voltage

$$e_0=(1/100)xy \text{ volt}$$

where x and y are both in volts will be described in connection with FIGURES 3 and 4 in which FIGURE 3 corresponds to the input unit and FIGURE 4 comprises both stages of the multiplier. In order to understand the operation of the circuit it is best to proceed from output voltage e_0 backwards to the input signals.

The second stage of the multiplier comprises terminals T_1, T_2, T_3, diodes D_1, D_2, D_3 connected thereto, respectively, said diodes having a common cathode connection at output terminal T_0 whereat output voltage e_0 is produced. Positive current is withdrawn from terminal T_0 through resistor R_0 connected to negative potential means at E_. We denote the voltages at terminals T_1, T_2, T_3 by e_1, e_2, e_3. The second stage transfers a signal representing $-(1/100)v^2$ and simultaneously produces a signal representing $(1/100)u^2$. Production of $(1/100)u^2$ alone would require input signals

$$e'_1=(1/100)(2uU-U^2)$$

where $U=(2i-1)\cdot d$; $i=1,2,3$; v'_1 representing, in fact, the lines tangential to $(1/100)u^2$, touching this curve at $u=U$. The second stage is a selection circuit thus

approximating the required square function by three straight lines in a well known manner. In addition to v'_1 at terminal T_1; $i=1,2,3$; $-(1/100)v^2$ must be transferred and the required voltages at the input terminals to the second stage are therefore given by

$$e_1=(1/100)(2du-d^2-v^2)$$
$$e_2=(1/100)(6du-9d^2-v^2)$$
$$e_3=(1/100)(10du-25d^2-v^2$$

These signals are produced in the first stage of the multiplier, e_1, for example, is produced in a selection circuit comprising three input terminals fed with voltages v_{11}, v_{12}, v_{13}, respectively, one of which is selected in the selection circuit comprising diodes D_{11}, D_{12}, D_{13} which have a common anode connection at terminal T_1. Into T_1 positive current is injected through resistor R_1 which is connected to positive potential means at E+. This circuit for the production of e_1 transfers

$$(1/100)(2du-d^2)$$

from the input terminals to terminal T_1 simultaneously producing an approximation to $-(1/100)v^2$ from

$v'_{11}=(1/100)(-2vV+V^2)$, where $V=(2i-1)\cdot d$

$i=1,2,3$; these signals representing the lines tangential to $-(1/100)v^2$ touching this curve at $v=V$. The required input voltages are therefore

$$v_{11}=(1/100)(2du-d^2-2dv+d^2)$$
$$v_{12}=(1/100)(2du-d^2-6dv+9d^2)$$
$$v_{13}=(1/100)(2du-d^2-10dv+25d^2)$$

Expressing u and v in terms of x and y we have,

$$v_{11}=(2d/100)(x)=(1/12)x$$
$$v_{12}=(2d/100)(2x-y+4d=(1/12)(2x-y+16.7)$$
$$v_{13}=(2d/100)(3x-2y+12d)$$
$$=(1/12)(3x-2y+50)$$

The other input voltages are similarly given by

$$v_{21}=(1/12)(2x+y-16.7)$$
$$v_{22}=(1/12)(3x)$$
$$v_{23}=(1/12)(4x-y+33.4)$$
$$v_{31}=(1/12)(3x+2y-50)$$
$$v_{32}=(1/12)(4x+y-33.4)$$
$$v_{33}=(1/12)(5x)$$

The nine input voltages v_{ij}; $i,j=1,2,3$; are readily produced in linear resistive circuits from voltages x, y, $-y$, 50 volts and -50 volts. FIGURE 3 is a schematic diagram of circuits for the production of v_{11}, v_{12}, v_{13}. The other six input voltages can be produced in similar circuits. v_{11}, for example, is produced at terminal **6**, FIGURE 3, at a low impedance level. Terminal **6** is the cathode connection of cathode follower **5** whose grid connection is at terminal **4**. The voltage at terminal **4** was in one example equal to $v_{11}-1.8$ volt. This voltage is produced from voltage x and a voltage of -50 volt by a combining circuit comprising resistors **1**, **2**, **3**.

It is of interest to note that the voltages v_{ij} represent planes tangential to the surface corresponding to $e_0=(1/100)xy$ at the centres of the nine squares in FIGURE 2. The reason is as follows: In operation, the selection circuits of FIGURE 4 conductively connect output terminal T_0 with one and only one input terminal at any given instant. e_0 is then equal to the input voltage at the input terminal so selected. The circuit of FIGURE 4 can select only one of nine input voltages, each of which is a linear function of x and y. e_0 does therefore correspond to a piecewise-linear approximation to the required exact product function. The nine linear pieces which are produced are shown in FIGURE 2.

FIGURE 5 is a schematic diagram of another embodiment of this invention. It produces at output terminal **0** the voltage

$$e_0=(1/E)xy$$

where x and y are in volts and $E=25$ volts, provided that u and v are as defined above and u,v are between 0 and 25 volts. The second stage of the multiplier comprises input terminals **1, 2 3**, equal interpolating resistors r' connected in series with diodes D' which have a common cathode connection at output terminal **0** from which constant positive current of strength i' is withdrawn. The principle of operation of interpolating function generators as used in this stage is explained in said copending application. In this stage of the multiplier voltage $-(1/E)v^2$ is transferred from terminals **1, 2, 3** to terminal **0**. The second stage is operative as a half squarer for the production of $(1/E)u^2$ at **0** from suitable input voltages. The voltages at **1, 2 3** are

$$e_1=(1/E)(-v^2+2du-d^2)+i'r'$$
$$e_2=(1/E)(-v^2+10du-25d^2)+i'r'$$
$$e_3=(1/E)(-v^2+18du-81d^2)+i'r'$$

respectively. Thus, voltage $(1/E)(-v^2)+i'r'$, being equally applied to all input terminals of the second stage, is transferred, whereas voltages $(1/E)(2du-d^2)$, $(1/E)(10du-d^2)$, $(1/E)(18du-81d^2)$, produce at **0** a voltage corresponding to $(1/E)u^2-i'r'$. In this example $d=E/10=2.5$ volts, and the produced function $(1/E)u^2$ consists of an approximation curve comprising five linear segments.

A_1, A_2 A_3 are sign changers having a gain $A=-2$ each. They are fed from terminals T_1, T_2, T_3 which are at voltages e'_1, e'_2, e'_3, respectively, where

$$e'_1=(1/2E)(v^2-2du+d^2)-i'r'/2$$
$$e'_2=(1/2E)(v^2-10du+25d^2)-i'r'/2$$
$$e'_3=(1/2E)(v^2-18du+81d^2)-i'r'/2$$

e'_1 is produced in this example by a first stage comprising another interpolating function generator. Its input terminals **11, 12, 13** are fed with voltages e_{11}, e_{12}, e_{13}, respectively. Each input terminal is connected to an interpolating resistor of resistance r in series with diode D. These diodes have a common cathode connection at terminal T_1 from which positive current i is withdrawn. Voltage $(1/2E)(-2du+d^2)-i'r'/2+ir$ is simultaneously applied to all three input terminals and is thereby transferred to terminal T_1. Simultaneously the voltages $(1/2E)(2dv-d^2)$, $(1/2E)(10dv-25d^2)$, $(1/2E)(18dv-81d^2)$ are additively applied to terminals **11, 12, 13**, thereby producing an approximation to $(1/2E)v^2-ir$ volt at terminal T_1. The total voltage produced at terminal T_1 is therefore equal to $(1/2E)(-2du+d^2)-i'r'/2+ir+(1/2E)v^2-ir$ which is equal to e'_1, as required. The input voltages e_{11}, e_{12}, e_{13} at terminals **11, 12, 13**, respectively, are thus equal to

$$e_{11}=(1/2E)(-2du+d^2+2dv-d^2)+ir-i'r'/2$$
$$e_{12}=(1/1E)(-2du+d^2+10dv-25d^2)+ir-i'r'/2$$
$$e_{13}=(1/2E)(-2du+d^2+18dv-81d^2)+ir-i'r'/2$$

In this example $ir=i'r'/2=1$ volt and therefore, expressing u,v in terms of x and y,

$$e_{11}=(d/E)(-x)=(1/10)(-x) \text{ volt}$$
$$e_{12}=(d/E)(-3x+2y-12d)$$
$$=(1/10)(-3x+2y-30) \text{ volt}$$
$$e_{13}=(d/E)(-5x+4y-40d)$$
$$=(1/10)(-5x+4y-100) \text{ volt}$$

Voltages e'_2, e'_3 are produced in similar interpolating function generating circuits from input voltages

$$e_{11}=(d/E)(-x)=(1/10)(-x) \text{ volt}$$
$$e_{22}=(1/10)(-5x)$$
$$e_{23}=(1/10)(-7x+2y-70)$$
$$e_{31}=(1/10)(-5x-4y+100)$$
$$e_{32}=(1/10)(-7x-2y+70)$$
$$e_{33}=(1/10)(-9x)$$

at terminals **21 22, 23, 31, 32, 33**, respectively. Any ine of the nine input voltages e_{ij}; $i,j=1, 2, 3$; is readily produced from x, y and constant voltages in circuits similar to those corresponding to FIGURE 3.

In one example of the multiplier of FIGURE 5, $i=i'=1$ ma.; $r=1$ kilohm; $r'=2$ kilohms. Aplifiers A_1, A_2, A_3 draw negligible current from their input terminals and have a low output impedance. Output terminal **0** must not be substantially loaded, a condition which can be achieved by connecting an adder having a high input resistance to terminal **0** and connecting any load to the output terminal thereof. These conditions ensure that substantially all currents i, $-i'$ supplied by the current generators supplying currents i and $-i'$ flow into the diodes adjacent to said common connections.

A still further embodiment of the invention will be described in connection with FIGURE 6 which is a schematic diagram of a multiplier producing at output terminal **0** the voltage $e_0=(1/E)xy$ where $E=56$ volts provided that u, v are between **0** and **25** volts. u and v are as defined above and voltage d is $25/6=4.17$ volts, in this example. The operation of this circuit is best understood by following output signal formation from output terminal **0** to the input terminals of the multiplier. **41** is a triode connected as a cathode follower and producing the voltage e_0 at terminal **0** at a low impedance level without loading its input terminal T_0. **36, 37** are the anode and cathode resistors of said triode connected to positive and negative voltage means at +B and —, respectively. The voltage at terminal T_0 is denoted by e'_0. It is equal in this example to

$$e'_0=(1/E')xy-1.8 \text{ volts}$$

where $E'=55$ volts. The second stage of the multiplier comprises terminals **1** and **2**, two resistive interpolating branches connected to terminals **1, 2**, respectively, and having a common output connection at terminal T_0, each of said branches comprising a series combination of a linear resistor and a diode D, the resistance of the combination being denoted by r'. The polarity of the diodes is such that their cathodes are connected to terminal T_0. Constant negative current in supplied to terminal T_0 by triode **40** whose anode is connected to said terminal. **35** is the cathode resistor of said triode and the series combination of resistors **32, 33, 34** provides the required grid voltage to triode **40**. For this purpose the grid of triode **40** is connected to the adjustable contact of resistor **33**. Resistor **32** is connected to ground and resistors **34** and **35** are connected to negative potential means at —. Said adjustable contact permits adjustment of the current supplied by said triode. Denoting the current thus supplied by i', which is a negative quantity in this example, the voltages e_1 and e_2 at terminals **1, 2**, respectively, are given by

$$e_1=(1/E')(2ud-d^2-v^2)-1.8-i'r'$$
$$e_2=(1/E')(10ud-25d^2-v^2)-1.8-i'r'$$

Thereby, voltage $(1/E')(-v^2)-1.8-i'r'$ is transferred to terminal T_0 whereas voltages $(1/E')(2ud-d^2)$ and $(1/E')(10ud-25d^2)$ produce thereat an approximation to $(1/E')u^2+i'r'$. Thus the total voltage produced at terminal T_0 is approximately equal to e'_0, as required.

38 and **39** are triodes connected as cathode followers and substantially transferring the voltages at terminals T_1, T_2 to terminals **1, 2**, respectively. Considering the gain of the cathode followers and their bias voltages the voltages e'_1 and e'_2 at terminals T_1 and T_2 are, respectively,

$$e'_1=(1/E'')(2ud-d^2-v^2)-3.6-i'r'$$
$$e'_2=(1/E'')(100d-25d^2-v^2)-3.6-i'r'$$

where $E''=54$ volts.

e'_1, e'_2 are produced in the first stage of the multiplier from voltages x, y, $-y$, V, and $-V$. Considering, for example, production of E'_1, this is produced in a transferring interpolating function generator comprising first and second input terminals fed with voltages e_{11}, e_{12}, respectively, two similar interpolating resistive branches connected to said terminals each having resistance r and comprising a diode D, where said diodes have a common anode connection at terminal T_1, substantially constant

positive current i being applied to said common connection through resistor R_1 connected to constant potential means at +. Taking $ir=-i'r'$, the expressions for e_{11}, e_{12} are

$$e_{11}=(1/E'')(2ud-d^2-2vd+d^2)-3.60$$
$$e_{12}=(1/E'')(2ud-d^2-10vd+25d^2)-3.60$$

or, in terms of x and y,

$$e_{11}=(2d/E'')x-3.60$$
$$e_{12}=(2d/E'')(3x-2y+12d)-3.60$$

Voltage $(1/E'')(2ud-d^2)-3.60$, being equally applied to both input terminals, is transferred to terminal T_1 while voltages $(1/E'')(-2vd+d^2)$ and

$$1/E'')(-10vd+25d^2)$$

produce thereat an approximation to

$$(1/E'')v^2+ir=(1/E'')v^2-i'r'$$

The total voltage thus produced at terminal T_1 is equal to e'_1, as required.

A similar first stage function generator produces voltage e'_2 at terminal T_2 from e_{21} and e_{22} as input voltages, where

$$e_{21}=(2d/E'')(3x+2y-12d)-3.60$$
$$e_{22}=(2d/E'')(5x)-3.60$$

In FIGURE 6 the circuit comprising resistors **11** through **14**, fed by voltages x and $-V$ and connected to terminal T_{11} which is the cathode connection of diode D, is equivalent to a resistor of resistance r fed by voltage e_{11} and connected to terminal T_{11}. Thus the resistance seen from T_{11} looking into said resistors, when the input terminals are connected to ground, is equal to r, and the resistors are so chosen that the required linear combination of x and a constant voltage as given in the expression for e_{11} is produced at T_{11}. Production of e_{12}, e_{21}, e_{22} at terminals T_{12}, T_{21}, T_{22} proceeds in a similar manner.

In the above examples, $r=15.0$ kilohms; $i'=0.168$ ma.; $r=15.5$ kilohms; $R_1=1.83$ megohms; $R_2=1.79$ megohms; voltage at +B, 200 volts; voltage at —, —300 volts; voltage at +, +300 volts; voltage $V=50$ volts. Resistors **12**, **17**, **22**, **25** are adjustable and **33** is a potentiometer. Resistance values, in kilohm, are listed below:

11, 100; **12**, 100 (max.); **13**, 150; **14**, 20.0; **15**, 33.3; **16**, 50.0; **17**, 100 (max.); **18**, 150; **19**, 105; **20**, 33.3; **21**, 50.0; **22**, 50 (max.); **23**, 50; **24**, 20.0; **25**, 100 (max.); **26**, 150; **27**, 100; **28**, 0.51; **29**, 41; **30**, 0.51; **31**, 41; **32**, 100; **33**, 50; **34**, 200; **35**, 1200; **36**, 0.51; **37**, 41. All triodes of type 12AT7.

The adjustment of the multiplier proceeds as follows:

(1) Adjust potentiometer **33** for an anode current of 0.168 ma. in triode **40**;
(2) With $x=0.00$ volt and $y=8$ volts, adjust resistor **12** for $e_0=0.00$ volt;
(3) With $x=0.00$ volt and $y=43$ volts, adjust resistor **25** for $e_0=0.00$ volt;
(4) With $x=-16.7$ volts and $y=25.0$ volts adjust resistor 17 for $e_0=-7.45$ volts;
(5) With $x=16.7$ volts and $y=25.0$ volts adjust resistor **21** for $e_0=7.45$ volts.

While the above examples of multipliers comprise impedance converting means between the first and second stages thereof, this is by no means an essential feature of the invention as will now be shown in connection with FIGURE 7 which is a schematic diagram of a direct coupled embodiment of the invention. The multiplier corresponding to FIGURE 7 produces at output terminal **0** the voltage $e_0=(1/E)xy$ where $E=58.7$ volts. For the purpose it uses first and second stages each comprising transferring function generators embodying resistive interpolation. **90** is a cathode follower substantially transferring the voltage at grid terminal T to output terminal T_0, which is also designated **0**. **87**, **88** are the anode and cathode resistors of triode **90**, respectively. **89** is a triode having its anode connected to terminal T withdrawing therefrom a constant positive current i'. **83** through **85** are resistors supplying the required grid voltage to triode **89** and **86** is its cathode resistor. Said triode operates as a constant current source in a well-known manner. Adjustment of potentiometer **84** permits adjustment of current strength i'.

The voltage at terminal T is equal to

$$e'_0=(1/E')xy-1.8 \text{ volts}$$

where $E'=57.5$ volts, provided that u, v which are as defined above, are confined to the interval of 0 to 25 volts. The second stage of the multiplier comprises terminals **1**, **2**, **3** and three series combinations of diodes D and linear interpolating resistors of resistance r' each, where $r'=10.0$ kilohms. Said diodes have their anodes connected to respective input terminals of said second stage, while said interpolating resistors have a common connection at T. The voltages at terminals **1**, **2**, **3**, are, respectively,

$$e_1=(1/E')(-v^2+2du-d^2)-1.8+i'r'$$
$$e_2=(1/E')(-v^2+10du-25d^2)-1.8+i'r'$$
$$e_3(1/E')(-v^2+18du-81d^2)-1.8+i'r'$$

where, in this example, $i'=0.094$ ma. and $r'=10.0$ kilohms. The production of voltage e'_0 at terminal T will be quite clear from the previous examples. Voltages e_1, e_2, e_3 are produced in similar resistive interpolating function generators from voltages x, y, $-y$, V and $-V$, received by a plurality of input terminals. All interpolating resistances in said first stage are equal to $r=2.61$ kilohms. In general, in a direct coupled multiplier the interpolating resistance of the second stage must be made several times as much as that of the first stage in order not to introduce large errors into the produced output function. The reason is that the second stage withdraws variable current from the output terminals of the first stage and this current must therefore be not more than a fraction of the current i flowing into the first stage. In this example $ir=i'r'$, and a ratio r'/r of 4, approximately, therefore corresponds to a ratio of i/i' which is equally about 4. Such a ratio of current yields sufficiently accurate performance. The computation of the resistive input networks proceeds in a manner similar to that explained in connection with FIGURE 6.

In one example the following components and values are used:

89, **90** double triode type 12AT7

Voltage at +B, 200 volts, voltage at +, 300 volts; voltage at —, —300 volts. $V=50$ volts. Resistances as listed below, where row A is the resistor and B is the corresponding resistance in kilohms.

A	51	52	53	54	55	56	57	58	59	60	61	62
B	30.0	61.5	3.00	10.00	15.0	266	4.72	6.00	7.50	19.8	30.8	10.0

A	63	64	65	66	67	68	69	70	71	72	73	74	75
B	15.0	27.6	5.55	6.00	61.5	5.00	4.28	15.0	31.2	19.2	6.00	7.50	12.0

A	76	77	78	79	80	81	82	83	84	85	86	87	88
B	4.28	15.0	15.5	52.5	3.33	61.5	15.0	100	50	200	2000	10	40

The following resistors are adjustable: **56, 60, 67, 71, 75, 78, 81.** The above table lists values corresponding to one adjustment of these resistors. **84** is a potentiometer.

The procedure of adjustment of the multiplier is as follows: Column A in the following table lists the component which is to be adjusted. Columns x and y list the values of x and y required during the adjustment. Column e_0 lists the required value of output voltage which must be obtained by adjustment of the corresponding component in column A.

A	x	y	e_0
84	0.00	5	0.00
56	−10.0	15.0	−2.55
60	−20.0	25.0	−8.52
64	10.0	15.0	2.55
67	0.00	25	0.00
71	−10.0	35.0	−5.96
75	20.0	25.0	8.52
78	10.0	35.0	5.96
81	0.00	45	9.00

While the above examples of the invention are operative in the quadrant of the plane of variables defined by the given limitations on u and v, this limitation is by no means inherent in the invention and is to be taken purely as an illustration. Similar embodiments are operative as four quadrant multipliers, for example. Moreover, it will be appreciated that the use of linear interpolating resistors in the examples is given by way of illustration and example. In any of the above embodiments the linear interpolating resistors can be replaced by suitable nonlinear resistors, resulting in a further increase of accuracy, as described in said copending application.

As a further example of the invention the multiplier corresponding to the schematic diagram of FIGURE 8 will now be described. This multiplier provides four quadrant multiplication within the shaded area of the plane of variables shown in the plot of FIGURE 8A and limited by $x,y=\pm 5$ volts.

The second stage of the multiplier has input terminals **1** and **2** and output terminal **0** whereat the voltage

$$e_0=(1/10)xy$$

is produced at a low impedance level. This second stage comprises a nonlinear interpolating squarer which, when fed at **1** and **2** with voltages u and $-u$ produces an output voltage $(1/10)u^2-7.5$ volts in accordance with said copending application. Two similar nonlinear interpolating resistors each of resistance r when traversed by current i, where i is the positive current withdrawn from their common connection at terminal T_0 by transistor **106**, are connected to terminals **1** and **2**, respectively. In this example said nonlinear resistors comprise series combinations of fixed nonlinear resistors and adjustable linear resistors. NPN transistor **106** is used as a constant current source in a standard connection. Zener diode **105** fixes the base potential of said transistor. Emitter resistor **109** is adjustable, permitting adjustment of said current i, whereas resistor **108** is a temperature dependent resistor having a negative temperature coefficient. With increasing temperature, the resistance of resistor **108** decreases and current i therefore increases. This increase in current compensates for temperature drift in the squarer. In particular, resistance r decreases when temperature increases thereby raising the potential of terminal T_0. An increase in i, on the other hand, lowers the potential at terminal T_0. The use of a suitable temperature dependent resistor at **108** thus permits compensation of the two opposing effects. **107** is a PNP transistor used as an emitter follower for the provision of the output signal at **0** at a low impedance level without substantially loading terminal T_0.

The voltages at terminals **1** and **2** are in this example

$$e_1=-(1/10)v^2+7.5+u$$
$$e_2=-(1/10)v^2+7.5-u$$

where u and v are again as defined above. Voltage $-(1/10)v^2+7.5$ is thereby transferred to terminal **0** while u and $-u$ produce thereat the voltage $(1/10)u^2-7.5$. The total output voltage at terminal **0** is therefore equal to e_0, as required.

e_1 and e_2 are produced in similar interpolating function generators, in the first stage of the multiplier. Thus the device having input terminals **11** and **12** is a squarer producing at terminal **1** the voltage $-(1/10)v^2+7.5$ volts when terminals **11** and **12** are at potentials v and $-v$, respectively. This first stage squarer comprises interpolating resistors r connected to terminals **11** and **12** having a common output connection at T_1, PNP transistor **104** operating as a constant current source its base potential being fixed by Zener diode **101** and its current being adjustable by resistor **103**. Resistor **102** is a negative temperature coefficient resistor for the compensation of temperature drift. PNP transistor **104** functions as an impedance converter, in an emitter follower connection. Positive current i is supplied to terminal T_1 by transistor **100**. The voltages at **11** and **12** are, respectively,

$$e_{11}=u+v=x$$
$$e_{12}=u-v=y$$

Voltage u is thereby transferred to terminal **1** whereas voltages v and $-v$ produce thereat the voltage

$$-(1/10)v^2+7.5$$

The total voltage produced at terminal **1** is thus equal to e_1, as required.

A similar squarer produces at terminal **2** the voltage e_2 from input voltages

$$e_{21}=-u-v=-y$$
$$e_{22}=-u+v=-x$$

at terminals **21** and **22**, respectively.

This example of a multiplier of the invention thus requires voltages x, $-x$, y, and $-y$ as input signals. Any one of the nonlinear resistors has a characteristic given by

$$V=60\cdot I^{0.33}$$

where V is the voltage drop in volts and I is the current in amperes. The adjustable resistors in series with said nonlinear resistors have a maximum resistance of 2 kilohms. In each of the two first stage squarers the current supplied to the common connection of the input branches is equal to 0.9 ma., approximately, and the current supplied to the common connection T_0 of the two interpolating branches of the second stage squarer is equal to −0.9 ma., approximately.

A block diagram of the multiplier of FIGURE 8 is given in FIGURE 9 in which each first stage squarer is identified by A and said second stage squarer is identified by B.

FIGURE 10 is a block diagram of another four quadrant multiplier of the invention which requires only signals x and y as input signals and comprises only two B units, one A unit and one sign changer. The signal at **1** is produced as before. The first stage B unit is connected to terminals **11** and **12** and thus receives input signals x and y and produces therefrom at its output terminal **2'** the voltage $(1/10)v^2-7.5+u=-e_2$. Sign changer SC accepts the signal at terminal **2'** and produces therefrom at its output terminal **2** the voltage e_2. Second stage squarer B produces from e_1 and e_2 at terminals **1** and **2**, respectively, the required output signal at terminal **0**, as before.

FIGURE 11 is a block diagram of a multiplier in which the first stage comprises only one squarer, FG_1, for the

production of one of the input voltages of the second stage, e_1 in this example, while all other second stages input voltages, e_2, e_3, . . . , are produced from e_1, x, and y in the linear network N. In any one of the examples of multipliers of the invention recited above, the difference of any two signals e_1, e_2, . . . , which are input signals to the second stage, is a linear function of x and y. Thus, having produced one of said signals, all the other said signals are readily produced in a linear network. Such a multiplier will be called "bilinear."

A specific example of a bilinear multiplier of the invention will be described in connection with FIGURE 12 which is a schematic diagram thereof. Input voltages x and y are accepted by input terminals **11** and **12**, respectively, of a first stage squarer producing therefrom at terminal **1** the voltage

$$e_1=-(1/E)v^2+E'$$

where E and E' are constant voltages and u, v are as defined above. Sign changing adder **115** is fed with voltages x and y and produces at its output terminal **114** the voltage $-(x+y)$. **110** and **111** are equal resistors connected between terminals **1** and **114** and produced at their common connection at terminal **2'** the voltage

$$e_1/2-(x+y)/2=e'_2$$

Resistors **112** and **113** have equal resistance and serve as a potential dividing network producing at terminal **1'** the voltage $e_1/2=e'_1$. Expressing e'_2 in terms of u and v we have,

$$e'_2=-(1/2E)v^2-u/2+E'/2$$

while

$$e'_1=-(1/2Ev^2)+u/2+E'/2$$

A second stage transfers $-(1/2E)v^2+E'/2$ to output terminal **0** and produces from $u/2$ and $-u/2$ the additive output voltage $(1/2E)u^2-E'/2$, thus yielding a total output voltage equal to

$$e_0=(1/2E)(u^2-v^2)=(1/2E)xy$$

The examples of FIGURES 8 through 12 relate to function generators in which the second stage comprises only two interpolating branches. This is given by way of example and illustration only. Any plurality of such branches can be used in the invention. Similarly, the first stage may comprise more than two interpolating branches.

If greater accuracy is required in a multiplier of the invention than can be achieved with two interpolating branches it is necessary to use three or more thereof. As an example for the use of three branches in the second stage of the multiplier of FIGURE 8, the embodiment including the device of FIGURE 13A will be described. This is a scrap schematic diagram of the structure required to replace the input circuit, between terminals **1**, **2** and terminal T_0 in FIGURE 8. There are now three input terminals, **1**, **2**, **3**, each connected to terminal T_0 through the series combination of a nonlinear resistor of resistance r and diodes **116**, **117**, **118**, respectively. The cathodes of said diodes have a common connection at T_0. The current source connected to T_0 as well as the output impedance converting stage are as in FIGURE 8. The characteristics of r are likewise identical with those in the example of FIGURE 8. Diode **117** is optional.

If terminals **1**, **2**, **3** are fed with voltages $-u$, 10 volts, $+u$, respectively, the produced output voltage at terminal **0** is equal to $(1/10)u^2$ for u between -20 and $+20$ volts. In this example of the mutiplier the following voltages are received by terminals **1**, **2**, **3**:

$$e_1=-(1/10)v^2-u$$
$$e_2=-(1/10)v^2+10$$
$$e_3=-(1/10)v^2+u$$

and the output voltage $e_0=(1/10)xy$ is thereby produced at output terminal **0**, provided that x and y are between -10 and $+10$ volts.

The voltages e_1, e_2, e_3 are produced in a first stage of the multiplier and it will be quite clear from the above examples how this can be done in the invention.

The circuit corresponding to FIGURE 13A can be replaced by that of FIGURE 13B which, in operation, is completely equivalent to it. Diodes **114** and **115** accept voltages e_1 and e_3, respectively, and select at terminal **1'** the larger thereof. The diodes have a common cathode connection at terminal **1'** to which a negative current is supplied through a resistor connected to negative potential means at —. We have, therefore at terminals **1'** and **2**

$$e'_1=-(1/10)v^2+|u|$$
$$e_2=-(1/10)v^2+10$$

respectively. Input voltage $|u|$ and 10 volts produce in the half squarer which they feed the voltage $(1/10)u^2$, the additional voltage $-(1/10)v^2$ being simultaneously transferred to the output terminal, so that, again, the voltage at terminal **0** is equal to $(1/10)xy$.

Although this invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of this invention being limited only by the terms of the appended claims.

What I claim is:

1. An electronic analog multiplier for producing an output signal having a magnitude substantially proportional to the product of the magnitudes of first and second input signals, comprising a plurality of first means for receiving said first and second input signals, second means responsive to said input signals for generating therefrom a plurality of third signals substantially equal to respective ones of a plurality of linear functions of the sum of said input signals and the square of their difference; a plurality of third means responsive to respective ones of said third signals and having a common output connection, for producing thereat a fourth signal substantially equal to a linear function of said square signal and the square of the sum of said input signals, said fourth signal being said output signal; wherein said third means comprise unilaterally conductive means, fourth means connected to said common connection for supplying a current to at least one of said conductive means at any given instant.

2. The multiplier as recited in claim **1**, wherein said third means include interpolating resistor means having resistive values to cause at least two of them to conduct simultaneously for suitable values of said input signals.

3. The multiplier as recited in claim **2**, wherein said fourth means is adapted to cause the magnitude of the current flowing through said common connection into said plurality of third means to be substantially independent of the magnitudes of said input signals.

4. The multiplier as recited in claim **3**, wherein said fourth means includes means responsive to temperature for causing the current supplied by said fourth means to be temperature dependent for the compensation of temperature drift.

5. An electronic analog multiplier for producing an output signal having a magnitude substantially proportional to the product of the magnitudes of first and second input signals, comprising a plurality of first means for receiving said first and second input signals, second means responsive to said input signals for generating therefrom a plurality of third signals substantially equal to respective ones of a plurality of linear functions of the sum of said input signals and the square of their difference; a plurality of third means responsive to respective ones of said third signals and having a common out-

put connection, for producing thereat a fourth signal substantially equal to a linear function of said square signal and the square of the sum of said input signals, said fourth signal being said output signal; wherein said third means comprise bilaterally conductive nonlinear interpolating means, fourth means connected to said common connection for supplying a current to at least one of said conductive means at any given instant, said third means having resistive values to cause at least two of them to conduct simultaneously for suitable values of said input signals.

6. The multiplier as recited in claim 5, wherein said fourth means is adapted to cause the magnitude of the current flowing through said common connection into said plurality of third means to be substantially independent of the magnitudes of said input signals.

7. The multiplier as recited in claim 6, wherein said fourth means includes means responsive to temperature for causing the current supplied by said fourth means to be temperature dependent for the compensation of temperature drift.

8. An electronic analog multiplier for producing an output signal having a magnitude substantially proportional to the product to the magnitudes of first and second input signals, comprising a plurality of first means for receiving said first and second input signals, second means responsive to said input signals for generating therefrom a plurality of third signals substantially equal to respective ones of a plurality of linear functions of the sum of said input signals and the square of their difference; a plurality of third means responsive to respective ones of said third signals and having a common output connection, for producing thereat a fourth signal substantially equal to a linear function of said square signal and the square of the sum of said input signals, said fourth signal being said output signal; wherein said second means includes a plurality of unilaterally conductive means responsive to said input signals having a common output connection for producing thereat one of said third signals; fifth means connected to said common connection for supplying a current to at least one of said conductive means at any given instant.

9. The multiplier as recited in claim 8, wherein said conductive means include interpolating resistor means having resistive values to cause at least two of them to conduct simultaneously for suitable values of said input signals.

10. A bilinear multiplier comprising the device as recited in claim 8, wherein said second means includes linear means responsive to said third signal and to said input signals for the production of at least one other signal of said plurality of third signals.

11. A fourth quadrant multiplier comprising the device as recited in claim 8, wherein said second means comprises a second plurality of unilaterally conductive means having a common output connection, for producing thereat a signal having a magnitude substantially equal to the inverse of the magnitude of a second of said third signals; sign changing means connected thereto for inverting the sign of said inverse signal.

12. An electronic analog multiplier for producing an output signal having a magnitude substantially proportional to the product of the magnitudes of first and second input signals, comprising a plurality of first means for receiving said first and second input signals, second means responsive to said input signals for generating therefrom a plurality of third signals substantially equal to respective ones of a plurality of linear functions of the sum of said input signals and the square of their difference; a plurality of third means responsive to respective ones of said third signals and having a common output connection, for producing thereat a fourth signal substantially equal to a linear function of said square signal and the square of the sum of said input signals, said fourth signal being said output signal; wherein said second means includes first and second pluralities of unilaterally conductive means responsive to said input signals each having a common output connection for producing thereat respective third signals; first and second fifth means connected to respective ones of said output connections each for supplying a current to at least one conductive means of said respective plurality of conductive means at any given instant.

13. A four quadrant multiplier comprising the device as recited in claim 12; first and second sixth means for receiving first and second inverse input signals having magnitudes substantially equal to the negative of the magnitudes of said first and second input signals, respectively; wherein said first and second pluralities of unilateral means are connected to respective ones of said first and second first and sixth means respectively.

14. An electronic analog multiplier for producing an output signal having a magnitude substantially proportional to the product of the magnitudes of first and second input signals, comprising a plurality of first means for receiving said first and second input signals, second means responsive to said input signals for generating therefrom a plurality of third signals substantially equal to respective ones of a plurality of linear functions of the sum of said input signals and the square of their difference; a plurality of third means responsive to respective ones of said third signals and having a common output connection, for producing thereat a fourth signal substantially equal to a linear function of said square signal and the square of the sum of said input signals, said fourth signal being said output signal; wherein said second means comprises a plurality of bilaterally conductive nonlinear interpolating means responsive to said input signals having a common output connection for producing thereat one of said third signals; fifth means connected to said common connection for supplying a current to at least one of said conductive means at any given instant; said conductive means having resistive values to cause at least two of them to conduct simultaneously for suitable values of said input signals.

15. A bilinear multiplier comprising the device as recited in claim 14, wherein said second means includes linear means responsive to said third signal and to said input signals for the production of at least one other signal of said plurality of third signals.

16. A four quadrant multiplier comprising the device as recited in claim 14, wherein said second means comprises a second plurality of bilaterally conductive nonlinear means having a common output connection, for producing thereat a signal having a magnitude substantially equal to the inverse of the magnitude of a second of said third signals; sign changing means connected thereto for inverting the sign of said inverse signal.

17. An electronic analog multiplier for producing an output signal having a magnitude substantially proportional to the product of the magnitudes of first and second input signals, comprising a plurality of first means for receiving said first and second input signals, second means responsive to said input signals for generating therefrom a plurality of third signals substantially equal to respective ones of a plurality of linear functions of the sum of said input signals and the square of their difference; a plurality of third means responsive to respective ones of said third signals and having a common output connection, for producing thereat a fourth signal substantially equal to a linear function of said square signal and the square of the sum of said input signals, said fourth signal being said output signal; wherein said second means includes first and second pluralities of bilaterally conductive nonlinear interpolating means responsive to said input signals each having a common output connection for producing thereat respective third signals, first and second fifth means connected to respective ones

of said output connections each for supplying a current to at least one conductive means of said respective plurality of conductive means at any given instant.

18. A four quadrant multiplier comprising the device as recited in claim **17**; first and second sixth means for receiving first and second inverse input signals having magnitudes substantially equal to the negative of the magnitudes of said first and second input signals, respectively; wherein said first and second pluralities of conductive means are connected to respective ones of said first and second first and sixth means respectively.

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MALCOLM A. MORRISON, *Primary Examiner.*

K. W. DOBYNS, *Assistant Examiner.*