(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 254 511**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **87306394.5**

(22) Date of filing: **20.07.87**

(51) Int. Cl.4: **G11B 15/18** , G11B 15/467 , //G11B5/008

(30) Priority: **22.07.86 JP 172029/86**
29.08.86 JP 204084/86

(43) Date of publication of application:
27.01.88 Bulletin 88/04

(84) Designated Contracting States:
DE FR GB NL

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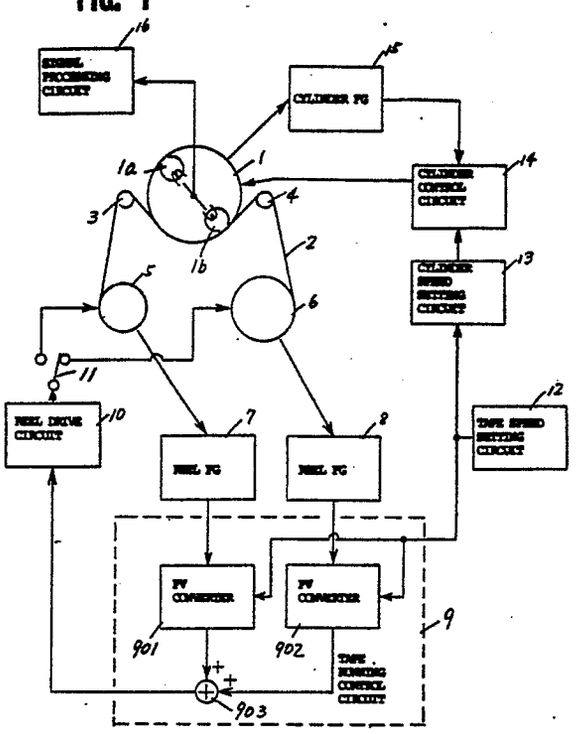
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(54) Apparatus for reproducing signals recorded on a tape.

(57) Disclosed herein is an apparatus for reproducing signals recorded in slanting tracks on a recording tape including a tape position information recorded at a specified area on each track. The apparatus has a tape speed setting circuit capable of setting a plurality of tape speeds, and a cylinder speed setting circuit for setting such a rotational speed of a rotary cylinder that the track direction speed component of a reproducing head mounted on the rotary cylinder is kept constant. A tape running control circuit controls a reel drive circuit so that the tape runs at a speed set by the tape speed setting circuit. A cylinder control circuit controls the rotary cylinder so that the rotary cylinder rotates at a speed set by the cylinder speed setting circuit. In a transition state from a normal reproduction mode to a high speed search mode, the tape speed setting circuit changes the tape speed in step-wise so that the deviation of the track direction speed component of the head in each step of tape speed change is within a range in which the tape position information is correctly read.

FIG. 1



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Apparatus for reproducing signals recorded on a tape

1. Field of the Invention

This invention relates to an apparatus such as a video tape recorder ("VTR" hereinafter) and a digital audio tape recorder ("DATA") for reproducing information by recorded in slanting tracks on a recording tape such as a magnetic tape.

2. Description of the Prior Art

It is important for a DAT or VTR which can record and play 2 to 8 hours of programs such as musics and moving pictures to search a recorded position of desired program quickly.

An Example of search of position on a tape at high speed ("high speed search") hereinafter) for DAT is shown in "SERVO TECHNOLOGY OF R-DAT" by Akihiko Hitomi, et al (IEEE Transactions on Consumer Electronics, vol. CE-32, No. 3, August 1986, PP430-431). In the example described in this report, when the tape speed is made 200 times faster than that in normal reproduction, the speed of the rotary cylinder on which a head is mounted is made 3025 r.p.m. in the fast forward ("FF") direction and 994 r.p.m. in the rewind ("REW") direction. This allows the speed component in the track direction of the reproduction head to be equal to that in the normal reproduction so that the head can read a tape position information recorded on a track.

By this method, however, it is not assured that the increase of the tape speed coincides with the increase of the rotary cylinder speed in the transition stage when the tape speed is accelerated from the stop state to the speed 200 times faster than the normal reproduction speed. Therefore, the track direction speed component of the head would become different from that in the normal reproduction in the transition stage, so that there would be the possibility that the tape position information could not be read.

SUMMARY OF THE INVENTION

An object of this invention is to provide a tape reproduction apparatus which enables reliable high-speed search without failure for reading tape position information recorded on the track even in the above-described transition stage.

In order to attain the above object, the tape reproducing apparatus according to this invention uses a recording tape on which information signals are recorded in slanting tracks and a positional information is recorded at a specified position on each track, and comprises:

a rotary cylinder on which a head and a cylinder speed director is mounted;

cylinder control means for controlling the rotary cylinder rotation according to an output of the cylinder speed detector;

two reels on which the tape is wound;

two reel rotation detectors for detecting rotational speeds of the two reels, respectively;

tape driving means for driving either one of the two reels to run the tape;

tape running control means for controlling the tape driving means according to outputs of the two reel rotation detectors;

tape speed setting means for setting a plurality of kinds of speeds for the tape running control means;

cylinder speed setting means for setting a cylinder rotational speed for the cylinder control means to maintain constant a track direction speed component of the head according to tape speed; and

a signal processing circuit for reading the positional information recorded on the tape.

The apparatus controls the tape to run at a plurality of speeds and the rotary cylinder to rotate to maintain the track direction speed component of the head. For example, the tape speed is increased in step-wise like 1 fold, 25 fold, 50 fold, ---up to 200 fold faster than the normal speed, and the rotary cylinder speed follows to increase in step-wise. Resultantly, the track direction speed component of the head will not deviate so significantly from that in normal reproduction mode, so that reliable search free from failure can be realized.

Further, the tape running speed is controlled according to the outputs of the two reel rotation detectors to eliminate errors in the tape running even when a dropout occurs in the reading by the head. In this case, the tape running speed may vary depending on the tape length, etc. To avoid such variation, it is preferable to detect the relative speed of the tape to the track by using an output signal of a PLL circuit in the signal processing circuit synchronized with a head reading signal, and correct the tape speed set for the tape running control means to a correct target value. With this arrangement, the position information reading accuracy is further enhanced.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a first embodiment according to this invention,

Fig. 2 is a diagram of an example of recorded track pattern on a magnetic tape used for an apparatus according to this invention,

Fig. 3 is a diagram showing an operation of the head in the first embodiment according to this invention

Figs. 4, 5 and 6 are explanatory operational diagrams of the embodiment of Fig. 1,

Fig. 7 is a block diagram of an example of PV converter in the first embodiment according to this invention,

Fig. 8 is an operational waveform diagram of Fig. 7,

Fig. 9 is a block diagram of an example of cylinder speed setting circuit and cylinder control circuit in the first embodiment according to this invention.

Fig. 10 is a block diagram of a second embodiment according to this invention,

Fig. 11 is an explanatory operating diagram of the embodiment of Fig. 10.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a block diagram showing a magnetic tape reproducing apparatus as an embodiment of this invention. In this figure, denoted by numeral 1 is a rotary cylinder, 1a and 1b are heads, 2 is a magnetic tape, 3 and 4 are posts forming a running path of the tape, 5 and 6 are reels, 7 and 8 are reel frequency generators (reel FG) to detect the rotational speeds of the reels 5 and 6, respectively, 9 is a tape running control circuit comprising period/voltage converters ("PV converter" hereinafter) 901 and 902 and an adder 903, 10 is a reel drive circuit, 11 is a switch to change over the driven reel, 12 is a tape speed setting circuit, 13 is a cylinder speed setting circuit, 14 is a cylinder control circuit, 25 is a cylinder FG acting as a cylinder speed detector, and 16 is a signal processing circuit for processing a read-out signal from the heads.

The embodiment in Fig. 1 arranged as described above functions as follows.

The tape speed setting circuit 12 actually comprises a microcomputer or the like and sets an operating point of the cylinder control circuit 14 through the cylinder speed setting circuit 13 and operating points of the PV converters 901 and 902. The tape speed setting circuit 12 can change these operating points to various conditions. The cylinder control circuit 14 causes the cylinder 1 rotate at a constant speed using the output of the cylinder FG 15 and based on the operating point which has been set up. That is, the rotating speed of the cylinder 1 can be changed to various speeds according to the operating point set by the tape speed setting circuit 12.

The frequency of the output signal of the cylinder FG 15 corresponds to the rotational speed of the rotary cylinder 1. Or, the period of the output signal of the cylinder FG 15 corresponds to the cycle of the rotation of the rotary cylinder 1 and thus is proportional to the reciprocal value of the rotational speed. The periods of the output signals of the reel FGs 7 and 8 correspond to the rotational cycles of the reels 5 and 6, respectively, and thus are proportional to the reciprocal values of the rotational speeds of the reels 5 and 6, respectively. The running speed of the tape 2 can be represented by the reciprocal value of the sum of the periods of the output signals of the reel FGs 7 and 8. Therefore, to keep constant the sum of the periods of the two reel FG output signals means to keep constant the tape running speed.

The rotating speeds of the reel 5 and 6 are detected by the reel FGs 7 and 8 and the frequencies of their output signals are respectively converted to voltage signals by the PV converters 901 and 902. The voltage outputs of the PV converters 901 and 902 are added by the adder 903 and the added signal is applied to the reel drive circuit 10. The drive circuit 10 drives either the reel 5 or 6 selected by the switch 11 to run the tape 2. This reel control system can maintain the sum of the periods of the periodic output signals from the reel FGs 7 and 8 constant to run the tape at a constant speed. Here, since the operating points of the PV converters 901 and 902 can be changed by the tape speed setting circuit 12, the tape speed can be changed to various speeds by the tape speed setting circuit 12.

The rotational speed of the cylinder 1 is controlled so that the speed component in the track direction recorded on the tape of each of the heads 1a and 1b are the same as those for normal reproduction mode by the cylinder speed setting circuit 13 corresponding to the tape speed set by the tape speed setting circuit 12. Therefore, the signal processing circuit 16 can correctly read output signals of the heads 1a and 1b.

If the tape speed setting circuit 12 changes the tape speed in step-wise with a small variation width, the track direction speed component of each head will not deviate significantly from the desired condition even in the transition situation when the tape speed and cylinder speed are changing, so that the date on the track can be reliably read out in the transition situation.

The above operation will be explained in more detail with reference to Figs. 2 to 6.

Fig. 2 is an example of recorded track pattern on the magnetic tape 2, in which numeric 21 shows a track, 22 and 23 show tape position information recorded areas on the track 21, 24 shows tape running direction, and 25 shows head moving direction during recording and normal reproduction.

Fig. 3 shows a condition that the tape as shown in Fig. 2 is running at a higher speed than that in normal reproduction mode. In Fig. 3, denoted by 26 is a vector showing the tape running direction when the tape is running at high speed in the same direction as that in normal reproduction mode (called "FF" mode), 27 is a vector showing the moving direction of the head during FF mode, 28 is a vector showing the tape running direction when it is running at a high speed in the reverse direction to that in normal reproduction mode (called "REW" mode), and 29 is a vector showing the head moving direction during REW mode.

When the tape is made to run at a speed of 100 times faster than that in normal reproduction mode, it is impossible to rotate the cylinder at a speed of 100 times faster than its normal speed. As shown in Fig. 3, on the other hand, when the tape is made to run at a high speed, the head moving direction slants with respect to the direction of the track 21 unless the cylinder is rotated at a proportionately high speed to that of the tape.

Fig. 4 shows the track direction speed component of the head moving speed in FF mode, in which denoted by numerical 41 is a vector showing the tape running speed relative to the head moving speed in normal reproduction mode (reverse to the actual tape running direction), 42 is a vector showing the head moving speed when the tape running is ignored, 43 is a vector showing the head moving speed relative to the tape running speed in normal reproduction mode, 44 is a vector showing the tape running speed relative to the head moving speed in FF mode, 45 is a vector showing a desired head moving speed in FF mode when the tape running is ignored, and 46 is a vector showing the head moving direction relative to the tape running speed in FF mode.

Naturally vector 43 is a composite vector of vectors 41 and 42 and the vector 46 is a composite vector of vectors 44 and 45. Here the desired head moving vector 45 is set so that the magnitude of the component of vector 46 in the direction of vector 43 coincides with the magnitude of vector 43. Therefore, the track direction speed component of the head coincides with that in normal reproduction mode even in FF mode, so that it is possible to read data in the tape position information areas 22 and 23 on the track. The same thing can be said in the REW mode.

It is the rotational speed of the cylinder that determines the head movement. A proper cylinder rotational speed with respect to a tape speed for maintaining a constant track direction speed component of the head is determined by a certain relation as explained below.

Fig. 5 is a diagram showing an example of relationship between the cylinder rotational speed and the tape speed.

In Fig. 5, the abscissa indicates the tape speed, numeral 501 shows the normal tape speed in normal reproduction mode, FF200 shows the 200 fold speed in FF mode, and REW200 shows the 200 hold speed in REW mode. The ordinate indicates the cylinder rotational speed (r.p.m.).

As shown in Fig. 5, the cylinder rotatiohal speed is 2000 r.p.m. in normal reproduction mode, about 3000 rpm at the 200 fold tape speed in FF mode, and 1000 rpm at the 200 fold tape speed in REW mode. The cylinder rotational speed at a tape speed between those two points of REW200 and FF200 is obtained as a value on the line connecting points A and B.

Fig. 5 shows also the variation rate of the track direction speed component of the head when the tape speed is changed while the cylinder speed is kept constant, or vice versa. For instance, when the tape is running at the 200 fold speed in the FF direction while the cylinder speed is kept 2000 r.p.m., the variation is obtained as follows:

$(3000 - 2000)/2000 = 0.5$

That is, a variation of 50% is caused. However, at the 25 fold speed in the FF direction, the variation is as follows:

$50x(25/200) = 6.25\%$

Therefore, when the operable (signal readable) range of the signal processing circuit 16 in Fig. 2 is ±10% in terms of variation in the signal frequency, the position information on the tape can be read reliably irrespective of the increase in the tape speed within 25 fold. It is the same when the tape speed is changed at steps of 25 fold such as from 25 to 50 fold, from 50 to 75 fold, and so on.

Fig. 6 shows the tape speed, cylinder rotational speed, and track direction speed component of the head when the tape speed is changed at small steps by the tape speed setting circuit 12.

In Fig. 6, numeral 602 indicates time axis, 601 an axis of coordinates showing the tape and cylinder speeds, 603 variation of the cylinder rotational speed, 604 variation of the tape speed, 606 time axis, 605 an axis of coordinates showing variation of the track direction speed component of the head, 607 variation of displacement of the track direction speed component of the head, 610 and 611 the operable limits of the signal processing circuit, and 608 the operably range of the signal processing circuit.

When a target tape speed is set by the tape speed setting circuit 12, the tape speed 604 changes towards the target tape speed. The cylinder speed setting circuit 13 receives an instruction corresponding to the target tape speed from the tape speed setting circuit 12 and sets up a rotational frequency obtained by the relationship shown in Fig. 5 so that the cylinder control circuit 14 controls the cylinder 1 to cause the cylinder speed variation 603. For the purpose of explanation, the tape speed and cylinder rotational speed are shown using the same scale in Fig. 6, though actual values are different.

As shown in Fig. 6, the transition conditions of the tape speed and cylinder rotational speed up to their respective target values are not coincident with each other. When the tape speed and cylinder rotational frequency change in this way, the track direction speed component of the head also change naturally as shown by 607 in Fig. 6. When the variation width of 607 is within the range 608 between the operably limits 610 and 611 of the signal processing circuit 16, the position information on the tape can be reliably read. For instance, when the tape speed is changed at steps of 20 or 25 fold, the position information on the tape can be reliably read as described above.

Fig. 7 shows a favorable example of the PV converter 901 in the embodiment of Fig. 1. The PV converter 902 also has the same configuration. Fig. 8 shows the operation waveforms a through g at positions a through g in Fig. 7.

In Fig. 7, numeral 921 denotes a clock signal generating circuit, 922 a 1/12 frequency divider, 923 a 1/6 frequency divider, 924 a 1/4 frequency divider, 925 a 1/3 frequency divider, 926 a selector, 927 a pulse counter, 928 a differentiating circuit, 929 a delay circuit, 930 a latch, 931 a DA converter, and 932 an output terminal of the PV converter 901. Numeral 933 denotes a clock signal selection circuit comprising the frequency dividers 922 through 925 and the selector 926.

The clock signal generating circuit 921 generates a clock signal of a constant frequency, which is applied to the frequency dividers 922, 923, 924 and 925 to be divided to 1/12, 1/6, 1/4 and 1/3, respectively. One of output signals from the four frequency dividers is selected by the selector 926. That is, the clock signal selection circuit 933 selects one of the four types of clock signals. The selector 926 selects one of the clock signals according to a command supplied from the tape speed setting circuit 12. The pulse counter 927 counts pulses of the signal selected by the clock signal selection circuit 933. The waveform d in Fig. 8 shows an example of the output signal of the clock signal selection circuit 933, and e, f, g, ... show output states of the pulse counter 927.

In Fig. 7, the input signal a shown in Fig. 8 supplied from the reel FG 7 is differentiated at its rising edge by the differentiating circuit 928 to become a pulse signal b shown in Fig. 8. The output of the pulse counter 927 is latched by the latch 930 in response to the pulse signal b, and the data latched by the latch 930 is converted into an analog signal by the DA converter 931 and outputted through the output terminal 932. On the other hand, the delay circuit 929 delays the pulse signal b for a very short time to obtain a delayed pulse signal c, which clears the pulse counter 927. Therefore, the pulse counter 927 is cleared immediately after a rising edge of the output signal of the reel FG 7, and the data obtained by counting the pulses of the selected clock signal until the next rising edge.

In other words, an analog voltage proportional to the period of the output signal of the reel FG 7 is obtained at the output terminal 932, that is, the period is converted to a voltage.

In addition, the clock signal fed to the pulse counter 927 is changed into 4 types by the tape speed setting circuit 12 and their frequency ratio is 1:2:3:4. Therefore, the operating frequency of the reel FG in stable condition doubles when the output of the 1/6 frequency divider 923 is select, triples when the output of the 1/4 frequency divider 924 is selected, and quadrupules when the output of the 1/3 frequency divider 925 is selected, compared to the frequency when the output of the 1/12 frequency divider 922 is selected. In other words, the tape speed can be set at 4 different speeds with integral ratios of 1, 2, 3 and 4.

At this time, by setting the frequency of the clock signal generating circuit 921 so that the tape speed is 25 fold when the output of the 1/12 frequency divider 922 is selected, the tape speed which can be set by the tape speed setting circuit 12 becomes 25, 50, 75, or 100 fold. Thus, the tape position information on the tape can be reliable read.

The tape speed setting method can also be realized by dividing the frequency of the ouptut of the reel FG instead of this embodiment.

Fig. 9 shows an example of configuration of the cylinder speed setting circuit 13 and cylinder control circuit 14 in the embodiment of Fig. 1.

In Fig. 9, numeral 1302 denotes a read only memory ("ROM"), 1301 an address setting circuit for generating the address of the ROM, 1401 a differentiating circuit, 1402 a delay circuit, 1403 a presettable counter, 1404 a latch, 1405 a DA converter, 1406 a drive circuit, 1407 a cylinder clock generator, and 1408 an output terminal of the cylinder control circuit 14. In the cylinder control circuit 14, the differentiating circuit 1401, delay circuit 1402, latch 1404, and DA converter 1405 operate in

the same way as the differentiating circuit 928, delay circuit 929, latch 930, and DA converter 931 of the PV converter 901. Therefore, detailed description of them is omitted here.

ROM 1302 stores preset data for the presettable counter 1403 equivalent to the desired rotational speed of the cylinder having the relationship to the tape speed as shown in Fig. 5. When the tape speed setting circuit 12 sets a running speed of the magnetic tape 2, the address setting circuit 1301 generates an address of ROM 1302 from the output of the tape speed setting circuit 12. Data in the ROM designated by the address is outputted to the presettable counter 1403.

On the other hand, the differentiating circuit 1401 generates a pulse at a rising edge of the output signal of the cylinder FG 15. In response to this pulse, the latch 1404 latches count value of the presettable counter 1403. The same pulse is delayed for a very short time by the delay circuit 1402. In response to the delayed pulse, the presettable counter 1403 presets the output data of the ROM 1302. Then the presettable counter 1403 counts the clock pulses generated by the cylinder clock generator 1407 until the next rising edge of the output signal of the cylinder FG 15 comes.

Since the drive circuit 1406 always operates with keeping same condition, the ouptut value of the presettable counter 1403 latched by the latch 1404 in stable condition is approximately constant irrespective of the data presets by the ROM 1302. Therefore, the period of the output signal of the cylinder FG 15 in the stable condition of the cylinder is determined by the preset value set up by the ROM 1302. Since data corresponding to desired rotating speeds of the cylinder in accordance with Fig. 5 are stored in the ROM 1302, the rotational speed of the cylinder can be adjusted to properly correspond to the speed which is set up by the tape speed setting circuit 12.

Fig. 10 shows a magnetic tape reproducing apparatus as a second embodiment of this invention.

In Fig. 10, numerals 947 and 948 denote differentiating circuits, 941 and 944 delay circuits, 942 and 945 presettable counters, 943 and 946 D-latches, 921 a clock signal generating circuit, 933 a clock signal selection circuit, 955 a binary full adder, 956 a DA converter, 952 a ROM, 951 a fixed-value adding circuit, 953 a memory, 954 a binary full adder, 1602 a PLL circuit, 1603 a reference oscillator, 1604 an AND circuit, 1605 a PLL pulse counter, 1606 a data latch, 1608 a ROM, and 1607 a substractor. Numeral 950 denotes a period target value calculating (PTVC) circuit comprising the ROM 952, fixed-value adding circuit 951, memory 953, and binary full adder 954.

The PV converter 901 comprises the differentiating circuit 947, delay circuit 941, presettable counter 942, and D-latch 943. The PV converter 902 comprises the differentiating circuit 948, delay circuit 944, presettable counter 945, and D-latch 946. The adder 903 comprises the binary full adder 955 and DA converter 956. The tape running control circuit 9 comprises the PV converter 901, PV converter 902, period target value calculating circuit 950, adder 903, clock signal generating circuit 921 and clock signal selection circuit 933. Here, the clock signal generating circuit 921 and clock signal selection circuit 933 function in the same way as those shown in Fig. 7. Numeral 1601 denotes a PLL operating point detecting (PLL, OPD) circuit comprising PLL circuit 1602, reference oscillator 1603, AND circuit 1604, PLL pulse counter 1605, data latch 1606, ROM 1608, and subtractor 1607. The signal processing circuit 16 includes the PLL circuit 1602 and PLL operating point detecting circuit 1601.

In Fig. 10, one of a plurality of clock signals generated by the clock signal generating circuit 921 is selected by the clock signal selection circuit 933 according to the output of the tape speed setting circuit 12 in the same way as in the example shown in Fig. 7. The PV converter 901 counts the pulses of the selected clock signal during a period of the output signal of the reel FG 7, i.e., from a rising edge of the output signal of the reel FG 7 to the next rising edge. The PV converter 902 functions in the same way for the output signal for the reel FG 8. The output data of the PV converters 901 and 902 are digitally added by the binary full adder 955, and then converted by the DA converter 956 to an analog signal, which is outputted to the reel drive circuit 10.

The driving load is almost constant and the output of the DA converter 956 remains approximately constant under stable condition. Therefore, a control loop is composed to keep constant the sum of the periods of the output signals of the reel FGs 7 and 8 through the reel drive circuit 10.

Here, the preset values of the presettable counters 942 and 945 are given by the period target value calculating circuit 950 to change the operating points. In other words, when the preset values are made large, differences from the operation stabilizing values of the presettable counters 942 and 945 decrease, and resultantly, the cycles of the reel FGs 7 and 8 become short and stable. That is, the reel rotating speed increases and thus the tape speed increases.

The process until the period target value calculating circuit 950 outputs the preset value is described below.

The output signal of the head 1a or 1b is amplified by a head amplifier (not illustrated) and then inputted to the PLL circuit 1602. The PLL circuit 1602 outputs an oscillating signal synchronized with the head output signal. The reference oscillator 1603 periodically generates high level pulses each having a predetermined duration. The AND circuit 1604 passes the oscillating signal of the PLL circuit 1602 only during the duration of each of the high level pulses from the reference oscillator 1603, and the pulses of the passed signal are counted by the PLL pulse counter 1605. The count result of the PLL pulse counter 1605 is latched by the data latch 1606 at the falling edge of each of the high level pulses from the reference oscillator 1603.

Thus, data showing how many waves were outputted from the PLL circuit 1602 during the predetermined duration of each high level pulse is stored in the data latch 1606. The ROM 1608 constantly outputs a data showing the number of waves that the PLL circuit 1602 should output in normal reproduction mode. The substractor 1607 calculates the difference between the number of waves actually outputted from the PLL circuit 1602 and the output of the ROM 1608. The output of the subtractor 1607 becomes the output of the PLL operating point detecting circuit 1601.

In other words, the PLL operating point detection circuit 1601 calculates a deviation of the actual operating frequency of the PLL circuit 1602 from the desired operating frequency of the PLL circuit 1602 and outputs the result. all of the above processing done based on digital data.

In the period target value calculating circuit 950, such an operation is repeated at intervals of equal to or longer than one cycle of the cylinder 1 that the output data of the PLL operating point detecting circuit 1601 and an output data of the memory 953 are added by the binary full adder 954 and the resultant data is rewritten into the memory 953. The ROM 952 stores minimum value of digital data required as the preset values for the presettable counters 942 and 945. A constant value given by the ROM 952 is added to the output of the binary full adder 954 by the fixed-value adding circuit 951, and the result becomes the output of the period target value calculating circuit 950. That is, the tape running speed is finely adjusted by the output of the period target value calculating circuit 950 until the output data of the PLL operating point detecting circuit 1601 becomes 0, when the value of the memory 953 is renewed.

Fig. 11 shows the preset values of the presettable counters 942 and 945 and the reel FG cycle target values in terms of the count clock values of the presettable counters 942 and 945 when the output of the binary full adder 954 is assumed 6-bit digital data. The number of settable tape speed is equal to the number of this reel FG cycle target values.

The output of the binary full adder 954 has 64 kinds of values from "000000" to "111111" as shown in column 1101 on the table in Fig. 11. Assuming the ROM value be "010100" and the number of bits of the output of the fixed-value adding circuit 951 be 8 bits, the output of the fixed-value adding circuit 951 is as shown in column 1102. (Here, the lower 6 bits are added.) Assuming the number of bits of each of the presettable counters 942 and 945 be also 8 bits, the number of clocks from the preset value of each of the presettable counters 942 and 945 to the center value of the counter is as shown in column 1103. Here, the center value of the counter is "10000000". When the values in column 1103 are expressed by decimal number, the results are as shown in column 1104.

Since the target value of the sum of the periods of the reel FG output signals is twice the values in column 1104, the number of clocks varies from 90 to 216. Since the tape speed is proportional to the reciprocal value of the sum of the periods of the reel FG output signals, the tape speed for clock number 90 is 216/90 = 2.4 times the tape speed for clock number 216.

Thus, the tape speed can be set up to 64 kinds of equally divided speeds between 1 and 2.4 based on the 64 kinds of outputs of the binary full adder 954. The data stored in the memory 953 in the period target value calculating circuit 950 has either one of the above described 64 kinds so that the output data of the PLL operating point detecting circuit 1601 becomes 0.

Therefore, even if the tape length or tape thickness is changed, the deviation of the tape speed due to such changes can be adjusted.

As will be known from the above description, since the ROM 1608 and ROM 952 may store only one kind of data, it is clear that these ROMs may be replaced by more simple elements such as DIP switches.

As described above, according to this invention, tape position information recorded on the tracks can be read precisely while magnetic tape is running at high speed. Especially even in the transition stage when the tape running speed increases, the tape position information can be correctly read to enable high speed search. By detecting the track direction speed component of the head from the reproduced signal frequency from the head to adjust the tape speed, a more reliable search becomes possible.

This invention was explained above according to embodiments, but it is needless to say that the applications of this invention are not limited to the embodiment explained above. For example, the recording tape is not limited to magnetic tape, but other tapes employing optical recording, magneto-optic recording, etc. may be used.

Claims

1. An apparatus for reproducing signals recorded in slanting tracks on a recording tape including a tape position information recorded at a specified area on each track, comprising:
a rotary cylinder mounting thereon a reproducing head;
a cylinder rotation detector for producing a periodic signal corresponding to a rotational speed of said rotary cylinder;
two reels on which said tape is wound for running said tape;
two reel rotation detectors for producing periodic signals corresponding to rotational speeds of said two reels, respectively;
a reel drive means for driving either one of said two reels to run said tape;
a tape speed setting means capable of setting a plurality of tape speeds and outputting a signal indicative of one of the settable plurality of tape speeds;
a tape running control means for outputting a drive signal to said reel drive means according to the output signals from said two reel rotation detectors and the output signal from said tape speed setting means so that said tape runs at the speed set by said tape speed setting means;
a cylinder speed setting means for setting such a rotational speed of said rotary cylinder that a track direction speed component of said head is kept constant according to the output signal from said tape speed setting means and outputting a signal indicative of the set rotational speed;
a cylinder control means for controlling said rotary cylinder according to the output signal from said cylinder rotation detector and the output signal from said cylinder speed setting means so that said rotary cylinder rotates at the speed set by said cylinder speed setting means;
and
a signal processing circuit for reading information picked up by said head from said tape.

2. An apparatus according to claim 6, wherein said tape running control means comprises:
two period-to-voltage conversion means for converting periods of the respective periodic output signals from said two reel rotation detectors to two voltage signals according to the output signal from said tape speed setting means; and
an adding means for adding the two voltage signals to obtain said drive signal.

3. An apparatus according to claim 2, wherein each of said period-to-voltage conversion means comprises:
a clock signal generating means for generating a plurality of clock signals having different frequencies from one another and outputting one of the plurality of clock signals according to the output signal from said tape speed setting means;
a counter for counting clocks of the output clock signal from said clock signal generating means;
a latch circuit for latching a count output of said counter at intervals of time corresponding to the period of the periodic output signal from corresponding one of said two reel rotation detectors;
a latch pulse generating circuit for generating a latch pulse for said latch circuit from the periodic output signal from the corresponding one of said two reel rotation detectors;
a reset pulse generating circuit for generating a reset pulse from said latch pulse for resetting said counter; and
a DA converter for converting a latched output of said latch circuit to an analog signal which is one of said two voltage signals.

4. An apparatus according to claim 1, wherein said cylinder speed setting means comprises:
a memory storing therein a plurality of rotational speed data corresponding to a plurality of rotational speeds of said rotary cylinder for keeping the track direction speed component of said head constant; and
an address setting circuit for outputting an address for said memory according to the output signal from said tape speed setting means so that said memory outputs one of said plurality of rotational speed data, and
said cylinder control means comprises:
a clock signal generator for generating a clock signal;
a presettable counter which presets the output rotational speed data from said cylinder speed setting means and counts clocks of the clock signal from said clock signal generator;
a latch circuit for latching a count output of said counter at intervals of time corresponding to the period of the periodic output signal from said cylinder rotation detector;
a latch pulse generating circuit for generating a latch pulse for said latch circuit from the periodic output signal from said cylinder rotation detector;
a preset pulse generating circuit for generating a preset pulse from said latch pulse for presetting the rotational speed data from said cylinder speed setting means to said counter;
a DA converter for converting a latched output of

said latch circuit into an analog signal; and
a drive circuit for driving said rotary cylinder according to said analog signal.

5. An apparatus according to claim 1, wherein, during a transition state in which the tape speed is changed from one speed to another, said tape speed setting means changes the tape speed in step-wise so that a deviation of the track direction speed component of said tape in each step of change of the tape speed is within a range in which said signal processing circuit can correctly read said tape position information.

6. An apparatus for reproducing signals recorded in slanting tracks on a recording tape including a tape position information recorded at a specified area on each track, comprising:
a rotary cylinder mounting thereon a reproducing head;
a cylinder rotation detector for producing a periodic signal corresponding to a rotational speed of said rotary cylinder;
two reels on which said tape is wound for running said tape;
two reel rotation detectors for producing periodic signals corresponding to rotational speeds of said two reels, respectively;
a signal processing circuit for processing signals picked up by said head from said tape;
a reel drive means for driving either one of said two reels to run said tape;
a tape speed setting means capable of setting a plurality of tape speeds and outputting a signal indicative of one of the settable plurality of tape speeds,
a period target value calculating means for producing a period target value from an output signal from said signal processing circuit;
a tape running control means for outputting a drive signal to said reel drive means according to the output signals from said two reel rotaiton detectors, the output signal from said tape speed setting means and said period target value so that said tape runs at the speed set by said tape speed setting means;
a cylinder speed setting means for setting such a rotational speed of said rotary cylinder that a track direction speed component of said head is kept constant according to the output signal from said tape speed setting means and outputting a signal indicative of the set rotational speed; and
a cylinder control means for controlling said rotary cylinder according to the output signal from said cylinder rotation detector and the output signal from said cylinder speed setting means so that said rotary cylinder rotates at the speed set by said cylinder speed setting means.

7. An apparatus according to claim 6, wherein said tape running control means comprises:
a clock signal generating means for generating a plurality of clock signals and outputting one of the plurality of clock signals according to the output signal from said tape speed setting means;
a first presettable counter which presets said period target value and counts clocks of the output clock signal from said clock signal generating means during a first interval corresponding to the period of the periodic output signal from one of said two reel rotation detectors;
a first latch circuit for latching a count output of said first presettable counter at the end of said first interval;
a second presettable counter which presets said period target value and counts clocks of the output clock signal from said clock signal generating means during a second interval corresponding to the period of the periodic output signal from the other of said two reel rotation detectors;
a second latch circuit for latching a count output of said second presettable counter at the end of said second interval;
an adder for adding latched outputs of said first and second latch circuits; and
a DA converter for converting an added output of said adder to an analog signal which is said drive signal.

8. An apparatus according to claim 6, wherein said signal processing circuit has:
a PLL circuit for producing an oscillation signal synchronized with a signal picked up by said head from said tape; and
a PLL operating point detecting circuit for detecting a difference of the number of waves of the oscillation signal from a predetermined number of waves and outputting a difference value indicative of said difference as said output signal of said signal processing circuit.

9. An apparatus according to claim 8, wherein said period target value calculating means comprises:
a first memory and a first adder, said first adder adding said difference value outputted from said signal processing circuit with a value stored in said first memory, an added output value of said first adder being written into said first memory;
a second memory storing a predetermined fixed value; and
a second adder for adding the added output value of said first adder with said predetermined fixed value to obtain said period target value.

FIG. 1

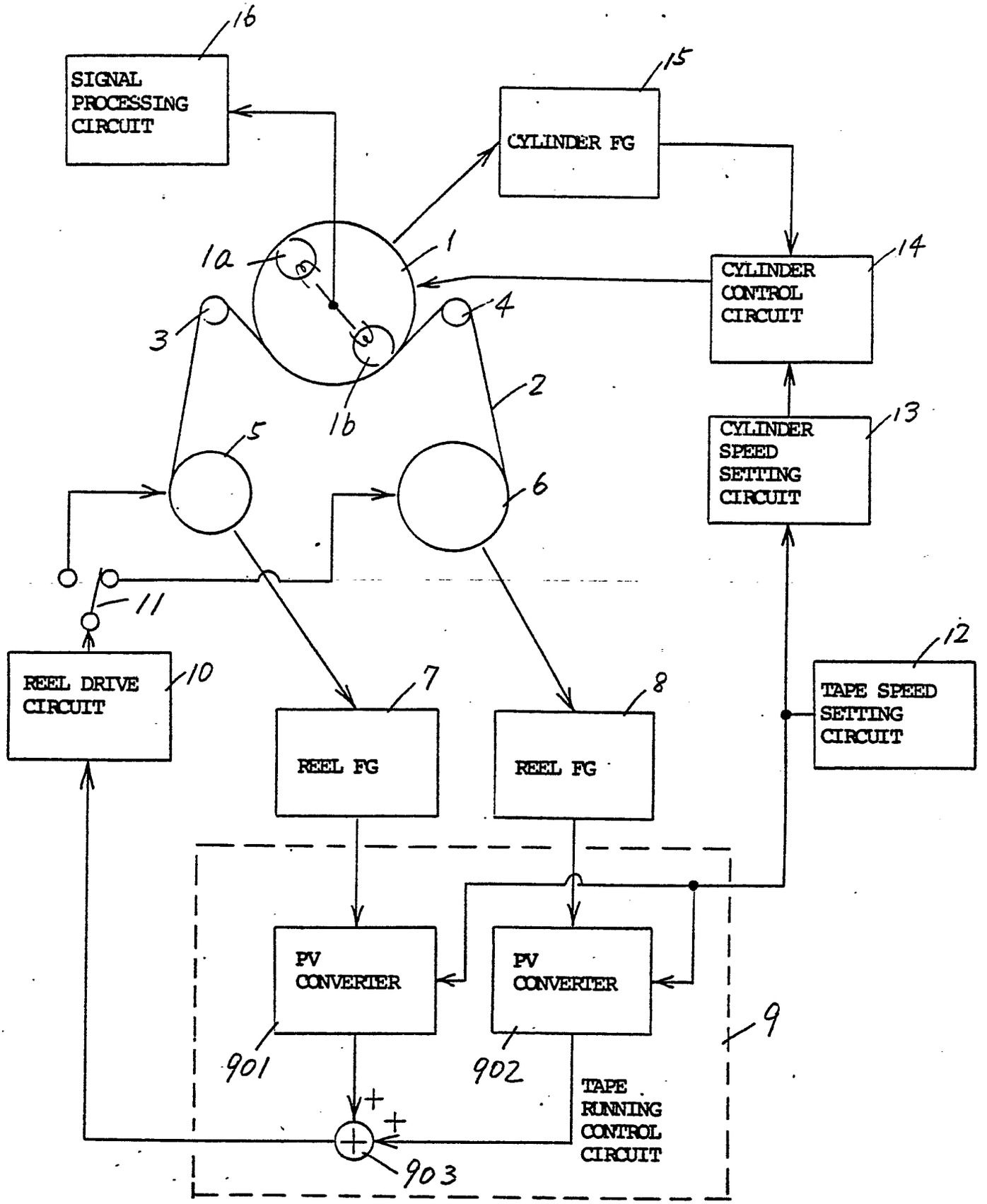

16
SIGNAL PROCESSING CIRCUIT
15
CYLINDER FG
1
1a
1b
14
CYLINDER CONTROL CIRCUIT
3
4
2
5
6
13
CYLINDER SPEED SETTING CIRCUIT
11
12
REEL DRIVE CIRCUIT
10
7
8
TAPE SPEED SETTING CIRCUIT
REEL FG
REEL FG
PV CONVERTER
PV CONVERTER
9
901
902
TAPE RUNNING CONTROL CIRCUIT
+
+
903

FIG. 2

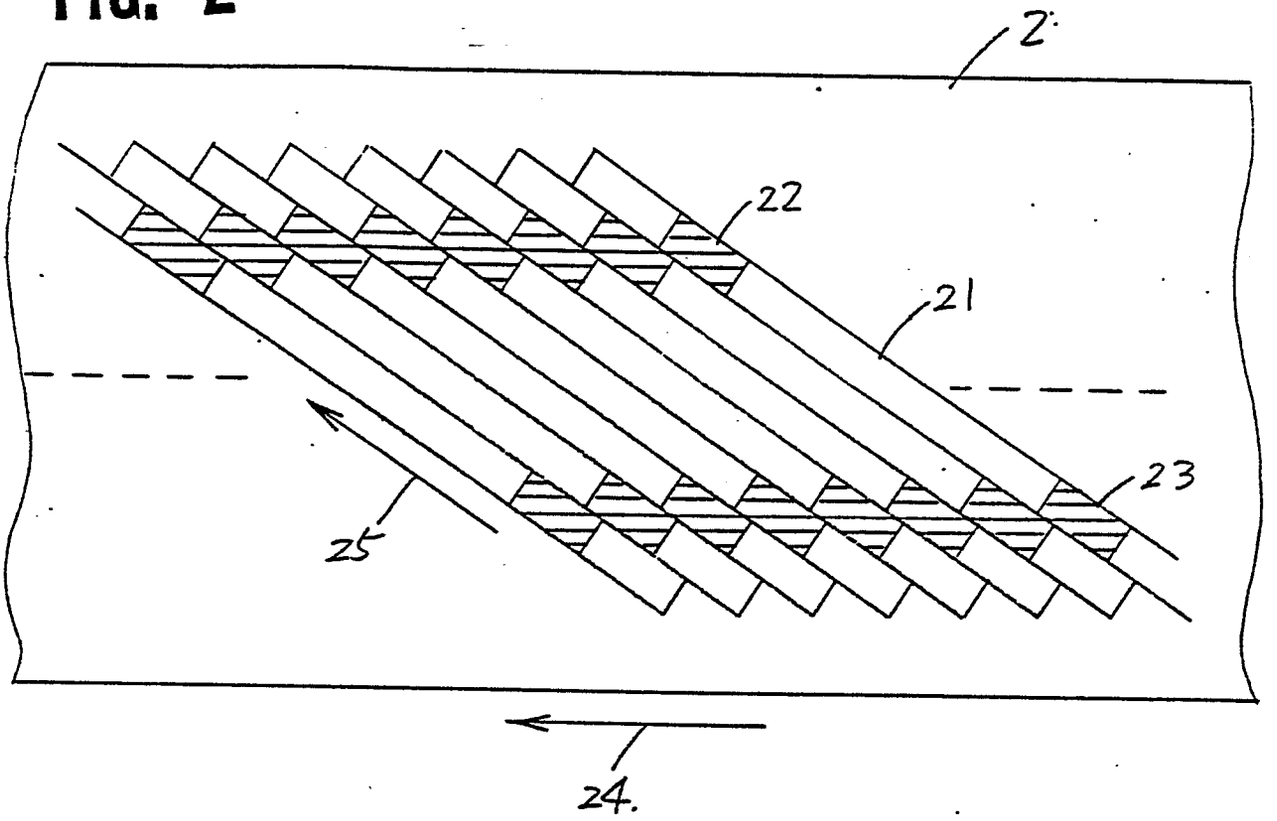


FIG. 3

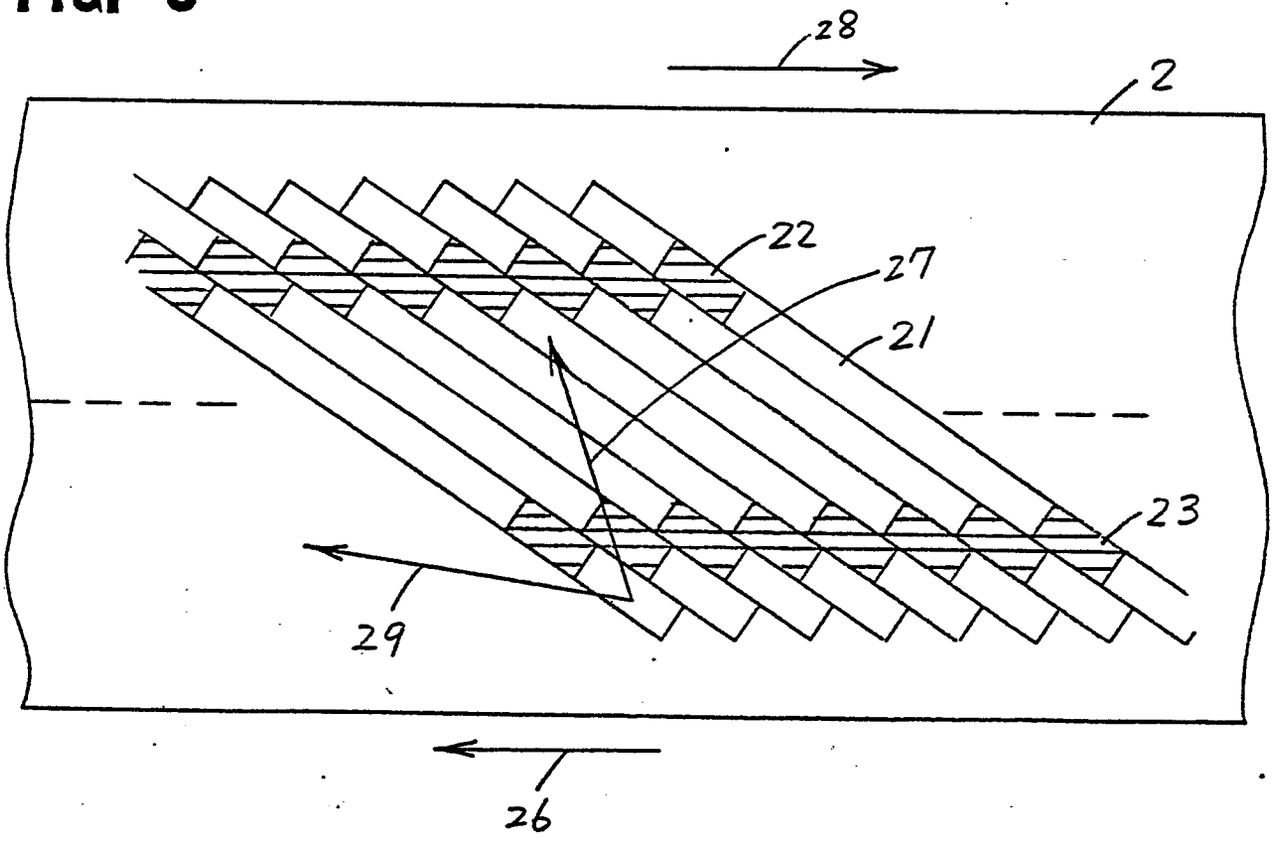


FIG. 4

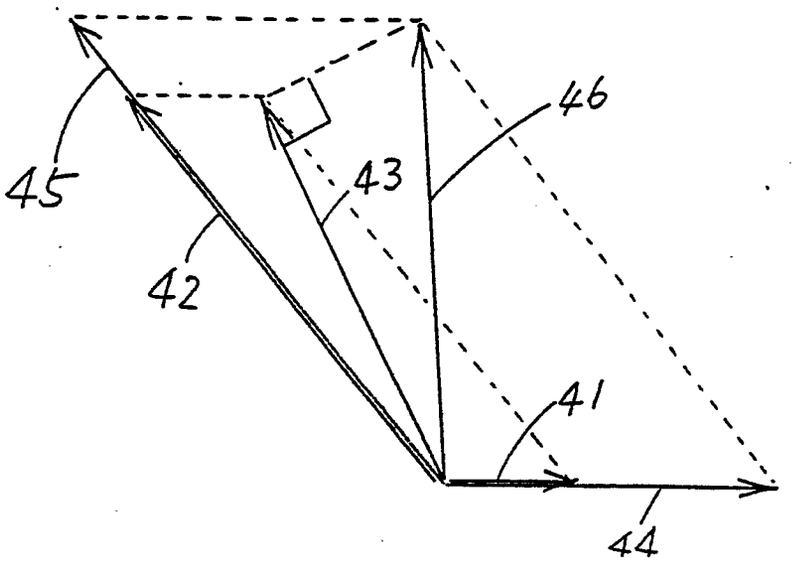


FIG. 5

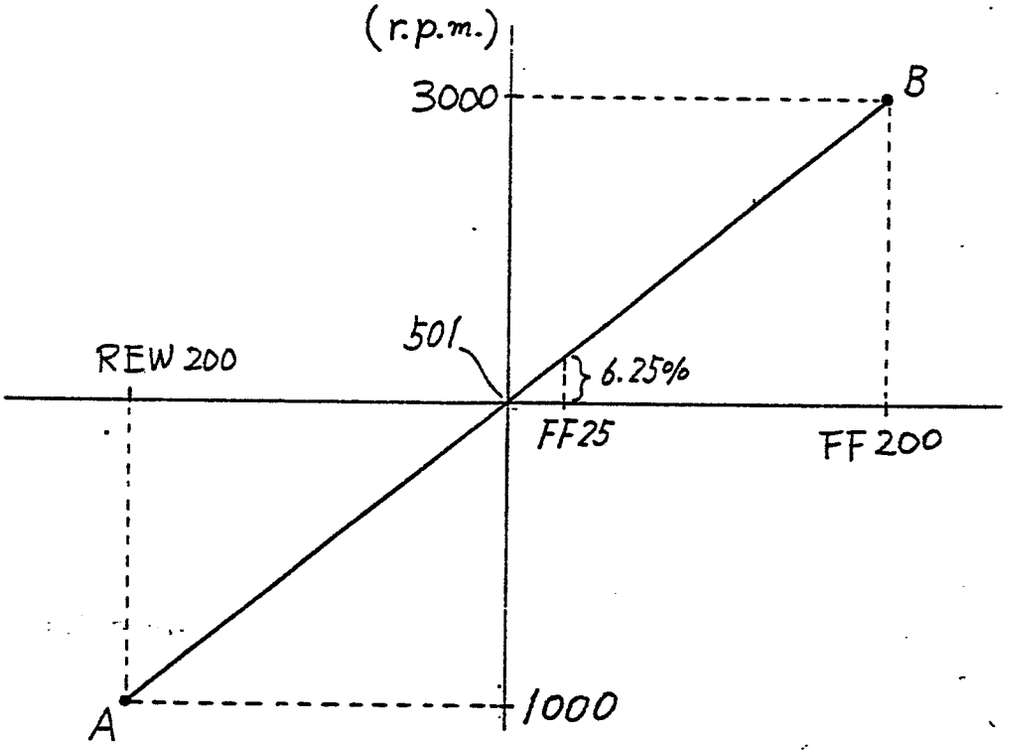


FIG. 6

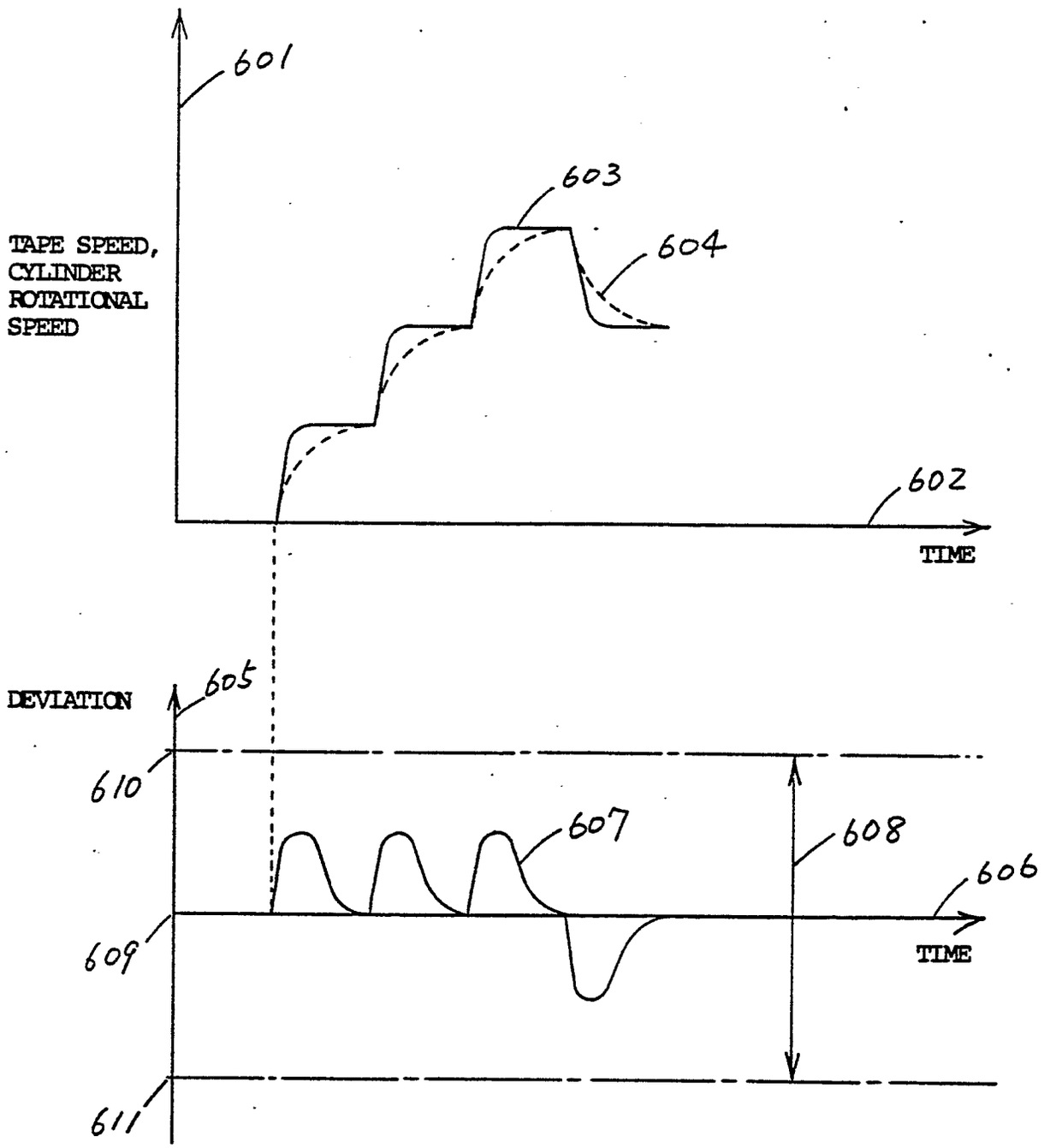

601
603
604
TAPE SPEED,
CYLINDER
ROTATIONAL
SPEED
602
TIME
DEVIATION
605
610
607
608
606
609
TIME
611

FIG. 7

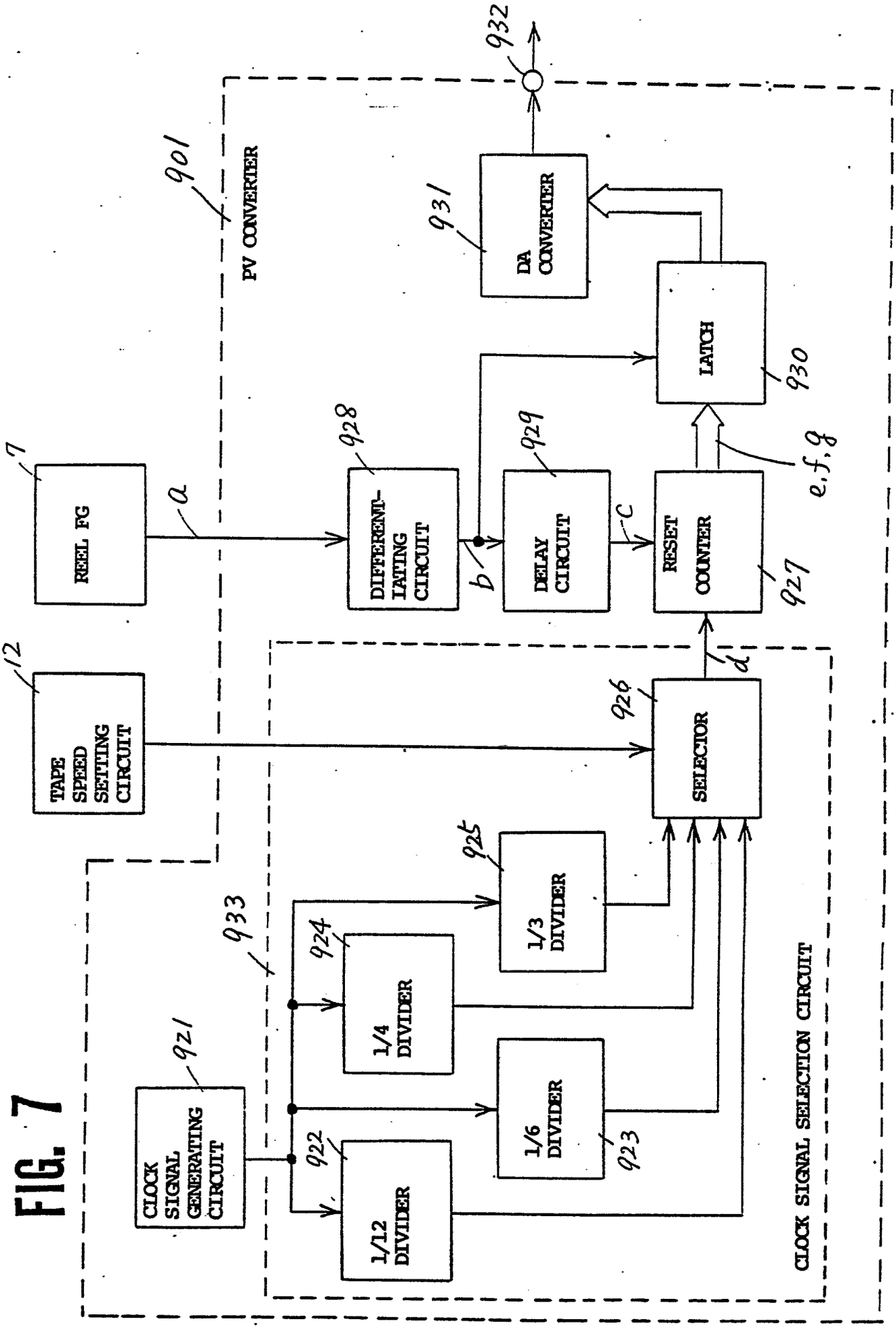

901
PV CONVERTER
CLOCK SIGNAL SELECTION CIRCUIT
7
REEL FG
12
TAPE SPEED SETTING CIRCUIT
921
CLOCK SIGNAL GENERATING CIRCUIT
933
922
1/12 DIVIDER
923
1/6 DIVIDER
924
1/4 DIVIDER
925
1/3 DIVIDER
926
SELECTOR
927
RESET COUNTER
928
DIFFERENTIATING CIRCUIT
929
DELAY CIRCUIT
930
LATCH
931
DA CONVERTER
932
a
b
c
d
e, f, g

FIG. 8

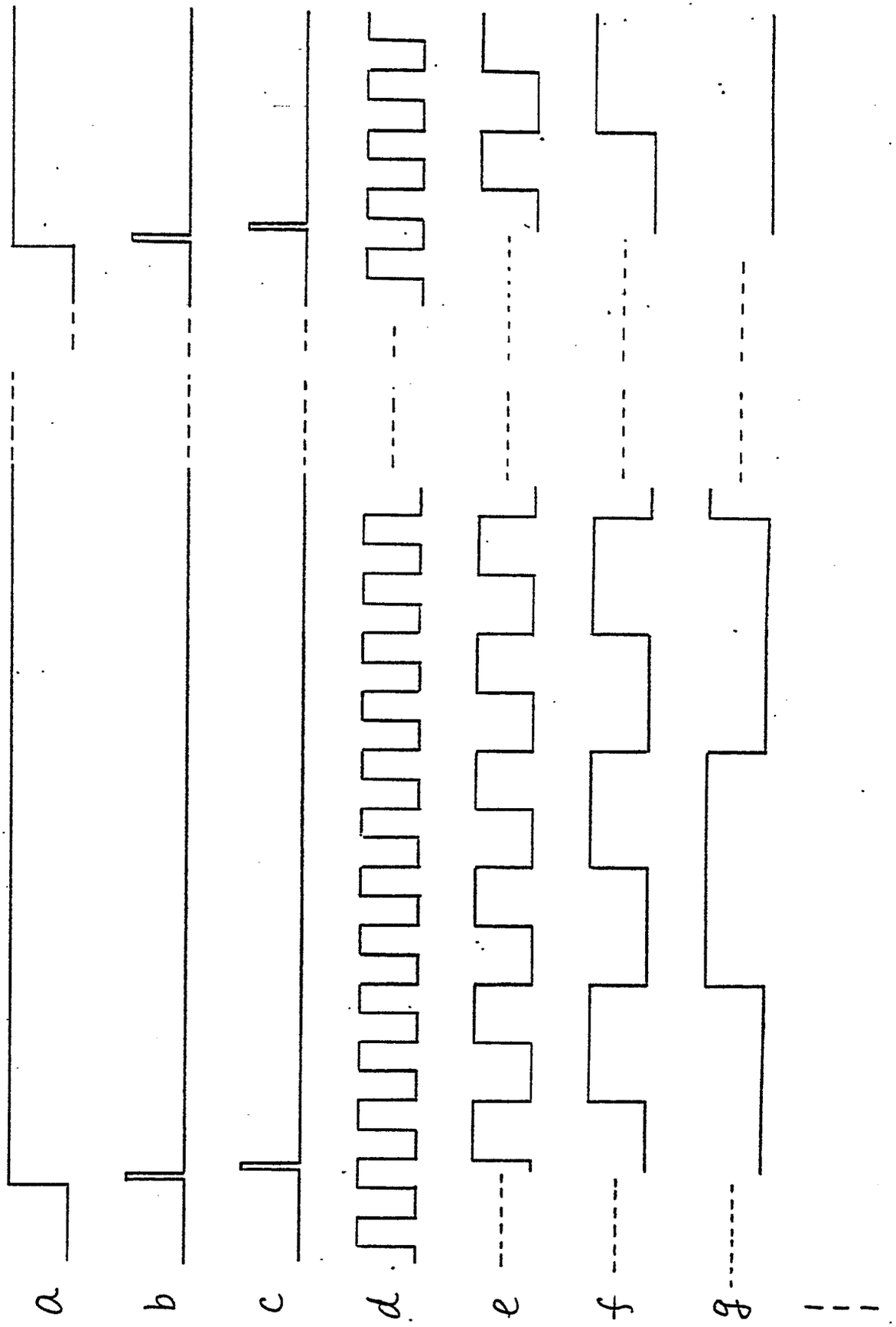


FIG. 9

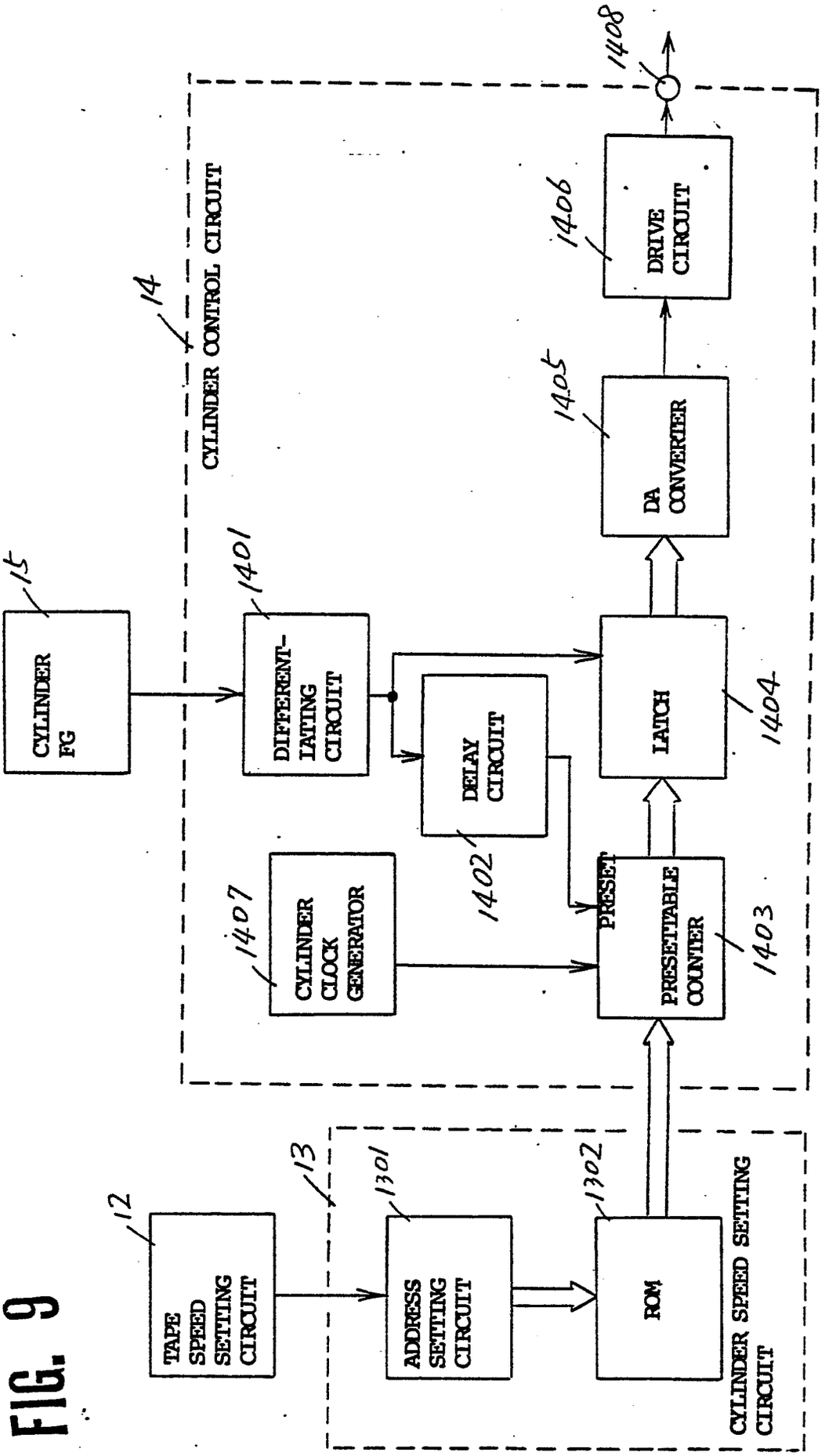

TAPE SPEED SETTING CIRCUIT
12
CYLINDER SPEED SETTING CIRCUIT
13
ADDRESS SETTING CIRCUIT
1301
ROM
1302
CYLINDER CONTROL CIRCUIT
14
CYLINDER FG
15
DIFFERENTIATING CIRCUIT
1401
DELAY CIRCUIT
1402
CYLINDER CLOCK GENERATOR
1407
PRESET
PRESETTABLE COUNTER
1403
LATCH
1404
DA CONVERTER
1405
DRIVE CIRCUIT
1406
1408

FIG.10

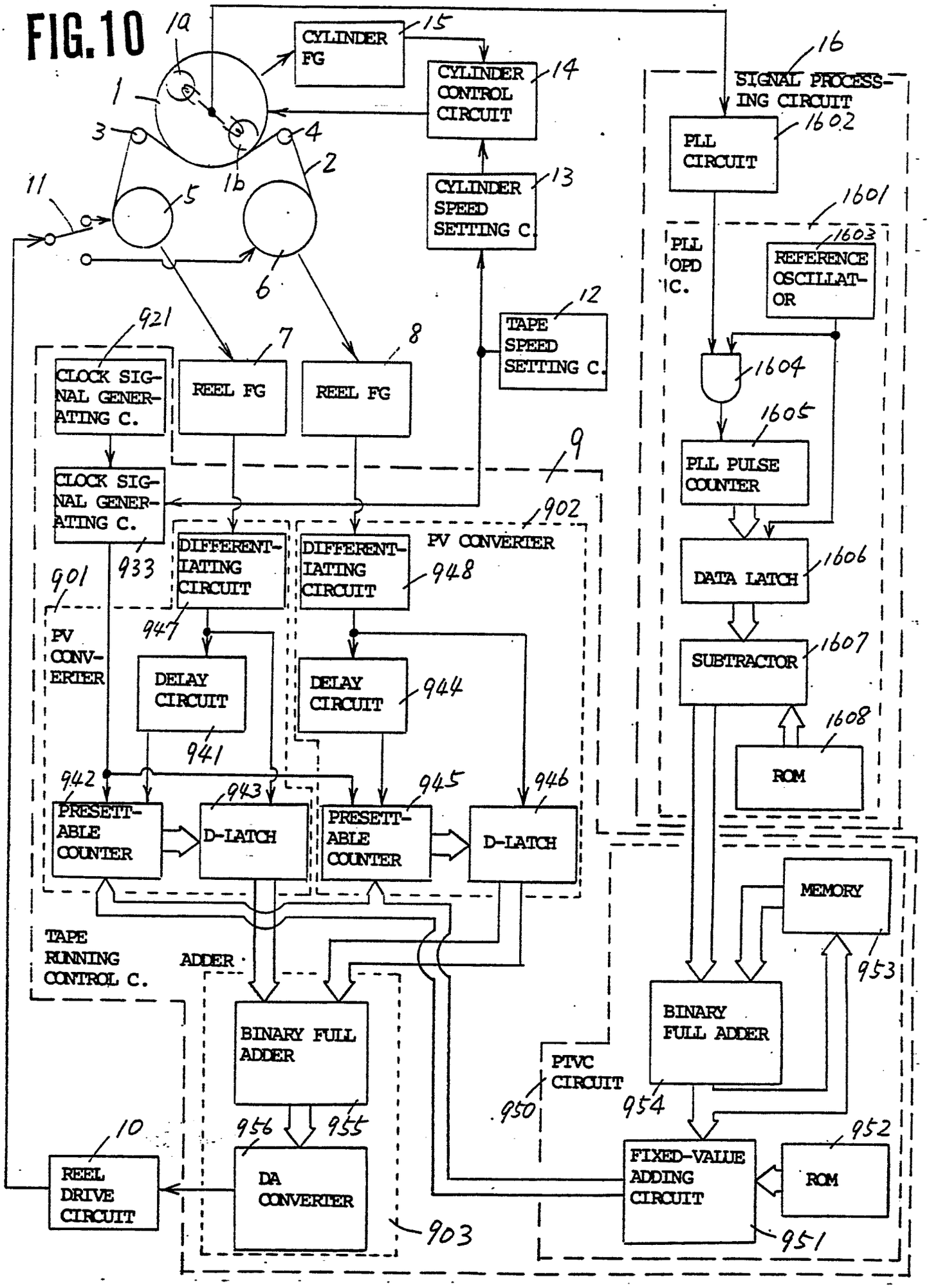

1a
1
3
4
2
1b
11
5
6
CYLINDER FG
15
CYLINDER CONTROL CIRCUIT
14
CYLINDER SPEED SETTING C.
13
TAPE SPEED SETTING C.
12
SIGNAL PROCESSING CIRCUIT
16
PLL CIRCUIT
1602
1601
PLL OPD C.
REFERENCE OSCILLATOR
1603
1604
1605
PLL PULSE COUNTER
DATA LATCH
1606
SUBTRACTOR
1607
ROM
1608
921
CLOCK SIGNAL GENERATING C.
REEL FG
7
REEL FG
8
9
CLOCK SIGNAL GENERATING C.
933
902
PV CONVERTER
DIFFERENTIATING CIRCUIT
948
DIFFERENTIATING CIRCUIT
901
PV CONVERTER
947
DELAY CIRCUIT
941
DELAY CIRCUIT
944
942
943
945
946
PRESETTABLE COUNTER
D-LATCH
PRESETTABLE COUNTER
D-LATCH
TAPE RUNNING CONTROL C.
ADDER
MEMORY
953
BINARY FULL ADDER
BINARY FULL ADDER
PTVC CIRCUIT
950
954
10
956
955
REEL DRIVE CIRCUIT
DA CONVERTER
903
FIXED-VALUE ADDING CIRCUIT
951
952
ROM

FIG.11

1101 OUTPUT OF BINARY FULL-ADDER 954	1102 OUTPUT OF FIXED-VALUE ADDING CIRCUIT 951	1103 NUMBER OF CLOCKS TO THE CENTER VALUE OF THE COUNTER	1104 DECIMAL EXPRESSION OF THE NUMBER OF CLOCKS
0 0 0 0 0 0	0 0 0 1 0 1 0 0	0 1 1 0 1 1 0 0	108
0 0 0 0 0 1	0 0 0 1 0 1 0 1	0 1 1 0 1 0 1 1	107
0 0 0 0 1 0	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 0	106
0 0 0 0 1 1	0 0 0 1 0 1 1 1	0 1 1 0 1 0 0 1	105
0 0 0 1 0 0	0 0 0 1 1 0 0 0	0 1 1 0 1 0 0 0	104
⋮	⋮	⋮	⋮
1 1 1 1 1 0	0 1 0 1 0 0 1 0	0 0 1 0 1 1 1 0	46
1 1 1 1 1 1	0 1 0 1 0 0 1 1	0 0 1 0 1 1 0 1	45

0 254 511