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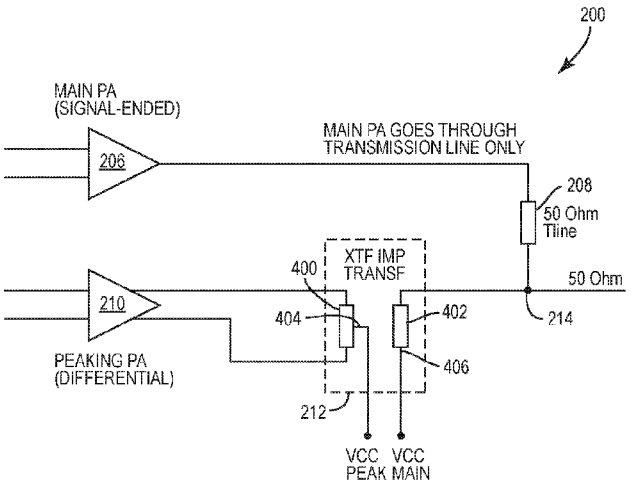

FIG. 4

(57) Abstract: A broadband Doherty power amplifier is disclosed. A Doherty power amplifier includes a main power amplifier and a peaking amplifier. In contrast to conventional approaches that combine outputs from the main and peaking amplifiers before an impedance transformation circuit, the Doherty power amplifier combines the outputs after an impedance transformation circuit in the peaking amplifier output path. This eliminates, or at least reduces, a possible impedance step down and corresponding impedance step up for the main output path. Reduction or elimination of such a step down and step up reduces insertion loss and allows increased efficiency at the first efficiency peak, as well as improving the fractional bandwidth of the Doherty power amplifier.

[Continued on next page]

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BROADBAND DOHERTY POWER AMPLIFIER

PRIORITY APPLICATION

[0001] The present application claims the benefit of and is related to U.S. Provisional Patent Application Serial No. 63/602,791 filed on November 27, 2023, and entitled "BROADBAND DOHERTY POWER AMPLIFIER," the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND

I. Field of the Disclosure

[0002] The technology of the disclosure relates generally to power amplifiers and, more particularly, to broadband Doherty power amplifiers that may be used, for example, in a wireless transmission circuit.

II. Background

[0003] Computing devices abound in modern society, and more particularly, mobile communication devices have become increasingly common. The prevalence of these mobile communication devices is driven in part by the many functions that are now enabled on such devices. Increased processing capabilities in such devices means that mobile communication devices have evolved from pure communication tools into sophisticated mobile entertainment centers, thus enabling enhanced user experiences. With the advent of the myriad functions available to such devices, there has been increased pressure to find ways to increase the amount of data that may be sent to and received from such devices. This pressure has resulted in, for example, evolving cellular standards, which impose stringent requirements on transmitters within mobile communication devices. These requirements include having the ability to handle signals in bandwidths that are comparatively large compared to historical requirements. Concurrently, there is pressure to reduce the overall size of the circuits used in the transmitters. Balancing these design criteria provides room for innovation.

SUMMARY

[0004] Aspects disclosed in the detailed description include systems and methods for providing a broadband Doherty power amplifier. In particular, a Doherty power amplifier

includes a main power amplifier and a peaking amplifier. In contrast to conventional approaches that combine outputs from the main and peaking amplifiers before an impedance transformation circuit, aspects of the present disclosure combine the outputs after an impedance transformation circuit in the peaking amplifier output path. This eliminates, or at least reduces, a possible impedance step down and corresponding impedance step up for the main output path. Reduction or elimination of such a step down and step up reduces insertion loss and allows increased efficiency at the first efficiency peak as well as improving the fractional bandwidth of the Doherty power amplifier.

[0005] In this regard, in one aspect, a Doherty power amplifier is disclosed. The Doherty power amplifier includes a main power amplifier having a main output, a phase shifter coupled to the main output and a combining node, and a peaking power amplifier having a peaking output. The Doherty power amplifier also includes an impedance transfer transformer circuit coupled to the peaking output at an input side and coupled to the combining node at an output side.

[0006] In another aspect, a Doherty power amplifier is disclosed. The Doherty power amplifier includes a main path through a main power amplifier, the main path comprising a ninety-degree phase shift after the main power amplifier, and a peaking path through a peaking power amplifier having an inverted input path for a differential signal to create a negative one hundred eighty-degree phase shift, the peaking path comprising an initial ninety-degree phase shift before the peaking power amplifier and at least one tunable element to add delay to the peaking path such that the negative one hundred eighty-degree phase shift is canceled.

[0007] In another aspect, a method of operating a Doherty power amplifier is disclosed. The method includes providing a first signal through a main path having a main power amplifier and phase shifting the first signal by ninety degrees using a phase shifter. The method also includes providing a second signal through a peaking path having a peaking power amplifier, stepping up the impedance of the peaking path using an impedance transfer transformer circuit, and, after stepping up the impedance of the peaking path, combining the main path and the peaking path.

[0008] In another aspect, a mobile terminal comprising a transceiver, the transceiver comprising a power amplifier stage, is disclosed. The mobile terminal includes a Doherty power amplifier comprising a main power amplifier having a main output, a phase shifter

coupled to the main output and a combining node, and a peaking power amplifier having a peaking output. The mobile terminal further includes an impedance transfer transformer circuit coupled to the peaking output at an input side and coupled to the combining node at an output side.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1A is a block diagram of a conventional Doherty power amplifier that is used in wireless communication devices;

[0010] Figures 1B-1D are block diagrams of variations on the Doherty power amplifier of Figure 1A with various transformations between single-ended and differential signals;

[0011] Figure 1E is a block diagram of a conventional Doherty power amplifier that highlights the shortcomings of the basic Doherty design;

[0012] Figure 2 is a block diagram of a first exemplary aspect of a Doherty power amplifier having output paths combined after an impedance transformation for a peaking amplifier;

[0013] Figure 3 is a block diagram of a second exemplary aspect of a Doherty power amplifier having output paths combined after an impedance transformation for a peaking amplifier but retaining a small impedance step down in an output path of a main power amplifier;

[0014] Figure 4 is a block diagram of another exemplary aspect of a Doherty power amplifier where a direct current (DC) bias is provided for a peaking power amplifier through an impedance transfer transformer circuit, thereby reducing a need for an extra radio frequency (RF) choke;

[0015] Figure 5 is a block diagram of another exemplary aspect of a Doherty power amplifier where a DC bias is provided for both a peaking power amplifier and main power amplifier through an impedance transfer transformer circuit, thereby reducing the need for an extra RF choke;

[0016] Figure 6 is a block diagram of a Doherty power amplifier with an output path combination point according to the present disclosure with a delay compensation circuit to preserve Doherty action;

[0017] Figure 7 is a block diagram of a Doherty power amplifier according to aspects of the present disclosure with additional analog predistortion to assist in linearization;

[0018] Figures 8 and 9 are block diagrams of two possible design choices reflecting how some circuitry can be digital versus analog;

[0019] Figure 10 is a flowchart illustrating an exemplary process for operating a Doherty power amplifier according to aspects of the present disclosure; and

[0020] Figure 11 is a block diagram of a mobile terminal, which may include the Doherty power amplifier of Figures 2-9 in a transceiver, according to the present disclosure.

DETAILED DESCRIPTION

[0021] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0022] It will be understood that although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and similarly, a second element could be termed as a first element without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0023] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element, or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, no intervening elements are present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other

element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, no intervening elements are present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element, or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, no intervening elements are present.

[0024] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0025] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including," when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0026] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0027] In keeping with the above admonition about definitions, the present disclosure uses the term "transceiver" in a broad manner. Current industry literature uses "transceiver" broadly to refer to a plurality of circuits that send and receive signals. Exemplary circuits may include a baseband processor, an up/down conversion circuit, filters, amplifiers, couplers, and the like coupled to one or more antennas. Likewise, some authors in the industry literature refer to a circuit positioned between a baseband processor

and a power amplifier circuit as a transceiver. This intermediate circuit may include the up/down conversion circuits, mixers, oscillators, filters, and the like, but generally does not include the power amplifiers. As used herein, the term transceiver is used in the first sense. Where relevant to distinguish between the two definitions, the terms "transceiver chain" and "transceiver circuit" are used respectively.

[0028] Aspects disclosed in the detailed description include systems and methods for providing a broadband Doherty power amplifier. In particular, a Doherty power amplifier includes a main power amplifier and a peaking amplifier. In contrast to conventional approaches that combine outputs from the main and peaking amplifiers before an impedance transformation circuit, aspects of the present disclosure combine the outputs after an impedance transformation circuit in the peaking amplifier output path. This eliminates, or at least reduces, a possible impedance step down and corresponding impedance step up for the main output path. Reduction or elimination of such a step down and step up reduces insertion loss and allows increased efficiency at the first efficiency peak as well as improving the fractional bandwidth of the Doherty power amplifier.

[0029] Before addressing aspects of the present disclosure, an overview of a conventional Doherty power amplifier is provided with reference to Figures 1A-1D. Specific issues that provide challenges to designers are discussed with reference to Figure 1E, and solutions to these challenges are discussed beginning with reference to Figure 2.

[0030] In this regard, Figure 1A is a block diagram of a simplified conventional Doherty amplifier 100. The Doherty amplifier 100 has an input node 102 and an output node 104. At the input node 102, an incoming signal is split. A first signal path 106 goes to a primary or main power amplifier 108. A secondary signal path 110 is active when switches 112A, 112B are on (i.e., closed so that a signal may pass therethrough) and inactive when the switches 112A, 112B are off (i.e., open or open circuits such that no signal passes therethrough). When the secondary signal path 110 is active, signals thereon go through a phase shifter 114 that imposes a ninety-degree phase shift on the signal. A peaking power amplifier 116 amplifies the shifted signal. A combiner 118 combines the signal paths 106, 110 and provides the summed signal to the output node 104.

[0031] Thus, in operation, at low power level boosts, the switches 112A, 112B are open, and only the main power amplifier 108 is used to amplify signals. When gain beyond what is possible with the main power amplifier 108 is required, the switches

112A, 112B are closed, and peaking power amplifier 116 is used to create an additional boost to the signal such that when the signals on paths 106, 110 are summed a sufficiently amplified signal is present at the output node 104. To make sure the phases of the signal paths 106, 110 are the same, a phase shifter 120 may be provided in the first signal path 106. Note that the combiner 118 is at the output node 104 may be a simple shared conductive node and need not be explicit circuitry.

[0032] Doherty amplifiers have, by design, a single-ended output. However, there may be instances where a differential signal is desired for any number of reasons. Figures 1B-1D illustrate a few of the possible configurations as well as possible variations in the signal paths in terms of signal conditioning. It should be appreciated that, absent a clear indication to the contrary, aspects of the present disclosure may work with any of these basic structures independent of what specific elements lie within what signal paths and independent of whether a particular portion of the path is single-ended or differential-ended.

[0033] Figure 1B illustrates a Doherty power amplifier 100B having a differential-ended portion in the peaking path and driver amplifier stages in each path. More particularly, the Doherty power amplifier 100B has an input node 102 and an output node 104 with a main path 126 and a peaking path 128. The main path 126 has a main driver amplifier 130 and a main amplifier 132, along with a phase shifter 134. The peaking path 128 has a phase shifter 136, a single-ended to differential-ended driver amplifier 138, a differential-ended peaking amplifier 140, and a differential-ended to single-ended filter 142. The paths 126, 128 are combined at the output node 104.

[0034] Figure 1C illustrates a Doherty power amplifier 100C having a differential-ended main portion in the main path. More particularly, the Doherty power amplifier 100C has an input node 102 and an output node 104 with a main path 146 and a peaking path 148. The main path 146 has a single-ended to differential-ended driver amplifier 150, a differential main power amplifier 152, a differential-ended to single-ended filter 154, and a phase shifter 156. The peaking path 148 has a phase shifter 114, a single-ended driver amplifier 160, and a single-ended peaking power amplifier 162. The paths 146 and 148 are combined at the output node 104.

[0035] Figure 1D illustrates a Doherty power amplifier 100D having differential main path 166 and differential peaking path 168. More particularly, the Doherty power

amplifier 100D has an input node 102 and an output node 104. The main path 166 has a single-ended driver amplifier 170, a single-ended to differential-ended interstage match circuit 172, a differential main power amplifier 174, and a phase shifter 175. The peaking path 168 has a phase shifter 114, a single-ended driver amplifier 178, a single-ended to differential-ended interstage match circuit 180, and a differential peaking power amplifier 182. The paths 166, 168 are combined at a combining node 184 and a differential-ended to single-ended filter 186 couples the combining node 184 to the output node 104.

[0036] Regardless of whether there are just single-ended components or there is some mix of differential components, and regardless of the presence of driver amplifiers or interstage match circuits, conventional Doherty amplifiers use a phase shifter in the main path (e.g., phase shifters 120, 134, 156, 175 of main paths 106, 126, 146, 166 respectively).

[0037] A generic representation of this structure is provided in Figure 1E, where a Doherty amplifier 100E has a main path 190 and a peaking path 192. The main path has a main power amplifier 193 and a phase shifter 194, while the peaking path 192 has a peaking amplifier 195, and the paths are combined at a node 196. An impedance transfer transformer circuit 198 is provided at the node 196 for the reasons explained below.

[0038] The phase shifter 194 (and its corollary phase shifters 120, 134, 156, 175) is used for load modulation and specifically to put the signal in the main path 190 at the same phase as the signal in the peaking path 192. In most cases, the phase shifter 194 may be a transmission line of a certain length that, by virtue of its length, shifts the phase of the main path 190. It is also possible to synthesize a transmission line with an LC-circuit that imposes the same sort of phase shift.

[0039] The output of the peaking amplifier 195 is typically a low impedance. This low impedance is used because it is easier to push power out of a power amplifier at a low impedance than at a higher impedance. Thus, the node 196 may be around, for example, ten ohms (10 Ω). To get the proper impedance match between the paths 190, 192 at the node 196, the phase shifter 194 (i.e., the transmission line) may step down (shown by the Z ↓ symbol) the impedance from a comparatively high impedance (e.g., 40 Ω) to the low impedance of the node 196. While conceivably possible to have a low impedance at the output of the main amplifier 193, the requirements of the phase shifter 194 make this approach impractical.

[0040] To get the output of the Doherty amplifier 100E back to a level suitable for use by other elements in the amplifier chain, the impedance transfer transformer circuit 198 steps the impedance back up (shown by the Z ↑ symbol), typically to fifty ohms.

[0041] This arrangement imposes two penalties. First, bandwidth is a function of the square root of the total impedance transformation, so having two impedance transformations after the main amplifier 193 limits the bandwidth. When operating frequencies were in the relatively low-frequency bands, this bandwidth penalty was not too troublesome. However, with the increasing frequencies of emerging cellular and other wireless standards, this bandwidth penalty is becoming commercially impractical. Second, having these two functions after the main amplifier 193 imposes two insertion losses, which reduces efficiency.

[0042] By design, a Doherty amplifier has the best efficiency when both the main amplifier 193 and the peaking amplifier 195 are operational but spends most of its time at an average power, meaning the peaking amplifier 195 is turned off. Thus, most of the time, when only the main amplifier 193 is being used, the efficiency is degraded by the two insertion losses. Efficiency improves when the peaking amplifier 195 and its solitary insertion loss are operational, but again, this benefit is only available for a small portion of the total time.

[0043] Exemplary aspects of the present disclosure reposition the combination node after an impedance transfer transformer such that the main path no longer suffers the penalties associated with two large impedance transfers, thereby improving main path bandwidth and efficiency.

[0044] In a first exemplary aspect, illustrated in Figure 2, the impedance step down for the combining node is eliminated. Specifically, a Doherty amplifier 200 has a main path 202 and a peaking path 204. The main path 202 includes a main power amplifier 206 and a phase shifter 208, which may be a transmission line or synthesized line, as discussed above. The peaking path 204 has a peaking power amplifier 210 and an impedance transfer transformer circuit 212, which may also perform a differential to single-ended transfer function. After the impedance transfer transformer circuit 212, the paths 202 and 204 are combined at a combining node 214. Relevantly, the phase shifter 208 may have a uniform impedance along the length of the transmission line and may match the stepped-up impedance resulting from the impedance transfer transformer

circuit 212 (e.g., 50 Ω). Now the main path 202 has no penalty from an impedance transfer and only has the insertion loss of the phase shifter 208, thereby improving both bandwidth and efficiency.

[0045] It should be appreciated that while shown as a single-ended main path 202 and a differential peaking path 204, any of the arrangements shown in Figures 1A-1D and other variations may still benefit from the arrangement of Figure 2.

[0046] It should be noted that having a fifty ohms (50 Ω) output impedance for the main power amplifier 206 may require that the main power amplifier 206 have a supply voltage as high as six (or higher) volts (6+ V). Not every mobile computing device can provide this level of supply voltage. Thus, a Doherty amplifier 300, illustrated in Figure 3, may be used instead. In particular, the Doherty amplifier 300 has a main path 302 and a peaking path 304. The main path 302 includes a main power amplifier 306 and a phase shifter 308, which may be a transmission line or synthesized line, as discussed above. The peaking path 304 has a peaking amplifier 310 and an impedance transfer transformer circuit 312, which may also perform a differential to single-ended transfer function. After the impedance transfer transformer circuit 312, the paths 302 and 304 are combined at a combining node 314.

[0047] In contrast to the phase shifter 208 of Figure 2, the phase shifter 308 may also include a small impedance step-up. For example, the combining node 314 may have an intermediate impedance of thirty-five ohms (35 Ω). The phase shifter 308 may step up a low initial impedance (e.g., 10 Ω) to this intermediate impedance. Then another small impedance transfer circuit 316 may be present to step up the impedance to fifty ohms. By having two smaller impedance steps, the bandwidth is impacted less than the step down-step up arrangement of Figure 1E. Likewise, by only placing relatively small impedance transfers, the overall efficiency remains relatively high compared to the arrangement of Figure 1E. Alternatively, the phase shifter 308 has no impedance function, and the main power amplifier 306 outputs into the intermediate impedance.

[0048] Figure 4 provides additional details about the impedance transfer transformer circuit 212 and provides an ancillary benefit that may be provided for a differential peaking power amplifier 210. Specifically, a direct current (DC) bias signal is generally provided to the peaking power amplifier 210 through a large radio frequency (RF) choke. This RF choke is usually expressed through an inductor. Inductors generally take up

relatively large amounts of space. However, by having a transformer in the impedance transfer transformer circuit 212, an opportunity for reduction or elimination of an extra inductor is created. Specifically, the impedance transfer transformer circuit 212 may include a primary coil (i.e., an inductor) 400 and a secondary coil (i.e., also an inductor) 402. A DC bias signal may be supplied through a center tap 404 on the primary coil 400 to the peaking power amplifier 210. Similarly, a DC bias signal may be supplied to the main power amplifier through the bottom 406 of the secondary coil 402. While not shown, the bottom 406 may need to be at an alternating current (AC) ground. This ground may be provided by appropriate capacitors, as is better explained below.

[0049] Where both the peaking power amplifier and the main power amplifier are differential, two center taps may be provided, as illustrated by Doherty amplifier 500 in Figure 5. The Doherty amplifier 500 may include a main path 502 and a peaking path 504. The main path 502 has a differential main power amplifier 506 and phase shifters 508A, 508B. The peaking path 504 has a differential peaking power amplifier 510 and impedance transfer transformer circuit 512. The paths 502, 504 are combined at differential node 514. A differential to single-ended filter 516 is coupled to the node 514 and provides the single-ended output at output node 518.

[0050] With continued reference to Figure 5, the impedance transfer transformer circuit 512 (like impedance transfer transformer circuit 212) has a primary coil 520 and a secondary coil 522. A center tap 524 on the primary coil 520 provides a DC bias signal for the peaking power amplifier 510. A center tap 526 on the secondary coil 522 provides a DC bias signal for the main power amplifier 506.

[0051] It should be noted that the active elements of the Doherty amplifier, according to aspects of the present disclosure, may impose some phase delay in the signals in the peaking path relative to the main path. When the transform frequency (FT) is large compared to the operating frequency (OF), such delays may be considered negligible. However, modern operating frequencies are increasing and thus more likely to be a substantial portion of the FT. Accordingly, these delays may be large enough to negatively impact the Doherty effect (because the signals are no longer in phase at the combining node).

[0052] Figure 6 provides a solution for this unwanted phase shift. Note that this complication is not necessary for every Doherty amplifier according to aspects of the

present disclosure, but this solution may be helpful to designers in certain circumstances. Specifically, a Doherty amplifier 600 has a main path 602 and a peaking path 604. The main path 602 has a driver amplifier 608A and a main power amplifier 608B along with a phase shifter 610 that provides a ninety-degree phase shift as previously discussed.

[0053] The peaking path 604 includes an initial phase shifter 612 (analogous to phase shifters 114 and 136 of Figures 1A-1D) that provides a phase shift of ninety degrees. The peaking path 604 also includes a driver amplifier 614A and a peaking power amplifier 614B. However, instead of a direct connection between the driver amplifier 614A and the peaking power amplifier 614B, the inputs of the peaking power amplifier 614B are inverted, which effectively provides a negative one hundred eighty-degree phase shift. Then, the impedance transfer transformer circuit 616 has tunable elements 618A, 618B added that allow the delay of the peaking path to be expanded to one hundred eighty degrees (some portion from the inherent delay of the active elements and the remainder tuned from the tunable elements 618A, 618B). By forcing the delay to be one hundred eighty degrees and providing an effective negative one hundred eighty degrees, the phases are in line at the combining node 620. Note that capacitor 622 is added as the AC ground discussed above.

[0054] The assignee of the present disclosure also has a variety of disclosures relating to analog predistortion (APD), and any of those techniques may be added to a front-end module (FEM) 700, as illustrated in Figure 7. Specifically, a baseband circuit 702 may provide information to a transceiver circuit 704 and/or the FEM 700 and specifically an APD linearization circuit 706. Additionally, a sensor 708 may provide information to the APD linearization circuit 706. The APD linearization circuit 706 may force on or off the peaking amplifier 710 or control a bias for either the peaking amplifier 710 or the main amplifier 712. Likewise, there may be other tunable elements in the FEM 700 that may be adjusted to assist in APD linearization.

[0055] Figures 8 and 9 provide options for a fully analog (e.g., gallium arsenide) Doherty approach (Figure 8) compared to a hybrid approach where a part of the Doherty approach is implemented in a complementary metal oxide semiconductor (CMOS) chip. Thus, APD signals may be sent from a CMOS controller 800 in Figure 8 to a GaAs Doherty amplifier 802 versus predriver amplifiers 900A, 900B in a CMOS controller 902. The remainder of the Doherty amplifier may be in the GaAS chip 904.

[0056] A method of operating a Doherty amplifier according to aspects of the present disclosure is provided in process 1000, illustrated in Figure 10. The process 1000 starts by splitting a signal onto a main path and a peaking path (block 1002). The peaking signal is phase-shifted (block 1004), amplified (block 1006), and then impedance-transformed using an impedance transfer transformer circuit (block 1008).

[0057] Concurrently, the main signal is amplified (block 1010) and phase-shifted (block 1012). After blocks 1008 and 1012, the signals are combined (block 1014). Optionally, and not shown, an additional impedance transfer may be applied. Relevantly, the impedance transform at block 1008 only occurs on the peaking signal and only when the peaking path is active.

[0058] With reference to Figure 11, the concepts described above may be implemented in various types of user elements 1100, such as mobile terminals, smart watches, tablets, computers, navigation devices, access points, and like wireless communication devices that support wireless communications, such as cellular, wireless local area network (WLAN), Bluetooth, and near field communications. The user elements 1100 will generally include a control system 1102, a baseband processor 1104, transmit circuitry 1106, receive circuitry 1108, antenna switching circuitry 1110, multiple antennas 1112, and user interface circuitry 1114. In a non-limiting example, the control system 1102 can be a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC), as an example. In this regard, the control system 1102 can include at least a microprocessor(s), an embedded memory circuit(s), and a communication bus interface(s). The receive circuitry 1108 receives radio frequency signals via the antennas 1112 and through the antenna switching circuitry 1110 from one or more base stations. A low noise amplifier and a filter of the receive circuitry 1108 cooperate to amplify and remove broadband interference from the received signal for processing. Downconversion and digitization circuitry (not shown) will then downconvert the filtered, received signal to an intermediate or baseband frequency signal, which is then digitized into one or more digital streams using an analog-to-digital converter(s) (ADC).

[0059] The baseband processor 1104 processes the digitized received signal to extract the information or data bits conveyed in the received signal. This processing typically comprises demodulation, decoding, and error correction operations. The baseband

processor 1104 is generally implemented in one or more digital signal processors (DSPs) and ASICs.

[0060] For transmission, the baseband processor 1104 receives digitized data, which may represent voice, data, or control information, from the control system 1102, which it encodes for transmission. The encoded data is output to the transmit circuitry 1106, where a digital-to-analog converter(s) (DAC) converts the digitally encoded data into an analog signal, and a modulator modulates the analog signal onto a carrier signal that is at a desired transmit frequency or frequencies. A power amplifier will amplify the modulated carrier signal to a level appropriate for transmission and deliver the modulated carrier signal to the antennas 1112 through the antenna switching circuitry 1110 to the antennas 1112. The multiple antennas 1112 and the replicated transmit and receive circuitries 1106, 1108 may provide spatial diversity. Modulation and processing details will be understood by those skilled in the art.

[0061] It is also noted that the operational steps described in any of the exemplary aspects herein are described to provide examples and discussion. The operations described may be performed in numerous different sequences other than the illustrated sequences. Furthermore, operations described in a single operational step may actually be performed in a number of different steps. Additionally, one or more operational steps discussed in the exemplary aspects may be combined. It is to be understood that the operational steps illustrated in the flowchart diagrams may be subject to numerous different modifications, as will be readily apparent to one of skill in the art. Those of skill in the art will also understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0062] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations. Thus, the disclosure is not intended to be limited to

the examples and designs described herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A Doherty power amplifier comprising:

a main power amplifier having a main output;

a phase shifter coupled to the main output and a combining node;

a peaking power amplifier having a peaking output; and

an impedance transfer transformer circuit coupled to the peaking output at an input side and coupled to the combining node at an output side.

2. The Doherty power amplifier of claim 1, wherein the phase shifter comprises a transmission line sized so as to provide a ninety-degree phase shift.

3. The Doherty power amplifier of claim 1, wherein the phase shifter comprises an LC circuit that provides a ninety-degree phase shift.

4. The Doherty power amplifier of claim 1, wherein the phase shifter has an output impedance of approximately fifty ohms (50 Ω).

5. The Doherty power amplifier of claim 1, wherein the phase shifter has an output impedance between twenty and forty ohms (20-40 Ω).

6. The Doherty power amplifier of claim 5, further comprising a second impedance transfer circuit coupled to the combining node and configured to step up impedance to approximately fifty ohms (50 Ω).

7. The Doherty power amplifier of claim 1, wherein the peaking power amplifier comprises a differential output.

8. The Doherty power amplifier of claim 1, further comprising a direct current bias coupled to a primary coil of the impedance transfer transformer circuit.

9. The Doherty power amplifier of claim 1, further comprising an inverter circuit coupled to an input of the peaking power amplifier.

10. The Doherty power amplifier of claim 9, further comprising a tuning circuit coupled to the impedance transfer transformer circuit, the tuning circuit adding a delay up to one hundred eighty degrees to a peaking path of the peaking power amplifier.

11. A Doherty power amplifier comprising:

a main path through a main power amplifier, the main path comprising a ninety-degree phase shift after the main power amplifier;

a peaking path through a peaking power amplifier having an inverted input path for a differential signal to create a negative one hundred eighty-degree phase shift, the peaking path comprising an initial ninety-degree phase shift before the peaking power amplifier and at least one tunable element to add delay to the peaking path such that the negative one hundred eighty-degree phase shift is canceled.

12. The Doherty power amplifier of claim 11, wherein the at least one tunable element comprises a tunable capacitor.

13. The Doherty power amplifier of claim 12, further comprising an impedance transfer transformer circuit and the tunable capacitor is associated with the impedance transfer transformer circuit.

14. The Doherty power amplifier of claim 11, further comprising a combining node, wherein the peaking path comprises an impedance transfer transformer circuit positioned before the combining node.

15. The Doherty power amplifier of claim 14, further comprising a second impedance transfer circuit positioned after the combining node.

16. A method of operating a Doherty power amplifier comprising:

providing a first signal through a main path having a main power amplifier;

phase shifting the first signal by ninety degrees using a phase shifter;

providing a second signal through a peaking path having a peaking power amplifier;

stepping up impedance of the peaking path using an impedance transfer transformer circuit; and

after stepping up impedance of the peaking path, combining the main path and the peaking path.

17. The method of claim 16, further comprising after combining, providing an additional impedance step up to approximately fifty ohms (50 Ω).

18. The method of claim 16, further comprising providing a direct current (DC) bias in the peaking path through the impedance transfer transformer circuit.

19. The method of claim 16, further comprising a direct current (DC) bias in the main path through the impedance transfer transformer circuit.

20. A mobile terminal comprising a transceiver, the transceiver comprising a power amplifier stage comprising:

a Doherty power amplifier comprising:

a main power amplifier having a main output;

a phase shifter coupled to the main output and a combining node;

a peaking power amplifier having a peaking output; and

an impedance transfer transformer circuit coupled to the peaking output at an input side and coupled to the combining node at an output side.

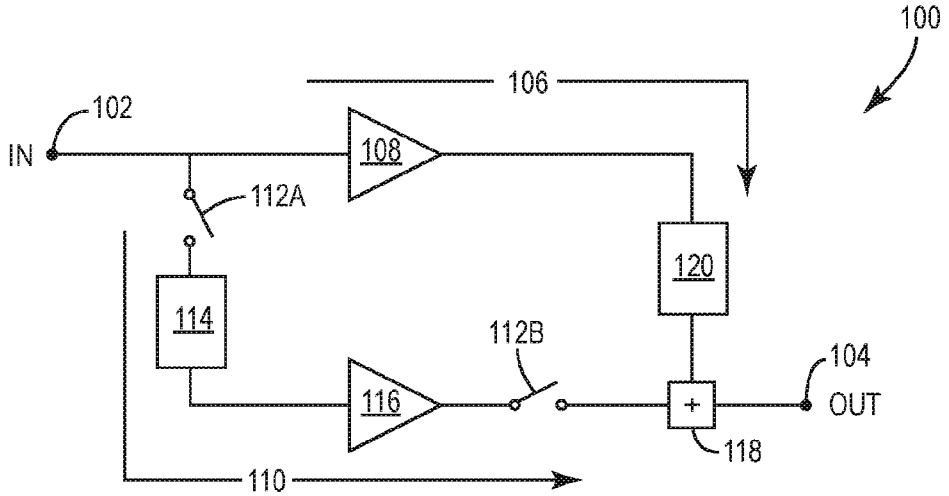

FIG. 1A

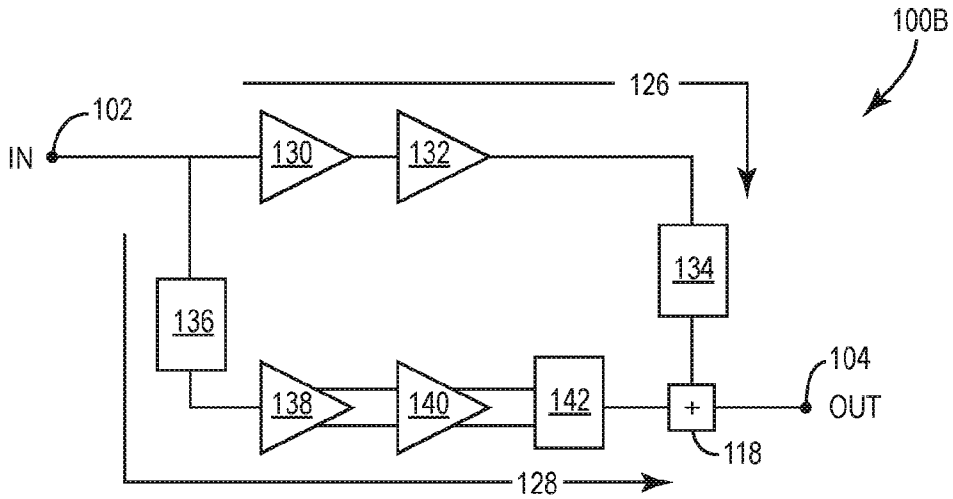

FIG. 1B

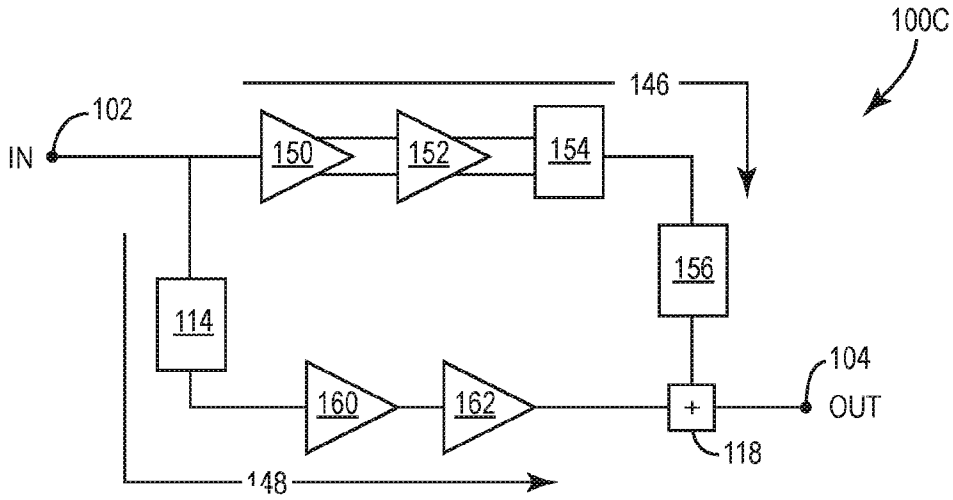

FIG. 1C

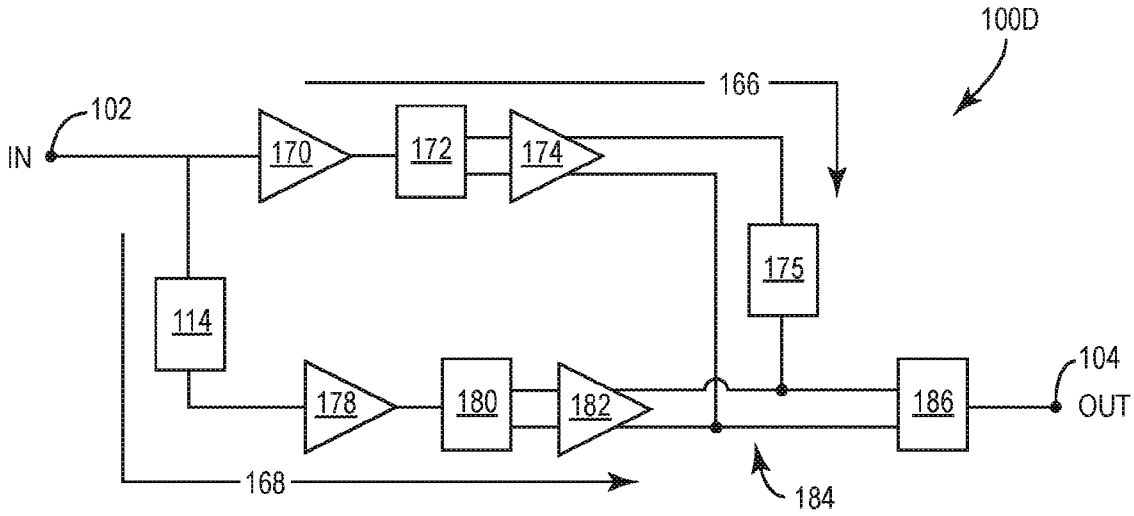
100D
166
102
IN
170
172
174
175
114
178
180
182
186
104
OUT
168
184

FIG. 1D

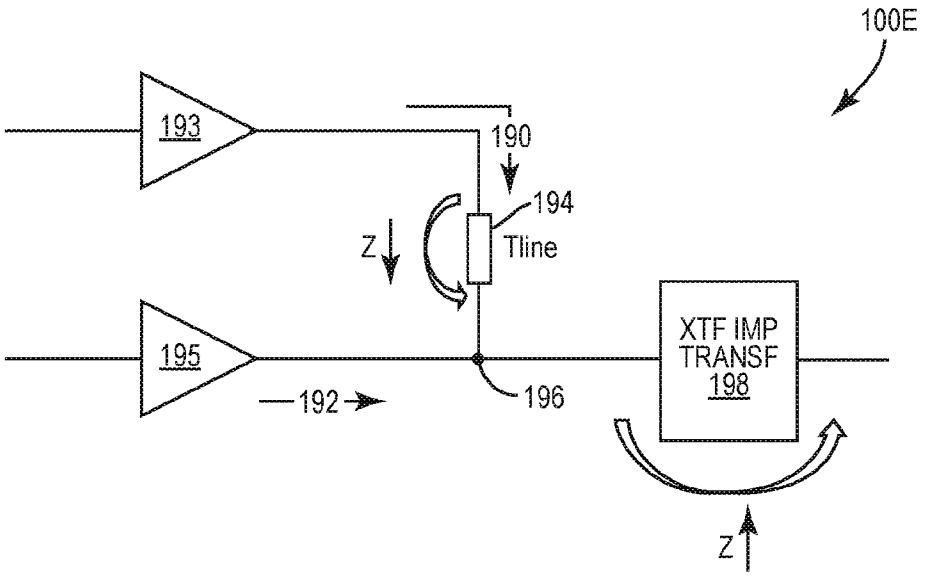
100E
193
190
194
Z
Tline
195
192
196
XTF IMP
TRANSF
198
Z

FIG. 1E

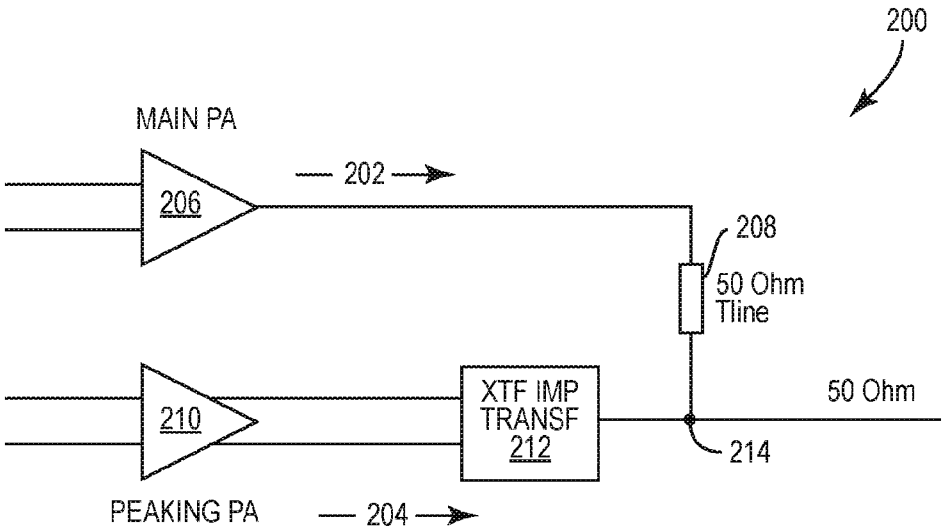
200
MAIN PA
206
202
208
50 Ohm
Tline
210
XTF IMP
TRANSF
212
50 Ohm
214
PEAKING PA
204

FIG. 2

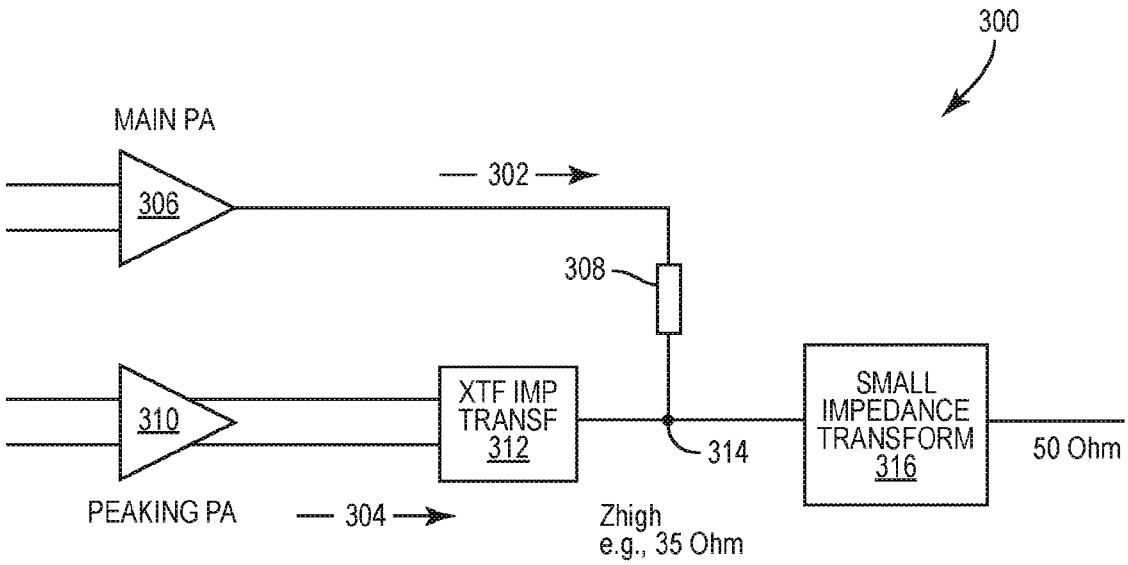
300
MAIN PA
306
302
308
310
XTF IMP
TRANSF
312
314
SMALL
IMPEDANCE
TRANSFORM
316
50 Ohm
PEAKING PA
304
Zhigh
e.g., 35 Ohm

FIG. 3

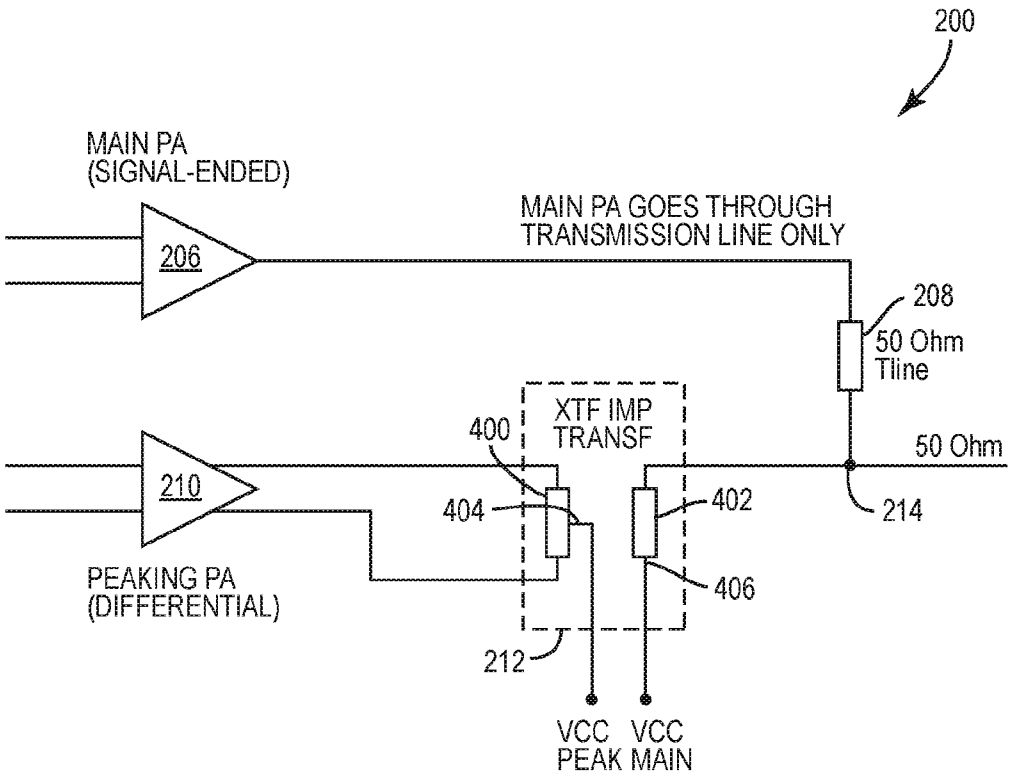
200
MAIN PA
(SIGNAL-ENDED)
206
MAIN PA GOES THROUGH
TRANSMISSION LINE ONLY
208
50 Ohm
Tline
XTF IMP
TRANSF
400
50 Ohm
210
404
402
214
406
PEAKING PA
(DIFFERENTIAL)
212
VCC
PEAK
VCC
MAIN

FIG. 4

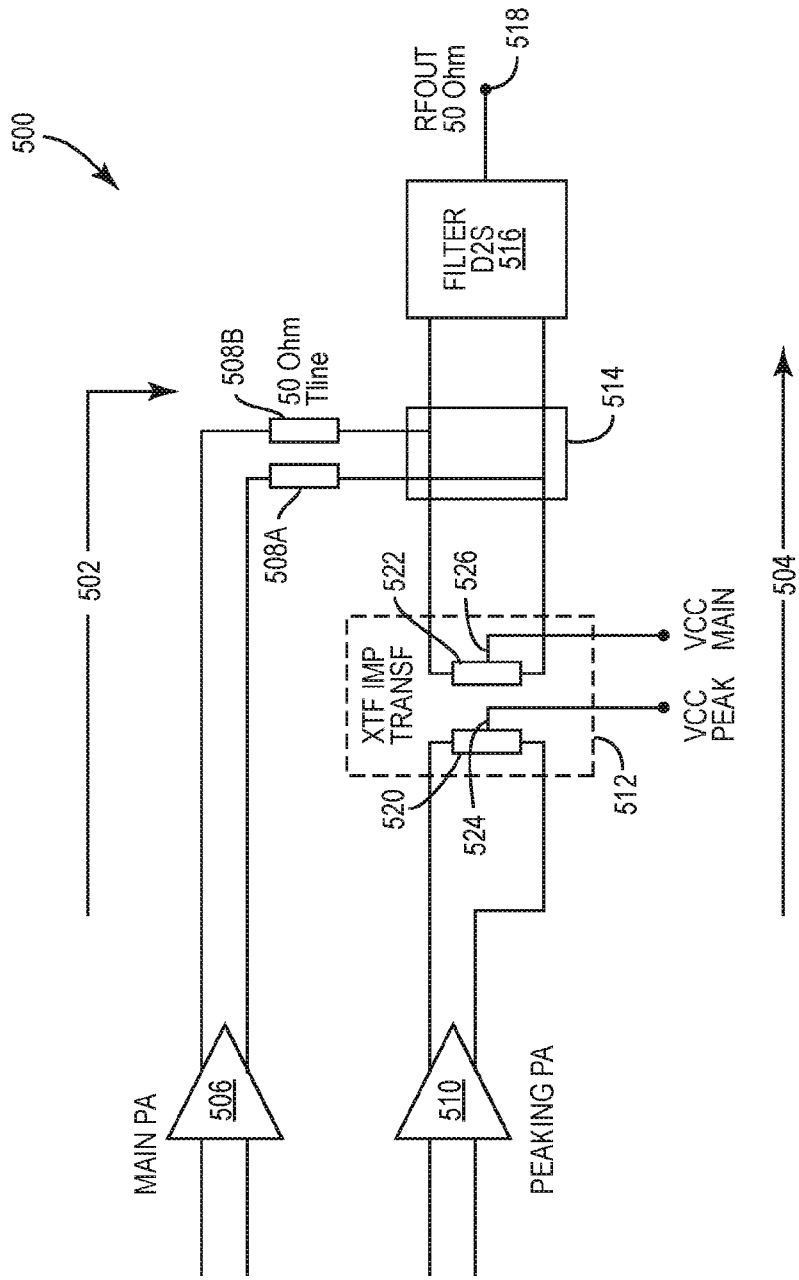
500
RFOUT
50 Ohm
518
FILTER
D2S
516
508B
50 Ohm
Tline
514
502
508A
522
526
XTF IMP
TRANSF
VCC
MAIN
504
VCC
PEAK
520
524
512
MAIN PA
506
510
PEAKING PA

FIG. 5

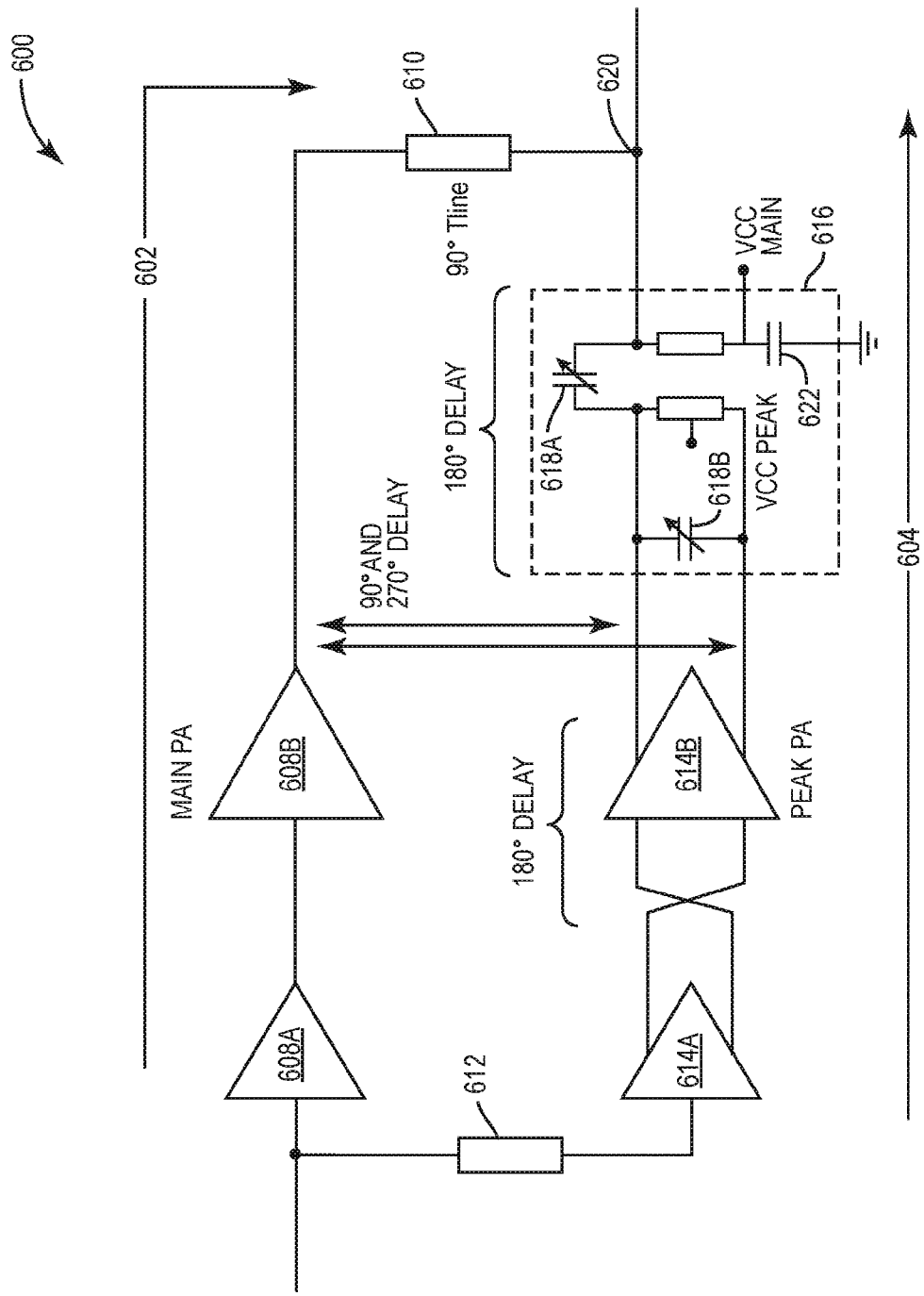
600
602
610
620
90° Tline
VCC MAIN
616
180° DELAY
618A
622
VCC PEAK
618B
90°AND 270° DELAY
604
MAIN PA
608B
614B
PEAK PA
180° DELAY
608A
614A
612

FIG. 6

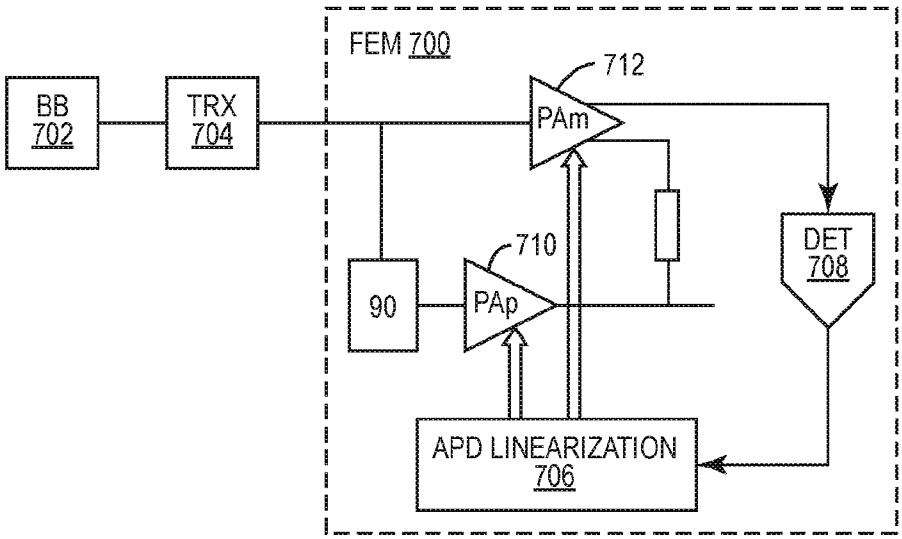
FEM 700
712
BB
702
TRX
704
PAm
DET
708
710
90
PAp
APD LINEARIZATION
706

FIG. 7

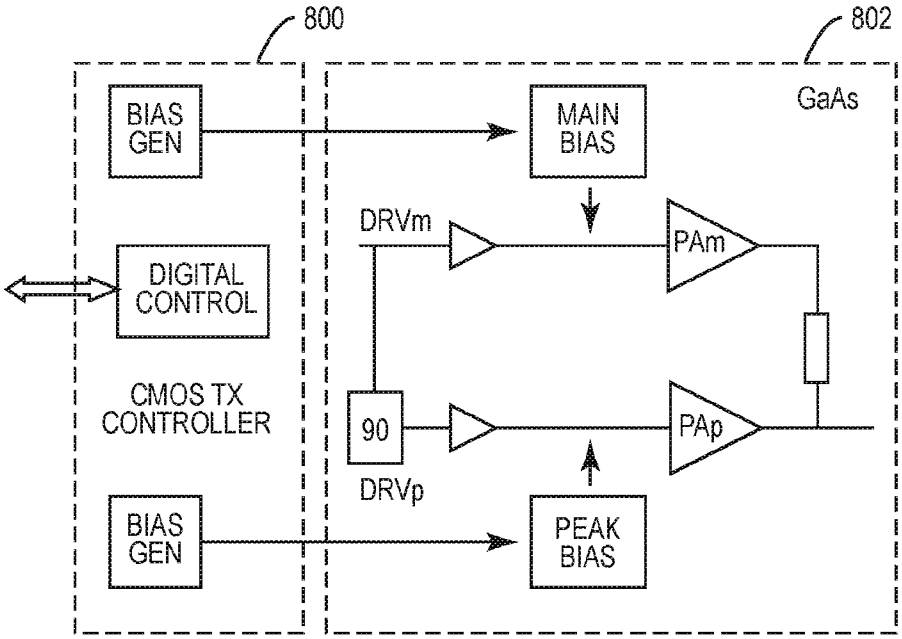
800
802
GaAs
BIAS GEN
MAIN BIAS
DRVm
PAm
DIGITAL CONTROL
CMOS TX CONTROLLER
90
PAp
DRVp
BIAS GEN
PEAK BIAS

FIG. 8

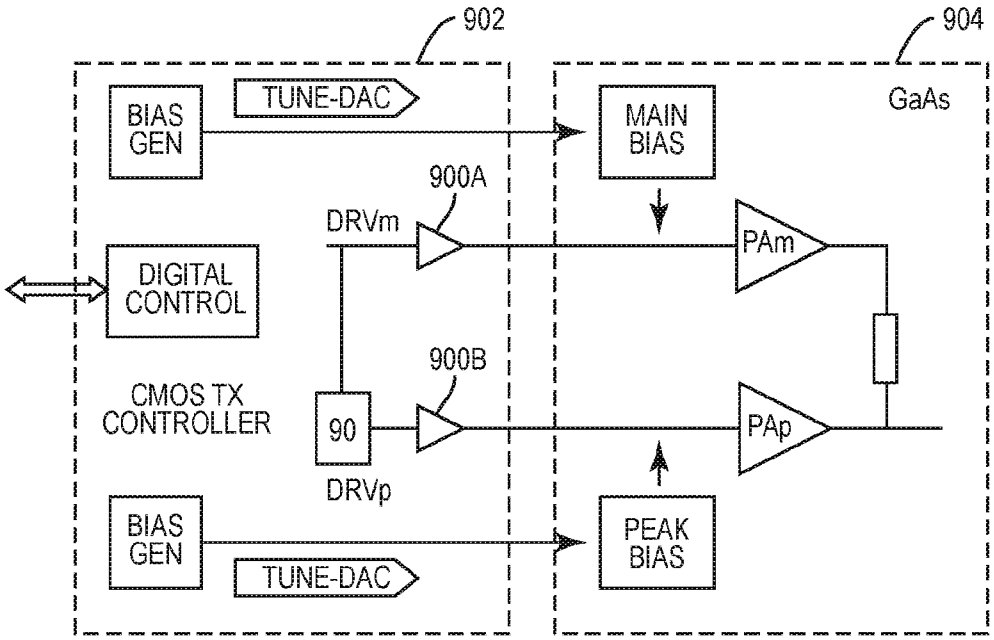
902
904
GaAs
BIAS GEN
TUNE-DAC
MAIN BIAS
900A
DRVm
PAm
DIGITAL CONTROL
900B
CMOS TX CONTROLLER
90
PAp
DRVp
BIAS GEN
TUNE-DAC
PEAK BIAS

FIG. 9

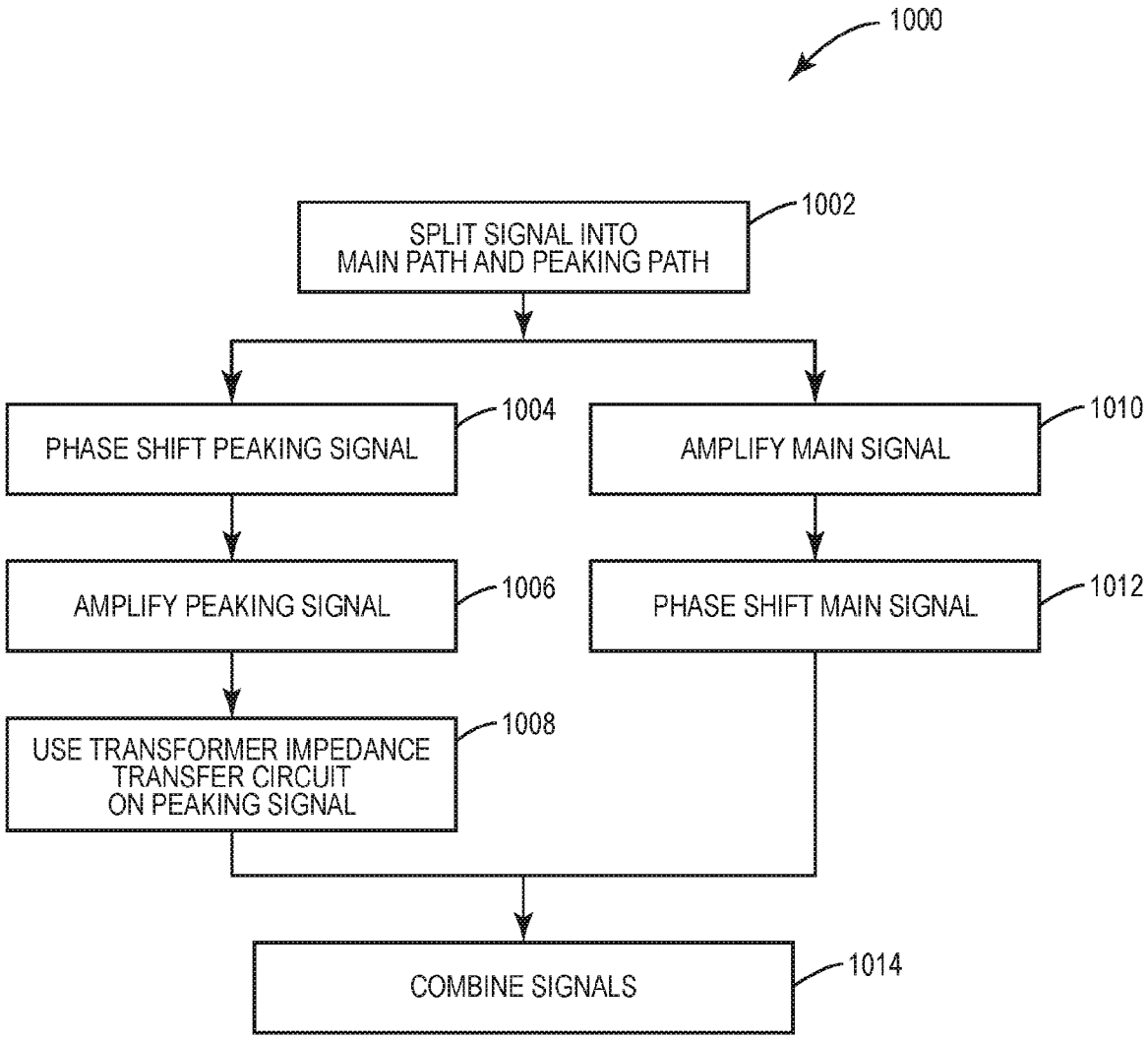
1000
SPLIT SIGNAL INTO MAIN PATH AND PEAKING PATH
1002
PHASE SHIFT PEAKING SIGNAL
1004
AMPLIFY PEAKING SIGNAL
1006
USE TRANSFORMER IMPEDANCE TRANSFER CIRCUIT ON PEAKING SIGNAL
1008
AMPLIFY MAIN SIGNAL
1010
PHASE SHIFT MAIN SIGNAL
1012
COMBINE SIGNALS
1014

FIG. 10

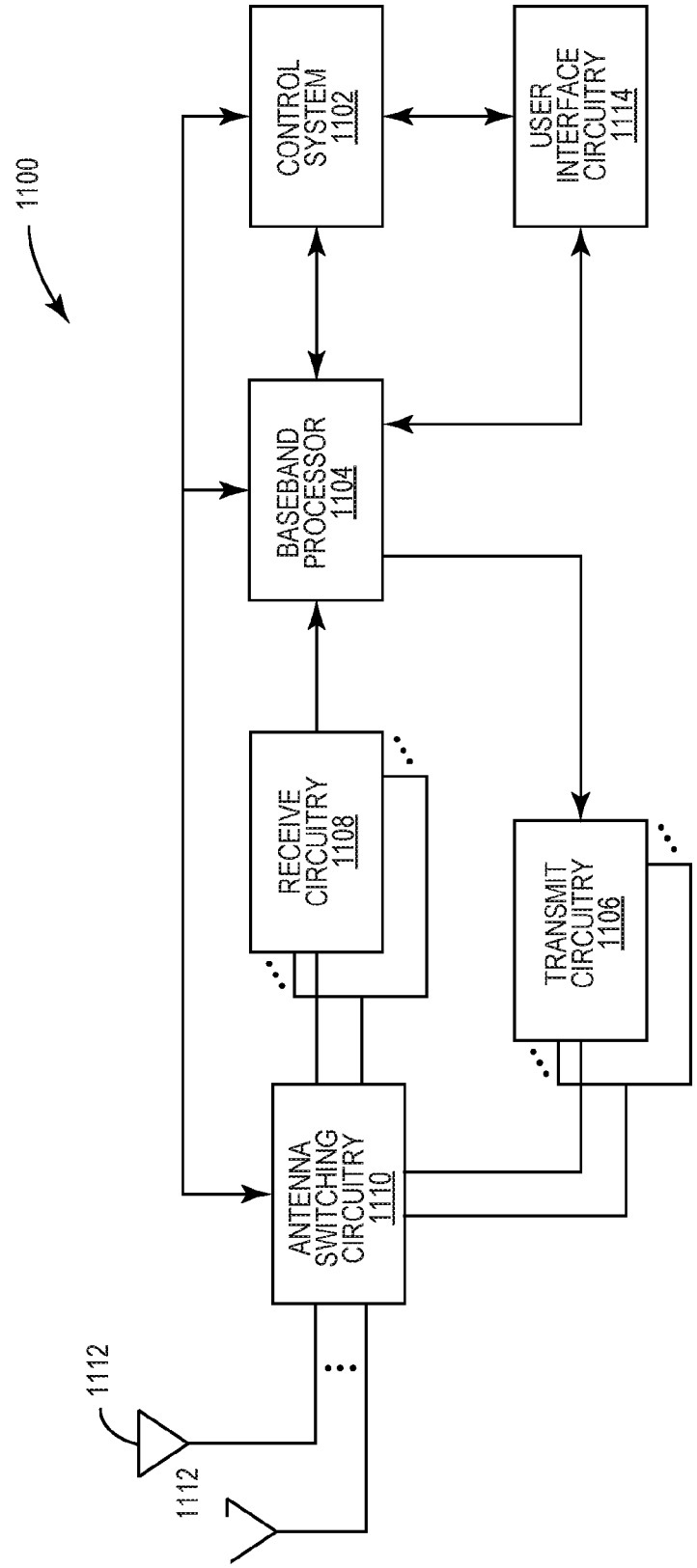
1100
CONTROL SYSTEM 1102
USER INTERFACE CIRCUITRY 1114
BASEBAND PROCESSOR 1104
RECEIVE CIRCUITRY 1108
TRANSMIT CIRCUITRY 1106
ANTENNA SWITCHING CIRCUITRY 1110
1112
1112

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2024/056463

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03F1/02 H03F1/42
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2018/006612 A1 (VAN DER HEIJDEN MARK PIETER [NL] ET AL) 4 January 2018 (2018-01-04) figures 1-4 paragraphs [0001] - [0090], [0124] -----	1-8, 16-20
X	US 10 050 588 B2 (NXP BV [NL]) 14 August 2018 (2018-08-14) figures 1-2 column 1, line 1 - column 6, line 55 -----	1-8, 16-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 February 2025	11/04/2025

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Jespers, Michaël

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2024/056463

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims;; it is covered by claims Nos.:
1-8, 16-20

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2024/056463

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2018006612 A1	04-01-2018	CN 107565909 A	09-01-2018
		EP 3264595 A1	03-01-2018
		US 2018006612 A1	04-01-2018
US 10050588 B2	14-08-2018	CN 107565908 A	09-01-2018
		EP 3264597 A1	03-01-2018
		US 2018006611 A1	04-01-2018

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-8, 16-20

   Broadband Doherty implementation

   ---

2. claims: 9-15

   Doherty tuning
