



(51) International Patent Classification:

H01Q 1/38 (2006.01) *H01Q* 3/01 (2006.01)
H01Q 7/00 (2006.01) *H01Q* 13/10 (2006.01)

(21) International Application Number:

PCT/SG2010/000029

(22) International Filing Date:

29 January 2010 (29.01.2010)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

200900658-6 30 January 2009 (30.01.2009) SG
200900659-4 30 January 2009 (30.01.2009) SG

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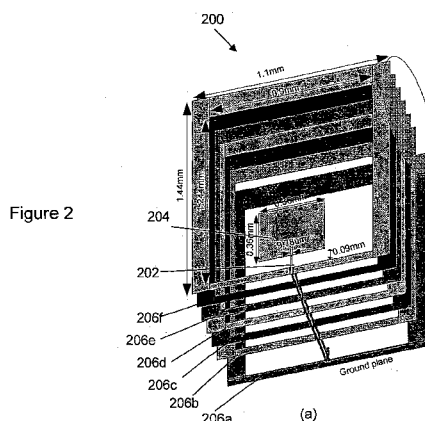
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: AN ANTENNA AND METHOD FOR MANUFACTURING THE SAME



(57) Abstract: An antenna and method for manufacturing the same. The antenna comprises a plurality of metal layers separated from each other by respective dielectric layers wherein a bottom metal layer comprises a closed loop while remaining metal layers comprise open loops; the plurality of metal layers being connected by respective vias; a feed line terminating in a stub in a top metal layer and disposed in an area defined by the loops; a bulk silicon layer disposed below the plurality of metal layers; and a mass ground layer disposed below the bulk silicon layer.

AN ANTENNA AND METHOD FOR MANUFACTURING THE SAME

FIELD OF INVENTION

The present invention relates broadly to an antenna and method for manufacturing the same.

BACKGROUND

Recently, 7 Gigahertz (GHz) of unlicensed bandwidth around 60GHz was opened allowing for a variety of applications including Gigabit per second (Gb/s) point-to-point links, extremely high-capacity wireless local area networks, and vehicular radar at nearby frequencies. Presently, the exploitation of this frequency band is minimal because of the high cost of the compound semiconductor technology needed to process the millimetre (mm)-wave signals, i.e. electromagnetic waves having wavelengths in the millimetre range. However, with the improved high-frequency capabilities of the Complementary Metal Oxide Semiconductor (CMOS) technology, low-cost radio solutions operating at this frequency band are beginning to appear. Although mm-wave CMOS circuits have been demonstrated, the design of an integrated chip antenna is still a bottleneck of the overall transceiver design.

A major problem encountered in on-chip antennas is signal loss. One possible reason is that the CMOS substrate usually has low resistivity, e.g. in the region of ≈ 10 Ohm-centimetre ($\Omega\cdot\text{cm}$), and high permittivity (e.g. $\epsilon_r \approx 12$). In addition, the standard CMOS process often involves a very thin substrate ($\approx 200\mu\text{m} \ll \lambda_g/10$ for antenna implementation). Thus, the use of such thin substrate for on-chip antenna implementation can result in poor radiation property in the broadside and bad impedance bandwidth.

Figure 1 shows a diagram (not to scale) illustrating the effect of an image current on the radiation transmitted. Here, for ease of illustration, the substrate has

been omitted and its effect on the radiation ignored. As can be seen from Figure 1, a current J flows from left to right above a ground plane. In the presence of the ground plane, an oppositely charged image current J_{image} is induced and located at a distance below the ground plane that is equal to the distance from the current J to the ground plane. The oppositely charged image current J_{image} , which represents the reflected path of the wave from the ground plane, can destructively interfere with the directed wave before it reaches a receiving point P , resulting in low gain and multiple nulls in the broadside.

To solve the above problem, one prior art approach proposes increasing the substrate thickness in order to improve the broadside radiation pattern. Another prior art approach proposes adopting a silicon lens at the backside of the chip. However, in doing so, special shaping of the bulk silicon substrate into a convex lens is needed in order to ensure constructive interference of the wave at the backside of the chip. Thus, such approaches may inadvertently increase the overall process fabrication cost.

Other prior art approaches include using a metallic reflector placed at some distance away (typically a quarter of a wavelength) so as to improve the broadside radiation, adopting a high dielectric constant for efficient radiation, and using suspended dipole or monopole-base antennas. However, with the presence of the metallic plate, it is very difficult to miniaturize the overall chipset. The electromagnetic compatibility (EMC) decoupling between the antenna and circuitries may be reduced. Furthermore, the backside ground is generally needed in most of the integrated circuits so as to have an efficient die-attachment to other circuitries. Thus, the typical monopole-based antenna design is no longer attractive using CMOS technology.

A need therefore exists to provide an antenna and method for manufacturing the same that seek to address at least one of the above problems.

SUMMARY

In accordance with a first aspect of the present invention, there is provided an antenna comprising:

- a plurality of metal layers separated from each other by respective dielectric layers wherein a bottom metal layer comprises a closed loop while remaining metal layers comprise open loops; the plurality of metal layers being connected by respective vias;

- a feed line terminating in a stub in a top metal layer and disposed in an area defined by the loops;

- a bulk silicon layer disposed below the plurality of metal layers; and

- a mass ground layer disposed below the bulk silicon layer.

The plurality of metal layers alternately may comprise parallel wires or an artificial magnetic conductor structure respectively disposed in the area defined by the loops, excluding the top metal layer.

Each layer of the artificial magnetic conductor structure may comprise rows of C-shaped elements.

Each of the C-shaped elements may be positioned symmetrically opposite to an adjacent C-shaped element on the same row.

Each of the C-shaped elements may be separately coupled to a wire directly below said layer of the artificial magnetic conductor structure.

Each of the plurality of metal layers, excluding the top metal layer, may comprise parallel strips disposed in the area defined by the loops such that an inclined artificial magnetic conductor structure may be formed.

The number of parallel strips may increase sequentially from an upper metal layer to a lower metal layer for forming an inclined artificial magnetic conductor structure.

The stub may be substantially rectangular.

The stub may be open-circuited.

The antenna may further comprise a second stub in an intermediate metal layer and disposed in an area defined by the loops.

The second stub may comprise substantially the same shape as the first stub.

The second stub may be connected to the first stub by one or more vias.

The bulk silicon layer may be a CMOS substrate.

A substantially large portion of the bulk silicon layer and the mass ground layer in the area defined by the loops may be removed.

The antenna may be configured to operate at a frequency band around 60 GHz.

In accordance with a second aspect of the present invention, there is provided a method for manufacturing an antenna, the method comprising the steps of:

- forming a mass ground layer on a CMOS substrate;
- forming a bulk silicon layer above the mass ground layer;
- forming a plurality of metal layers above the bulk silicon layer and separated from each other by respective dielectric layers wherein a bottom metal layer comprises a closed loop while remaining metal layers comprise open loops; the plurality of metal layers being connected by respective vias; and
- forming a feed line terminating in a stub in a top metal layer and disposed in an area defined by the loops;

The forming of the plurality of metal layers further may comprise forming parallel wires or an artificial magnetic conductor structure respectively in the area defined by the loops, excluding the top metal layer.

The forming of the plurality of metal layers may further comprise forming parallel strips in the area defined by the loops in each of the plurality of metal layers, excluding the top metal layer, for forming an inclined artificial magnetic conductor structure.

The method may further comprise removing a substantially large portion of the bulk silicon layer and the mass ground layer in the area defined by the loops.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 shows a diagram (not to scale) illustrating the effect of an image current on the radiation transmitted.

Figure 2(a) shows a perspective view of an antenna according to an example embodiment.

Figure 2(b) shows a partial sectional view of the layers of the antenna of Figure 2(a).

Figure 3 shows graphs comparing loss responses of the antenna of Figure 2(a) with an etched hole on the ground plane and one with a full ground plane based on simulation results.

Figure 4 shows graphs comparing gains of the antenna of Figure 2(a) with an etched hole on the ground plane and one with a full ground plane based on simulation results.

Figure 5(a) shows a perspective view of an improved antenna based on the antenna of Figure 2(a) according to an example embodiment.

Figure 5(b) shows an enlarged perspective view of a physical unit cell of the antenna of Figure 5(a).

Figure 5(c) shows a diagram (not to scale) illustrating the improvement in the antenna of Figure 5(a).

Figure 6 shows a graph illustrating the loss response of the antenna of Figure 5(a) based on simulation results.

Figure 7 shows a graph illustrating the gain response of the antenna of Figure 5(a) based on simulation results.

Figure 8 shows graphs illustrating electric (E) and magnetizing (H)-plane radiation patterns of the antenna of Figure 5(a) based on simulation results.

Figure 9 shows an image of the antenna of Figure 5(a) as fabricated according to an example embodiment.

Figure 10 shows a graph of return loss of the antenna of Figure 9 backed by a full ground carrier based on measured results.

Figure 11 shows an image of an experiment set-up for measuring peak gain of the fabricated antenna of Figure 9 according to an example embodiment.

Figure 12(a) shows a perspective view of an antenna according to an alternate embodiment.

Figure 12(b) shows a partial sectional view of the layers of the antenna of Figure 12(a).

Figure 13 shows graphs comparing loss responses of the antenna of Figure 12(a) with an etched hole on the ground plane and one with a full ground plane based on simulation results.

Figure 14 shows graphs comparing gains of the antenna of Figure 12(a) with an etched hole on the ground plane and one with a full ground plane based on simulation results.

Figure 15(a) shows a perspective view of an improved antenna based on the antenna of Figure 12(a) according to an example embodiment.

Figure 15(b) shows an enlarged perspective view of an area defined by the metal layers of the antenna of Figure 15(a).

Figure 15(c) shows a diagram (not to scale) illustrating the improvement in the antenna of Figure 15(a).

Figure 16 shows a graph illustrating the loss response of the antenna of Figure 15(a) based on simulation results.

Figure 17 shows a graph illustrating the gain response of the antenna of Figure 15(a) based on simulation results.

Figure 18 shows graphs illustrating electric (E) and magnetizing (H)-plane radiation patterns of the antenna of Figure 15(a) based on simulation results.

Figure 19 shows an image of the antenna of Figure 15(a) as fabricated according to an example embodiment.

Figure 20 shows a graph of return loss of the antenna of Figure 19 backed by a full ground carrier based on measured results.

Figure 21 shows an image of an experiment set-up for measuring peak gain of the fabricated antenna of Figure 19 according to an example embodiment.

Figure 22 shows a flow chart illustrating a method for manufacturing an antenna according to an example embodiment.

DETAILED DESCRIPTION

Figure 2(a) shows a perspective view of an antenna 200 according to an example embodiment. Figure 2(b) shows a partial sectional view of the layers of the antenna 200 of Figure 2(a).

A 50Ω coplanar feed line 202, which is designed to work at about 60GHz and used to excite the antenna 200 in the example embodiment, is terminated with an extended tap-stub 204 so as to preferably give a good matching for frequencies between 54.4GHz to 67.6GHz in the absence of a mass (or bulk) ground plane. As can be seen from Figure 2(a), the width of the feed line 202 is about 9.78 micrometres (μm), while the size of the tap-stub 204 is about 0.36mm x 0.36mm in the example embodiment. Also, as the example embodiment seeks to implement an antenna that consumes as small an estate area as possible, a finite ground-plane coplanar waveguide (also known as grounded coplanar waveguide) is limited to a finite ground width of about $0.02\lambda_0$, or 0.1 mm, in the example embodiment. Preferably, the whole antenna 200 is restricted to an area of about 1.44mm by 1.1mm footprint as shown in Figure 2(a).

In addition, in the example embodiment, a plurality of connected rings are provided within the perimeter of the antenna 200 to form a cavity for confining the wave. Here, as can be seen in Figure 2(b), the connected rings comprise six metal

layers 206a-f separated by respective dielectric layers 208. It will be appreciated that the number and thickness of the metal layers 206 and respective dielectric layers 208 may vary depending factors such as the type of CMOS process used. For example, the thickness of metal layers 206a-e is about 0.594 μm , while the thickness of metal layer 206f is about 2.15 μm in the example embodiment. The width of the metal layers 206a-f is about 0.1 mm (i.e. about $0.02\lambda_0$) as explained above. Further, in the example embodiment, four vertical vias (not shown) at the feed-end (i.e. ends of the metal layers 206 adjacent to the feed line 202) are inserted to ensure that the dominant mode is being propagated into the extended tap-stub 204.

Also, as can be seen from Figure 2(b), a bulk silicon layer 210 is disposed below the plurality of metal layers 206, and a mass ground layer 212 is disposed below the bulk silicon layer 210 in the example embodiment.

In a simulated analysis, a substantially big hole is etched at the center of the mass ground plane of the antenna 200 to remove the ground image current effect. The performance of modified antenna is then compared with one having a full mass ground plane using commercial simulation software, e.g. IE3D from Zeland Software, Inc. in the example embodiment.

Figure 3 shows graphs comparing loss responses of the antenna of Figure 2(a) with an etched hole on the ground plane and one with a full mass ground plane based on simulation results. Figure 4 shows graphs comparing gains of the antenna of Figure 2(a) with an etched hole on the mass ground plane and one with a full mass ground plane based on simulation results. In Figures 3 and 4, the antenna with an etched hole on the mass ground plane are represented by lines 302 and 402 respectively, while the antenna with a full mass ground plane are represented by lines 304 and 404 respectively. As can be seen in Figures 3 and 4, the antenna with the full main ground plane is operative, with a somewhat narrow bandwidth and low gain. On the other hand, the antenna with an etched hole on the mass ground plane has significantly improved impedance bandwidth and gain performance. For example, the trough of line 302 is relatively wide while the trough of line 304 is

relatively narrow. Also, the simulated gain shown by line 402 is 3.8dBi as compared to -7dBi shown by line 404 at 58.29GHz.

Figure 5(a) shows a perspective view of an improved antenna 500 based on the antenna of Figure 2(a) according to an example embodiment. Figure 5(b) shows an enlarged perspective view of a physical unit cell 510 of the antenna 500 of Figure 5(a). Figure 5(c) shows a diagram (not to scale) illustrating the improvement in the antenna 500 of Figure 5(a).

In Figure 5(a), the feed line 202, tap-stub 204 and metal layers 206a-f of the antenna 500 are the same as those described above with respect to the antenna 200 of Figure 2(a). In addition, alternate layers of an artificial magnetic conductor (AMC) 502 and thin wires 504 are disposed in the cavity defined by the metal layers 206. For example, the thin wires 504 are provided adjacent to metal layer 206a, while the AMC 502 is provided adjacent to metal layer 206b in the example embodiment. The alternating pattern is repeated for the remaining layers 206c-206f. Typically, the AMC 502 is also known as high impedance surface or frequency selective surface, among other names as understood by a person skilled in the art, and generally comprises an electromagnetic band gap material. In the description, the term AMC is used interchangeably with the term perfect magnetic conductor (PMC).

In the example embodiment, each unit cell 510 comprises two C-shaped AMC elements 502 faced oppositely and separately coupled to a thin wire 504 placed directly below the respective layer. The size of each C-shaped element 502 is about $45\ \mu\text{m} \times 55\ \mu\text{m}$. The width of the AMC in each C-shaped element 502 is about $10\ \mu\text{m}$. The separation between the two adjacent and opposite C-shaped elements 502 is about $5\ \mu\text{m}$. In the example embodiment, the width of the thin wire 504 is also about $5\ \mu\text{m}$ while the thickness of the thin wire 504 is the same as the thickness of the metal layer, i.e. $0.594\ \mu\text{m}$. As can be seen from Figure 5(a), the unit cell 510 is repeated throughout the metal layers 206a-f. It will be appreciated that the AMC elements 502 can have other shapes and dimensions in alternate embodiments.

Referring to Figure 5(c), for a current J flowing from left to right, in the presence of the AMC, a current KJ is induced between the AMC and ground plane, having the same flow direction as current J . As a result, two image currents J_{image} and KJ_{image} are induced below the ground plane due to ground plane effect, and which in turn, induce image currents KJ_{image} and K^2J_{image} respectively above the ground plane. Further image currents (not shown) with diminishing magnitudes may be induced above and below the ground plane such that the effects of the image currents advantageously cancel out one another, thereby substantially reducing destructive interference. That is, the image currents can in turn re-enhance the radiation pattern in the broadside even though the substrate thickness may be very thin. In doing so, the counter-effect of the ground plane can be advantageously minimized.

Figure 6 shows a graph illustrating the loss response of the antenna of Figure 5(a) based on simulation results. Figure 7 shows a graph illustrating the gain response of the antenna of Figure 5(a) based on simulation results. Comparing Figures 6 and 3, it can be seen that the antenna 500 having an artificial magnetic conductor inserted (Figure 6) can retain substantially the same bandwidth as one without the AMC (Figure 3). In addition, as shown in Figure 7, there is a significant improvement in the overall antenna gain with a maximum gain of about 3.75dBi occurring at 61.09GHz, as compared to the gain of the antenna without AMC and with a full mass ground plane.

Figure 8 shows graphs illustrating electric (E) and magnetizing (H)-plane radiation patterns of the antenna of Figure 5(a) based on simulation results. In Figure 8, the E-plane radiation pattern is represented by line 802 while the H-plane radiation pattern is represented by line 804.

Figure 9 shows an image of the antenna 500 of Figure 5(a) as fabricated according to an example embodiment. The feed line 202, tap-stub 204 and C-shaped elements 502 can be seen in Figure 9. The fabricated antenna 500 is next die-attached onto a gold carrier and measured by an analyzer, e.g. a 110GHz vector network analyzer 37000D series from Anritsu Corporation.

Figure 10 shows a graph of return loss of the antenna of Figure 9 backed by a full ground carrier based on measured results. As can be seen from Figure 10, an ultra-broadband impedance bandwidth of about 126%, ranging from 15GHz to 66GHz has been achieved in the example embodiment. In addition, there is a broadening of the bandwidth as compared to Figure 6 which is mainly due to the fact that the losses in the substrate have not been taken into consideration for the simulation results given in Figures 3 and 6. Moreover, in the simulation, it is assumed that the metal thickness is infinitely thin so as to speed-up the computational time.

The inventors have also measured the gain of the fabricated antenna of Figure 9. Figure 11 shows an image of an experiment set-up for measuring peak gain of the fabricated antenna of Figure 9 according to an example embodiment. For the ease of demonstration, the box absorbers surrounding the probes, the cables, horn antenna and the chip-set have been removed in the example embodiment. Proper antenna calibrations inclusive of the cables are first performed using the same set-up. The measured gain at 60GHz is found to be about 2dBi in the example embodiment.

Figure 12(a) shows a perspective view of an antenna 1200 according to an alternate embodiment. Figure 12(b) shows a partial sectional view of the layers of the antenna 1200 of Figure 12(a).

Similar to the antenna 200 of Figure 2, the antenna 1200 of Figure 12(a) can be considered a wide-slot squared antenna. A 50Ω coplanar feed line 1202, which is designed to work at about 60GHz in the example embodiment, is used to excite the wide-slot squared antenna 1200 through an open-circuited stub 1204. In the example embodiment, the stub 1204 comprises a main section that is substantially a rectangle with two corners removed, and four substantially narrow corner extensions extending in a direction parallel to the length of the stub, thus resembling a traditional Chinese hat. As can be seen in Figure 12(a), the overall dimension of the main section is about 0.45mm x 0.24 mm, while the width of the extensions is about 9 μ m. The particular design of the stub 1204 in the example embodiment can advantageously achieve greater broadband and can be more robust to dimensional

variations. However, it will be appreciated that different shapes and dimensions can be used for the stub 1204 in alternate embodiments, for example, the stub 204 of Figure 2.

In the example embodiment, to achieve a better matching between 57.5GHz and 66GHz, in the example embodiment, an additional stub 1214 having the same shape as the stub 1204 is duplicated onto an intermediate metal layer (to be described in more detail below). The stubs 1204 and 1214 are connected through a via. Also, as the example embodiment seeks to implement an antenna that occupies as small an estate area as possible, a coplanar ground plane is limited to a finite ground width of about $0.02\lambda_0$ in the example embodiment. Preferably, the whole antenna 1200 is restricted to an area of about 1.3mm by 1.1mm footprint as shown in Figure 12(a).

In addition, in the example embodiment, a plurality of connected rings are provided within the perimeter of the antenna 1200 to form a cavity for confining the wave. Here, as can be seen in Figure 12(b), the connected rings comprise nine metal layers 1206 (M1 to M9) separated by respective dielectric layers 1208. Also, as can be seen in the Figure 12(a), the intermediate metal layers (M2 to M8) form 3 sides of a rectangular loop. It will be appreciated that the number and thickness of the metal layers 1206 and respective dielectric layers 1208 may vary depending factors such as the type of CMOS process used. Further, in the example embodiment, four vertical vias 1210 that connect the rings together are inserted at the feed-end to ensure that the dominant mode is being propagated into the open-circuited stub 1204.

Similar to the antenna of Figure 2, a bulk silicon layer (not shown in Figure 12(b)) is disposed below the plurality of metal layers 1206, and a mass ground layer (not shown in Figure 12(b)) is disposed below the bulk silicon layer in the example embodiment.

In a simulated analysis, a substantially big hole is etched at the center of the mass ground plane of the antenna 1200 to remove the ground image current effect. The performance of modified antenna is then compared with one having a full mass

ground plane using commercial simulation software, e.g. IE3D from Zeland Software, Inc. in the example embodiment.

Figure 13 shows graphs comparing loss responses of the antenna of Figure 12(a) with an etched hole on the mass ground plane and one with a full mass ground plane based on simulation results. Figure 14 shows graphs comparing gains of the antenna of Figure 12(a) with an etched hole on the mass ground plane and one with a full mass ground plane based on simulation results. In Figures 13 and 14, the antenna with an etched hole on the mass ground plane are represented by lines 1302 and 1402 respectively, while the antenna with a full mass ground plane are represented by lines 1304 and 1404 respectively. As can be seen in Figures 13 and 14, the antenna with an etched hole on the mass ground plane has significantly improved impedance bandwidth and gain performance. For example, line 1302 has a relatively wide trough while line 1304 has a very small trough. Also, the simulated gain shown by line 1402 is 2.85dBi as compared to -37.02dBi shown by line 404.

Figure 15(a) shows a perspective view of an improved antenna 1500 based on the antenna 1200 of Figure 12(a) according to an example embodiment. Figure 15(b) shows an enlarged perspective view of an area 1510 defined by the metal layers of the antenna 1500 of Figure 15(a). Figure 15(c) shows a diagram (not to scale) illustrating the improvement in the antenna 1500 of Figure 15(a).

In Figure 15(a), the feed line 1202, stubs 1204, 1214 and metal layers 1206 of the antenna 1500 are the substantially same as those described above with respect to the antenna 1200 of Figure 2(a). In addition, a plurality of artificial magnetic conductors (AMC) are disposed in the cavity formed by the metal layers 1206. In the example embodiment, the AMC comprise straight planar lines 1502 extending from side 1504 to side 1506 of the metal layers 1206. Further, as can be seen in Figure 15(a) and 15(b), the planar lines 1502 are aligned in a staircase manner so as to emulate an inclined artificial magnetic conductor (to be discussed in details below), i.e. the number of planar lines 1502 increases sequentially from the top metal layer to the bottom metal layer. The width of each planar line 1502 is about 34 μm and the separation between two adjacent lines on the same plane is

also about 34 μm in the example embodiment. It should be appreciated that different width and separation values can be used in alternate embodiments.

Referring to Figure 15(c), in the absence of the bulk substrate and the presence of the artificial magnetic conductors defining an inclined surface at a predetermined angle θ , a pluralities of image currents J_{image} , KJ_{image} , K^2J_{image} , etc appearing above and below the axes $z=0$ and $v=0$ are formed. Some of the image currents cancel out one another in the example embodiment, resulting in a re-enhancement of the broadside radiation even though the substrate thickness may be substantially very thin. That is, the counter-effect of the ground plane can be advantageously minimized.

Figure 16 shows a graph illustrating the loss response of the antenna of Figure 15(a) based on simulation results. Figure 17 shows a graph illustrating the gain response of the antenna of Figure 15(a) based on simulation results. Comparing Figs. 16 and 13, it can be noted that the antenna having the artificial magnetic conductors inserted (Figure 16) can retain about the same bandwidth as one without the AMC (Figure 13). In addition, as shown in Figure 17, there is no degradation in the overall antenna gain by having the AMC inserted.

Figure 18 shows graphs illustrating electric (E) and magnetizing (H)-plane radiation patterns of the antenna 1500 of Figure 15(a) based on simulation results. In Figure 8, the E-plane radiation pattern is represented by line 1802 while the H-plane radiation pattern is represented by line 1804.

Figure 19 shows an image of the antenna 1500 of Figure 15(a) as fabricated according to an example embodiment. The feed line 1202, stub 1204 and AMC planar lines 1502 can be seen in Figure 19. In the example embodiment, there are 3 planar lines 1502 adjacent to the top metal layer. As described above, the number of planar lines 1502 (or strips) increases sequentially from the top metal layer to the bottom metal layer such that an inclined artificial magnetic conductor is emulated in the example embodiment. It can also be seen from Figure 19 that the planar lines 1502 are not in physical contact with the metal layers. The fabricated antenna 1500

is next die-attached onto a gold carrier and measured by an Anritsu 110GHz network analyzer, similar to the one described above.

Figure 20 shows a graph of return loss of the antenna of Figure 19 backed by a full ground carrier based on measured results. As can be seen in Figure 20, except for the high-frequency bandwidth broadening, the measured response is, in general, very similar to the simulated response given in Figure 16 even though the whole antenna is now die-attached to a flat gold carrier. As compared to Figure 16, the broadening of the bandwidth is mainly due to the fact that the losses in the substrate have not been taken into the consideration for the simulation results given in Figures 13 and 16. Overall, the observed bandwidth is found to be much larger than 116% in the example embodiment.

The inventors have also measured peak gain of the fabricated antenna of Figure 19. Figure 21 shows an image of an experiment set-up for measuring peak gain of the fabricated antenna of Figure 19 according to an example embodiment. For ease of illustration, the box absorber surrounding the probes, the horn antenna and the chip-set are removed in Figure 21. A proper calibration is first conducted to remove the effect of the cables and probes. The measured gain at 60GHz is found to be 2dBi in the example embodiment.

Thus described above are embodiments of an integrated antenna that is suitable in compact and conductive environment or substrates. Such CMOS on-chip antenna can be implemented as magnetic-dipole or loop antenna. In addition, broadband can be realized in the example embodiments by wide-slot design, which may alleviate the need to use suspended dipole-based or monopole-based antenna technique. In the example embodiments, the $\frac{1}{4}$ wavelength reflector requirement is advantageously removed by perfect magnetic conductor (PMC), i.e. artificial magnetic conductor, placement, which can lead to greater level of miniaturization. Also, the conductive metal layer is used as perfect electric conductor (PEC) to provide good EMC grounding, which can preserve broad impedance bandwidth and free estate area below the on-chip antenna for other integrated circuit design. The CMOS multi-layer features advantageously create options for efficient miniaturization implementation. Furthermore, the many ways of implementing PMC

and integration can further lead to efficient elimination of the ground image current, i.e. a new solution for removing ground image current while preserving efficient radiation. The example embodiments also show one way of integrating an artificial magnetic conductor in standard 0.18 μm CMOS technology, all compacted within a small area of about 1.4 mm by 1.1 mm.

Further to the above, it should be appreciated that the example embodiments advantageously make use of the conventional CMOS technology without any added fabrication treatment in the fabrication process. In addition, the antenna according to the example embodiments preferably has good electromagnetic compatibility as it is slot-based rather than coplanar-based. Thus, expensive substrate area beneath the antenna can be more fully utilized. Furthermore, the antenna of the example embodiments can advantageously have good impedance bandwidth and antenna gain while achieving significant miniaturization through differential feed topology.

Figure 22 shows a flow chart 2200 illustrating a method for manufacturing an antenna according to an example embodiment. At step 2202, a mass ground layer is formed on a CMOS substrate. At step 2204, a bulk silicon layer is formed above the mass ground layer. At step 2206, a plurality of metal layers are formed above the bulk silicon layer and separated from each other by respective dielectric layers wherein a bottom metal layer comprises a closed loop while remaining metal layers comprise open loops; the plurality of metal layers being connected by respective vias. At step 2208, a feed line terminating in a stub in a top metal layer and disposed in an area defined by the loops is formed.

It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

CLAIMS

1. An antenna comprising:
 - a plurality of metal layers separated from each other by respective dielectric layers wherein a bottom metal layer comprises a closed loop while remaining metal layers comprise open loops; the plurality of metal layers being connected by respective vias;
 - a feed line terminating in a stub in a top metal layer and disposed in an area defined by the loops;
 - a bulk silicon layer disposed below the plurality of metal layers; and
 - a mass ground layer disposed below the bulk silicon layer.
2. The antenna as claimed in claim 1, wherein the plurality of metal layers alternately comprise parallel wires or an artificial magnetic conductor structure respectively disposed in the area defined by the loops, excluding the top metal layer.
3. The antenna as claimed in claim 2, wherein each layer of the artificial magnetic conductor structure comprises rows of C-shaped elements.
4. The antenna as claimed in claim 3, wherein each of the C-shaped elements is positioned symmetrically opposite to an adjacent C-shaped element on the same row.
5. The antenna as claimed in claims 3 or 4, wherein each of the C-shaped elements is separately coupled to a wire directly below said layer of the artificial magnetic conductor structure.
6. The antenna as claimed in claim 1, wherein each of the plurality of metal layers, excluding the top metal layer, comprises parallel strips disposed in the area defined by the loops such that an inclined artificial magnetic conductor structure is formed.
7. The antenna as claimed in claim 6, wherein the number of parallel strips increases sequentially from an upper metal layer to a lower metal layer for forming an inclined artificial magnetic conductor structure.

8. The antenna as claimed in any one of the preceding claims, wherein the stub is substantially rectangular.

9. The antenna as claimed in any one of the preceding claims, wherein the stub is open-circuited.

10. The antenna as claimed in any one of the preceding claims, further comprising a second stub in an intermediate metal layer and disposed in an area defined by the loops.

11. The antenna as claimed in claim 10, wherein the second stub comprises substantially the same shape as the first stub.

12. The antenna as claimed in claims 10 or 11, wherein the second stub is connected to the first stub by one or more vias.

13. The antenna as claimed in any one of the preceding claims, wherein the bulk silicon layer is a CMOS substrate.

14. The antenna as claimed in any one of the preceding claims, wherein a substantially large portion of the bulk silicon layer and the mass ground layer in the area defined by the loops is removed.

15. The antenna as claimed in any one of the preceding claims, configured to operate at a frequency band around 60 GHz.

16. A method for manufacturing an antenna, the method comprising the steps of:

forming a mass ground layer on a CMOS substrate;

forming a bulk silicon layer above the mass ground layer;

forming a plurality of metal layers above the bulk silicon layer and separated from each other by respective dielectric layers wherein a bottom metal layer comprises a closed loop while remaining metal layers comprise open loops; the plurality of metal layers being connected by respective vias; and

forming a feed line terminating in a stub in a top metal layer and disposed in an area defined by the loops;

17. The method as claimed in claim 16, wherein the forming of the plurality of metal layers further comprises forming parallel wires or an artificial magnetic conductor structure respectively in the area defined by the loops, excluding the top metal layer.

18. The method as claimed in claim 16, wherein the forming of the plurality of metal layers further comprises forming parallel strips in the area defined by the loops in each of the plurality of metal layers, excluding the top metal layer, for forming an inclined artificial magnetic conductor structure.

19. The method as claimed in any one of claims 16 to 18, further comprising removing a substantially large portion of the bulk silicon layer and the mass ground layer in the area defined by the loops.

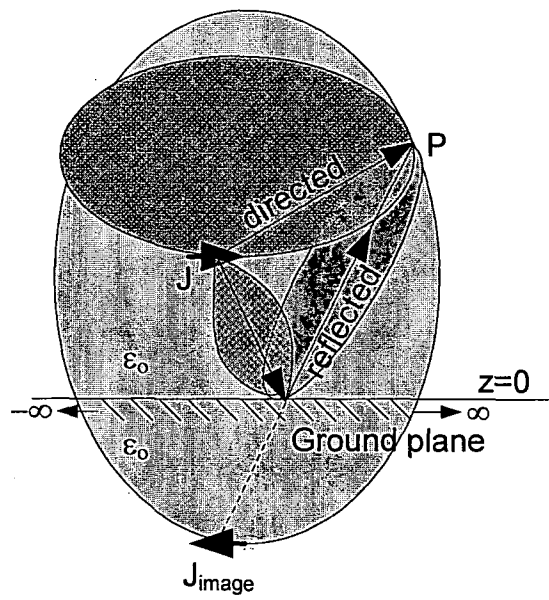


Figure 1
(PRIOR ART)

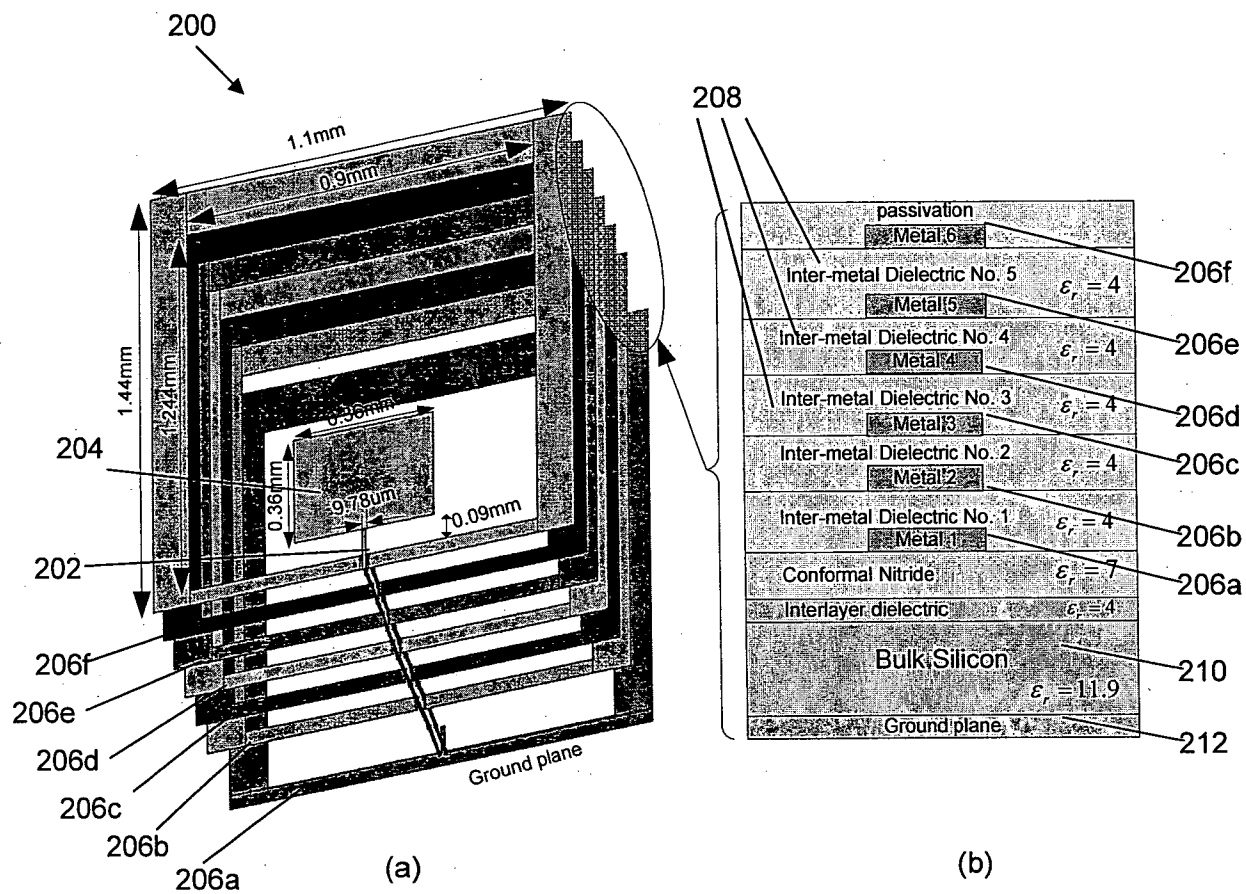


Figure 2

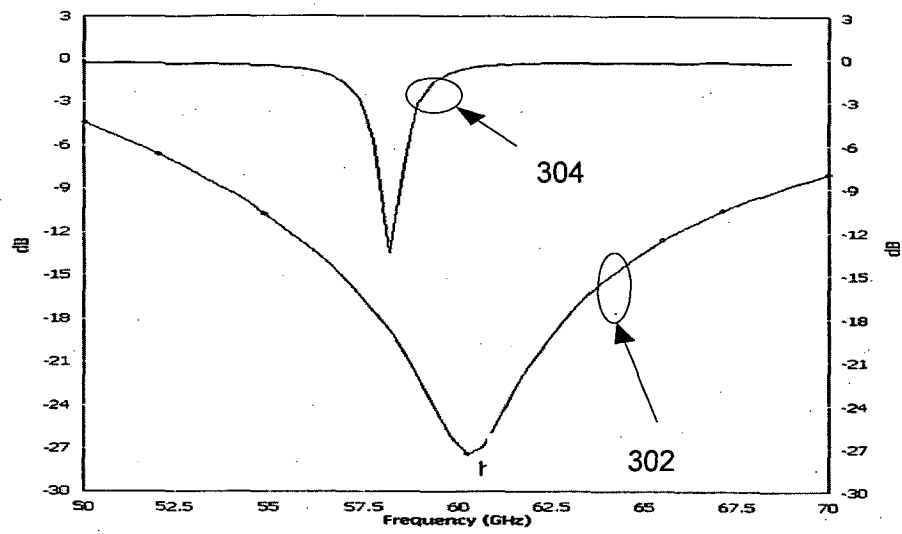


Figure 3

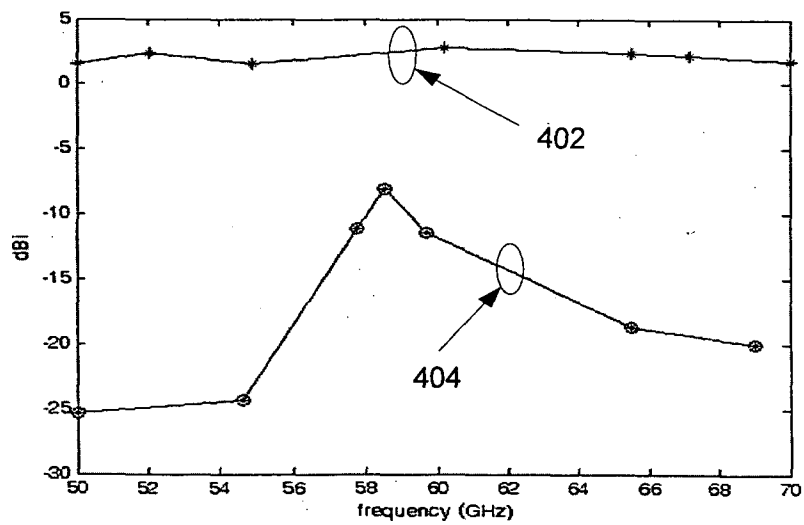


Figure 4

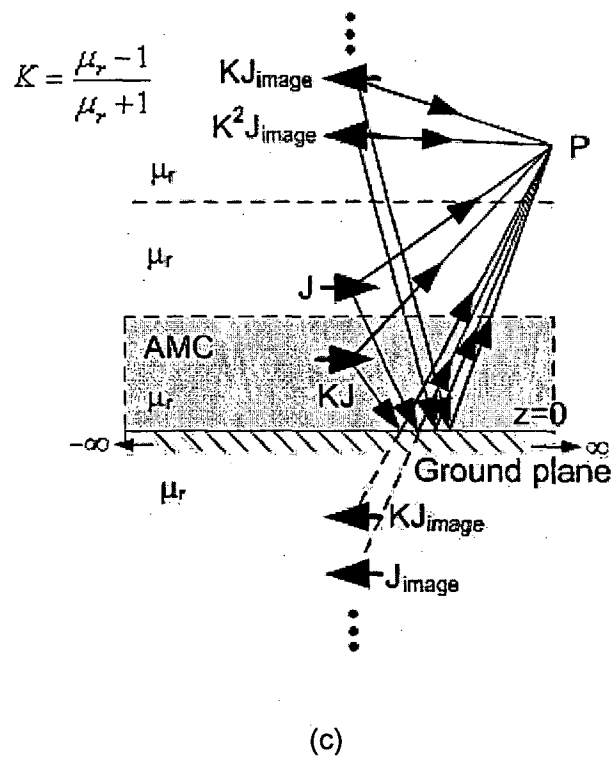
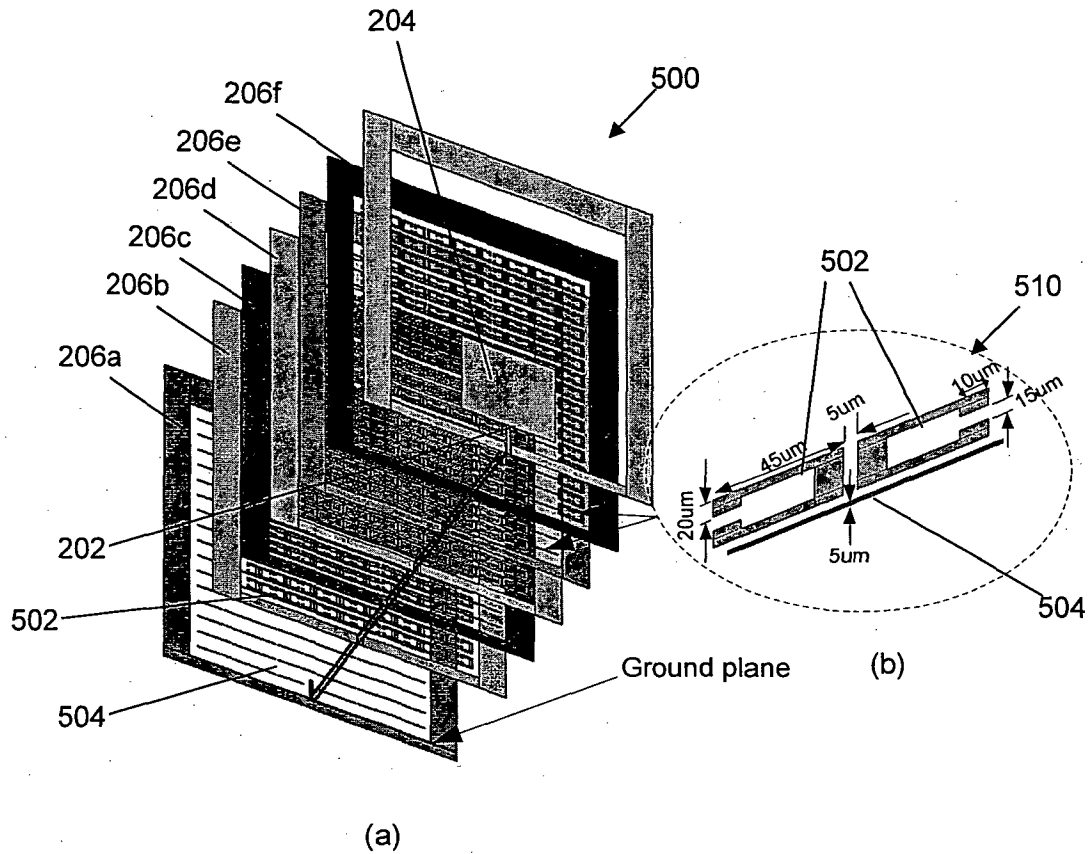


Figure 5

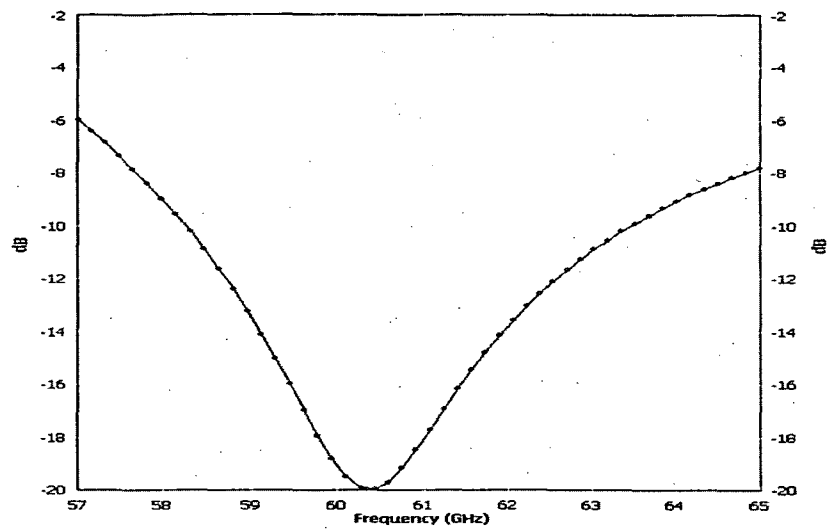


Figure 6

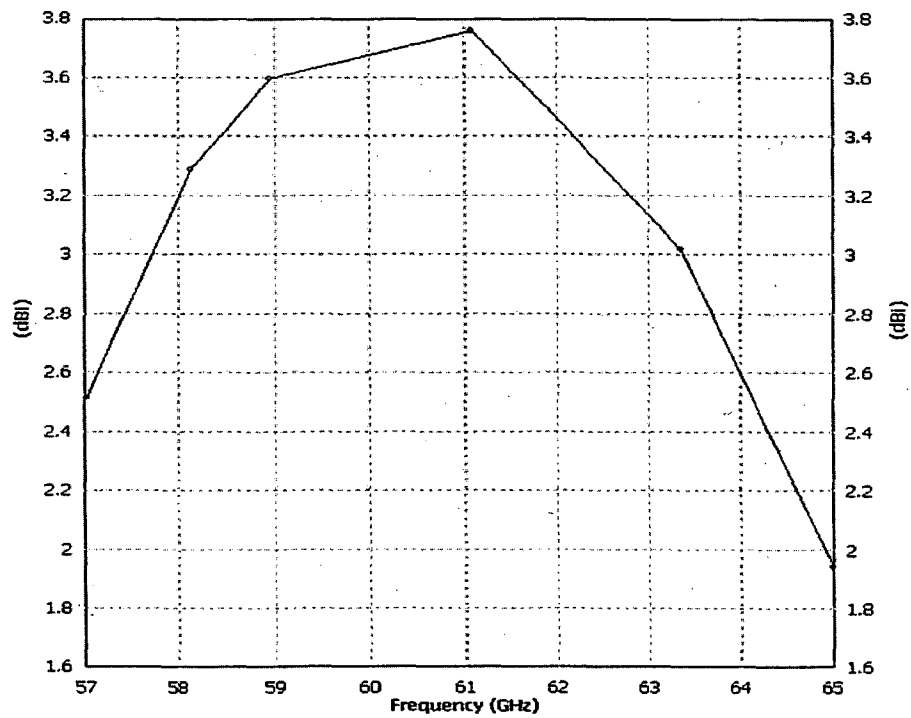


Figure 7

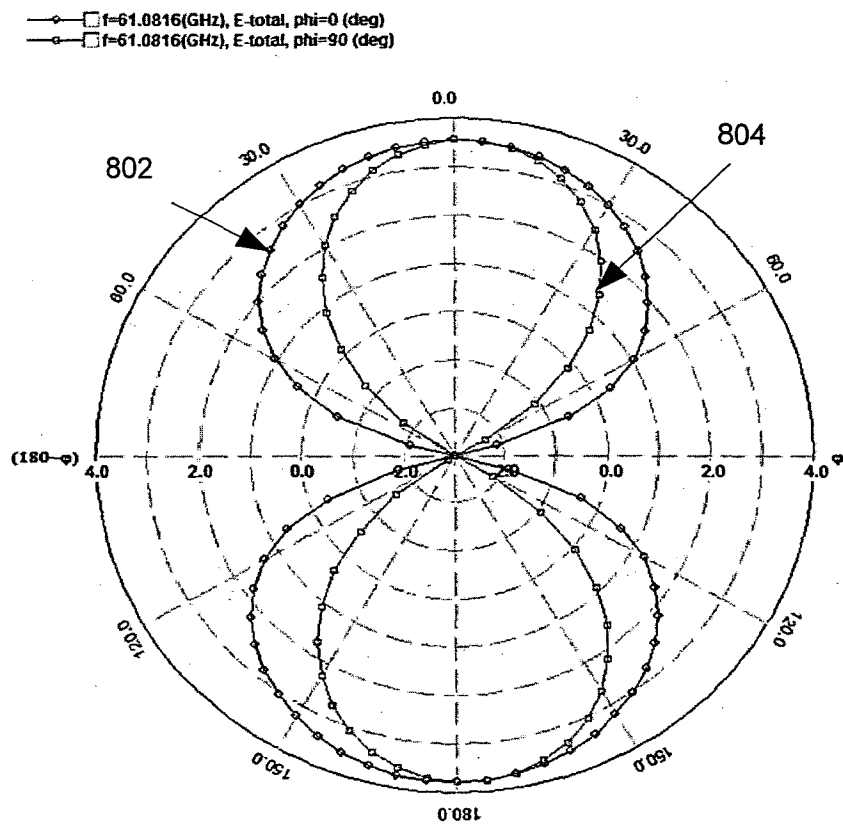


Figure 8

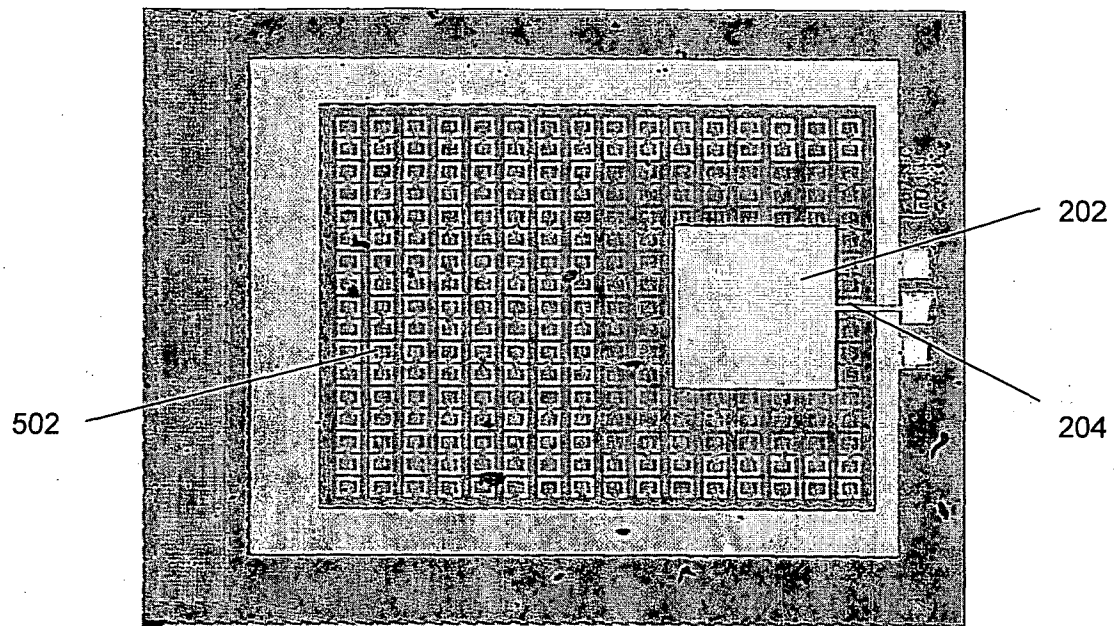


Figure 9

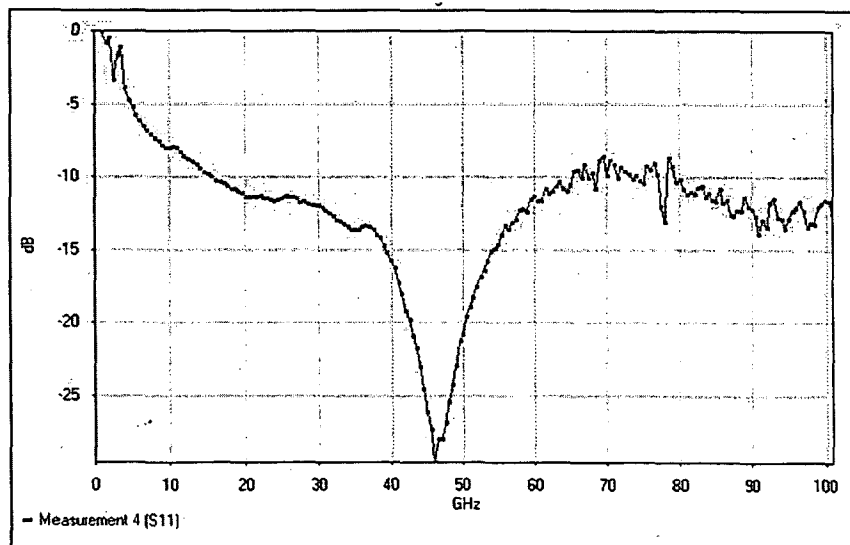


Figure 10

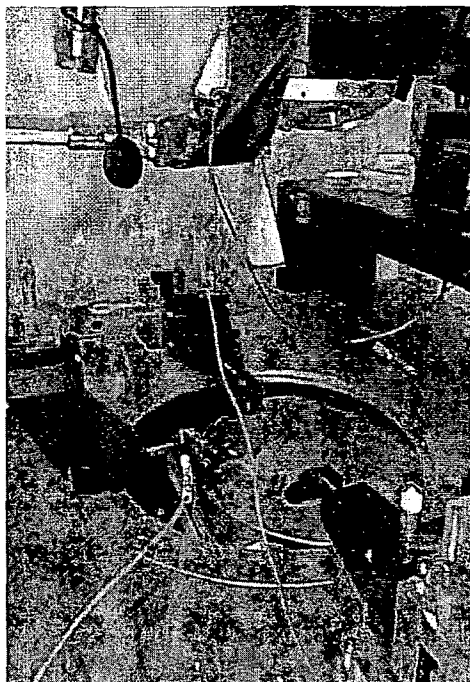


Figure 11

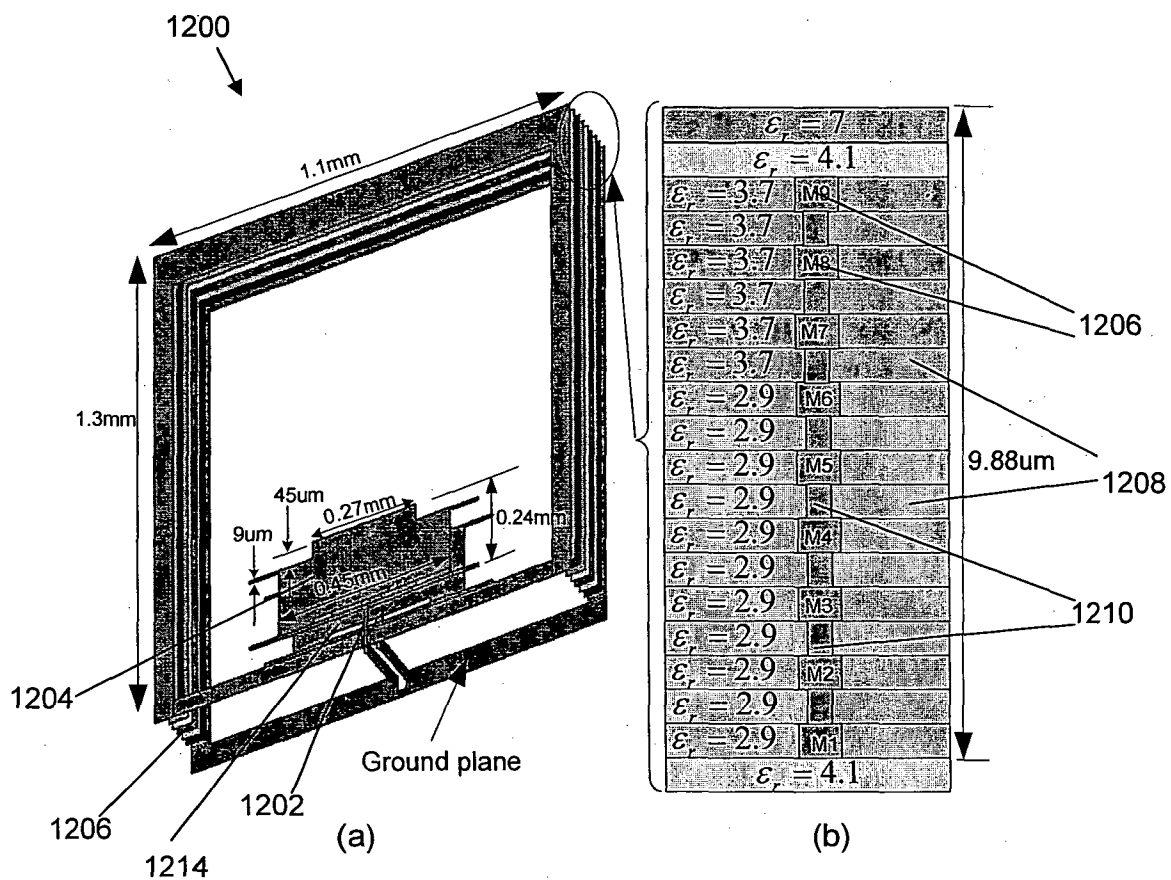


Figure 12

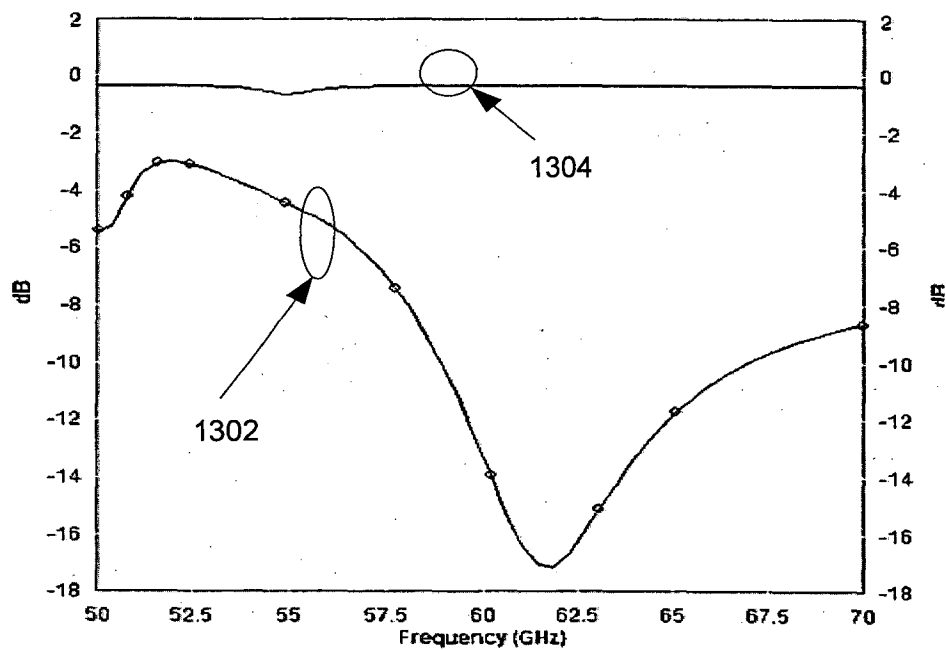


Figure 13

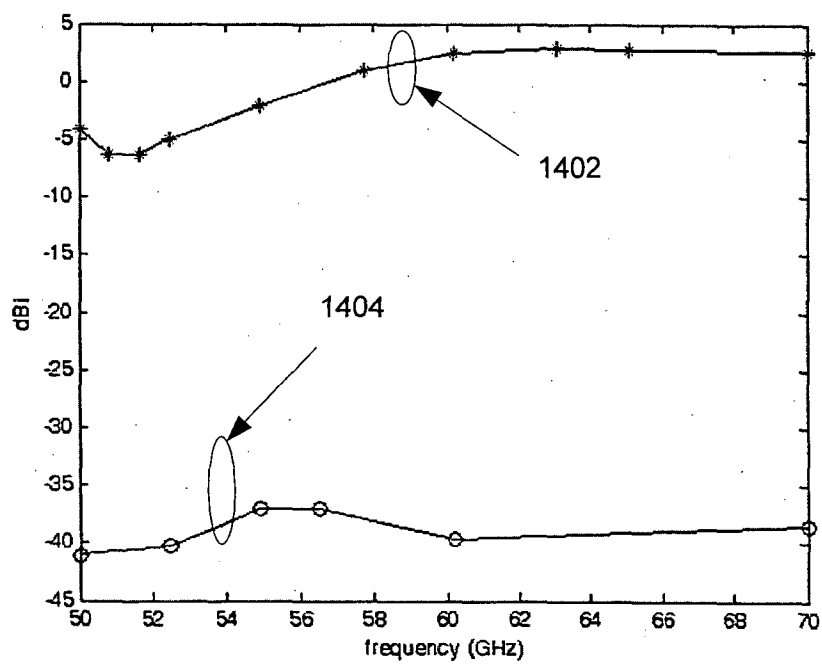


Figure 14

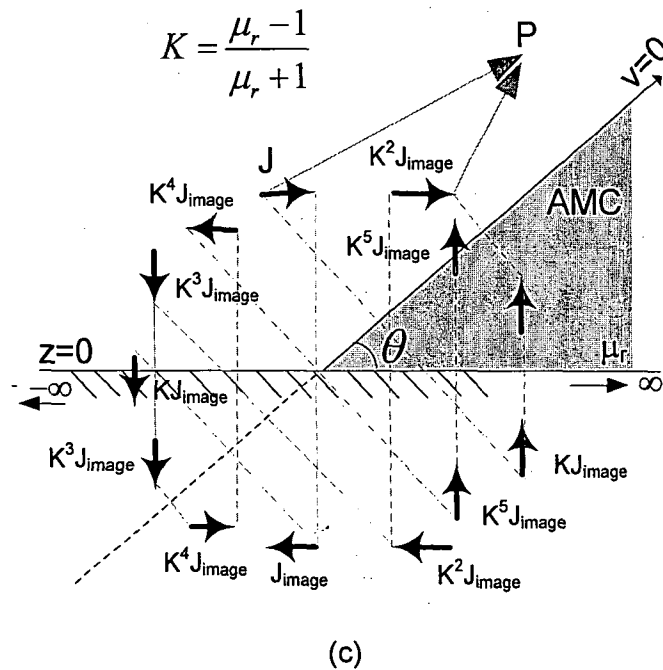
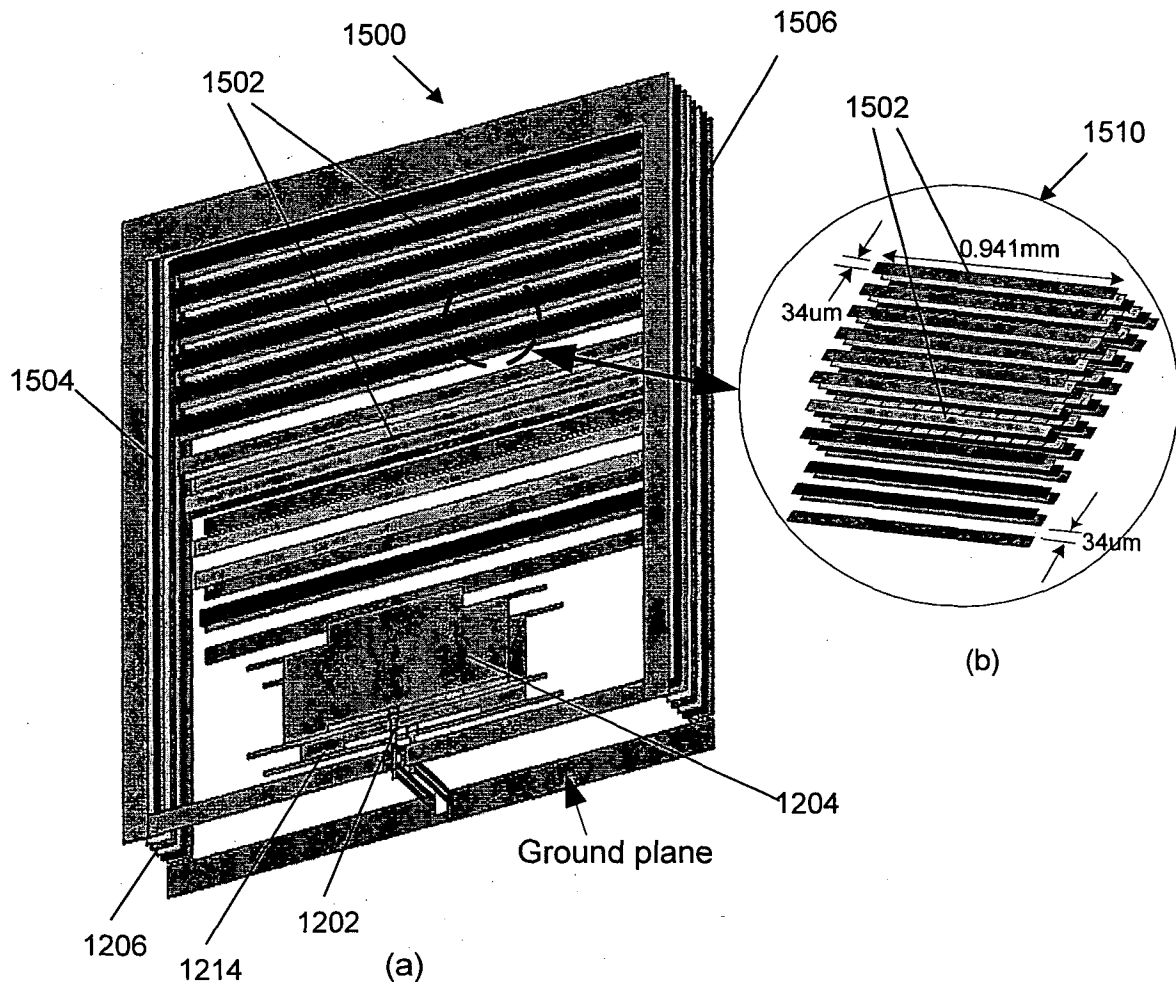


Figure 15

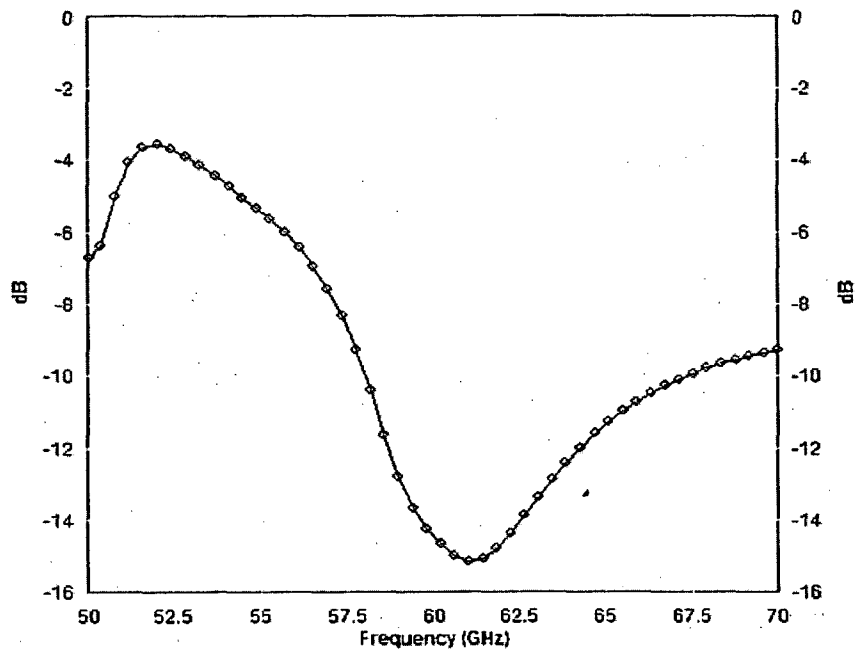


Figure 16

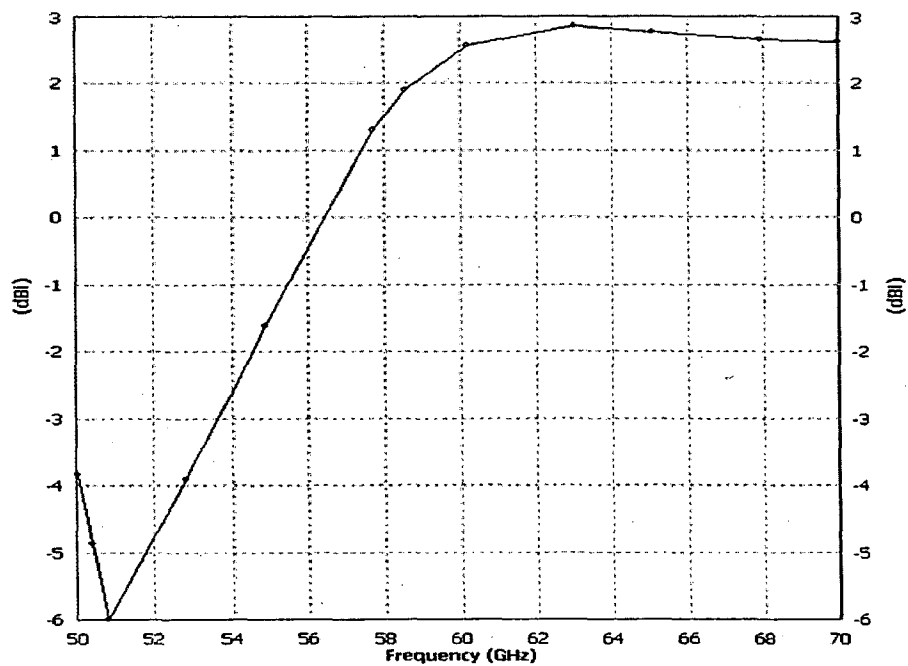


Figure 17

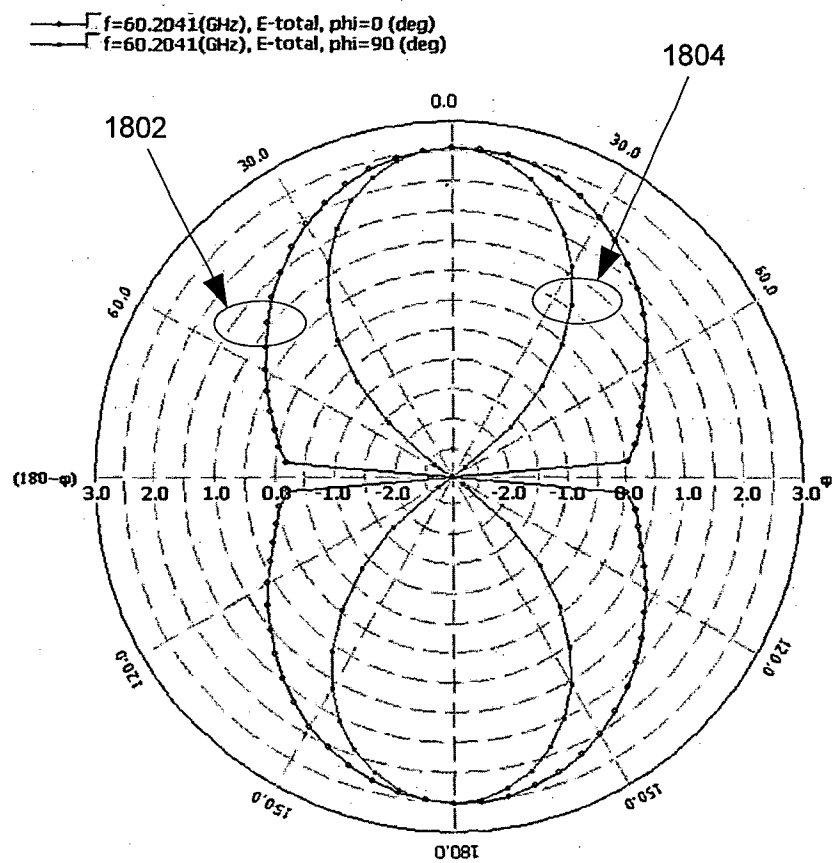


Figure 18

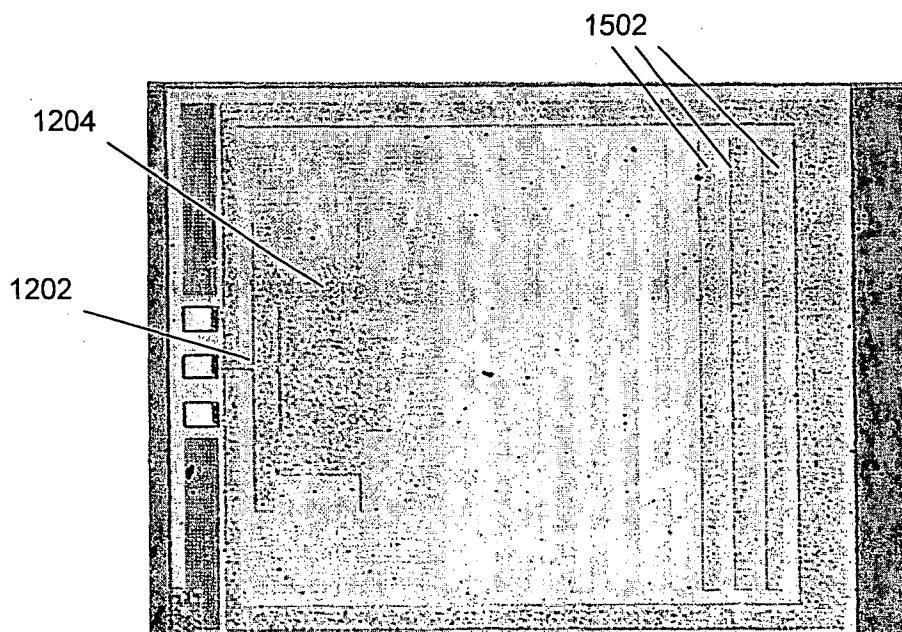


Figure 19

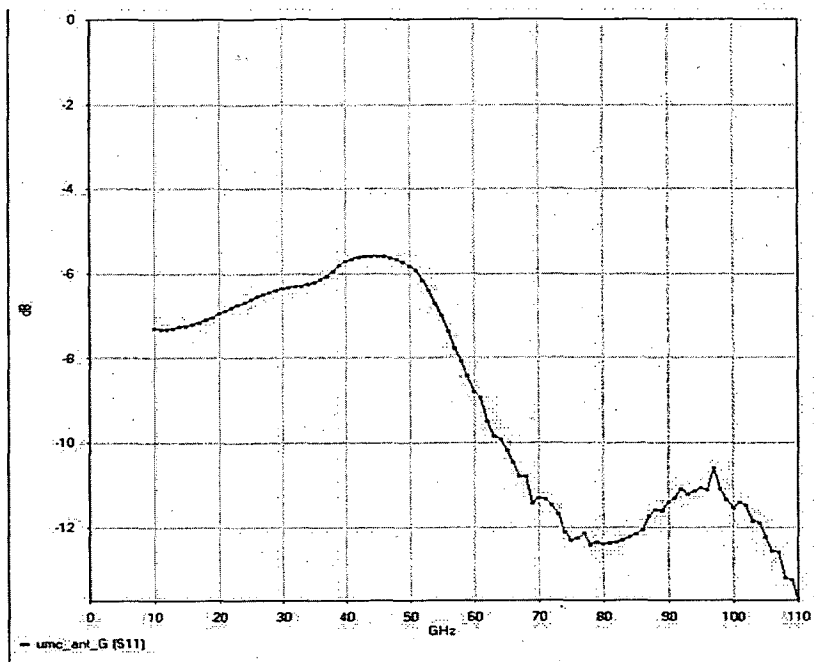


Figure 20

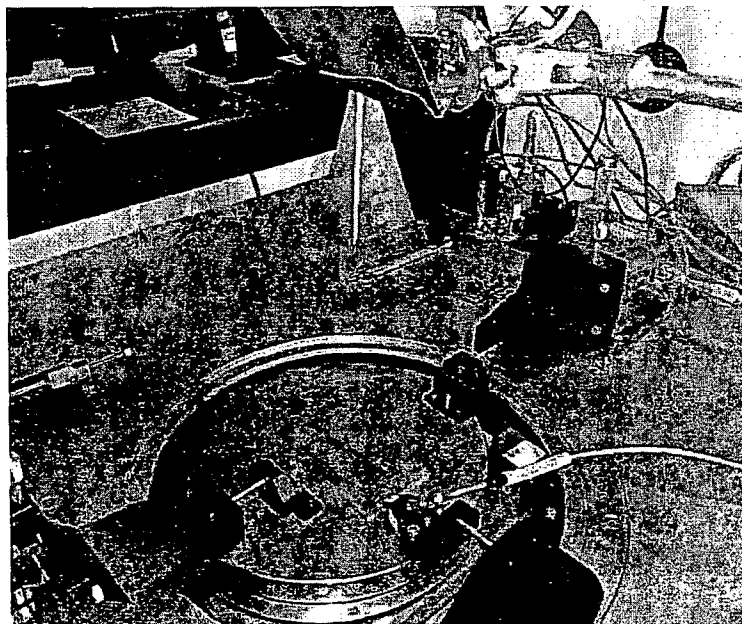
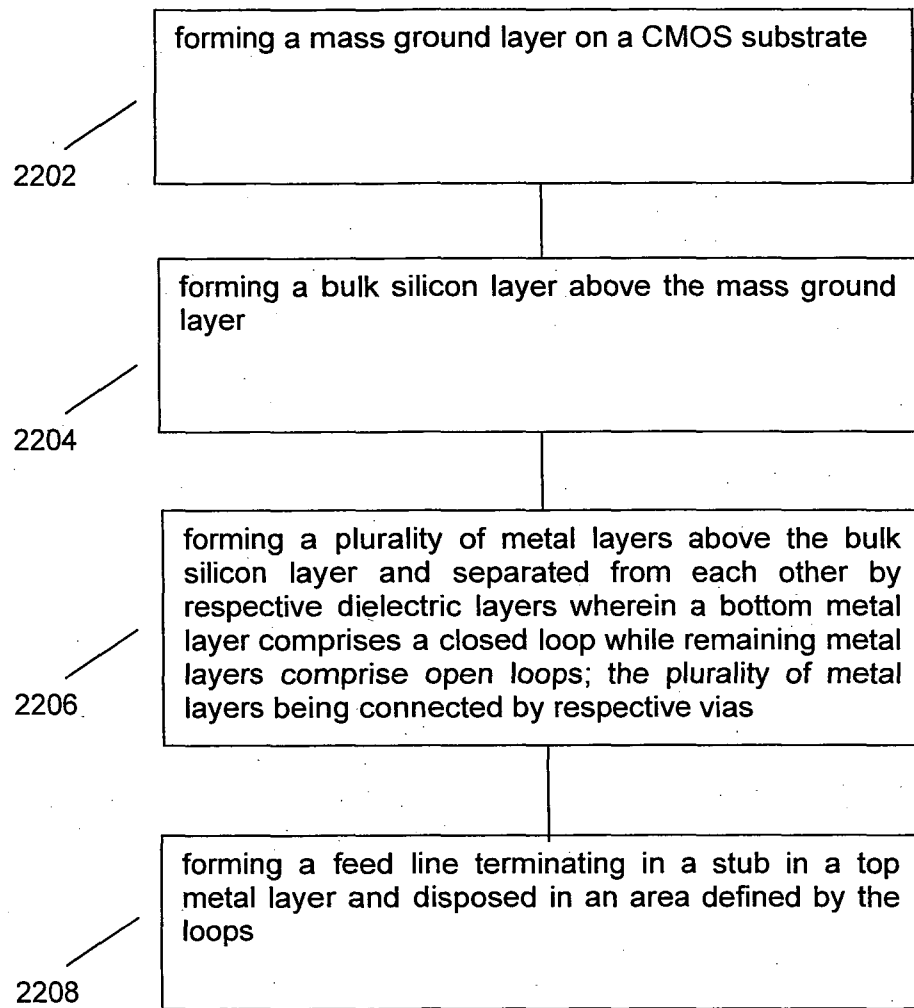


Figure 21



2200

Figure 22

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2010/000029

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H01Q 1/38 (2006.01)

H01Q 7/00 (2006.01)

H01Q 3/01 (2006.01)

H01Q 13/10 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Google Patents, Espacenet, WPI, EPODOC: antenna, metal, layers, loop, ring, slot and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6373447 B1 (ROSTOKER et al) 16 April 2002 Abstract, column 10 lines 5-63, Figs 7A, 7B	1, 2, 4, 5, 9-12, 15-17 6, 14, 18, 19
Y	US 2004/0183735 A1 (JECKO et al) 23 September 2004	
X	Abstract, paragraphs [0106], [0126], [0130], Fig 6	1-3, 4, 5, 8-12, 15-17 6, 14, 18, 19
Y	US 6885344 B2 (MOHAMADI) 26 April 2005	
Y	Abstract, column 1 line 52 – column 2 line 24, Fig 14b	6, 18
Y	US 6215454 B1 (TRAN) 10 April 2001 Whole document	14, 19



Further documents are listed in the continuation of Box C



See patent family annex

* Special categories of cited documents:	
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search
07 April 2010

Date of mailing of the international search report 14 APR 2010

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2010/000029

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	6373447	NONE					
US	2004/0183735	CA	2449359	EP	1407512	FR	2826186
		US	7129899	WO	2002/103844		
US	6885344	US	2004/0095287	US	6870503	US	2004/0100405
		US	2004/0095277	US	6963307	US	2005/0151698
		US	7126541	US	2005/0156789	US	7126542
		US	2005/0116864	US	7126554	US	2004/0095256
		US	7358848	US	2005/0169319	US	7522641
		US	2008/0252442				
US	6215454	AU	27726/99	BR	9904873	CA	2287329
		EP	0978153	IL	132268	WO	1999/043040
		ZA	9811839				
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.							
END OF ANNEX							