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(54) Title: SEMICONDUCTOR DEVICES INCLUDING A RECESSED ISOLATION FILL, AND METHODS OF MAKING THE SAME

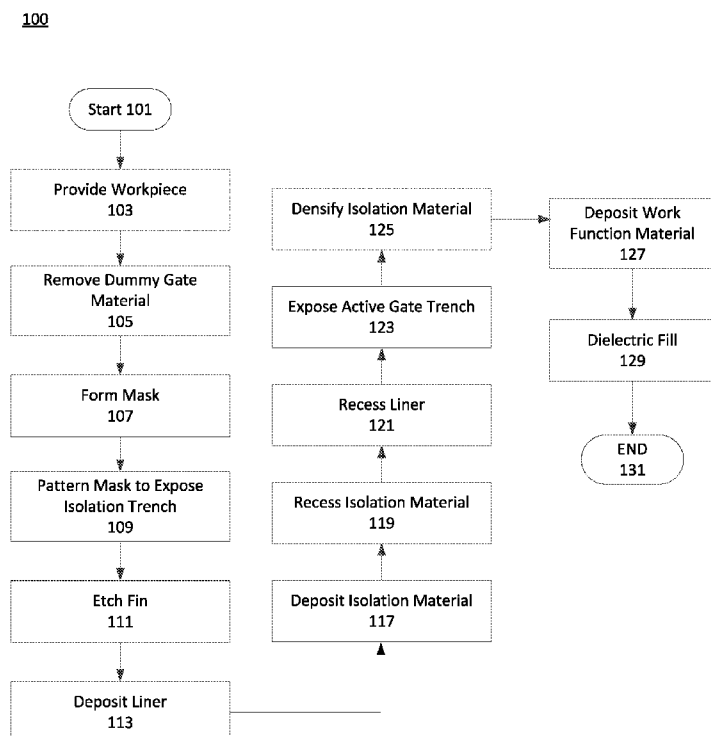


FIG. 1

(57) Abstract: Technologies for manufacturing semiconductor devices including isolation structures having a recessed isolation fill are disclosed. In some embodiments the technologies include methods for forming a recessed isolation fill within an isolation trench that electrically isolate at least two active transistor gates from one another. In further embodiments, methods for forming local interconnects in the isolation trench are also disclosed. Semiconductor devices including active transistors isolated by a recessed isolation fill and systems including such devices are also described.



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## SEMICONDUCTOR DEVICES INCLUDING A RECESSED ISOLATION FILL, AND METHODS OF MAKING THE SAME

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### FIELD

[0001] The present disclosure generally relates to semiconductor devices and, in particular, to semiconductor devices including a recessed isolation fill. Methods of making such devices are also described.

### BACKGROUND

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[0002] For the past several decades, feature scaling has been a driving force in the production of integrated circuits in the semiconductor industry. Scaling features to smaller and smaller size can enable the production of devices that include a larger number of functional units within the limited real estate of a semiconductor chip. For example, shrinking transistor size may allow for an increased number of memory devices to be placed within a given area of a semiconductor chip, leading to the production of memory devices with increased storage capacity. However, shrinking feature size can also lead to challenges during manufacturing that in some instances can be difficult to address.

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[0003] In the manufacture of integrated circuit devices, multi-gate transistors such as tri-gate transistors have become more prevalent as device dimensions continue to shrink. In some processes, single and multiple gate transistors such as tri-gate transistors may be formed using a so-called “replacement gate” process, in which a dielectric material is used to form dummy gates at a relatively early stage of a process for manufacturing an integrated circuit. In many instances the dummy gates serve as a placeholder for a later active or inactive gate structures, and in some cases they may also serve as a mask during various etching or other processes that may be carried out to form other features of a device. In any case, dummy gates are generally removed at some point during the manufacturing process, and replaced with an active or inactive gate structure, as desired. For example, a dummy gate may be removed and replaced

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with conductive material to form an active gate channel of a tri-gate and/or other fin-based transistor.

[0004] Although replacement gate processes have proven to be an effective technique for forming single and multiple gate transistors, challenges have arisen as  
5 device configurations continue to evolve. Aspects of the present disclosure are directed at addressing at least some of those challenges.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Features and advantages of embodiments of the claimed subject matter will become apparent as the following Detailed Description proceeds, and upon  
10 reference to the Drawings, wherein like numerals depict like parts, and in which:

[0006] **FIG. 1** is a flow chart of operations consistent with one example embodiment of a method of forming a semiconductor device including a recessed isolation fill consistent with the present disclosure.

[0007] **FIGS. 2A-2I** stepwise illustrate perspective and cross-sectional views of  
15 various operations in a method of forming a workpiece consistent with embodiments of the present disclosure.

[0008] **FIGS. 3A-3N** stepwise illustrate cross-sectional views of various operations in a method of forming a semiconductor device including a recessed isolation fill consistent with the present disclosure.

[0009] **FIG. 4** is a top down view of one example of a layout of a plurality of fin-based transistors in an integrated circuit device consistent with embodiments of the  
20 present disclosure.

[0010] **FIG. 5** is a block diagram of a computing device consistent with embodiments of the present disclosure.

#### DETAILED DESCRIPTION

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[0011] As noted in the background, replacement gate processes are sometimes used to produce semiconductor devices, such single and multiple gate transistors (e.g., tri-gate transistors), fin-based field effect transistors (FINFETS), combinations thereof, and the like. In such processes, dielectric material may be deposited and patterned  
30 relatively early in the production of the device to produce dummy gates. Among other things, a dummy gate may function as a placeholder for a transistor gate that will be formed later in the process. For example after a dummy gate is formed it may be replaced with an active gate structure. Use of that technique may limit or prevent

damage to the active gate structure, which may have been adversely affected by processing steps executed after the formation of the dummy gate but prior to the formation of the active gate structure.

[0012] As device dimensions continue to shrink and device configurations continue to evolve interest has grown in the bulk production of FINFETS and other semiconductor devices using replacement gate techniques. In that regard, processes have been developed wherein one or a plurality of long fins (hereinafter, a “master fin” or “master fins”) are formed from a substrate. Each master fin may include (or may be processed to include) a plurality of source, drain and channel regions, such that a plurality of active transistors may be formed from the same master fin.

[0013] Before or after the formation of the source, drain, and channel regions, a dielectric material layer may be bulk deposited on a master fin and patterned to form a plurality of dummy gates that are separated by one or more trenches (e.g., source drain trenches) in the dielectric material. Source/drain contacts may then be formed in the trenches. For example, formation of a source/drain contact may be accomplished by initially forming a spacer layer and an etch stop layer on the sidewalls of the trenches in the dielectric material of the dummy gates. Subsequently source/drain contacts (e.g., metal or other electrically conductive contacts) may be formed within the trenches, e.g., on the etch stop and/or spacer layer.

[0014] Following the formation of the source/drain contacts, subsequent operations may be conducted to process the plurality of dummy gates to form one or more active gates and/or isolating regions between active gates. With respect to the latter, as noted above one feature of the above described process is that it may permit the formation of a plurality of active transistors on a common master fin. Because all or a portion of the material of the master fin may be conductive, it may be desirable to electrically isolate adjacent (or nearby) active transistors on a common master fin from one another, e.g., so as to limit and or prevent potential electrical shorts between such devices.

[0015] In some replacement gate processes electrical isolation between active transistors on a common master fin may be accomplished by removing individual or a relatively small number of dummy gates, etching out a portion of the fin underlying the removed dummy gate(s), and filling the resulting structure with an insulating (dielectric) material. Select removal of dummy gates may be accomplished, for

example, by masking dummy gates that are to be retained and subjecting those that are to be removed to a dry etching chemistry that is designed to remove the dielectric material of a target dummy gate, as well as a portion of the material of the fin that is exposed target dummy gate. The result of such etching may be the formation of an isolation trench corresponding to one of the removed dummy gates (also referred to herein as a target dummy gate), and the formation of an isolation region within a portion of the fin underlying the target dummy gate. After dry etching, a dielectric material such as a nitride may be deposited to fill the isolation region and the isolation trench. Thereafter the remaining dummy gates may be removed to form corresponding active gate trenches, and operations may be carried out to form active gates therein.

**[0016]** Although the above described process are effective to form semiconductor devices including a plurality of active transistors that are electrically isolated from one another along a common master fin, their use can present some challenges. For example the dry etching chemistry used to remove select (i.e., target) dummy gates and form isolation regions in the portion of the fin underlying such dummy gates may not be highly selective to the spacer and/or etch stop layers that are used in the source/drain contact regions of the device, and which may be proximate (e.g., adjacent) a target dummy gate. Indeed in some instances the dry etching chemistry may remove at least a portion of the spacer and/or etch stop layers of a proximate source/drain contact, which may negatively affect device operation. In some instances, this lack of selectivity may be reflected by a “flaring” of the isolation trench, e.g., proximate a surface thereof, and a corresponding flaring of the dielectric (e.g., nitride) fill subsequently formed therein.

**[0017]** Moreover as noted above, some dummy gate processes may completely fill an isolation region and isolation trench with a dielectric material prior to the removal of the remaining dummy gates and the execution of subsequent source/drain contact forming operations. As a result, it may be difficult and/or impracticable to form local interconnects within the isolation trenches previously formed in the process. As such local interconnects are becoming of increasing interest, this may be considered a material limitation of many replacement gate processes such as the one described above.

[0018] With the foregoing in mind one aspect of the present disclosure relates to methods for forming semiconductor devices that include one or a plurality of single or multiple gate transistors, wherein such devices include an isolation trench including a recessed isolation fill. As will become apparent from the following discussions, the technologies described herein may enable the production of semiconductor devices that include one or more interconnects (hereinafter, “local interconnects”) within an isolation trench. As such, the methods described herein may facilitate or otherwise enable the production of semiconductor devices including such local interconnects.

[0019] Reference is therefore made to FIG. 1, which is a flow chart of example operations in accordance with one embodiment of the present disclosure. For the sake of convenience and ease of understanding, it is noted that certain operations of the method of FIG. 1 will be described in conjunction with FIGS. 2A-2I, which stepwise illustrate and that certain other operations of FIG. 1 will be described in conjunction with FIGS. 3A-3N. Specifically, FIGS. 2A-2I are referenced in connection with the stepwise production of one example of a workpiece that may be used in accordance with the present disclosure. In contrast, FIGS. 3A-3N are referenced in connection with the stepwise production of one example of a semiconductor device consistent with the present disclosure, beginning with the workpiece shown in FIG. 2I.

[0020] It should be understood of course that FIGS. 2A-2I and 3A-3N are illustrative only and that the geometry, scale, and/or general configuration of the workpiece shown in FIG. 2I and the semiconductor device shown in FIG. 3N are for the sake of example. Indeed as will be appreciated by one of ordinary skill in the art, the methods described herein are not limited to a particular workpiece structure (or method of producing the same), or to a particular semiconductor device structure. Moreover it will also be appreciated that the elements of FIGS. 2A-2I and 3A-3N are not to scale, and are presented at a scale that is intended to facilitate understanding of the general structure of certain workpieces and semiconductor devices consistent with the present disclosure.

[0021] Returning to FIG. 1, method 100 may begin at block 101. The method may proceed to optional block 103, pursuant to which a workpiece (e.g., a device precursor) may be provided. As used herein, the terms “workpiece” and “device precursor” are interchangeably used to refer to a structure that may be processed to form a semiconductor device, such as but not limited to a semiconductor device

including one or a plurality of single or multi gate transistors, e.g., one or more FINFETS. In some embodiments and as will be described below, the methods described herein may form or otherwise utilize a workpiece that is consistent with the structure of FIG. 2I, which is described later. As noted previously however the methods of the present disclosure are not limited to the use of workpieces consistent with FIG. 2I, and may be used on and/or with any suitable workpiece. Without limitation, in some embodiments the workpiece is a structure that may be used in the formation of a plurality of single or multi-gate transistors along a common master fin, e.g., via a replacement gate process.

10 [0022] It is also emphasized that the methods of the present disclosure are not conditioned on any particular method of providing a workpiece. As such, it should be understood that the operations of block 103 are optional, and that a workpiece may be provided in any suitable manner. For example, the present disclosure envisions embodiments in which a suitable workpiece may be obtained in some other manner (e.g., from a different manufacturing process, via purchase from a third party, etc.). In such instances, the operations of block 103 may be omitted and the method may proceed directly from block 101 to block 105. Nonetheless in the interest of completeness and to facilitate understanding of the technologies described herein the present disclosure will proceed to describe one example of a workpiece that may be used, with reference to FIGS. 2A-2I.

[0023] With the foregoing in mind, the operations of optional block 103 may begin with the provision of a starting structure that may be suitable for forming one or a plurality of fin based semiconductor devices, such as one or a plurality of FINFETS. As one example of such a structure reference is made to FIG. 2A, which depicts starting structure 200. As shown in the illustrated embodiment, starting structure 200 includes a fin 204 (e.g., a three dimensional semiconductor body) formed above substrate 202. For the sake of ease of understanding, starting structure 200 has been illustrated as including a single fin 204, but it will be appreciated that multiple fins may be included. In any case, starting structure 200 further includes an isolation dielectric layer 206, which may serve to isolate fin 204, e.g., from adjacent fins or other structures that may be included or otherwise formed in/on starting structure 200.

30 [0024] In various embodiments and as shown in FIG. 2A, substrate 202 may be a bulk semiconductor substrate, and fin 204 may be formed therefrom. In that regard,

substrate 202 (and hence, fin 204) may be formed from any material that is suitable for use as a substrate and/or fin of a semiconductor device, and in particular for non-planar transistors such as FINFETs and/or other single or multi-gate transistors. Non-limiting examples of suitable materials that may be used as substrate 202 and fin 204  
5 therefore include silicon (Si), germanium (Ge), silicon-germanium (SiGe), silicon-carbide (SiC), sapphire, a III-V compound semiconductor, a silicon on insulator (SOI) substrate, combinations thereof, and the like. Without limitation, in some embodiments substrate 202 and fin 204 are formed from or includes single crystal silicon, which may or may not be strained.

10 **[0025]** Fin 204 may have any suitable dimensions, and in some embodiments may be dimensioned such that a plurality of semiconductor devices such as FINFETs may be formed thereon. That is, FIN 204 may be a master fin which is relatively long, such that it may support a plurality of single or multi-gate transistors. In such instances, some or all of the plurality of semiconductor devices may be electrically isolated from  
15 one another, e.g., in a manner consistent with the present disclosure.

**[0026]** Isolation dielectric layer 206 may be composed of a material that is suitable to electrically isolate or contribute to the isolation of semiconductor devices that may be formed on fin 204 and, in particular, to isolate permanent gate structures that may be formed on fin 204 from an underlying portion of substrate 202. Non-limiting  
20 examples of suitable materials that may be used as or in isolation dielectric layer 206 therefore include dielectric materials such as silicon dioxide, silicon nitride, silicon oxynitride, carbon doped silicon nitride, combinations thereof, and the like.

**[0027]** Isolation dielectric layer 206 may be formed in any suitable manner. For example, isolation dielectric layer 206 may be formed by depositing a bulk layer of a dielectric material, followed by recessing the dielectric layer to expose at least a  
25 portion of fin 204. Of course, other methods of forming isolation dielectric layer 206 may be used and are envisioned by the present disclosure.

**[0028]** With reference to FIGS. 2B-2D, the operations of optional block 103 may continue with the preparation of a plurality of dummy gate structures that are  
30 orthogonal to fin 204 and are located on at least a portion of isolation dielectric layer 206. As best shown in FIG. 2B, the formation of dummy gate structures may be initiated by bulk depositing a layer 208 of a dielectric material. Following such bulk deposition and as best shown in FIG. 2C, layer 208 may be patterned (e.g., via

lithography or another suitable method) to form a plurality of dummy gates 210<sub>1</sub>-210<sub>n</sub>, where n is an integer greater or equal to 2. In some instances, n is at least greater than or equal to 3. In such instances it may be appreciated that at least three dummy gates are provided.

5 [0029] For the sake of illustration the present disclosure focuses on embodiments in which layer 208 and dummy gates 210<sub>1</sub>-210<sub>n</sub> are formed from polycrystalline silicon (polysilicon), but it should be understood that other materials may also be used. For example, in some embodiments layer 208 and dummy gates 210<sub>1</sub>-210<sub>n</sub> are composed of any material that is suitable for removal by a replacement gate and/or isolation  
10 trench forming operation, as discussed below. In that regard, example materials that may be used to form dummy gates 210<sub>1</sub>-210<sub>n</sub> include polycrystalline silicon, amorphous silicon, silicon dioxide, silicon nitride, or one or more combinations thereof. Without limitation, in some embodiments layer 208 and dummy gates 210<sub>1</sub>-210<sub>n</sub> are each formed from polycrystalline silicon.

15 [0030] Reference is now made to FIG. 2D, which is a cross-sectional view along a plane A extending vertically through fin 204 in a region B of FIG. 2C, i.e., with dummy gates 210<sub>1</sub>-210<sub>n</sub> extending into and out of the page. As shown, patterning of the layer 208 may result in the production of a plurality of source/drain trenches 212<sub>y</sub>, wherein y is an integer greater than or equal to 1. At this stage doped tips and/or  
20 source/drain regions 214 may be formed in or on fin 104, e.g., using dummy gates 210<sub>1</sub>-210<sub>n</sub> as a mask. Alternatively, source/drain regions 214 may be formed in FIG. 104 at another time, e.g., prior to the deposition of the layer 208 of dielectric material.

[0031] In some embodiments production of a workpiece may continue with the formation of a gate spacer structure within source/drain trenches 212<sub>y</sub>. In general, the  
25 gate spacer structure may be configured to electrically isolate, or contribute to the isolation of a permanent gate structures (e.g., which may replace dummy gates 210<sub>1</sub>-210<sub>n</sub>) from adjacent gate contacts (e.g., which may be formed in source/drain trenches 212<sub>y</sub>. Moreover, the gate spacer structure may isolate the gate contacts from source/drain regions on or within fin 104. Moreover, all or a portion of the gate spacer  
30 structure may act as an etch stop to protect certain components (e.g., later formed source/drain contacts) during etching operations that may be carried out later in the process.

[0032] For the sake of illustration the present disclosure will focus on the formation of a gate spacer structure that includes multiple layers, namely a spacer layer 216 and an etch stop layer 218. It should be understood however that use of a multilayer spacer is not required, and that any suitable gate spacer structure may be used.

5 Indeed the present disclosure envisions embodiments in which a gate spacer structure including one, two or more layers are used, wherein at least one of such layers is electrically insulating.

[0033] Turning now to FIG. 2E, in the illustrated embodiment production of a gate spacer may begin with the deposition of a spacer layer 216 on the structure of FIG.

10 2D. In general, spacer layer 216 may be configured to separate a later formed gate contact from other components of the device, such as one or more source drain regions. In that regard spacer layer 216 may be formed by any suitable process, and may be of any suitable material. Non-limiting examples of suitable materials that may be used to form spacer layer 216 include carbides, nitrides, and oxides, such as  
15 but not limited to silicon carbide, silicon nitride, silicon oxides, carbon doped silicon nitrides, combinations thereof, and the like. Without limitation, in some embodiments spacer layer 216 is a carbon doped silicon nitride (SiCN)

[0034] Following its deposition, an etching or other selective removal process (e.g., a lithographic process) may be executed to remove a spacer layer 216 from the  
20 horizontal surfaces of FIG. 2E. This concept is shown in FIG. 2F, which depicts spacer layer 216 as extending down the sidewalls of dummy gates 210<sub>n</sub>, but as being removed from the upper surface of fin 204 and the upper surface of dummy gates 210<sub>1</sub>-210<sub>n</sub>. This may be accomplished, for example, by exposing the structure of FIG. 2E to a wet or dry etching chemistry that anisotropically etches spacer layer 216 but is  
25 selective to the materials of dummy gates 210<sub>1</sub>-210<sub>n</sub> and source/drain regions 214.

[0035] At this point production of the gate spacer structure may continue with the formation of a etch stop layer on the structure of FIG. 2F. In this regard reference is made to FIGS. 2G and 2H, which stepwise illustrate the formation of etch stop layer 218. Independently or in conjunction with spacer layer 216, etch stop layer 218 may  
30 function to electrically isolate source/drain contacts (which may be later formed in source/gate trenches 212<sub>y</sub>) from conductive materials that may be used in an active gate structure that replaces one or more of dummy gates 210<sub>1</sub>-210<sub>n</sub>. Moreover, etch stop layer 218 may include or be formed from materials that are unaffected or

substantially unaffected by an etching chemistry that may later be used, e.g., to remove dummy gates 210<sub>1</sub>-210<sub>n</sub> in accordance with a process for forming a semiconductor device including a recess isolation fill consistent with the present disclosure.

5 [0036] Non-limiting examples of materials that may be used as or included in etch stop layer 218 include metal carbides, nitrides, and oxynitrides, such as but not limited to silicon carbide, silicon nitride, silicon oxynitride, carbon doped silicon nitride (SiCN), combinations thereof, and the like. In some embodiments etch stop layer 218 and spacer layer 216 are formed from the same or different dielectric materials. Without limitation, in some instances etch stop layer 218 is formed from a second dielectric material, spacer layer 216 is formed from a first dielectric material, and the first and second dielectric materials are the same as or different from one another. For example, in some instances spacer layer 216 is silicon nitride or carbon doped silicon nitride (SiCN), and etch stop layer 218 is a carbon doped silicon nitride (SiCN) or another dielectric material.

[0037] As shown in FIG. 2G, formation of etch stop layer 218 may begin with the bulk deposition of the material of etch stop layer 218 on the structure of FIG. 2F, e.g., via chemical vapor deposition, physical vapor deposition, atomic layer deposition, combinations thereof, and the like. Following such deposition, a polishing or other suitable process may be used to remove the portion of etch stop layer 218 and spacer layer 216 that is present on the upper surface of dummy gates 210<sub>1</sub>-210<sub>n</sub>. For example, in some instances the structure of FIG. 2G may be subject to chemical mechanical planarization to remove the etch stop layer 218 and spacer layer 216 from the upper surface of dummy gates 210<sub>1</sub>-210<sub>n</sub>, resulting in the structure shown in FIG. 2H.

[0038] At this stage, production of a workpiece may proceed with the formation of source/drain contacts 220 between dummy gates 210<sub>1</sub>-210<sub>n</sub> and etch stop layer 218. The position and structure of contacts 220 may be layout dependent. In some instances source/drain contacts 220 may be formed by deposition and planarization of a conductive material, such as a metal, metal alloy, and/or metal-semiconductor alloy. Alternatively or additionally, one or more of source/drain contacts 220 may be a dummy contact, i.e., composed of a dummy dielectric material that may be replaced at a later time with a conductive material.

[0039] In any case the result of such operations may be the production of workpiece 250, which may have the structure shown in FIG. 2I. More specifically and as shown in the embodiment of FIG. 2I, workpiece 250 may include one or more fins 204, each of which may include a plurality of source drain regions 214, a plurality of source/drain contacts 220, and a plurality of dummy gates 210, wherein each source/drain contact 220 is formed above a respective one of the plurality of source/gate regions 214, and at least two of the source/gate contacts 220 are separated by at least one of the dummy gates 210<sub>1</sub>-210<sub>n</sub>. Moreover as further shown in the embodiment of FIG. 2I, source/drain contacts 220 may have a top surface, a bottom surface, and first and second sidewalls (not labeled), and workpiece 250 may further include an etch stop layer 218 that is present between each of the first and second sidewalls and a corresponding sidewall of a dummy gate. In some embodiments and as further shown, at least a portion of etch stop layer 218 in some embodiments may also be present between the bottom surface of the source/drain contact and an upper surface of fin 204 or, more specifically, an upper surface of a source/drain region 214. Finally and as further shown, workpiece 250 in some embodiments may include a spacer layer 216 between the etch stop layer 218 and one or more sidewalls of a dummy gate.

[0040] Returning to FIG. 1, the operations of optional block 103 may be considered complete upon the provision of a workpiece, such as workpiece 250. Subsequently, operations may be performed to form a semiconductor device including a recessed isolation fill, as described below. It is noted that for the sake of example that the present disclosure will proceed to describe an example method in which operations are performed starting from workpiece 250 of FIG. 2I to form a semiconductor device consistent with the present disclosure. It is again emphasized that the use of workpiece 250 is not required, and that the technologies and in particular the methods described herein may be suitably applied to produce semiconductor devices with recessed isolation fills starting from a workpiece having a different structure.

[0041] Following the provision of workpiece 250 or another suitable workpiece, method 100 may proceed from block 103 to block 105. Pursuant to block 105, operations may be carried out to remove dummy gates 210<sub>1</sub>-210<sub>n</sub>. Such removal may be carried out in any suitable manner, such as via an etching or other suitable process that may selectively remove the material of dummy gates 210<sub>1</sub>-210<sub>n</sub>, while leaving the

remainder of the components of workpiece 250 substantially unaffected. For example in instances where dummy gates  $210_1$ - $210_n$  are formed from or include polycrystalline silicon, removal of dummy gates  $210_1$ - $210_n$  may be accomplished in bulk by isotropically or anisotropically etching the polycrystalline silicon with an etching chemistry that is selective to the materials of spacer layer 216 and fin 204. For example, a dry chloride ( $CL_2$ ) or hydrogen bromide dry etch may be initially performed, followed by a wet etch with tetramethylammonium hydroxide (TMAH) to remove the material of dummy gates  $210_1$ - $210_n$ . As may be appreciated, this is distinct from some other replacement gate methods, wherein only select dummy gates may be removed, e.g., with a dry etch. That is, the operations of block 105 may be understood to result in the removal of all or substantially all of dummy gates  $210_1$ - $210_n$ , as compared to the selective removal of one or relatively few dummy gates as may be carried out in other replacement gate processes.

[0042] Moreover, it should be understood that in some embodiments use of a wet chemical etch may enable the highly selective removal of polycrystalline silicon (or other materials of dummy gates  $210_1$ - $210_n$ ), without or without substantially removing or otherwise affecting other materials in the structure. For example, use of a highly selective wet etch at this stage may enable bulk removal of the material of dummy gates  $210_1$ - $210_n$ , without or without substantially affecting the quality and/or structure of spacer layer 216, etch stop layer 218, or a combination thereof. This may be manifested by the absence or relative lack of flaring of spacer layer 216, etch stop layer 218, or a combination thereof, e.g., proximate an upper surface of source/drain contact 220.

[0043] In any case, removal of dummy gates  $210_1$ - $210_n$  may result in the production of a plurality of gate trenches  $301_1$ - $301_n$  as shown in FIG. 3A, wherein  $n$  is an integer greater than or equal to 2. As can be seen in this embodiment, gate trenches  $301_1$ - $301_n$  may expose an upper surface (not labeled) of fin 204.

[0044] Returning to FIG. 1, following the above operations the method may proceed from block 105 to block 107, pursuant to which a mask may be deposited on the structure of FIG. 3A. One purpose of the mask may be to protect an active gate trench region (i.e., a portion of the workpiece which may ultimately support an active gate of a single or multi-gate transistor) during the execution of other process steps. With this in mind, the mask may include one or a plurality of layers. For example and as shown

in FIG. 3B (which is a magnified view of region C of FIG. 3A), in some embodiments the operations of block 107 may include the formation of a first hard mask 315, a second hard mask layer 320, and a photoresist layer 325 on the exposed surfaces of the structure of FIG. 3A.

5 [0045] As will become apparent from the following discussion, one function of first hard mask 315 is to protect an active gate trench 305 while other operations are being performed on an inactive gate trench 310, which may be adjacent or otherwise proximate thereto. For the sake of illustration, various FIGS. illustrate and the present disclosure focuses on embodiments in which an active gate trench 305 is adjacent to  
10 an inactive gate trench 320. It should be understood however that such a configuration is not required, and that the arrangement of inactive gate trench region(s) 320 and active gate trench region(s) 315 may be layout dependent.

[0046] In any case, first hard mask 315 may be formed from any suitable hard mask material. In some embodiments, first hard mask 315 is a metal hard mask, such as a  
15 hard mask formed from or containing ruthenium, tantalum, tungsten, hafnium, molybdenum, silicon, nitrides thereof, carbides thereof, oxides thereof, combinations thereof, and the like. Alternatively or additionally, in some embodiments first hard mask 315 is a carbon hard mask (CHM). Without limitation, in some embodiments first hard mask 315 is a CHM, such as a CHM that may be removed via plasma ashing  
20 (e.g., fluorine or oxygen plasma ashing).

[0047] First hard mask 315 may be deposited in any suitable manner, such as via spin on deposition, sputtering, chemical vapor deposition, atomic layer deposition, combinations thereof, and the like. Without limitation, in some embodiments first hard mask 315 is a carbon hard mask that is deposited via spin on deposition.

25 [0048] Second hard mask layer 320 may also be formed from any suitable hard mask material, such as but not limited to those noted above as being suitable for the first hard mask 315. For example, in some instances second hard mask layer 320 may be formed from a second hard mask material, first hard mask 315 may be formed from a first hard mask material, wherein the first and second hard mask materials are the  
30 same or different. Without limitation, in some embodiments, second hard mask layer 320 is formed from a different hard mask material than first hard mask 315. For example, first hard mask 315 may be a carbon hard mask, and second hard mask layer

320 may be a silicon hard mask (e.g., a silicon antireflective coating (SiARC)), a nitride hard mask (e.g., silicon nitride), combinations thereof, and the like.

[0049] It is also noted that while FIG. 3B depicts second hard mask layer 320 as a single layer of material, multiple second hard mask layers may be deposited on first hard mask 315. Indeed the present disclosure envisions embodiments in which second hard mask layer 320 includes multiple hard mask layers. For example in some embodiments second hard mask layer 320 may include a layer of a nitride hard mask and a layer of a silicon hard mask (e.g., a SiARC) formed on an upper surface of first hard mask 315. In such instances the nitride hard mask layer may in some embodiments be formed directly on the surface of first hard mask 315 and the silicon hard mask layer may be formed on the nitride hard mask layer. Alternatively the silicon hard mask layer may be formed directly on the surface of first hard mask 315 and the nitride hard mask layer may be formed on the silicon hard mask layer. Irrespective of the structure of second hard mask layer 320, a photoresist layer 325 may be deposited on an upper surface thereof.

[0050] In any case the operations of block 107 may result in the production of the structure shown in FIG. 3B. As shown in the illustrated embodiment, first hard mask 315 may extend over an upper surface of source/drain contacts 220 and into gate trenches 301<sub>1</sub>-301<sub>n</sub> down to the upper surface of fin 204. Second hard mask layer 320 in this embodiment is deposited on the upper surface of first hard mask 315. Finally, photoresist layer 325 in this embodiment is formed on the upper surface of second hard mask layer 320. As may be appreciated in this embodiment first hard mask 315, second hard mask layer 320, and photoresist layer 325 present a tri-layer arrangement which may be used to protect certain regions of the workpiece, e.g., during the formation of isolation regions within an isolation trench.

[0051] Returning to FIG. 1, method 100 may proceed from block 107 to block 109, pursuant to which the photoresist and other mask layers may be patterned to expose one or more inactive gate trenches. In this regard, as noted previously the global removal of the material of dummy gates 210<sub>1</sub>-210<sub>n</sub> may result in the formation of a plurality of corresponding gate trenches 301<sub>1</sub>-301<sub>n</sub>, any of which may be used to later as a trench for an active gate structure or as a trench for an isolation structure that may be present between active semiconductor devices on the same master fin. For the sake of clarity, gate trenches 301<sub>1</sub>-301<sub>n</sub> that are to support active gates are referred to

herein as “active gate trenches” whereas those that are to be used to support an isolation structure are referred to herein as “isolation trenches.” With that in mind, the present disclosure will focus on embodiments in which an active trench 305 is disposed proximate (e.g., adjacent) to an isolation trench, as shown in FIGS. 3B-3N.

- 5 It should be understood that such discussion and illustration are for the sake of example and that other configurations are possible and are envisioned by the present disclosure.

[0052] As shown in FIG. 3C, in some embodiments the operations pursuant to block 109 may begin with the patterning of photo resist layer 325. For example, a photolithographic or other suitable process may be executed to remove at least a portion of photo resist layer 325 that is disposed above isolation trench 310. This concept is best shown in FIG. 3C, which illustrates photoresist layer 325 as being patterned such that at least a portion of it has been removed from the region above isolation trench 310.

- 15 [0053] Turning to FIGS. 3D and 3E, the operations of block 109 may continue by selectively removing portions of second hard mask layer 320 and first hard mask 315 from the region above and/or within isolation trench 310. In some embodiments this may be accomplished in a stepwise fashion, such that at least a portion of second hard mask layer 320 above isolation trench 310 is removed, while leaving first hard mask 315 unaffected or substantially unaffected, as shown in FIG. 3D. That may be accomplished, for example, by exposing the structure of FIG. 3C to an etching chemistry that can remove the material of second hard mask layer 320, but which is selective to photoresist layer 325 and first hard mask 315. For example, in instances where second hard mask layer 320 is a silicon containing layer such as SiARC, it may be removed by exposing the structure of FIG. 3C to a carbon tetrafluoride (CF<sub>4</sub>) etch. In such instances the CF<sub>4</sub> may also remove a portion of photo resist layer 325, but photoresist layer 325 may be sufficiently thick such that at least a portion of it remains, e.g., over active gate region 305. The remaining portion of photoresist 325 may be used as a mask for the selective removal of a portion of second hard mask layer 320, and first hard mask 315 may be used as an etch stop.

[0054] To continue the stepwise exposure of isolation trench 310, the method may proceed with the selective removal of the material of first hard mask 315 from isolation trench 310. This concept is best shown in FIG. 3E, which illustrates one

example embodiment in which first hard mask 315 has been selectively removed from isolation trench 310. Such removal may be accomplished, for example, by exposing the structure of FIG. 3D to a wet or dry etching chemistry that can remove the material of first hard mask 315 (and in this case, photoresist layer 325), but which is selective to the material of second hard mask 320 and spacer layer 216. For example when first hard mask is a carbon hard mask (CHM), it may be removed by subjecting the structure of FIG. 3D to dry plasma etching, such as with an oxygen plasma which may remove the CHM while leaving the material of second hard mask substantially unaffected. In that way, second hard mask 320 may act as a mask for the underlying portions of first hard mask 315, and spacer layer 216 may act as an etch stop, thereby resulting in the structure of FIG. 3E.

[0055] It should be understood that while the above discussion focuses on embodiments in which photoresist layer 325, second hard mask layer 320, and first hard mask 315 are patterned in a stepwise fashion to expose isolation trench 310, such processing is not required and the patterning of such layers may be accomplished in any suitable manner. For example the present disclosure envisions embodiments in which two or more of such layers are patterned at the same time. In any case the result may be the production of a structure consistent with FIG. 3E, i.e., one in which isolation trench 310 is exposed to an upper surface of fin 204, whereas a “plug” of remaining mask material (in this case the remaining second hard mask layer 320 and first hard mask 315) is present on and/or within active gate trench 305.

[0056] Returning to FIG. 1, method 100 may then proceed from block 109 to block 111, pursuant to which at least a portion of fin 204 may be removed to form an isolation region therein. More specifically, operations pursuant to block 111 may include selectively removing a portion of fin 204 that is exposed proximate a bottom of isolation trench 310, so as to form isolation region 330 therein, as best shown in FIG. 3F. In that regard, selective removal of a portion of fin 204 may be accomplished in any suitable manner. For example, in some embodiments the structure of FIG. 3E may be exposed to wet or dry etching chemistry which is selective to the material of second hard mask layer 320 and to the material of spacer layer 216, but which can remove (e.g., etch) the material of fin 204. In some embodiments this may be accomplished by etching the structure of FIG. 3E with a

chloride (Cl<sub>2</sub>) or hydrogen bromide (HBr) etch chemistry, so as to selectively remove the material of fin 204.

[0057] In any case, the operations of block 111 may result in the selective removal of material of FIN 204, e.g., proximate the bottom of isolation trench 310, resulting in the formation of isolation region 330 as shown in FIG. 3F. As may be appreciated, the depth of isolation region 330 may vary widely, and may have an impact on the degree to which the isolation structure that will be formed therein may electrically isolate an active gate structure (e.g., to be formed in active gate trench 305) from other components/devices which may be formed on or with fin 204 (e.g., adjacent or nearby transistors). In that regard, in some embodiments isolation region has a depth ranging from about 40 to about 200 nanometers (nm), such as from about 50 to about 200 nm, or even about 70nm to about 200nm. Without limitation, in some embodiments isolation region has a depth that extends at least to a portion of fin 204 that is below the bottom of the active regions of fin 204, e.g., below source/drain regions 214.

[0058] Returning to FIG. 1, following the operations of block 111 the method may advance to block 113 pursuant to which a liner may be deposited on the structure of FIG. 3F, e.g., prior to or after the removal of the second hard mask layer 320. For the sake of illustration, the present disclosure focuses on embodiments in which a liner is deposited after the second hard mask layer 320 is removed. In this regard reference made to FIG. 3G, which depicts one example embodiment in which a liner 335 is deposited on the exposed surfaces of first hard mask 315, source/drain contacts 220, spacer layer 216, and the surface of isolation region 330.

[0059] In general, liner 335 is configured to function as an etch stop during the recession of a dielectric material that may be deposited within isolation trench 310 later in the processes described herein. That is, liner 335 may be configured to provide a selective etch with regard to the material(s) that will be used to fill isolation trench 310. For example, in some embodiments liner 335 may be formed from or include a material that is unaffected or substantially unaffected by an etching chemistry which may be applied to remove a (e.g., porous) dielectric material to be deposited within isolation trench 310. In that regard liner 335 may be formed from or include any suitable etch stop material, including but not limited to various metal oxides, nitrides, carbides, and combinations thereof (e.g., silicon dioxide, aluminum

oxide ( $\text{Al}_2\text{O}_3$ ), hafnium oxide ( $\text{HfO}_2$ ), carbon doped silicon nitride, silicon nitride, aluminum nitride etc.). Without limitation, in some embodiment liner 335 is formed from aluminum oxide ( $\text{Al}_2\text{O}_3$ ). In any case, liner 335 may be deposited in any suitable manner, such as via chemical various deposition, physical vapor deposition, sputtering, atomic layer deposition, combinations thereof, and the like.

[0060] Returning to FIG. 1, following the operations of block 113 the method may advance to block 117 pursuant to which an isolation material may be deposited on the structure of FIG. 3G. In this regard reference made to FIG. 3H, which depicts one example embodiment in which an isolation material 340 deposited on the exposed surfaces of liner 335. As shown in the illustrated embodiment, deposition of isolation material 340 may be performed such that isolation material 340 fills isolation trench 310 and isolation region 330 within fin 204.

[0061] In general, isolation material 340 is a non-conductive (i.e., insulating/dielectric) fill that may function to electrically isolate or contribute to the electrical isolation of active gate trench 305 (and an active gate structure to be formed therein) from one or more additional active gates formed on or with fin 204. In that regard isolation material 340 may be or include any suitable non-conductive (dielectric material), such as but not limited to dielectric oxides, nitrides, and carbides. Without limitation, in some embodiments isolation material 340 is or includes a porous dielectric material, such as but not limited to a porous silicon oxide ( $\text{SiO}$ ), porous silicon dioxide ( $\text{SiO}_2$ ), porous carbon doped silicon nitride ( $\text{SiCN}$ ), porous silicon oxynitride, combinations thereof, and the like.

[0062] As used herein, the term “porous dielectric material” refers to dielectric materials that have an as deposited density that is less than about 95% of the full density of its constituent materials. For example, the full density of both silicon oxide ( $\text{SiO}$ ) and silicon dioxide is about 2.65 grams per cubic centimeter ( $\text{g/cm}^3$ ). Therefore in instances where isolation material 340 is a porous silicon oxide or a porous silicon dioxide, the density of isolation material 340 (e.g., as deposited) may be less than about 95% of  $2.65 \text{ g/cm}^3$ , i.e., less than or equal to about  $2.52 \text{ g/cm}^3$ . In some instances, porous silicon oxide is used as isolation material 340. As may be appreciated, in some embodiments the porous dielectric may be capable of being densified (e.g., by annealing or another process), such that its density increases to

greater than 95% of the full density of its constituent materials, resulting in the formation of an isolation dielectric.

[0063] Deposition of isolation material 340 may be performed in any suitable manner. For example, in instances where isolation material 340 is a porous silicon oxide or porous silicon dioxide, deposition of isolation material 340 may be carried out via a conformal or non-conformal silicon deposition, as understood in the art. In any case the result of such operations may be the formation of the structure shown in FIG. 3H, i.e., wherein isolation material extends from the bottom of isolation region 330 at least to a point proximate the opening of isolation trench 310.

[0064] At that point, the resulting article may be optionally polished (e.g., via chemical mechanical planarization or another suitable technique) to remove excess isolation material 340, e.g., such that an upper surface of isolation material 340 above isolation trench 310 is substantially coplanar with surface of liner 335 above active gate trench 305. Of course such polishing is not required, and the present disclosure will for the sake of clarity continue to describe an embodiment in which such polishing is not performed.

[0065] Returning to FIG. 1, following the operations of block 117 the method may proceed to block 119, pursuant to which isolation material 340 may be recessed within isolation trench 310. This concept is best shown in FIG. 3I, which depicts isolation material 340 as being recessed such that an upper surface thereof is below the aperture (not labeled) of isolation trench 340.

[0066] In some embodiments isolation material 340 is recessed such that it has a depth  $d$  within isolation trench 310, wherein the depth  $d$  is defined as the distance between the upper surface of isolation material 340 and the bottom most point of isolation region 330. As will be appreciated from the following discussion, the depth of isolation material 340 within isolation trench 310 may impact the position of a local interconnect which may be formed within isolation trench 310. It may therefore be desirable to recess isolation material 340 such that it has a suitable depth,  $d$ . For example, in some embodiments isolation material 340 may be recessed such that an upper surface thereof is coplanar or substantially coplanar with the upper surface of fin 204. This may be accomplished, for example, by recessing isolation material 340 until it has a depth that is about 5 to about 15% larger than the depth of isolation region 330. Thus for example where isolation region 330 has a depth of about 40 to

about 200 nm, the depth (d) of isolation material 330 may be about 42 to about 220 nm, such as about 45 to about 210 nm.

[0067] Recession of isolation material 340 may be accomplished in any suitable manner, such as by an etching or other selective removal process. For example, in some embodiments isolation dielectric is or includes porous silicon oxide or porous silicon dioxide, and is recessed within isolation trench 310 by subjecting the structure of FIG. 3H to a wet or dry etching chemistry that is selective to liner 335 but which is capable of removing isolation material 340. In non-limiting embodiments, the structure of FIG. 3H is exposed to a dry etching chemistry that is selective to liner 335, but which anisotropically etches isolation material 340. Alternatively, the structure of FIG. 3H may be subject to a wet etching chemistry that anisotropically or isotropically removes isolation material 340, but which is selective to liner 335.

[0068] Returning to FIG. 1, following the operations of block 119 the method may advance to block 121, pursuant to which liner 335 may be removed from the upper surfaces of the structure of FIG. 3I and recessed within isolation trench 310. This concept is best shown in FIG. 3J, which depicts second isolation layer 320 as being removed from the upper surfaces of first hard mask 315 and source/gate contacts 220, and as being recessed within isolation trench 310. As shown in the illustrated embodiment, liner 335 may be recessed within isolation trench 310 such that an upper surface thereof is substantially coextensive with an upper surface of isolation material 340. Alternatively, in some embodiments liner 335 may be recessed within isolation trench 310 such that an upper surface thereof is above an upper surface of isolation material 340. As may be appreciated, this may obviate the need to further recess isolation material 340 (or an isolation dielectric 340') further at a later point in the process, e.g., so as to facilitate deposition of a first work function material.

[0069] Recession of liner 335 may be performed in any suitable manner. For example, in some embodiments recession of liner 335 may be accomplished by exposing the structure of FIG. 3I to an etching chemistry that is selective to first hard mask 315 and spacer layer 216, but which can remove (e.g. etch) the material of liner 335. For example where spacer layer 216 is a nitride and liner 335 is aluminum oxide, recession of liner 335 within isolation trench 310 may be accomplished by exposing the structure of FIG. 3I to a hydrofluoric acid etch chemistry. Of course, use

of a hydrofluoric acid etch is not required, and other methods may be used to recess liner 335 within isolation trench 310.

[0070] Returning to FIG. 1, following the operations of block 121 the method may proceed from block 121 to block 123, pursuant to which operations may be carried out to expose the active gate trench. More specifically, operations may be carried out to remove all or a portion of the plug of first hard mask 315, so as to expose the surface of fin 204 at a bottom of active gate trench 305. This concept is best shown in FIG. 3K, which depicts an embodiment in which first hard mask 315 has been removed, thereby exposing the surface 345 of fin 204 at a region proximate the bottom of active gate trench 305.

[0071] Removal of first hard mask 315 may be accomplished in any suitable manner, such as via an etching process, an ion milling process, a plasma ashing process, combinations thereof, and the like. Without limitation, in some embodiments first hard mask 315 is a carbon hard mask (or another suitable material) and the operations of block 123 include executing a plasma ashing process (e.g., an oxygen plasma ashing process) to remove the carbon hard mask, thereby exposing the surface of fin 204 within active gate trench 204.

[0072] Following the operations of block 123, the method may proceed to optional block 125, pursuant to which isolation material 340 may optionally be densified, e.g., by an annealing or other suitable process. For example in instances where isolation material 340 is a porous silicon oxide or porous silicon dioxide, an annealing process may be executed to increase the density of the porous silicon oxide/dioxide to above 95% of its full density, resulting in the formation of an isolation dielectric 341.

[0073] After the operations of block 125 (or if such operations are not required), method 100 may advance to block 127, pursuant to which one or more local interconnects may be formed within isolation trench 310. As used herein the term “local interconnect” refers to a conductive pathway that may extend between at least two isolation trenches within an integrated circuit device, so as to enable electrical connection of such trenches and/or other components of the device. In that regard reference is made to FIGS. 3L-3N, which stepwise illustrate one example of a method of forming a local interconnect within a isolation trench consistent with the present disclosure.

[0074] As shown in FIG. 3L, in some embodiments the formation of a local interconnect may begin with the further recession of isolation material 340 (or isolation dielectric 341) within isolation trench 310. Alternatively in instances where an upper surface of liner 335 is recessed within isolation trench 310 such that an upper surface thereof is above the upper surface of isolation material/dielectric 340/341, further recession of isolation material/dielectric 340/341 may be omitted. In either case, the result may be the formation of a cup within isolation trench 310, wherein the cup includes sidewalls defined at least in part by liner 335, and a bottom defined at least in part by isolation material/dielectric 340/341, as shown in FIG. 3L. Alternatively in some embodiments the formation of such a cup is not required and may be omitted.

[0075] Following the further recession of isolation material/dielectric 340/341 (or if such recession is omitted), the formation of a local interconnect may continue with the deposition of a work function material 350 within the cup (discussed above) or on the upper surfaces of liner 335 and isolation material/dielectric 340/341, e.g., as shown in FIG. 3M. At the same time, the work function material may be deposited on the surface of fin 204 without active gate trench 305. In this way all or a portion of an active gate structure may be formed within active gate trench 305, and conductive material may be deposited in inactive gate trench 310 and used to form a local interconnect, as discussed below.

[0076] Deposition of work function material 350 may be accomplished in any suitable manner. For example, work function material 350 may be bulk deposited on the exposed surfaces of the structure of FIG. 3L. Subsequently at least a portion of the bulk deposited first work function material 350 may be removed (e.g., via etching), while leaving at least a portion thereof within active gate trench 305 and inactive gate trench 310, as shown in FIG. 3M.

[0077] Work function material 350 may be any suitable material for forming a local interconnect and/or a conductive gate within a semiconductor device. Non-limiting examples of such materials include such as metals (e.g. titanium, tungsten, aluminum, tantalum, cobalt, copper), metal nitrides (e.g., titanium nitride, tantalum nitride, etc.), metal carbides (e.g., titanium aluminum carbide (TiAlC), tantalum aluminum carbide (TaAlC), combinations thereof, and the like.

[0078] As shown in FIG. 3M, in some embodiments the surface of work function material 350 within isolation trench 310 may be coplanar or substantially coplanar with an upper surface of liner 335. In any case, work function material 350 may be configured such that it may form a local interconnect with a work function material  
5 within an adjacent or otherwise nearby isolation or active gate trench, or some other component of a semiconductor device (e.g., a gate voltage controller (VCG)).

[0079] In any case, following the deposition of first work function material 350, the method 100 may proceed from block 127 to block 129, pursuant to which active trench 305 and isolation trench 310 may be filled with a dielectric fill. This concept is  
10 illustrated in FIG. 3N, wherein a dielectric fill 355 is shown as being formed within active trench 305 and isolation trench 310, and as having a surface that is coplanar or substantially coplanar with the surface of source/drain contacts 220. This may be accomplished in any suitable manner, for example, bulk depositing the material of dielectric fill 355, and selectively removing the material of first dielectric fill that is  
15 present on the upper surface of source/drain contacts 220.

[0080] In any case, the dielectric fill 355 may be formed from any suitable dielectric material, such as but not limited to a dielectric oxide, nitride, carbide, combinations thereof, and the like. Non-limiting examples of such materials include silicon nitride, carbon doped silicon nitride (SiCN), silicon oxynitride, and silicon dioxide.

20 [0081] At this point the operations of method 100 may be considered complete, and the method may proceed from block 129 to block 131 and end.

[0082] Another aspect of the present disclosure relates to semiconductor devices including one or more single or multi-gate transistor elements having the structure shown in FIG. 3N. Without limitation, in some embodiments the semiconductor  
25 devices described herein include a master fin 204 that includes at least a first and a second active transistor formed thereon, wherein each of said first and second active transistors includes an active gate trench including a gate structure, and at least first and second gate contacts formed above corresponding first and second source/drain regions within the master fin.

30 [0083] In addition, the semiconductor devices described herein may include an isolation structure formed on the master fin and between the first and second active transistors, wherein the isolation structure is to electrically isolate the first active transistor from the second active transistor. In some embodiments the isolation

structure may include an isolation trench formed between third and fourth gate contacts, wherein the isolation trench extending to an isolation region formed in said master fin. In some embodiments the isolation trench may be partially filled with a recessed isolation material, as described above. The upper surface of the recessed isolation material may be recessed below the aperture of the isolation trench.

[0084] In some embodiments, the isolation structure further includes a etch stop layer formed that is present between the recessed isolation material and the surface of the master fin, as well as between the recessed isolation material and a sidewall of the third and fourth source/drain contacts, as described above. Moreover as previously described, a first work function material may be present within the isolation trench (e.g., within a cup defined by the etch stop layer and an upper surface of the recessed dielectric material). In such instances the first work function material may be configured to function as a local interconnect, e.g., between nearby transistors and/or other components of the semiconductor device. In further embodiments, the isolation trench may also be filled with a first dielectric fill, e.g., which may extend from an upper surface of the first work function metal to a region proximate the aperture of the isolation trench.

[0085] In additional embodiments, the gate structure of each active transistor may include a second work function material, which may be the same as or different from the first work function material. In addition, in some embodiments the gate structure may include a second dielectric fill which is formed above an upper surface of the second work function material. In some embodiments the second dielectric fill extends at least to a region proximate the aperture of the active gate trench. The second dielectric fill in some embodiments is the same as or different from the first dielectric fill, as noted above. Without limitation, in some embodiments the second dielectric fill is formed from or includes a high-k dielectric.

[0086] Reference is now made to FIG. 4, which depicts one example of a semiconductor device consistent with the present disclosure. As shown, semiconductor device 400 includes a plurality of fins 204<sub>1</sub>-204<sub>z</sub>, wherein z is an integer greater than 2. Each of fins 204<sub>1</sub>-204<sub>n</sub> may be a master fin that includes or otherwise supports a plurality of active single or multi-gate transistors 501, wherein at least two of active transistors 501 are separated by an isolation structure 502 consistent with the present disclosure. That is, each of active transistors 501 may

include first and second source/drain contacts, and an active gate trench including an active gate structure, wherein the first and second source/drain contacts are formed above respective source/drain regions within one of fins 204<sub>1</sub>-204<sub>z</sub>, as previously described. Likewise each isolation structure 502 may include third and fourth  
5 source/drain contacts and an isolation trench there between, the isolation trench including an isolation material/dielectric recessed therein, and a first work function material 350 formed on the isolation material/dielectric, as previously described. As shown in the embodiment of FIG. 4, first work function material 350 may in some embodiments be used to form local interconnects 503 that may electrically connect  
10 active transistors 501 to one or more additional components, such as a voltage gate control (VGC) source. As may be appreciated, use of local interconnects 503 may enable the connection of active transistors 501 to the VCG through nearby isolation structures, which may not have been possible using prior replacement gate techniques.

[0087] Another aspect of the present disclosure relates to a computing device  
15 including semiconductor devices consistent with the present disclosure. In this regard reference is made to FIG. 5, which illustrates a computing device 500 in accordance with various embodiments of the present disclosure. As shown, computing device 500 includes motherboard 802, which may include various components such as but not limited a processor 404, communications circuitry (COMMS) 506, any or all of  
20 which may be physically and electronically coupled with motherboard 502.

[0088] Depending on its application, computing device 500 may also include other components, such as but not limited to volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen controller, a battery,  
25 various codecs, various sensors (e.g., a global positioning system (GPS), accelerometer, gyroscope, etc.), one or more speakers, a camera, and/or a mass storage device.

[0089] COMMS 406 may be configured to enable wired or wireless communication for the transfer of data to and from the computing device 400. In some embodiments,  
30 COMMS 406 may be configured to enable wireless communications via any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE),

EV-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond.

[0090] Semiconductor devices such as those previously described may be included in integrated circuit dies that may be present in various components of computing device 500. For example, in some embodiments processor 504 may include an integrated circuit die that includes a plurality of active single or multi-gate transistors that are formed on a common master fin, and which are electrically isolated from one another using an isolation structure as previously described. Likewise, COMMS 406 may include an integrated circuit die that may include one or more semiconductor devices consistent with the present disclosure. Moreover, various other memories of computing device 500 (e.g., DRAM, ROM, mass storage, etc.) may be made up of or include semiconductor devices consistent with the present disclosure.

[0091] Computing device 500 may be any or a wide variety of computing devices, including but not limited to a laptop computer, a netbook computer, a notebook computer, an ultra book, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder, combinations thereof, and the like. Of course such devices are enumerated for the sake of example only, and computing device 500 may be any suitable type of mobile or stationary electronic device.

#### [0092] ADDITIONAL EMBODIMENTS

[0093] The following examples represent additional non-limiting embodiments of the present disclosure.

[0094] **Example 1:** According to this example there is provided a method of forming a semiconductor device, including: removing a plurality of gates from a workpiece including a substrate, a master fin, and the plurality of dummy gates formed on the master fin, thereby forming a plurality of trenches; forming at least a first active gate trench, a second active gate trench, and an isolation trench from the plurality of trenches, the isolation trench being between the first and second active gate trenches, wherein:

forming the isolation trench includes forming an isolation region within the fin proximate a bottom of at least one of the plurality of trenches, and forming a recessed

isolation dielectric within the isolation trench and the isolation region; the isolation trench includes an aperture; and an upper surface of the recessed isolation dielectric is below the aperture.

5     **[0095] Example 2:** This example includes any or all of the features of example 1, and further includes forming a local interconnect within the isolation trench.

**[0096] Example 3:** This example includes any or all of the features of example 2, wherein the local interconnect includes a work function material.

10   **[0097] Example 4:** This example includes any or all of the features of example 2, wherein the local interconnect has an upper surface that is below the aperture, and the method further includes filling the isolation trench with a dielectric fill.

**[0098] Example 5:** This example includes any or all of the features of example 1, and further includes, prior to forming the recessed isolation dielectric, forming a liner within the isolation trench and the isolation region.

15   **[0099] Example 6:** This example includes any or all of the features of example 5, wherein the liner includes a metal oxide, metal nitride, metal carbide, or a combination thereof.

**[00100] Example 7:** This example includes any or all of the features of example 2, and further includes forming an active gate structure within at least one of the first and second active gate trenches.

20   **[00101] Example 8:** This example includes any or all of the features of example 7, wherein the active gate structure includes a work function material.

**[00102] Example 9:** This example includes any or all of the features of any one of examples 7 and 8, wherein an upper surface of the active gate structure is below an aperture of the first or second active gate trench.

25   **[00103] Example 10:** This example includes any or all of the features of example 9, further including filling the first or second active gate trench with a dielectric fill.

30   **[00104] Example 11:** This example includes any or all of the features of any one of examples 1 to 10, wherein the workpiece further includes a plurality of source/drain contacts, wherein at least one of the source/drain contacts is between the first active gate trench and the isolation trench, and at least one of the source/drain contacts is between the second active gate trench and the isolation trench.

**[00105] Example 12:** This example includes any or all of the features of example 11, wherein the workpiece further includes a plurality of source/drain regions, wherein at least one source drain region is formed below each of the plurality of source/drain contacts.

- 5 **[00106] Example 13:** This example includes any or all of the features of any one of examples 1 to 10, wherein: the workpiece further includes a plurality of source/drain contacts and a plurality of source/drain regions formed under the plurality of source/drain contacts; and forming the first active gate trench, second active gate trench, and isolation trench includes: forming a mask within the plurality  
10 of trenches; and removing a portion of the mask to expose at least one of the plurality of trenches that is to become an isolation trench, a remaining portion of the mask protecting at least two of the plurality of trenches that are to become the first and second active gate trenches.

- [00107] Example 14:** This example includes any or all of the features of example  
15 13, wherein forming the mask includes: depositing a first hard mask within the plurality of trenches; and depositing a second hard mask on the first hard mask.

**[00108] Example 15:** This example includes any or all of the features of example 14, wherein the first hard mask is a carbon hard mask, and the second hard mask is a silicon containing hard mask.

- 20 **[00109] Example 16:** This example includes any or all of the features of example 15, wherein the second hard mask is a silicon anti reflective coating.

**[00110] Example 17:** This example includes any or all of the features of any one of examples 13 to 16, wherein the workpiece further includes a spacer formed on sidewalls of the plurality of source/drain contacts.

- 25 **[00111] Example 18:** This example includes any or all of the features of any one of examples 1 to 18, wherein forming the recessed isolation dielectric within the isolation trench and the isolation region includes: depositing an isolation material within the isolation trench and the isolation region; and recessing the isolation material within the isolation trench, thereby defining the recessed isolation dielectric.

- 30 **[00112] Example 19:** This example includes any or all of the features of example 18, wherein the isolation material is a porous dielectric material.

**[00113] Example 20:** This example includes any or all of the features of example 19, wherein the porous dielectric material is selected from the group consisting of porous silicon oxide, porous silicon dioxide, porous carbon doped silicon nitride (SiCN), porous silicon oxynitride, or a combination thereof.

5 **[00114] Example 21:** This example includes any or all of the features of any one of examples 19 and 20, wherein forming the recessed isolation dielectric further includes annealing the porous dielectric material.

**[00115] Example 22:** This example includes any or all of the features of example 22, wherein the annealing is performed after recessing the isolation material within  
10 the isolation trench.

**[00116] Example 23:** This example includes any or all of the features of any one of examples 21 and 22, wherein the annealing increases the density of the porous dielectric material.

**[00117] Example 24:** According to this example there is provided an an integrated  
15 circuit device, including: a master fin having a first active transistor, second active transistor, and an isolation structure formed thereon; wherein: the isolation structure is between first and second active transistors and is to electrically isolate the first active transistor from the second active transistor; the isolation structure includes an isolation trench, an isolation region formed in the fin proximate a bottom of the  
20 isolation trench, and recessed isolation dielectric in the isolation trench and the isolation region; the isolation trench has an aperture; and an upper surface of the recessed isolation dielectric is below the aperture.

**[00118] Example 25:** This example includes any or all of the features of example 24, further including a local interconnect at least partially formed within the isolation  
25 trench.

**[00119] Example 26:** This example includes any or all of the features of example 25, wherein the local interconnect includes a work function material formed on the upper surface of the recessed isolation dielectric.

**[00120] Example 27:** This example includes any or all of the features of any one  
30 of examples 24 to 26, further including a dielectric fill on the recessed isolation dielectric and within the isolation trench.

[00121] **Example 28:** This example includes any or all of the features of any one of examples 24 to 27, further including a liner within the isolation trench and the isolation region, at least a portion of the liner being between the recessed isolation dielectric and the master fin.

- 5 [00122] **Example 29:** This example includes any or all of the features of example 29, wherein the liner includes a metal oxide, metal nitride, metal carbide, or a combination thereof.

- [00123] **Example 30:** This example includes any or all of the features of example 24, wherein the first and second active transistors comprise first and second active gate trenches, respectively, wherein a first active gate structure is present in the first active gate trench, and a second active gate structure is present in the second active gate trench.

- [00124] **Example 31:** This example includes any or all of the features of example 30, wherein the first and second active gate structures each comprise a work function material.

- [00125] **Example 32:** This example includes any or all of the features of any one of examples 30 and 31, wherein: the first and second active gate structures have first and second upper surfaces, respectively; the first and second active gate trenches have first and second active gate trench apertures, respectively; and the first and second upper surfaces are below the first and second active gate trench apertures, respectively.

- [00126] **Example 33:** This example includes any or all of the features of example 32, further including a dielectric fill on the first and second active gate structures and within the first and second active gate trenches.

- 25 [00127] **Example 34:** This example includes any or all of the features of any one of examples 24 to 33, wherein the first and second active transistors each further includes a plurality of source/drain contacts, wherein at least one source drain region is formed below each of the plurality of source/drain contacts.

- [00128] **Example 35:** This example includes any or all of the features of example 34, further including a spacer formed on sidewalls of the plurality of source/drain contacts.

[00129] **Example 36:** This example includes any or all of the features of any one of examples 24 to 35, wherein the isolation dielectric includes a densified porous dielectric material.

5 [00130] **Example 37:** This example includes any or all of the features of example 28, wherein: the upper surface of the recessed isolation dielectric is below an upper surface of the liner, such that cup is defined within the isolation trench by the upper surface of the recessed isolation dielectric and the liner.

[00131] **Example 38:** This example includes any or all of the features of example 37, further including a local interconnect within the isolation trench, wherein at least a  
10 portion of the local interconnect is formed within the cup.

[00132] **Example 39:** This example includes any or all of the features of example 38, wherein the local interconnect includes a work function material.

[00133] **Example 40:** This example includes any or all of the features of any one of examples 38 and 39, wherein an upper surface of the local interconnect is below or  
15 substantially coplanar with the upper surface of the liner.

[00134] **Example 41:** This example includes any or all of the features of any one of examples 25, 26, 38 and 39, wherein the local interconnect is coupled to a voltage gate control source.

[00135] The terms “over,” “under,” “between,” and “on,” are often used herein to  
20 refer to a relative position of one material layer or component with respect to other material layers or components. For example, one layer disposed on (e.g., over or above) or under (below) another layer may be directly in contact with the other layer, or may have one or more intervening layers. Moreover one layer disposed between two other layers may be directly in contact with the two other layers or may be  
25 separated by one or more of the other layers, e.g., by one or more intervening layers. Similarly unless expressly indicated to the contrary, one feature that is adjacent to another feature may be in direct contact with the adjacent feature, or may be separated from the adjacent feature by one or more intervening features. In contrast, the terms “directly on” or “directly below” are used to denote that one material layer is in direct  
30 contact with an upper surface or a lower surface, respectively, of another material layer. Likewise, the term “directly adjacent” means that two features are in direct contact with one another.

[00136] The terms and expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described (or portions thereof), and it is recognized that various modifications are possible within the scope of the claims. Accordingly, the claims are intended to cover all such equivalents. Various features, aspects, and embodiments have been described herein. The features, aspects, and embodiments are susceptible to combination with one another as well as to variation and modification, as will be understood by those having skill in the art. The present disclosure should, therefore, be considered to encompass such combinations, variations, and modifications.

CLAIMS

What is claimed is:

- 5     1.     A method of forming a semiconductor device, comprising:  
            removing a plurality gates from a workpiece comprising a substrate, a master  
fin, and said plurality of dummy gates formed on said master fin, thereby forming a  
plurality of trenches;  
            forming at least a first active gate trench, a second active gate trench, and an  
10    isolation trench from said plurality of trenches, the isolation trench being between the  
first and second active gate trenches,  
            wherein:  
                forming the isolation trench comprises forming an isolation region  
within said fin proximate a bottom of at least one of said plurality of trenches, and  
15    forming a recessed isolation dielectric within said isolation trench and said isolation  
region;  
                said isolation trench comprises an aperture; and  
                an upper surface of said recessed isolation dielectric is below said  
aperture.  
20
2.     The method of claim 1, further comprising forming a local interconnect within  
said isolation trench.
3.     The method of claim 2, wherein said local interconnect has an upper surface  
25    that is below said aperture, and the method further comprises filling said isolation  
trench with a dielectric fill.
4.     The method of claim 1, further comprising, prior to forming said recessed  
isolation dielectric, forming a liner within said isolation trench and said isolation  
30    region.
5.     The method of claim 4, wherein said liner comprises a metal oxide, metal  
nitride, metal carbide, or a combination thereof.

6. The method of claim 2, further comprising forming an active gate structure within at least one of said first and second active gate trenches.

5 7. The method of claim 6, wherein an upper surface of said active gate structure is below an aperture of said first or second active gate trench.

8. The method of claim 7, further comprising filling said first or second active gate trench with a dielectric fill.

10

9. The method of any one of claims 1 to 8, wherein said workpiece further comprises a plurality of source/drain contacts, wherein at least one of said source/drain contacts is between said first active gate trench and said isolation trench, and at least one of said source/drain contacts is between said second active gate trench and said isolation trench.

15

10. The method of claim 9, wherein said workpiece further comprises a plurality of source/drain regions, wherein at least one source drain region is formed below each of said plurality of source/drain contacts.

20

11. The method of any one of claims 1 to 8, wherein:  
said workpiece further comprises a plurality of source/drain contacts and a plurality of source/drain regions formed under the plurality of source/drain contacts;  
and

25 forming said first active gate trench, second active gate trench, and isolation trench comprises:

forming a mask within said plurality of trenches; and

removing a portion of said mask to expose at least one of said plurality of trenches that is to become an isolation trench, a remaining portion of said mask protecting at least two of said plurality of trenches that are to become said first and second active gate trenches.

30

12. The method of claim 11, wherein forming said mask comprises:  
depositing a first hard mask within said plurality of trenches; and

depositing a second hard mask on the first hard mask.

13. The method of claim 12, wherein the first hard mask is a carbon hard mask, and the second hard mask is a silicon containing hard mask.

5

14. The method of any one of claims 1 to 8, wherein forming said recessed isolation dielectric within said isolation trench and said isolation region comprises:  
depositing an isolation material within said isolation trench and said isolation region; and

10 recessing said isolation material within said isolation trench, thereby defining said recessed isolation dielectric.

15. An integrated circuit device, comprising:

a master fin having a first active transistor, second active transistor, and an isolation structure formed thereon;

15 wherein:

the isolation structure is between first and second active transistors and is to electrically isolate the first active transistor from the second active transistor;

the isolation structure includes an isolation trench, an isolation region  
20 formed in said fin proximate a bottom of said isolation trench, and recessed isolation dielectric in the isolation trench and the isolation region;

the isolation trench has an aperture; and

an upper surface of the recessed isolation dielectric is below said aperture.

25

16. The integrated circuit device of claim 15, further comprising a local interconnect at least partially formed within said isolation trench.

17. The integrated circuit device of claim 16, wherein said local interconnect  
30 comprises a work function material formed on the upper surface of said recessed isolation dielectric.

18. The integrated circuit of claim 15, further comprising a dielectric fill on said recessed isolation dielectric and within said isolation trench.

19. The integrated circuit device of claim 15, further comprising a liner within said isolation trench and said isolation region, at least a portion of the liner being between the recessed isolation dielectric and said master fin.

5

20. The integrated circuit device of any one of claims 15 to 18, wherein said first and second active transistors comprise first and second active gate trenches, respectively, wherein a first active gate structure is present in said first active gate trench, and a second active gate structure is present in said second active gate trench.

10

21. The integrated circuit device of claim 20, wherein:

said first and second active gate structures have first and second upper surfaces, respectively;

15 said first and second active gate trenches have first and second active gate trench apertures, respectively; and

said first and second upper surfaces are below said first and second active gate trench apertures, respectively.

22. The integrated circuit device of any one of claims 15 to 18, wherein said first and second active transistors each further comprises a plurality of source/drain contacts, wherein at least one source drain region is formed below each of said plurality of source/drain contacts.

23. The integrated circuit device of claim 19, wherein:  
25 the upper surface of said recessed isolation dielectric is below an upper surface of said liner, such that cup is defined within said isolation trench by the upper surface of said recessed isolation dielectric and said liner;

the device further comprises a local interconnect within said isolation trench, wherein at least a portion of said local interconnect is formed within said cup.

30

24. The integrated circuit device of any one of claims 16, 17, 19, and 23, wherein said local interconnect is coupled to a voltage gate control source.

25. The integrated circuit device of claim 22, further comprising a spacer formed on sidewalls of each of said plurality of source/drain contacts.

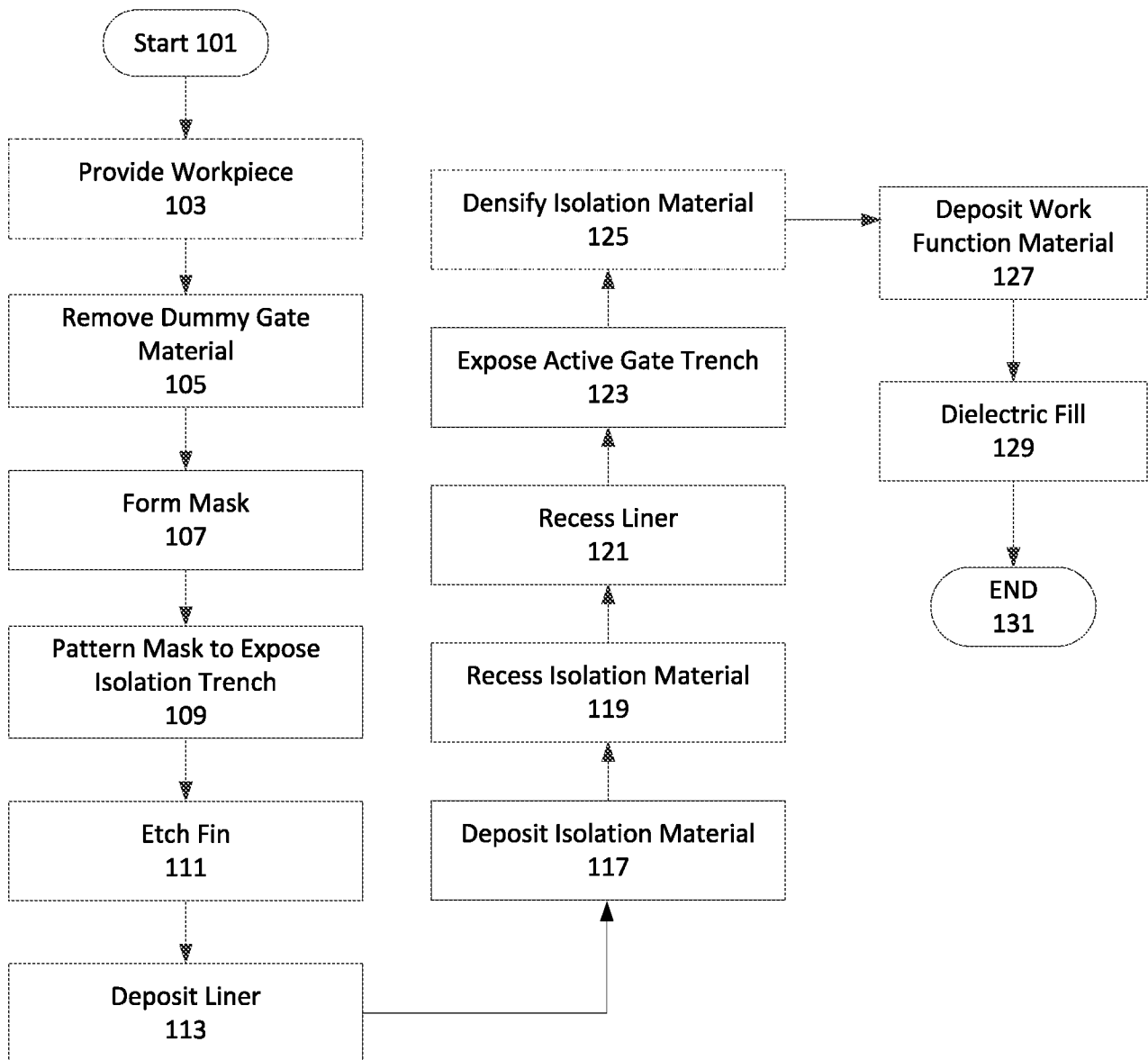
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FIG. 1

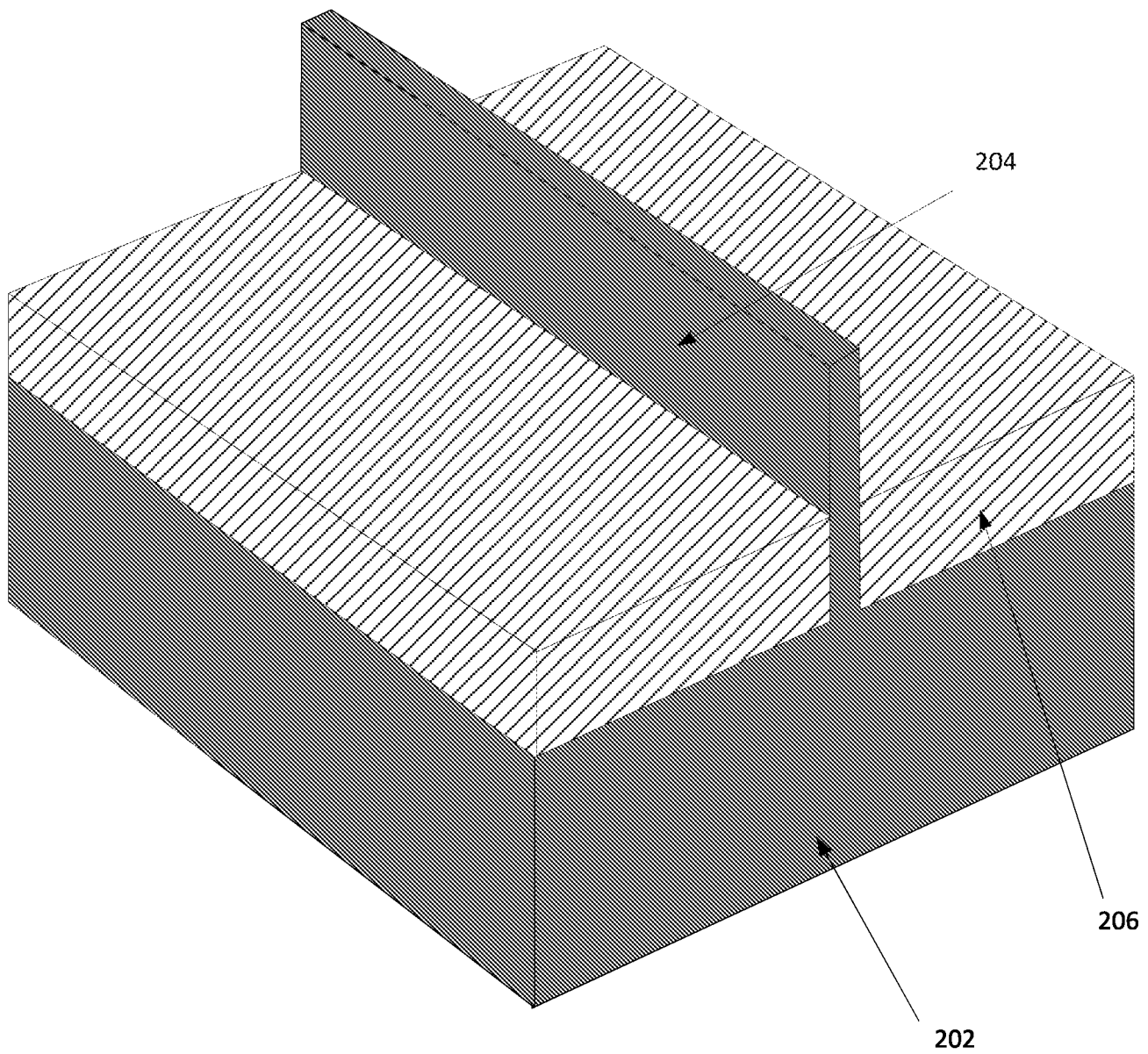
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FIG. 2A

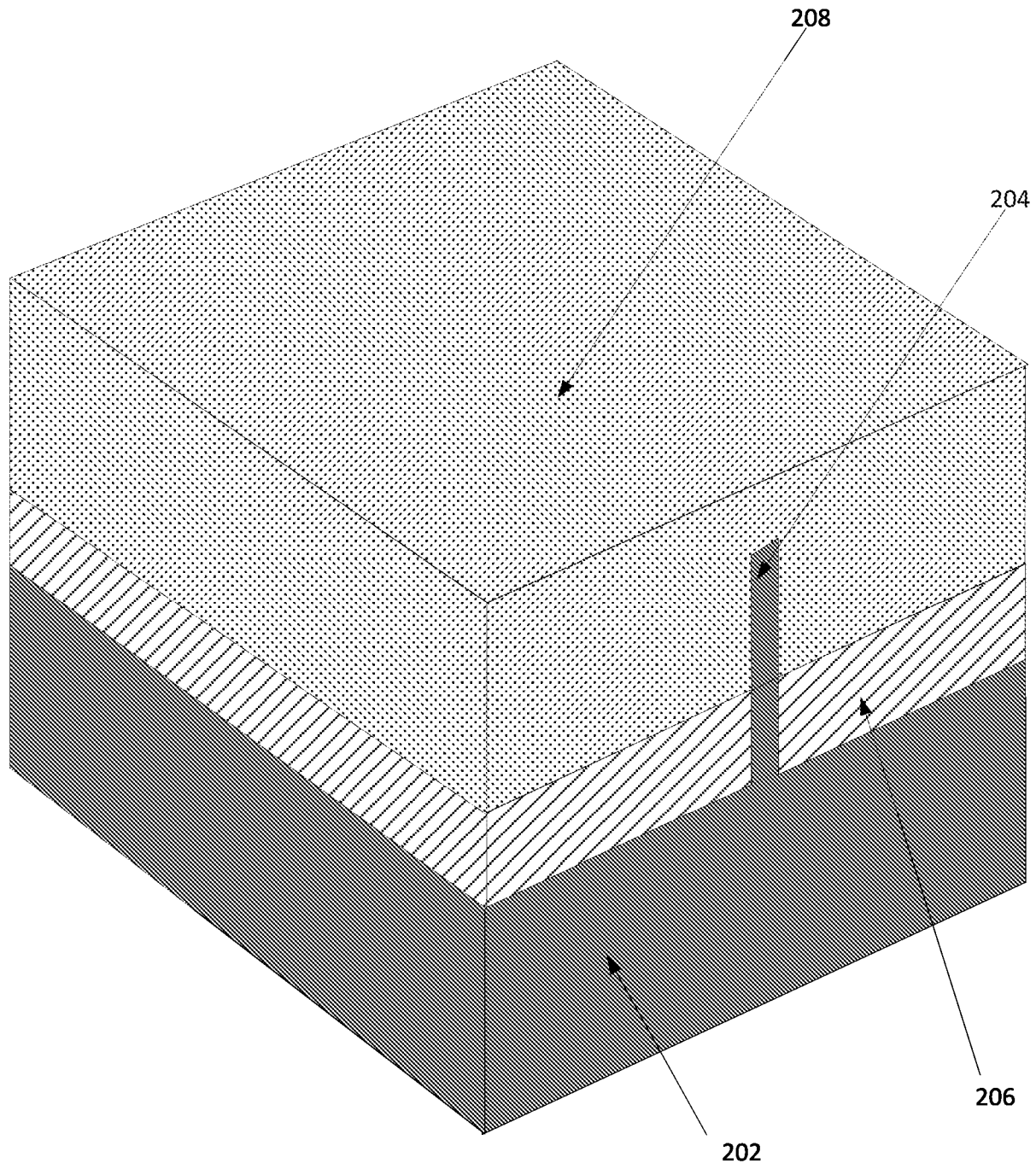
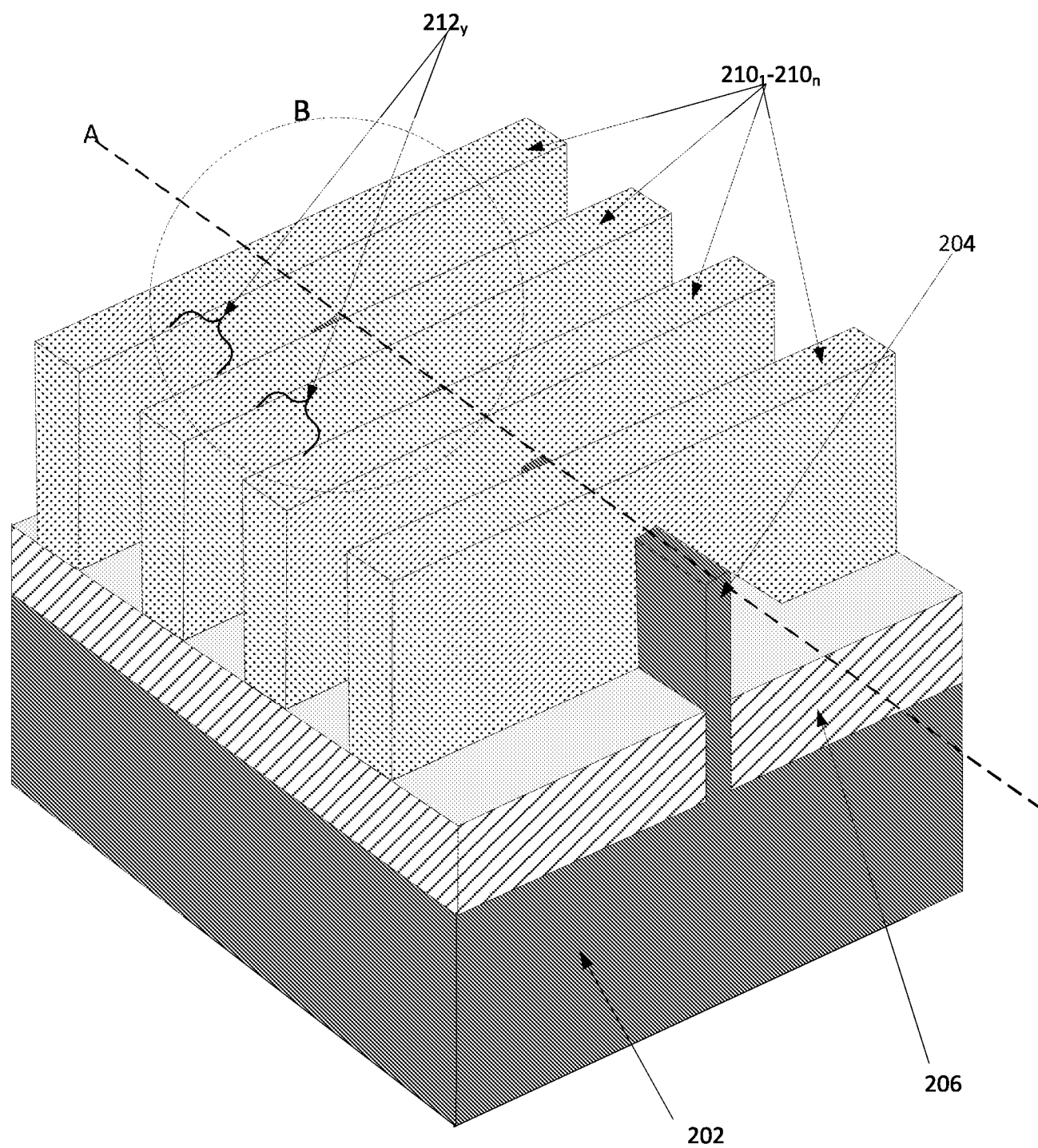


FIG. 2B



**FIG. 2C**

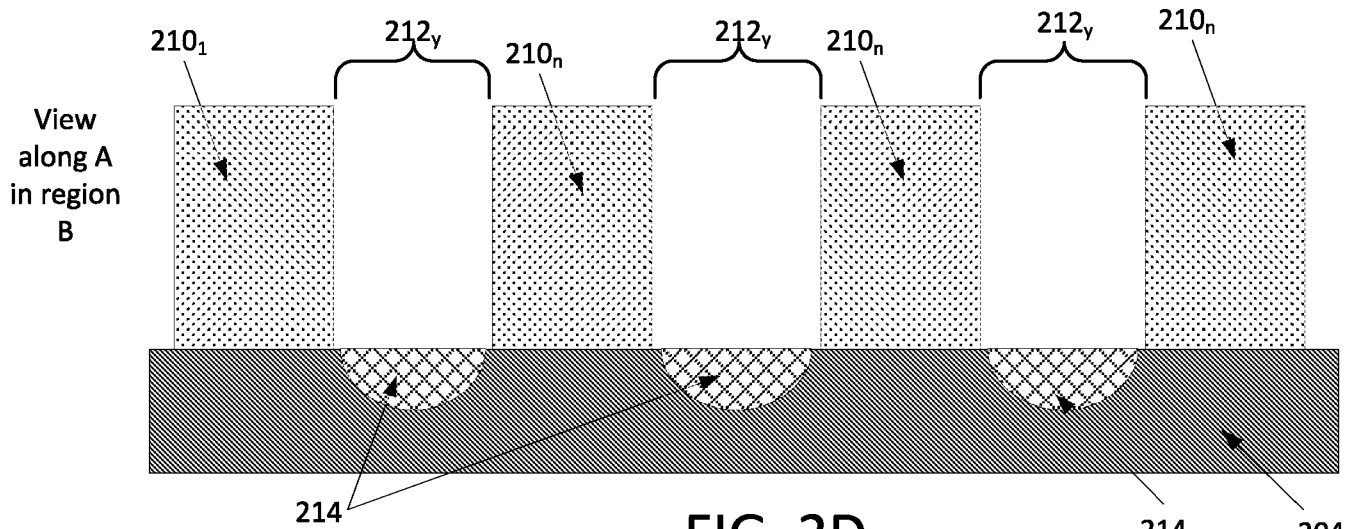


FIG. 2D

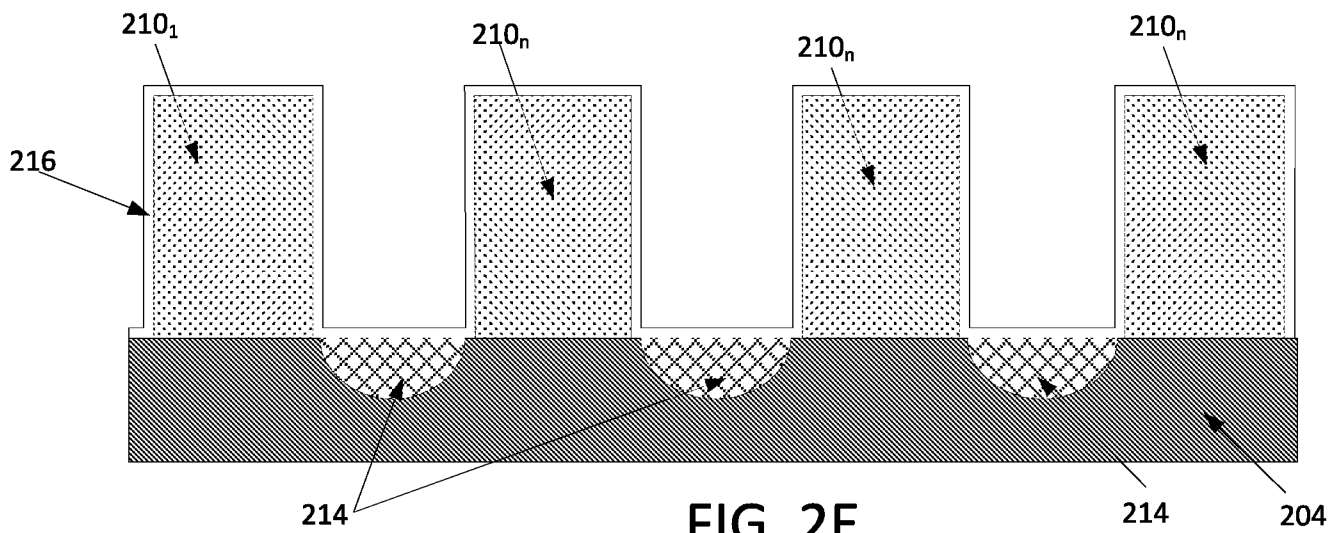


FIG. 2E

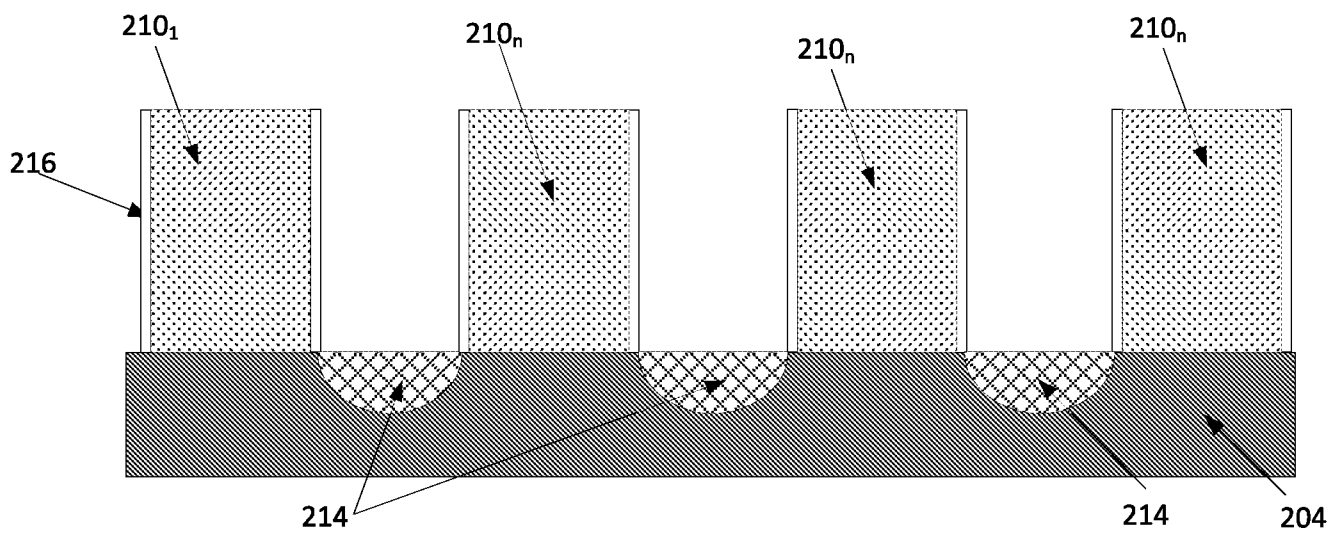


FIG. 2F

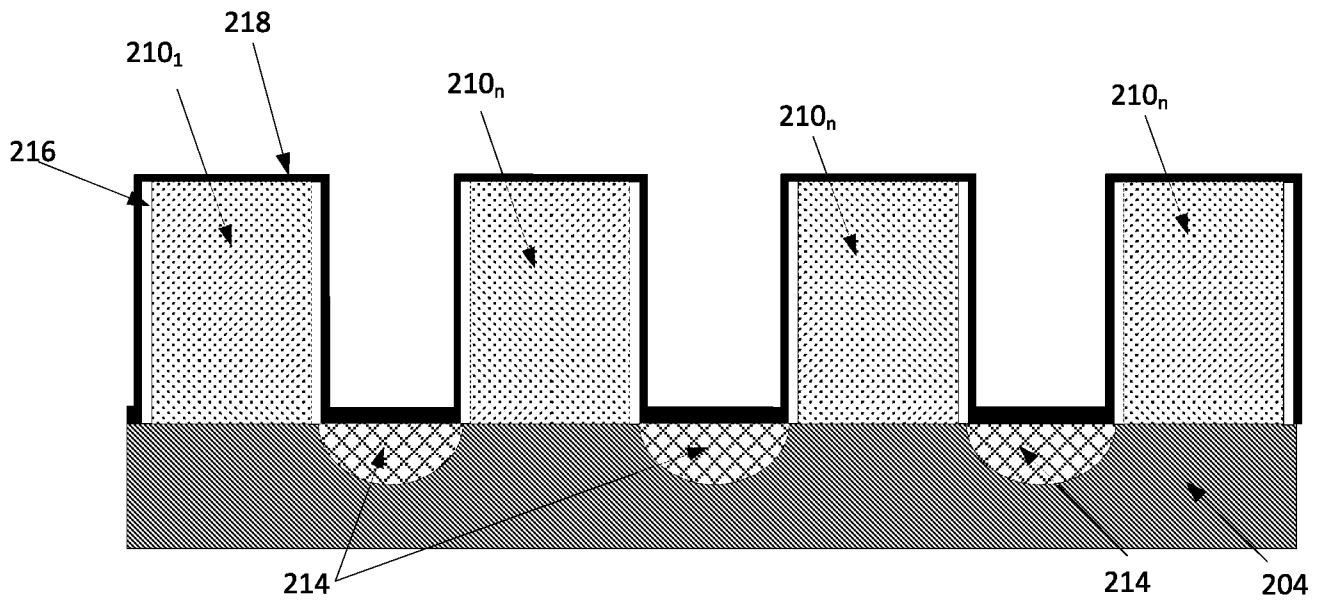


FIG. 2G

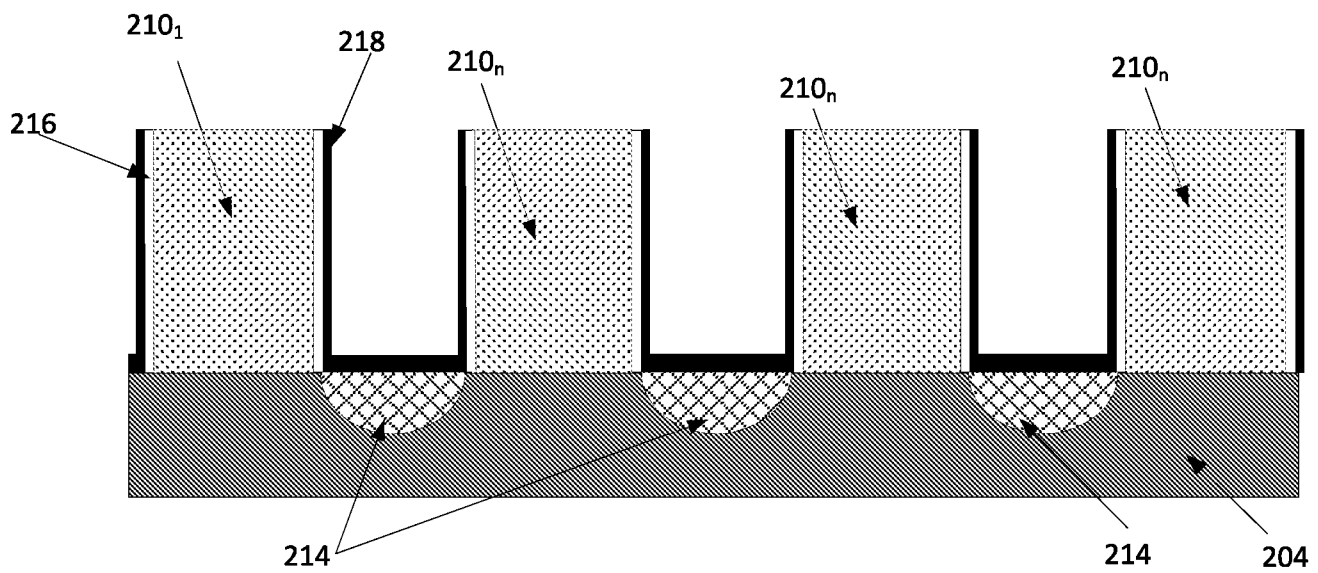


FIG. 2H

250

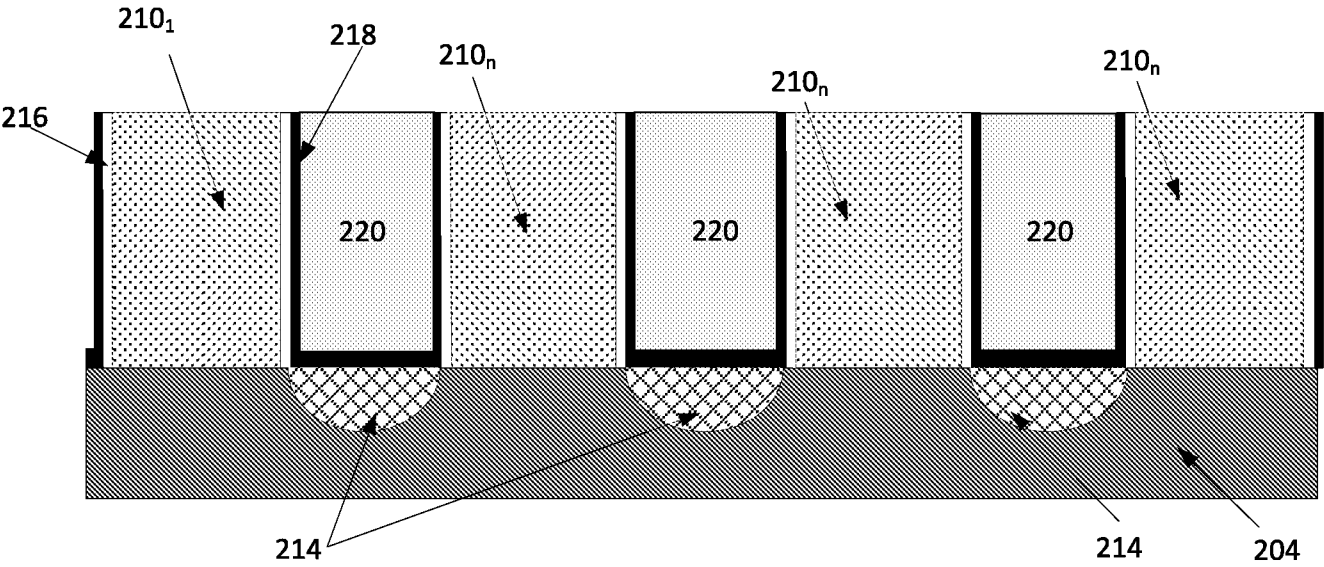


FIG. 21

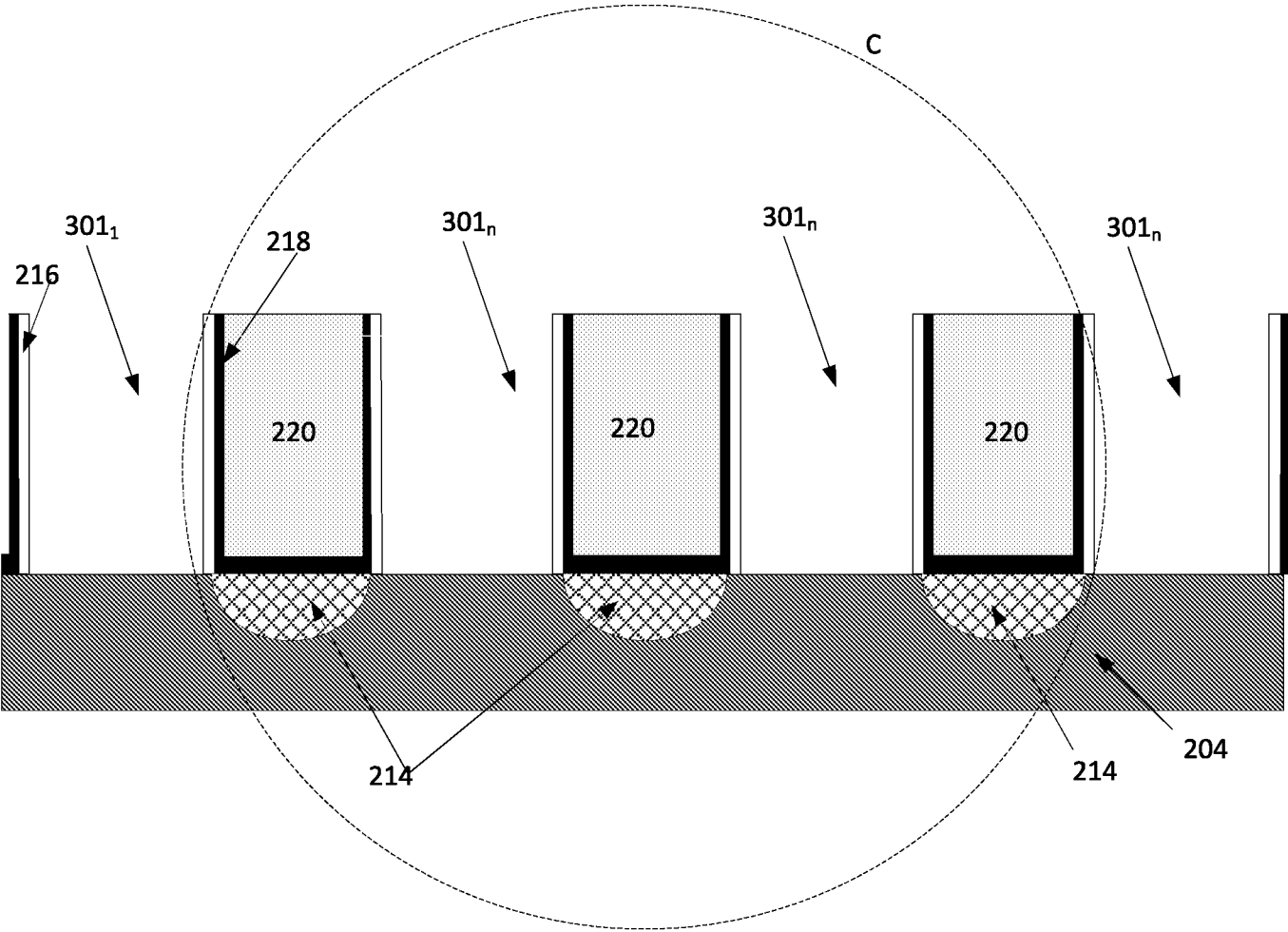


FIG. 3A

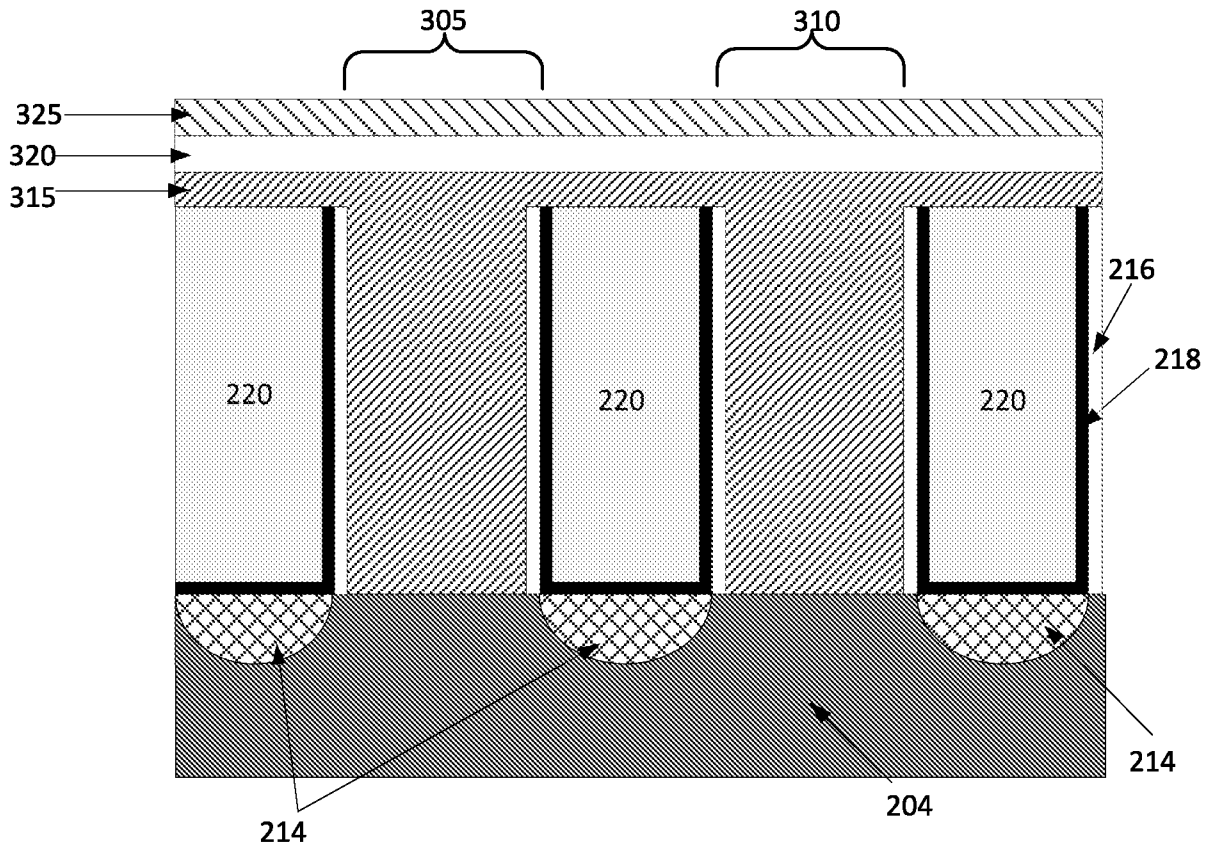


FIG. 3B

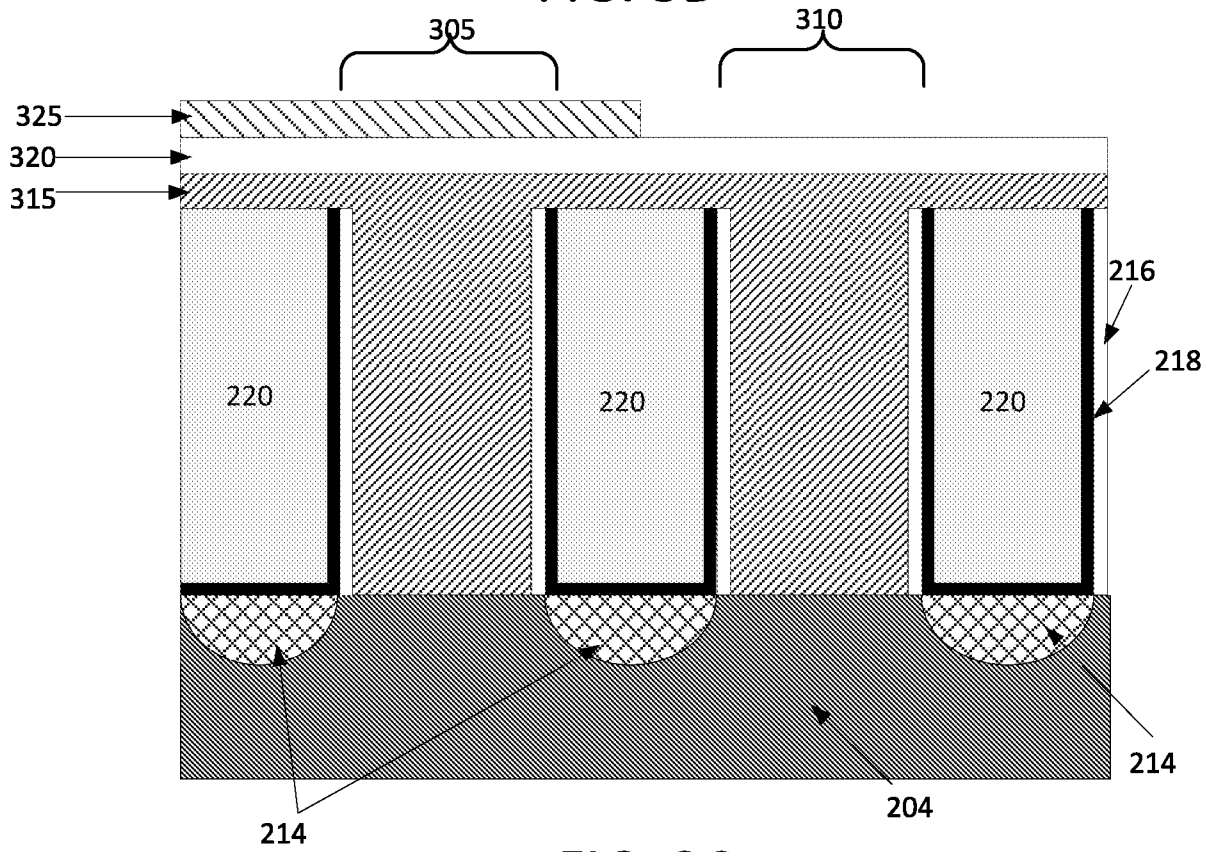


FIG. 3C

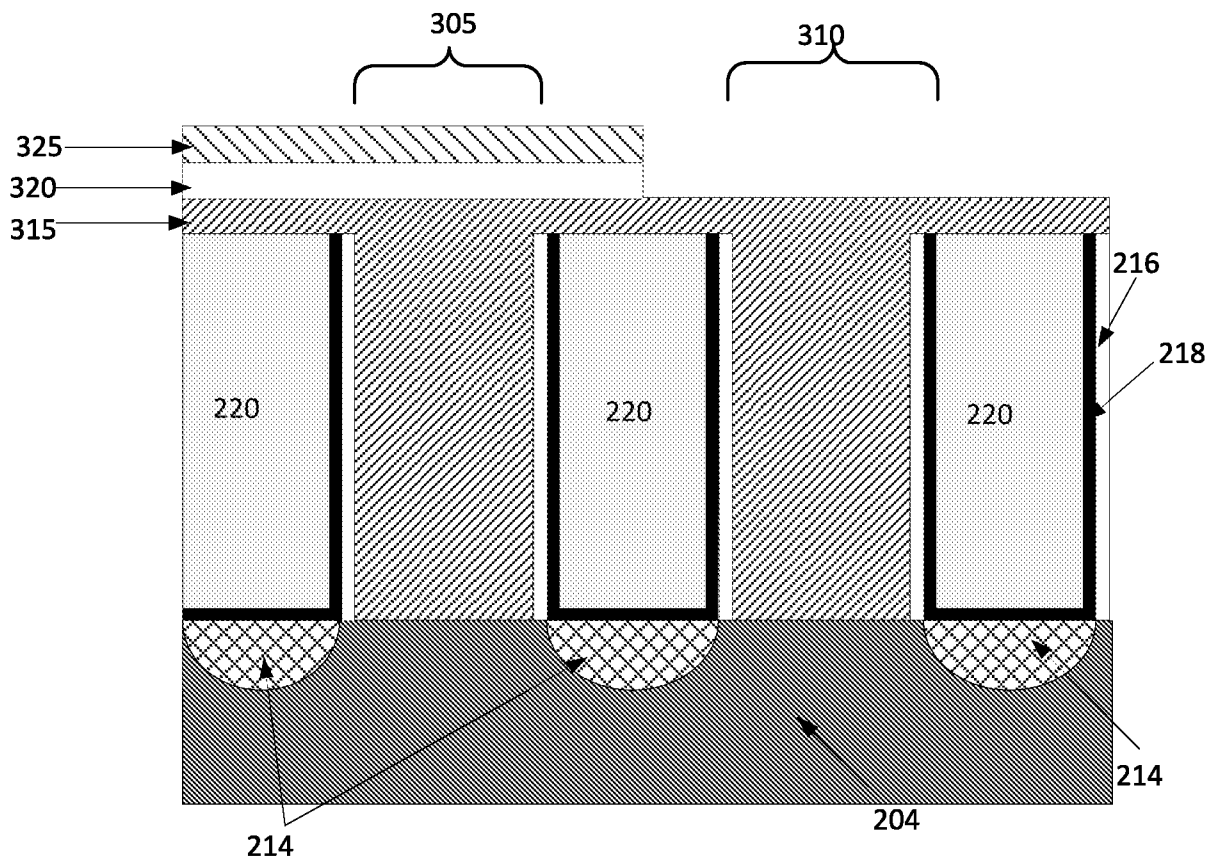


FIG. 3D

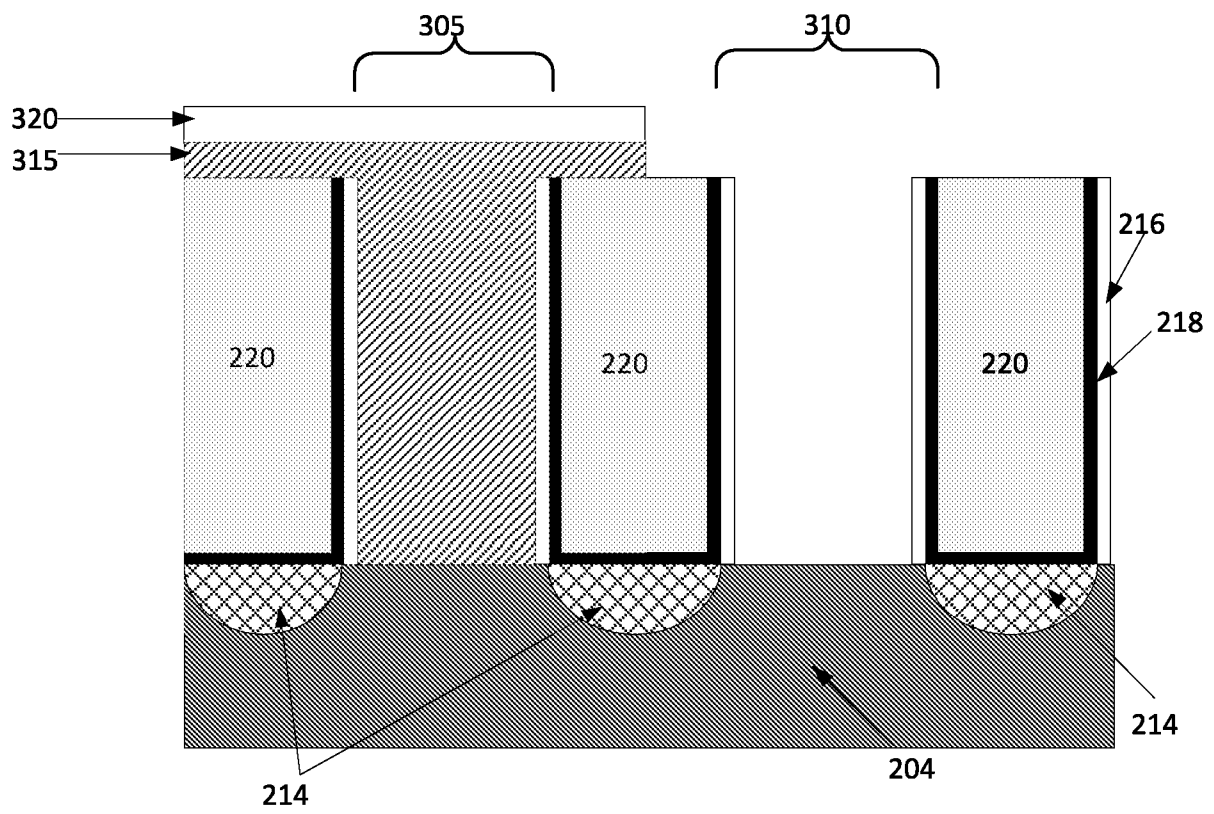


FIG. 3E

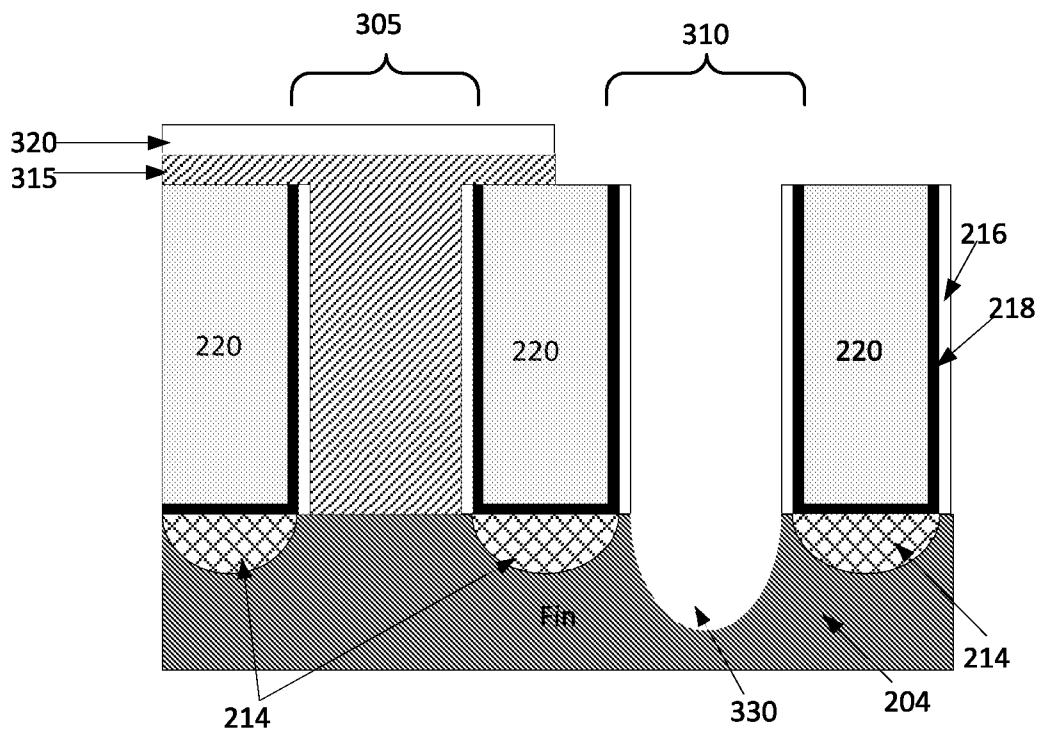


FIG. 3F

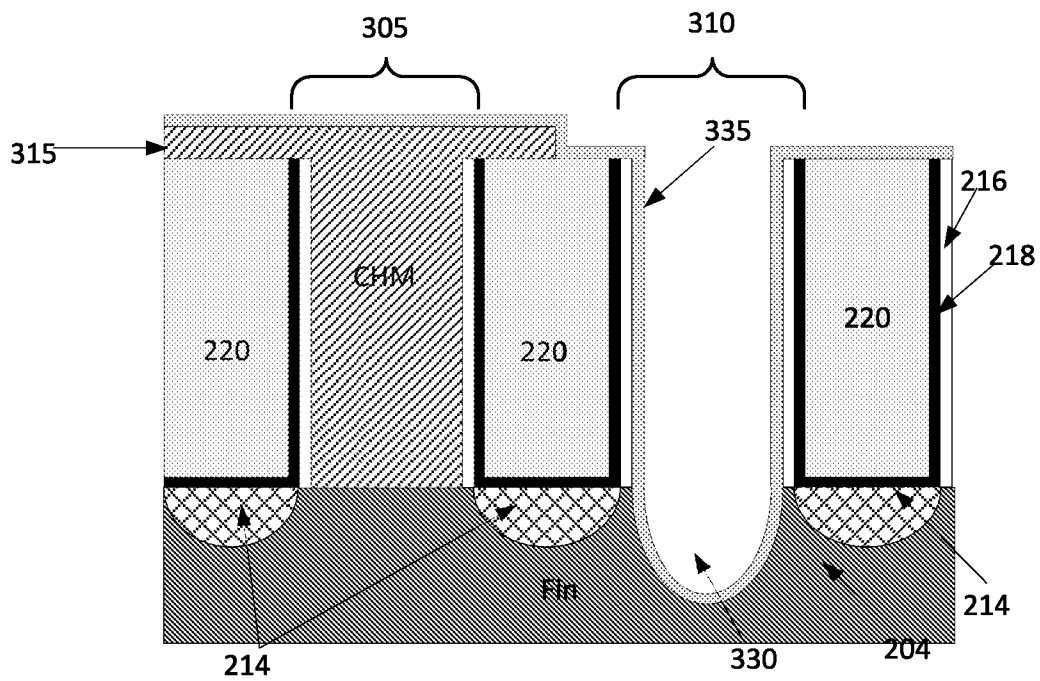


FIG. 3G

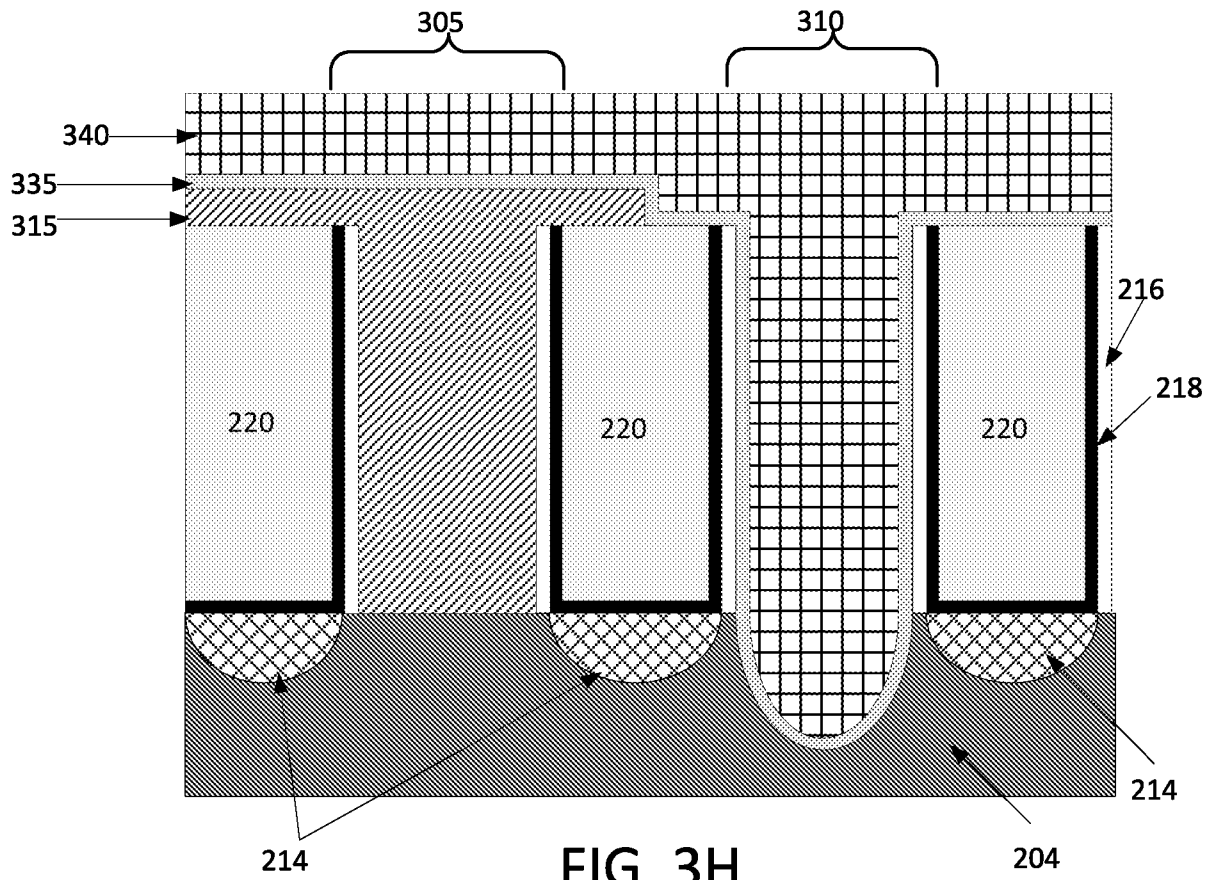


FIG. 3H

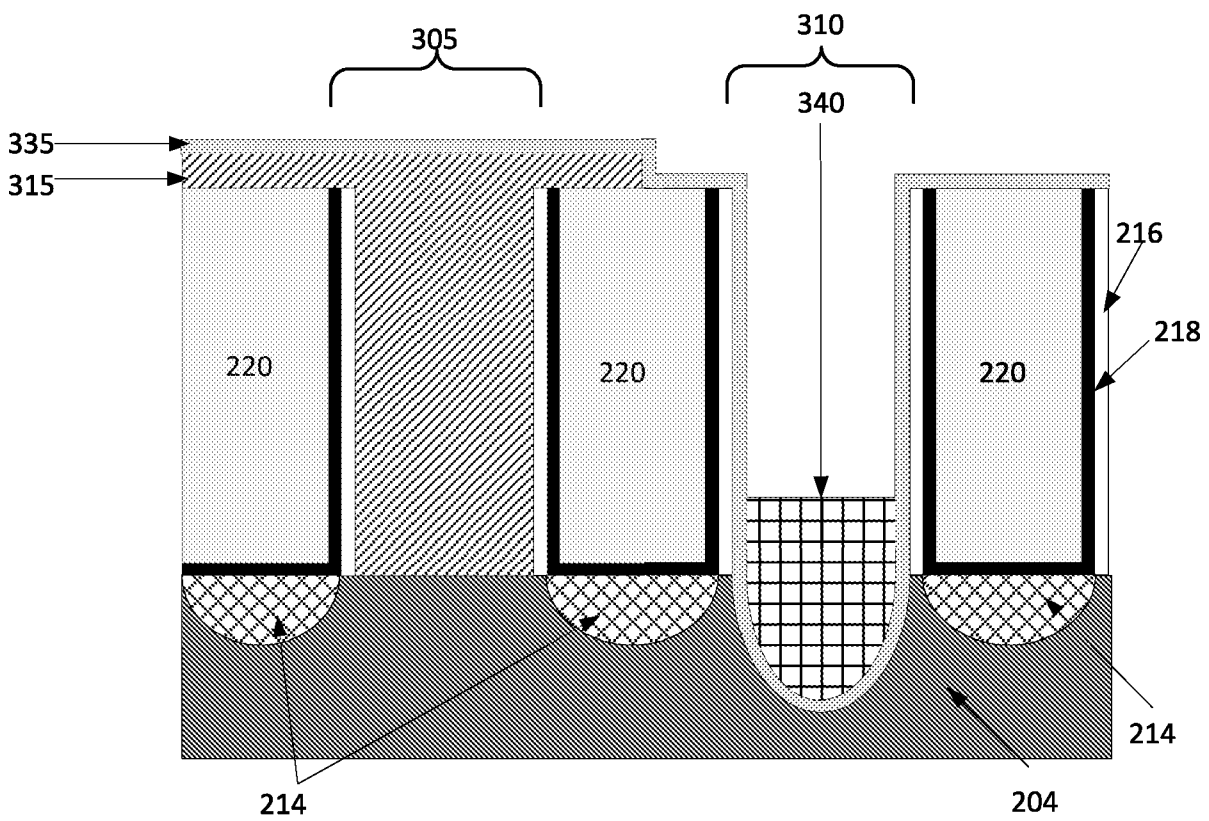


FIG. 3I

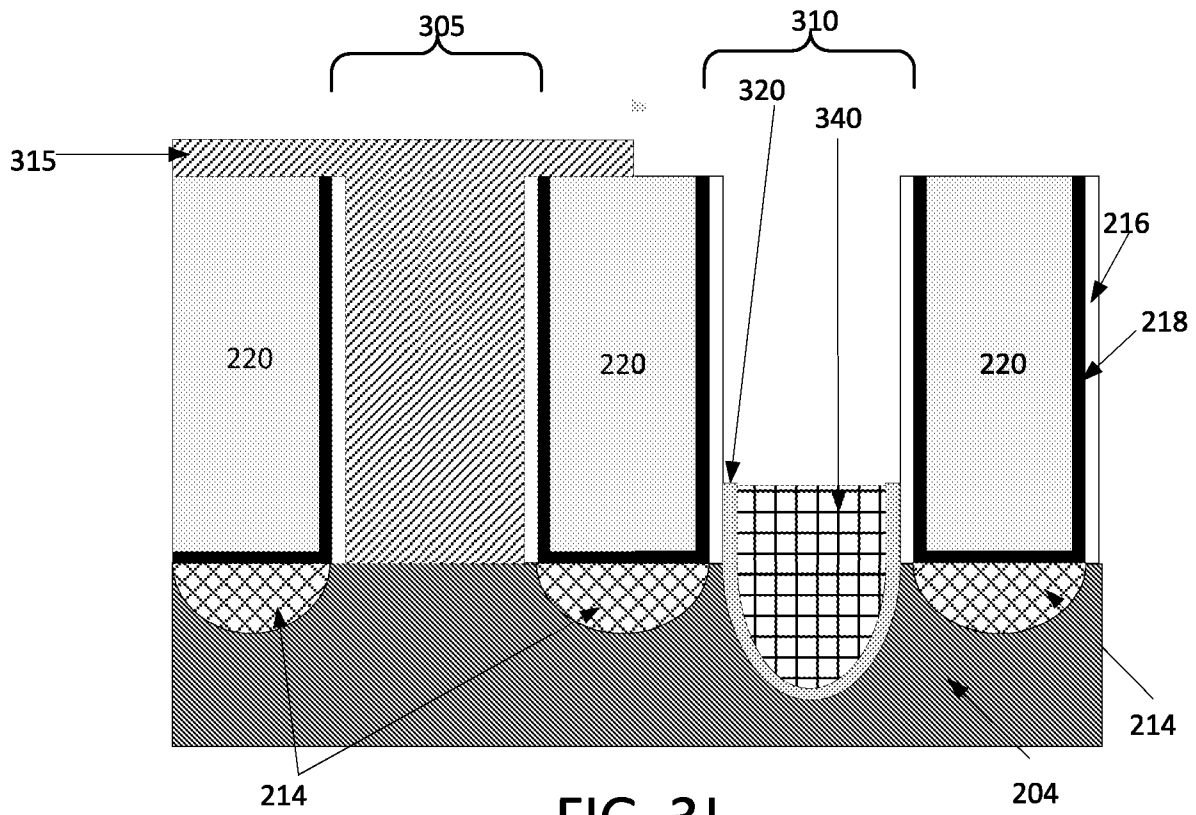


FIG. 3J

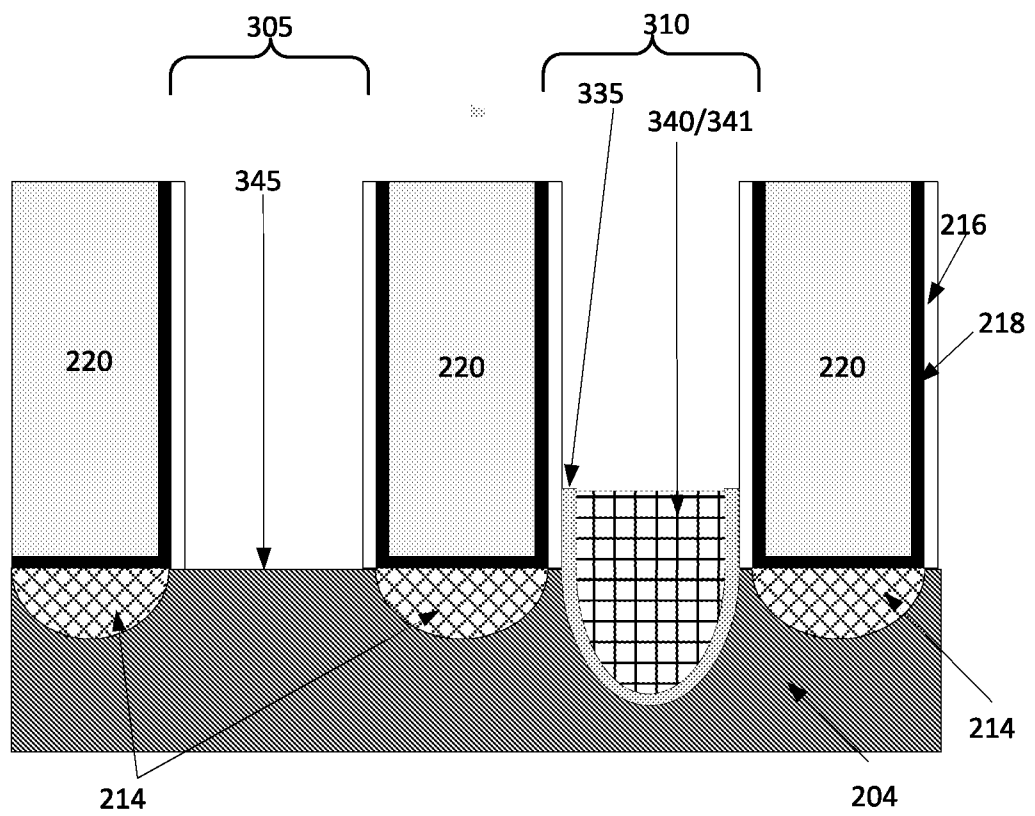


FIG. 3K

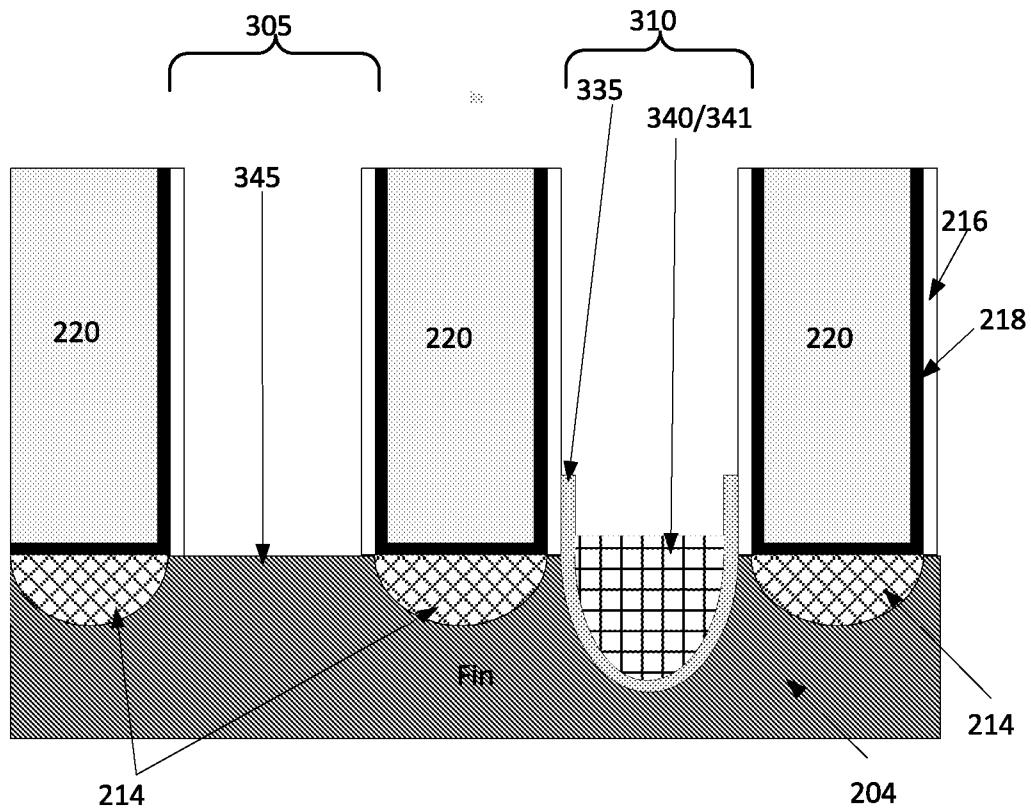


FIG. 3L

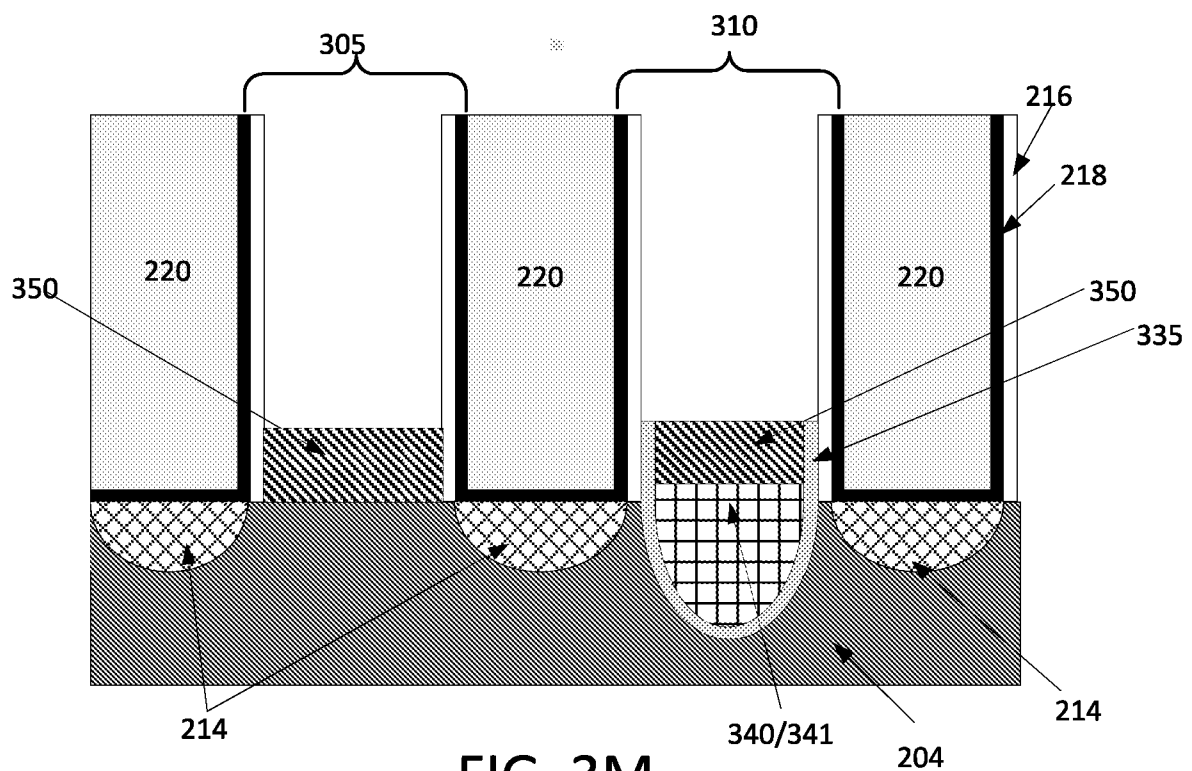


FIG. 3M

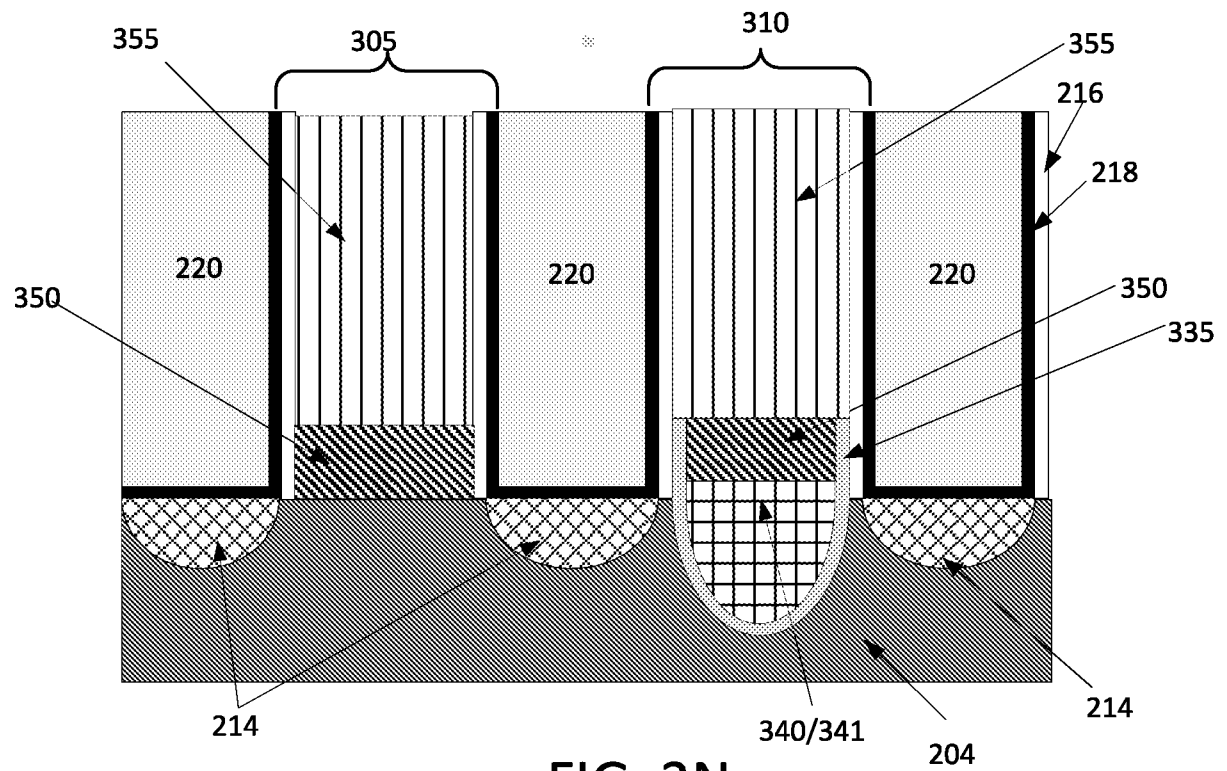


FIG. 3N

400

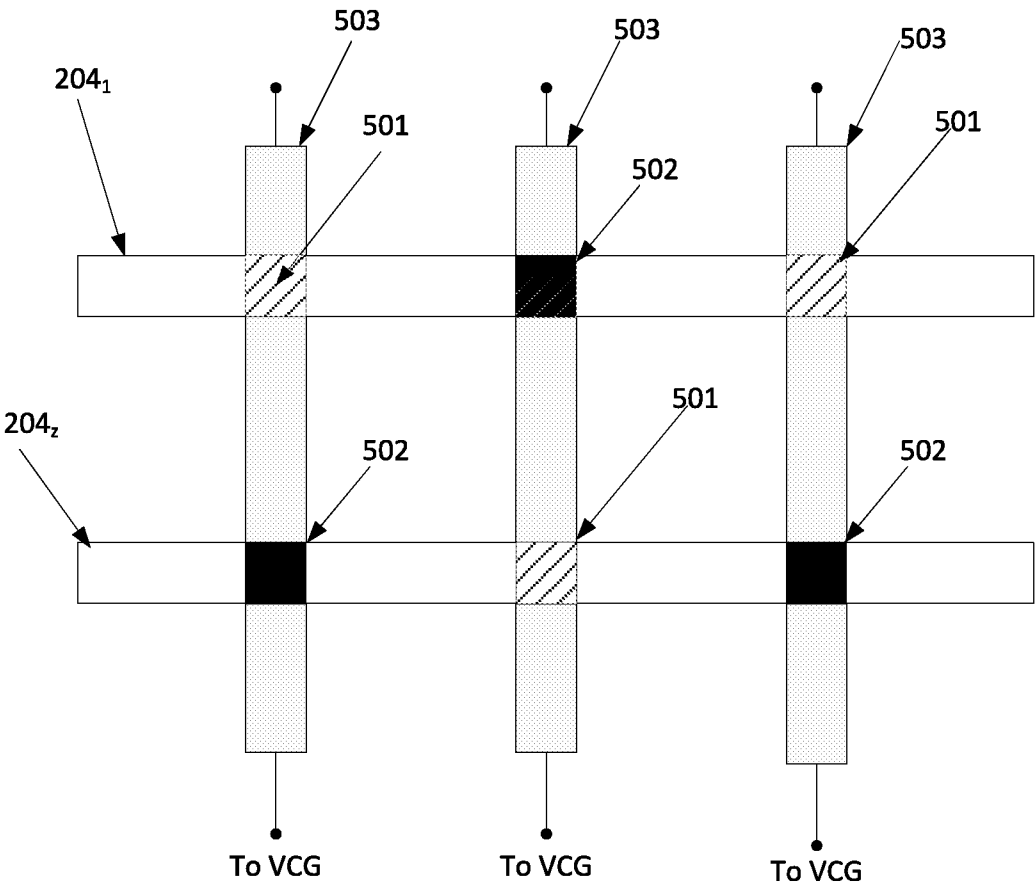


FIG. 4

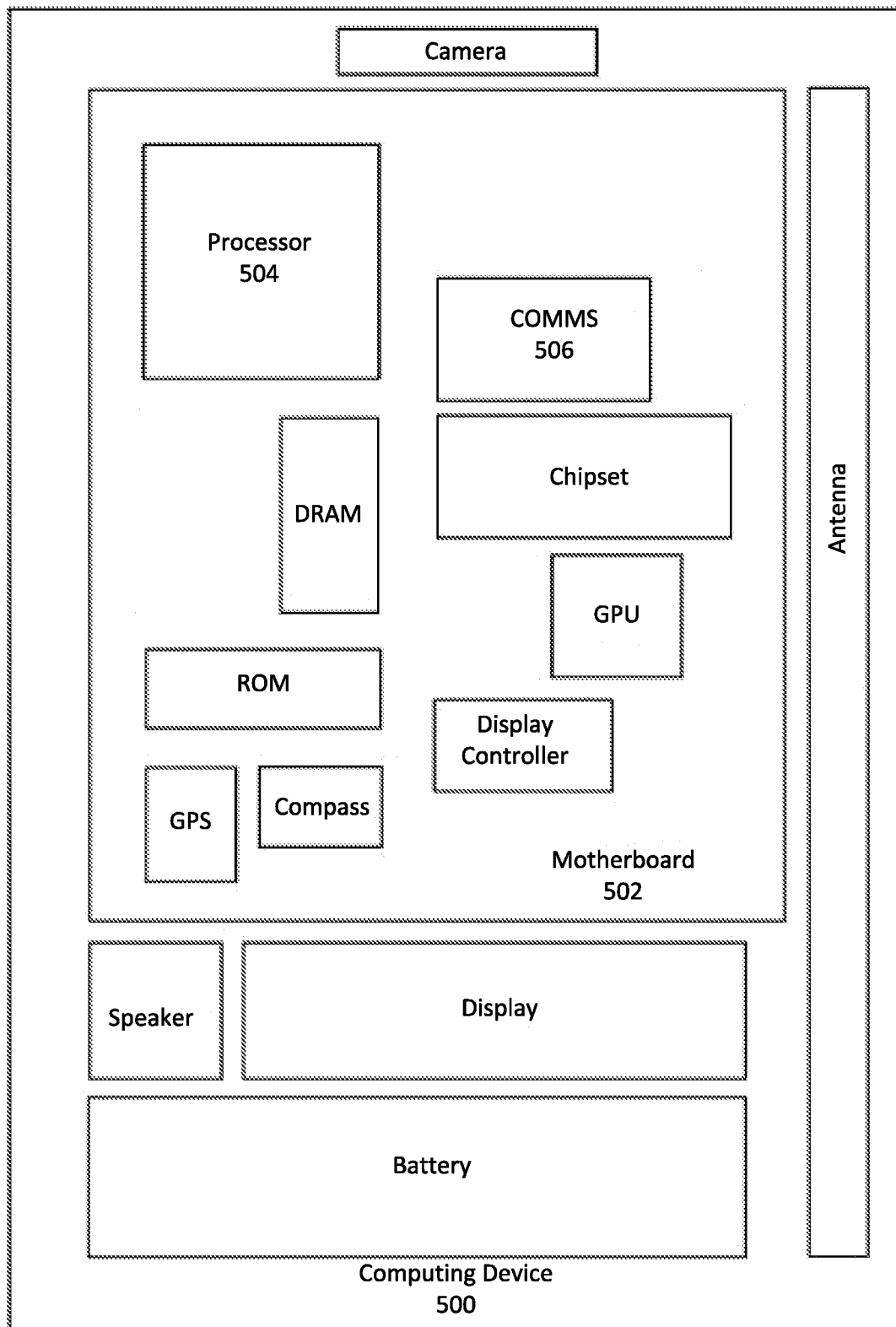


FIG. 5

**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/336(2006.01)i, H01L 29/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/336; H01L 27/088; H01L 29/41; H01L 29/78; H01L 21/762; H01L 21/8238; H01L 27/092; H01L 21/76

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: transistor, fin, dummy, gate, isolation trench, dielectric, gate

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                       | Relevant to claim No. |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| A         | US 2015-0060959 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.)<br>05 March 2015<br>See paragraphs [0033]-[0037], claims 1-11 and figures 19, 20.  | 1-25                  |
| A         | KR 10-2013-0137508 A (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.)<br>17 December 2013<br>See paragraphs [0005]-[0014], claims 1, 6 and figures 1-3. | 1-25                  |
| A         | US 2015-0035069 A1 (UNITED MICROELECTRONICS CORP.) 05 February 2015<br>See paragraphs [0012]-[0016], claims 1-11 and figure 1.                           | 1-25                  |
| A         | US 2014-0103450 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION)<br>17 April 2014<br>See paragraphs [0091], [0092], claims 19-25 and figures 18A, 18B.   | 1-25                  |
| A         | JP 2008-060219 A (ELPIDA MEMORY INC.) 13 March 2008<br>See paragraphs [0031]-[0035], claim 8 and figures 6-8.                                            | 1-25                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

31 May 2016 (31.05.2016)

Date of mailing of the international search report

**31 May 2016 (31.05.2016)**

Name and mailing address of the ISA/KR

International Application Division

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Telephone No. +82-42-481-8291



**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2015/052162**

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                            | Publication<br>date                                  |
|-------------------------------------------|---------------------|-----------------------------------------------------------------------|------------------------------------------------------|
| US 2015-0060959 A1                        | 05/03/2015          | None                                                                  |                                                      |
| KR 10-2013-0137508 A                      | 17/12/2013          | TW 201351505 A<br>TW I493628 B<br>US 2013-0330906 A1<br>US 8735252 B2 | 16/12/2013<br>21/07/2015<br>12/12/2013<br>27/05/2014 |
| US 2015-0035069 A1                        | 05/02/2015          | US 8981487 B2                                                         | 17/03/2015                                           |
| US 2014-0103450 A1                        | 17/04/2014          | WO 2014-058552 A1                                                     | 17/04/2014                                           |
| JP 2008-060219 A                          | 13/03/2008          | JP 4487266 B2<br>US 2008-0054374 A1<br>US 7683437 B2                  | 23/06/2010<br>06/03/2008<br>23/03/2010               |