The present invention reduces bounce in the power (VCC) or ground (VSS) supply voltages of an integrated circuit chip by gradually turning output drivers (407b) both on and off, so there is not a sharp discontinuity in current flow to an external device (PAD). Greatest current flow occurs at the middle of a transition period. The gradual turn-off at the end of a transition is achieved by feeding back voltage of the output signal (408) to a device (501) which controls the output driver (407b). As output voltage approaches its final value, the output driver (407b) gradually turns off, preventing a sharp transient in the power (VCC) or ground (VSS) voltage of the integrated circuit chip.
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6 FIELD OF THE INVENTION
7 The invention relates to output buffers for integrated
8 circuit devices, more particularly to an output buffer which
9 can be programmed differently to drive different types of
10 load devices.
11
12 BACKGROUND OF THE INVENTION
13 Current process technology allows an output driver to
14 generate rapid changes in output voltage. Fast transitions
15 are desirable, but can lead to unwanted noise on internal
16 power and ground busses. Since power and ground busses are
17 coupled to internal logic signals, noise on the power and
18 ground busses may cause erroneous states to be generated in
19 the internal logic signals. Fast transitions can also cause
20 ringing on the output pin signal, which may cause erroneous
21 data to appear in a receiving device being driven by the
22 output pin signal.
23 The fundamental cause of noise on the power and ground
24 busses is due to the transition of the voltage level driving
25 the load. Fig. 1 shows an output driver circuit 101 in
26 combination with an output load device 106 driven through pad
27 105 and inductive elements 102 and 107 internal to the
28 integrated circuit and additional inductive elements 103 and
29 108 comprising bond pads and wires connected to positive and
30 negative power supplies, and printed circuit traces 104 and
31 109 external to the integrated circuit device. When the pad
32 signal is a logical 1, transistor 101a is on, and a current
33 $i_{TR}$ flows from the positive power supply through trace 104,
34 bond wire 103, integrated circuit power line 102, transistor
35 101a, pad 105, to load 106. When transistor 101a suddenly
36 shuts off, the induction of elements 104, 103, and 102 causes
37 a voltage buildup, allowing $VCC_{INT}$, the internal power supply
38 voltage, to be greater than $VCC_{EXT}$, the external power supply
39 voltage. At this point, load 106 is at a positive voltage
level, for example 5 volts. When transistor 101b suddenly
turns on and current \( i_{TF} \) begins to flow, the inductance of
elements 107, 108, and 109 limits current flow and causes a
voltage buildup across elements 107, 108, and 109, allowing
\( VSS_{INT} \) to be greater than \( VSS_{EXT} \). Opposite variations in VCC
and VSS occur due to opposite transitions of transistors 101a
and 101b. When multiple transistors equivalent to
transistors 101a and 101b switch simultaneously, the voltage
variations on the power and ground busses can be unacceptably
large, causing erroneous data to be generated internally.
Erroneous data can also be generated at the load device in
response to a fast transition.

Prior efforts to control power and ground bounce
(variation in VCC and VSS voltages) have included a staged
turn-on technique, a ramped pre-drive technique and a
feedback circuit. These are now discussed.

Fig. 2A shows a prior art circuit for reducing variation
in VCC and VSS levels by generating parallel drive signals
with different delays in response to an unbuffered output
signal. As shown in Fig. 2A, in the staged turn-on
technique, the output driver is formed as a number of smaller
drivers 203, 205, and 207 placed in parallel between VCC and
VSS. Delay devices 204 and 206 cause delays to the driving
signal on line 202 so that drivers 203, 205, and 207 switch
at slightly different times, causing a more gradual voltage
change at pad 208.

Fig. 2B shows a circuit which provides a ramped pre-
drive. Weak pre-driver inverter 212 has a relatively small
channel width and responds relatively slowly to a switching
input signal. Thus driver 214 switches more slowly and
therefore causes less bounce in VCC and VSS.

Fig. 2C shows an output driver with feedback to VCC and
VSS. Resistors 223 and 225 limit current flow to and from
pad 226. The feedback occurs because, for example, when the
gate-to-source voltage difference at transistor 224b is high,
transistor 224b is hard on. But a high current \( i \) from pad
226 through resistor 225 to VSS raises the voltage at the
source of transistor 224b, turning transistor 224b partly off. As the voltage on pad 226 approaches the VSS voltage, current through resistor 225 decreases, so the source voltage of transistor 224b decreases, transistor 224b turns more on, and current continues to flow. A similar effect happens with resistor 223 and transistor 224a.

None of these prior art devices eliminates the ground bounce which occurs at the end of a switching transition.

SUMMARY OF THE INVENTION

The present invention takes into account the type of load being driven by the output driver in determining the drive characteristics. Some output loads are predominately capacitive, that is the load device behaves like a capacitor plate attached to the output terminal so there is no DC component (except for a transient just after switching occurs). Other output loads are predominantly resistive-capacitive, acting like a resistor and capacitor attached to the output terminal. These devices have a steady state DC component in addition to the transient just after switching occurs.

In the case of a resistive-capacitive load, the output is typically terminated by a resistor divider network. The resistor divider network reduces variation in the VCC and VSS voltages by initially limiting the amount of current, and at the end of the transition by maintaining the current. For this type of load, the output driver must be strong enough to switch the load quickly and to sink enough current to pull the resistor network voltage down to an acceptable level. Any of the prior art circuits work satisfactorily for resistive-capacitive loads.

In the case of a capacitive load, the current is supplied only from stored charge. At the end of a switching transition, with any of the prior art circuits discussed above, the inductors tend to maintain the current flowing, and the capacitor allows voltage to overshoot past the nominal power or ground voltage. None of the prior art
circuits protect adequately against voltage variation from such a load.

According to the present invention, the drive capability of the output device is reduced as voltage approaches its intended level, thus gradually reducing current flow through the inductive elements. In one embodiment the output device is a P-channel transistor connected in series with an N-channel transistor where control of at least one transistor is by means of a two-input logic gate (such as an AND gate for an N-channel transistor or an OR gate for a P-channel transistor). The gate receives as one of its inputs the unbuffered output signal and as the other of its inputs the buffered and inverted output signal. In the case where the N-channel transistor is controlled by output of an AND gate, feeding back the buffered output to the AND gate causes the AND gate output to go low as the output device approaches its low level. This turns off the N-channel transistor gradually, so that current between the load and the VSS line changes gradually, and the inductive effect has much less influence on the VSS level.

In another embodiment, a multiplexer selects between turning off the transistor gradually and turning off in response to the unbuffered output signal directly. This embodiment uses a conventional circuit to operate with a resistive-capacitive load with resulting fast switching, and uses the gradual turn-off to operate with a capacitive load, with resulting reduced ground (or power) variation.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows an output driver circuit and load, with inherent inductive elements included.

Figs. 2A-2C show prior art circuits for controlling slew rate.

Fig. 3A shows a circuit representing a resistive-capacitive load.

Fig. 3B shows a circuit representing a capacitive load.

Figs. 4A-4G show circuits according to the present
invention for reducing variation in ground voltage when switching.

Fig. 4H shows a circuit according to the present invention for reducing variations in both power and ground voltage when switching.

Fig. 4I shows another circuit for reducing bounce in both the internal VCC and VSS supplies.

Figs. 5A shows a prior art circuit for reducing bounce when a circuit begins switching which is preferably used in combination with one of the circuits of Fig. 4A to 4I.

Fig. 5B shows the preferred layout of the circuit of Fig. 5A.

Figs. 6A, 6B, and 6C shows curves for, respectively, output (pad) voltage, pad current, and internal ground voltage VSSINT as functions of time.

DETAILED DESCRIPTION OF SOME EMBODIMENTS OF THE INVENTION

Figs. 3A and 3B show two types of loads typically driven by an output circuit of an integrated circuit device. As shown in Fig. 3A an output signal is buffered through a CMOS inverter 214, through a pad 215, and to a load which comprises capacitor C301 and a resistor divider network comprising resistors R301 and R302. Fig. 3B, on the other hand, uses a load which primarily comprises capacitor C302. These two types of loads have different effects on the voltage levels in the integrated circuit driving the loads and require very different output buffers to drive these two types of loads in order to minimize the variation in power and ground voltages of the integrated circuit. In the case of Fig. 3A, the resistor divider network formed from resistors R301 and R302 reduces variation in power and ground voltage by limiting the initial current and by maintaining current at the end of the transition, the current path being through one of resistors R301 and R302. Initial current is limited by the series resistor according to the well-known formula I = V/R. At the end of a transition, the DC current through one of the resistors R301 or R302 prevents any sharp
discontinuity of current with resulting ground bounce. For
the type of load shown in Fig. 3A, output driver circuit 214
must be strong enough to switch the voltage at the load
quickly and to sink enough current to pull the resistor
network voltage down to an acceptable level. Any of the
prior art techniques will work for resistive-capacitive loads
such as shown in Fig. 3A.

In the case of a capacitive load, such as capacitor C302
shown in Fig. 3B, the load supplies current from stored
charge. At the end of a switching transition, inductors such
as shown in Fig. 1 tend to maintain current flow, and since
there is no current path through the load, voltage at
capacitor C302 swings past an equilibrium voltage, producing
the condition commonly described as "ground bounce." The
present invention applies particularly to loads such as shown
in Fig. 3B. To minimize ground bounce, the drive capability
of the output devices begins to be reduced as the switching
event completes.

Figs. 4A through 4H show several embodiments of the
present invention which can handle pure capacitive loads.
The simplest case is shown in Fig. 4A. As shown in Fig. 4A,
an unbuffered output signal on line 401 is applied to a
gating device 501. Gating device 501 also receives feedback
on line 408 from the buffered output signal applied to the
pad. Gating device 501 is of a type which gradually reduces
the voltage on the gate of transistor 407b in response to a
decreasing output voltage on line 408 which results when the
signal OUT goes high on line 401. This causes transistor
407b to turn off gradually as the pad voltage decreases.
This in turn prevents the load capacitance associated with
the pad in combination with inductances associated with the
ground line from producing a disturbance in the ground
voltage at VSS.

Fig. 4B shows another embodiment of the invention in
which resistor R1 is replaced with P-channel transistor 407A
in a conventional CMOS output driver. In another embodiment
(not shown), resistor R1 can be replaced with an N-channel
pull-up transistor controlled through an inverter. The
function of device 501 and transistor 407b is the same as
described in connection with Fig. 4A.
In Fig. 4C device 501 is controlled by memory cell M
such that in one state transistor 407b is turned off
gradually in response to a signal on line 408 and in another
state, transistor 407b is controlled only in response to a
signal on line 401. This memory cell may be an SRAM cell,
that is, a volatile cell which is typically loaded when the
chip is powered up. Alternatively, memory cell M may be one
or two antifuses which programmably connect the multiplexer
control line to either power or ground. Likewise, memory
cell M could be an EPROM cell (a nonvolatile cell) or it
could be two selectable vias, one of which is formed during
manufacture of the device to connect the multiplexer to the
appropriate voltage source.

Fig. 4D shows a further implementation in which a second
output driver 417 is controlled in a conventional manner by
an output signal on line 401. In this embodiment transistor
407b is a relatively large transistor which pulls down the
pad quickly in response to an increasing voltage on line 401.
Output driver 417 includes small transistors 417a and 417b.
When transistor 407b turns off due to the feedback through
control device 501, the voltage on line 408 is held low by
transistor 417b, which remains on in response to the high
voltage on line 401.

Fig. 4E shows an embodiment of the control device 501
which comprises multiplexer 503 in combination with AND gate
502. AND gate 502 receives input signals from line 408 and
line 401. If either of these signals is low, the output of
AND gate 502 is low. A logical one in memory cell M causes
multiplexer 503 to pass the input signal from AND gate 502 to
the gate of transistor 407b. In response to a falling signal
on line 408, a falling signal out of multiplexer 503 causes
transistor 407b to turn off gradually, preventing ground
bounce.

If memory cell M carries a logic 0, the signal on line
401 is passed directly to the gate of transistor 407b, and therefore controls transistor 407b without regard to the voltage on line 408. The embodiment of Fig. 4E is useful when the circuit will be driving either of the load devices shown in Figs. 3A and 3B. For driving the load device in Fig. 3A, memory cell M is loaded with a logical 0 such that transistor 407b is controlled directly by a signal on line 401. When the load device is a capacitive load such as shown in Fig. 3B, memory cell M is loaded with a logical one and causes multiplexer 503 to produce the gradually decreasing voltage on the gate of transistor 407b in response to the decreasing voltage on line 408.

Fig. 4F shows a particular implementation of AND gate 502, comprising transmission gate 504 and pull down transistor 506. Pull down transistor 506 turns on when transmission gate 504 is off; preventing a floating input on line 507 in the case where line 401 is a logical 0. As the signal on line 401 moves to logical 1, and as line 408 moves toward the voltage VSS, the lowering voltage on line 507 is passed by multiplexer 503 to the gate of transistor 407b, turning this transistor gradually off such that the variation in voltage level VSS is minimized. Note that if transistor 407b is fully off, and transistor 506 is off, that line 507 which controls multiplexer 503 and the gate to transistor 407b can be left floating. But if the gate to transistor 407b floats to a high enough voltage to turn transistor 407b partly on, the corresponding decrease in voltage on line 408 again lowers the voltage on line 507. Thus no intermediate voltages persist.

Fig. 4G shows an embodiment in which the implementation of Fig. 4F is combined with a second output driving device such as shown in Fig. 4D. Small transistors 417a and 417b pull the output voltage to the rails and prevents the drifting of output voltage which occurs with the single stage of Fig. 4F.

Fig. 4H shows yet another embodiment in which both ground voltage and power voltage are controlled by a gradual
turn off device such as discussed earlier in connection with
the ground voltage only. Elements 511-516 correspond to
elements 501-506 respectively.

Fig. 4I shows another circuit for reducing bounce in
both the internal VCC and VSS supplies. The primary output
driver 447 differs from a standard CMOS inverter by having
the P-channel transistor 447b connected to ground and the N-
channel transistor 447a connected to the positive voltage
supply. The circuit is a non-inverting buffer and does not
pull the output voltage to the rails. To pull the output to
the rails, a smaller secondary driver 427 comprising two
standard CMOS inverters is provided. Circuit 427 pulls the
pad voltage to one of VCC or VSS, but because transistors in
circuit 427 are smaller than in circuit 447, the current
through circuit 427 is low and the ground bounce of this
circuit is small. Since drive current through circuit 447 is
reduced before output voltage reaches its final value, the
ground bounce of the circuit of Fig. 4I is reduced.

Actually, to minimize ground (and power) bounce, it is
necessary that the current flow both begin slowly and end
slowly. The present invention relates to assuring that the
current flow ends slowly. Prior art circuits such as shown
in Fig. 5A cause the current to begin slowly so that no
appreciable ground bounce occurs on either the beginning or
the end of a transition. Such a circuit is preferably used in
combination with one of the circuits of Fig. 4A to 4I.

Fig. 5B shows the preferred layout of the circuit of
Fig. 5A. The output transistor such as 407b is implemented
as a set of parallel transistors 407b1 through 407b5, and the
gates of these transistors are formed as a single
polycrystalline silicon line 551, which is resistive, as
represented by resistors R61 through R65. There is
capacitance between the gate 551 and the N-diffusion in which
the transistor sources and drains are formed. This
capacitance is represented by capacitors C61 through C65.
This combination of resistance and capacitance produces a
delay between the turn-on of transistor 407b1 and the turn-on
of transistor 407b5. Thus ground bounce at the turn-on of
transistor 407b is minimized by laying out transistor 407b as
shown in Fig. 5B.

The combination of the present invention with the prior
art implementation of Fig. 5B is illustrated in Figs. 6A, 6B,
and 6C. These curves show, respectively, output (pad)
voltage, pad current, and internal ground voltage VSS_{INT} as
functions of time. The dotted line in Fig. 6C is included to
illustrate the resulting bounce which would occur if the
present invention were not used.

In light of the several embodiments illustrated above,
other embodiments will become obvious to those skilled in the
art and are intended to be included in the scope of the
present invention.
1. A structure for reducing variation in power supply voltage in an integrated circuit device comprising:
   an output driver circuit comprising
   at least one output drive transistor (407b) having
   current carrying terminals connected between an
   output terminal (408) and a first power supply
   terminal (gnd) having a first power supply voltage;
   means (R1 or 407a) for supplying a second power
   supply voltage to said output terminal;
   means (501 or 502) for controlling said output drive
   transistor, said means for controlling being
   responsive to an unbuffered output signal (401) and
   to a voltage at said output terminal (408).

2. A structure for reducing variation in power supply voltage as in Claim 1 in which said means (R1 or 407a) for
   supplying a second power supply voltage to said output terminal comprises a second output drive transistor (407a).

3. A structure for reducing variation in power supply voltage as in Claim 2 further comprising means (see Fig. 4H)
   for controlling said second output drive transistor (407a).

4. A structure for reducing variation in power supply voltage as in Claim 1 further comprising means (503 and M)
   for causing said means for controlling said output drive transistor to respond only to said unbuffered output signal.

5. A structure for reducing variation in power supply voltage as in Claim 4 in which said means for causing said
   means for controlling said output drive transistor to respond
   only to said unbuffered output signal comprises:
   a multiplexer (503); and
   a logic gate (502) which receives at one terminal an
   output signal from said output terminal and at
   another terminal said unbuffered output signal, and
provides a signal to said multiplexer; wherein
said multiplexer in a first state passes said output
signal from said logic gate to a control terminal of
said output drive transistor and in a second state
passes said unbuffered output signal to said control
terminal of said output drive transistor.

6. A structure for reducing variation in power supply
voltage as in Claim 5 in which said multiplexer is controlled
by a memory cell.

7. A structure for reducing variation in power supply
voltage as in Claim 6 in which said memory cell is an SRAM
cell.

8. A structure for reducing variation in power supply
voltage as in Claim 6 in which said memory cell is at least
one antifuse connected to a voltage source.

9. A structure for reducing variation in power supply
voltage as in Claim 6 in which said memory cell is a
nonvolatile EPROM cell.

10. A structure for reducing variation in power supply
voltage as in Claim 6 is which said memory cell is at least
one optional via which connects to a voltage source.

11. A structure for reducing variation in power supply
voltage as in Claim 5 in which said logic gate comprises an
AND gate, said AND gate comprising:
a CMOS transmission gate having its control terminal
connected to said unbuffered output signal and its
input terminal connected to said output terminal of
said output driver circuit, and having an output
terminal;
a pull-down transistor having a current carrying
terminal connected to said output terminal of said
CMOS transmission gate and another current carrying
terminal connected to ground, and a control terminal
connected through an inverter to said unbuffered
output signal.

12. A structure for reducing variation in power supply
voltage as in Claim 1 further comprising:
a second output driver circuit comprising:
   at least one second output driver transistor (417b)
   having current carrying terminals connected between
   said output terminal (408) and said first power
   supply terminal and a control terminal controlled
   by said unbuffered output signal.
AMENDED CLAIMS
[received by the International Bureau on 4 February 1994 (04.02.94);
original claims 1-3 cancelled; original claims 4-12 amended;
(3 pages)]

4. A structure for reducing variation in power supply voltage in an integrated circuit device comprising:
   an output driver circuit comprising
   at least one output drive transistor (407b) having current carrying terminals connected between
   an output terminal (408) and a first power supply terminal (gnd) having a first power supply voltage;
   means (R1 or 407a) for supplying a second power supply voltage to said output terminal;
   means (501 or 502) for controlling said output drive transistor, said means for controlling being responsive to an unbuffered output signal (401) and to a voltage at said output terminal (408);
   and
   means (503 and M) for causing said means for controlling said output drive transistor to respond only to said unbuffered output signal.

5. A structure for reducing variation in power supply voltage as in Claim 4 in which said means for causing said means for controlling said output drive transistor to respond only to said unbuffered output signal comprises:
   a multiplexer (503); and
   a logic gate (502) which receives at one terminal an output signal from said output terminal and at another terminal said unbuffered output signal, and provides a signal to said multiplexer; wherein said multiplexer in a first state passes said output signal from said logic gate to a control terminal of said output drive transistor and in a second state passes said unbuffered output signal to said control terminal of said output drive transistor.
6. A structure for reducing variation in power supply voltage as in Claim 5 in which said multiplexer is controlled by a memory cell.

7. A structure for reducing variation in power supply voltage as in Claim 6 in which said memory cell is an SRAM cell.

8. A structure for reducing variation in power supply voltage as in Claim 6 in which said memory cell is at least one antifuse connected to a voltage source.

9. A structure for reducing variation in power supply voltage as in Claim 6 in which said memory cell is a nonvolatile EPROM cell.

10. A structure for reducing variation in power supply voltage as in Claim 6 is which said memory cell is at least one optional via which connects to a voltage source.

11. A structure for reducing variation in power supply voltage as in Claim 5 in which said logic gate comprises an AND gate, said AND gate comprising:

   a CMOS transmission gate having its control terminal connected to said unbuffered output signal and its input terminal connected to said output terminal of said output driver circuit, and having an output terminal;

   a pull-down transistor having a current carrying terminal connected to said output terminal of said CMOS transmission gate and another current carrying terminal connected to ground, and a control terminal connected through an inverter to said unbuffered output signal.

12. A structure for reducing variation in power supply voltage as in Claim 5.
voltage in an integrated circuit device comprising:
  a first output driver circuit comprising
    at least one output drive transistor (407b) having
    current carrying terminals connected between
    an output terminal (408) and a first power
    supply terminal (gnd) having a first power
    supply voltage;
    means (R1 or 407a) for supplying a second power
    supply voltage to said output terminal;
    means (501 or 502) for controlling said output drive
    transistor, said means for controlling being
    responsive to an unbuffered output signal (401)
    and to a voltage at said output terminal (408);
  a second output driver circuit comprising:
    at least one second output driver transistor
    (417b) having current carrying terminals
    connected between said output terminal (408)
    and said first power supply terminal and a
    control terminal controlled by said
    unbuffered output signal.
FIG. 5A PRIOR ART

FIG. 5B PRIOR ART
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
   IPC(5) : G05F 3/02, 3/16
   US CL. : 307/296.6; 323/265, 293
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
   Minimum documentation searched (classification system followed by classification symbols)
   U.S.: 307/296.6; 323/265, 293

   Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

   Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US, 4,701,635 (Kawazoe et al) 20 Oct. 1987, col. 2, lines 57 through col. 3 line 3.</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>US, 4,894,560 (Chung) 16 Jan. 1990, col. 1, lines 33-50.</td>
<td>2, 4</td>
</tr>
<tr>
<td>X</td>
<td>US, 4,906,871 (Iida) 06 Mar. 1990, col. 4, lines 37-44.</td>
<td>3</td>
</tr>
</tbody>
</table>

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search
29 November 1993

Date of mailing of the international search report
06 DEC 1993

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Commissioner of Patents and Trademarks
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Washington, D.C. 20231
Facsimile No. NOT APPLICABLE

Authorized officer
JOHN HEYMAN

Telephone No. (703) 305-3487

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