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(54) **PMOS PIXEL STRUCTURE WITH LOW CROSS TALK FOR ACTIVE PIXEL IMAGE SENSORS**

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(60) Provisional application No. 60/737,298, filed on Nov. 16, 2005.

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H01L 27/10	(2006.01)

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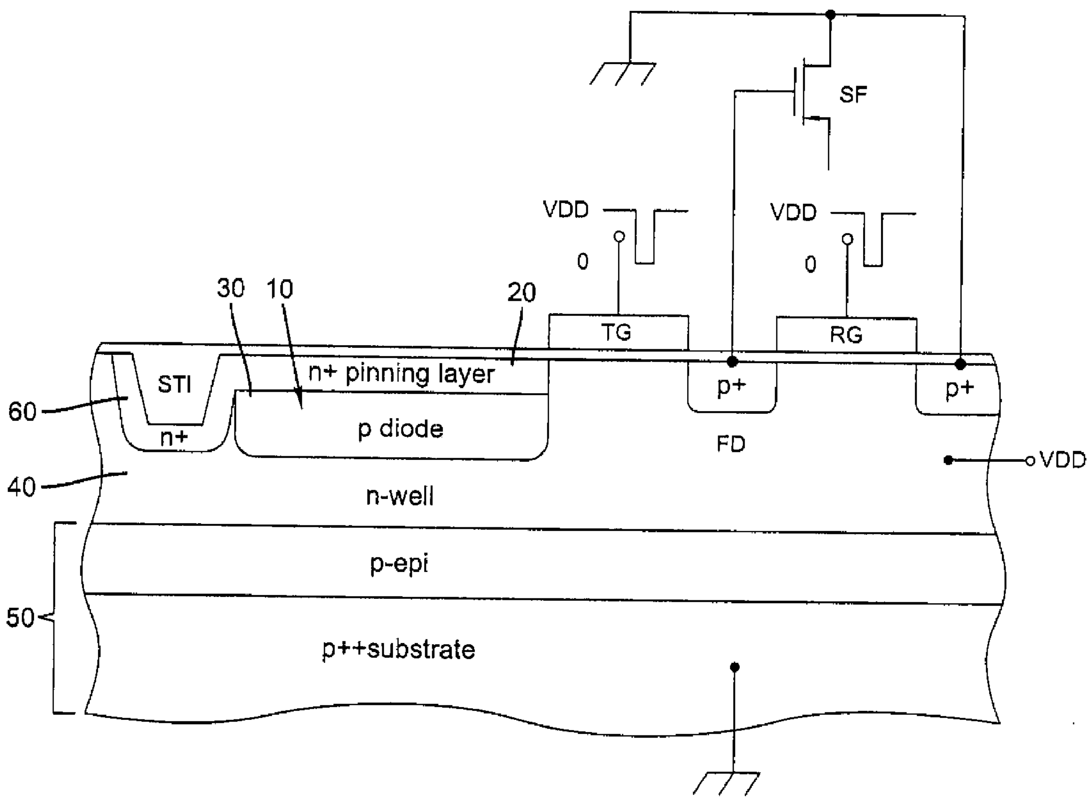
(57) **ABSTRACT**

An image sensor with an image area having a plurality of pixels each having a photodetector of a first conductivity type, the image sensor includes a substrate of the first conductivity type; a first layer of the second conductivity type between the substrate and the photodetectors, spanning the image area and biased at predetermined potential with respect to the substrate for driving excess carriers into the substrate to reduce cross talk; one or more adjacent active electronic components disposed in the first layer within each pixel; and electronic circuitry disposed in the substrate outside of the image area.



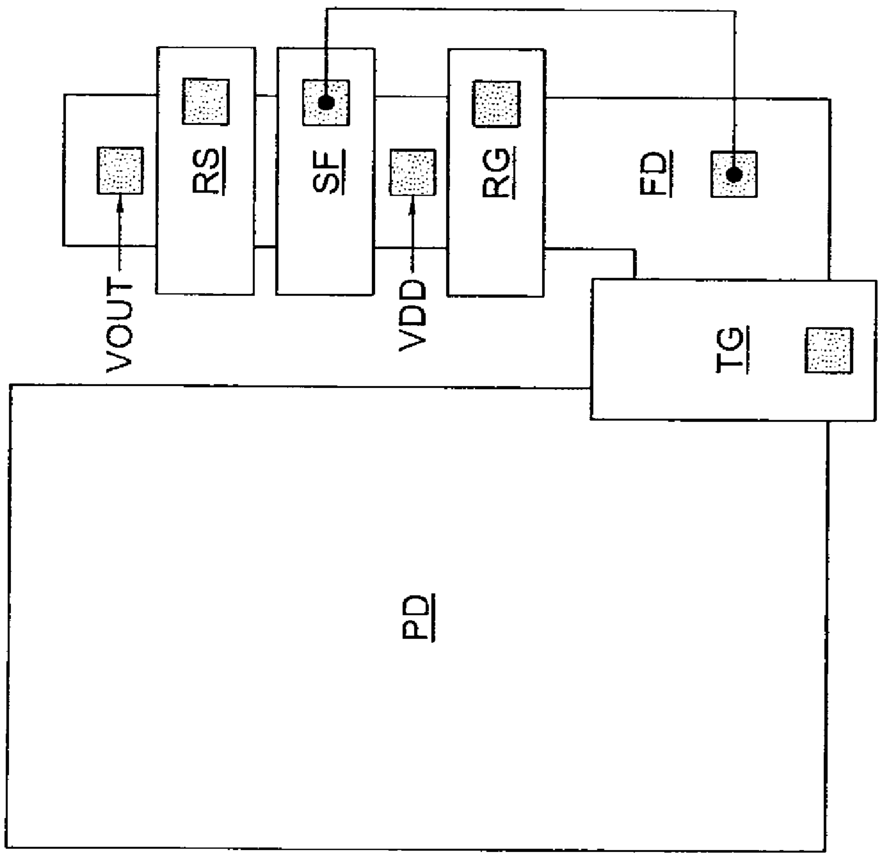


FIG. 1
PRIOR ART

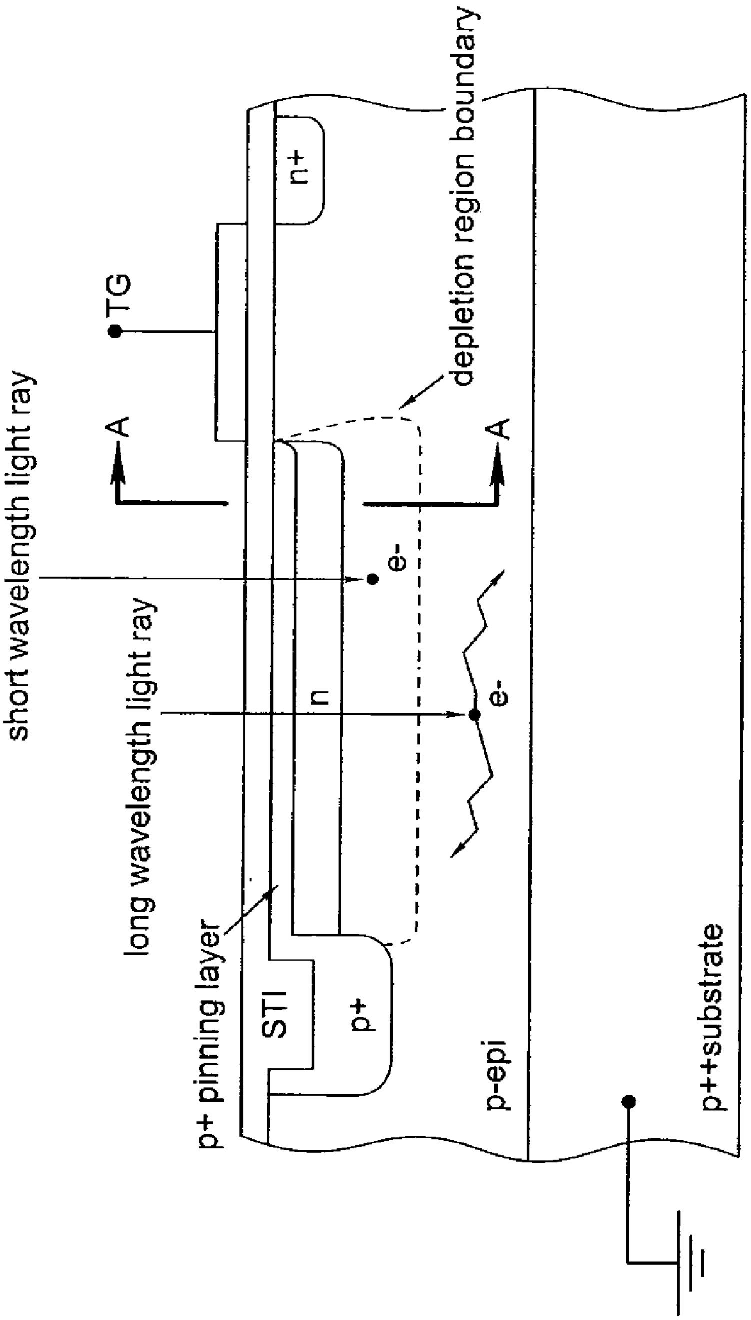


FIG. 2a
PRIOR ART

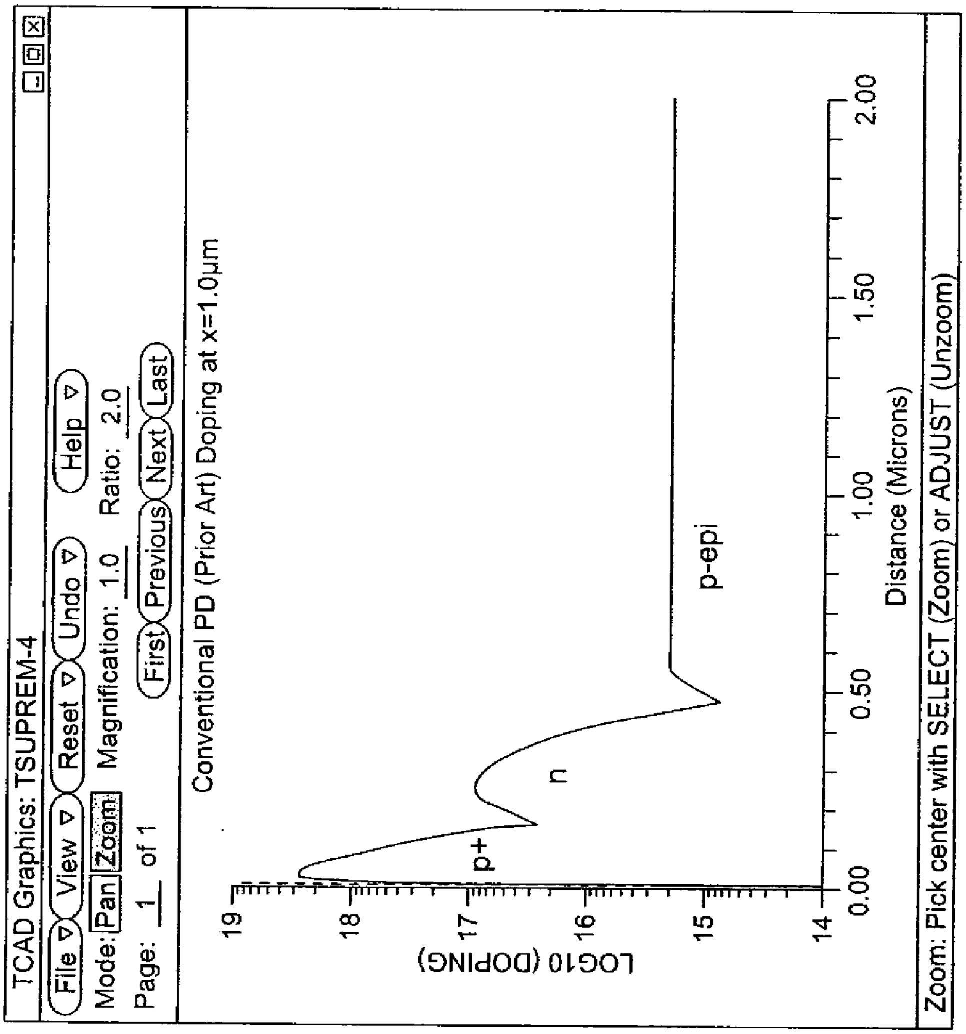


FIG. 2b
PRIOR ART

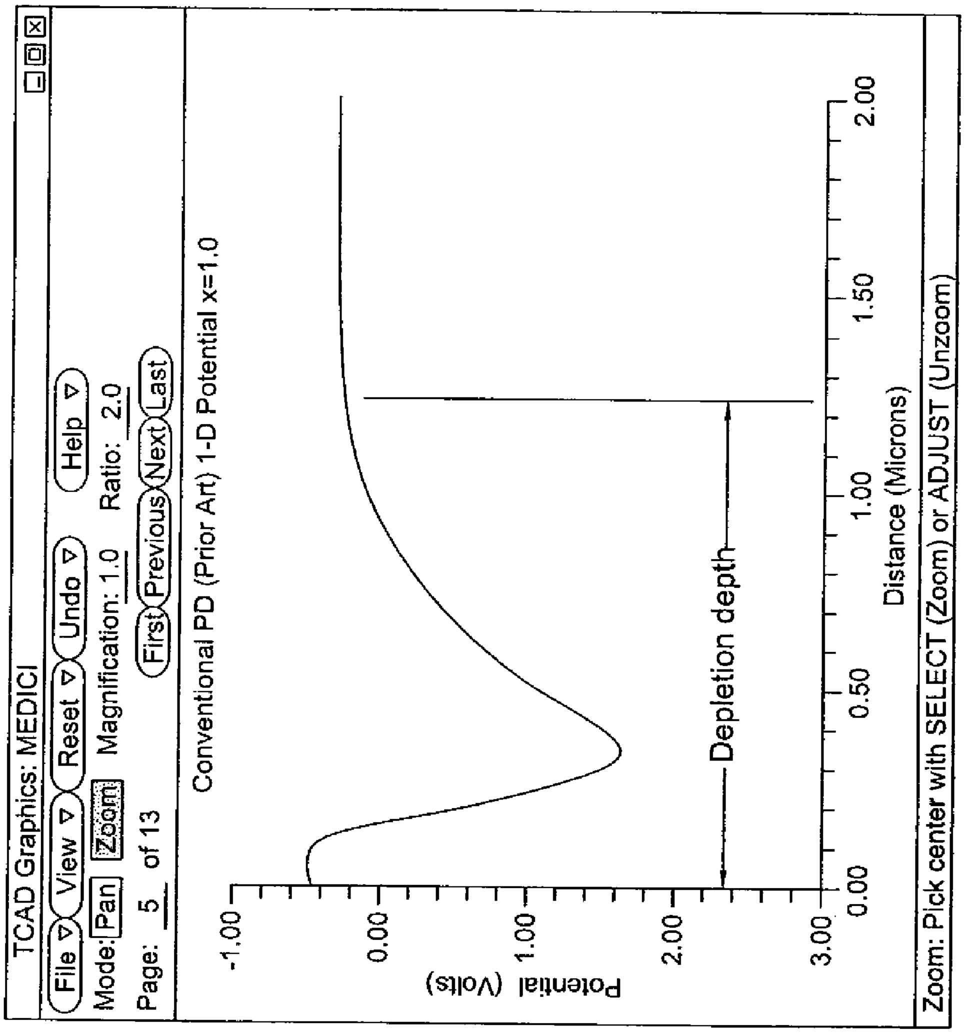


FIG. 2c
PRIOR ART

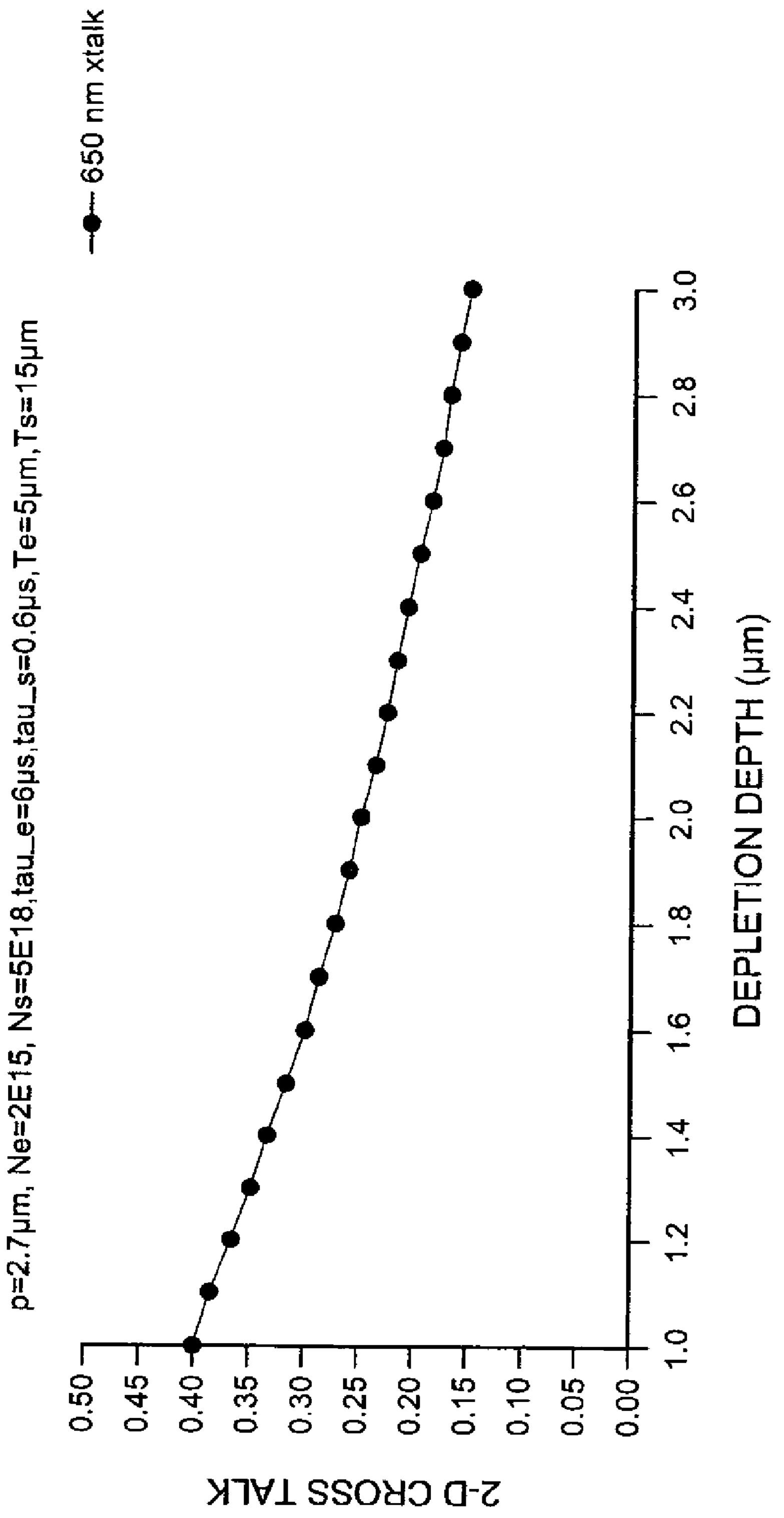


FIG. 3
PRIOR ART

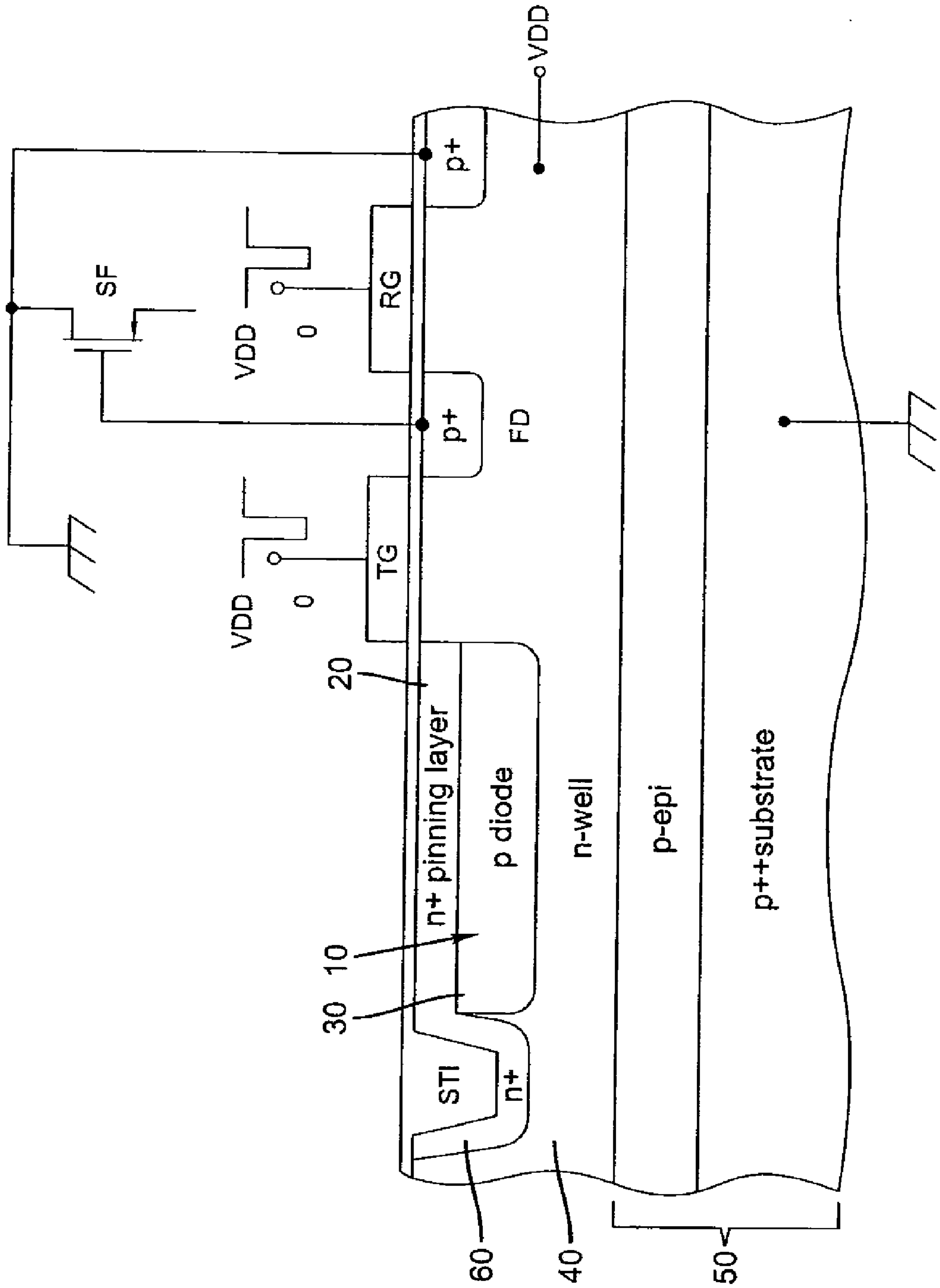

VDD
p+
SF
RG
VDD
0
p+
FD
TG
VDD
0
20
n+ pinning layer
p diode
n-well
p-epi
p++substrate
10
30
STI
n+
60
40
50

FIG. 4a

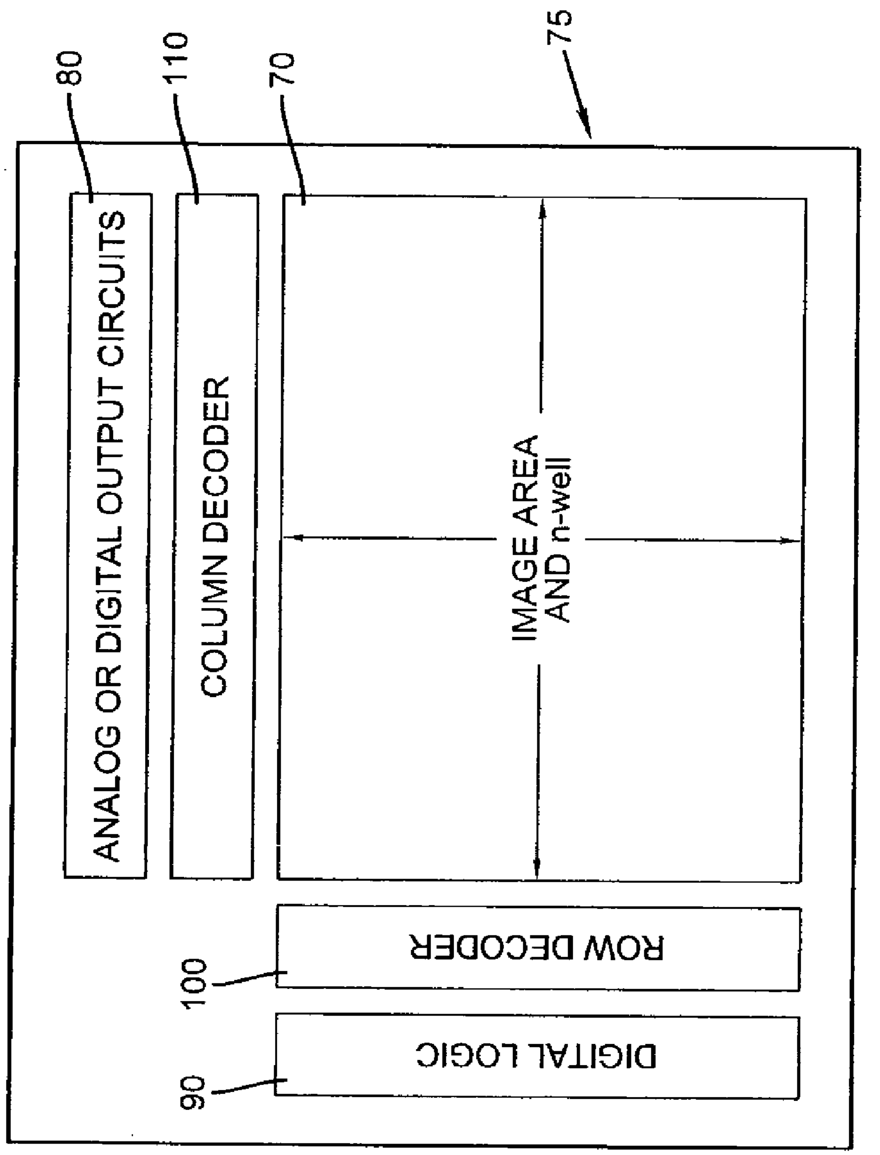

80
110
70
75
ANALOG OR DIGITAL OUTPUT CIRCUITS
COLUMN DECODER
IMAGE AREA
AND n-well
ROW DECODER
DIGITAL LOGIC
100
90

FIG. 4b

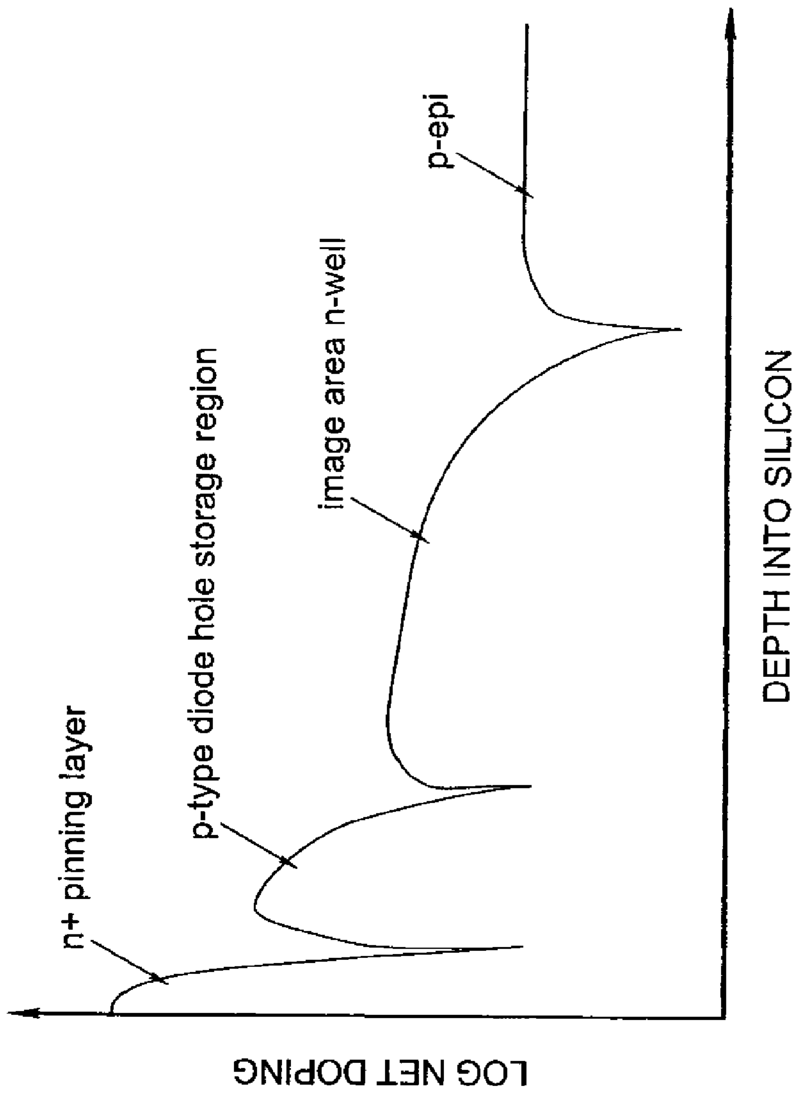

n+ pinning layer
p-type diode hole storage region
image area n-well
p-epi
LOG NET DOPING
DEPTH INTO SILICON

FIG. 4c

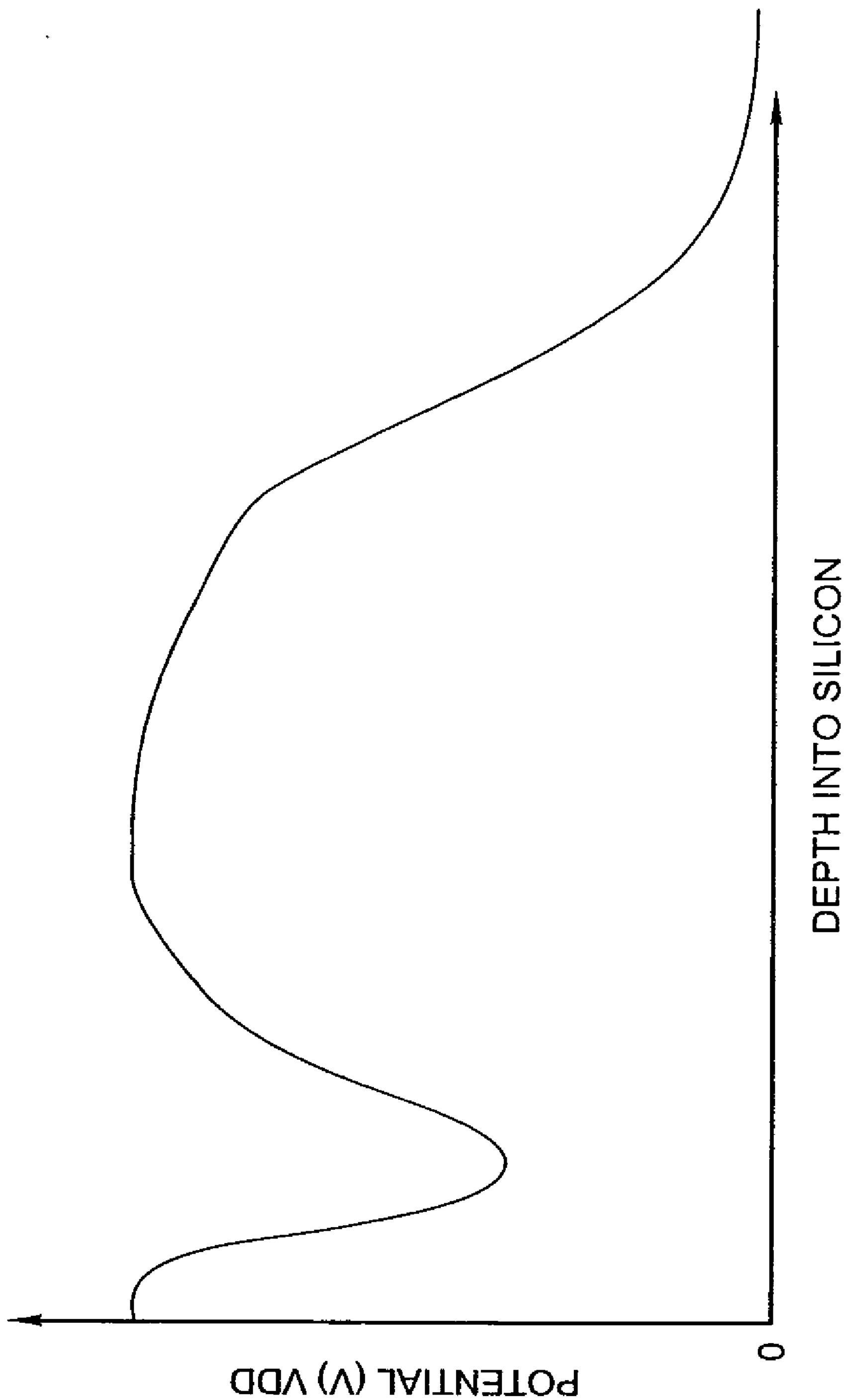


FIG. 4d

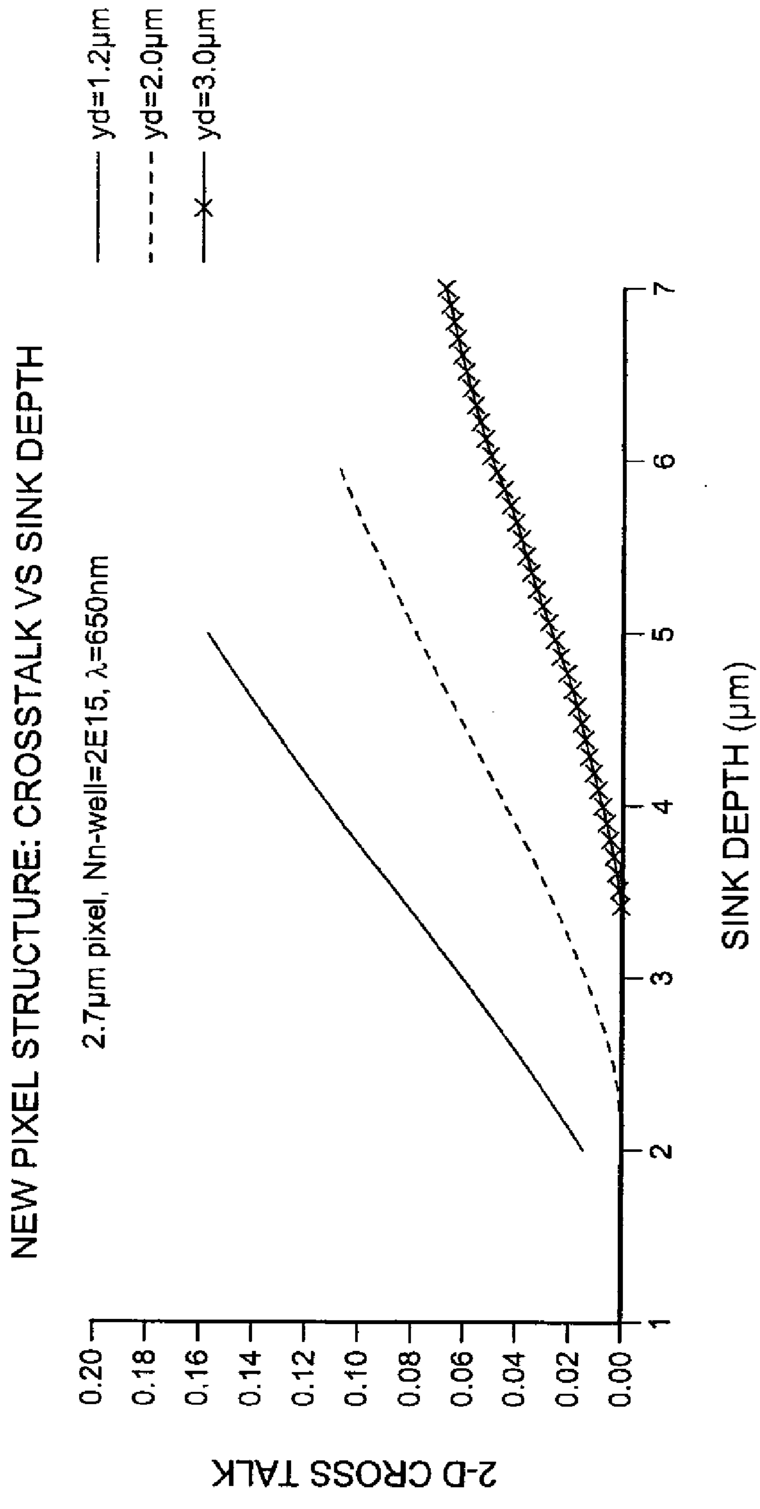

NEW PIXEL STRUCTURE: CROSSTALK VS SINK DEPTH
2.7µm pixel, Nn-well=2E15, λ=650nm
yd=1.2µm
yd=2.0µm
yd=3.0µm
2-D CROSS TALK
0.20
0.18
0.16
0.14
0.12
0.10
0.08
0.06
0.04
0.02
0.00
1
2
3
4
5
6
7
SINK DEPTH (µm)

FIG. 5

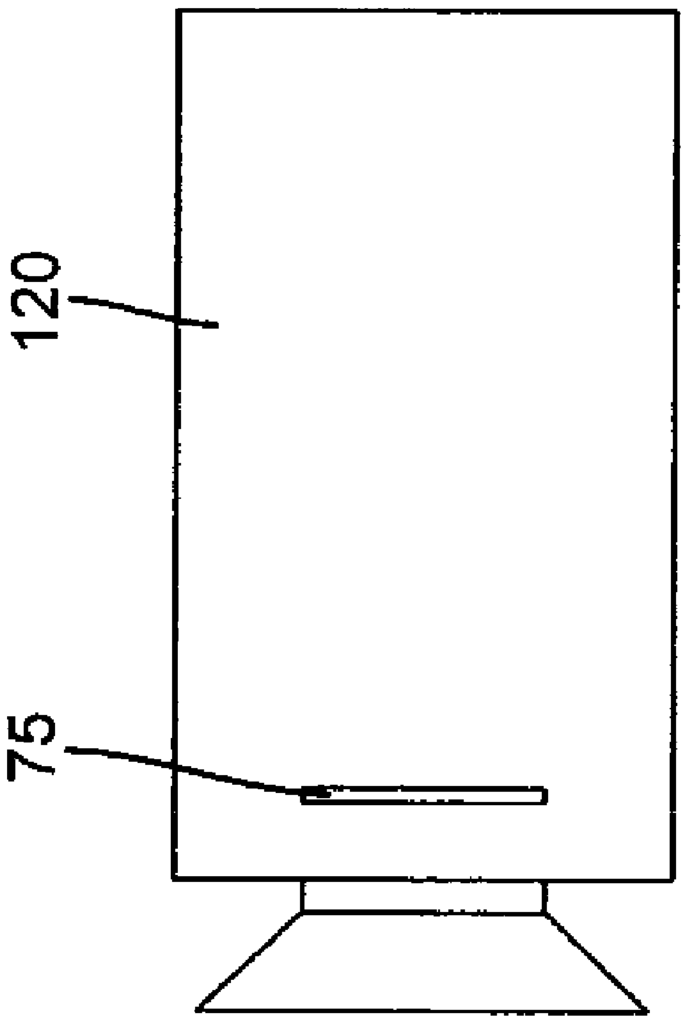


FIG. 6

PMOS PIXEL STRUCTURE WITH LOW CROSS TALK FOR ACTIVE PIXEL IMAGE SENSORS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This is a continuation application of U.S. application Ser. No. 11/455,985 filed Jun. 20, 2006. Reference is made to and priority claimed from U.S. Provisional Application Ser. No. 60/737,298, filed Nov. 16, 2005, entitled PMOS PIXEL STRUCTURE WITH LOW CROSS TALK FOR ACTIVE-PIXEL IMAGE SENSORS.

FIELD OF THE INVENTION

[0002] The invention relates generally to the field of image sensors, and in particular to active pixel image sensors having an n-type pinning layer and a p-type collection region in an n-type well for reducing cross talk.

BACKGROUND OF THE INVENTION

[0003] Current day active pixel image sensors are typically built on either p- or n-type silicon substrates. Active pixel sensors refer to sensors having an active circuit element such as an amplifier in, or associated with, each pixel. CMOS refers to "complimentary metal oxide silicon" transistors in which two transistors composed of opposite dopants (one of p-type and one of n-type) are wired together in a complimentary fashion. Active pixel sensors also typically use CMOS transistors, and as such, are used interchangeably.

[0004] The CMOS sensors built on p-type substrates typically contain a higher level of circuit integration on chip due to the fact that the process is derived from standard CMOS, which is already fully developed and contains all the necessary devices and circuit libraries to support this high level of integration. Unfortunately, these sensors suffer from high levels of pixel-to-pixel cross talk that results from the lateral diffusion of minority carriers within the p-type substrates on which they are built. On the other hand, CMOS image sensors built using processes derived from typical interline CCD image sensors, (wherein the focal plane is built in a p-well on an n-type substrate), have much lower cross talk due to the elimination of lateral carrier diffusion as a result of the vertical-overflow drain (VOD) structure. For these devices, color cross talk is primarily optical as limited by the transmission of the overlying CFAs.

[0005] Although there have been several recent proposals to reduce the electrical cross talk within the silicon substrates for CMOS sensors built on p-type substrates, (U.S. Provisional Application Nos. 60/721,168 and 60/721,175, both filed on Sep. 28, 2005), the cross talk can not be reduced low enough using these techniques for certain applications. And although a CMOS process could be developed on n-type substrates, it would require the complete re-engineering of all of the support circuitry and devices. It would also require that the AC ground plane, in this case the substrate, be biased at the VDD supply voltage, which is not desirable from a noise point of view. N-type substrates are also more difficult to get than p-type substrates, which can result in a higher level of dark current defects.

[0006] Therefore, there exists a need within the art to provide a CMOS image sensor with reduced cross talk while maintaining all of the current advantages and level of development of existing mainstream CMOS processes.

SUMMARY OF THE INVENTION

[0007] The present invention is directed to overcoming one or more of the problems set forth above. Briefly summarized, according to one aspect of the present invention, the present invention resides in an image sensor with an image area having a plurality of pixels each having a photodetector of a first conductivity type, the image sensor comprising a substrate of the first conductivity type; a first layer of the second conductivity type between the substrate and the photodetectors, spanning the image area and biased at predetermined potential with respect to the substrate for driving excess carriers into the substrate to reduce cross talk; one or more adjacent active electronic components disposed in the first layer within each pixel; and electronic circuitry disposed in the substrate outside of the image area.

[0008] These and other aspects, objects, features and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

Advantageous Effect of the Invention

[0009] The present invention has the advantage of reducing cross talk and the bulk-diffusion component of dark current while retaining all the advantages of using mainstream standard CMOS integrated on a p-type substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. **1** shows the top view of an image-area pixel used in a typical prior art CMOS image sensor;

[0011] FIG. **2***a* shows a schematic view of a two-dimensional doping structure taken through a cross section through the transfer gate and floating diffusion of a typical prior art pinned photodiode detector;

[0012] FIG. **2***b* shows the 1-D doping profile vs. depth into the silicon through the middle of the prior art photodiode;

[0013] FIG. **2***c* shows the 1-D potential profile vs. depth into the silicon through the middle of the prior art photodiode;

[0014] FIG. **3** illustrates example results of a 2-D calculation of pixel-to-pixel cross talk vs. depletion depth of a prior art CMOS active pixel image sensor pixel;

[0015] FIG. **4***a* shows a schematic view of a two-dimensional doping structure for the PMOS pixel structure of the present invention taken through a cross section through the transfer gate, floating diffusion, and reset gate;

[0016] FIG. **4***b* shows a top view of an exemplary layout for the image sensor of FIG. **4***a;*

[0017] FIG. **4***c* shows the 1-D doping profile vs. depth into the silicon through the middle of the PMOS pixel structure of the present invention;

[0018] FIG. **4***d* shows the 1-D potential profile vs. depth into the silicon through the middle of the PMOS pixel structure of the present invention;

[0019] FIG. **5** shows the results of a 2-D calculation of pixel-to-pixel cross talk vs. overflow or sink depth for various photodiode depletion depths for the PMOS pixel structure of the present invention built in a well; and

[0020] FIG. **6** is an illustration of a digital camera for illustrating a typical commercial embodiment of the present invention to which the ordinary consumer is accustomed.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Historically, charge-coupled device (CCD)-based image sensors have primarily used electrons as the signal-charge carrier to take advantage of their higher mobility to maintain good transfer efficiency at high data rates. To reduce color cross talk and smear, and to provide blooming protection, CCD imagers are also typically built in a well, or vertical-overflow drain (VOD) structure (see for example U.S. Pat. No. 4,527,182). Therefore, building a VOD structure along with the requirement for an n-channel requires that a p-well be formed in an n-type substrate.

[0022] CMOS-based image sensors have since become more readily available. Current day CMOS image sensors are typically built on either p- or n-type silicon substrates. Those built on p-type substrates using mainstream CMOS processing can contain high levels of circuit integration, but suffer from high levels of color cross talk. Those built using a typical CCD-like process on n-type substrates (S. Inoue et al., "A 3.25 M-pixel APS-C size CMOS Image Sensor," in Eizojoho Media Gakkai Gijutsu Hokoku (Technology Report, The Institute of Image Information and Television Engineers) Eijogakugiho, vol. 25, no. 28, pp. 37-41, March 2001. ISSN 1342-6893.) have low color cross talk, but have other shortcomings as previously described above.

[0023] Unlike CCD image sensors, CMOS image sensors have only one transfer, i.e., from the photodiode to the floating diffusion. Hence, a CMOS image sensor does not require as high a charge carrier mobility. As such, the lower mobility of holes would not be a deficiency for a CMOS image sensor. It is therefore one object of the present invention to disclose a CMOS image sensor employing a PMOS (p-channel) pixel structure using holes as the signal-charge carrier. This PMOS structure of the present invention allows the pixel to be built in an n-well on p-type epi to reduce pixel-to-pixel cross talk. However, unlike a typical CCD-based image sensor, this well is only used underneath (or spanning) the imaging section of the sensor. All of the digital and analog CMOS support circuitry integrated on the chip is formed in the p-type epi (see FIG. **4***b*, i.e., analog or digital circuits **80**, digital logic **90**, row decoder **100**, and column decoder **110**). This means that all of the physical aspects of the devices in the standard CMOS circuitry portion of the chip are retained. Additionally, unlike the CCD image sensors built in a well wherein this well is biased at ground and the substrate at some positive potential, by biasing the n-well of the present invention structure at VDD, the ground plane (i.e., the p-type epitaxial substrate) for the CMOS circuitry can be maintained at 0 V. This means that all of the electrical aspects of the standard CMOS circuitry portions of the chip are also retained. Only the direction of some logic pulses and the signal swing(s) in the digital and analog sections need to be inverted where appropriate, which is readily accomplished by those skilled in the art. Therefore, all of the advantages of p-type substrates mentioned above in the Background section are retained. The well-type structure also reduces dark current by eliminating the diffusion component from the substrate.

[0024] The top view of a typical prior art CMOS image sensor pixel is shown in FIG. **1**. The typical pixel consists of a photodiode (PD); a transfer gate (TG) for reading charge out of the photodiode; a floating diffusion (FD) for converting the signal charge into a voltage signal; a source-follower transistor (SF) which acts as a signal buffer whose gate is electrically connected to FD; a row-select transistor (RS) that selectively connects the outputs of the source-follower transistors to the column output circuits (not shown in FIG. **1**); and a reset gate (RG) for resetting the potential of the floating diffusion. A power supply voltage (VDD) is used to power the source follower and drain off signal charge from the floating diffusion during its reset operation.

[0025] A typical prior art CMOS image sensor pixel contains a pinned photodiode with a p+ type pinning layer and an n-type storage region built on p−/p++ epitaxial silicon wafers as illustrated by way of example in FIGS. **2***a*-**2***c*. The depletion region depth (shown in FIGS. **2***a* and **2***c*) defines the collecting boundary of the photodiode. An example doping profile down through the center of the prior art photodiode is shown in FIG. **2***b*. Charge carriers (electrons) generated from shorter wavelength light that are created within the collecting region (i.e., depletion region boundary) are captured and stored as signal charge. Charge carriers generated from longer wavelengths that are created past this depletion depth are free to diffuse in any direction via thermal diffusion. Any charge that diffuses laterally and gets collected by adjacent pixels is called electrical cross talk.

[0026] Cross talk can be quantified by defining it as the ratio of the signal in the non-illuminated to the illuminated pixel (s), and can be expressed as either a fraction or percentage. Therefore, cross talk represents the relative amount of signal that does not get collected by the pixel(s) under which it was generated. The dependence of cross-talk on depletion depth for the example prior-art pixel is illustrated in FIG. **3**. The cross-talk calculation assumes that every other pixel along a line is illuminated (and the alternating, interleaved pixels are not). A wavelength of 650 nm is assumed, because cross talk is more of a problem at longer wavelengths because the optical absorption coefficient is lower at longer wavelengths, (i.e., the photons are absorbed deeper). It can be seen from this figure that although increasing the depletion depth can reduce cross talk, it does not go to zero even for depletion depths up to 3 um, which is approximately one over the absorption coefficient for silicon at 650 nm.

[0027] A cross section of the PMOS pixel architecture of the present invention is shown in FIG. **4***a*. The top view of an example CMOS image sensor containing this pixel structure is shown in FIG. **4***b*. An example doping profile down through the center of the photodiode is shown in FIG. **4***c*. An example potential profile down through the center of the empty photodiode is shown in FIG. **4***d*. As can be seen by FIGS. **4***a* and **4***c*, the pinned photodiode **10** of the present invention embodies an n+ pinning layer **20** and p-type buried storage region **30** built within an n-type well **40** on a p−/p++ epitaxial substrate **50**. Because the photodiode's surface pinning layer **20** of the present invention is n-type, arsenic can be used. This makes it easier to create a shallow pinning layer due to the shorter implant range of arsenic compared to that of boron. (The prior art structure has a p-type pinning layer for which boron is typically used). Also, because the photodiode's storage region **30** is now p-type instead of n-type, boron can be used, (which has a longer implant range than phosphorous or arsenic as required for the storage region of the prior art structure), thereby making it easier to make this implant deep. The n+ pinning layer **20** is electrically connected to the n-well **40** via the n+ type isolation implant **60** around the typical shallow trench isolation (STI) region as can be seen in FIG.

4*a*. This pinning layer **20** maintains the surface of the diode in accumulation (of electrons). Signal charge is stored in the form of holes in the p-type buried storage region **30** of the pinned photodiode **10**. The n-type well **40** is only formed in the image area **70** having a plurality of pixel as illustrated by the top view shown in FIG. **4***b*. By forming this well **40** only in the image area **70**, the image sensor **75** uses standard mainstream CMOS devices and circuitry in the analog or digital circuits **80**, digital logic **90**, row decoder **100**, and column decoder **110** while retaining all the benefits of a p-type substrate. It is preferable to form this n-well **40** at the beginning of the process so that its formation does not affect other device structures. For example, if it is formed via an implant and thermal drive, by doing this prior to the standard CMOS processing, the thermal drive step will not cause diffusion of shallow junction regions as required by the devices used in the CMOS support circuitry surrounding the image area. When formed in this n-well **40**, the pixel's transfer gate (TG), reset gate (RG), and source follower (SF) transistors are all preferably p-type metal oxide silicon (note that the gate is not usually metal; it is polysilicon, and sometimes the dielectric is not solely oxide), field effect transistors (PMOS FETs). A row select transistor (RS not shown) in series with the output of the source follower amplifier (SF) would also be a PMOS device. All of the peripheral supporting CMOS circuitry **80**, **90**, **100** and **110** is formed within the p−/p++ epitaxial substrate. The substrate is at ground and the n-well **40** is biased at a convenient positive bias, such as VDD. After (or during) image integration, the floating diffusion (FD) is reset with a negative going pulse on the reset gate (RG) prior to signal transfer from the photodiode. A convenient FD reset voltage level is ground. After the floating diffusion is reset, (i.e., after the RG pulse), transfer of charge (holes) from the photodiode to floating diffusion is initiated by a negative going pulse on the transfer gate, TG. An example of convenient clock voltages (VDD) used for these pulses are shown in FIG. **4***a*. Other voltages may be possible without departing from the scope of the invention. Since the signal charge is holes for the present invention structure, the signal swing on the floating diffusion and source follower (SF) output will be positive going. Any photosignal (holes) that is generated within the n-well **40** beneath the photodiodes collecting region **30** is swept into the substrate **50** before it can diffuse to neighboring pinned photodiodes **10**, thereby eliminating electrical cross talk. The signal would be read out from the chip in the usual manner as would be well known by those working in the art. The potential barrier between the substrate and photodiode that results from this structure also eliminates the diffusion component of dark current from the substrate (bulk) into the photodiode.

[0028] Electrical cross talk for the pixel structure of the present invention with a pinned photodiode built in an n-well on a p-type substrate is greatly reduced as shown in FIG. **5**. Cross talk is shown versus sink depth (the depth past which carriers are drained to the substrate) for various depletion depths. The calculations are carried out by the methods described by E. G. Stevens and J. P. Lavine in *IEEE Trans. on Electron Devices,* vol. 41, no. 10, p. 1753, October 1994. For this sample calculation, a constant n-well doping concentration vs. depth was assumed. For an actual device wherein the n-well would preferably be formed via ion implantation, the resulting doping gradient (such as shown in FIG. **4***c*) would create a potential gradient (as shown in FIG. **4***d*) such that minority carriers (holes) in the n-well would be driven into the substrate thereby resulting in the virtual elimination of electrical cross talk and the substrate dark current component.

[0029] Referring to FIG. **6**, there is shown a digital camera **120** having an image sensor **75** of the present invention disposed therein for illustrating a typical commercial embodiment to which the ordinary consumer is accustomed.

[0030] Although the preferred embodiment of the present invention shown incorporates a pinned photodiode consisting of an n+ pinning (top surface) layer and a p-type buried collecting region within an n-well on a p-type epi substrate, it will be understood the those skilled in the art that other structures can be used without departing from the scope of the invention. For example, a simple unpinned p-type diode formed in an n-type well could be used, if desired. Also, although a simple non-shared pixel architecture is shown, a shared architecture, (such as U.S. Pat. No. 6,107,655 for example), could also be used without departing from the scope of the invention.

[0031] The invention has been described with reference to a preferred embodiment. However, it will be appreciated that variations and modifications can be effected by a person of ordinary skill in the art without departing from the scope of the invention.

PARTS LIST

[0032] **10** pinned photodiode
[0033] **20** n+ pinning layer
[0034] **30** p-type buried storage region
[0035] **40** n-type well
[0036] **50** p−/p++ epitaxial substrate
[0037] **60** n+ type isolation implant
[0038] **70** image area
[0039] **75** image sensor
[0040] **80** analog or digital circuits
[0041] **90** digital logic
[0042] **100** row decoder
[0043] **110** column decoder
[0044] **120** digital camera

1. An image sensor including an image area having a plurality of pixels with at least one pixel having a photodetector of a p conductivity type which use holes as charge carriers, the image sensor comprising:

a substrate of the p conductivity type;

a first layer of n conductivity type between the substrate and the at least one p-type photodetector, wherein the first layer spans the entire image area having the plurality of pixels; and

a contact electrically connected to the first layer for biasing the first later at a predetermined potential with respect to the substrate for driving excess carriers into the substrate to reduce cross talk.

2. The image sensor as in claim **1**, further comprising:

one or more adjacent active P-channel Metal Oxide Semiconductor (PMOS) electronic components disposed in the first layer with the at least one pixel; and

CMOS electronic support circuitry disposed in the substrate outside of the image area and electrically connected to the image area.

3. The image sensor as in claim **1**, further comprising an isolation region disposed adjacent to a portion of at least one photodetector.

4. The image sensor as in claim **3**, further comprising an isolation implant of n conductivity type surrounding at least a portion of at least one photodetector.

5. The image sensor as in claim **3**, wherein the isolation implant of n conductivity type comprises an arsenic implant region.

6. The image sensor as in claim **1**, further comprising a pinning layer of the n conductivity type.

7. The image sensor as in claim **6**, wherein the pinning layer of the n conductivity type comprises an arsenic implant region.

8. The image sensor as in claim **1**, wherein the photodetector of the p conductivity type comprises a boron implant region.

9. The image sensor as in claim **1**, further comprising a p-epitaxial layer disposed between the substrate and the first layer.

10. The image sensor as in claim **3**, further comprising a pinning layer of the n conductivity type connected to the isolation region.

11. The image sensor as in claim **2**, wherein the predetermined potential is set to a supply voltage connected to at least one PMOS electronic component.

12. An image capture device, comprising:

an image sensor including an image area having a plurality of pixels with at least one pixel having a photodetector of a p conductivity type which use holes as charge carriers, the image sensor comprising:

a substrate of the p conductivity type;

a first layer of n conductivity type between the substrate and the at least one p-type photodetector, wherein the first layer spans the entire image area having the plurality of pixels; and

a contact electrically connected to the first layer for biasing the first later at a predetermined potential with respect to the substrate for driving excess carriers into the substrate to reduce cross talk.

13. A method for producing an image sensor including an imaging area having a plurality of pixels and a CMOS device area disposed outside of the imaging area, the method comprising:

prior to producing any structures in the CMOS device area, forming a first layer of n conductivity type over a substrate of p conductivity type, wherein the first layer spans the entire image area; and

forming the plurality of pixels and at least one structure in the CMOS device area.

* * * * *