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Jordan et al. [43] **Apr. 5, 1977**

[54] **VOLTAGE-MODE LOGIC CIRCUITRY WITH IMPROVED INPUT/OUTPUT CHARACTERISTICS**

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[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **710,764**

[22] Filed: **July 30, 1976**

Related U.S. Application Data

[63] Continuation of Ser. No. 450,279, March 11, 1974, abandoned, which is a continuation of Ser. No. 265,136, June 22, 1972, abandoned.

[51] Int. Cl.[2] **H03K 19/08**; H01L 27/00

[52] U.S. Cl. ..... **307/213**; 307/215; 307/270; 307/317 A; 307/DIG. 1

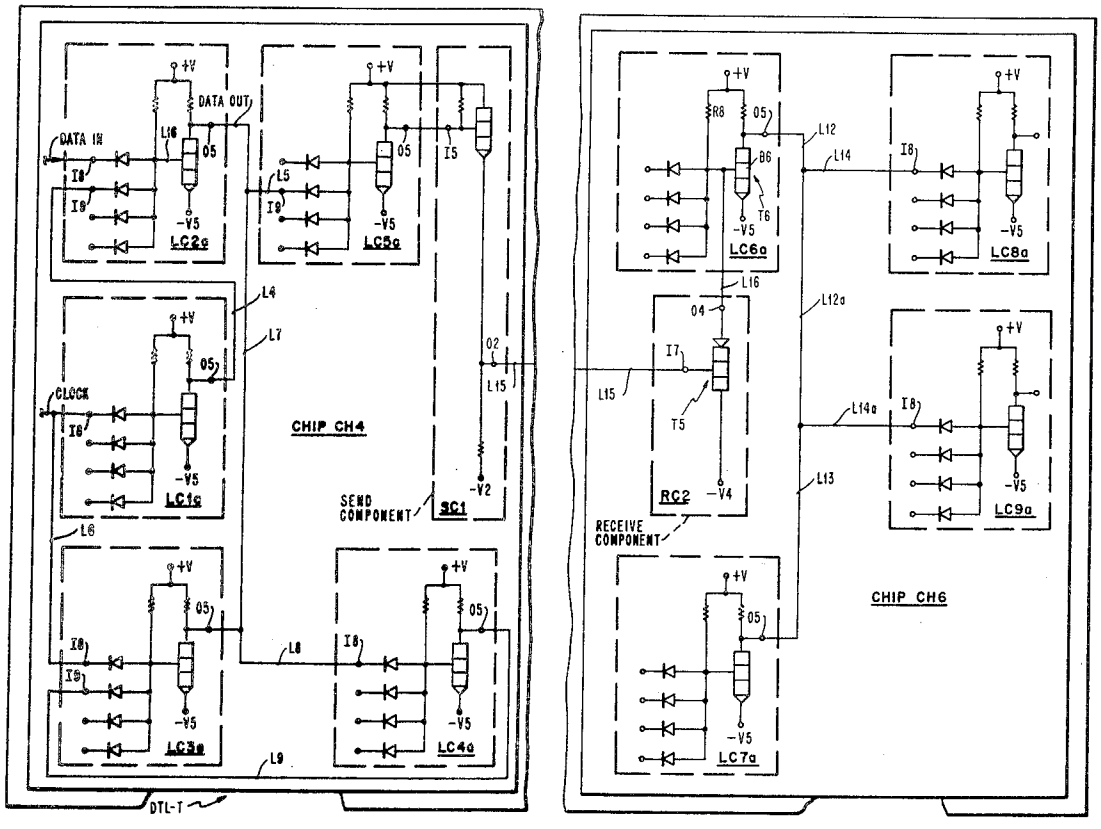
[57] **ABSTRACT**

Coupling of signals between Large Scale Integrated Circuit chips is facilitated by provision of an emitter follower output stage for the chip. Special input circuits are also provided. The logic circuits may be DTL or Schottky TTL. The special input circuit may be a DTL type or a CTL (complementary transistor logic) type. Pull down resistors may be employed with the emitter follower output driver and the special DTL input circuit.

1 Claim, 9 Sheets Drawing,

22 Pages Specification

The file of this unexamined application may be inspected and copies thereof may be purchased (849 O.G. 1221, Apr. 9, 1968).



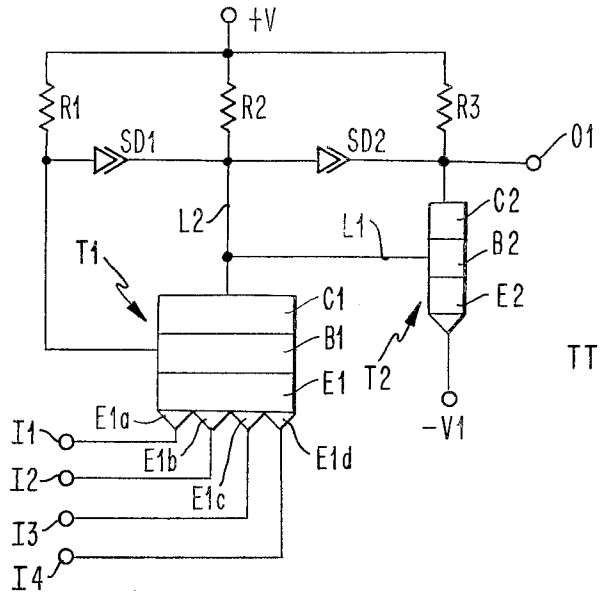


FIG. 1
TTL LOGIC CIRCUIT
PRIOR ART

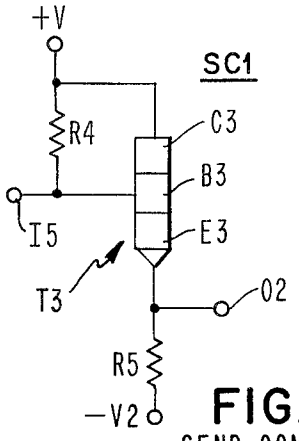


FIG. 2
SEND COMPONENT

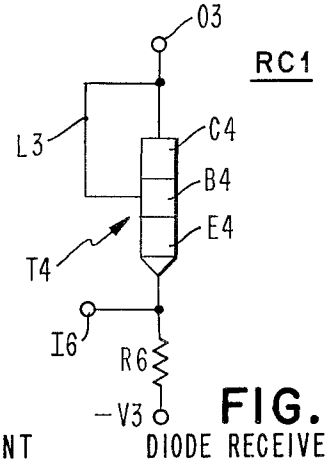


FIG. 3
DIODE RECEIVE COMPONENT

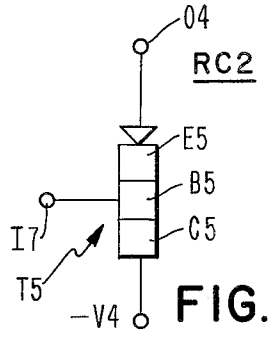


FIG. 5
TRANSISTOR
RECEIVE COMPONENT

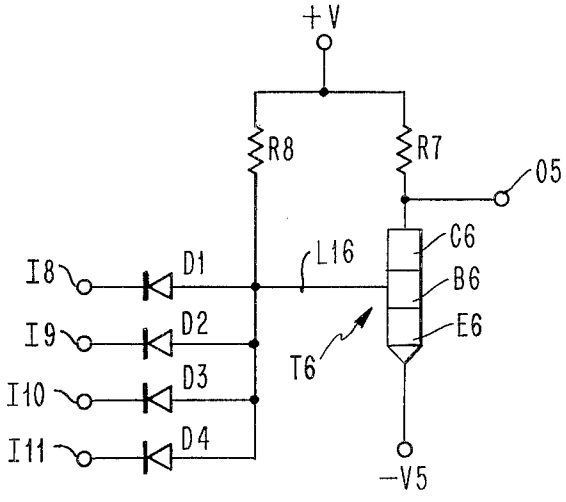


FIG. 7
DTL LOGIC CIRCUIT
PRIOR ART

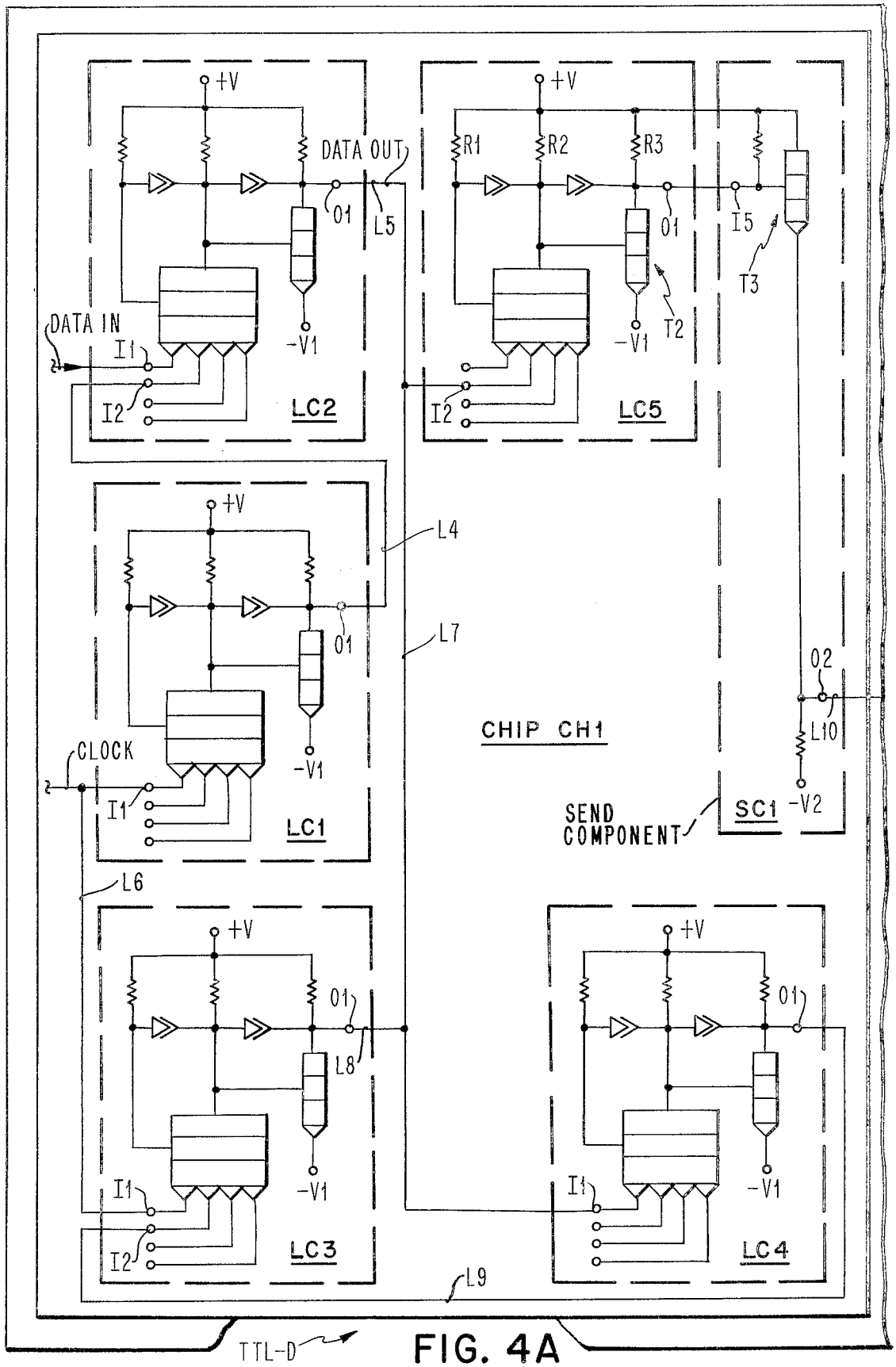

+V
DATA OUT
O1
L5
DATA IN
I1
I2
-V1
LC2
R1
R2
R3
I5
T3
T2
LC5
L4
L7
CLOCK
LC1
CHIP CH1
O2
L10
-V2
SEND COMPONENT
SC1
L6
L8
LC3
LC4
L9
TTL-D

FIG. 4A

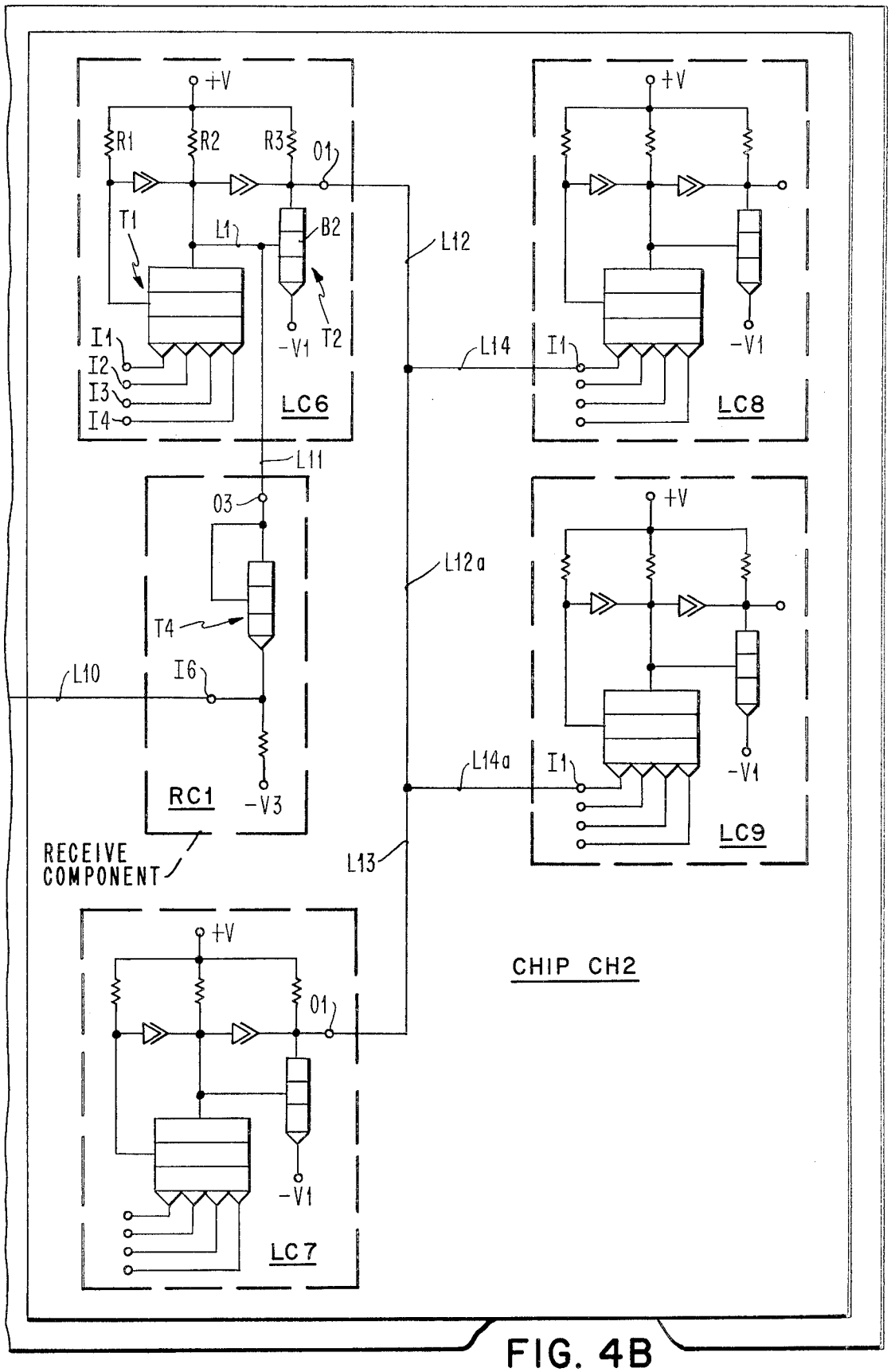

+V
R1
R2
R3
O1
T1
L1
B2
T2
-V1
I1
I2
I3
I4
LC6
L12
L14
LC8
L11
O3
T4
I6
L10
RC1
-V3
RECEIVE COMPONENT
L12a
L14a
LC9
L13
CHIP CH2
LC7

FIG. 4B

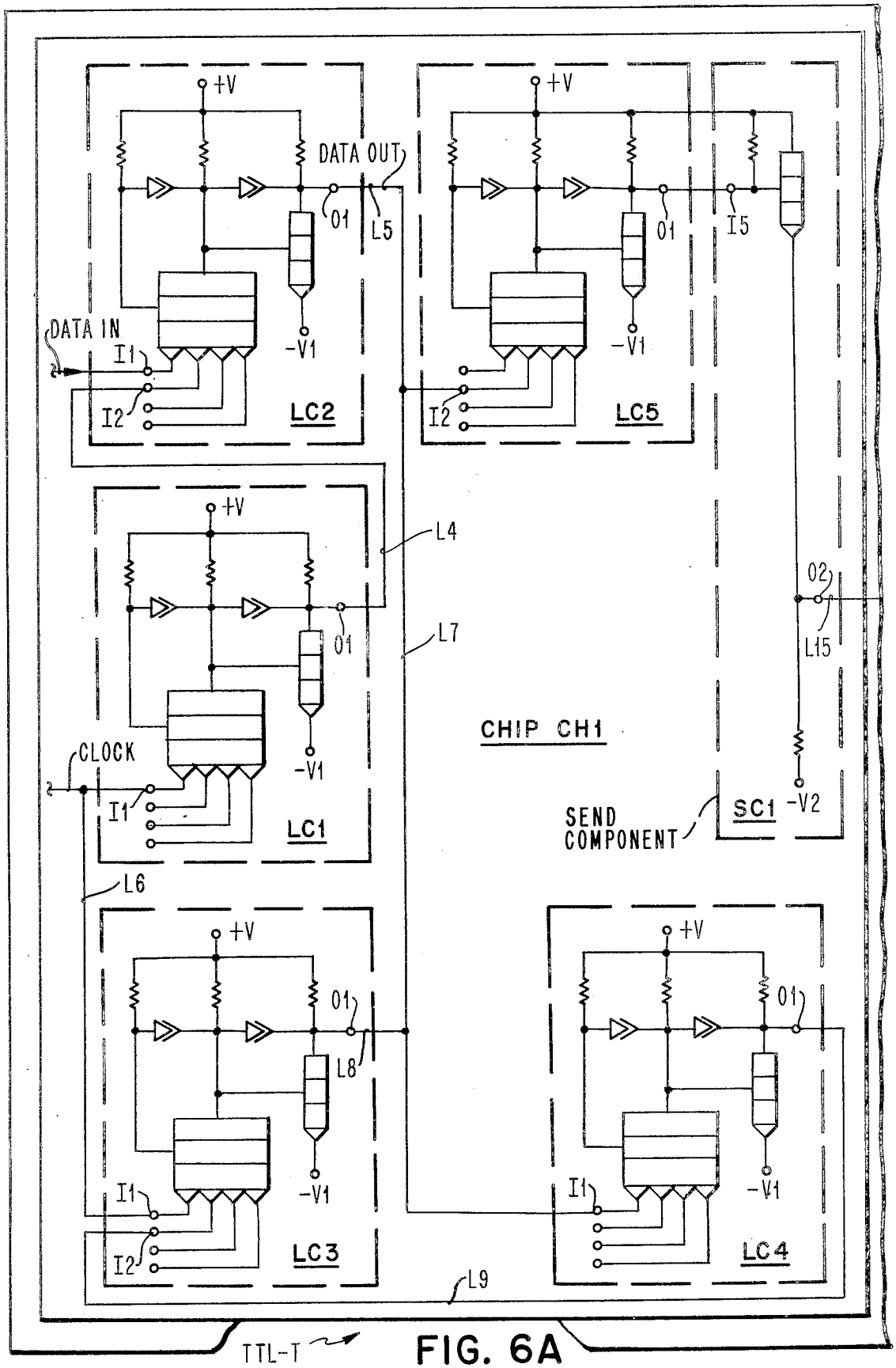

+V
DATA OUT
O1
L5
DATA IN
I1
I2
-V1
LC2
+V
O1
I5
-V1
I2
LC5
+V
L4
O1
L7
CLOCK
I1
-V1
LC1
CHIP CH1
O2
L15
SEND COMPONENT
SC1
-V2
L6
+V
O1
L8
I1
I2
-V1
LC3
+V
O1
I1
-V1
LC4
L9
TTL-T

FIG. 6A

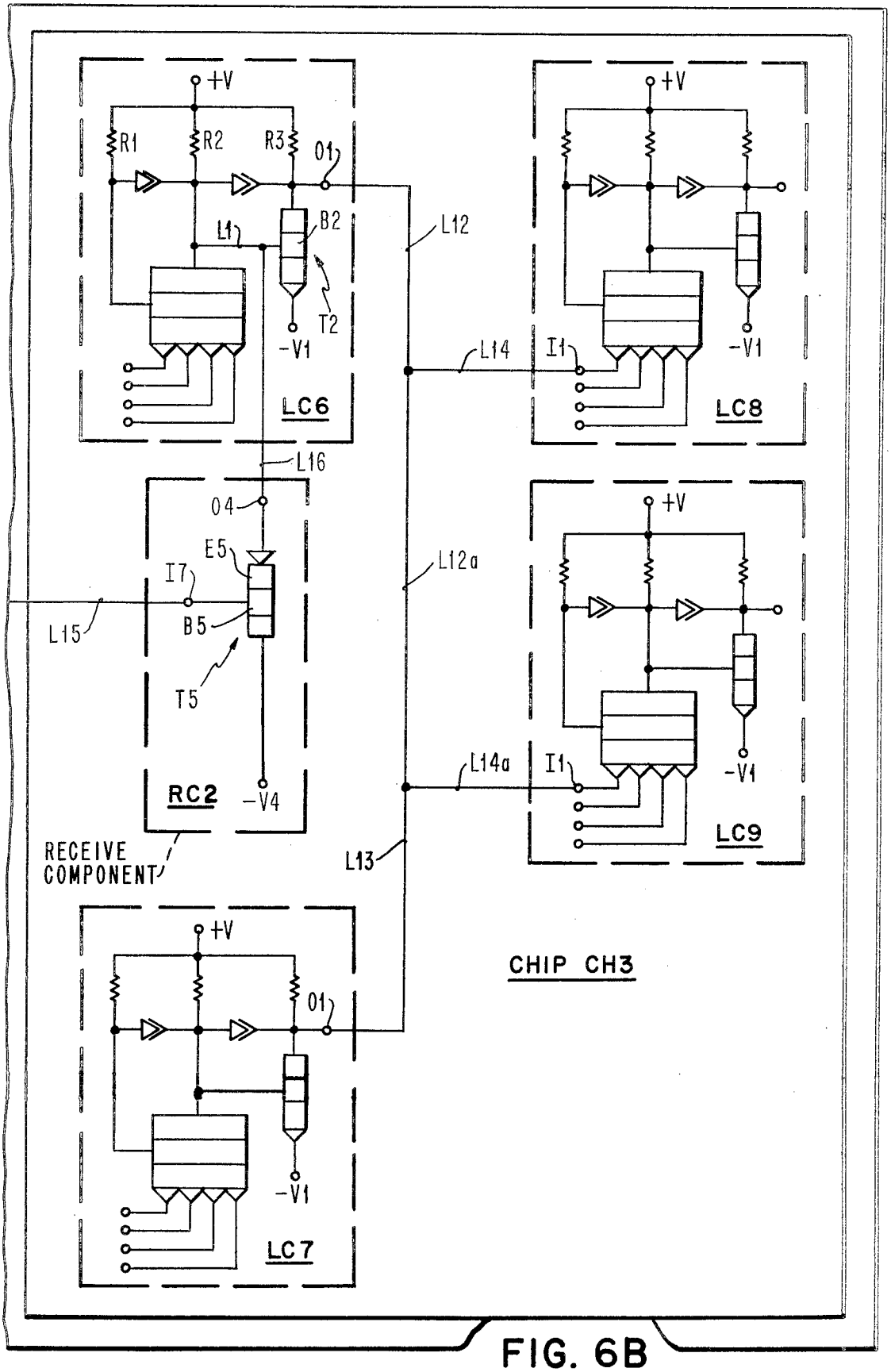

+V
R1
R2
R3
01
L1
B2
T2
-V1
LC6
L12
L14
I1
LC8
L16
04
E5
I7
L15
B5
T5
RC2
-V4
RECEIVE COMPONENT
L12a
L14a
LC9
L13
CHIP CH3
LC7

FIG. 6B

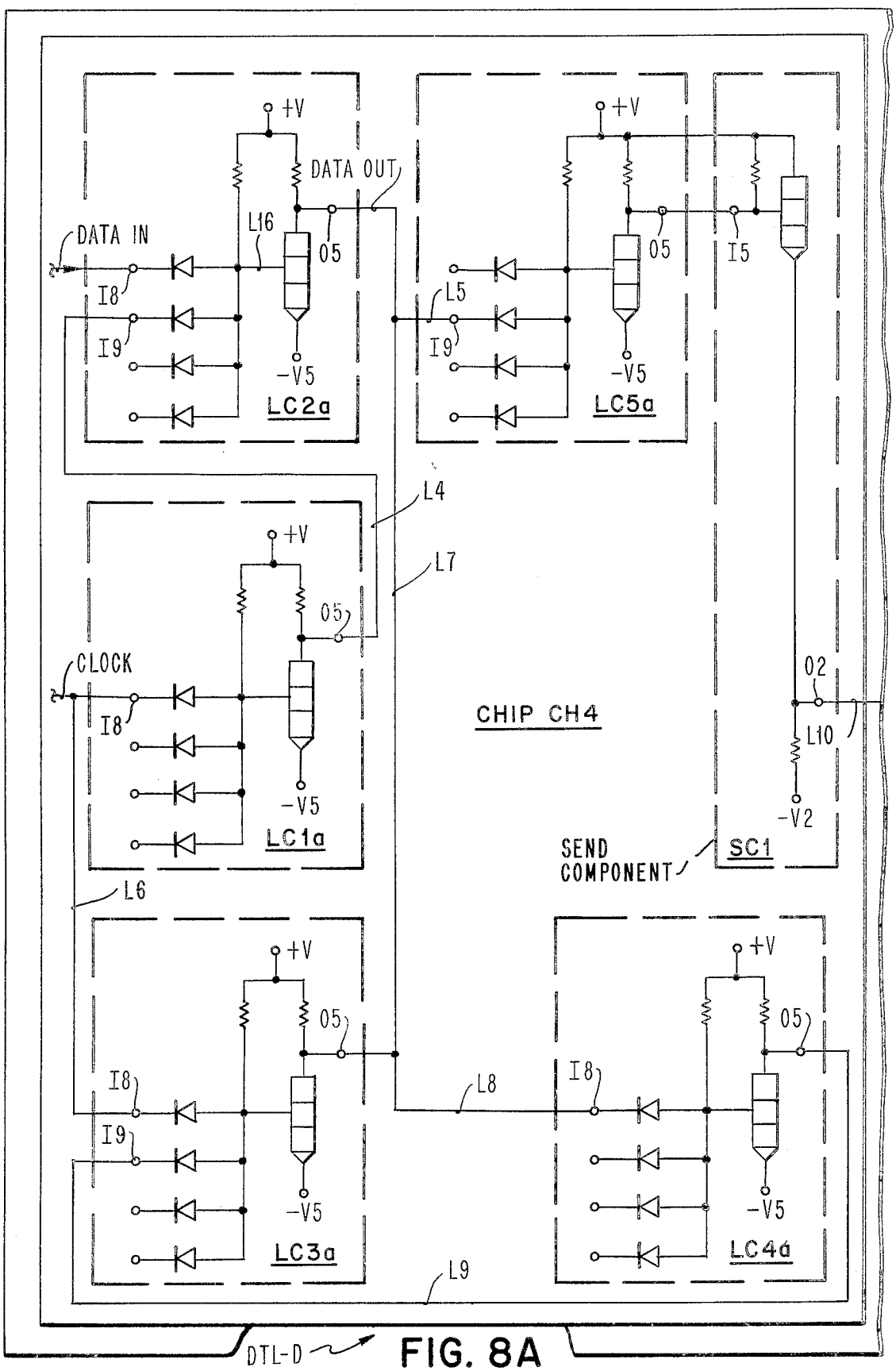

+V
DATA OUT
DATA IN
L16
05
I8
I9
-V5
LC2a
L5
LC5a
I5
L4
L7
CLOCK
LC1a
CHIP CH4
02
L10
-V2
SEND COMPONENT
SC1
L6
LC3a
L8
LC4a
L9
DTL-D

FIG. 8A

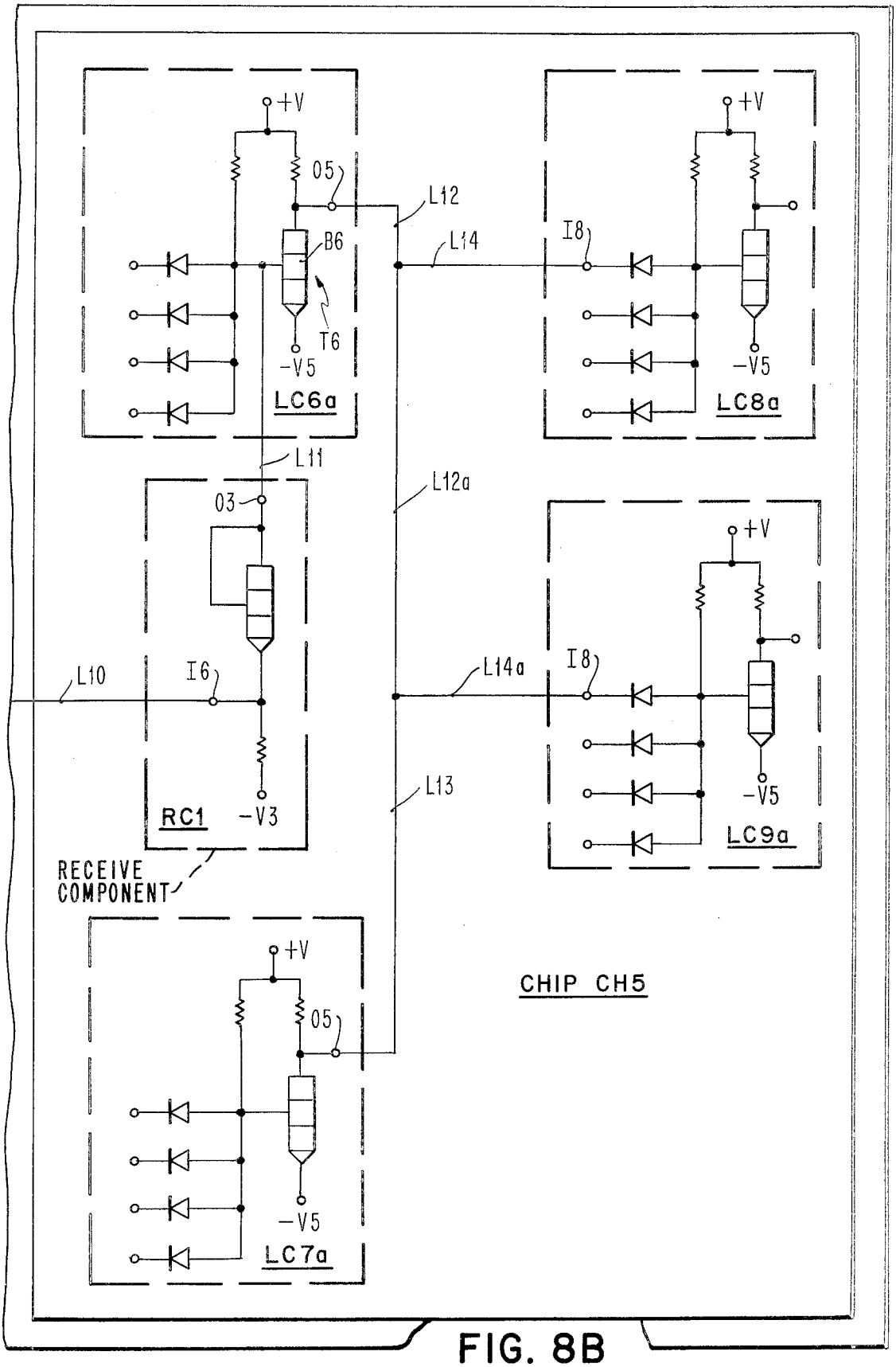

+V
05
L12
B6
L14
T6
-V5
LC6a
I8
+V
-V5
LC8a
L11
L12a
03
+V
I8
L10
I6
L14a
-V5
LC9a
RC1
-V3
L13
RECEIVE COMPONENT
CHIP CH5
+V
05
-V5
LC7a

FIG. 8B

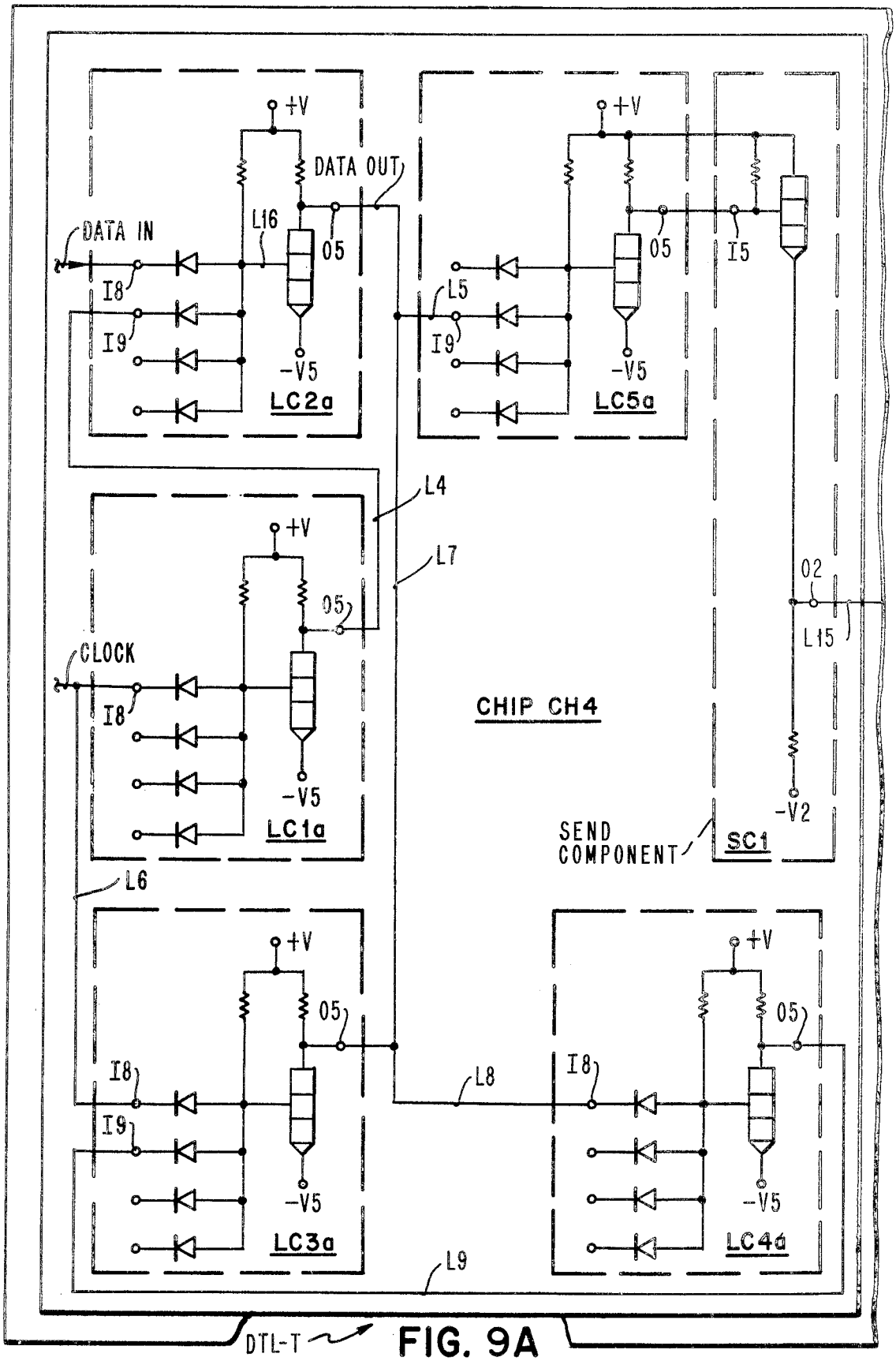

+V
DATA OUT
DATA IN
L16
05
I8
I9
-V5
LC2a
+V
05
I5
L5
I9
-V5
LC5a
L4
L7
+V
05
CLOCK
I8
-V5
LC1a
CHIP CH4
02
L15
-V2
SEND COMPONENT
SC1
L6
+V
05
I8
I9
-V5
LC3a
L8
+V
05
I8
-V5
LC4a
L9
DTL-T

FIG. 9A

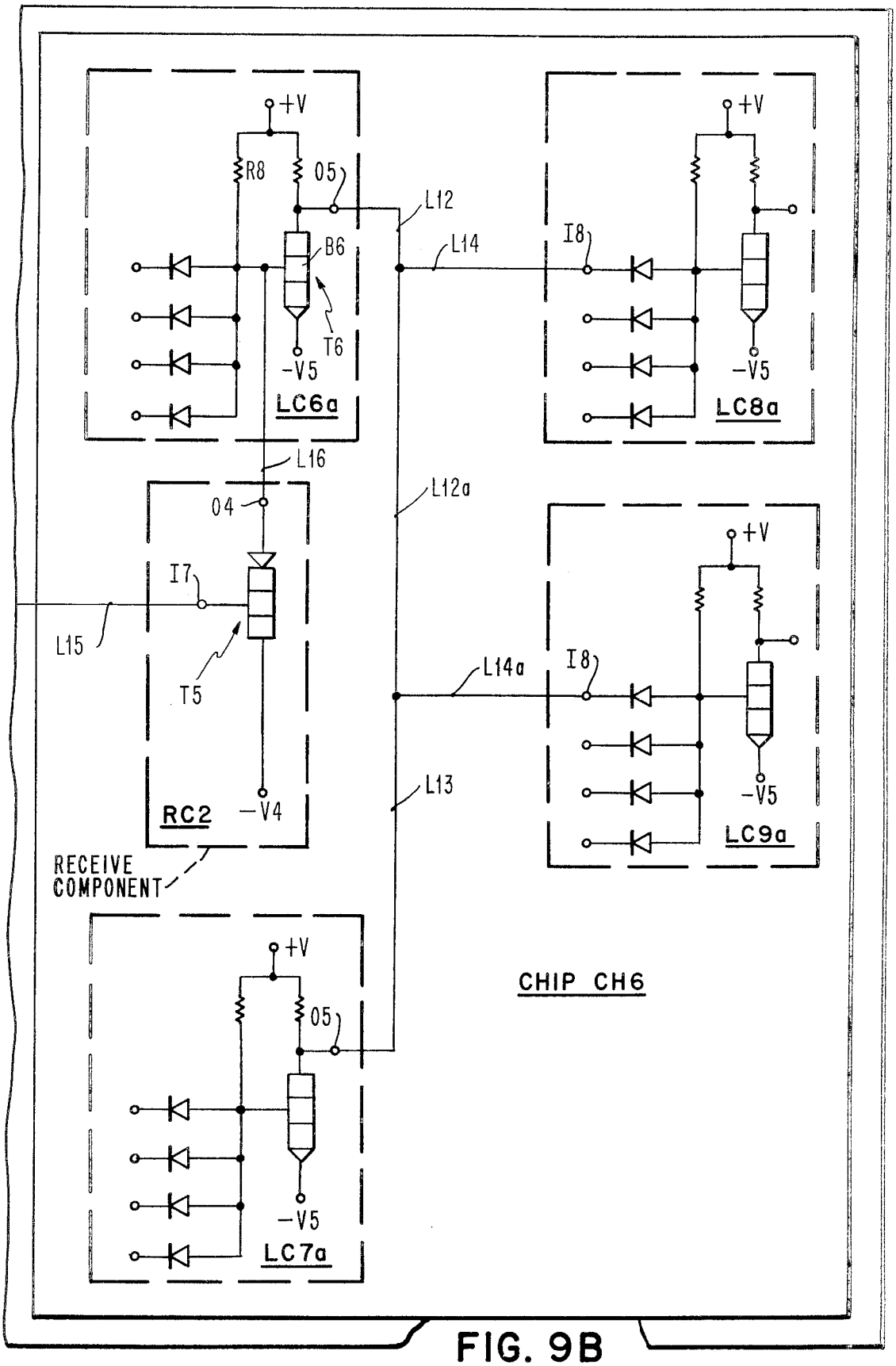

+V
R8
05
L12
L14
B6
T6
-V5
LC6a
I8
LC8a
L16
L12a
04
I7
L15
T5
RC2
-V4
L14a
L13
RECEIVE COMPONENT
LC9a
CHIP CH6
LC7a

FIG. 9B