United States Patent

McIntosh

[15] **3,664,117**

[45] **May 23, 1972**

[54] NON-TIME INDICATING NUMBER CORRECTION CIRCUIT

[72] Inventor: **Bruce C. McIntosh,** Utica, N.Y.

[73] Assignee: **General Electric Company**

[22] Filed: **June 5, 1970**

[21] Appl. No.: **43,786**

[52] **U.S. Cl.** .....**58/35 W,** 235/92 T

[51] **Int. Cl.**.....**G04c 9/02**

[58] **Field of Search** .....58/23, 34, 35 W; 235/92 PE, 235/92 T; 328/48

[56] **References Cited**

UNITED STATES PATENTS

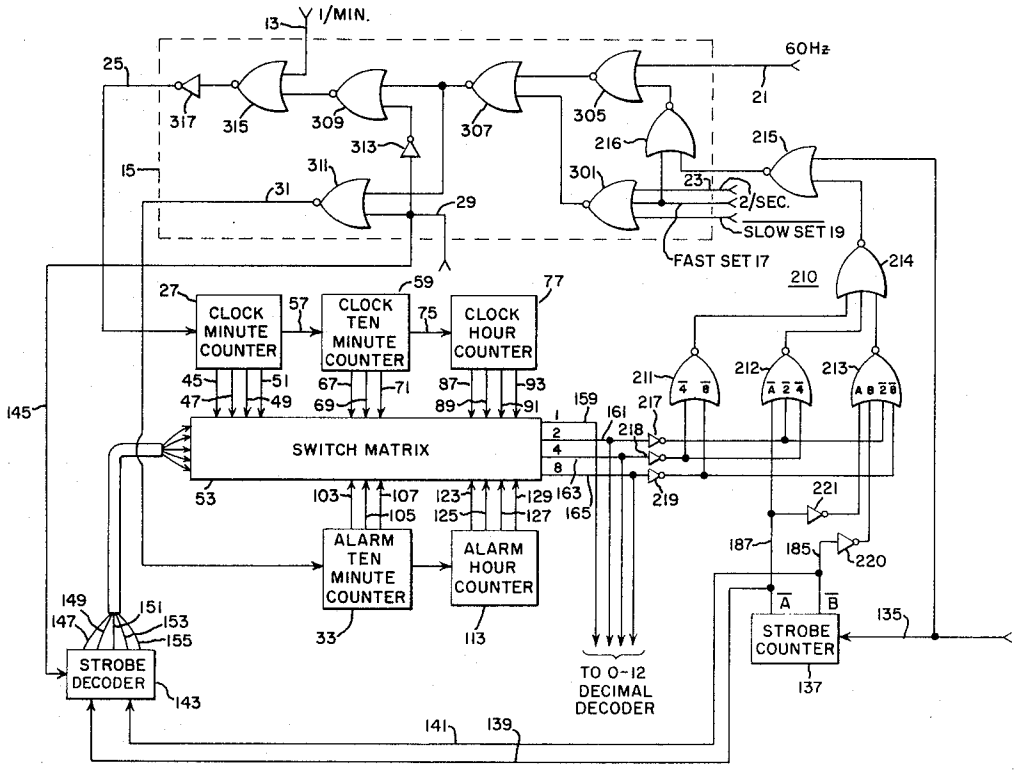
3,051,855	8/1962	Lee	328/48 X
3,067,936	11/1962	Kasper et al.	235/92
3,163,747	12/1964	Veverka	235/92
3,178,586	4/1965	Rosenfield	328/48 X
3,307,023	2/1967	Burger	235/92
3,350,580	10/1967	Harrison	328/48 X

Primary Examiner—Richard B. Wilkinson
Assistant Examiner—Edith C. Simmons
Attorney—Marvin A. Goldenberg, W. Joseph Shanley, Jr., Frank L. Neuhauser, Oscar B. Waddell and Joseph B. Forman

[57] **ABSTRACT**

When power is applied to a digital clock, the counters therein can assume forbidden states and non-time indicating numbers are generated. This problem is eliminated by a gate circuit responsive to each such non-time indicating number to apply a high frequency signal source to the counter to advance the counter to a time indicating number. Because non-time indicating numbers can also occur on a transient basis, the gate circuit also includes a time delay to avoid response to such transients. The time delay may be provided by a second signal synchronized with the source of transient generation and gated with the strobe signal in a phase to block response to the transient for one-half cycle of the second signal. This non-time indicating number correction circuit is also employed to correct non-time indicating numbers in the alarm time counter when the digital clock is switched to present an alarm time indication.

6 Claims, 3 Drawing Figures



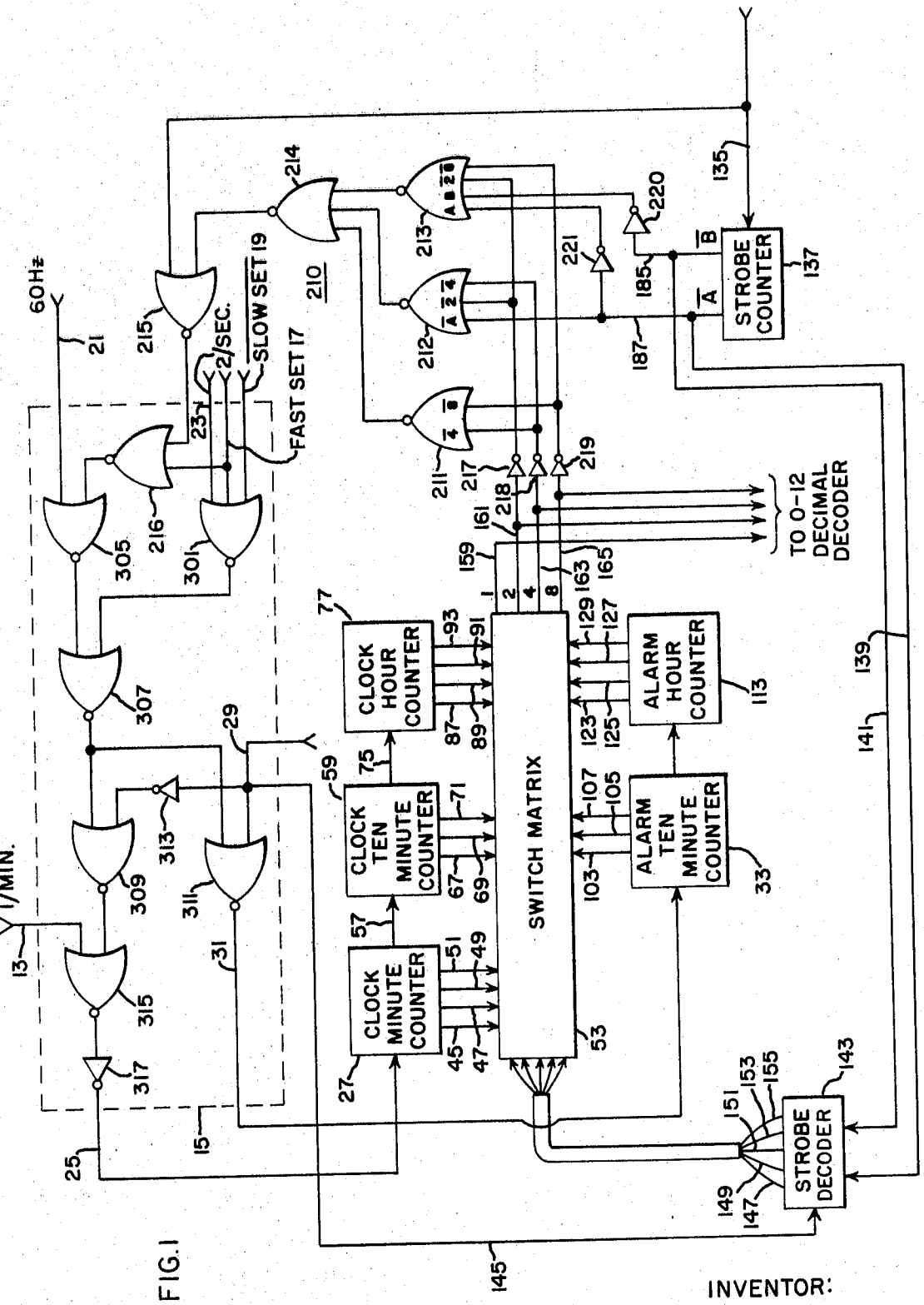


FIG. 1

INVENTOR:
BRUCE C. McINTOSH,
BY Stanley C Corwin
HIS ATTORNEY.

FIG.2

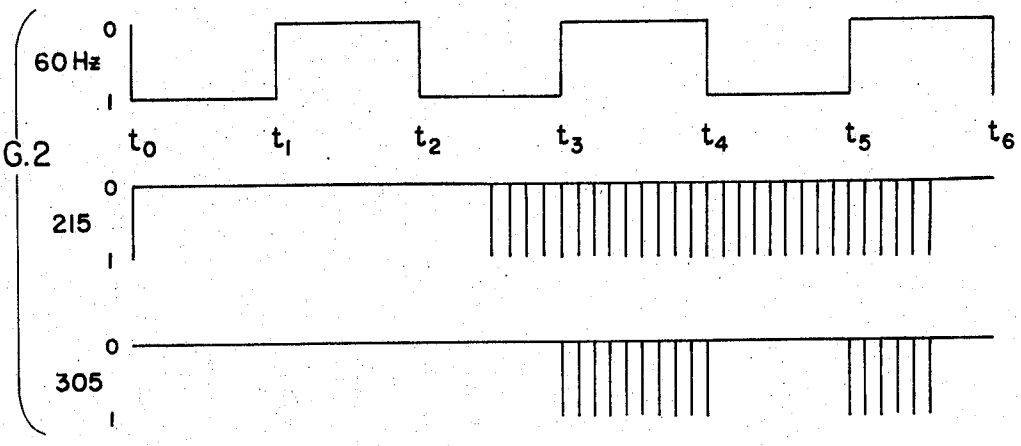
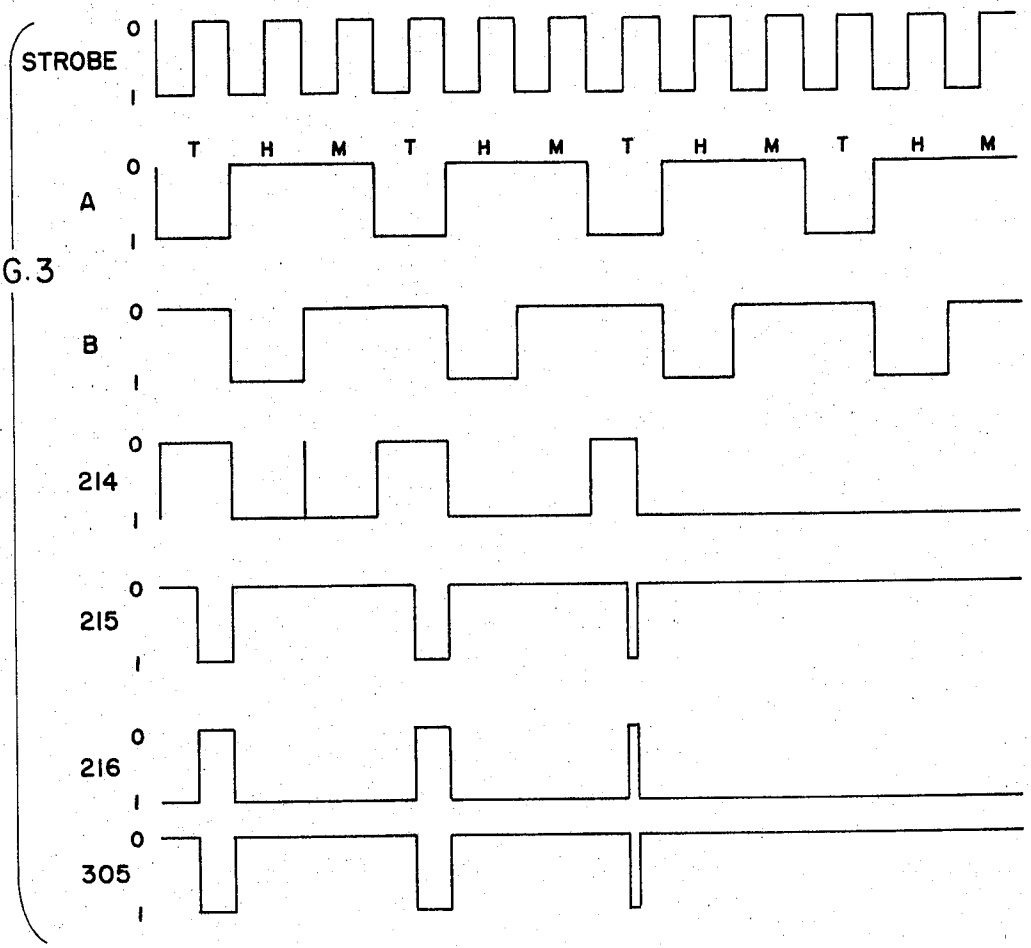


FIG.3



INVENTOR:
BRUCE C. McINTOSH,

BY Stanley Cowin

HIS ATTORNEY.

NON-TIME INDICATING NUMBER CORRECTION CIRCUIT

FIELD OF THE INVENTION

This invention relates to a counter correction circuit and more particularly to a circuit for correcting a time indicating counter whenever the counter registers a non-time indicating number.

HISTORY OF THE ART

In application Ser. No. 25,930, entitled Digital Clock Controlled by Voltage Level of Clock Reference Signal, and assigned to the same assignee as the instant application filed Apr. 6, 1970, by Paul Emerson, Hans Thamhain and Bruce McIntosh, there is described a digital clock. This clock utilizes a plurality of binary counters to formulate a digital representation of time. One drawback of such counters is that usually each is made of a greater number of flip-flops than necessary for the modulus desired from the counter. Thus, for example, the 0 to 9 minutes counter would require four flip-flops capable of counting from 0 to 15. While these four flip-flops are gated to recycle upon reaching a count of 9, when power is first applied, or after a power interruption, the counter is capable of assuming states representing non-time indicating numbers such as 10, 11, 12, 13, 14 and 15. Although the counters will eventually advance to time indicating numbers, the display of a non-time indicating number is undesirable as it may be taken as a malfunction by the user of the clock.

SUMMARY OF THE INVENTION

A solution for the elimination of non-time indicating numbers includes a gate circuit responsive to each number outside the time indicating range of numbers of each counter. A high frequency signal source, such as the strobe signal which, as described in the above-mentioned application, sequentially switches the time indicating counters to the time display device, is applied to the counters by the gate circuit to rapidly change the count. This count advancing continues until the gate circuit no longer sees a non-time indicating number.

The counters in the digital clock described in the above-mentioned application are sequentially read out to the display. Accordingly, it is possible to have a count overlay momentarily appear during the transition in sequential switching from the readout of one counter to the readout of another counter so that non-time indicating number may be transiently presented to the gate circuit for correction of such numbers. It is also possible to realize a forbidden count for the moment when the counter changes from one count to the next. As employed in the present discussion, forbidden count is intended to mean a count falling outside of the logic constraints imposed upon the circuitry, which count may result in the display of a non-time indicating number. Thus a delay is provided to prevent response by the gate circuit to such transiently occurring non-time indicating numbers.

In the case where a forbidden number momentarily is present due to the count change of a counter, the delay to the gate means is occasioned by applying to the gate circuit the 60 Hz signal from which the time counters' count change signals are derived. Because each counter can only change on the 0 to 1 transition of the 60 Hz signal, this signal is of proper phase to block gate circuit response to the transient for one-half cycle (8.3 milliseconds). This delay is sufficient for the transient to disappear before corrective action is taken.

When a non-time indicating number transiently appears due to a code overlap, i.e. when the counters are being sequentially presented to the output display, the sequencing strobe itself is gated into the gate means to provide a half cycle delay before such a forbidden number can be responded to for correction by the gate circuit. The sequencing strobe, like the 60 Hz signal, is synchronized with the changes in the clock causing the transiently appearing improper codes, so that when these signals are applied in blocking phase relation to the transients they will inhibit response by the gate circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and objects of the present invention as well as a more complete understanding will be obtained from the following detailed description of the invention made with reference to the drawings, in which

FIG. 1 presents a logic diagram of one embodiment of the non-time indicating number correction circuit and a block diagram of the time counter, alarm counter and related portions of a digital clock;

FIG. 2 is a timing diagram showing the relationship between the 60 Hz delay signal and the application of the high frequency strobe to the counter; and

FIG. 3 is a timing diagram showing the relationship between the high frequency strobe and a corrective signal being applied to the counter.

DETAILED DESCRIPTION

In FIG. 1 the portions of the digital clock circuit of the above-mentioned commonly assigned application Ser. No. 25,930 bear the same reference numerals to be found in that application. FIG. 1 shows a time counter made up of a minute counter **27**, a 10 minute counter **59** and an hour counter **77**; an alarm counter made up of a 10 minute counter **33** and an hour counter **113**. Each of these counters is connected to a switch matrix **53** where the information from the counters are sequentially applied to a display device. Note, for example, the connection of counter **27** to matrix **53** is via lines **45**, **47**, **49** and **51**. A strobe signal from a source not shown is applied via line **135**, strobe counter **137**, leads **139** and **141** and strobe decoder **143** to switch matrix **53** to cause the sequential application of information from the counters to a display device. The display device, although not shown, receives the indication of each counter in sequence via lines **159**, **161**, **163** and **165**, the decimal decoder indicated in FIG. 1 and, for example, a 7 bar decoder (shown in FIG. 1 of the above-mentioned application).

It should be noted that NOR gate logic is used throughout the description. The NOR gate responds to any 1 input to produce a 0 output and to an all 0 input to produce a 1 output. With a two input NOR gate, if one input is always 0, the output is an inversion of any binary data stream applied to the other input. Thus when a constant 1 is applied to one input, the NOR gate will block binary data on the other input.

The digital clock gate circuit **15** is also shown in FIG. 1. This gate circuit is substantially identical to the gate circuit shown in FIG. 3 of the above-mentioned application, with the exception that NOR gate **216** has replaced inverting amplifier **303**. Gate **15** serves to direct 1 pulse per minute to the clock minute counter during "normal operation," 2 pulses per second during slow set operation, 60 pulses per second during fast set operation, and with the addition of NOR gate **216**, 3.3 K pulses per second during counter correction operation to either the clock minute counter **27** or the alarm 10 minute counter **33**. Although described in greater detail in the above-cited application, briefly gate **15** accomplishes this function as follows. The input **29** to gate **15** controls whether the output of the gate is directed to the clock counter or to the alarm counter. Thus the application of a 1 to NOR gate **311** on line **29** produces a 0 output from NOR gate **311** while inverter **313** changes the 1 to a 0 input for gate **309** and any time-set information from NOR gate **307** is passed by gate **309**. If a 0 is presented to gate **311** by line **29**, the output of gate **307** is passed by gate **311** and the 1 presented to gate **309** prevents this gate from passing the information from gate **307**. Thus NOR gates **309**, **311** and inverter **313** provide a data stream switch to control whether the time counter or the alarm counter receives time-set strobing from either the 60 Hz source applied to gate **305** or the 2 pulse per second source applied to gate **301**.

During normal operation, a 1 appears on line **29** to establish a clock display condition. At this time, a 0 and a 1 are applied to NOR gate **301** via lines **17** and **19** respectively. The 1 on line **19** insures that gate **301** has a 0 output. The 0 on line **17**

permits gate **216** to pass high frequency correction pulses from NOR gate **215** of the non-time indicating number impossible time correction circuit **210**. In the absence of an output from NOR gate **215**, the 0 applied from lead **17** to NOR gate **216** will be inverted and appear as a 1 at the output thereof to insure that the 60 Hz pulse input on lead **21** will not pass gate **305**. Thus, the 1 pulse per minute applied to gate **315** on lead **13** is the only input to the clock time counter. Since during normal operation the two inputs to gate **307** are 0, the output of this gate is a 1, causing gate **309** to be 0 so that the 1 pulse per minute applied to gate **315** and inverted thereby is again inverted by inverter **317** and applied to the time clock minute counter **27**.

During slow set operation, the 1 on line **19** becomes 0, permitting the two pulse per second input on line **23** to pass gate **301**. The 0 output from gate **305** remains, permitting the two per second pulses at the input of gate **307** to pass to gate **309** and be applied to gate **315**. Since the input at gate **315** is 0 except for the 1 pulse per minute, the two per second pulses are passed, inverted, again inverted by inverter **317** and applied to the clock minute counter.

During fast set operation, the input on line **17** becomes 1, which is inverted by NOR gate **216** to appear as a permitting 0 at gate **305**, allowing the 60 Hz pulses to be applied to gate **307**. The other input to this gate is a 0 due to the inversion by gate **301** of its 1 input on line **17**.

It can be seen that only during fast set, when a 1 appears on line **17**, the correction afforded by the non-time indicating number gate circuit **210** cannot be received by gate circuit **15** due to the 1 appearing at the second input to gate **216**. This is appropriate because during the time of fast set, the clock indication is being corrected to a desired time.

FIG. **1** also shows that the output of the time and alarm counters, as sequentially strobed to the output lines of switch matrix **53** by the decoded strobe signal, is applied to the non-time indicating number correction circuit **210**, comprised of NOR gates **211**, **212**, **213**, **214** and **215**. Gates **211**, **212** and **213** respond to all the non-time indicating counts of time counters **27**, **59** and **77** or alarm counters **33** and **113**.

It will be recognized that minute counter **27** is a modulo **10** counter, ten minute counter **59** is a modulo **6** counter and hour counter **77** is a modulo **12** counter. Accordingly, four flip-flops make up minute counter **27**, three flip-flops make up 10 minute counter **59** and four flip-flops make up hour counter **77**. Alarm 10 minute counter **33** is made up of three flip-flops and alarm hour counter **113** is made up of four flip-flops. Thus, it can be seen that each of the counters can assume non-time indicating numbers. For example, as indicated in Table I, the four flip-flops in the hours counter can assume various states when power is first applied or after power has been interrupted so that the numbers **12**, **13**, **14** or **15** could be generated; the four flip-flop modulo 10 minute counter can assume codes from **10** through **15**, all non-time indicating numbers; and Table I, shows that the three flip-flop modulo **6** 10 minute counter can assume the non-time indicating numbers **6** and **7**.

TABLE I

Counter number						
Decimal	Binary					
	1	2	4	8		
0	0	0	0	0		
1	1	0	0	0		
2	0	1	0	0		
3	1	1	0	0		
4	0	0	1	0		
5	1	0	1	0		
6	0	1	1	0	Forbidden ten minute codes (A=1, B=0).	
7	1	1	1	0		
8	0	0	0	1		
9	1	0	0	1		
10	0	1	0	1		
11	1	1	0	1		
12	0	0	1	1	Forbidden hour codes (B=1, A=0); (these codes are forbidden for all counters).	Forbidden minute codes (A=0, B=0).
13	1	0	1	1		
14	0	1	1	1		
15	1	1	1	1		

By reference to Table I, which indicates all the non-time indicating numbers which the digital clock counters can assume, the inputs to gates **211**, **212**, and **213** will be recognized. NOR gate **211** responds to those forbidden codes which are forbidden anytime, i.e. regardless of which counter is having its output presented to the display device via lines **159**, **161**, **163** and **165**. Thus, if a 1 appears in the **4** column and in the **8** column, which would indicate numbers **12** or greater, such a number would be improper for any counter. NOR gate **211** is accordingly responsive to $\overline{4}$ and $\overline{8}$, the 4 and 8 outputs on leads **163** and **165** respectively as inverted by inverters **218** and **219**. When $\overline{4}$ and $\overline{8}$ are both 0, gate **211** produces a 1 at its output so that the gate **214** output is 0 and NOR gate **215** is thereby enabled to pass the high frequency correction pulses from the strobe source at line **135**.

Gate **212** is responsive to forbidden codes generated by the ten minute counters **59** or **33**. As indicated by Table I, a number **6** and a number **7** are both forbidden numbers which the three flip-flops of the 10 minute counters can assume. Thus, a 1 indication in both the binary 2 and the binary 4 output positions converted by inverters **217** and **218** to a 0 for $\overline{2}$ and $\overline{4}$ are inputs to NOR gate **212**. In addition, when the A output of strobe counter **137** (a three state counter producing a $A=0$, $B=0$ output for the minute counter readout; a $A=1$, $B=0$ output for the 10 minute counters readout; and a $A=0$, $B=1$ for the hour counters readout) is 1, the 10 minute counter information is present at the output of the switch matrix **53** and accordingly gate **212** responds to a 0 from the $\overline{A}$ output of strobe counter **137**. When $\overline{2}$, $\overline{4}$ and $\overline{A}$ are all 0, NOR gate **212** presents a 1 to NOR gate **214** so that this gate applies a 0 to enable gate **215** to pass the high frequency correcting signal to gate **15**.

NOR gate **213** responds to forbidden counts from the clock minute counter **27**. Table **1** shows that this modulo **10** four flip-flop counter can assume the binary states of the numbers **10** through **15**. Since NOR gate **211** responds to the forbidden numbers **12** through **15**, only the numbers **10** and **11** need be recognized by NOR gate **213**. The numbers **10** and **11** are both made up of a binary 2 and a binary 8. Thus, this NOR gate responds to $\overline{2}$ and $\overline{8}$ in the 0 state. When strobe counter **137** provides a $A=0$ output and a $B=0$ output to NOR gate **213** via inverters **221** and **220**, the minute counter **27** is being read out and ready for monitoring. Thus, NOR gate **213** provides a 1 to NOR gate **214** when A and B and $\overline{2}$ and $\overline{8}$ are all 0 so that the high frequency strobe is applied to gate **15**.

Those skilled in the art will recognize that NOR gates **211**, **212**, **213** and **214** contain no deliberate delay producing components and will respond almost instantly to any improper time indication presented by the switch matrix **53**. Accordingly, non-time indicating numbers which transiently appear will be needlessly detected by these gates.

One source of transiently appearing non-time indicating is derived from the counters themselves. When the states of the flip-flops change, an forbidden code may momentarily be present. To prevent the non-time indicating number correction circuit from responding to such transients, a delay is included in the correction path by adding the 60 Hz signal to NOR gate **305** in gate circuit **15**. Reference is made to FIG. **2** for illustration of the delay obtained by adding the 60 Hz signal.

FIG. **2** shows the shaped 60 Hz square wave as presented to NOR gate **305** on lead **21**, the high frequency strobe signal output from gate **215** (gate **216** merely acts as an inverter to the output of gate **215** when a 0 appears at its other input), and the resultant output from gate **305**. It will be recognized by reference to the above-identified application Serial No. 25, 930, that the very same 60 Hz signal serves as the clock signal for the time and alarm counters. These counters respond to the 60 Hz clock and the signals derived therefrom (2/sec and 1/min) only on the 0 to 1 transition. This is illustrated in FIG. **2** where it is noted that at time t_0 a 0 to 1 transition of the 60 Hz signal occurs and the output of NOR gate **215** indicates that the non-time indicating number correction circuit is responding to a non-time number by passing one pulse of the

strobe signal. Because NOR gate **305** is receiving a 1 input from the 60 Hz signal at this time, the transient correction does not pass gate **305**.

FIG. **2** also shows that when power is interrupted and reapplied between times t_2 and t_3 so that a nontransient non-time indicating number is generated by the counters, the high frequency strobe is passed by gate **215**. NOR gate **305**, however, responds to pass the high frequency strobe only when the 60 Hz signal is in the 0 state. Thus, between times t_3 and t_4 the high frequency signal is applied to correct the forbidden indication in, for example, the 10 minute counter where the faulty number was located, but there is no correction between times t_4 and t_5 when the 60 Hz signal is in the 1 state. Correction continues at time t_5, correction being completed between times t_5 and t_6.

The second source of transiently occurring forbidden numbers is the switch matrix **53**. As the matrix switches from reading one counter to reading another counter, one or more gates of the matrix may not switch fast enough and a code overlay can momentarily occur. FIG. **3** shows that the solution provided by the non-time indicating number correction circuit is to incorporate a second delay in the form of the high frequency strobe itself. It will be appreciated that the gating of the 60 Hz cycle into the correction data stream at NOR gate **305** does not provide correction for transients occurring in the switch matrix, since such transients can occur during the 0 state of the 60 Hz signal and thus correction information would be passed by gate **305**.

FIG. **3** shows, from top to bottom, the strobe signal as applied to gate **215**, the A output of strobe counter **137**, the B output of this counter and the output of NOR gates **214**, **215**, **216** and **305**. FIG. **3** is related to FIG. **2** by again showing correction of a continuing forbidden code in the ten minute counter. FIG. **3** provides an exploded view of the signals passed by the gates in the t_5, t_6 time period of FIG. **2**.

Since NOR gate **212** responds to a forbidden 10 minute count, the A output of the strobe counter **137** is presented in FIG. **3**. The B output of this counter is also presented to indicate the generation of a transient non-time indicating number by switch matrix **53**.

The output of NOR gate **214** is an inversion of the output of gate **212**. When inputs $\overline{A}$, $\overline{2}$ and $\overline{4}$ are in the 0 state to produce a 1 at the output of gate **212**, gate **214** is accordingly in the 0 state. This occurs during the 10 minute state of strobe counter **137**, as indicated in FIG. **3** by the letter T directly beneath the strobe signal illustration. During the next cycle, counter **137** is in the hour counter read state as indicated by H and the output of NOR gate **214** has dropped to the 1 state. During this time there is a transition in the switch matrix between reading the hour counter and the minute counter as indicated by the **B** output of counter **137** and a forbidden count is shown transiently occurring at the output of gate **214**. Here again, it should be recognized that strobe counter **137** and thus switch matrix **53** changes states in response to the 0 to 1 transition of the strobe so that a forbidden code can be generated only at this transition. Thus, it is readily seen that the next half cycle of the strobe after the transient forbidden code is produced is a 1 state half cycle so that the output of gate **215** is 0 and the transient correction pulse present at the output of gate **214** does not pass.

FIG. **3** also shows the correction pulses for correcting the illegal count in the ten minute counter passing gates **215**, **216**, and **305**. It is seen that during the third readout of the 10 minute counter (indicated by the third T) a legal count is recognized and the pulse of strobe signal is cut short upon recognition of a legal number by gate **212**.

It is noted that gates **211**, **212**, and **213** of the non-time indicating number correction circuit **210** provide an AND function with input inversion, and that gate **214** provides an OR function plus output inversion.

A substitute for the NOR logic employed is AND gates to replace NOR gates **211**, **212** and **213** and to eliminate inverters **217**, **218** and **219**. NOR gate **214** could be replaced by an OR gate and an inverter. The AND gate replacing NOR gate **211** would respond to counter **4** and **8** information; the AND gate replacing NOR gate **212** would respond to A, 2 and 4 inputs; and the NOR gate **213** replacement would respond to $\overline{A}$, $\overline{B}$, 2 and 8 inputs. Those skilled in the art will recognize many other combinations of logic circuits to provide the correction function described.

It should also be recognized that while particular signals were selected to provide the delays to avoid correction for transiently occurring non-time indicating numbers, the only requirements are that the signal selected to provide the delay be synchronized with the source creating the transients and that the signals be applied through inverters if necessary to insure blockage of corrective response to the transient during the half cycle in which it occurs.

If the counters are not sequentially read out, but instead, continuously applied to display devices, the switch matrix is eliminated as a source of transient forbidden counts and the 60 Hz signal may be used for count correction as well as for delay. In this case, separate detectors would be needed for each counter, but the outputs of all such detectors could be summed together for presentation to the non-time indicating number correction circuit.

What is claimed and desired to be secured by Letters Patent of the United States is:

1. In a digital clock having a time counter, a non-time indicating number correction circuit comprising

a signal source,

said signal source having a repetition rate that is high compared to the normal time change rate of said counter, and

gate means responsive to counter non-time indicating numbers to apply said signal source to advance said counter to a time indicating number.

2. A correction circuit as recited in claim **1** wherein said gate means includes delay means to delay the application of said signal source to advance said counter to avoid response to transient occurrence of non-time indicating numbers.

3. A correction circuit as recited in claim **2** wherein said delay means includes a signal source synchronized with counter changes producing said transients and applied to said gate means in blocking phase relation to the transients, whereby a non-time indicating number must endure for more than one half cycle of the synchronized signal source to be corrected.

4. A correction circuit as recited in claim **3** wherein the signal source applied as a correction strobe to advance said counter and the delay signal source are the same.

5. A correction circuit as recited in claim **2** wherein said time counter includes a minute counter, a ten minute counter and an hour counter sequentially switched to a display such that non-time indicating numbers may transiently appear at the count transition of the counters and with the sequential readout switching of the counters,

said delay means includes a signal source synchronized with count transitions of the counters,

the delaying signal being combined with the correction strobe signal in blocking phase relating to count transition transients, and

said correction strobe signal being synchronized with counter readout switching and applied to said gate means in blocking phase relating to readout switching transients, whereby said gate means will not respond to a non-time indicating number transiently occurring at a count transition for one half cycle of said delaying signal and one half cycle of said strobe signal after occurrence of a non-time indicating number due to counter readout switching.

6. A correction circuit as recited in claim **1** wherein said digital clock further includes an alarm counter and switch means to permit display of the alarm time indication, said correction circuit being responsive to alarm counter non-time indicating numbers for correction thereof when said switch means is in the alarm display position.

* * * * *