



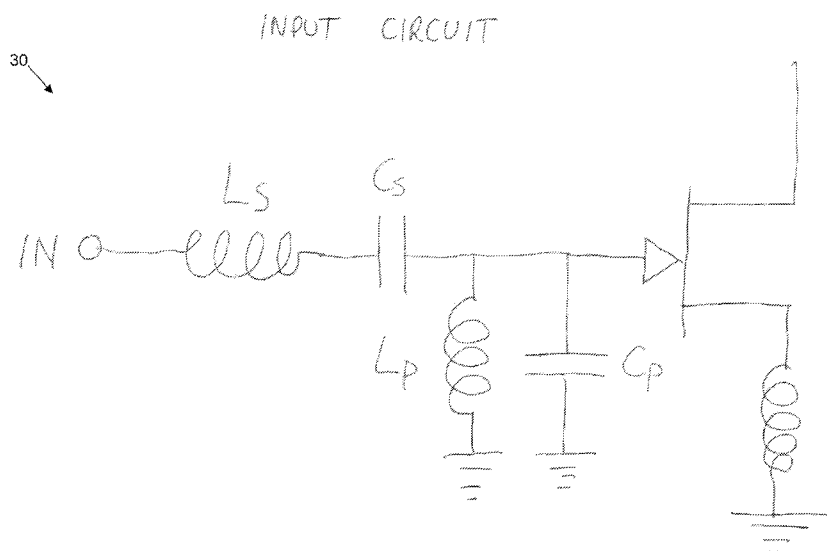
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(54) **Title:** LOW NOISE AMPLIFIER METHOD AND APPARATUS**FIG. 3**

(57) **Abstract:** A low noise amplifier circuit including: at least a first input and first output; at least a first stage of transistor amplification having a transistor input terminal; the circuit further comprising: an input driving circuit interconnecting the first input to the transistor input terminal, the input driving circuit including a parallel resonant circuit interconnected between the transistor input terminal and ground and a series resonant circuit interconnecting between the input terminal and the transistor input terminal, the input driving circuit functioning as an input matching network for the circuit in conjunction with an input bias and decoupling network.



Low Noise Amplifier Method and Apparatus

FIELD OF THE INVENTION

[0001] The present invention relates to the field of low noise amplifiers, and in particular, discloses a wide bandwidth low noise amplifier suitable for use in a non-cryogenic environment. Additionally, the present invention has particular suitability for utilisation in self complementary phased array feeds utilised in radio astronomy.

BACKGROUND

[0002] Any discussion of the background art throughout the specification should in no way be considered as an admission that such art is widely known or forms part of common general knowledge in the field.

[0003] Applications of low-noise amplifiers are many and varied. However, one particular application is for the amplification of weak detected signals in radio astronomy or sensing.

[0004] Low-noise amplifiers are generally designed for a nominal system impedance of a certain value over at least the bandwidth of operation. This impedance is normally independent of frequency. Often it is 50 ohms, and sometimes 75 ohms. This state of affairs comes about for two reasons, firstly, that measurement equipment operates at 50 ohm impedance; and secondly, that the feed to which the low-noise amplifier's input connects is normally designed for a 50 ohm impedance. Normally, an antenna feed and the low-noise amplifier are both optimised to present to one other an impedance as close to 50 ohms as possible. This is done for ease of design and ease of measurement, since both components need to be compatible with measurement equipment. Of course, other standard values could be chosen.

[0005] The standardisation of choice on a 50 ohm system impedance also normally dictates the use of coaxial transmission lines at the amplifier's input and output ports. A coaxial transmission line features a signal conductor and a ground conductor, and by its nature requires an amplifier connected to it to be single-ended, meaning it has one (non-ground) input conductor and one non-ground output conductor.

[0006] In the state of the art, provision is usually made for matching networks between the amplifier's input port and the amplifying transistor's input on the one hand, and the amplifier's output port and the amplifying transistor's output on the other hand. The input matching network is designed for best compromise between impedance match and noise match, while the output matching network is generally optimised for impedance match. Again, these networks are designed to match the transistors utilised to a system impedance of 50 ohms over the intended frequency band.

[0007] In contrast to the single-ended amplifier, a differential amplifier has two non-ground input conductors, driven out of phase. A differential amplifier may also have two output conductors, with a 180-degree phase relationship between them. Differential low-noise amplifiers are in the state of the art, but are considerably less employed than their single-ended counterparts, because they require connection to a balanced feed structure. A complementary antenna structure, such as a chequerboard phased-array feed is one such structure.

[0008] An example of one such self complementary array taking a chequerboard array structure is disclosed in PCT Application Number PCT/AU2011/000862, entitled: "Reconfigurable Self Complementary Array", the contents of which are hereby incorporated by cross reference.

[0009] A single-ended, 50-ohm low-noise amplifier cannot successfully be employed as the receiving element for a chequerboard phased-array feed. The amplifier's input impedance is too low, and the amplifier needs to have a differential input. The chequerboard phased-array feed's "natural" impedance is much higher, of the order of 377 ohms, the characteristic impedance of free space. It may be theoretically possible to interpose a balun (short for balanced-to-unbalanced transformer) between a balanced feed and an unbalanced low-noise amplifier, but the inevitable loss of the balun adds directly to the noise temperature of the low-noise amplifier, rendering this approach unworkable.

[0010] Furthermore, the optimum noise match impedance of a chequerboard phased-array feed is not purely resistive, but has a reactive (capacitive or inductive) component, and this impedance (a complex quantity) varies as a function of frequency. A low-noise amplifier optimised for use in a chequerboard phased-array feed requires a differential

input, high differential-mode input impedance, low common-mode input impedance, and optimum wide-band noise match to a complex, frequency-variable optimum source impedance. Such an amplifier has not previously been realised.

SUMMARY OF THE INVENTION

[0011] It is an object of the invention, in its preferred form to provide an improved form of low noise amplifier.

[0012] In accordance with a first aspect of the present invention, there is provided a low noise amplifier circuit including: at least a first input and first output; at least a first stage of transistor amplification having a transistor input terminal; the circuit further comprising: an input driving circuit interconnecting the first input to the transistor input terminal, the input driving circuit including a parallel resonant circuit interconnected between the transistor input terminal and ground and a series resonant circuit interconnected between the input terminal and the transistor input terminal, the input driving circuit functioning as an input matching network for the circuit in conjunction with an input bias and decoupling network.

[0013] In some embodiments the resonant circuits are preferably provided by inductive and capacitive components. In some arrangements the capacitive components are preferably formed by package and inter-electrode parasitic capacitances.

[0014] In some embodiments, the inductive component of the series resonant circuit can be large and the capacitive component of the series resonant circuit can be small. The inductive component of the series resonant circuit can be above about 14 nH. The inductive component of the parallel resonant circuit can be in the range of 22 to 27 nH.

[0015] The low noise amplifier circuit preferably can include at least a first and second stage of transistor amplification.

[0016] In some arrangements, the low noise amplifier circuit can be utilised in at least one input to a differential amplifier. In other arrangements, the low noise amplifier circuit can be used in single ended amplifiers.

[0017] In accordance with another aspect of the present invention, there is provided a differential mode low noise amplifier including: a first and second single-ended amplifier circuit, said single ended amplifiers circuit performing the amplification of a differential input signal by a multistage to produce a differential output signal, and a second order band pass filter network interconnected to the input of the multistage transistor network; and a combining circuit for combining the differential output signals.

[0018] In accordance with a another aspect of the invention, there is provided a differential mode low noise amplifier formed on a printed circuit board (PCB), the PCB including a conductive ground plane substantially covering the PCB, the ground plane having a series of apertures therein; the amplifier including a series of input feeds which can be located centrally on the PCB, with the input feeds being interconnected to the PCB within the apertures located in the ground plane.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

[0020] Fig. 1 illustrates schematically a differential mode low noise amplifier;

[0021] Fig. 2 is a circuit drawing of the half-LNA component of the arrangement of Fig. 1;

[0022] Fig. 3 illustrates schematically the portions of the simplified input circuit of the half-LNA of the first embodiment;

[0023] Fig. 4 illustrates a PCB layout of a pair of differential mode low noise amplifier;

[0024] Fig. 5 illustrates the arrangement of Fig. 4 with assembled components;

[0025] Fig. 6 illustrates the radiofrequency portion of the circuit of a differential mode low noise amplifier; and

[0026] Fig. 7 illustrates the bias supply portion of the circuit of a differential mode low noise amplifier;

DETAILED DESCRIPTION

[0027] The first embodiment provides a differential-input low-noise amplifier of high differential-mode input impedance and moderate common-mode input impedance. The input impedance and optimum noise match impedance are, in the first embodiment, both optimised for the output impedance and optimum noise match impedance which a chequerboard phased-array feed presents it. These features allow the invention to overcome the incompatibility of a single-ended, 50-ohm low-noise amplifier with a chequerboard phased-array feed.

[0028] The embodiments provide an advantageous differential single-ended structure, featuring wideband noise and impedance matching to a planar connected array; the optimization of the differential- and common-mode input impedances for operation with a planar connected array. The arrangement is provided in a stably operating low noise amplifier (LNA).

[0029] The operational environment for the low noise amplifier is illustrated 10 in Fig. 1. As the amplifier operates in a differential manner, a differential input 13 is received from the feed array. Each arm is subjected to separate amplification by half-LNA amplifiers 11, 12, before being combined 14 and equalised 15. The combiner and equaliser can be of standard construction.

[0030] Fig. 2 illustrates a simplified circuit diagram of one of the half-LNAs 20. The half-LNA is a two-stage common-source amplifier having stages 21, 22. The transistors Q1, Q2 used are the Avago ATF-35143. Other transistors may offer improved performance after evaluation. The two stages 21, 22 are capacitively coupled via capacitors C1, C2 and C3, forming the main signal path. The transistor gates are biased via inductors L2 and L4. The drain loads of the transistors are composed by networks R1-C4-L3 and R2-C5-L5 respectively. The source terminals of the transistors are connected to ground through inductors L6 and L7.

[0031] In the first embodiment, the input matching components are absorbed into the input bias and decoupling networks. Wideband low-noise performance results when the input circuit to the first stage transistor Q1 is in the form of a second-order bandpass matching network. Turning to Fig. 3, there is illustrated one such network 30, where a

parallel-resonant L-C circuit (L_p and C_p) is connected between the input transistor's gate and ground, and a series L-C circuit (L_s and C_s) is connected between the amplifier's input terminal and the transistor's gate. Inter-electrode and parasitic capacitances account for C_p , the gate bias inductor L_2 of Fig. 2 accounts for L_p . The input coupling capacitor C_1 of Fig. 2 accounts for C_s . The series inductor L_1 of Fig. 2 accounts for L_s .

[0032] It should be noted that such a matching technique is also applicable to single-ended low-noise amplifiers.

[0033] Returning to Fig. 2, a wideband impedance match also results from the use of this second-order bandpass matching network at the LNA's input. To obtain a high input impedance, L_2 has to be small. The lower L_2 , the higher the input impedance, although at the expense of minimum noise figure. 22 to 27 nH is suitable.

[0034] L_1 and C_1 form part of the input matching network to the LNA. Normal practice is for L_1 to be small and C_1 to be large. In the first embodiment, L_1 is large, and C_1 small, so as to produce a large "reactance slope parameter". Optimum value for L_1 is physically unrealizable: around 28 nH. State of the art values are 14 nH for L_1 and 1.5 pF for C_1 . As C_1 is reduced and L_1 increased in value, the passband shifts downwards in frequency and the minimum noise figure is reduced. A sharp gain peak appears at the bottom of the passband if L_1 and C_1 are pushed past optimum values. This effect is used to advantage to define a sharp, flat-topped lower band edge.

[0035] The drain loads are a 100 ohm resistor (R_1 and R_2 respectively) in series with an inductor (L_3 and L_5 respectively), and a small shunt capacitance to ground (C_4 and C_5 respectively). The main component of the drain load is the resistor. Inductors L_3 and L_5 may be thought of as providing inductive peaking to define and sharpen the passband shape. They are 22 and 27 nH respectively.

[0036] It is difficult to make the LNA stable over a very wide frequency range. Stability may be achieved in the 5-15 GHz region, but at the expense of stability in the UHF band, just below the lower band edge. The LNA's input reflection coefficient can rise above one just below 500 MHz unless L_4 is as large as practical. 100 nH is typical. C_4

reduces the input reflection coefficient magnitude below-band, at the expense of slightly reduced gain. 0.5 pF is the nominal value.

[0037] Inductive source degeneration of the transistors (via L6 and L7) is a known technique for improving the transistors impedance and noise match. . The technique must be applied with care, for if too much degeneration is applied, parasitic oscillations in the 5-15 GHz range result. These are caused by parasitic capacitance of the transistor's source leads and circuit board pad capacitance forming a parallel-resonant circuit at microwave frequencies. Source degeneration is not employed on Q2 (L7 is about 0.05 nH). Q1 has only a modest amount of source degeneration to avoid high-frequency parasitic oscillations (L6 is about 0.35 nH, and is embodied as a printed circuit board trace).

[0038] In the first embodiment, input capacitance has a deleterious effect. Parasitic capacitance affects performance. The higher the input capacitance, the higher the amplifier's noise figure, the lower the input impedance, and the higher the optimum noise match source impedance. The only good effect of input capacitance is to stabilise the amplifier. As the parasitic capacitance to ground is reduced, Q1 is more prone to high-frequency parasitic oscillations. It is then necessary to reduce Q1's source inductor L6 to stabilise Q1. The reduction in L6 then wipes out most of the improvement in noise figure, input impedance and optimum noise match source impedance resulting from the reduction in shunt capacitance.

[0039] In order to preserve good circuit performance in a high-impedance environment, special layout techniques can be utilised. Fig. 4 illustrates the PCB layout 40. The PCB ground plane is removed around the amplifier's inputs 42, 43 to minimise shunt capacitance. As discussed earlier, L1 is at the upper limit of physically realizable values. This limit is imposed by L1's self-resonant frequency, which decreases as the inductance increases. The self-resonant frequency is influenced strongly by stray capacitance. To keep stray capacitance to a minimum, L1 is situated above the ground-plane cutout 44 and oriented at 45 degrees to the signal flow. In this way connections to its terminals are located as far from each other as practical. The L1-C1 node is a series-resonant point, and is particularly sensitive to stray capacitance. The connection associated with this node is made as small as possible. The transistors Q1 and Q2 are also oriented at 45 degrees to the signal flow, as this orientation allows the shortest signal paths and dis-encumbers Q1's

source connections from the other circuit elements. In order for the differential-single-ended architecture to be applied successfully, the total width of a half-section LNA, when laid out on a circuit board, must be less than 10 mm, the feedwire spacing of the chequerboard array. The 45-degree orientation of the transistors allows this width constraint to be observed. To minimise shunt capacitance, particularly at Q1's gate, the bias inductors must be laid out so the signal path passes through the inductors' pad, instead of forming a short stub-line to connect to the bias inductors.

[0040] Fig. 5 illustrates the PCB with assembled components.

[0041] Returning to Fig. 1, the differential-single-ended amplifier structure 10 consists of two single-ended amplifiers 11, 12 operated in parallel, whose outputs are combined 14 in antiphase to produce an apparently differential input. The single-ended amplifiers' outputs may be combined by any standard technique, such as a push-pull output transformer, or a balun transformer, or a 180-degree hybrid combiner. The first embodiment is a balun transformer, for ease of application and compactness. Nonetheless a balun transformer suffers from imperfect isolation between the input ports. The output network of the LNA is never a perfect impedance match, and a small proportion of the output signal from one side of the LNA is reflected from the load back into the "other" side of the LNA, where it modifies the load impedance seen by the "other" side, which in turn causes the impedance seen at the "other" input to be perturbed. The net effect of this is to unbalance the inputs of the LNA. If the two input ports are labelled 1 and 3, from an S-parameter viewpoint the imperfect isolation between the amplifiers output causes the appearance of cross terms S_{31} and S_{13} at the amplifier's inputs. In the first embodiment, these cross terms add to the input terms S_{11} and S_{33} in such a way as to increase the differential-mode input impedance (desirable) and reduce the common-mode input impedance (undesirable, as it can result in resonant passband notches). The imperfect balance of the differential-single-ended LNA also causes energy transfer between the common-mode input signal and the output, which effectively reduces the common-mode rejection ratio. A 180-degree hybrid combiner may offer better isolation than a balun transformer, and may offer improved performance.

[0042] Finally, the combiner's output is connected to an equalizer circuit 15, the function of which is to flatten the amplifier's passband. The first embodiment of this

function is a single-section bridged-T bandpass filter, the centre frequency and bandwidth of which are chosen for best overall amplifier passband flatness.

[0043] The first embodiment provides a low noise amplifier optimised for the special requirements of a self complementary array such as the aforementioned chequerboard phased-array feed.

[0044] By way of further illustration, Fig. 6 illustrates the radiofrequency portion of the circuit design of a differential mode low noise amplifier.

[0045] By way of further illustration, Fig. 7 illustrates the bias supply portion of the circuit design of a differential mode low noise amplifier.

[0046] The embodiment also has other applications where low noise amplification is required. For example, low noise amplifiers have applications in medical imaging, security scanning, and other forms of sensitive scanning and detection technologies of very weak signals.

[0047] Other embodiments can be constructed. For example, where different transistors are used, they will have different operational characteristics which should be individually examined. Different transistors may have different minimum noise temperature. Ideally, the noise parameters of potentially suitable transistors should be separately measured and characterised. One form of suitable alternative transistor was found to be the ATF-38143. If a different transistor is used in the LNA, the component values required for optimum performance may vary. This is particularly the case for the input matching components.

Interpretation

[0048] Reference throughout this specification to “one embodiment”, “some embodiments” or “an embodiment” means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases “in one embodiment”, “in some embodiments” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in

any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

[0049] As used herein, unless otherwise specified the use of the ordinal adjectives "first", "second", "third", etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

[0050] In the claims below and the description herein, any one of the terms comprising, comprised of or which comprises is an open term that means including at least the elements/features that follow, but not excluding others. Thus, the term comprising, when used in the claims, should not be interpreted as being limitative to the means or elements or steps listed thereafter. For example, the scope of the expression a device comprising A and B should not be limited to devices consisting only of elements A and B. Any one of the terms including or which includes or that includes as used herein is also an open term that also means including at least the elements/features that follow the term, but not excluding others. Thus, including is synonymous with and means comprising.

[0051] As used herein, the term "exemplary" is used in the sense of providing examples, as opposed to indicating quality. That is, an "exemplary embodiment" is an embodiment provided as an example, as opposed to necessarily being an embodiment of exemplary quality.

[0052] It should be appreciated that in the above description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, FIG., or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the Detailed Description are hereby expressly incorporated into this Detailed Description, with each claim standing on its own as a separate embodiment of this invention.

[0053] Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those skilled in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

[0054] In the description provided herein, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

[0055] Similarly, it is to be noticed that the term coupled, when used in the claims, should not be interpreted as being limited to direct connections only. The terms "coupled" and "connected," along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Thus, the scope of the expression a device A coupled to a device B should not be limited to devices or systems wherein an output of device A is directly connected to an input of device B. It means that there exists a path between an output of A and an input of B which may be a path including other devices or means. "Coupled" may mean that two or more elements are either in direct physical or electrical contact, or that two or more elements are not in direct contact with each other but yet still co-operate or interact with each other, including in an electromagnetic coupling sense.

[0056] Thus, while there has been described what are believed to be the preferred embodiments of the invention, those skilled in the art will recognize that other and further modifications may be made thereto without departing from the spirit of the invention, and it is intended to claim all such changes and modifications as falling within the scope of the invention. For example, any formulas given above are merely representative of procedures that may be used. Functionality may be added or deleted from the block diagrams and operations may be interchanged among functional blocks. Steps may be added or deleted to methods described within the scope of the present invention.

CLAIMS:

1. A low noise amplifier circuit including:
at least a first input and first output;
at least a first stage of transistor amplification having a transistor input terminal;
the circuit further comprising:
an input driving circuit interconnecting the first input to the transistor input terminal, the input driving circuit including a parallel resonant circuit interconnected between the transistor input terminal and ground and a series resonant circuit interconnected between the input terminal and the transistor input terminal, the input driving circuit functioning as an input matching network for said circuit in conjunction with an input bias and decoupling network.
2. The low noise amplifier as claimed in claim 1 wherein the input driving circuit comprises a second order band pass filter.
3. The low noise amplifier circuit as claimed in claim 1 wherein said resonant circuits are provided by inductive and capacitive components.
4. The low noise amplifier circuit as claimed in claim 3 wherein the capacitive components of the resonant circuits comprise parasitic capacitances.
5. The low noise amplifier circuit as claimed in claim 4 wherein the inductive component of the series resonant circuit is large and the capacitive component of the series resonant circuit is small.
6. The low noise amplifier circuit as claimed in claim 5 wherein the inductive component of the series resonant circuit is above about 14 nH.
7. The low noise amplifier circuit as claimed in claim 3 wherein the inductive component of the parallel resonant circuit is in the range of 22 to 27 nH.
8. The low noise amplifier circuit as claimed in any previous claim wherein said circuit includes at least a first and second stage of transistor amplification.

9. The low noise amplifier circuit as claimed in any previous claim wherein said circuit is utilised in at least one input to a differential amplifier .

10. The low noise amplifier circuit as claimed in any previous claim wherein the inductive component of the series resonant circuit is spaced apart from any conductive ground plane so as to minimise parasitic capacitances.

11. A differential mode low noise amplifier including:

a first and second single-ended amplifier circuit, said single-ended amplifiers circuits performing the amplification of a differential input signal by a multistage transistor network to produce a differential output signal, and a second order band pass filter network interconnected to the input of the multistage transistor network; and a combining circuit for combining the differential output signals.

12. A differential mode low noise amplifier formed on a printed circuit board (PCB), the PCB including a conductive ground plane substantially covering the PCB, the ground plane having a series of apertures therein;

the amplifier including a series of input feeds located on the PCB, with the input feeds being interconnected to the PCB within the apertures located in the ground plane.

13. A differential mode low noise amplifier as claimed in claim 12 wherein the series of input feeds are located centrally on the PCB.

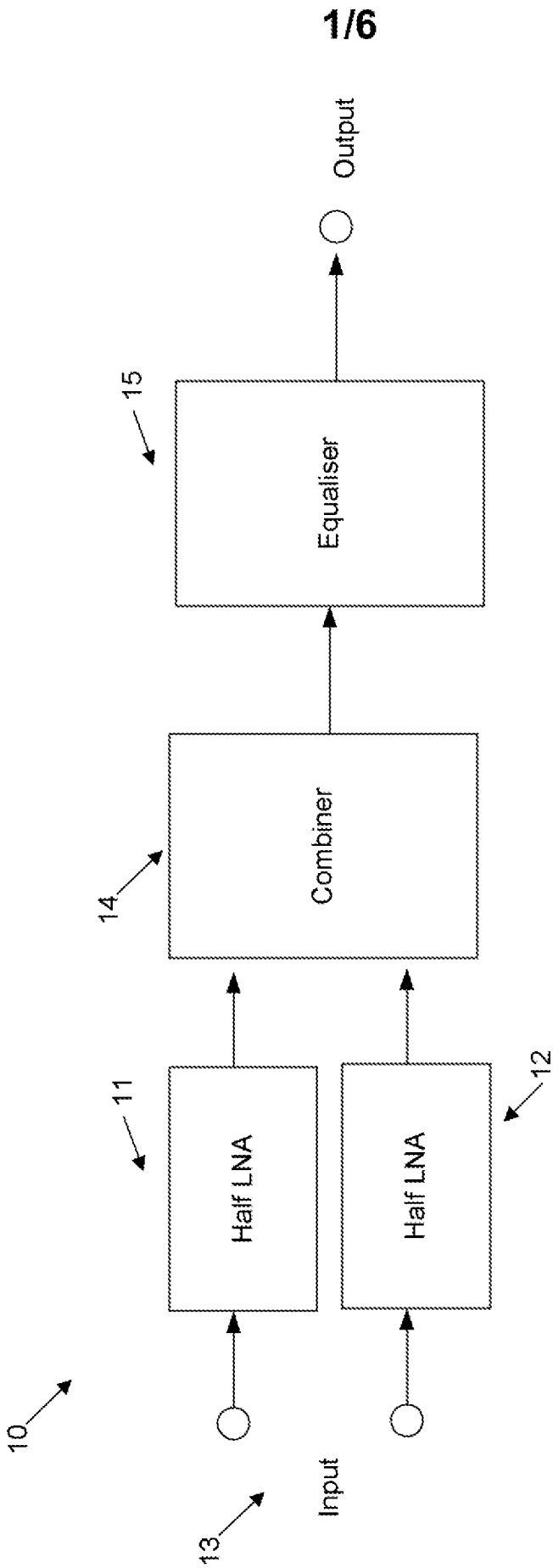


FIG. 1

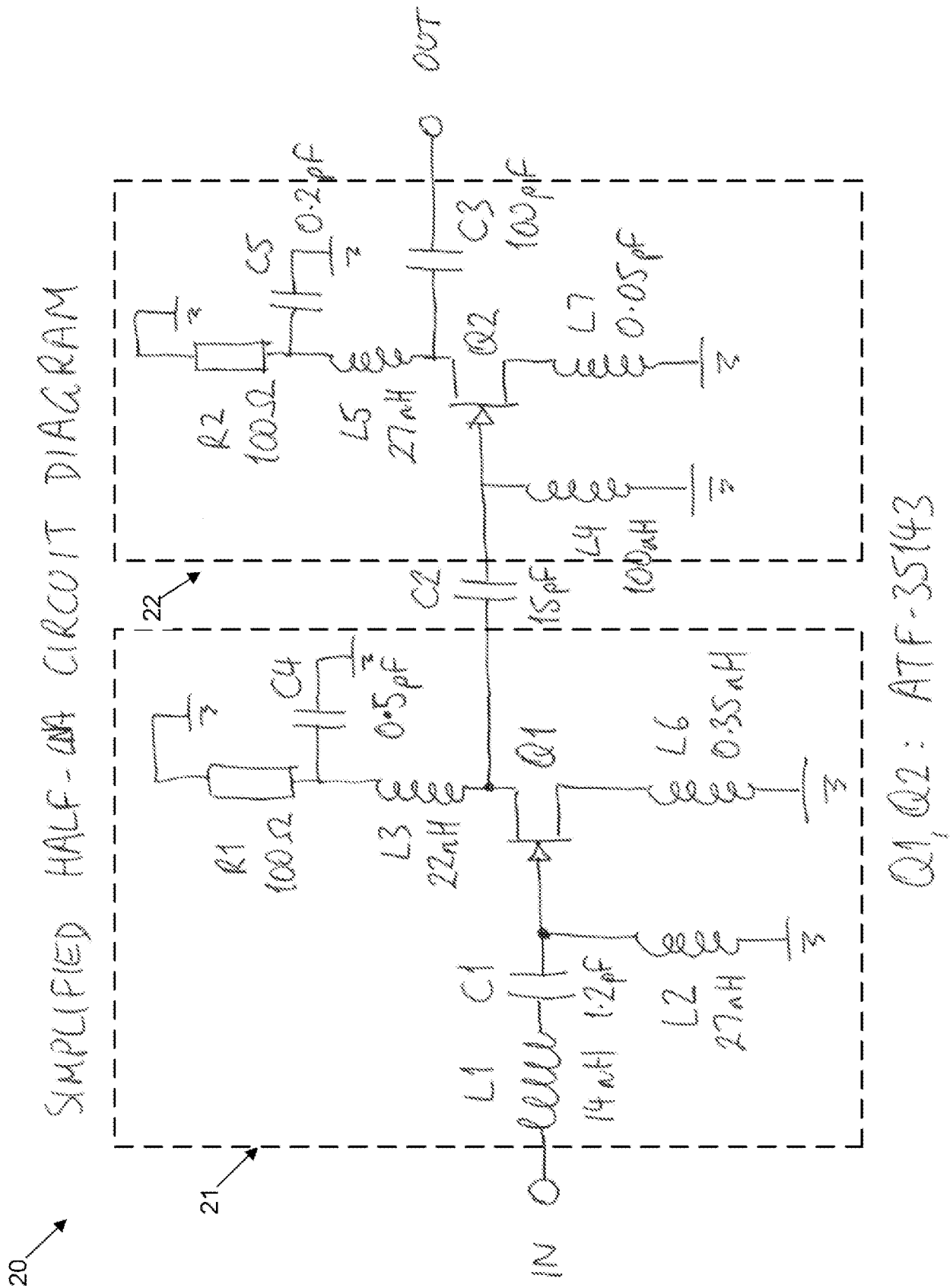


FIG. 2

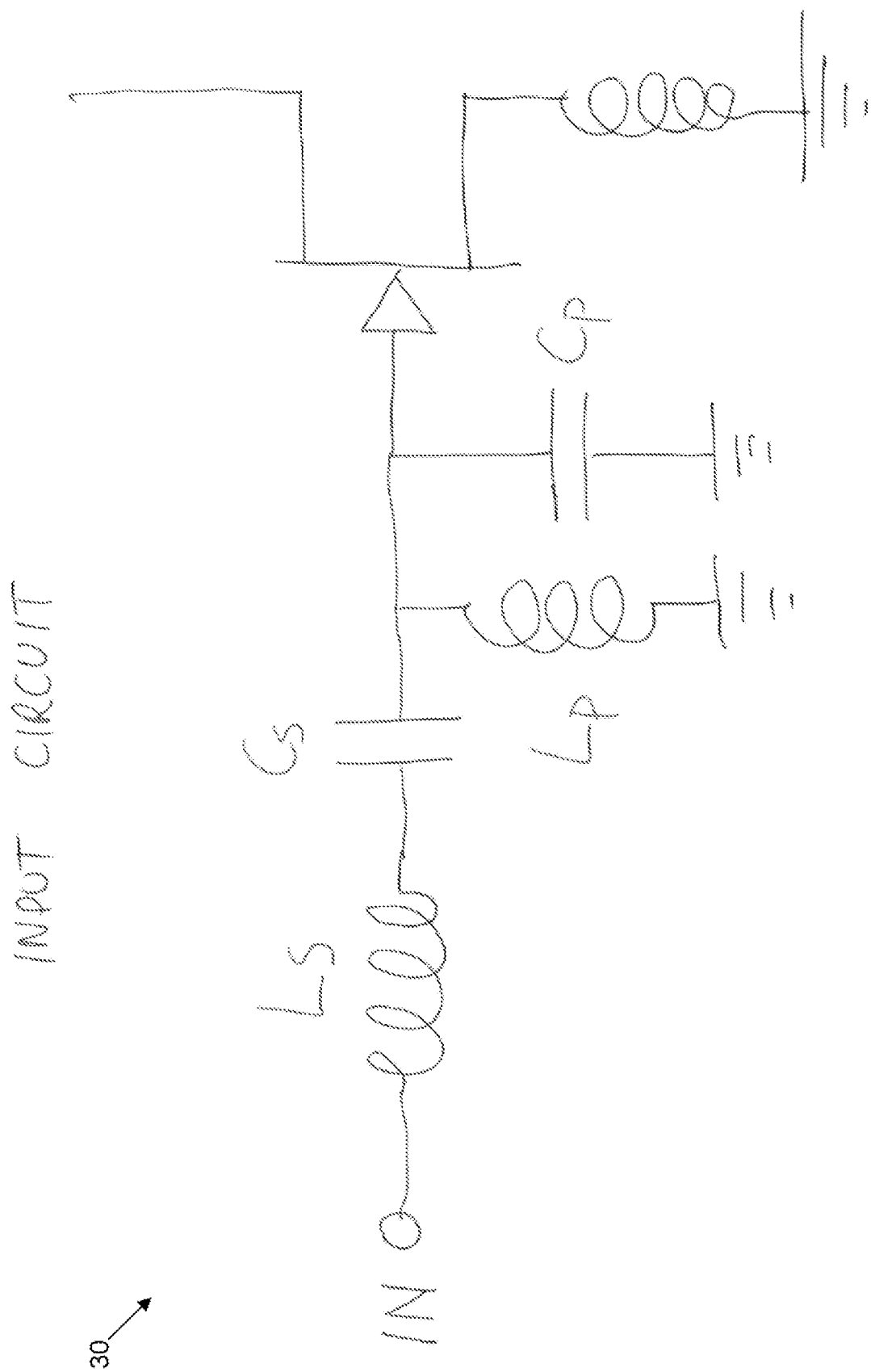


FIG. 3

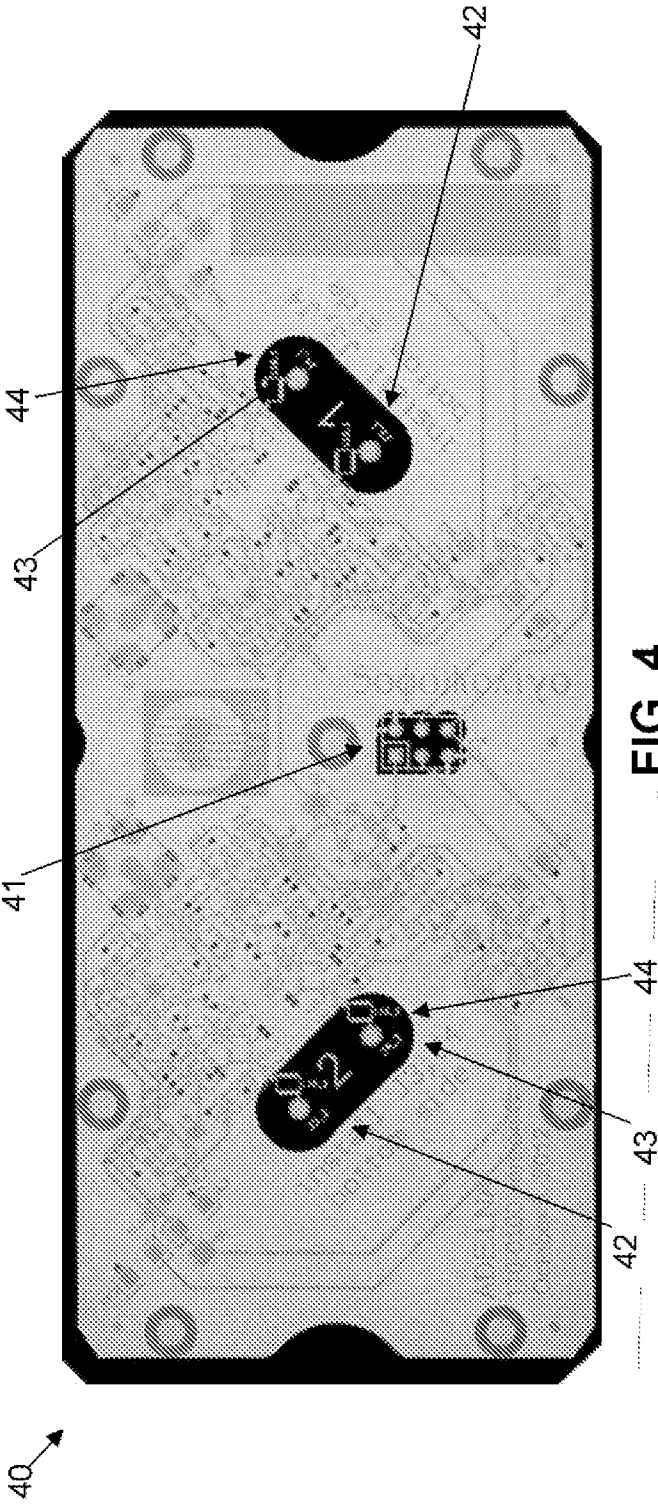


FIG. 4

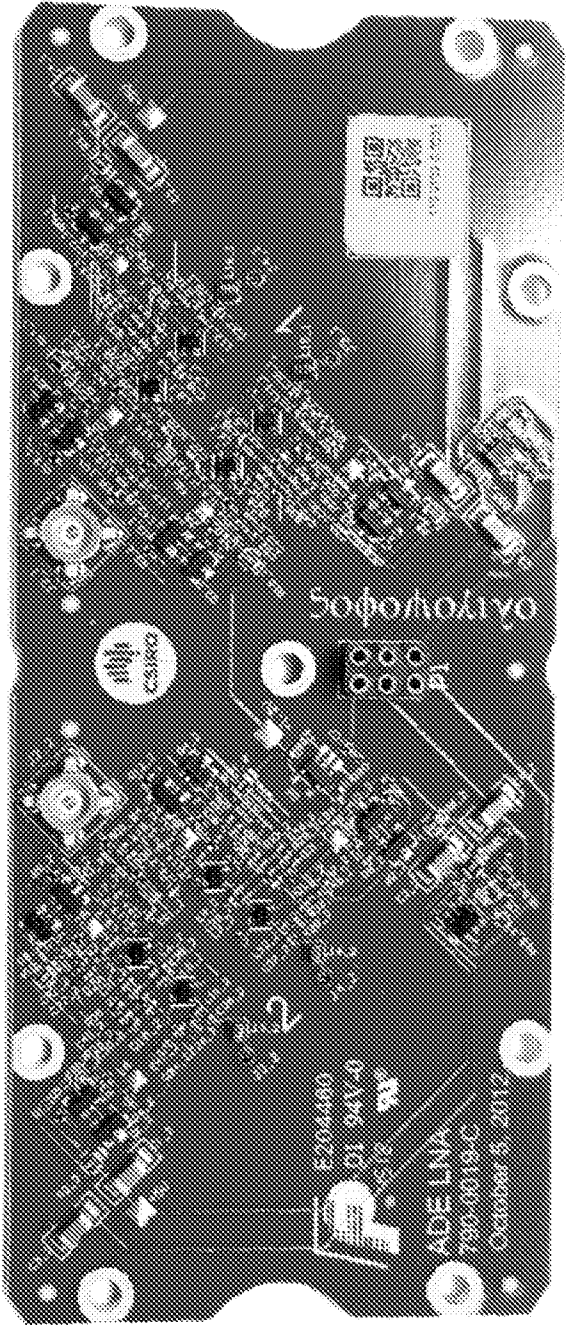


FIG. 5

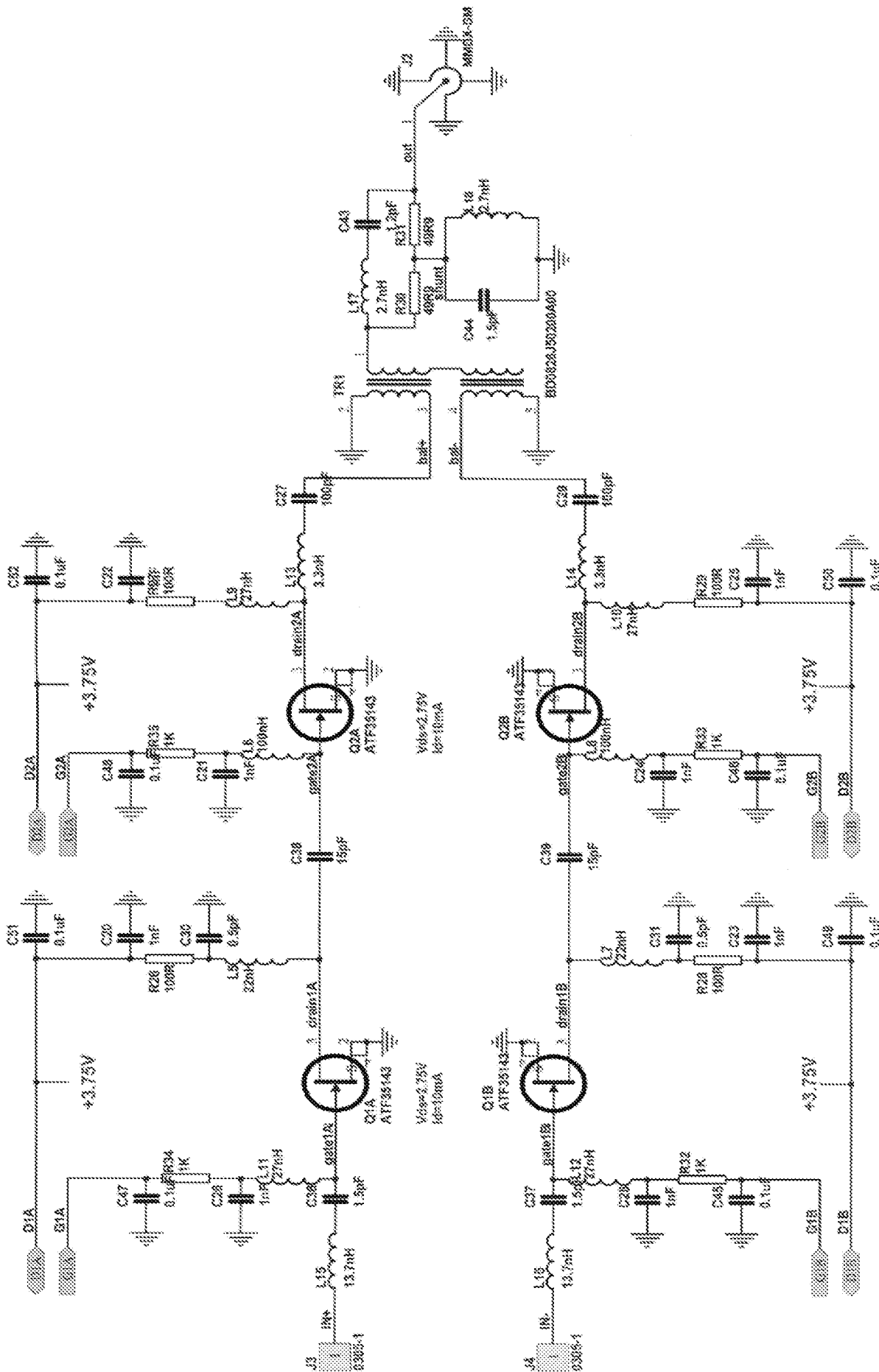


FIG. 6

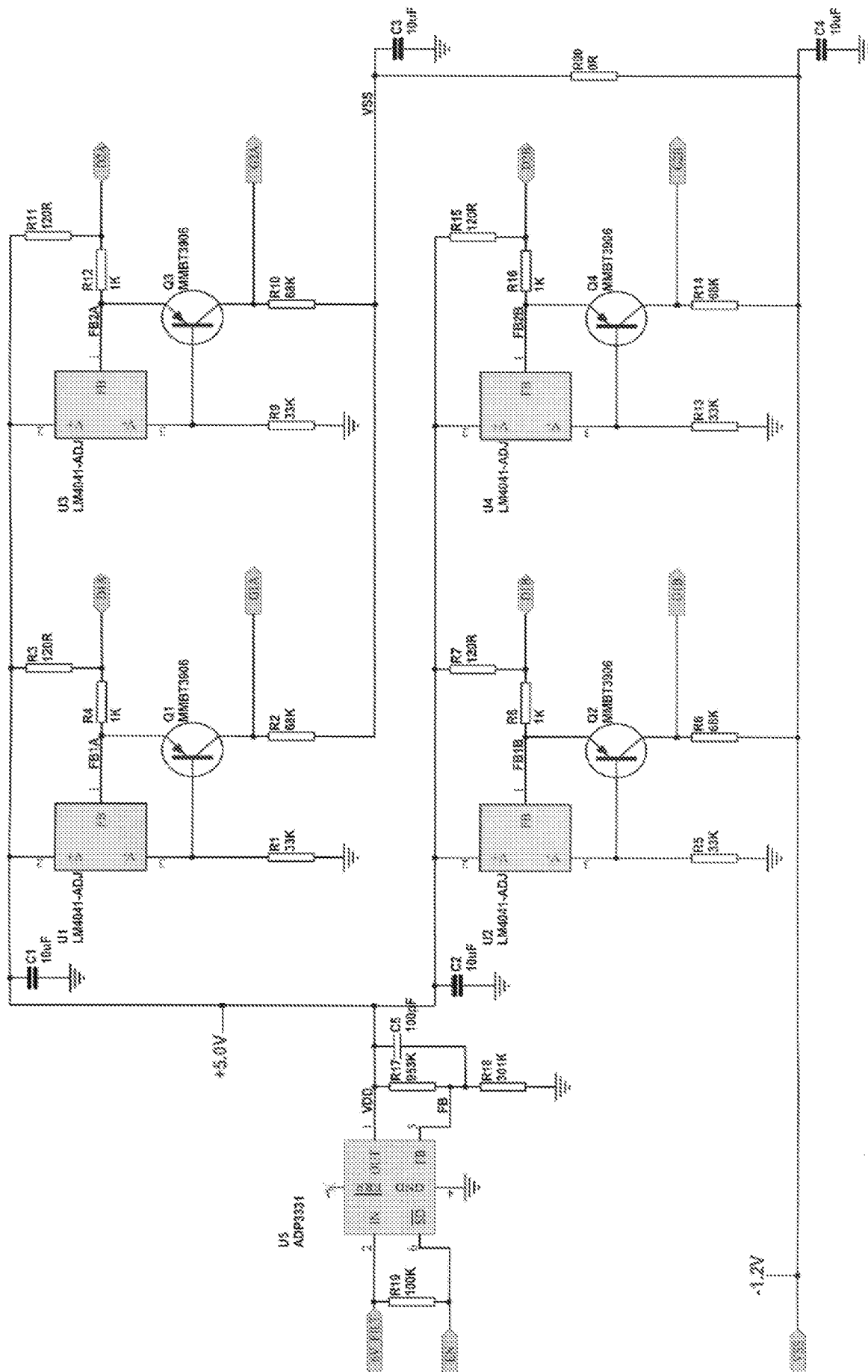


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2014/000484

A. CLASSIFICATION OF SUBJECT MATTER

H03F 1/26 (2006.01) H03F 3/45 (2006.01) H03F 3/181 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: EPODOC, WPI, INSPEC, GOOGLE and GOOGLE PATENTS: keywords (LNA, LC, Resonant, circuit, parallel, series, match) & like terms.

Databases: The LENS: Invention Title (LOW NOISE AMPLIFIER METHOD AND APPARATUS), applicant's name (COMMONWEALTH SCIENTIFIC AND INDUSTRIAL RESEARCH ORGANISATION) and inventor's Name (SHAW, Robert Douglas) searched.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search 21 July 2014		Date of mailing of the international search report 21 July 2014	
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaaustralia.gov.au		Authorised officer Nidhal Odeh AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. 0262832498	

INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		PCT/AU2014/000484
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GARCÍA-VÁZQUEZ et al. 'Flatness Improvement for a Shunt-peaked Ultra-wideband Low Noise Amplifier', Microwave Journal, Vol. 53, No. 11, pages 1-5. 10 November 2010. Abstract; Pages 1-3; Fig. 1.	1-10

Form PCT/ISA/210 (fifth sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.

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Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
the subject matter listed in Rule 39 on which, under Article 17(2)(a)(i), an international search is not required to be carried out, including
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See Supplemental Box for Details

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-10

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

Supplemental Box**Continuation of: Box III**

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

This Authority has found that there are different inventions based on the following features that separate the claims into distinct groups:

- Claims 1-10 define a low noise amplifier with an input driving circuit which include a parallel and series resonant circuits. The feature of input driving circuit which includes a parallel and series resonant circuits in the specific arrangements as defined in claim 1 is specific to this group of claims.
- Claim 11 defines a differential mode low noise amplifier which comprises a multistage transistor network and a band pass filter; and a combining circuit for combining the differential output signal. The feature of combining circuit for combining the differential output signal is specific to this group of claims.
- Claims 12-13 define a differential mode low noise amplifier formed on a printed circuit board having series of apertures, the amplifier including a series of feeds located on the PCB. The feature of printed circuit board (PCB) having series of apertures is specific to this group of claims.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

When there is no special technical feature common to all the claimed inventions there is no unity of invention.

In the above groups of claims, the identified features may have the potential to make a contribution over the prior art but are not common to all the claimed inventions and therefore cannot provide the required technical relationship. The only feature common to all of the claimed inventions and which provides a technical relationship among them is **Low Noise Amplifier (LNA)**

However it is considered that this feature is generic in this particular art. Therefore in this light this common feature cannot be a special technical feature. Hence there is no special technical feature common to all the claimed inventions and the requirements for unity of invention are consequently not satisfied *a priori*.

INTERNATIONAL SEARCH REPORT Information on patent family members		International application No. PCT/AU2014/000484	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
End of Annex			
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001. Form PCT/ISA/210 (Family Annex)(July 2009)			