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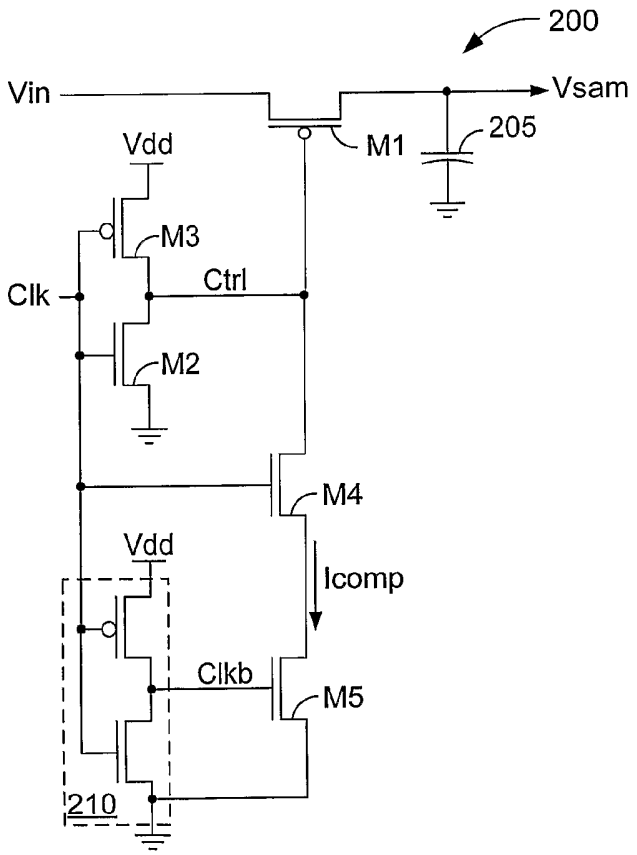
(54) Title: PASS TRANSISTORS WITH MINIMIZED CAPACITIVE LOADING



(57) Abstract: A tracking switch (100, 200) includes an MOS switching transistor (M1) with a control terminal coupled to a CMOS inverter. The relative geometries of the transistors that make up the inverter (M2, M3) are significantly imbalanced, resulting is substantially different drive strengths (i.e., substantially different on-resistances). The gate of the switching transistor (Ml) exhibits parasitic capacitances (Crs, Crd) between its current-handling terminals and its control terminal. When the switching transistor (Ml) is on, these capacitances (Crs, Crd) shunt a portion of the switched signal (Vin) to a power-supply node, with the problem increasing with the frequency of the propagated signal. The geometry of the transistor used to turn on the switching transistor (Ml) is selected to produce a high on-resistance, which introduces a high-impedance path from the control terminal of the switching transistor when the switch is closed. The high-impedance path isolates the control terminal of the switching transistor from the supply, thus mitigating the capacitive loading effects of the parasitic capacitances. The transistor used to turn off the switching transistor has a much lower on-resistance than the transistor used to bias the switching transistor on, preventing undesirable signal feed-through from occurring when the switching transistor is off.

WO 2006/050443 A1

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PASS TRANSISTORS WITH MINIMIZED CAPACITIVE LOADING

Ramin Farjad-rad

FIELD OF THE INVENTION

[0001] The present invention relates generally to the field of communications, and more particularly to high speed electronic signaling within and between integrated circuit devices.

BACKGROUND

[0002] MOS devices are commonly used as tracking switches. Such applications include samplers, multiplexers, track/hold circuits, etc. In the high-speed domain, the non-zero resistance and capacitance of an MOS transistor used to implement such a switch introduce bandwidth limitations that degrade the signal quality. There are techniques for reducing the channel resistance of MOS transistors, and consequently extending the operable bandwidth of tracking switches that utilize them. These techniques include driving the transistor gate by a voltage greater than the supply voltage. Using such so-called "overdrive" gate voltages provides higher channel conductance, and thus lower on-resistance; however, the circuitry required to generate the overdrive voltage above or below the supply voltages (e.g. greater than Vdd or less than ground potential) may be complex and require overdrive protection. There is therefore a need in the art for methods and circuits capable of switching high-speed signals without undue signal attenuation, particularly at relatively high frequencies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0004] Figure 1A depicts a switch 100, in accordance with one embodiment, that selectively passes a high-speed signal between an input terminal Vin and an output terminal Vout.

[0005] Figure 1B is a waveform diagram 105 illustrating the operation of switch 100 of Figure 1A.

[0006] Figure 2 depicts a tracking switch 200 in accordance with another embodiment. Switch 200 is similar in some way to switch 100 of Figure 1A, like-numbered elements being the same or similar.

[0007] Figure 2B is a waveform diagram illustrating the operation of switch 200 of Figure 2A.

[0008] Figure 3 depicts a tracking switch 300 in accordance with another embodiment. Switch 300 is similar to switch 200 in Figure 2A, but includes an NMOS transistor M1 disposed between an input terminal Vin and an output terminal Vsam.

[0009] Figure 4 depicts a transmission gate 400 in accordance with yet another embodiment. Pass gate 400 includes NMOS and PMOS transistors 405 and 410, respectively, coupled in parallel between terminals T1 and T2.

DETAILED DESCRIPTION

[0010] Figure 1A depicts a switch 100, in accordance with one embodiment, that selectively passes a high-speed signal between an input terminal Vin and an output terminal Vout. Figure 1B is a waveform diagram 105 illustrating the operation of switch 100 of Figure 1A. Switch 100 includes a PMOS switching transistor M1 with a first current-handling terminal (e.g., a source S) coupled to input terminal Vin, a second current-handling terminal (e.g., a drain D) coupled to output terminal Vout, and a control terminal (e.g., a gate G) coupled to a control line Ctrl. Control line Ctrl is coupled to switch select terminal Sel via a CMOS inverter comprised of an NMOS transistor M2 and a PMOS transistor M3.

[0011] When select signal Sel is de-asserted (i.e., at a relatively low voltage expressive of a logic zero), transistor M3 pulls control line Ctrl high, in this case toward supply voltage Vdd, turning off transistor M1; conversely, when select signal Sel is asserted (i.e., at a relatively high voltage expressive of a logic one), transistor M2 pulls control line Ctrl low, in

this case toward ground, turning on transistor M1. Though not shown, select signal Sel and transistors M2 and M3 can likewise control additional pass transistors.

[0012] At the schematic level, switch 100 is no different from some conventional switches. The improvement lies in the relative geometries of the transistors. In a conventional switch, transistors M2 and M3 are of similar strength, providing approximately the same on-resistance. Conventional inverters thus produce an inverted version of select signal Sel that follows changes in select signal Sel. Such a hypothetical inverted select signal is depicted in Figure 1B as control signal Ctrl', which is shown as a dashed line mirroring select signal Sel. In switch 100, however, transistor M2 has a relatively high on-resistance, realized by a relatively narrow, long-channeled NMOS device in this example. Transistor M3 is relatively wider and shorter, and consequently exhibits a much lower on-resistance. The control signal Ctrl applied to transistor M1 thus rises rapidly when transistor M3 is turned on (and transistor M2 off) and falls relatively slowly when transistor M2 is turned on (and transistor M3 off). The impedance between the current-handling terminals of a transistor biased on is primarily resistive, and is therefore referred to herein as an "on-resistance," whereas the impedances between the current-handling terminals and the gate is primarily capacitance, and is therefore referred to as an impedance.

[0013] With reference to Figure 1B, an illustrative signal Ctrl shows that the rise and fall times are substantially different due to the disparate on-resistances of transistors M3 and M2. Switch 100 thus turns off much more quickly than on. The relatively slow turn-on speed is not important for some applications, such as when switch 100 is to be part of a programmable interconnect structure, and results in considerable performance gains when switch 100 is employed to transmit high-frequency signals.

[0014] The gate of transistor M1 exhibits parasitic capacitances Crs and Crd between respective current-handling terminals and the control terminal. These capacitances result from misalignment and overlap of the gate of transistor M1 with respect to source and drain

diffusions. Transistor M1 additionally exhibits a channel capacitance Cch, the value of which is primarily a function of the gate area and properties of the gate insulator. For a more detailed discussion of the parasitic and inherent elements of a typical MOS transistor, see pp. 435-445 of "Device Electronics for Integrated Circuits, Second Edition," by R.S. Muller and T.I. Kamins (1986), which is incorporated herein by reference. Notably, that reference separates channel capacitance Cch into gate-to-source capacitance Cgs and gate-to-drain capacitance Cgd.

[0015] When switch 100 is on, transistor M2 connects both current-handling terminals of transistor M1 to ground via the parasitic and channel capacitances. As is well known, the impedance Z through a capacitance reduces with frequency, and is described using the following equation: $Z=(C2\pi f)^{-1}$, where C is capacitance and f is signal frequency. The impedance Z from the current-handling terminals of transistor M1 to line Ctrl, and thus to ground, consequently reduces with frequency. Transistor 100, when turned on, therefore acts as a low-pass filter, shunting high-frequency signal components to ground via transistor M2.

[0016] The geometry of transistor M2 is selected to produce a high on-resistance, which introduces a high-impedance path from the control terminal of transistor M1 to ground. The high-impedance path isolates the control terminal of transistor M1 from ground, thus mitigating the capacitive loading effects of parasitic capacitors C1 and C2. In other words, as the frequency of the input signal increases, the high series impedance provided by transistor M2 limits the effective conductance from the current-handling terminals of transistor M1 to ground. Transistor M3 has a much lower on-resistance than transistor M2, and is thus capable of turning off transistor M1 quickly and preventing signal feed-through when switch 100 is biased off.

[0017] The length "L" of transistors is most commonly the minimum feature size afforded by the process used to form the transistors. This convention holds true for transistors

M1 and M3, but transistor M2 has a length ten times the minimum feature size. The respective geometries of the transistors of Figure 1 are as follows:

a. transistor M1 has a W/L ratio of 60, which is to say that the gate width of transistor M1 is 60 times the length;

b. transistor M2 has a W/L ratio of 1/10, which is to say that the gate length of transistor M2 is 10 times the width; and

c. transistor M3 has a W/L ratio of 10, which is to say that the gate width of transistor M3 is 10 times the length.

[0018] The W/L ratio of transistor M3 is thus 100 times the W/L ratio of transistor M2, in this example. The relationship between the geometries of transistors M2 and M3 can vary, however. The W/L ratio of transistor M3 might be at least ten times the W/L ratio of transistor M2, for example.

[0019] Changing transistor length-to-width ratios is only one way to alter transistor behavior. For example, capacitive values for an MOS transistor can change with the type and thickness of the gate dielectric, and resistive values can vary considerable for different types of devices, doping levels, feature geometries, supply voltage levels, etc. As a consequence of such variations, some embodiments characterize the relationship between transistors M1, M2, and M3 in terms of impedance.

[0020] The minimum impedance Z_{min} from the current-handling terminals of transistor M1 to control line Ctrl may be expressed as $Z_{min}=(C2\pi f_{max})^{-1}$, where C is the total gate capacitance (Crs+Crd+Cch) of transistor M1 and f_{max} is the maximum frequency of input signal Vin. In one embodiment, the on-resistance of transistor M2 may be greater than impedance Z_{min}, over an order of magnitude greater in some examples. Stated in another way, at frequency f_{max} the absolute value of the voltage V_{GS} developed between terminal Vin and line Ctrl is less than or equal to the absolute value of voltage Vin divided by the square root of two. Stated mathematically, when signal Vin is at frequency f_{max}:

$$|V_{GS}| \leq \frac{|V_{in}|}{\sqrt{2}} \quad (1)$$

The relationship of equation (1) ignores some minor variables for simplicity, but is a reasonably accurate approximation. To ensure transistor M1 turns off quickly and to minimize signal feedthrough when transistor M1 is off, the on-resistance of transistor M3 is typically at least an order of magnitude lower than impedance Z_{min}.

[0021] Figure 2 depicts a tracking switch 200 in accordance with another embodiment. Switch 200 may be similar in some ways to switch 100 of Figure 1A, like-numbered elements being the same or similar. Figure 2B is a waveform diagram 212 illustrating the operation of switch 200 of Figure 2A.

[0022] Switch 200 is a tracking switch adapted for use in e.g. high-speed voltage samplers, however, and so is modified in accordance with another embodiment to turn on more quickly than switch 100 of Figure 1. Switch 200 switches on and off in response to a clock signal Clk on a like-named input terminal to sample an input signal on input terminal Vin. Sampled voltages are stored across a load capacitor 205 as a sampled voltage Vsam. Two additional NMOS transistors M4 and M5 and a CMOS inverter 210 assist transistor M2 in pulling the control terminal of transistor M1 down to turn transistor M1on quickly in response to rising edges of clock signal Clk.

[0023] Switch 200 responds to falling edges on line Clk in much the same way switch 100 of Figure 1 responds to falling edges on line Ctrl. Turning to Figure 2B, inverter 210 responds with a corresponding rising edge and transistor M3 pulls control line Ctrl high (toward Vdd). The rising edge on line Clkb turns on transistor M5, but this has little or no effect because the falling edge of clock signal Clk turns transistor M4 off, isolating the control terminal of transistor M1 from ground.

[0024] Switch 200 responds to rising edges on line Clk in much the same way switch 100 of Figure 1 responds to rising edges on line Sel, but transistors M4 and M5 create an open a

path to ground for an instant, passing a current spike Icomp to help transistor M2 quickly turn off transistor M1. The resulting signals are exaggerated in Figure 2A for ease of illustration.

[0025] Transistor M5 is on when clock signal Clk is high, and thus offers a path to ground upon the arrival of he first rising clock edge 220 of clock signal Clk. Rising edge 220 turns on transistors M2, M4, and the NMOS transistor of inverter 210. Due to the delay inherent in inverter 210, transistor M4 begins turning on before transistor M5 begins turning off. Transistors M4 and M5 thus shunt charge away from the control terminal of transistor M1, as illustrated by a current spike 230 in Figure 2B. The duration of current spike 230 can be adjusted by altering the delay induced by inverters 210. In some embodiments, inverter 210 is programmable, as by the selective inclusion of parallel transistors or by controlling the level of supply current.

[0026] Transistor M2, with the help of current spike 230, pulls line Ctrl low to turn transistor M1 on. Transistor M2 then holds the on state beyond the duration of spike 230, at which time transistor M5 is off. As in the example of Figure 1A, transistor M2 is highly resistive in the on state, which reduces the impact of the gate capacitance of transistor M1 on higher-frequency signals. Switch 200 thus turns on quickly without a low-resistance path between the control terminal of transistor M1 and ground. (A dashed line 235 indicates the slow fall-time of signal Ctrl that would occur in the absence of the help from current spike 230.) The strength of transistors M4 and M5 may be selected to match that of transistor M3. In one embodiment, for example, transistors M4 and M5 each have the same W/L ratio of transistor M3. PMOS transistors are generally about twice as resistive as NMOS transistors, so the on-resistance of each of NMOS transistors M4 and M5 is about half that of transistor M3. Resistance adds in series however, so the on-resistance of transistors M4 and M5 combined approximately matches the on-resistance of transistor M3.

[0027] Figure 3 depicts a tracking switch 300 in accordance with another embodiment. Switch 300 is similar to switch 200 in Figure 2A, but includes an NMOS transistor M1 in

place of the PMOS transistor M1 in Figure 2A. In this example, transistor M2 exhibits a much lower on-resistance than transistor M3, and transistors M4 and M5 and an inverter 310 assist transistors M3 in turning on transistor M1 quickly. As is well understood in the art, PMOS transistors employ channels of p-type material that is generally less conductive than the n-type material employed in NMOS transistors. The desired relationship between the on-resistances of transistors M2 and M3 may therefore be obtained using somewhat different respective W/L ratios as compared with the examples of Figures 1A and 2A.

[0028] Figure 4 depicts a transmission gate 400 in accordance with yet another embodiment. Pass gate 400 includes NMOS and PMOS transistors 405 and 410, respectively, coupled in parallel between terminals T1 and T2. Transmission gate 400 can pass signals between terminals T1 and T2 in either direction without a threshold drop. An active-low select signal SELb selectively closes gate 400 via a series-coupled pair of CMOS inverters.

[0029] As in the foregoing examples, the control gates of transistors M1 and M2 are coupled to ground and Vdd, respectively, via transistors exhibiting relatively high on-resistances, and are coupled to Vdd and ground, respectively, via transistors exhibiting relatively high on-resistances. The W/L ratios of the four transistors M3, M4, M5, and M6 that control transistors M1 and M2 in one embodiment are as follows: M3=10W/L, M4=W/10L, M5=W/4L and M6=5W/L. Where switching speed is an issue, configurations of the type described above in connection with Figures 2A and 3 to reduce the turn-on time of pass transistors can be included to momentarily assist transistors M4 and M5.

[0030] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols are set forth to provide a thorough understanding of the present invention. In some instances, the terminology and symbols may imply specific details that are not required to practice the invention. For example, the interconnection between circuit elements or circuit blocks may be shown or described as multi-conductor or single conductor signal lines. Each of the multi-conductor signal lines may alternatively be

single-conductor signal lines, and each of the single-conductor signal lines may alternatively be multi-conductor signal lines. Signals and signaling paths shown or described as being single-ended may also be differential, and vice-versa. Similarly, signals described or depicted as having active-high or active-low logic levels may have opposite logic levels in alternative embodiments. As another example, circuits described or depicted as including metal oxide semiconductor (MOS) transistors may alternatively be implemented using bipolar technology or any other technology in which a signal-controlled current flow may be achieved. With respect to terminology, a signal is said to be "asserted" when the signal is driven to a low or high logic state (or charged to a high logic state or discharged to a low logic state) to indicate a particular condition. Conversely, a signal is said to be "de-asserted" to indicate that the signal is driven (or charged or discharged) to a state other than the asserted state (including a high or low logic state, or the floating state that may occur when the signal driving circuit is transitioned to a high impedance condition, such as an open drain or open collector condition). A signal driving circuit is said to "output" a signal to a signal receiving circuit when the signal driving circuit asserts (or de-asserts, if explicitly stated or indicated by context) the signal on a signal line coupled between the signal driving and signal receiving circuits. A signal line is said to be "activated" when a signal is asserted on the signal line, and "deactivated" when the signal is de-asserted. Additionally, the prefix symbol "/" attached to signal names indicates that the signal is an active low signal (i.e., the asserted state is a logic low state). Whether a given signal is an active low or an active high will be evident to those of skill in the art.

[0031] An output of the design process for an integrated circuit, or a portion of an integrated circuit, may be a computer-readable medium (e.g., a magnetic tape or an optical or magnetic disk) encoded with data structures or other information defining circuitry that may be physically instantiated as an integrated circuit or portion of an integrated circuit. These data structures are commonly written in Caltech Intermediate Format (CIF) or GDSII, a

proprietary binary format. Those of skill in the art of mask preparation can develop such data structures from schematic diagrams of the type detailed above.

[0032] While the present invention has been described in connection with specific embodiments, variations of these embodiments will be obvious to those of ordinary skill in the art. For example:

1. While the foregoing embodiments employ MOS transistors formed using standard CMOS processes, other transistor types or combinations of transistor types might also be used.
2. As noted in the background section above, some conventional devices overdrive the switched transistor to reduce the on-resistance, and consequently increase speed performance. Embodiments of the invention can be adapted to overdrive the gate to achieve still better high frequency performance.
3. Pass gates in accordance with other embodiments can be adapted to including clocking, e.g. in the manner described above in connection with Figures 2A and 3.

Moreover, some components are shown directly connected to one another while others are shown connected via intermediate components. In each instance the method of interconnection, or "coupling," establishes some desired electrical communication between two or more circuit nodes, or terminals. Such coupling may often be accomplished using a number of circuit configurations, as will be understood by those of skill in the art. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description.

CLAIMS

What is claimed is:

1. A circuit (100, 200) comprising:

a first transistor (M1) having first and second current-handling terminals, a first control terminal, and a first width-to-length ratio;

a second transistor (M2) having a third current-handling terminal coupled to the first control terminal, a fourth current-handling terminal, a second control terminal, and a second width-to-length ratio; and

a third transistor (M3) having a fifth current-handling terminal coupled to the first control terminal, a sixth current-handling terminal, a third control terminal, and a third width-to-length ratio at least ten times the second width-to-length ratio.

2. The circuit (100, 200) of claim 1, wherein the second width-to-length ratio is less than 0.2 times the first width-to-length ratio.

3. The circuit (200) of claim 1, further comprising a capacitor (205) coupled to the second current-handling terminal.

4. The circuit (100, 200) of claim 1, wherein the fourth current-handling termi-nal is connected to a power-supply terminal.

5. The circuit (100, 200) of claim 4, wherein the sixth current-handling terminal is connected to a second power-supply terminal.

6. The circuit (200) of claim 1, further comprising:

a fourth transistor (M4) having a seventh current-handling terminal coupled to the

first control terminal, an eighth current-handling terminal, and a fourth control terminal coupled to the second control terminal;

a fifth transistor (M5) having a ninth current-handling terminal coupled to the eighth current-handling terminal, a tenth current-handling terminal, and a fifth control terminal; and

a delay element coupled between the second control terminal and the fifth control terminal.

7. The circuit (200) of claim 6, wherein the delay element includes an inverter (210).

8. The circuit (100, 200) of claim 1, wherein the first and third transistors (M1, M3) are PMOS transistors.

9. The circuit (200) of claim 1, further comprising a clock node coupled to the second and third control terminals and receiving a clock signal.

10. A circuit (100, 200) comprising:

an input node receiving an input signal of a maximum input frequency;

a first transistor (M1) having a first current handling terminal coupled to the input node, a second current-handling terminal, and a first control terminal, wherein the first transistor (M1), when biased on, exhibits an impedance to the input signal at the maximum input frequency between the first current-handling terminal and the first control terminal;

a second transistor (M2) having a third current-handling terminal coupled to the first control terminal, a fourth current-handling terminal, and a second control terminal, wherein the second transistor (M2) exhibits a first on-resistance be-tween the third and

fourth current-handling terminals, and wherein the first on-resistance is greater than the impedance; and

a third transistor (M3) having a fifth current-handling terminal coupled to the first control terminal, a sixth current-handling terminal, and a third control termi-nal, wherein the third transistor (M3) exhibits a second on-resistance between the fifth and sixth current-handling terminals, and wherein the second on-resistance is less than ten percent of the first on-resistance.

11. The circuit (100, 200) of claim 10, wherein the first on-resistance is more than five times the second on-resistance.

12. The circuit (200) of claim 10, further comprising a capacitor (205) coupled to the second current-handling terminal.

13. The circuit (100, 200) of claim 10, wherein the fourth current-handling ter-minal is coupled to a power-supply terminal.

14. The circuit (100, 200) of claim 13, wherein the sixth current-handling terminal is coupled to a second power-supply terminal.

15. The circuit (200) of claim 10, further comprising:

a fourth transistor (M4) having a seventh current-handling terminal coupled to the first control terminal, an eighth current-handling terminal, and a fourth control terminal coupled to the second control terminal;

a fifth transistor (M5) having a ninth current-handling terminal coupled to the eighth current-handling terminal, a tenth current-handling terminal, and a fifth control

terminal; and

a delay element coupled between the second control terminal and the fifth control terminal.

16. The circuit (200) of claim 15, wherein the delay element includes an in-verter (210).

17. The circuit (100, 200) of claim 10, wherein the first and third transistors (M1, M3) are PMOS transistors.

18. A computer-readable medium having stored thereon a data structure defin-ing an integrated circuit (100, 200) to be formed on and within a semiconductor layer, the data structure comprising:

data specifying an input node receiving an input signal of a maximum input frequency;

data specifying a first transistor (M1) having a first current handling terminal coupled to the input node, a second current-handling terminal, and a first control terminal, wherein the first transistor (M1), when biased on, exhibits an impedance to the input signal at the maximum input frequency between the first current-handling terminal and the first control terminal;

data specifying a second transistor (M2) having a third current-handling terminal coupled to the first control terminal, a fourth current-handling terminal, and a second control terminal, wherein the second transistor (M2) exhibits a first on-resistance between the third and fourth current-handling terminals, and wherein the first on-resistance is greater than the impedance; and

data specifying a third transistor (M3) having a fifth current-handling terminal coupled to the first control terminal, a sixth current-handling terminal, and a third

control terminal, wherein the third transistor (M3) exhibits a second on-resistance between the fifth and sixth current-handling terminals, and wherein the second on-resistance is less than ten percent of the first on-resistance.

19. A circuit (100, 200) comprising:

a first voltage terminal providing a first voltage;

a second voltage terminal providing a second voltage;

a switch transistor (M1) having first and second current-handling terminals and a control terminal, the switch transistor (M1) exhibiting a capacitance between the current-handling terminals and the control terminal; and

means for turning the switch transistor (M1) on and off, the means including:

means (M2) for coupling the control terminal to the first voltage terminal via a first impedance to turn the switch transistor (M1) on; and

means (M3) for coupling the control terminal to the second voltage terminal via a second impedance to turn the switch transistor (M1) off;

wherein the first impedance is at least ten times greater than the second impedance.

20. The circuit (200) of claim 19, further comprising a capacitor (205) coupled to the second current-handling terminal.

21. The circuit (100, 200) of claim 19, wherein the first current-handling terminal receives an input signal of a maximum input frequency, and wherein the switch transistor (M1), when on, exhibits a capacitive impedance $Z = (C2\pi f_{max})^{-1}$ to the input signal between the control terminal and the first and second current-handling terminals.

22. The circuit (100, 200) of claim 21, wherein the first impedance is greater than the capacitive impedance.

23. The circuit (100, 200) of claim 22, wherein the first impedance is at least five times the capacitive impedance.

24. A circuit (100, 200) comprising:

an input node receiving an input signal of a maximum input frequency and a first voltage at the maximum input frequency;

a first transistor (M1) having a first current handling terminal coupled to the input node, a second current-handling terminal, and a first control terminal, wherein the first transistor (M1), when biased on, exhibits a first impedance to the input signal at the maximum input frequency between the first current-handling terminal and the first control terminal; and

a second transistor (M2) having a third current-handling terminal coupled to the first control terminal, a fourth current-handling terminal, and a second control terminal, wherein the second transistor (M2) exhibits a second impedance, when biased on, between the third and fourth current-handling terminals; and

wherein the first transistor (M1) develops a second voltage, between the first current-handling terminal and the control terminal; and

wherein the absolute value of the second voltage at most equals the absolute value of the first voltage divided by the square root of two.

25. The circuit (100, 200) of claim 24, further comprising a third transistor (M3) having a fifth current-handling terminal coupled to the first control terminal, a sixth current-handling terminal, and a third control terminal, wherein the third transistor (M3)

exhibits a third impedance, when biased on, between the fifth and sixth current-handling terminals, and wherein the third impedance is less than ten percent of the second impedance.

26. The circuit (100, 200) of claim 24, wherein the second impedance is an on-resistance.

27. The circuit (200) of claim 24, further comprising:

a fourth transistor (M4) having a seventh current-handling terminal coupled to the first control terminal, an eighth current-handling terminal, and a fourth control terminal coupled to the second control terminal;

a fifth transistor (M5) having a ninth current-handling terminal coupled to the eighth current-handling terminal, a tenth current-handling terminal, and a fifth control terminal; and

a delay element coupled between the second control terminal and the fifth control terminal.

28. The circuit (200) of claim 27, wherein the delay element includes an inverter (210).

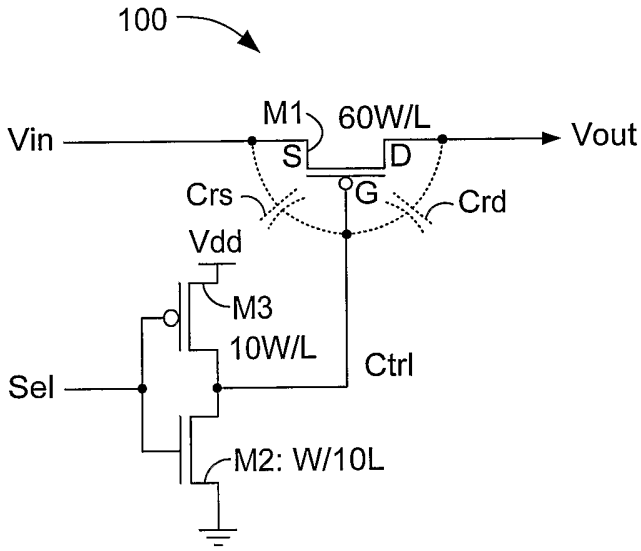


FIG. 1A

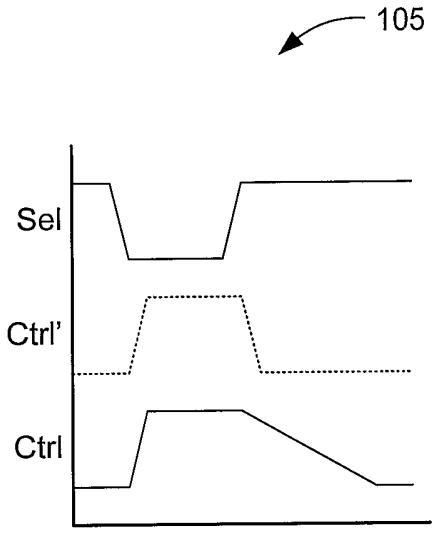


FIG. 1B

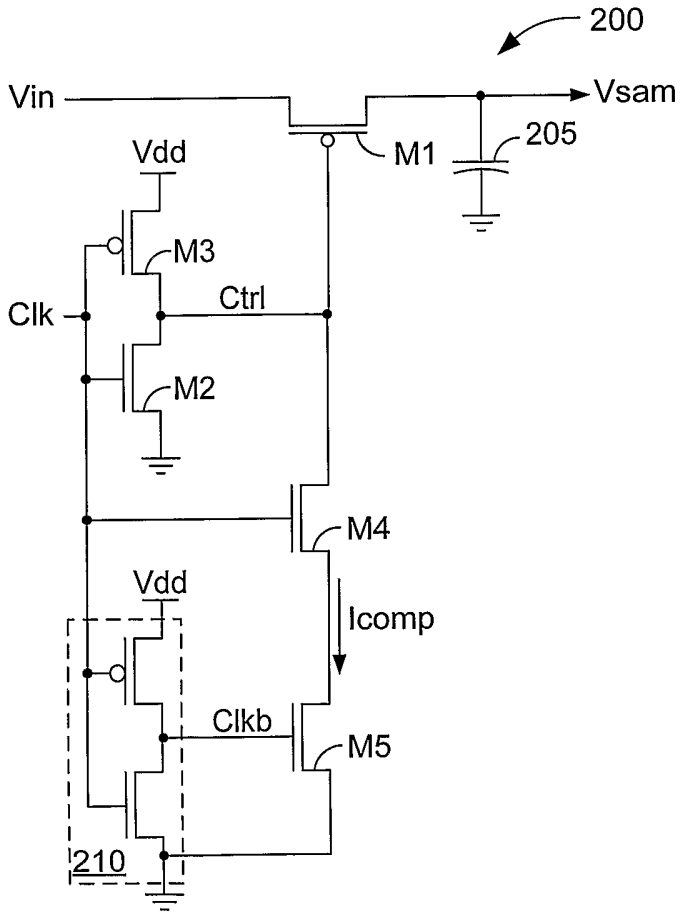


FIG. 2A

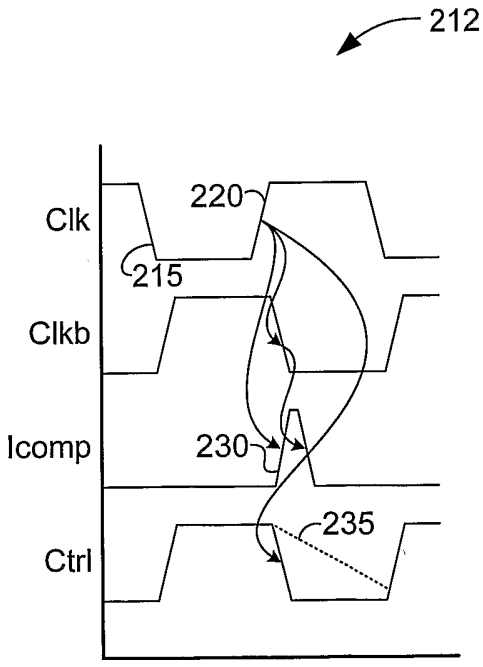
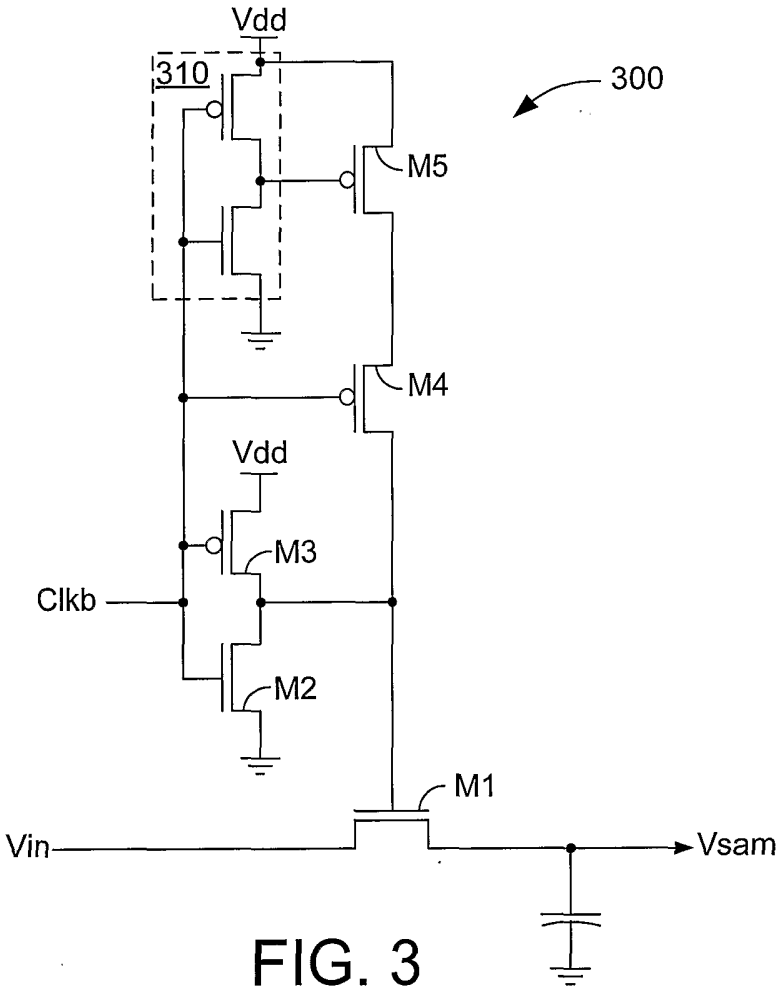


FIG. 2B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300
M5
M4
Vdd
M3
Clkb
M2
M1
Vin
Vsam

FIG. 3

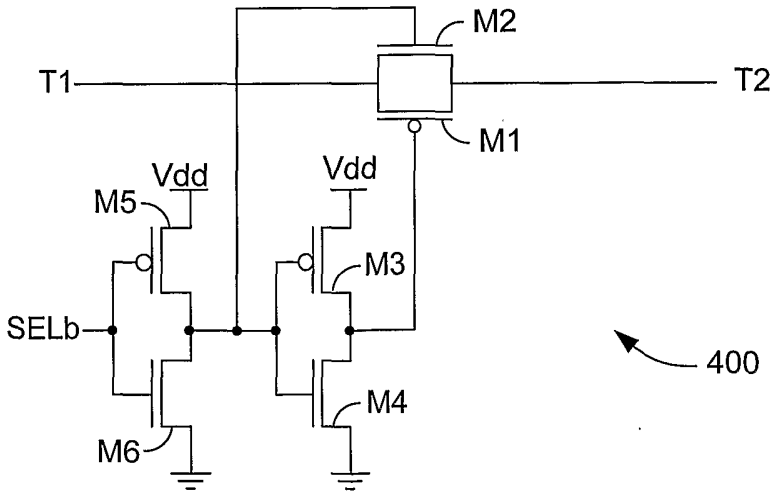
M2
T1
T2
M1
Vdd
Vdd
M5
M3
SELb
400
M4
M6

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/039700

A. CLASSIFICATION OF SUBJECT MATTER
H03K17/041 H03K17/16 H03K17/687

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2001/007430 A1 (GOODELL TRENOR F) 12 July 2001 (2001-07-12) paragraph [0012] - paragraph [0039]; figure 5	1-5, 8-14, 17-26 6,7,15, 16,27,28
Y	EP 1 115 202 A (NISSAN MOTOR CO., LTD) 11 July 2001 (2001-07-11) paragraph [0080] - paragraph [0081]; figures 9,13	6,7,15, 16,27,28
X	US 3 872 325 A (ADAMS ET AL) 18 March 1975 (1975-03-18) column 2, line 15 - column 4, line 45; figure 2	19-23

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
15 March 2006	27/03/2006

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/039700

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/196089 A1 (O'DONNELL JOHN J ET AL) 7 October 2004 (2004-10-07) figures 7,8	19-23
X	US 6 380 644 B1 (ILIASEVITCH STEPAN) 30 April 2002 (2002-04-30) figure 12	19-23
A	DE 44 28 548 A1 (ROBERT BOSCH GMBH, 70469 STUTTGART, DE) 15 February 1996 (1996-02-15) the whole document	1-28

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2005/039700

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2001007430 A1	12-07-2001	DE 10047647 A1	07-06-2001
		JP 2001217701 A	10-08-2001
EP 1115202 A	11-07-2001	DE 60020064 D1	16-06-2005
		DE 60020064 T2	12-01-2006
		JP 3664061 B2	22-06-2005
		JP 2001251173 A	14-09-2001
		US 2001005152 A1	28-06-2001
US 3872325 A	18-03-1975	AU 7001774 A	18-12-1975
		DE 2433965 A1	30-04-1975
		FR 2248652 A1	16-05-1975
		IT 1015558 B	20-05-1977
		JP 50068213 A	07-06-1975
		NL 7409361 A	21-04-1975
		SE 7409291 A	18-04-1975
US 2004196089 A1	07-10-2004	CN 1543069 A	03-11-2004
US 6380644 B1	30-04-2002	CA 2324695 A1	26-05-2001
DE 4428548 A1	15-02-1996	WO 9605654 A1	22-02-1996