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METAL OXIDE THIN FILM TRANSISTORS WITH CONTROLLED HYDROGEN

Field

Embodiments of the present disclosure generally relate to the field of integrated circuits, and more particularly, to transistors.

Background

A thin-film transistor (TFT) is a kind of field-effect transistor including various layers, e.g., an oxide semiconductor material as a channel layer, a gate dielectric layer, and metallic contacts, over a supporting but non-conducting substrate. A TFT differs from a conventional transistor, where a channel of the conventional transistor is typically within a substrate, such as a silicon substrate. Impurities such as hydrogen may diffuse into the channel layer of a TFT. Hydrogen in the channel layer of a TFT may cause large threshold voltages of the TFT.

Brief Description of the Drawings

Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

Figure 1 schematically illustrates a diagram of a thin-film transistor (TFT) with a hydrogen diffusion barrier (HDB) layer, in accordance with some embodiments.

Figures 2(a)-2(j) schematically illustrate a process for forming a TFT with a HDB layer, in accordance with some embodiments.

Figure 3 schematically illustrates another process for forming a TFT with a HDB layer, in accordance with some embodiments.

Figure 4 schematically illustrates an interposer implementing one or more embodiments of the disclosure, in accordance with some embodiments.

Figure 5 schematically illustrates a computing device built in accordance with an embodiment of the disclosure, in accordance with some embodiments.

Detailed Description

Thin-film transistors (TFTs) hold great potential for large area and flexible electronics, e.g., displays. A TFT may have a channel layer formed by one or more of various materials, e.g., metal oxide materials. Indium gallium zinc oxide (IGZO) is a

5 semiconducting material, including indium (In), gallium (Ga), zinc (Zn) and oxygen (O), which can be used to form the channel layer of a TFT, i.e., an IGZO TFT. An IGZO TFT may be used in the backplane of flat-panel displays (FPDs), active-matrix organic light-emitting diode (AMOLED) displays, a thin-film-transistor liquid-crystal displays (TFT LCDs), micro light-emitting diode (μ LED) displays, or others. Other material comprising
10 zinc (Zn) and oxygen (O) may be used for the channel layer of a TFT additionally or alternatively.

Hydrogen may diffuse into the channel layer of a TFT, causing large threshold voltage of the TFT, and other problems. Hydrogen may diffuse to the channel layer from a gate dielectric layer or a passivation layer containing SiO_2 or Si_3N_4 formed by plasma-
15 enhanced chemical vapor deposition (PECVD).

In embodiments, a hydrogen diffusion barrier (HDB) layer may be formed to protect the channel layer of a TFT from hydrogen diffusion, e.g., from the gate dielectric layer. The material for a HDB layer may be selected to reduce hydrogen diffusion into the channel layer. For a channel layer comprising zinc (Zn) and oxygen (O), Al_2O_3 , TiO_2 ,
20 AlN , or doped Al_2O_3 or doped TiO_2 , e.g., doped by nitrogen, carbon, sulfur, may be selected as a material for the HDB layer to reduce hydrogen diffusion into the channel layer. The HDB layer covers the channel layer of the TFT, but may leave the source area and the drain area not covered by the HDB layer so that hydrogen may still diffuse into the source area and the drain area. Hydrogen diffused into the source area and the drain
25 area may reduce the contact resistance and improve the performance of the TFT.

Embodiments herein may present a semiconductor device, which includes a substrate, and a gate electrode above the substrate. A gate dielectric layer may conformally cover the gate electrode and the substrate. In addition, a HDB layer may be above the gate dielectric layer, and a channel layer may be above the HDB layer. Hence,
30 the HDB layer may be between the gate dielectric layer and the channel layer, reducing the hydrogen diffusion from the gate dielectric layer to the channel layer. Furthermore, a source area and a drain area may be formed within the channel layer, a source electrode may be coupled to the source area, and a drain electrode may be coupled to the drain area. The source area and the drain area may not be covered by the HDB layer so that
35 hydrogen may still diffuse into the source area and the drain area.

Embodiments herein may present an electrical system, which includes a processor, a memory device coupled to the processor, and a display coupled to the processor. In embodiments, the display may include a transistor having a substrate and a

5 gate electrode above the substrate. A gate dielectric layer may conformally cover the gate electrode and the substrate. Moreover, a HDB layer may be above the gate dielectric layer, and a channel layer may be above the HDB layer. Furthermore, the channel layer may include a source area and a drain area, a source electrode may be coupled to the source area, and a drain electrode may be coupled to the drain area.

10 In embodiments, a method for forming a semiconductor device may include: forming a gate electrode above a substrate, and forming a gate dielectric layer conformally covering the gate electrode and the substrate. The method may also include forming a HDB layer above the gate dielectric layer, and forming a channel layer above the HDB layer. In addition, the method may include forming a source area and a drain
15 area within the channel layer, forming a source electrode coupled to the source area, and a drain electrode coupled to the drain area.

In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to
20 those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances,
25 well-known features are omitted or simplified in order not to obscure the illustrative implementations.

Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure. However, the order of description should not be construed to imply that these operations are necessarily order
30 dependent. In particular, these operations may not be performed in the order of presentation.

For the purposes of the present disclosure, the phrase “A and/or B” means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B, and/or C” means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

35 The terms “over,” “under,” “between,” “above,” and “on” as used herein may refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers.

5 Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening features.

10 The description may use the phrases “in an embodiment,” or “in embodiments,” which may each refer to one or more of the same or different embodiments. Furthermore, the terms “comprising,” “including,” “having,” and the like, as used with respect to embodiments of the present disclosure, are synonymous.

The term “coupled with,” along with its derivatives, may be used herein.
15 “Coupled” may mean one or more of the following. “Coupled” may mean that two or more elements are in direct physical or electrical contact. However, “coupled” may also mean that two or more elements indirectly contact each other, but yet still cooperate or interact with each other, and may mean that one or more other elements are coupled or connected between the elements that are said to be coupled with each other. The term
20 “directly coupled” may mean that two or more elements are in direct contact.

In various embodiments, the phrase “a first feature formed, deposited, or otherwise disposed on a second feature” may mean that the first feature is formed, deposited, or disposed over the second feature, and at least a part of the first feature may be in direct contact (e.g., direct physical and/or electrical contact) or indirect contact
25 (e.g., having one or more other features between the first feature and the second feature) with at least a part of the second feature.

Where the disclosure recites “a” or “a first” element or the equivalent thereof, such disclosure includes one or more such elements, neither requiring nor excluding two or more such elements. Further, ordinal indicators (e.g., first, second, or third) for
30 identified elements are used to distinguish between the elements, and do not indicate or imply a required or limited number of such elements, nor do they indicate a particular position or order of such elements unless otherwise specifically stated.

As used herein, the term “circuitry” may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared,
35 dedicated, or group), and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable hardware components that provide the described functionality. As used herein, “computer-implemented method” may refer to any method executed by one or more

5 processors, a computer system having one or more processors, a mobile device such as a smartphone (which may include one or more processors), a tablet, a laptop computer, a set-top box, a gaming console, and so forth.

Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate
10 may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or
15 other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

A plurality of transistors, such as metal-oxide-semiconductor field-effect
20 transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the
25 implementations described herein may illustrate only planar transistors, it should be noted that the disclosure may also be carried out using nonplanar transistors.

Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide
30 (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide,
35 zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some

5 embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

 The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type work function metal or N-type work function metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations,
10 the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

 For a PMOS transistor, metals that may be used for the gate electrode include, but
15 are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a work function that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and
20 carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a work function that is between about 3.9 eV and about 4.2 eV.

 In some implementations, when viewed as a cross-section of the transistor along
25 the source-channel-drain direction, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface
30 of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

35 In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming

5 sidewall spacers are well known in the art and generally include deposition and etching process operations. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

As is well known in the art, source and drain regions are formed within the
10 substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes
15 them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon
20 alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal
25 and/or metal alloys may be used to form the source and drain regions.

One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon
30 doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

Figure 1 schematically illustrates a diagram of a TFT 110 with a HDB layer 109,
35 in accordance with some embodiments. In embodiments, the TFT 110 may include a substrate 101, a buffer layer 103, a gate electrode 105, a gate dielectric layer 107, the HDB layer 109, a channel layer 111, a source electrode 121 and a drain electrode 123, and an interlayer dielectric (ILD) layer 115. In addition, the TFT 110 may include an optional

5 HDB layer, e.g., a HDB layer 113.

In embodiments, the buffer layer 103 may be above the substrate 101. The gate electrode 105 may be above the buffer layer 103. The gate dielectric layer 107 may be above the gate electrode 105 and the buffer layer 103. The HDB layer 109 may be above the gate dielectric layer 107. The channel layer 111 may be above the HDB layer 109.
10 The HDB layer 113 may be above the channel layer 111. The ILD layer 115 may be above the HDB layer 113. The source electrode 121 may be coupled to a source area 117 within the channel layer 111, and the drain electrode 123 may be coupled to a drain area 119 within the channel layer 111. The source area 117 and the drain area 119 may not be covered by the HDB layer 109 or the HDB layer 113 so that hydrogen may still diffuse
15 into the source area 117 and the drain area 119.

The structure of the TFT 110 shown in Figure 1 may be for illustration purpose only and is not limiting. The TFT 110 may have other configurations. For example, the TFT 110 may have a reverse stagger structure in which the gate electrode 105 may be above the channel layer 111, separated by the gate dielectric layer 107 and the HDB layer
20 109 in between the gate electrode 105 and the channel layer 111.

In embodiments, the substrate 101 may be a glass substrate, such as soda lime glass or borosilicate glass, a metal substrate, a plastic substrate, or another suitable substrate. Other inter-metal dielectric layer may be formed on the substrate. The substrate 101 may include an inter-metal dielectric layer, or other devices, not shown for
25 clarity.

In embodiments, the buffer layer 103 may be optional. Some other embodiments may not have the buffer layer 103. The buffer layer 103 may include a silicon oxide (SiO) film, a silicon nitride (SiN) film, or another suitable material. In some embodiments, there may be multiple buffer layers included within the buffer layer 103.

30 In embodiments, the gate electrode 105 may be formed as a single layer or a stacked layer using one or more conductive films including a conductive material, e.g., copper, aluminum, tantalum, tungsten, tantalum nitride (TaN), titanium, titanium nitride (TiN), the like, and/or a combination thereof.

In embodiments, the gate dielectric layer 107 may include silicon oxide (SiO₂),
35 silicon nitride (SiN_x), yttrium oxide (Y₂O₃), silicon oxynitride (SiO_xN_y), aluminum oxide (Al₂O₃), hafnium(IV) oxide (HfO₂), tantalum oxide (Ta₂O₅), titanium dioxide (TiO₂), or other materials. The gate dielectric layer 107 may be formed by plasma enhanced chemical vapor deposition (PECVD) at about 100 °C to about 200 °C. The gate dielectric

5 layer 107 may prevent impurities, e.g., impurities in an atmosphere, such as moisture, or impurities included in the substrate, such as an alkali metal or a heavy metal, from entering the channel layer 111.

In embodiments, the HDB layer 109 may include Al_2O_3 , TiO_2 , AlN , or doped Al_2O_3 or TiO_2 , e.g., doped by nitrogen, carbon, sulfur, or another suitable material. The
10 HDB layer 109 may have a thickness in a range of about 5 nm to about 20 nm. The HDB layer 109 may be formed by physical vapor deposition (PVD), atomic layer deposition (ALD), or chemical vapor deposition (CVD).

In embodiments, the channel layer 111 may include the source area 117 and the drain area 119. The channel layer 111 may have a thickness in a range of about 10 nm to
15 about 100 nm. The channel layer 111 may include a material comprising zinc (Zn) and oxygen (O), such as, IGZO, amorphous InGaZnO (a-IGZO), crystal-like InGaZnO (c-IGZO), GaZnON, ZnON, or C-Axis Aligned Crystal (CAAC). TFTs with the channel layer 111 including a-IGZO may hold great potential for large area and flexible electronics. CAAC is a partially crystallized form of IGZO, which may retain the
20 uniformity of the amorphous phase while improving stability and exhibiting low leakage current.

In embodiments, an optional HDB layer, e.g., the HDB layer 113, may be formed above the channel layer 111. The HDB layer 113 may be similar to the HDB layer 109, including Al_2O_3 , TiO_2 , AlN , or doped Al_2O_3 or TiO_2 , e.g., doped by nitrogen, carbon,
25 sulfur, or another suitable material. In embodiments, the HDB layer 113 may have a different thickness than the thickness of the HDB layer 109.

In embodiments, the ILD layer 115 may be formed above the channel layer 111, and above the HDB layer 113. The ILD layer 115 may include O_3 -tetraethylorthosilicate (TEOS), O_3 -hexamethyldisiloxane (HMDS), plasma-TEOS oxide layer, or other materials.
30 The ILD layer 115 may be formed by chemical vapor deposition (CVD), PECVD, or another suitable technique.

In embodiments, the source electrode 121 and the drain electrode 123 may be formed through the ILD layer 115 and coupled to the source area 117 and the drain area 119, respectively. When there is an optional HDB layer, e.g., the HDB layer 113, the
35 source electrode 121 and the drain electrode 123 may be formed through the HDB layer 113 as well. The source electrode 121 and the drain electrode 123 may include titanium (Ti), molybdenum (Mo), gold (Au), platinum (Pt), aluminum (Al), nickel (Ni), copper (Cu), chromium (Cr), an alloy of Ti, Mo, Au, Pt, Al Ni, Cu, Cr, or another suitable

5 material.

Figures 2(a)-2(j) schematically illustrate a process 200 for forming a TFT 210 with a HDB layer 209, in accordance with some embodiments. In embodiments, the TFT 210 may be similar to the TFT 110 in Figure 1.

10 As shown in Figure 2(a), a substrate 201 may be provided. In embodiments, the substrate 201 may be similar to the substrate 101 in Figure 1. For example, the substrate 201 may be a glass substrate, such as soda lime glass or borosilicate glass, a metal substrate, a plastic substrate, or another suitable material.

15 As shown in Figure 2(b), a buffer layer 203 may be formed above the substrate 201. In embodiments, the buffer layer 203 may be similar to the buffer layer 103 in Figure 1. For example, the buffer layer 203 may include SiO₂, SiN, or another suitable material. There may be multiple buffer layers included within the buffer layer 203.

20 As shown in Figure 2(c), a gate electrode 205 may be formed above the buffer layer 203. In embodiments, the gate electrode 205 may be similar to the gate electrode 105 in Figure 1. For example, the gate electrode 205 may include one or more of conductive films including a conductive material, e.g., copper, aluminum, tantalum, tungsten, TaN, titanium, TiN, the like, and/or a combination thereof.

25 As shown in Figure 2(d), a gate dielectric layer 207 may be formed above the gate electrode 205. In embodiments, the gate dielectric layer 207 may be similar to the gate dielectric layer 107 in Figure 1. For example, the gate dielectric layer 207 may include SiO₂, SiN_x, Y₂O₃, SiO₂N_y, Al₂O₃, HfO₂, Ta₂O₅, TiO₂, or other materials. The gate dielectric layer 207 may conformally cover the gate electrode 205 and the substrate 201, where the dielectric layer 207 may follow the contour of the gate electrode 205, covering a top surface, the side surfaces of the gate electrode 205. Furthermore, the dielectric layer 207 may have a uniform thickness relative to the surface of the substrate 201, the top surface of the gate electrode 205, or the side surfaces of the gate electrode 205.

30 As shown in Figure 2(e), the HDB layer 209 may be formed above the gate dielectric layer 207. In embodiments, the HDB layer 209 may be similar to the HDB layer 109 in Figure 1. For example, the HDB layer 209 may include Al₂O₃, TiO₂, AlN, or doped Al₂O₃ or TiO₂, e.g., doped by nitrogen, carbon, sulfur, or other materials, formed by PVD, ALD, or CVD.

As shown in Figure 2(f), a channel layer 211 may be formed above the HDB layer 209. In embodiments, the channel layer 211 may be similar to the channel layer 111 in Figure 1. For example, the channel layer 211 may be a channel layer, including IGZO, a-

5 IGZO, c-IGZO, GaZnON, ZnON, CAAC, or other materials.

As shown in Figure 2(g), an optional HDB layer, e.g., a HDB layer 213, may be formed above the channel layer 211. In embodiments, the HDB layer 213 may be similar to the HDB layer 113 in Figure 1. For example, the HDB layer 213 may include Al_2O_3 , TiO_2 , AlN, or doped Al_2O_3 or TiO_2 , e.g., doped by nitrogen, carbon, sulfur, or other materials.

As shown in Figure 2(h), an ILD layer 215 may be formed above the HDB layer 213. In embodiments, the ILD layer 215 may be similar to the ILD layer 115 in Figure 1. For example, the ILD layer 215 may include TEOS, HMDS, plasma-TEOS oxide, or other materials.

15 As shown in Figure 2(i), an opening 212 and an opening 214 may be formed through the ILD layer 215 and the HDB layer 213 to expose an area 217 of the channel layer 211 to be a source area, and expose an area 219 of the channel layer 211 to be a drain area.

As shown in Figure 2(j), a source electrode 221 and a drain electrode 223 may be formed filling the opening 212 and the opening 214, and through the ILD layer 215 and the HDB layer 213. The source electrode 221 may be coupled with the source area 217, and the drain electrode 223 may be coupled with the drain area 219. In embodiments, the source electrode 221 and the drain electrode 223 may be similar to the source electrode 121 and the drain electrode 123 in Figure 1, respectively. For example, the source electrode 221 and the drain electrode 223 may include Ti, Mo, Au, Pt, Al, Ni, Cu, Cr, an alloy of Ti, Mo, Au, Pt, Al Ni, Cu, Cr, or another suitable material.

Figure 3 schematically illustrates another process 300 for forming a TFT with a HDB layer, in accordance with some embodiments. In embodiments, the process 300 may be applied to form the TFT 110 with the HDB layer 109 in Figure 1, or the TFT 210 with the HDB 209 in Figure 2(j). In addition, the process 200 shown in Figures 2(a)-2(j) may be an example of the process 300.

At block 301, the process 300 may include forming a gate electrode above a substrate. For example, the process 300 may include forming the gate electrode 205 above the substrate 201 as illustrated in Figure 2(c).

35 At block 303, the process 300 may include forming a gate dielectric layer conformally covering the gate electrode and the substrate. For example, the process 300 may include forming the gate dielectric layer 207 covering the gate electrode 205 and the substrate 201 as illustrated in Figure 2(d). In embodiments, the gate dielectric layer 207

5 may include SiO₂ or SiN_x, and may be formed by PECVD at about 100 °C to about 200 °C.

At block 305, the process 300 may include forming a HDB layer above the gate dielectric layer. For example, the process 300 may include forming the HDB layer 209 above the gate dielectric layer 207 as illustrated in Figure 2(e). In embodiments, the
10 HDB layer 209 may include Al₂O₃, TiO₂, AlN, or doped Al₂O₃ or TiO₂, e.g., doped by nitrogen, carbon, sulfur. The HDB layer 209 may be formed by PVD, ALD, CVD, or another suitable process.

At block 307, the process 300 may include forming a channel layer above the HDB layer. For example, the process 300 may include forming the channel layer 211
15 above the HDB layer 209 as illustrated in Figure 2(f). In embodiments, the channel layer 211 may include a material comprising zinc (Zn) and oxygen (O), such as, IGZO, a-IGZO, c-IGZO, GaZnON, ZnON, CAAC, or another suitable material.

In some embodiments, the channel layer 211 may be formed by depositing an a-IGZO film at about 25 °C to about 300 °C, e.g., by radio frequency (RF) sputtering, direct
20 current (DC) sputtering, magnetron sputtering, plasma enhanced atomic layer deposition (PEALD), or PECVD. In some other embodiments, the channel layer 111 may be formed by simultaneously sputtering IGZO and ZnO at a temperature in a range of about 25 °C to about 400 °C, e.g., by RF sputtering, DC sputtering, or magnetron sputtering, to form a crystal-like InGaZnO (c-IGZO) film.

25 At block 309, the process 300 may include forming a source area and a drain area within the channel layer. For example, the process 300 may include forming the source area 217 and the drain area 219, as shown in Figure 2(i), by forming the opening 212 and the opening 214 through the ILD layer 215 and the HDB layer 213.

At block 311, the process 300 may include forming a source electrode coupled to
30 the source area, and a drain electrode coupled to the drain area. For example, the process 300 may include forming the source electrode 221 coupled to the source area 217, and the drain electrode 223 coupled to the drain area 219, as illustrated in Figure 2(j). In embodiments, the source electrode 221 and the drain electrode 223 may include Ti, Mo, Au, Pt, Al, Ni, Cu, Cr, an alloy of Ti, Mo, Au, Pt, Al Ni, Cu, Cr, or other materials.

35 In addition, the process 300 may also include forming another HDB layer above the channel layer, and forming an interlayer dielectric (ILD) layer above the channel layer, not shown. The process 300 may further include forming a buffer layer above the substrate before forming the gate electrode.

5 **Figure 4** illustrates an interposer 400 that includes one or more embodiments of the disclosure. The interposer 400 is an intervening substrate used to bridge a first substrate 402 to a second substrate 404. The first substrate 402 may be, for instance, a substrate support for a TFT, e.g., the TFT 110 shown in Figure 1 or the TFT 210 shown in Figure 2(j). The second substrate 404 may be, for instance, a memory module, a
10 computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 400 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 400 may couple an integrated circuit die to a ball grid array (BGA) 406 that can subsequently be coupled to the second substrate 404. In some embodiments, the first and second substrates 402/404 are attached to
15 opposing sides of the interposer 400. In other embodiments, the first and second substrates 402/404 are attached to the same side of the interposer 400. And in further embodiments, three or more substrates are interconnected by way of the interposer 400.

 The interposer 400 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further
20 implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

 The interposer may include metal interconnects 408 and vias 410, including but not limited to through-silicon vias (TSVs) 412. The interposer 400 may further include
25 embedded devices 414, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the
30 interposer 400.

 In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer 400.

Figure 5 illustrates a computing device 500 in accordance with one embodiment of the disclosure. The computing device 500 may include a number of components. In
35 one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die, such as a SoC used for mobile devices. The components in the computing device 500 include, but are not limited to, an integrated circuit die 502 and

5 at least one communications logic unit 508. In some implementations the communications logic unit 508 is fabricated within the integrated circuit die 502 while in other implementations the communications logic unit 508 is fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 502. The integrated circuit die
10 502 may include a processor 504 as well as on-die memory 506, often used as cache memory, which can be provided by technologies such as embedded DRAM (eDRAM), or SRAM.

In embodiments, the computing device 500 may include a display or a touchscreen display 524, and a touchscreen display controller 526. A display or the
15 touchscreen display 524 may include a FPD, an AMOLED display, a TFT LCD, a micro light-emitting diode (μ LED) display, or others. For example, the touchscreen display 524 may include the TFT 110 shown in Figure 1, the TFT 210 shown in Figure 2(j), or a TFT formed according to the process 300 shown in Figure 3.

Computing device 500 may include other components that may or may not be
20 physically and electrically coupled to the motherboard or fabricated within a SoC die. These other components include, but are not limited to, volatile memory 510 (e.g., dynamic random access memory (DRAM), non-volatile memory 512 (e.g., ROM or flash memory), a graphics processing unit 514 (GPU), a digital signal processor (DSP) 516, a crypto processor 542 (e.g., a specialized processor that executes cryptographic algorithms
25 within hardware), a chipset 520, at least one antenna 522 (in some implementations two or more antenna may be used), a battery 530 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 528, a compass, a motion coprocessor or sensors 532 (that may include an accelerometer, a gyroscope, and a compass), a microphone (not shown), a speaker 534, a camera 536,
30 user input devices 538 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 540 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). The computing device 500 may incorporate further transmission, telecommunication, or radio functionality not already described herein. In some implementations, the computing device 500 includes a radio that is used to communicate
35 over a distance by modulating and radiating electromagnetic waves in air or space. In further implementations, the computing device 500 includes a transmitter and a receiver (or a transceiver) that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space.

5 The communications logic unit 508 enables wireless communications for the transfer of data to and from the computing device 500. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the
10 associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 508 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Infrared (IR), Near
15 Field Communication (NFC), Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 500 may include a plurality of communications logic units 508. For instance, a first communications logic unit 508 may be dedicated to shorter range wireless communications such as Wi-Fi, NFC, and Bluetooth and a second communications logic
20 unit 508 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

 The processor 504 of the computing device 500 includes one or more devices, such as transistors. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic
25 data into other electronic data that may be stored in registers and/or memory. The communications logic unit 508 may also include one or more devices, such as transistors.

 In further embodiments, another component housed within the computing device 500 may contain one or more devices, such as MRAM, or spin-transfer torque memory (STT-MRAM), that are formed in accordance with implementations of the current
30 disclosure, e.g., the memory array 100 shown in Figure 1, the MRAM memory cell 210 shown in Figure 2, or a MRAM memory cell formed according to the process 300 shown in Figure 3.

 In various embodiments, the computing device 500 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a
35 dumbphone, a tablet, a tablet/laptop hybrid, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 500 may be

5 any other electronic device that processes data.

The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various
10 equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

Some non-limiting Examples are provided below.

Example 1 may include a semiconductor device, comprising: a substrate; a gate electrode above the substrate; a gate dielectric layer conformally covering the gate
15 electrode and the substrate; a hydrogen diffusion barrier (HDB) layer above the gate dielectric layer; a channel layer above the HDB layer, wherein the channel layer includes a source area and a drain area; and a source electrode coupled to the source area, and a drain electrode coupled to the drain area.

Example 2 may include the semiconductor device of example 1 and/or some other
20 examples herein, further comprising: another HDB layer above the channel layer, wherein the source electrode is through the another HDB layer and coupled to the source area, and the drain electrode is through the another HDB layer and coupled to the drain area.

Example 3 may include the semiconductor device of example 1 and/or some other examples herein, further comprising: an interlayer dielectric (ILD) layer above the channel
25 layer, wherein the source electrode is through the ILD layer and coupled to the source area, and the drain electrode is through the ILD layer and coupled to the drain area.

Example 4 may include the semiconductor device of any of examples 1-3 and/or some other examples herein, wherein the HDB layer includes TiO_2 , Al_2O_3 , AlN , doped- TiO_2 , or doped- Al_2O_3 .

30 Example 5 may include the semiconductor device of any of examples 1-3 and/or some other examples herein, wherein the channel layer includes zinc (Zn) and oxygen (O).

Example 6 may include the semiconductor device of any of examples 1-3 and/or some other examples herein, wherein the channel layer includes InGaZnO (IGZO), amorphous InGaZnO (a-IGZO), crystal-like InGaZnO (c-IGZO), GaZnON, ZnON, or C-
35 Axis Aligned Crystal (CAAC).

Example 7 may include the semiconductor device of any of examples 1-3 and/or some other examples herein, wherein the channel layer has a thickness in a range of about 10 nm to about 100 nm.

5 Example 8 may include the semiconductor device of any of examples 1-3 and/or some other examples herein, wherein the gate dielectric layer includes silicon oxide (SiO_2), silicon nitride (SiN_x), yttrium oxide (Y_2O_3), silicon oxynitride (SiO_xN_y), aluminum oxide (Al_2O_3), hafnium(IV) oxide (HfO_2), tantalum oxide (Ta_2O_5), or titanium dioxide (TiO_2).

10 Example 9 may include the semiconductor device of any of examples 1-3 and/or some other examples herein, wherein the source electrode or the drain electrode includes titanium (Ti), molybdenum (Mo), gold (Au), platinum (Pt), aluminum (Al), nickel (Ni), copper (Cu), chromium (Cr), or an alloy of Ti, Mo, Au, Pt, Al Ni, Cu, Cr.

15 Example 10 may include the semiconductor device of any of examples 1-3 and/or some other examples herein, wherein the substrate includes a glass substrate, a metal substrate, or a plastic substrate.

20 Example 11 may include a computing device comprising: a processor; a memory device coupled to the processor; and a display coupled to the processor, the display including a transistor, and the transistor including: a substrate; a gate electrode above the substrate; a gate dielectric layer conformally covering the gate electrode and the substrate; a hydrogen diffusion barrier (HDB) layer above the gate dielectric layer; a channel layer above the HDB layer, wherein the channel layer includes a source area and a drain area; and a source electrode coupled to the source area, and a drain electrode coupled to the drain area.

25 Example 12 may include the computing device of example 11 and/or some other examples herein, wherein the transistor further includes: another HDB layer above the channel layer, wherein the source electrode is through the another HDB layer and coupled to the source area, and the drain electrode is through the another HDB layer and coupled to the drain area.

30 Example 13 may include the computing device of example 11 and/or some other examples herein, wherein the transistor further includes: an interlayer dielectric (ILD) layer above the channel layer, wherein the source electrode is through the ILD layer and coupled to the source area, and the drain electrode is through the ILD layer and coupled to the drain area.

35 Example 14 may include the computing device of any of examples 11-13 and/or some other examples herein, wherein the HDB layer includes TiO_2 , Al_2O_3 , AlN, doped- TiO_2 , or doped- Al_2O_3 .

 Example 15 may include the computing device of any of examples 11-13 and/or

5 some other examples herein, wherein the channel layer includes InGaZnO (IGZO), amorphous InGaZnO (a-IGZO), crystal-like InGaZnO (c-IGZO), GaZnON, ZnON, or C-Axis Aligned Crystal (CAAC).

Example 16 may include the computing device of any of examples 11-13 and/or some other examples herein, wherein the computing device is a wearable device or a
10 mobile computing device, the wearable device or the mobile computing device including one or more of an antenna, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, a Geiger counter, an accelerometer, a gyroscope, a speaker, or a camera coupled with the processor.

Example 17 may include a method for forming a semiconductor device, the
15 method comprising: forming a gate electrode above a substrate; forming a gate dielectric layer conformally covering the gate electrode and the substrate; forming a hydrogen diffusion barrier (HDB) layer above the gate dielectric layer; forming channel layer above the HDB layer; forming a source area and a drain area within the channel layer; and forming a source electrode coupled to the source area, and a drain electrode coupled to the
20 drain area.

Example 18 may include the method of example 17 and/or some other examples herein, further comprising: forming another HDB layer above the channel layer, wherein the source electrode is formed through the another HDB layer and coupled to the source area, and the drain electrode is formed through the another HDB layer and coupled to the
25 drain area.

Example 19 may include the method of example 17 and/or some other examples herein, further comprising: forming an interlayer dielectric (ILD) layer above the channel layer, wherein the source electrode is formed through the ILD layer and coupled to the source area, and the drain electrode is through the ILD layer and coupled to the drain area.

30 Example 20 may include the method of example 17 and/or some other examples herein, further comprising: forming a buffer layer above the substrate, and wherein the forming the gate electrode above the substrate includes forming the gate electrode above the buffer layer.

Example 21 may include the method of any of examples 17-20 and/or some other
35 examples herein, wherein the gate dielectric layer includes SiO_2 or SiN_x , and wherein the forming the gate dielectric layer includes forming the gate dielectric layer by plasma enhanced chemical vapor deposition (PECVD) at 100°C to 200°C .

Example 22 may include the method of any of examples 17-20 and/or some other

5 examples herein, wherein the HDB layer includes TiO_2 , Al_2O_3 , AlN , doped- TiO_2 , or doped- Al_2O_3 , and wherein the forming the HDB layer includes forming the HDB layer by physical vapor deposition (PVD), atomic layer deposition (ALD), or chemical vapor deposition (CVD).

10 Example 23 may include the method of any of examples 17-20 and/or some other examples herein, wherein the forming the channel layer includes depositing an amorphous InGaZnO (a-IGZO) film at 25°C to 300°C by radio frequency (RF) sputtering, direct current (DC) sputtering, magnetron sputtering, ALD, plasma enhanced atomic layer deposition (PEALD), or PECVD.

15 Example 24 may include the method of any of examples 17-20 and/or some other examples herein, wherein the forming the channel layer includes simultaneously sputtering InGaZnO (IGZO) and ZnO at a temperature in a range of 25°C to 400°C by radio frequency (RF) sputtering, direct current (DC) sputtering, or magnetron sputtering, to form a crystal-like InGaZnO (c-IGZO) film.

20 Example 25 may include the method of any of examples 17-20 and/or some other examples herein, wherein the channel layer includes InGaZnO (IGZO), amorphous InGaZnO (a-IGZO), crystal-like InGaZnO (c-IGZO), GaZnON , ZnON , or C-Axis Aligned Crystal (CAAC).

25 Various embodiments may include any suitable combination of the above-described embodiments including alternative (or) embodiments of embodiments that are described in conjunctive form (and) above (e.g., the “and” may be “and/or”). Furthermore, some embodiments may include one or more articles of manufacture (e.g., non-transitory computer-readable media) having instructions, stored thereon, that when executed result in actions of any of the above-described embodiments. Moreover, some embodiments may include apparatuses or systems having any suitable means for carrying
30 out the various operations of the above-described embodiments.

The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the embodiments of the present disclosure to the precise forms disclosed. While specific implementations and examples are described herein for illustrative purposes, various equivalent modifications
35 are possible within the scope of the present disclosure, as those skilled in the relevant art will recognize.

These modifications may be made to embodiments of the present disclosure in light of the above detailed description. The terms used in the following claims should not

- 5 be construed to limit various embodiments of the present disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

5

Claims

What is claimed is:

1. A semiconductor device, comprising:
a substrate;
a gate electrode above the substrate;
10 a gate dielectric layer conformally covering the gate electrode and the substrate;
a hydrogen diffusion barrier (HDB) layer above the gate dielectric layer;
a channel layer above the HDB layer, wherein the channel layer includes a source
area and a drain area; and
a source electrode coupled to the source area, and a drain electrode coupled to the
15 drain area.
2. The semiconductor device of claim 1, further comprising:
another HDB layer above the channel layer, wherein the source electrode is
through the another HDB layer and coupled to the source area, and the drain electrode is
20 through the another HDB layer and coupled to the drain area.
3. The semiconductor device of claim 1, further comprising:
an interlayer dielectric (ILD) layer above the channel layer, wherein the source
electrode is through the ILD layer and coupled to the source area, and the drain electrode
25 is through the ILD layer and coupled to the drain area.
4. The semiconductor device of any of claims 1-3, wherein the HDB layer
includes TiO_2 , Al_2O_3 , AlN , doped- TiO_2 , or doped- Al_2O_3 .
- 30 5. The semiconductor device of any of claims 1-3, wherein the channel layer
includes zinc (Zn) and oxygen (O).
6. The semiconductor device of any of claims 1-3, wherein the channel layer
includes InGaZnO (IGZO), amorphous InGaZnO (a-IGZO), crystal-like InGaZnO (c-
35 IGZO), GaZnON, ZnON, or C-Axis Aligned Crystal (CAAC).

5 7. The semiconductor device of any of claims 1-3, wherein the channel layer has a thickness in a range of about 10 nm to about 100 nm.

8. The semiconductor device of any of claims 1-3, wherein the gate dielectric layer includes silicon oxide (SiO_2), silicon nitride (SiN_x), yttrium oxide (Y_2O_3), silicon
10 oxynitride (SiO_xN_y), aluminum oxide (Al_2O_3), hafnium(IV) oxide (HfO_2), tantalum oxide (Ta_2O_5), or titanium dioxide (TiO_2).

9. The semiconductor device of any of claims 1-3, wherein the source electrode or the drain electrode includes titanium (Ti), molybdenum (Mo), gold (Au), platinum
15 (Pt), aluminum (Al), nickel (Ni), copper (Cu), chromium (Cr), or an alloy of Ti, Mo, Au, Pt, Al Ni, Cu, Cr.

10. The semiconductor device of any of claims 1-3, wherein the substrate includes a glass substrate, a metal substrate, or a plastic substrate.
20

11. A computing device comprising:
a processor;
a memory device coupled to the processor; and
a display coupled to the processor, the display including a transistor, and the
25 transistor including:
a substrate;
a gate electrode above the substrate;
a gate dielectric layer conformally covering the gate electrode and the substrate;
30 a hydrogen diffusion barrier (HDB) layer above the gate dielectric layer;
a channel layer above the HDB layer, wherein the channel layer includes a source area and a drain area; and
a source electrode coupled to the source area, and a drain electrode coupled to the drain area.

35 12. The computing device of claim 11, wherein the transistor further includes:

5 another HDB layer above the channel layer, wherein the source electrode is through the another HDB layer and coupled to the source area, and the drain electrode is through the another HDB layer and coupled to the drain area.

13. The computing device of claim 11, wherein the transistor further includes:
10 an interlayer dielectric (ILD) layer above the channel layer, wherein the source electrode is through the ILD layer and coupled to the source area, and the drain electrode is through the ILD layer and coupled to the drain area.

14. The computing device of any of claims 11-13, wherein the HDB layer
15 includes TiO_2 , Al_2O_3 , AlN , doped- TiO_2 , or doped- Al_2O_3 .

15. The computing device of any of claims 11-13, wherein the channel layer includes InGaZnO (IGZO), amorphous InGaZnO (a-IGZO), crystal-like InGaZnO (c-IGZO), GaZnON , ZnON , or C-Axis Aligned Crystal (CAAC).

20 16. The computing device of any of claims 11-13, wherein the computing device is a wearable device or a mobile computing device, the wearable device or the mobile computing device including one or more of an antenna, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS)
25 device, a compass, a Geiger counter, an accelerometer, a gyroscope, a speaker, or a camera coupled with the processor.

17. A method for forming a semiconductor device, the method comprising:
forming a gate electrode above a substrate;
30 forming a gate dielectric layer conformally covering the gate electrode and the substrate;
forming a hydrogen diffusion barrier (HDB) layer above the gate dielectric layer;
forming a channel layer above the HDB layer;
forming a source area and a drain area within the channel layer; and
35 forming a source electrode coupled to the source area, and a drain electrode coupled to the drain area.

5 18. The method of claim 17, further comprising:
 forming another HDB layer above the channel layer, wherein the source electrode
is formed through the another HDB layer and coupled to the source area, and the drain
electrode is formed through the another HDB layer and coupled to the drain area.

10 19. The method of claim 17, further comprising:
 forming an interlayer dielectric (ILD) layer above the channel layer, wherein the
source electrode is formed through the ILD layer and coupled to the source area, and the
drain electrode is through the ILD layer and coupled to the drain area.

15 20. The method of claim 17, further comprising:
 forming a buffer layer above the substrate, and wherein the forming the gate
electrode above the substrate includes forming the gate electrode above the buffer layer.

 21. The method of any of claims 17-20, wherein the gate dielectric layer includes
20 SiO₂ or SiN_x, and wherein the forming the gate dielectric layer includes forming the gate
dielectric layer by plasma enhanced chemical vapor deposition (PECVD) at 100 °C to
200 °C.

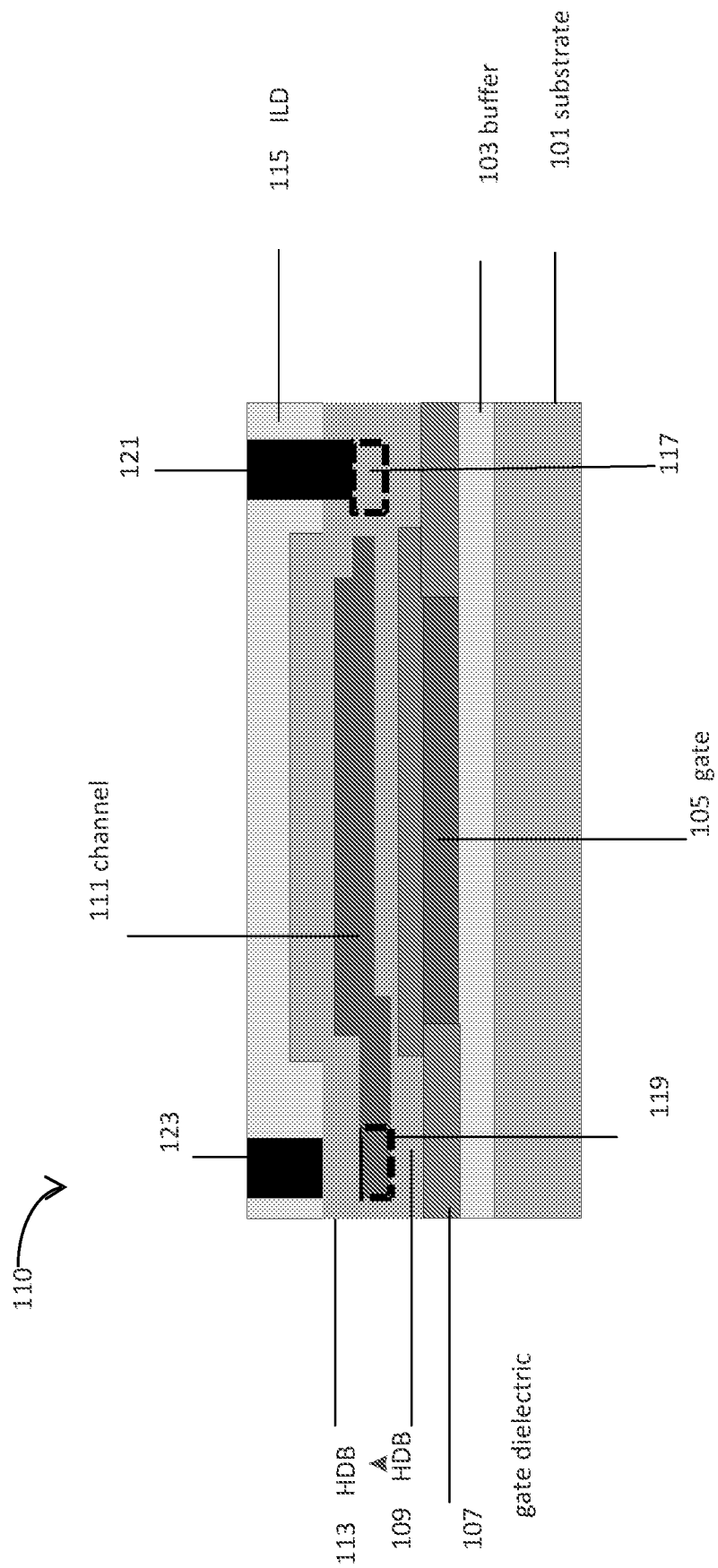
 22. The method of any of claims 17-20, wherein the HDB layer includes TiO₂,
25 Al₂O₃, AlN, doped-TiO₂, or doped-Al₂O₃, and wherein the forming the HDB layer
includes forming the HDB layer by physical vapor deposition (PVD), atomic layer
deposition (ALD), or chemical vapor deposition (CVD).

 23. The method of any of claims 17-20, wherein the forming the channel layer
30 includes depositing an amorphous InGaZnO (a-IGZO) film at 25 °C to 300 °C by radio
frequency (RF) sputtering, direct current (DC) sputtering, magnetron sputtering, ALD,
plasma enhanced atomic layer deposition (PEALD), or PECVD.

 24. The method of any of claims 17-20, wherein the forming the channel layer
35 includes simultaneously sputtering InGaZnO (IGZO) and ZnO at a temperature in a range
of 25 °C to 400 °C by radio frequency (RF) sputtering, direct current (DC) sputtering, or
magnetron sputtering, to form a crystal-like InGaZnO (c-IGZO) film.

- 5 25. The method of any of claims 17-20, wherein the channel layer includes
InGaZnO (IGZO), amorphous InGaZnO (a-IGZO), crystal-like InGaZnO (c-IGZO),
GaZnON, ZnON, or C-Axis Aligned Crystal (CAAC).

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Figure 2(a)

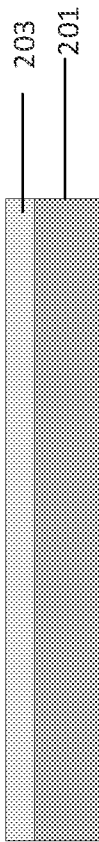


Figure 2(b)

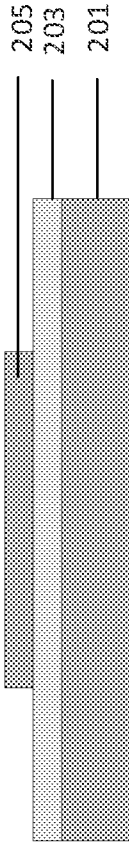


Figure 2(c)

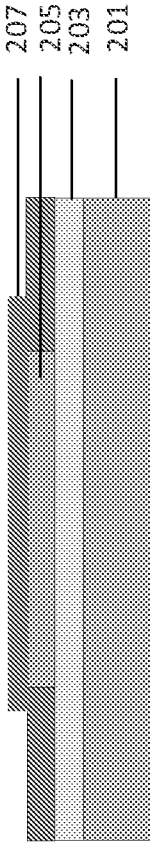
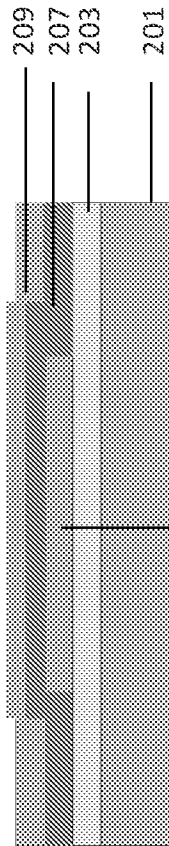


Figure 2(d)



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Figure 2(e)

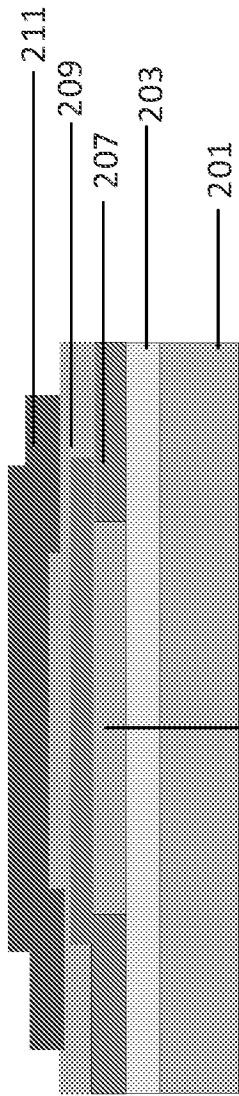


Figure 2(f)

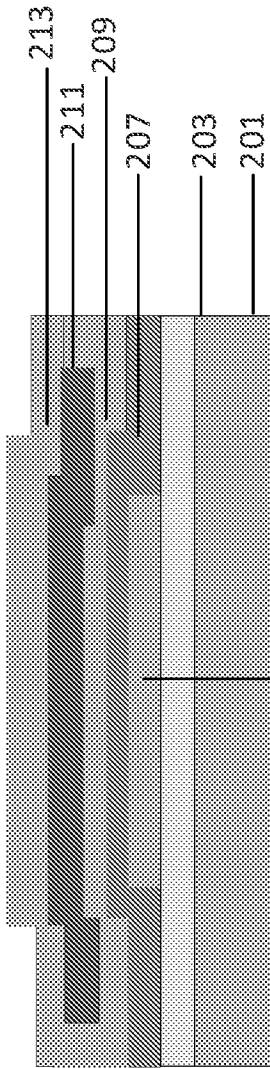


Figure 2(g)

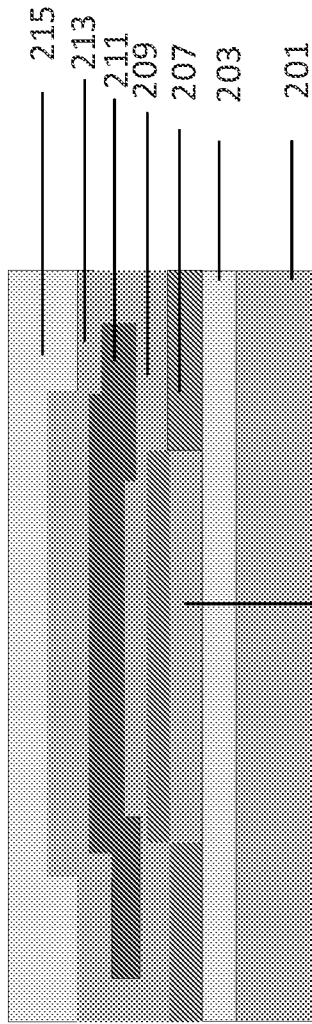


Figure 2(h)

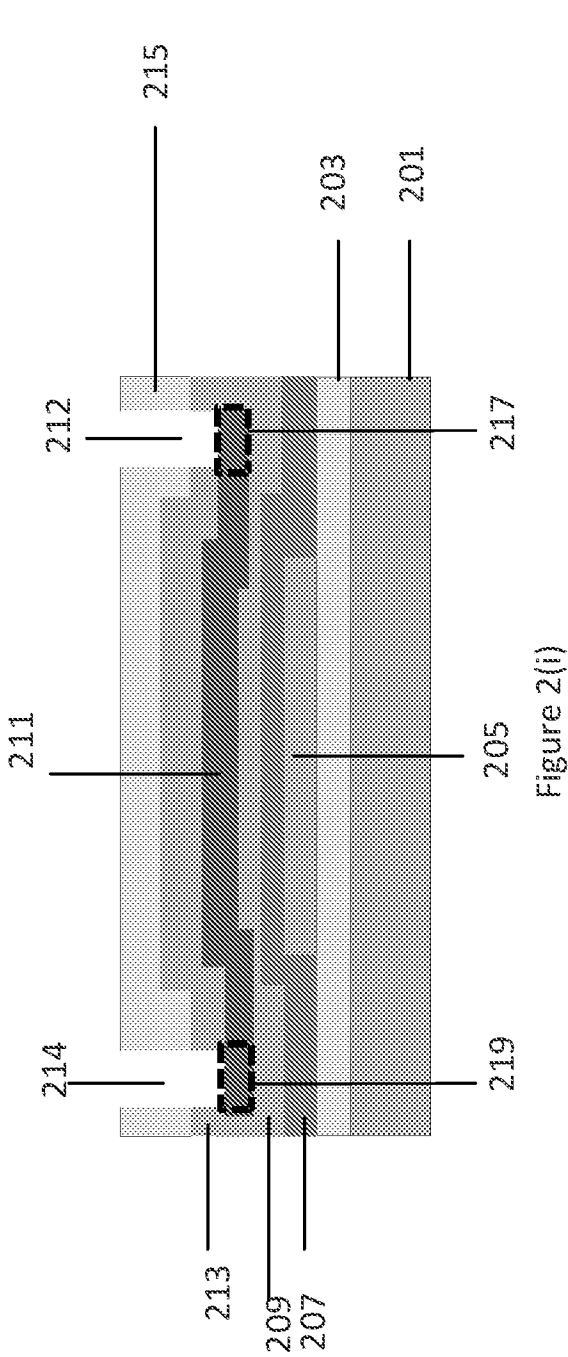


Figure 2(i)

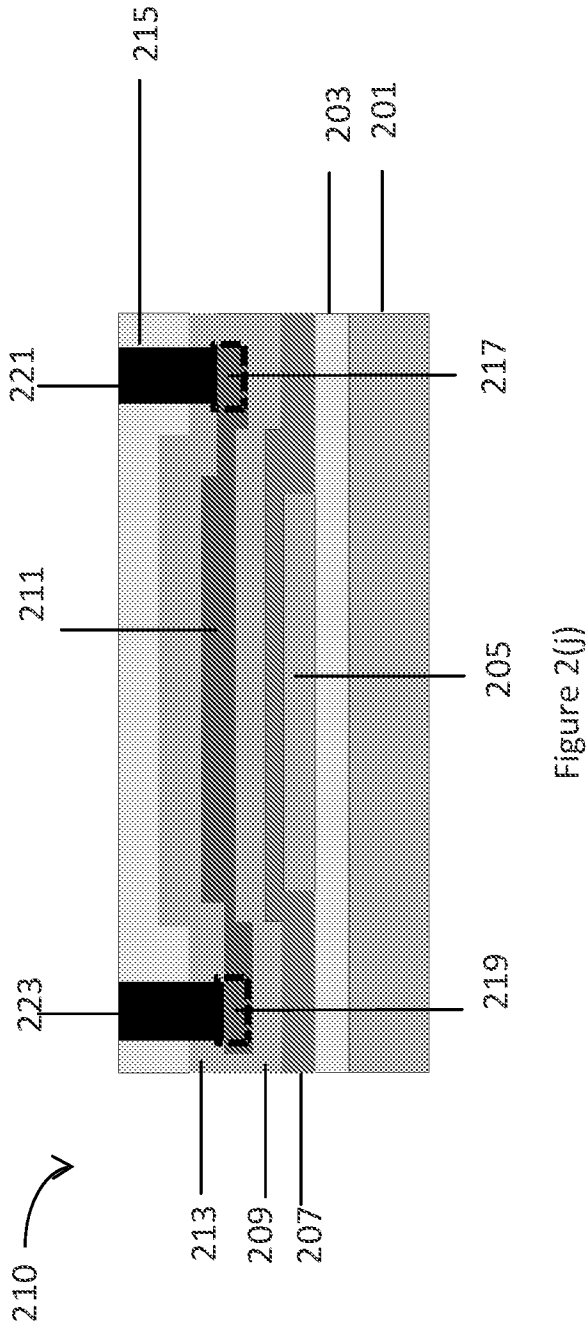


Figure 2(j)

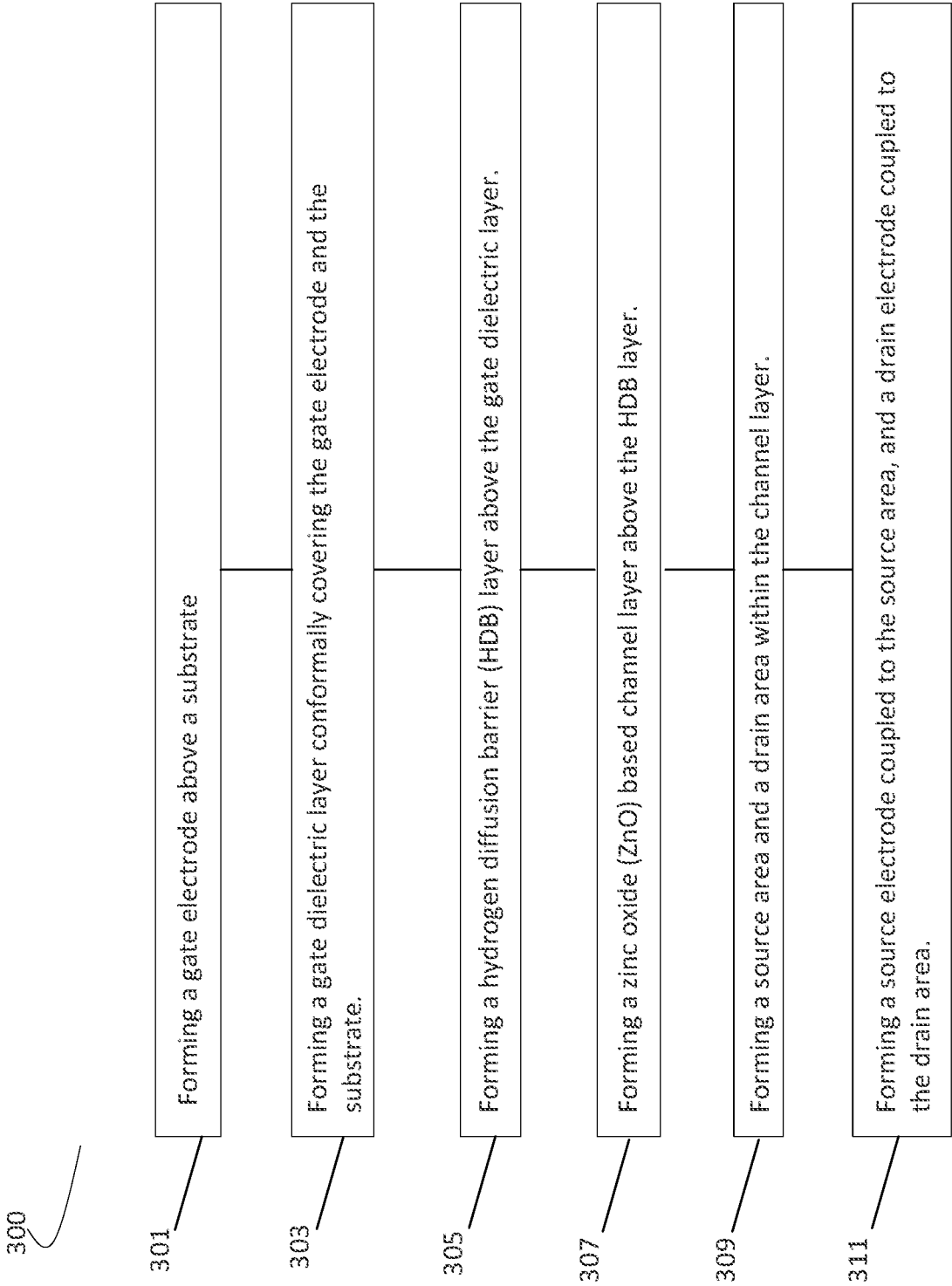


Figure 3

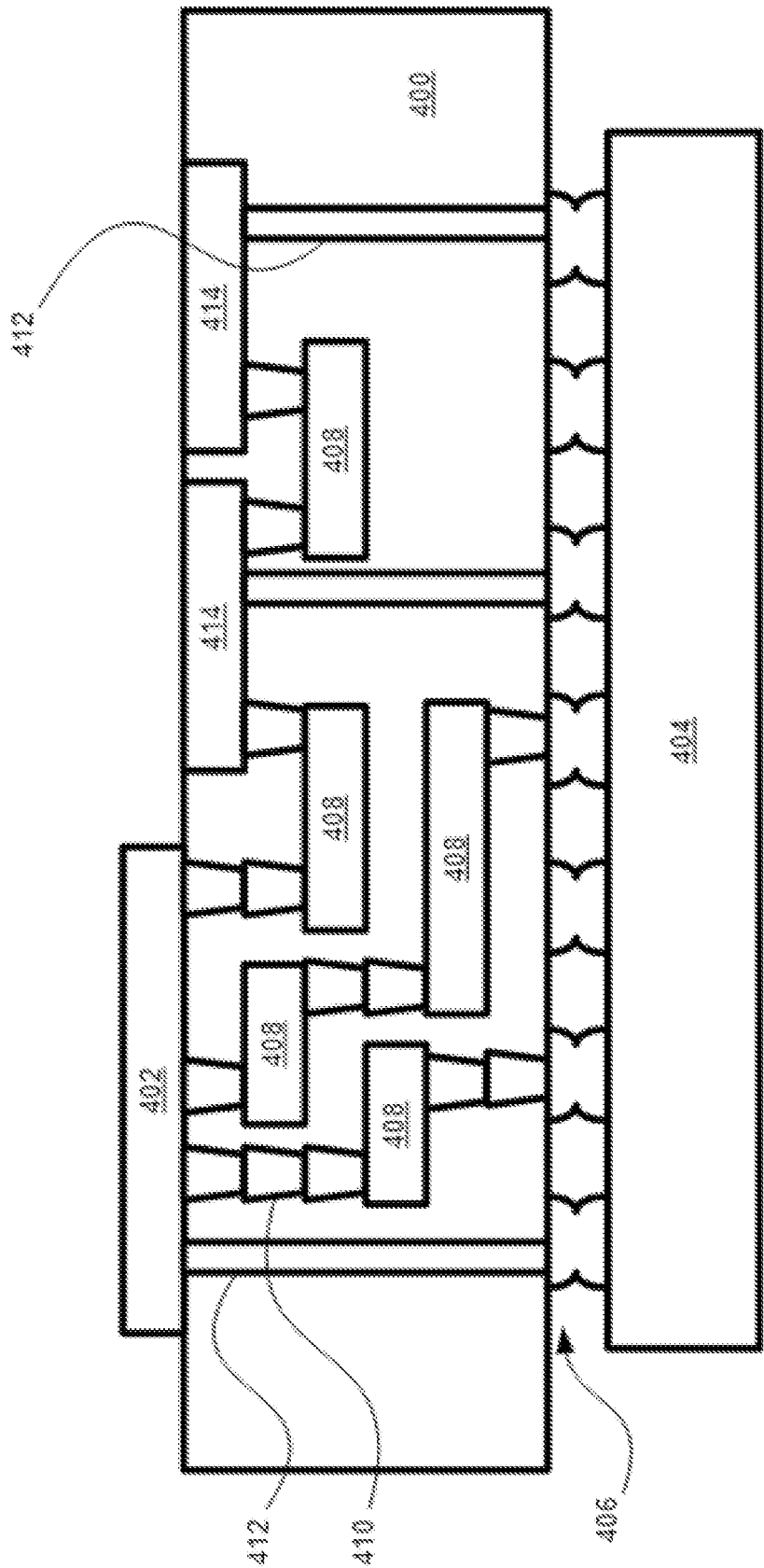


Figure 4

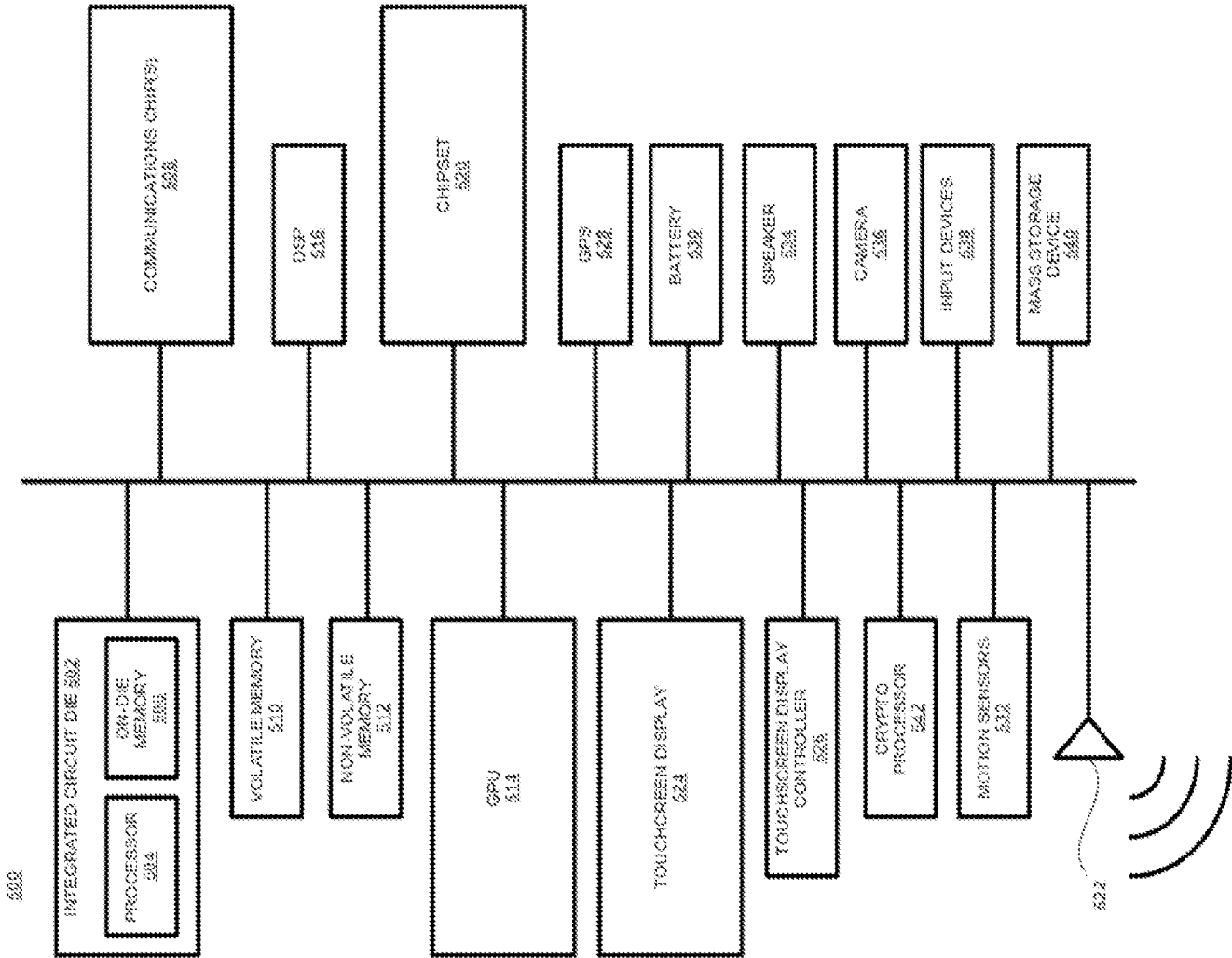


Figure 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/069213**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/786(2006.01)i, H01L 21/02(2006.01)i, H01L 21/768(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/786; H01L 21/336; H01L 23/00; H01L 21/28; H03K 3/01; H01L 21/338; H01L 27/108; H01L 21/02; H01L 21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: transistor, hydrogen diffusion barrier

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0052636 A1 (HYUN-SOO SHIN et al.) 01 March 2012 See paragraphs [0009], [0032]–[0037], [0050] and figure 5.	1–25
Y	US 2016-0149047 A1 (JAPAN DISPLAY INC.) 26 May 2016 See paragraphs [0012]–[0026] and figure 3.	1–25
A	US 2014-0002426 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 02 January 2014 See paragraphs [0104]–[0112] and figures 6A–6B.	1–25
A	US 2011-0136305 A1 (ADAM WILLIAM SAXLER et al.) 09 June 2011 See paragraphs [0061]–[0062] and figure 1F.	1–25
A	US 2005-0161724 A1 (YASUSHI IGARASHI) 28 July 2005 See paragraphs [0045]–[0047] and figure 1.	1–25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

31 August 2017 (31.08.2017)

Date of mailing of the international search report

31 August 2017 (31.08.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

KANG, Sung Chul

Telephone No. +82-42-481-8405



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/069213

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0052636 A1	01/03/2012	KR 10-0873081 B1 KR 10-2008-0104756 A US 2008-0303020 A1 US 8053773 B2 US 8871566 B2	09/12/2008 03/12/2008 11/12/2008 08/11/2011 28/10/2014
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