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(54) **PROGRAMMABLE TRANSMITTER AND RECEIVER INCLUDING DIGITAL RADIO FREQUENCY MEMORY**

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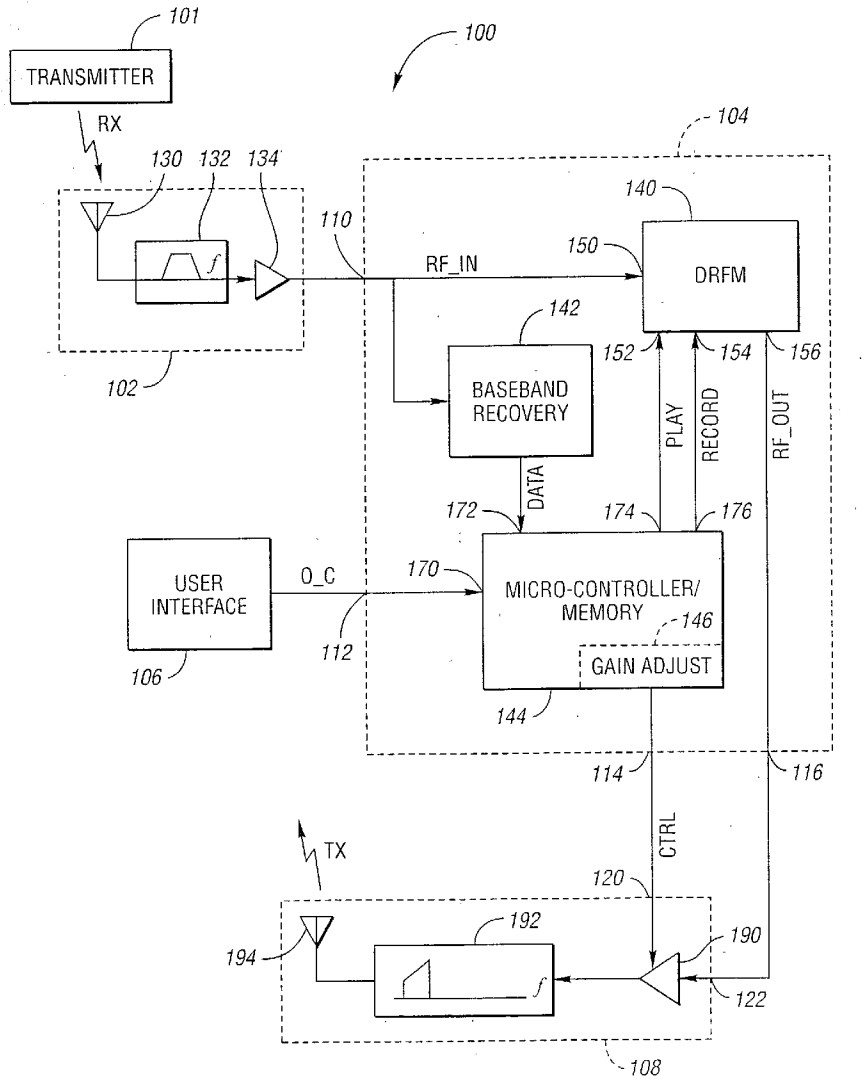
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(57) **ABSTRACT**

A vehicular programmable transceiver includes a digital radio frequency memory (DRFM) having at least one register configured to sample and hold a radio frequency input signal in response to a clock signal and to generate an output signal having a carrier frequency generated in response to the sampled and held input signal.



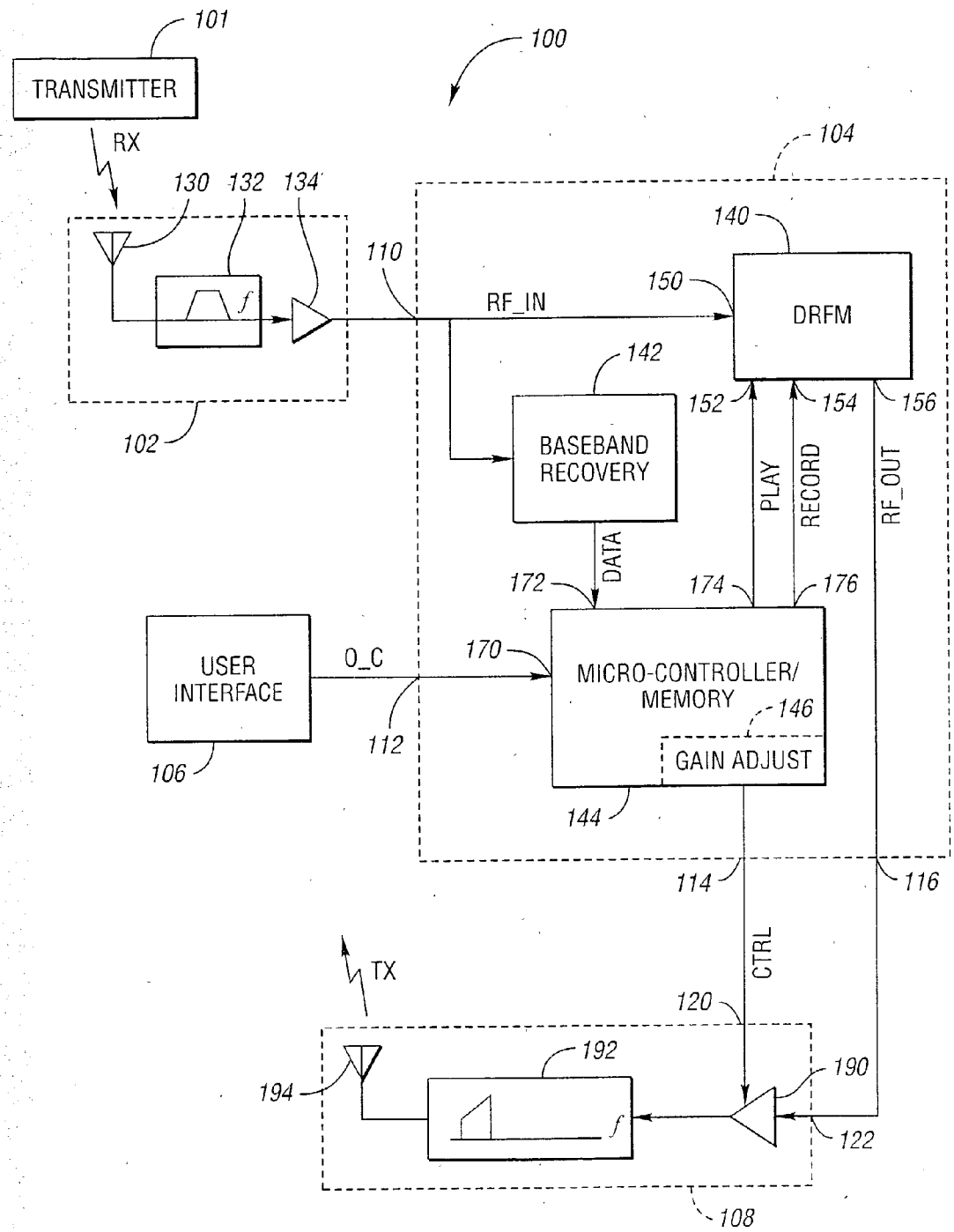

101
TRANSMITTER
RX
100
104
130
132
134
110
140
150
DRFM
RF_IN
142
BASEBAND RECOVERY
152
154
156
PLAY
RECORD
RF_OUT
102
DATA
172
174
176
USER INTERFACE
O_C
170
MICRO-CONTROLLER/ MEMORY
146
GAIN ADJUST
106
112
144
114
116
CTRL
TX
120
192
190
194
122
108

Fig. 1

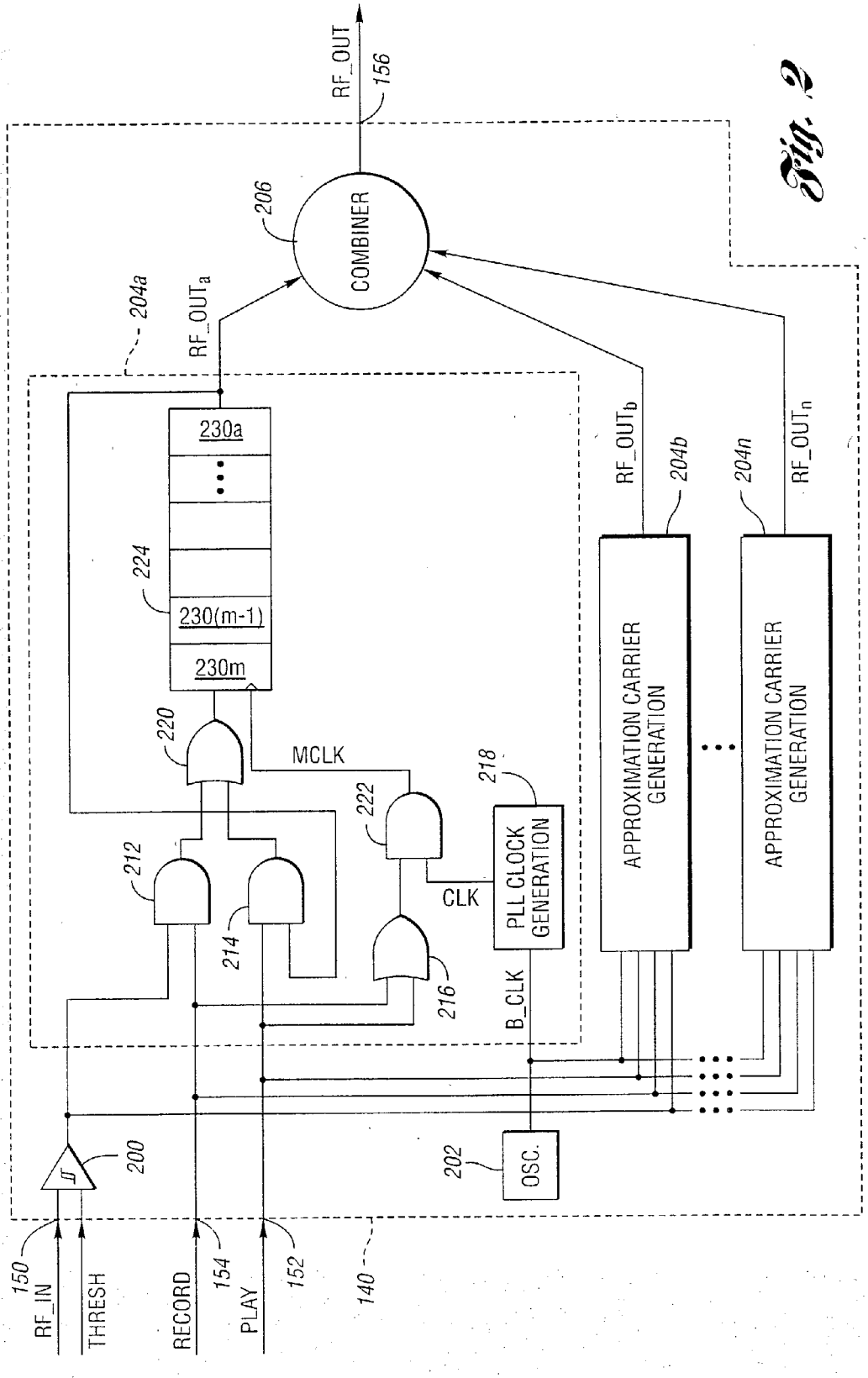

RF_OUT
156
206
COMBINER
204a
RF_OUT$_a$
230a
224
230(m-1)
230m
220
MCLK
222
218
212
214
216
CLK
PLL CLOCK GENERATION
B_CLK
RF_OUT$_b$
204b
204n
RF_OUT$_n$
APPROXIMATION CARRIER GENERATION
APPROXIMATION CARRIER GENERATION
200
202
OSC.
150
RF_IN
THRESH
RECORD
154
PLAY
152
140

Fig. 2

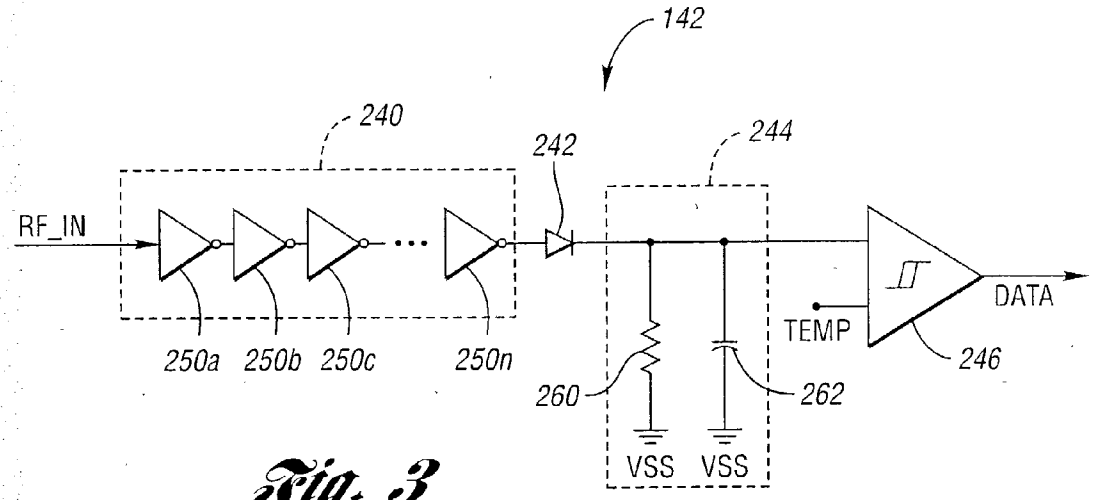

142
240
242
244
RF_IN
250a
250b
250c
250n
260
262
VSS
VSS
TEMP
DATA
246

Fig. 3

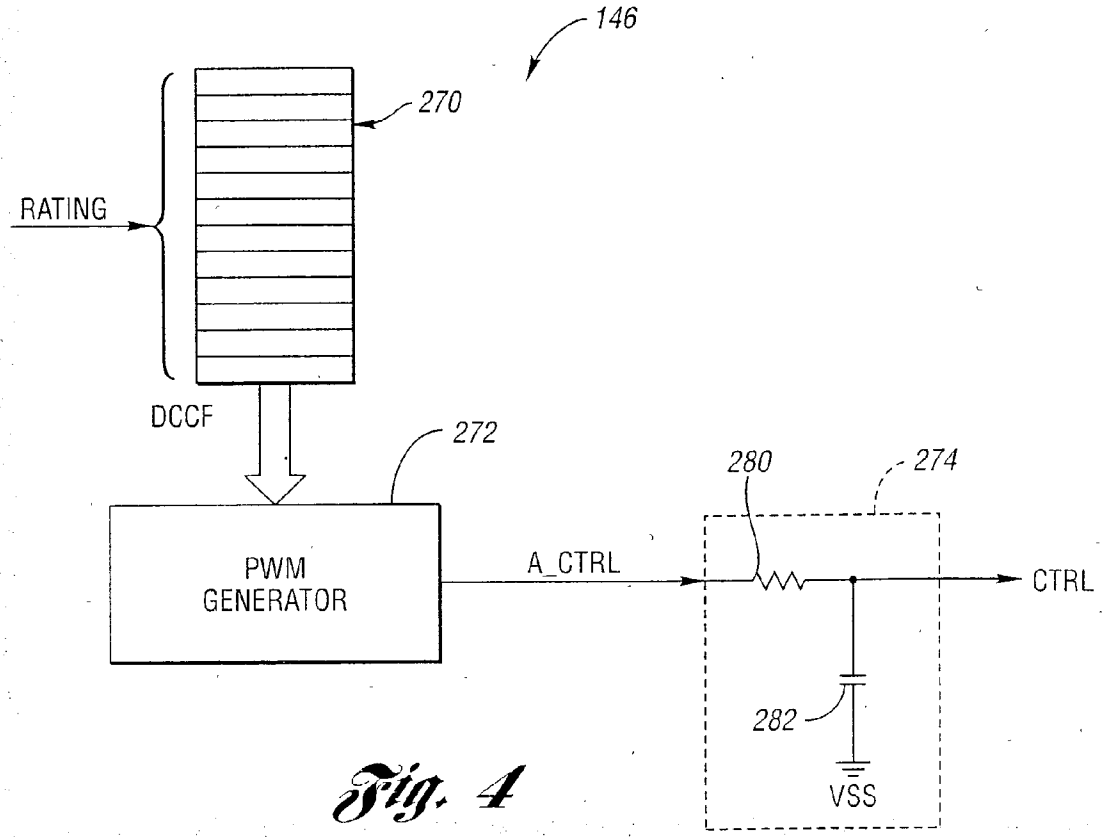

146
270
RATING
DCCF
272
280
274
PWM
GENERATOR
A_CTRL
CTRL
282
VSS

Fig. 4

PROGRAMMABLE TRANSMITTER AND RECEIVER INCLUDING DIGITAL RADIO FREQUENCY MEMORY

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to programmable transmitters and receivers.

[0003] 2. Background Art

[0004] Electrically operated appliances such as garage door opening (and closing) mechanisms are an increasingly popular home convenience. Such electrically operated appliances typically implement a battery operated transmitter and receiver (i.e., transceiver) remote control that transmits an encoded radio frequency (RF) signal to a receiver in the appliance. For example, a garage door opener transceiver in a vehicle transmits the coded signal to the receiver in the garage when a driver or passenger presses a button on the transceiver. Multiple transceivers are often purchased so that a number of vehicles can access the garage. Some types of transceivers may be programmed by the owner to operate a particular garage door mechanism (i.e., the transceivers are programmed to operate with the receiver in the owner's garage). The programming typically includes receiving the control signal from a previously programmed transceiver and storing the control signal for future transmissions.

[0005] A conventional programmable transceiver is typically implemented as a number of components and/or circuits on multiple circuit boards that can result in a bulky and cumbersome transceiver. The conventional transceiver can be slow to program. The slow programming can cause user frustration and dissatisfaction. Furthermore, component drift over time and with temperature changes can cause the conventional transceiver to drift off the proper frequency. When the conventional transceiver drifts off the proper frequency, the transceiver can become nonfunctional until reprogrammed. The multiple component and circuit board structure of conventional transceivers can be more susceptible to breakage when dropped than a single circuit board approach.

[0006] Thus, there exists a need for a programmable transceiver that has reduced circuit board area and/or cost when compared to conventional approaches, programs more quickly, is more resistant to breakage when dropped, and is more stable over changes in temperature and over time than conventional approaches.

SUMMARY OF THE INVENTION

[0007] Accordingly, the present invention provides an improved programmable transceiver including a digital radio frequency memory where the transceiver has reduced circuit board area, quicker programming, greater resistance to breakage, and more temperature and time stability than conventional approaches.

[0008] According to the present invention, a vehicular programmable transceiver is provided comprising a digital radio frequency memory (DRFM) having at least one register configured to sample and hold a radio frequency input signal in response to a clock signal, and to generate an output signal having a carrier frequency generated in response to the sampled and held input signal.

[0009] Also according to the present invention, for use in a home appliance remote control, a programmable transceiver is provided comprising a digital radio frequency memory (DRFM) configured to hold samples of an input signal during a programming operation, and to generate an output signal having a carrier during a transmit operation, wherein the carrier is shifted out of the DRFM.

[0010] Still further according to the present invention, for use in a programmable transceiver, a method for generating an output signal is provided. The method generally comprises sampling a radio frequency input signal, holding the sampled signal in at least one buffer, shifting from the buffer a carrier signal, and controlling an amplitude of the carrier signal to generate the transceiver output signal.

[0011] Still further according to the present invention, a method of remotely controlling a garage door opener that is remotely controlled by an existing transmitter is provided, the existing transmitter transmitting a signal comprising a carrier modulated by a code, the method comprising receiving the signal, detecting the code, sampling the signal at a time determined by the detected code, storing the sampled signal, receiving a request to remotely control the garage door opener, generating a carrier approximation by playing the stored sampled signal, controlling an amplitude of the carrier approximation, and transmitting the generated carrier approximation.

[0012] Still further according to the present invention, a programmable remote garage door opener is provided comprising a receiver, a detector, a transmitter, at least one register, and control logic. The receiver may be implemented for receiving a received signal comprising a received carrier modulated with a received code. The detector may be implemented for detecting the received code in the received signal. The transmitter may be implemented for transmitting an output signal. The at least one register may be implemented for holding a plurality of samples of the received signal. The control logic may be operative to determine when the received code is detected, signal the at least one register to sample and store the received signal based on detecting the received code, receive a request to transmit a remote control command, signal the at least one register to present the stored signal to the transmitter, and signal the transmitter to control an amplitude of the stored signal presented by the at least one register thereby generating the output signal.

[0013] The above features, and other features and advantages of the present invention are readily apparent from the following detailed descriptions thereof when taken in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] **FIG. 1** is a diagram of a transceiver according to an embodiment of the present invention;

[0015] **FIG. 2** is a diagram of a digital radio frequency memory of **FIG. 1**;

[0016] **FIG. 3** is a diagram of a baseband data recovery circuit of **FIG. 1**; and

[0017] **FIG. 4** is a diagram of a power output control circuit of **FIG. 1**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[0018] With reference to the Figures, the preferred embodiments of the present invention will now be described in detail. Generally, the present invention provides an improved method and system for a programmable transmitter and receiver (i.e., transceiver) including a digital radio frequency memory. In one example, the transceiver of the present invention may be implemented in connection with a vehicular home appliance remote control such as a garage door opener/closer system remote control. However, the transceiver of the present invention may be implemented in connection with any appropriate system and apparatus to meet the design criteria of a particular application.

[0019] Referring to **FIG. 1, a** diagram illustrating a programmable transceiver **100** in accordance with a preferred embodiment of the present invention is shown. The transceiver **100** generally receives a signal (e.g., RX) in at least one mode of operation and transmits a signal (e.g., TX) in at least one other mode of operation.

[0020] The signal RX is typically an encoded radio frequency (RF) on/off key (OOK) modulated signal that is asserted to control at least one operation (e.g., opening and closing a garage door). The signal RX may, however, be implemented as a continuously amplitude modulated (AM) signal, or the like, as appropriate to meet the design criteria of a particular application. The signal RX is generally transmitted by an existing transmitter **101**. The signal RX is generally transmitted to the transceiver **100** in connection with a programming operation for the transceiver **100**.

[0021] The signal TX may be a control signal transmitted by the transceiver **100**. The signal TX is generally similar to the signal RX. The signal TX is generally transmitted in connection with a transmit (i.e., normal) mode of operation of the transceiver **100** (e.g., when a user desires (or makes a request) to open or close a respective garage door, turn on or off at least one light, operate at least one appliance, etc.). However, other transmit and receive operations are within the scope of the present invention.

[0022] The transceiver **100** generally comprises an input or receiver circuit (or block) **102**, a controller circuit (or block) **104**, a user interface circuit (or block) **106**, and an output or transmitter circuit (or block) **108**. The input block **102** may have an input that may receive the signal RX and an output that may present a signal (e.g., RF_IN). The signal RF_IN is generally a filtered version of the signal RX.

[0023] The controller block **104** may have an input **110** that may receive the signal RF_IN, an input **112** that may receive at least one signal (e.g., O_C), an output **114** that may present a signal (e.g., CTRL), and an output **116** that may present a signal (e.g., RF_OUT). The signal O_C may be implemented as at least one control signal that is asserted to control at least one operation (e.g., programming, door opening, door closing, lights on, lights off, appliance on, appliance off, etc.) related to the transceiver **100**. The signal CTRL may be implemented as an output control signal that is configured to control at least one parameter (e.g., amplitude) of an output signal that is generated by the transceiver **100** (e.g., the signal TX). The signal RF_OUT may be implemented as a radio frequency carrier or carrier signal. The signal RF_OUT is generally a carrier approximation (i.e., an approximation to the carrier that corresponds to the signal RF_IN). In an embodiment of the present invention, the signal RF_OUT is an OOK RF signal.

[0024] The user interface block **106** may have an output that may present the at least one signal O_C. The user interface **106** generally comprises at least one signal activation device such as a button switch that may activate the generation and assertion of the signal O_C in response to a user action. For example, the signal O_C may be asserted when the user pushes a button switch (not shown) on the user interface **106**. The user interface **106** may further comprise at least one indicator (not shown) such as an LED that may indicate when the signal O_C is asserted, modes of operation of the transceiver **100**, etc.

[0025] The output block **108** may have an input **120** that may receive the signal CTRL, an input **122** that may receive the signal RF_OUT, and an output that may present the signal TX. In one embodiment, the signal TX is a modulated and filtered version of the signal RF_OUT. In another embodiment, the signal TX is a filtered version of the OOK signal RF_OUT. The signal TX is generally a signal approximation of the signal RX. The block **108** may further buffer and filter the signals RF_OUT and TX.

[0026] The input block **102** generally comprises an antenna **130** that may receive the signal RX and that may be serially connected to a filter **132**. The filter **132** may be serially connected to an amplifier **134**. The filter **132** may be implemented as a band limit filter that is configured to pass the signal RX only within a predetermined frequency range. The amplifier **134** may be implemented as a gain block (or input buffer) that is configured to provide gain to and/or buffer the signal RX and, thereby, generate the signal RF_IN.

[0027] The controller block **104** generally comprises at least one storage device such as a digital radio frequency memory (DRFM) circuit (or block) **140**, a baseband recovery (or detector) circuit (or block) **142**, and a micro-controller/memory circuit (or block) **144** that may include a gain control circuit (or block) **146**. The DRFM **140** may have an input **150** that may receive the signal RF_IN, an input **152** that may receive a signal (e.g., PLAY), an input **154** that may receive a signal (e.g., RECORD), and an output **156** that may present the signal RF_OUT.

[0028] The signals PLAY and RECORD are generally implemented as digital control signals as described below. The DRFM **140** is generally configured to determine and store a portion of the signal RF_IN, or a signal derived from the signal RF_IN and playback the stored signal (e.g., as the signal RF_OUT) in response to the signals RF_IN, PLAY, and RECORD.

[0029] The baseband recovery circuit **142** may have an input that may receive the signal RF_IN and an output that may present a signal (e.g., DATA). The signal DATA generally comprises the baseband data of the signal RF_IN. The signal DATA generally corresponds to the code that encodes the signal RF_IN. In one example, the signal DATA may be implemented as a binary signal. In another example (not shown), the signal DATA may be implemented as a con-

tinuous signal. The baseband recovery circuit **142** is generally configured to extract the baseband data (e.g., the signal DATA) from the signal RF_IN. The baseband recovery circuit **142** generally detects (i.e., demodulates, determines, etc.) the code that encodes the signal RF_IN (i.e., the signal DATA). The baseband recovery circuit **142** may be configured to generate the signal DATA in response to the signal RF_IN. When the signal DATA is implemented as a continuous signal, the baseband recovery circuit **142** generally includes an analog-to-digital converter (ADC) for converting the decoded analog signal into digital values.

[**0030**] The micro-controller **144** may have an input **170** that may receive the signal O_C, an input **172** that may receive the signal DATA, an output **174** that may present the signal PLAY, an output **176** that may present the signal RECORD, and an output that may present the signal CTRL. The micro-controller **144** generally comprises control logic configured (or operative) to control (or signal) the at least one operation of the transceiver **100**. The baseband recovery circuit **142** and the micro-controller **144** are generally configured to identify, filter, decode and store at least one baseband signal DATA (i.e., detect the code that encodes the signal RF_IN) in response to the signals O_C and RF_IN during a sampling operation (or mode) of the transceiver **100**.

[**0031**] The micro-controller **144** is generally configured to generate and assert the signal RECORD during the sampling mode. The micro-controller **144** generally does not present the signal RECORD unless a valid signal DATA is detected (i.e., the signal RF_IN has a valid encoding). The signal RECORD is then asserted for a period of time long enough to record (e.g., store) at least one portion of the carrier in the signal RF_IN. The micro-controller **144** is generally configured to generate and assert the modulating signal PLAY during a transmit operation (or mode) of the transceiver **100**. The power control (or gain adjust) circuit **146** is generally configured to generate the signal CTRL in response to the signal DATA.

[**0032**] The output block **108** generally comprises an amplifier **190** that may have a signal input that may receive the signal RF_OUT, a control input that may receive the signal CTRL, and an output that may be serially connected to a filter **192**. The filter **192** may be serially connected to an antenna **194**. The antenna **194** generally presents (e.g., transmits, broadcasts, etc.) the signal TX. The amplifier **190** may be implemented as a controlled gain block that is configured to provide gain and modulation (i.e., control) to the signal RF_OUT and, thereby, generate the signal TX. The amplifier **190** may be configured to generate the signal TX in response to the carrier frequency signal RF_OUT and the amplitude control (or adjust) signal CTRL. Alternatively, the signal CTRL may control only the gain of an OOK AM signal RF_OUT. The amplifier **190** may be configured to adjust the signal RF_OUT gain as a function of (e.g., in response to) the signal duty cycle of a data code carried by TX.

[**0033**] The filter **192** may be implemented as a clean-up filter that is configured to limit the signal TX to a predetermined frequency range, and reduce or eliminate spurious components of the signal TX. The filter **192** may also be configured to transmit greater power at higher frequencies than at lower frequencies, or as otherwise required to provide the maximum output power permitted by regulations. This permits output power to be based on the spectral characteristics of TX without any knowledge of those characteristics by transceiver **100**. Receive antenna **130** and transmit antenna **194** may be implemented as the same element or as separate antennae.

[**0034**] The present invention may be implemented in a variety of manners within the scope of the present invention. In one example, the blocks **140**, **142** and **190** may be manufactured as a single integrated circuit (e.g., an application specific integrated circuit (ASIC) chip) or on a single circuit board. The single integrated circuit or single circuit board implementation of the blocks **140**, **142** and **190** may provide a more robust (e.g., more resistant to breakage when dropped) transceiver **100** than conventional transceiver approaches. The single integrated circuit or single circuit board implementation of the blocks **140**, **142** and **190** may have reduced area and cost when compared to conventional approaches. The controller **144** may be implemented as a microprocessor together with or separate from other elements of the system **100**.

[**0035**] Referring to **FIG. 2, a** diagram illustrating an embodiment of the DRFM **140** is shown. The DRFM **140** generally comprises a comparator **200**, an oscillator **202**, at least one approximation carrier generation circuit **204** (e.g., circuits **204***a*-**204***n*), and a combiner **206**. Each circuit **204** generally comprises an AND gate **212**, an AND gate **214**, an OR gate **216**, a phase locked loop (PLL) clock circuit **218**, an OR gate **220**, an AND gate **222**, and a shift register (or buffer) **224**. While the gates **212**, **214**, **216**, **220**, and **222** have been shown as specific types of logic gates, any appropriate logic gates may be implemented to meet the design criteria of a particular application.

[**0036**] The number of approximation carrier generation circuits **204** (i.e., the value of n) implemented in a particular design is generally determined by the level of widely spaced spurious emissions that are allowed in connection with the transmitter signal RF_OUT. Generally, the lower the allowed level of spurious emissions, the larger the value of n (i.e., the greater the number of circuits **204**). Multiple (i.e., a plurality of) circuits **204** generally have outputs connected to the combiner **206**. In addition, multiple circuits **204** may be independently controlled to save and generate carriers of differing frequencies for FM transmission.

[**0037**] The comparator **200** may have a first input that may receive the signal RF_IN, a second input that may receive a signal (e.g., THRESH), and an output that may be connected to a first input of each AND gate **212**. The comparator **200** is generally used to change the analog signal RF_IN to a binary signal. The output of the comparator **200** is, thus, generally a pseudo-square wave signal having, on average, substantially the same fundamental frequency as the carrier frequency in the received signal RX (or the signal RF_IN). The signal THRESH may be implemented as a threshold level (or value). The threshold level THRESH may be selected (or determined) to be approximately an average of a DC level of the analog signal RF_IN. As such, the signal THRESH may ensure that the binary version of the signal RF_IN presented by the comparator **200** to each AND gate **212** is approximately a square wave.

[**0038**] In another example (not shown), the circuit **140** may be implemented without the comparator **200** and the

signal THRESH. The signal RF_IN may be presented directly to the first input of each AND gate **212**.

[**0039**] The AND gate **212** may have a second input that may receive the signal RECORD and an output that may be connected to a first input of the OR gate **220**. The AND gates **214***a*-**214***n* may have a first input that may receive the signal PLAY, a second input that may receive the signals RF_OUTa-RF_OUTn, respectively (or the signal RF_OUT as a feedback signal presented by the respective register **224**), and an output that may be connected to a second input of the OR gate **220**. The OR gate **216** may have first and second inputs that may receive the signals RECORD and PLAY, respectively, and an output that may be connected to a first input of the AND gate **222**.

[**0040**] In one example, the oscillator **202** may be implemented as a crystal controlled oscillator. However, the oscillator **202** may be implemented as any appropriate clock to meet the design criteria of a particular application. The oscillator **202** may have an output that may present a base (or reference) clock signal (e.g., B_CLK) to an input of each respective PLL clock circuit **218**. The PLL clock **218** may have an output that may present a signal (e.g., CLK). The PLL clock **218** may be configured to generate the signal CLK in response to the reference clock signal B_CLK. The signal CLK may have the same, a multiple of, or a dividend frequency relative to the frequency of the signal B_CLK.

[**0041**] The signal CLK may be implemented as a sampling clock signal. The signal CLK may be generated at an over-sampling frequency relative to any expected carrier frequency of the signal RF_IN. The clock signals CLKa-CLKn generated within each respective circuit **204***a*-**204***n* may be generated having substantially similar but not necessarily substantially the same frequency. The signals CLKa-CLKn may be generated having frequencies that differ within a range of, for example, 0% to 2%. The frequency of the signal CLK may be an over-sampling frequency. When the signal CLK has an over-sampling frequency, the clock signal CLK is typically generated at a frequency that is at least 2.5 times the highest expected carrier frequency of the signal RF_IN. For example, when the carrier frequency of the signal RF_IN is expected in the range of 300 MHZ-400 MHZ, the clock signal CLK may be generated at a frequency of 1.2 GHz. However, the clock signal CLK may be generated having any appropriate frequency to meet the design criteria of a particular application. For example, the signal CLK may be implemented as a sampling-frequency or under-sampling system clocking signal.

[**0042**] The output of the OR gate **220** may be connected to an input of the register **224**. The signal presented by the OR gate **220** to the register **224** is generally a digitized representation of the signal RF_IN. The AND gate **222** may have a second input that may receive the signal CLK and an output that may present a clock signal (e.g., MCLK) to a clock input of the register **224**. The shift register **224** is generally clocked (i.e., the signal RF_IN is generally sampled and held) at the frequency of the signal MCLK. The shift register **224** is generally configured to shift in samples of the signal RF_IN, store (or save) the samples of the signal RF_IN as a binary sequence, and shift out samples of the signal RF_IN (i.e., stored data) to generate and present the carrier approximation signal RF_OUT (e.g., signals RF_OUTa-RF_OUTn) in response to the clock signal MCLK.

[**0043**] Each shift register **224** generally comprises a plurality of storage fields (e.g., flip-flops, capacitors, or the like) **230***a*-**230***m*, where m is a number of sufficient size such that at least one cycle of the carrier signal in RF_IN is generally sampled and held (or stored). However, typically more than one cycle is stored. The fields **230** may be configured to store (or hold) consecutive (or successive) bits of the digitized signal RF_IN in response to the clock signal MCLK. For example, in the case of the clock signal MCLK having a frequency of 1.2 GHz, a shift register **224** where m equals 3000 (i.e., having three thousand of the fields **230**) may hold 2.5 μs of data of the signal RF_IN.

[**0044**] The combiner **206** is generally configured to combine the outputs of the circuits **204** (i.e., the signals RF_OUTa-RF_OUTn) to generate the signal RF_OUT. Since the signals CLKa-CLKn are generated via independent PLL clock circuits (i.e., the clocks **218***a*-**218***n*), the signals CLKa-CLKn are generally phase locked to a common reference (i.e., the signal B_CLK). In one example, the combiner **206** may be implemented as a linear averager that is configured to average the respective clocked outputs of the registers **224***a*-**224***n* substantially equally to generate the signal RF_OUT. In another example, the combiner **206** may be implemented as a weighted averager that is configured to average the respective clocked outputs of the registers **224***a*-**224***n* per a predefined (e.g., binary, exponential, time-averaged, etc.) weighting to generate the signal RF_OUT. In yet another example, the combiner **206** may be implemented as a summer that adds the respective clocked outputs of the registers **224***a*-**224***m*. However, the combiner **206** may be implemented as any appropriate circuit to meet the design criteria of a particular application.

[**0045**] The digitized signal RF_IN is generally clocked into the register **224** (e.g., sampled and held) in response to the control signal RECORD and the over-sampling clock signal MCLK during the sampling operation. The digitized, sampled signal RF_IN is generally shifted (or clocked) out of the register **224** as the signal RF_OUT in response to the control signal PLAY and the clock signal MCLK during the transmit (or normal) operation. Since the DRFM **140** generally samples and holds the digitized signal RF_IN and shifts out the signal RF_OUT in response to the over-sampling clock signal MCLK, the transceiver **100** is generally less prone to becoming de-programmed over time due to component aging and due to temperature sensitivity as in conventional approaches. The reduction or elimination of wait time from transmission of the signal TX from the time the signal O_C is presented may provide for more rapid programming of the transceiver **100** than conventional approaches. In addition, the signal PLAY may be used to directly generate an OOK signal (e.g., the signal TX) without having to modulate an existing carrier (e.g., by turning on and off the shifting out of the signal RF_OUT from the circuit **204**).

[**0046**] Referring to **FIG. 3, a** diagram illustrating the baseband recovery block **142** is shown. The block **142** generally comprises a gain stage (or block) **240**, a diode **242**, a filter circuit (or block) **244**, and a comparator **246** that are serially connected. The gain stage **240** generally receives

and presents the signal RF_IN. The gain stage **240** generally comprises at least one CMOS inverter **250** (e.g., serially connected inverters **250***a*-**250***n*), where n is a value such that the gain stage **240** provides sufficient amplification and successive inversion of the signal RF_IN to meet the design criteria of a particular application.

[**0047**] The diode **242** may have an anode terminal that may receive the signal RF_IN and a cathode terminal that may be connected to an input of the filter **244**. The filter **244** generally comprises a resistance **260** and a capacitance **262**. The resistance **260** and the capacitance **262** may each have a first terminal that may be connected to a first input (e.g., a data input) of the comparator **246** and a second terminal that may be connected to a ground potential (e.g., VSS).

[**0048**] The comparator **246** may have a second input (e.g., a threshold input) that may receive a signal (e.g., TEMP) and an output that may present the signal DATA. In one example, the comparator **246** may be implemented as a comparator having a temperature compensated threshold. The signal TEMP may be implemented as a temperature compensation threshold level. The trigger level of the comparator **246** as selected or determined via the signal TEMP is generally selected (e.g., via the micro-controller **144**) to reduce or eliminate temperature effects and spurious noise from the signal DATA.

[**0049**] Referring to **FIG. 4, a** diagram illustrating an embodiment of the power output control block **146** is shown. In one example, the power output control **146** comprises a look up table (LUT) **270**, a pulse width modulation (PWM) generator **272**, and a low pass filter (LPF) **274**. However, the power output control block **146** may implement any appropriate power output control (i.e., modulation) circuitry to meet the design criteria of a particular application.

[**0050**] The LUT **270** may have an input that may receive a signal (e.g., RATING) and an output that may present a signal (e.g., DCCF). The LUT **270** is generally sized in proportion to the size of the signals DATA and DCCF (or the signal CTRL). For example, when the signal RATING is an x bit signal and the signal DCCF is a y bit signal, the LUT **280** may be implemented as a $2^x \times 2^y$ matrix. The signal RATING may be a duty cycle rating. The signal RATING may be determined (e.g., calculated) by the micro-controller **144** in response to the duty cycle of the signal RF_IN as represented by the signal DATA.

[**0051**] The signal DCCF is generally configured as an intermediate modulation signal to provide control of amplitude of the signal RF_OUT that corresponds to an inverse of the duty cycle of the data. The signal DCCF may be generated and presented via the LUT **270** in response to the signal RATING. Since the output block **108** may be frequency dependent, the system **100** may customize (e.g., match, optimize, etc.) the output of the power control block **146** (e.g., the signal CTRL) via values of the signal DCCF that are stored in the LUT **270**.

[**0052**] The PWM generator **272** may have an input that may receive the signal DCCF and an output that may be connected to an input of the LPF **274**. The PWM generator **272** may be configured to generate an intermediate PWM control signal (e.g., A_CTRL) in response to the signal DCCF. The LPF **274** may have an input that may receive the signal A_CTRL and an output that may present the signal CTRL. The LPF **274** may comprise a resistance **280** and a capacitance **282**. The resistance **280** may have a first terminal that may receive the signal A_CTRL and a second terminal that may present the signal CTRL and may be connected to a first terminal of the capacitance **282**. The capacitance **282** may have a second terminal that may be connected to the ground potential VSS. However, the LPF **274** may be implemented as any appropriate LPF to meet the design criteria of a particular application. The LUT **270**, the PWM generator **272**, and the filter **274** may be implemented as stand-alone circuits (not shown) or in connection with the controller **144**.

[**0053**] Alternatively, the gain control **146** may be implemented within a microprocessor (e.g., the micro-controller/memory **144**) with the signal CTRL generated via a digital to analog converter (DAC) where the output signal is proportional to the input duty cycle contained in the signal RF_IN or contained in a data code generated by controller **144**. If the output TX is continuously amplitude modulated, the signal CTRL may also be used to modulate RF_OUT to produce TX.

[**0054**] As is readily apparent from the foregoing description, then, the transceiver **100** of the present invention provides an improved transceiver for implementation in such applications as home appliance remote control transceivers. The present invention may provide a transmitter and receiver (e.g., the transceiver **100**) that generally implements a digital radio frequency memory (e.g., the DRFM **140**). The transceiver **100** of the present invention may have reduced area and cost when compared to conventional approaches. Furthermore, the transceiver **100** may program more quickly, be more resistant to breakage when dropped, and be more stable over changes in temperature and time than conventional approaches.

[**0055**] While embodiments of the invention have been illustrated and described, it is not intended that these embodiments illustrate and describe all possible forms of the invention. Rather, the words used in the specification are words of description rather than limitation, and it is understood that various changes may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A vehicular programmable transceiver comprising:

a digital radio frequency memory (DRFM) having at least one register configured to sample and hold a radio frequency input signal in response to a clock signal, and to generate an output signal having a carrier frequency generated in response to the sampled and held input signal.

2. The transceiver of claim 1 wherein the transceiver is configured to sample and hold the input signal in response to at least one control signal during a programming operation.

3. The transceiver of claim 2 wherein the transceiver comprises an output circuit configured to generate the output signal in response to a carrier signal having the carrier frequency and an output control signal during a transmit operation.

4. The transceiver of claim 1 wherein the clock signal has an over-sampling frequency compared to the input signal.

5. The transceiver of claim 1 wherein the DRFM comprises circuitry which outputs a square wave signal having

a fundamental frequency substantially the same as a radio frequency input signal carrier frequency.

6. The transceiver of claim 5 wherein the DRFM stores at least one binary sequence representing the square wave signal.

7. The transceiver of claim 6 wherein the output signal is based on a combination of a plurality of binary sequences stored in the DRFM.

8. The transceiver of claim 3 wherein the DRFM comprises a plurality of registers connected in parallel and each register is connected to a combiner configured to present the carrier signal.

9. The transceiver of claim 3 wherein the transceiver further comprises a baseband recovery circuit configured to generate a baseband data signal in response to the input signal.

10. The transceiver of claim 9 wherein the transceiver further comprises a controller configured to generate the at least one control signal in response to at least one user interface signal.

11. The transceiver of claim 9 comprising a controller configured to generate the output control signal in response to the baseband data signal.

12. The transceiver of claim 10 wherein the transceiver further comprises an interface circuit configured to present the at least one user interface signal.

13. The transceiver of claim 11 wherein the controller generates an intermediate control signal that corresponds to an inverse of the duty cycle of the baseband data signal and generates the output control signal in response to the intermediate control signal.

14. The transceiver of claim 1 wherein the output signal is filtered to adjust output power based on spectral characteristics of the output signal.

15. For use in a home appliance remote control, a programmable transceiver comprising:

a digital radio frequency memory (DRFM) configured to hold samples of an input signal during a programming operation, and to generate an output signal having a carrier during a transmit operation, wherein the carrier is shifted out of the DRFM in response to a clock signal.

16. The transceiver of claim 15 wherein the transceiver is configured to generate the output signal in response to the carrier and an output control signal.

17. The transceiver of claim 15 wherein the clock signal has an over-sampling frequency compared to the input signal.

18. The transceiver of claim 16 wherein the DRFM comprises a plurality of registers connected in parallel and each register is connected to a combiner configured to present the carrier.

19. The transceiver of claim 16 wherein the transceiver comprises a baseband recovery circuit configured to generate a baseband data signal in response to the input signal and an output circuit configured to generate the output control signal in response to the baseband data signal.

20. For use in a programmable transceiver, a method for generating an output signal, the method comprising:

sampling a radio frequency input signal received from a remote control transmitter;

holding the sampled signal in at least one buffer;

shifting from the buffer a carrier signal; and

controlling an amplitude of the carrier signal to generate the transceiver output signal.

21. The method of claim 20 wherein on-off keyed signaling is generated by turning on and off the shifting from the buffer.

22. The method of claim 20 wherein sampling comprises over-sampling compared to a frequency of the input signal.

23. The method of claim 20 wherein the buffer comprises a plurality of registers connected in parallel and each register is connected to a combiner configured to generate the carrier signal.

24. The method of claim 20 wherein the method comprises generating a baseband data signal in response to the input signal, generating an output control signal in response to the baseband data signal, and controlling an amplitude of the carrier signal with the output control signal.

25. The method of claim 20 wherein the method comprises controlling the amplitude the carrier signal in response to an inverse of a duty cycle of the input signal.

26. The method of claim 20 wherein the method comprises determining an output power level of the output signal by filtering the output signal.

27. A method of remotely controlling a garage door opener that is remotely controlled by an existing transmitter, the existing transmitter transmitting a signal comprising a carrier modulated by a code, the method comprising:

receiving the signal;

detecting the code;

sampling the signal at a time determined by the detected code;

storing the sampled signal;

receiving a request to remotely control the garage door opener;

generating a carrier approximation by playing the stored sampled signal;

controlling an amplitude of the carrier approximation; and

transmitting the generated carrier approximation.

28. The method of claim 27 further comprising storing the detected code.

29. The method of claim 28 wherein the carrier amplitude is controlled based on the stored detected code.

30. The method of claim 27 wherein storing the sampled signal comprises storing the sampled signal in at least one shift register.

31. The method of claim 30 wherein generating a carrier approximation comprises shifting data out of the at least one shift register.

32. A programmable remote garage door opener comprising:

a receiver for receiving a received signal comprising a received carrier modulated with a received code;

a detector for detecting the received code in the received signal;

a transmitter for transmitting an output signal;

at least one register for holding a plurality of samples of the received signal; and

control logic operative to

(a) determine when the received code is detected,

(b) signal the at least one register to sample and store the received signal based on detecting the received code,

(c) receive a request to transmit a remote control command,

(d) signal the at least one register to present the stored signal to the transmitter, and

(e) signal the transmitter to control an amplitude of the stored signal presented by the at least one register thereby generating the output signal.

33. A programmable remote garage door opener as in claim 32 wherein the control logic is further operative to store the detected received code.

34. A programmable remote garage door opener as in claim 33 wherein the control logic signals the transmitter based on the stored code.

35. A programmable remote garage door opener as in claim 32 wherein the generated signal operates a garage door opener.

36. A programmable remote garage door opener as in claim 32 wherein the generated signal operates at least one light.

37. A programmable remote garage door opener as in claim 32 wherein the generated signal operates at least one appliance.

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