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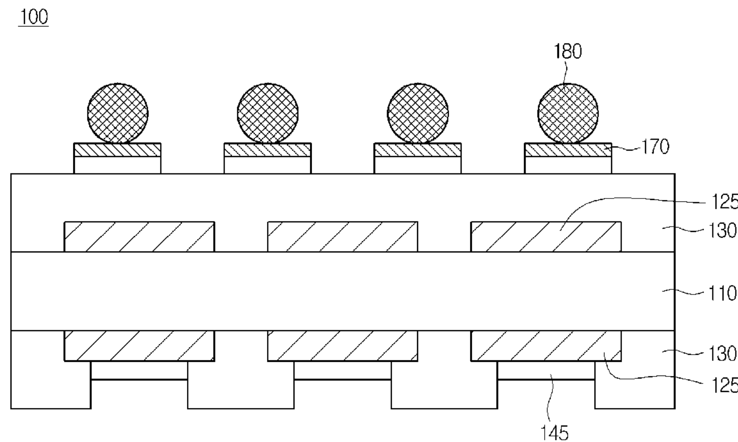
(54) Title: SEMICONDUCTOR PACKAGE SUBSTRATE, PACKAGE SYSTEM USING THE SAME AND METHOD FOR MANUFACTURING THEREOF



(57) Abstract: According to the embodiment, there is provided a semiconductor package substrate including an insulating substrate, a circuit pattern on the insulating substrate, a protective layer formed on the insulating substrate to cover the circuit pattern on the insulating substrate, a pad formed on the protective layer while protruding from a surface of the protective layer, and an adhesive member on the pad.

WO 2013/176519 A1

Description

Title of Invention: SEMICONDUCTOR PACKAGE SUBSTRATE, PACKAGE SYSTEM USING THE SAME AND METHOD FOR MANUFACTURING THEREOF

Technical Field

[1] The embodiment relates to a semiconductor substrate, and more particularly, to a semiconductor package substrate for a flash memory, a flash memory using the same, and a method for fabricating the same.

Background Art

[2] As electrical/electronic appliances have been advanced with high performance, the technology for attaching a greater number of packages onto a substrate having a limited size has been proposed and studied. However, since it is a rule to mount only one semiconductor chip in a package, there is limitation to obtain a desired capacity.

[3] As a method of increasing a capacity of a memory chip, that is, as a method of achieving high integration, the technology of installing a greater number of cells in a limited space has been generally known to those skilled in the art. However, such a method requires a high level technology such as a precise design rule, and a lot of development time. Thus, as a method for easily achieving high integration, a stacking technique has been developed and the study for the sacking technique has been currently performed very actively.

[4] To this end, an MCP (Multi Chip Package) technique has been recently utilized.

[5] The MCP is a semiconductor product prepared in the form of one package by stacking several memory chips, so the MCP not only reduces the volume of the semiconductor product, but also increases the data storage capacity, so that the MCP is mainly used in portable electronic equipment such as a mobile phone.

[6] In this case, since several tens of semiconductor chips are stacked to be stably operated while minimizing the thickness thereof, the high level technique is required from the design stage to the production stage.

[7] FIG. 1 is a view showing a package system according to the related art.

[8] Referring FIG. 1, the package system includes a semiconductor package substrate 10, a dummy die 20, and a memory chip 30.

[9] The semiconductor package substrate 10 includes at least one circuit pattern formed on an insulation substrate. A protection layer for protecting the circuit pattern is formed on the circuit pattern (uppermost layer of the semiconductor package substrate 10).

[10] The memory chip 30 may be a NAND flash memory chip.

[11] The dummy die 20 is formed between the semiconductor substrate 10 and the memory chip 30.

[12] The dummy die 20 provides an attaching space for allowing the memory chip 30 to be attached onto the semiconductor substrate 10 while spacing the semiconductor substrate 10 from the memory chip 30.

[13] However, since the package system described above must form the dummy die 20 between the semiconductor substrate 10 and the memory chip 30 for stacking the memory chip 30, an additional process is required in addition to a process for fabricating the semiconductor substrate 10, so that productivity of a manufacturer is reduced.

[14] Further, since the dummy die 20 is formed of an expensive silicon material, a cost of the entire package system is increased.

[15] In addition, since the silicon dummy die 20 has a predetermined thickness, the entire thickness of the package system is increased.

Disclosure of Invention

Technical Problem

[16] The embodiment provides a semiconductor package substrate having a novel structure, a package system using the same, and a method for manufacturing the same.

[17] In addition, the embodiment provides a semiconductor package substrate capable of improving the productivity of a package system and reducing the cost of the package system.

[18] The technical objects which will be achieved in the proposed embodiments are not limited to the above, but other technical objects which are not mentioned will be apparently understood to those skilled in the art.

Solution to Problem

[19] According to the embodiment, there is provided a semiconductor package substrate including an insulating substrate, a circuit pattern on the insulating substrate, a protective layer formed on the insulating substrate to cover the circuit pattern on the insulating substrate, a pad formed on the protective layer while protruding from a surface of the protective layer, and an adhesive member on the pad.

[20] In addition, the pad has a shape of a column having a lower width and an upper width equal to each other.

[21] Further, the adhesive member provides an adhesive strength between the pad and a semiconductor chip attached onto the pad.

[22] In addition, the pad includes a plating seed layer formed at a lower portion of the pad.

[23] In addition, the pad includes a first pad, which is formed on the protective layer and

has a first width, and a second pad which is formed on the first pad and has a second width different from the first width.

[24] Further, the second width of the second pad is narrower than the first width of the first pad.

[25] In addition, the adhesive member includes one of a solder ball, a micro-ball, an adhesive paste, and a copper core solder ball.

[26] In addition, the protective layer includes one of solder resist (SR), oxide, and gold (Au).

[27] Further, the pad makes contact with a top surface of the protective layer without making contact with the circuit pattern and the insulating substrate.

[28] Meanwhile, according to the embodiment, there is provided a package system including a semiconductor package substrate including an insulating substrate, a circuit pattern on one surface of the insulating substrate, and a protective layer formed on the insulating substrate to cover the circuit pattern, and a semiconductor chip attached to the semiconductor package substrate. The semiconductor package substrate comprises a pad formed on the protective layer through a plating scheme, and an adhesive member formed on the pad, and the semiconductor chip is attached onto the pad, which is formed on the semiconductor package substrate, by the adhesive member.

[29] In addition, the pad has a shape of a column having a lower width and an upper width equal to each other.

[30] In addition, the pad includes a first pad, which is formed on the protective layer and has a first width, and a second pad which is formed on the first pad and has a second width different from the first width, and wherein the semiconductor chip is attached onto the second pad by the adhesive member formed on the second pad.

[31] Further, the second width of the second pad is narrower than the first width of the first pad.

[32] In addition, the adhesive member includes one of a solder ball, a micro-ball, an adhesive paste, and a copper core solder ball.

[33] In addition, the pad makes contact with a top surface of the protective layer without making contact with the circuit pattern and the insulating substrate.

[34] Meanwhile, according to the embodiment, there is provided a method for manufacturing a package system. The method includes forming a circuit pattern on at least one surface of an insulating substrate, forming a protective layer on the insulating substrate to cover the circuit pattern, attaching a dry film, which has an opening to expose a region for formation of a pad, on the protective layer, forming the pad on the protective layer by filling the opening of the dry film, and forming an adhesive member on the formed pad.

[35] In addition, the opening of the dry film has a lower width and an upper width equal

to each other, and the pad has a shape of a column, which has a lower width and an upper width equal to each other, corresponding to a shape of the opening.

[36] Further, in the forming of the pad on the protective layer by filling the opening of the dry film, the pad makes contact with the protective layer without making contact with the insulating substrate and the circuit pattern.

[37] In addition, the method further includes forming a plating seed layer on the protective layer, wherein the formed pad includes the plating seed layer formed at a lower portion of the pad.

[38] Further, the attaching of the dry film, which has the opening to expose the region for formation of the pad, on the protective layer includes forming a first dry film, which has an opening having a first width, on the protective layer, and forming a second dry film, which has an opening having a second width, on the first dry film. The first width is different from the second width.

[39] In addition, the forming of the pad on the protective layer by filling the opening of the dry film includes forming a first pad by filling the opening of the first dry film, forming a second pad by filling the opening of the second dry film. The second pad is narrower than the first pad.

[40] Further, the forming of the adhesive member on the formed pad include forming at least one of a solder ball, a micro-ball, an adhesive paste, and a copper core solder ball on the pad.

[41] In addition, the method further includes attaching a semiconductor chip on the adhesive member.

Advantageous Effects of Invention

[42] As described above, according to the embodiment, the copper pad and the adhesive member are formed on the semiconductor package without the expensive dummy die, so that the productivity of a package system can be improved and the product cost can be reduced

[43] In addition, according to the embodiment, the pad is formed by using the stack structure of multiple layers having different widths, thereby improving the adhesive strength with the adhesive member, so that the reliability of the semiconductor package substrate can be improved.

[44] Further, according to the embodiment, the copper ball is used instead of the expensive dummy die, so that the fine pitch can be realized.

[45] In addition, according to the embodiment, the second adhesive member is formed by using the copper core solder ball, so that the high stand-off height can be maintained after the reflow process has been performed. Accordingly, the reliability of the semiconductor package substrate can be improved.

Brief Description of Drawings

[46] FIG. 1 is a view showing a package system according to the related art;

[47] FIG. 2 is a sectional view showing a semiconductor package substrate according to the first embodiment;

[48] FIGS. 3 to 15 are sectional views showing a method for fabricating the semiconductor package substrate shown in FIG. 2 in the sequence of process steps;

[49] FIG. 16 is a view showing a semiconductor package substrate according to the second embodiment;

[50] FIGS. 17 to 23 are sectional views showing the method for fabricating the semiconductor package substrate shown in FIG. 16 in the sequence of the process steps;

[51] FIGS. 24 and 25 are views showing a package system according to the embodiment; and

[52] FIG. 26 illustrates the comparison in the package system between the related art and the embodiment.

Mode for the Invention

[53] The embodiment of the disclosure will be described in detail with reference to accompanying drawings, so that those skilled in the art to which the disclosure pertains can easily realize the embodiment. However, the disclosure can be realized in various modifications, and is not limited to the embodiment.

[54] In the following description, when a predetermined part "includes" a predetermined component, the predetermined part does not exclude other components, but may further include other components if there is a specific opposite description.

[55] The thickness and size of each layer shown in the drawings may be exaggerated, omitted or schematically drawn for the purpose of convenience or clarity. In addition, the size of elements does not utterly reflect an actual size. The same reference numbers will be assigned the same elements throughout the drawings.

[56] In the description of the embodiments, it will be understood that, when a part is referred to as being "on" or "under" another part, it can be "directly" or "indirectly" on the other part, or one or more intervening parts may also be present. Such a position of the part has been described with reference to the drawings.

[57] The embodiment provides a semiconductor package substrate capable of improving the productivity of a package system and reducing the product cost by forming a copper pad and an adhesive member on the semiconductor package substrate through a hybrid bump technology without using an expensive dummy die.

[58] FIG. 2 is a view showing a semiconductor package substrate according to a first embodiment.

[59] Referring to FIG. 2, a semiconductor package substrate 100 according to the first em-

bodiment includes an insulating substrate 110, a circuit pattern 125 formed on at least one surface of the insulating substrate 110, a protective layer 130 formed on the insulating substrate 110 to protect the circuit pattern 120, a first adhesive member 145 formed on the circuit pattern 125 formed on an opposite surface to a surface, on which a semiconductor chip 300 (which will be described layer) is formed, in the insulating substrate 110, a pad 170 on the protective layer 130 provided on the top surface of the insulating substrate 110, and a second adhesive member 180 formed on the pad 170.

[60] The insulating plate 110 may include thermosetting substrate, thermoplastic polymer substrate, a ceramic substrate, an organic-inorganic composite material substrate, or a glass fiber impregnation substrate. If the insulating plate 110 includes a polymer resin, the insulating plate 110 may include an epoxy-based insulating resin, or may include polyimide-based resin.

[61] The insulating plate 110 is formed on at least one surface thereof with the circuit pattern 125.

[62] In addition, circuit patterns 125 may include conductive material, and may be formed by simultaneously patterning a copper film formed on both surfaces of the insulating substrate 110.

[63] The circuit pattern 125 may be made of the alloy including copper (Cu) and may have surface roughness.

[64] The insulating substrate 110 is provided thereon with the protective layer 130 covering the circuit pattern 125 formed on the top surface of the insulating substrate 110 while exposing a portion of the surface of the circuit pattern 125 formed on the bottom surface of the insulating substrate 110.

[65] The protective layer 130 is to protect the surface of the insulating substrate 110. The protective layer 130 is formed throughout the entire surface of the insulating substrate 110. The protective layer 130 has an opening (not shown) to open the surface of the circuit pattern 125 to be exposed, that is, the surface of the stacking structure of the circuit pattern 125 formed on the bottom surface of the insulating substrate 110.

[66] The protective layer 130 may include at least one layer including one of solder resist (SR), an oxide, and gold (Au).

[67] The first adhesive member 145 is formed on the surface of the circuit pattern 125 exposed through the protective layer 130.

[68] The first adhesive member 145 is formed for the purpose of attaching a conductive ball to the insulating substrate 110 in order to package the semiconductor package substrate 100 together with an additional substrate thereafter.

[69] The protective layer 130 is provided thereon with the pad 170.

[70] The pad 170 is formed on the protective layer 130 to cover the entire surface of the circuit pattern 125, and does not make contact with the insulating substrate 110 or the

circuit pattern 125.

[71] The pad 170 may include a conductive material. For example, the pad 170 may include copper (Cu).

[72] The pad 170 is formed on the protective layer 130 for the purpose of attaching the semiconductor chip onto the semiconductor package substrate 100 thereafter.

[73] In other words, according to the related art, in order to attach the semiconductor chip 300, a dummy die including silicon is formed on the semiconductor package substrate regardless of the fabrication of the semiconductor package substrate 100. However, according to the present embodiment, instead of the dummy die, the pad 170 is formed on the protective layer 130 through a hybrid bump technology in the fabrication process of the semiconductor package

[74] The second adhesive member 180 is formed on the pad 170.

[75] The second adhesive member 180 is formed on the pad 170 to provide the adhesive strength between the semiconductor chip 300 and the semiconductor package substrate 100.

[76] The second adhesive member 180 may have the typical form of a solder ball. Alternatively, the second adhesive member 180 may be formed by using an adhesive paste or a copper core solder ball.

[77] In addition, the adhesive paste may include a conductive material for the electrical conduction. If the adhesive paste includes the conductive material, the conductive material may preferably include one selected from the group consisting of copper (Cu), silver (Ag), gold (Au), aluminum (Al), a carbon nano-tube, and the combination thereof.

[78] As described above, according to the embodiment, the copper pad and the adhesive member are formed on the semiconductor package substrate without the expensive dummy die, so that the productivity of a package system can be improved and the product cost can be reduced

[79] In addition, as described above, according to the embodiment, the copper ball is used instead of the expensive dummy die, so that the fine pitch is possible.

[80] Further, as described above, according to the embodiment, the second adhesive member is formed by using a copper core solder ball 188, so that the high stand-off height can be maintained after the reflow process has been performed. Accordingly, the reliability of the semiconductor package substrate can be improved.

[81] FIGS. 3 to 15 are sectional views showing a method for fabricating the semiconductor package substrate shown in FIG. 2 in the sequence of process steps.

[82] First, after preparing the insulating substrate 110 as shown in FIG. 3, a metallic layer 120 is stacked on at least one surface of the insulating substrate 110.

[83] If the insulating substrate 110 includes an insulating layer, the stack structure of the

insulating layer and the metallic layer 120 may be a copper clad laminate (CCL) structure.

[84] In addition, the metallic layer 120 may be formed on the insulating substrate 110 by performing an electroless plating scheme. If the metallic layer 120 is formed through the electroless plating scheme, the roughness is applied to the surface of the insulating substrate 110, so that the plating process can be smoothly performed.

[85] The insulating substrate 110 may include epoxy-based resin or polyimide-based resin instead of the expensive ceramic material representing high thermal conductivity. The metallic layer 120 may include a copper thin film including copper high electrical conductivity and low resistance.

[86] Thereafter, as shown in FIG. 4, the circuit pattern 125 is formed by etching metallic layers 120, which are formed at the upper and lower portions of the insulating substrate 110, at a predetermined pattern.

[87] In this case, the circuit pattern 125 may be formed through the etching process based on the photolithography process or through a laser process to directly form a pattern by using the laser.

[88] In addition, the circuit pattern 125 may be formed on the upper and lower portions of the insulating substrate 110. Alternatively, the circuit pattern 125 may be formed only on the upper portion of the insulating substrate 110.

[89] Next, as shown in FIG. 5, the protective layer 130 is formed on the upper and lower portions of the insulating substrate 110 to bury the circuit pattern 125.

[90] The protective layer 130 is to protect the surface of the insulating substrate 110 or the circuit pattern 125. The protective layer 130 may include at least one layer including one of solder resist (SR), an oxide, and gold (Au).

[91] Next, as shown in FIG. 6, the protective layer 130 formed on the lower portion of the insulating substrate 110 is processed, thereby exposing the surface of the circuit pattern 125 formed on the bottom surface of the insulating substrate 110.

[92] In other words, the protective layer 130 formed under the insulating substrate 110 is processed by a laser to form the opening 140 to expose the surface of the circuit pattern 125 formed under the insulating substrate 110.

[93] The laser process is a cutting scheme to melt and evaporate a portion of a material by concentrating optical energy on a surface so that the surface has a desired shape. According to the laser process, the complex shape can be easily processed through a computer program, and mixed material, which may not be easily cut through another scheme, can be processed.

[94] In addition, the laser process has an advantage in that the cut diameter may be formed to at least 0,005 mm

[95] A laser drill for the laser process preferably includes an yttrium aluminum garnet

(YAG), a CO_2 laser, or an ultraviolet (UV) laser. The YAG laser may process both of the copper film and the insulating layer, and the CO_2 laser may process only the insulating layer.

[96] In this case, preferably, the laser process is performed by using the UV laser, so that the opening 140 having a smaller diameter may be formed.

[97] In addition, the opening 140 may expose only a portion of the circuit pattern 125.

[98] In other words, the opening 140 may have a width narrower than that of the circuit pattern 125, so that only the edge region of the circuit pattern 125 may be protected by the protective layer 130.

[99] Thereafter, as shown in FIG. 7, the first adhesive member 145 is formed on the circuit pattern 125 exposed by the opening 140.

[100] The first adhesive member 145 may be formed by coating an adhesive paste on the circuit pattern 125 exposed through the opening 140 by employing the protective layer 130 as a mask.

[101] The first adhesive member 145 is used to attach the solder ball, which provides an adhesive strength, between the semiconductor package substrate 100 and another substrate, so that the semiconductor package 100 is attached to the substrate.

[102] Thereafter, as shown in FIG. 8, a plating seed layer 150 is formed on the protective layer 130 formed at the upper portion of the insulating substrate 110 as shown in FIG. 8.

[103] The plating seed layer 150 may be formed through the chemical copper plating scheme.

[104] The chemical copper plating scheme may be performed in the sequence of a degreasing process, a soft etching process, a pre-catalyst process, a catalyst treatment process, an accelerator process, an electroless plating process, and an anti-oxidation treatment process.

[105] In addition, the copper plating scheme is classified into a heavy copper plating scheme (the thickness of about 2), a medium copper plating scheme (the thickness of 1 to 2), and a light copper plating scheme (the thickness of 1 or less) according to the thicknesses. In this case, the plating seed layer 150 having the thickness of 0.5 to 1.5 is formed through the medium copper plating scheme or the light copper plating scheme.

[106] Thereafter, as shown in FIG. 9, a dry film 160 is formed on the plating seed layer 150.

[107] The dry film 160 may have a window to open a portion opposite to the region in which the pad 170 is formed.

[108] In this case, the dry film 160 may surround the entire surface of the plating seed layer 150, so that the window to open the region for the pad 170 may be formed.

[109] Thereafter, as shown in FIG. 10, the pad 170 is formed on the plating seed layer 150

to bury the open window of the dry film 160.

[110] The pad 170 may be formed by electroless-plating metal such as copper (Cu) using the plating seed layer 150 as a seed layer.

[111] Thereafter, as shown in FIG. 11, the dry film 160 is delaminated.

[112] Subsequently, as shown in FIG. 12, the plating seed layer 150 formed on the remaining region is removed except for the region for the pad 170.

[113] In this case, a portion of the plating seed layer 150 exists under the pad 170, so that the whole structure of the pad 170 includes the plating seed layer 150.

[114] As described above, the pad 170 including the plating seed layer 130 is formed on the protective layer 130.

[115] Next, as shown in FIG. 13, the second adhesive member 180 is formed on the pad 170.

[116] In this case, the second adhesive member 180 according to the first embodiment may be formed by using a solder ball, or a micro-ball.

[117] The second adhesive member 180 may be formed on the pad 170 through a flux printing scheme, a ball printing scheme, a reflow scheme, a deflux scheme, and a coining scheme.

[118] Alternatively, as shown in FIG. 14, the second adhesive member 180 may be formed on the pad 170 by coating the adhesive paste 182 on the pad 170.

[119] In addition, alternatively, as shown in FIG. 15, the second adhesive member 180 may be formed on the pad 170 by using a copper core solder ball 188 including a copper ball 184 and a solder ball 186 surrounding the circumference of the copper ball 184.

[120] As described above, the pad 170 constituting the semiconductor package substrate 100 according to the first embodiment protrudes from the protective layer 130 and has the same width in the top and bottom surfaces.

[121] As described above, according to the embodiment, the copper pad and the adhesive member are formed on the semiconductor package substrate through the hybrid bump technology without the expensive dummy die, so that the productivity of a package system can be improved and the product cost can be reduced

[122] In addition, as described above, the second adhesive member 180 is formed by using the copper core solder ball 188, so that the high stand-off height can be maintained after the reflow process has been performed. Accordingly, the reliability of the semi-conductor substrate can be improved.

[123] FIG. 16 is a view showing a semiconductor package substrate according to the second embodiment.

[124] Referring to FIG. 16, a semiconductor package substrate 200 according to the second embodiment includes an insulating substrate 210, a circuit pattern 225 formed on at least one surface of the insulating substrate 210, a protective layer 230 formed on the

insulating substrate 210 to protect the circuit pattern 225, a first adhesive member 245 formed on the circuit pattern 225 formed on an opposite surface to a surface, on which a semiconductor chip 300 (which will be described layer) is formed, in the insulating substrate 210, a pad 270 formed on the protective layer 230 provided on the top surface of the insulating substrate 210, and a second adhesive member 280 formed on the pad 270.

[125] The pad 170 includes a first pad 272 formed on the protective layer 230 and a second pad 274 formed on the first pad 272.

[126] The insulating plate 210 may include thermosetting substrate, thermoplastic polymer substrate, a ceramic substrate, an organic-inorganic composite material substrate, or a glass fiber impregnation substrate. If the insulating plate 210 includes a polymer resin, the insulating plate 210 may include an epoxy-based insulating resin, or may include polyimide-based resin.

[127] The circuit pattern 225 is formed on at least one surface of the insulating substrate 210.

[128] In addition, circuit patterns 225 may include conductive material, and may be formed by simultaneously patterning a copper film formed on both surfaces of the insulating substrate 210.

[129] The circuit pattern 225 may be made of the alloy including copper (Cu) and may have surface roughness.

[130] The insulating substrate 210 is provided thereon with the protective layer 230 covering the circuit pattern 225 formed on the top surface of the insulating substrate 210 while exposing a portion of the surface of the circuit pattern 225 formed on the bottom surface of the insulating substrate 210.

[131] The protective layer 230 is to protect the surface of the insulating substrate 210. The protective layer 230 is formed throughout the entire surface of the insulating substrate 210. The protective layer 230 has an opening (not shown) to open the surface of the circuit pattern 225 to be exposed, that is, the surface of the stacking structure of the circuit pattern 225 formed on the bottom surface of the insulating substrate 210.

[132] The protective layer 230 may include at least one layer including one of solder resist (SR), an oxide, and gold (Au).

[133] The first adhesive member 245 is formed on the surface of the circuit pattern 225 exposed through the protective layer 230.

[134] The first adhesive member 245 is formed for the purpose of attaching a conductive ball to the insulating substrate 210 in order to package the semiconductor package substrate 200 together with an additional substrate thereafter.

[135] The protective layer 230 is provided thereon with the pad 270.

[136] The pad 270 is formed on the protective layer 230 to cover the entire surface of the

circuit pattern 225, and does not make contact with the insulating substrate 210 or the circuit pattern 225.

[137] The pad 270 may include a conductive material. For example, the pad 270 may include copper (Cu).

[138] The pad 270 is formed on the protective layer 230 for the purpose of attaching the semiconductor chip 300 onto the semiconductor package substrate 200 thereafter.

[139] In this case, the pad 270 includes a plurality of layers.

[140] In other words, the pad 270 includes the first pad 272 formed on the protective layer 230 and the second pad 274 formed on the first pad 272.

[141] The first pad 272 has the same width in the top and bottom surfaces thereof, and is formed on the protective layer 230.

[142] Even the second pad 274 has the same width in the top and bottom surfaces thereof, and is formed on the first pad 272.

[143] In this case, the width of the first pad 272 may have the first width, and the second pad 274 may have the second width narrower than the first width.

[144] In other words, according to the first embodiment, the pad 170 is formed in a single layer for the purpose of the attachment to the semiconductor chip 300.

[145] However, according to the second embodiment, the first and second pads 272 and 274 are formed in multiple layers for the purpose of the attachment to the semiconductor chip 300. In this case, the width of the second pad 274 is narrower than the width of the first pad 272, so that the adhesive strength with the second adhesive member, which is formed thereafter, may be improved.

[146] The second adhesive member 280 is formed on the second pad 274.

[147] The second adhesive member 280 is formed on the second pad 274 to provide the adhesive strength between the semiconductor chip 300 and the semiconductor package substrate 200.

[148] The second adhesive member 280 may have the typical form of a solder ball. Alternatively, the second adhesive member 280 may be formed by using the adhesive paste or the copper core solder ball.

[149] In addition, the adhesive paste may include a conductive material for the electrical conduction. If the adhesive paste includes the conductive material, the conductive material may preferably include one selected from the group consisting of copper (Cu), silver (Ag), gold (Au), aluminum (Al), a carbon nano-tube, and the combination thereof.

[150] As described above, according to the embodiment, the copper pad and the adhesive member are formed on the semiconductor package substrate through the hybrid bump technology without the expensive dummy die, so that the productivity of a package system can be improved and the product cost can be reduced

[151] FIGS. 17 to 23 are sectional views showing the method for fabricating the semiconductor package substrate shown in FIG. 16 in the sequence of the process steps.

[152] First, after preparing the insulating substrate 210 as shown in FIG. 17, a metallic layer 220 is stacked on at least one surface of the insulating substrate 110.

[153] If the insulating substrate 210 includes an insulating layer, the stack structure of the insulating layer and the metallic layer 120 may be a typical copper clad laminate (CCL) structure.

[154] In addition, the metallic layer 220 may be formed on the insulating substrate 210 by performing an electroless plating scheme. If the metallic layer 220 is formed through the electroless plating scheme, the roughness is applied to the surface of the insulating substrate 210, so that the plating process can be smoothly performed.

[155] The insulating substrate 210 may include epoxy-based resin or polyimide-based resin instead of the expensive ceramic material representing high thermal conductivity. The metallic layer 220 may include a copper thin film including copper high electrical conductivity and low resistance.

[156] Thereafter, as shown in FIG. 4, the circuit pattern 225 is formed by etching metallic layers 220, which are formed at the upper and lower portions of the insulating substrate 210, at a predetermined pattern.

[157] In this case, the circuit pattern 225 may be formed through the etching process based on the photolithography process or through a laser process to directly form a pattern by using the laser.

[158] In addition, the circuit pattern 225 may be formed on the upper and lower portions of the insulating substrate 210. Alternatively, the circuit pattern 225 may be formed only on the upper portion of the insulating substrate 210.

[159] Next, the protective layer 230 is formed on the upper and lower portions of the insulating substrate 210 to bury the circuit pattern 225.

[160] The protective layer 230 is to protect the surface of the insulating substrate 210 or the circuit pattern 225. The protective layer 230 may include at least one layer including one of solder resist (SR), an oxide, and gold (Au).

[161] Next, the protective layer 230 formed on the lower portion of the insulating substrate 210 is processed, thereby exposing the surface of the circuit pattern 225 formed on the bottom surface of the insulating substrate 210.

[162] Thereafter, the first adhesive member 245 is formed on the circuit pattern 225.

[163] Thereafter, as shown in FIG. 18, the plating seed layer 250 is formed on the protective layer 230 formed on the upper portion of the insulating substrate 210.

[164] The plating seed layer 250 may be formed through the chemical copper plating scheme.

[165] The chemical copper plating scheme may be performed in the sequence of a de-

greasing process, a soft etching process, a pre-catalyst process, a catalyst treatment process, an accelerator process, an electroless plating process, and an anti-oxidation treatment process.

[166] In addition, the copper plating scheme is classified into a heavy copper plating scheme (the thickness of about 2), a medium copper plating scheme (the thickness of 1 to 2), and a light copper plating scheme (the thickness of 1 or less) according to the thicknesses. In this case, the plating seed layer 250 having the thickness of 0.5 to 1.5 is formed through the medium copper plating scheme or the light copper plating scheme.

[167] Thereafter, as described in the first embodiment, a dry film may be formed on the plating seed layer 250. In this case, the dry film (not shown) may have a window to open a portion opposite to the region in which the pad 270 is formed.

[168] Thereafter, the first pad 272 is filled in the window of the dry film.

[169] The first pad 272 may be formed by electroless-plating metal such as copper (Cu) using the plating seed layer 250 as a seed layer.

[170] Thereafter, the formed dry film is removed.

[171] Thereafter, as shown in FIG. 19, the dry film 260 is formed on the plating seed layer 250.

[172] In this case, the dry film 260 may bury a portion of the surface of the first pad 272.

[173] In other words, the dry film 260 may have an opening to expose the surface of the first pad 272. In this case, the width of the opening of the dry film 260 is narrower than the width of the top surface of the first pad 272.

[174] Thereafter, as shown in FIG. 20, the second pad 274 is formed on the first pad 272 by using the dry film 260 as a mask, so that the second pad 274 is filled in the opening.

[175] In this case, the width of the opening is narrow than the width of the top surface of the first pad 272. Accordingly, the width of the second pad 274 is narrower than the width of the first pad 272.

[176] The pad 270 includes the first and second pads 272 and 274. The first pad 272 has a width different from that of the second pad 274 because the adhesive strength with the second adhesive member 280 is increased, so that the reliability of the semiconductor package substrate 200 can be improved.

[177] Next, as shown in FIG. 21, the plating seed layer 250 is removed from a remaining portion except for the region for the first pad 272.

[178] In this case, a portion of the plating seed layer 250 exists under the first pad 272, so that the whole structure of the first pad 272 includes the plating seed layer 250.

[179] As described above, the first pad 272 including the plating seed layer 250 is formed on the protective layer 230, and the second pad 274 is formed with the width, which is narrower than that of the first pad 272, on the first pad 272

[180] Next, as shown in FIG. 23, the second adhesive member 280 is formed on the pad

270.

[181] In this case, the second adhesive member 280 may be formed by using the solder ball or the micro-ball.

[182] If the second adhesive member 280 is formed by using the solder ball or the micro-ball, the second adhesive member 280 may be formed through processes such as a flux printing scheme, a ball printing scheme, a reflow scheme, a deflux scheme, and a coining scheme.

[183] Alternatively, the second adhesive member may be formed by coating adhesive paste. In addition, the second adhesive member may be formed by using a copper core solder ball including a copper ball and a solder ball surrounding the circumference of the copper ball.

[184] As described above, according to the embodiment, the copper pad and the adhesive member are formed on the semiconductor package substrate through the hybrid bump technology without the expensive dummy die, so that the productivity of a package system can be improved and the product cost can be reduced

[185] In addition, according to the embodiment, the pad is formed by using the stack structure of multiple layers, thereby improving the adhesive strength with the adhesive member, so that the reliability of the semiconductor package substrate can be improved.

[186] FIGS. 24 and 25 are views showing a package system according to the embodiment.

[187] Referring to FIGS. 24 and 25, the package system includes the semiconductor package substrate 100 and the memory chip 300 formed on the semiconductor package substrate 100.

[188] The memory chip 300 may include a NAND flash memory chip.

[189] In this case, the memory chip 300 is attached to the semiconductor package substrate 100 by the pad 170 and the second adhesive member 180 which are formed on the semiconductor package substrate 100.

[190] As described above, the memory chip 300 is attached to the pad 170 and the second adhesive member 180 through a hybrid bump technology during the process of fabricating the semiconductor package substrate 100 without using an expensive dummy die separately from the process of fabricating the semiconductor package substrate 100 in order to attach the memory chip 300.

[191] FIG. 26 illustrates the comparison in the package system between the related art and the embodiment.

[192] Referring to FIG. 26, according to the related art, an expensive dummy die 20 is formed on the package substrate 10, and a memory chip 30 is formed on the dummy die 20.

[193] Accordingly, the process of fabricating the package system according to the related

art is mainly divided into three steps.

[194] The first step is to fabricate the package substrate 10.

[195] In addition, the second step is to form the dummy die 20 on the fabricated package substrate 10. In this case, due to the process characteristics, the first and second steps are not performed at once, but performed through a plurality of sub-steps.

[196] The third step is to form the semiconductor chip 30 on the dummy die 20.

[197] However, according to the embodiment, the memory chip 300 is attached onto the pad 170 and the second adhesive member 180 through the hybrid bump technology.

[198] Accordingly, the process of fabricating the package system according to the embodiment is mainly divided into two sub-steps.

[199] The first step is to fabricate the package substrate 100. In this case, the step of fabricating the package substrate 100 includes the step of forming the pad 170 and the second adhesive member 180 formed through the hybrid bump technology.

[200] In addition, the second step is to attach the memory chip 300 onto the pad 170 and the second adhesive member 180 formed through the hybrid bump technology.

[201] As described above, according to the embodiment, the memory chip 300 is attached onto the pad 170 and the second adhesive member 180 formed through the hybrid bump technology without using the expensive dummy die, so that the fabrication cost can be reduced, and the fabrication process can be simplified.

[202] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

[Claim 1] A semiconductor package substrate comprising:
an insulating substrate;
a circuit pattern on the insulating substrate;
a protective layer formed on the insulating substrate to cover the circuit pattern on the insulating substrate;
a pad formed on the protective layer while protruding from a surface of the protective layer; and
an adhesive member on the pad.

[Claim 2] The semiconductor package substrate of claim 1, wherein the pad has a shape of a column having a lower width and an upper width equal to each other.

[Claim 3] The semiconductor package substrate of claim 1, wherein the adhesive member provides an adhesive strength between the pad and a semiconductor chip attached onto the pad.

[Claim 4] The semiconductor package substrate of claim 1, wherein the pad includes a plating seed layer formed at a lower portion of the pad.

[Claim 5] The semiconductor package substrate of claim 1, wherein the pad includes a first pad, which is formed on the protective layer and has a first width, and a second pad which is formed on the first pad and has a second width different from the first width.

[Claim 6] The semiconductor package substrate of claim 5, wherein the second width of the second pad is narrower than the first width of the first pad.

[Claim 7] The semiconductor package substrate of claim 1, wherein the adhesive member includes one of a solder ball, a micro-ball, an adhesive paste, and a copper core solder ball.

[Claim 8] The semiconductor package substrate of claim 1, wherein the protective layer includes one of solder resist (SR), oxide, and gold (Au).

[Claim 9] The semiconductor package substrate of claim 1, wherein the pad makes contact with a top surface of the protective layer without making contact with the circuit pattern and the insulating substrate.

[Claim 10] A package system comprising:
a semiconductor package substrate including an insulating substrate, a circuit pattern on one surface of the insulating substrate, and a protective layer formed on the insulating substrate to cover the circuit pattern; and
a semiconductor chip attached to the semiconductor package substrate,

wherein the semiconductor package substrate comprises a pad formed on the protective layer through a plating scheme, and an adhesive member formed on the pad, and
wherein the semiconductor chip is attached onto the pad, which is formed on the semiconductor package substrate, by the adhesive member.

[Claim 11] The package system of claim 10, wherein the pad has a shape of a column that has a lower width and an upper width equal to each other.

[Claim 12] The package system of claim 10, wherein the pad includes a first pad, which is formed on the protective layer and has a first width, and a second pad which is formed on the first pad and has a second width different from the first width, and wherein the semiconductor chip is attached onto the second pad by the adhesive member formed on the second pad.

[Claim 13] The package system of claim 12, wherein the second width of the second pad is narrower than the first width of the first pad.

[Claim 14] The package system of claim 10, wherein the adhesive member includes one of a solder ball, a micro-ball, an adhesive paste, and a copper core solder ball.

[Claim 15] The package system of claim 10, wherein the pad makes contact with a top surface of the protective layer without making contact with the circuit pattern and the insulating substrate.

[Claim 16] A method for manufacturing a package system, the method comprising:
forming a circuit pattern on at least one surface of an insulating substrate;
forming a protective layer on the insulating substrate to cover the circuit pattern;
attaching a dry film, which has an opening to expose a region for formation of a pad, on the protective layer;
forming the pad on the protective layer by filling the opening of the dry film; and
forming an adhesive member on the formed pad.

[Claim 17] The method of claim 16, wherein the opening of the dry film has a lower width and an upper width equal to each other, and the pad has a shape of a column, which has a lower width and an upper width equal to each other, corresponding to a shape of the opening.

[Claim 18] The method of claim 16, wherein, in the forming of the pad on the protective layer by filling the opening of the dry film, the pad makes

contact with the protective layer without making contact with the insulating substrate and the circuit pattern.

[Claim 19] The method of claim 16, further comprising forming a plating seed layer on the protective layer, wherein the formed pad includes the plating seed layer formed at a lower portion of the pad.

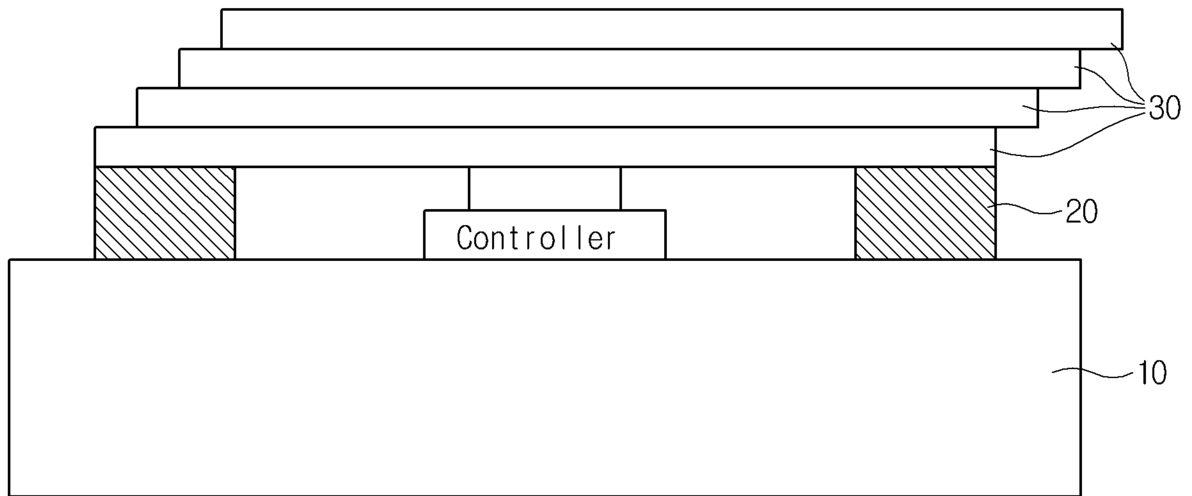
[Claim 20] The method of claim 16, wherein the attaching of the dry film, which has the opening to expose the region for formation of the pad, on the protective layer includes:
forming a first dry film, which has an opening having a first width, on the protective layer; and
forming a second dry film, which has an opening having a second width, on the first dry film;
wherein the first width is different from the second width.

[Claim 21] The method of claim 20, wherein the forming of the pad on the protective layer by filling the opening of the dry film includes:
forming a first pad by filling the opening of the first dry film;
forming a second pad by filling the opening of the second dry film; and
wherein the second pad is narrower than the first pad.

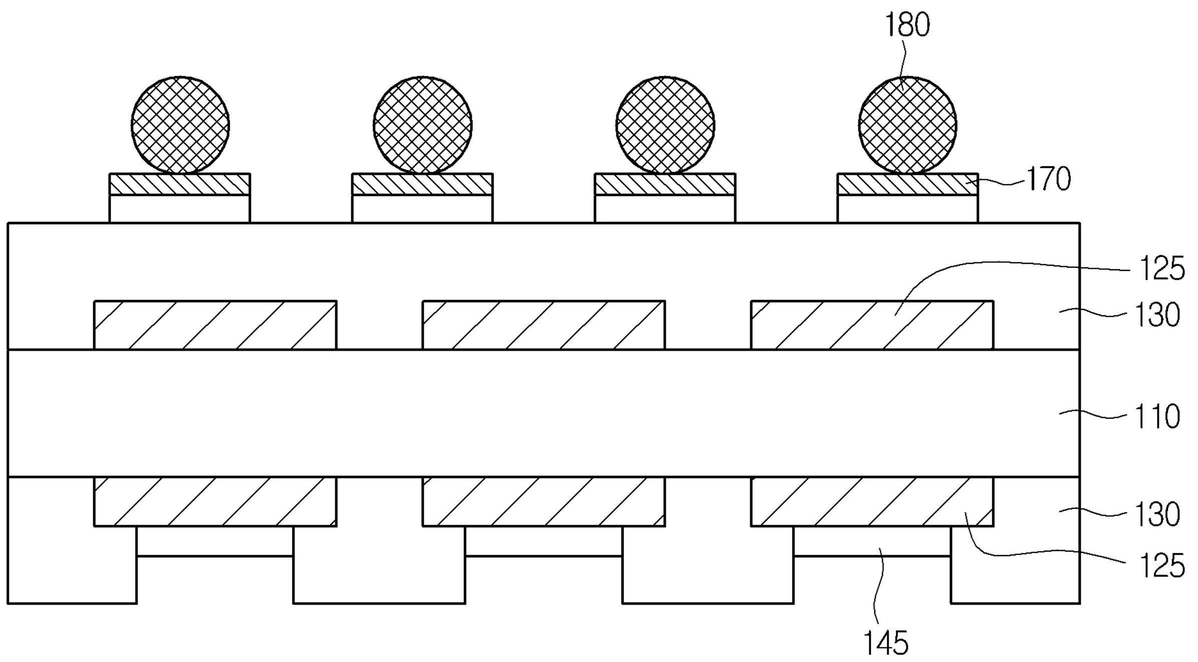
[Claim 22] The method of claim 16, wherein the forming of the adhesive member on the formed pad include forming at least one of a solder ball, a micro-ball, an adhesive paste, and a copper core solder ball on the pad.

[Claim 23] The method of claim 16, further comprising attaching a semiconductor chip on the adhesive member.

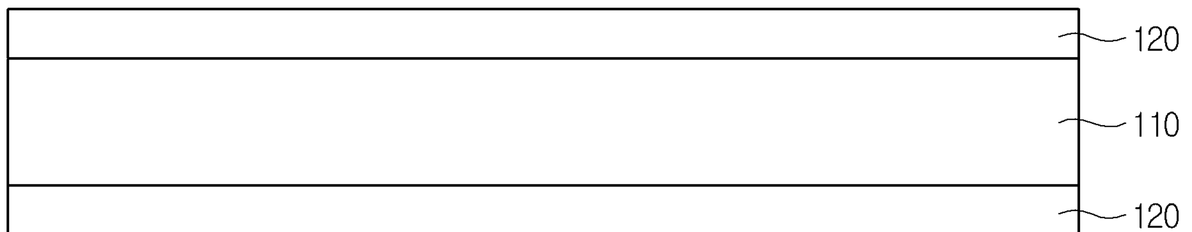
[Fig. 1]



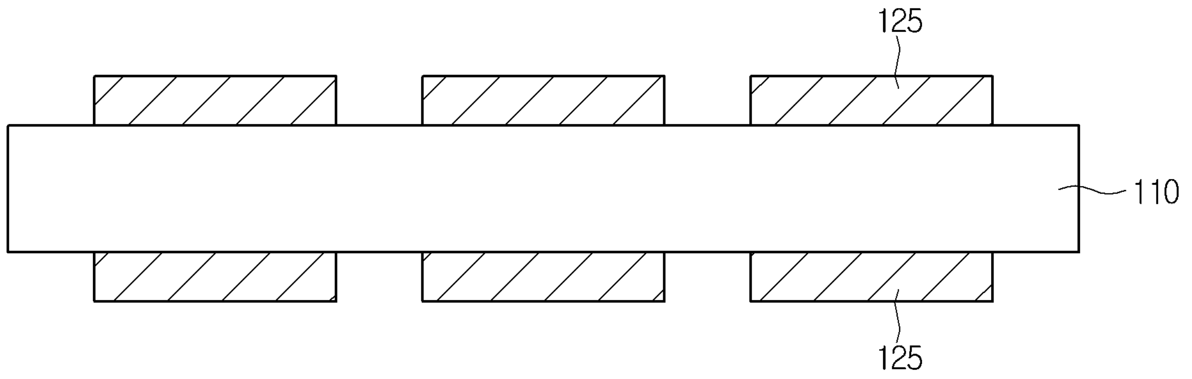
[Fig. 2]



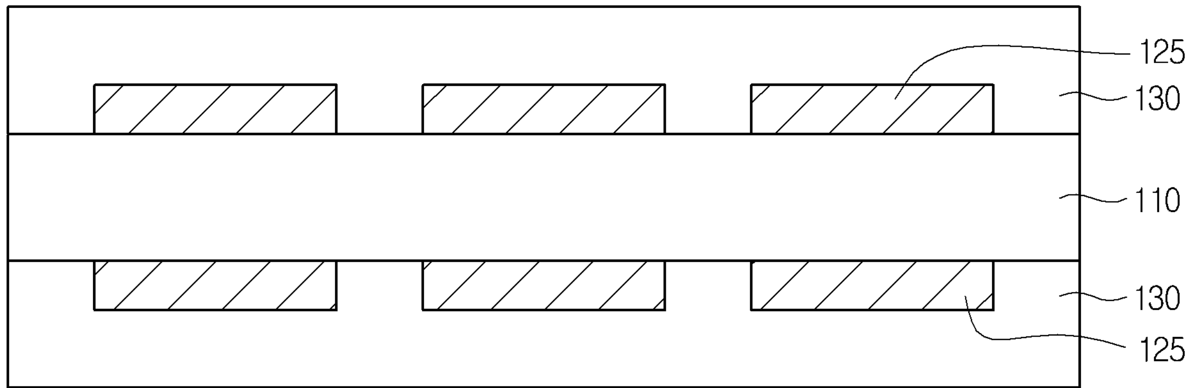
[Fig. 3]



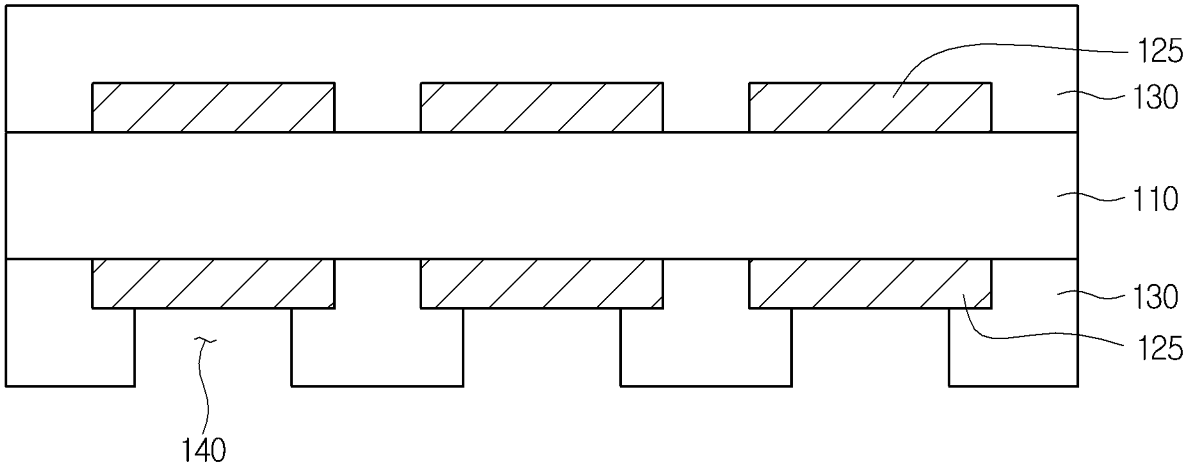
[Fig. 4]



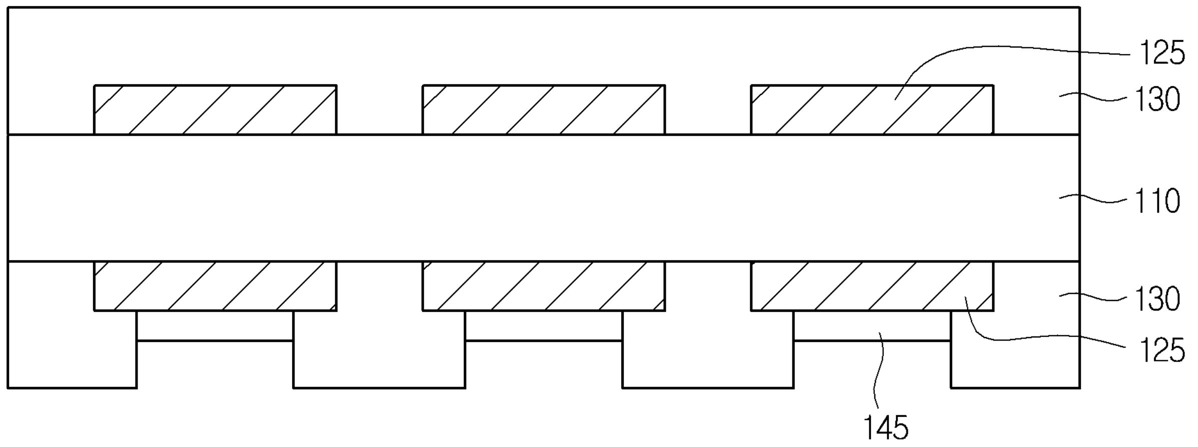
[Fig. 5]



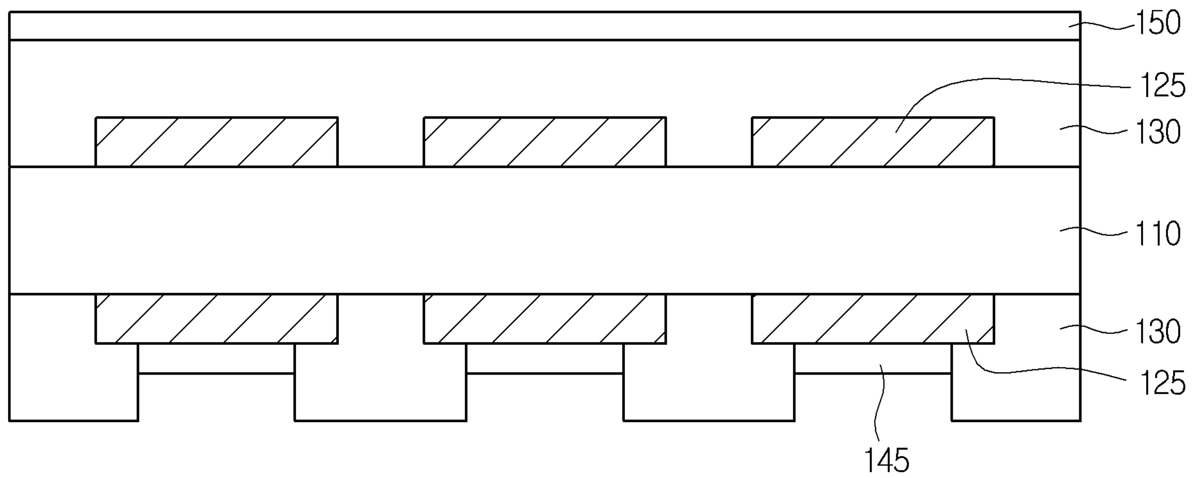
[Fig. 6]



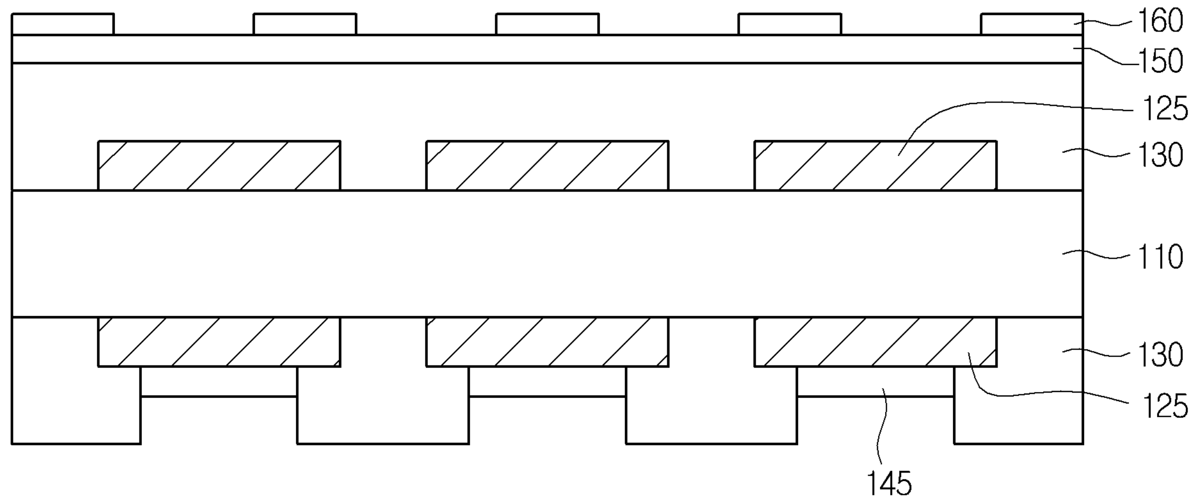
[Fig. 7]



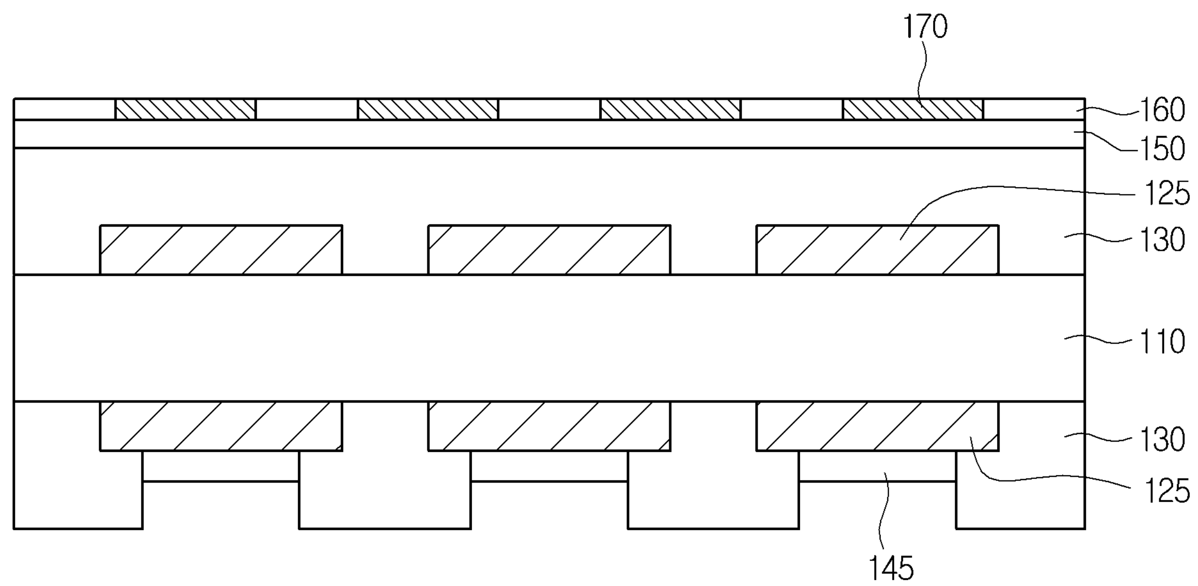
[Fig. 8]



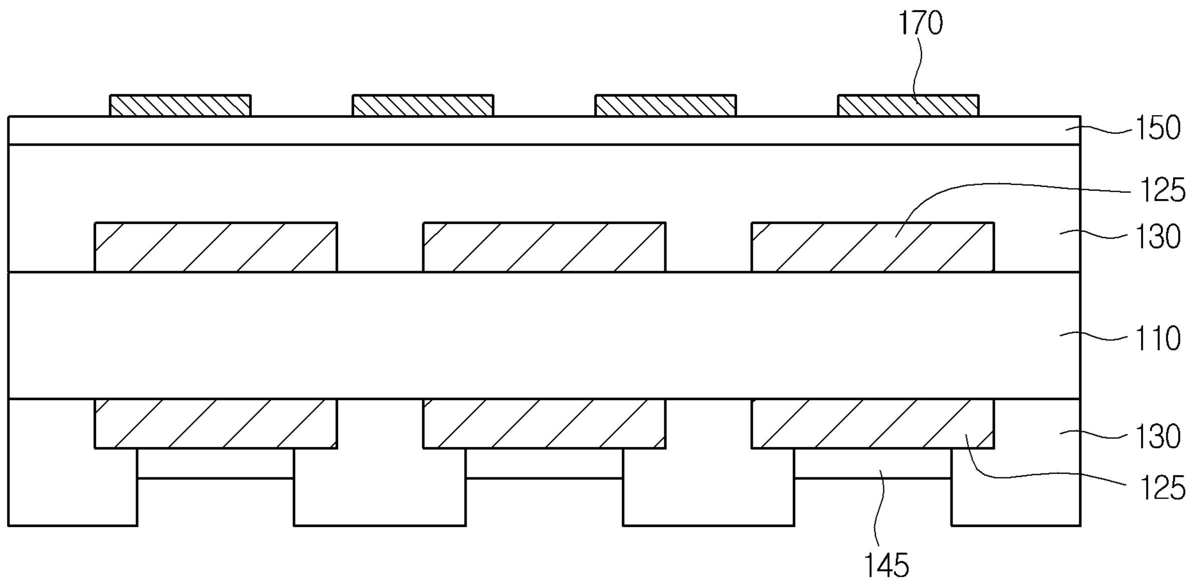
[Fig. 9]



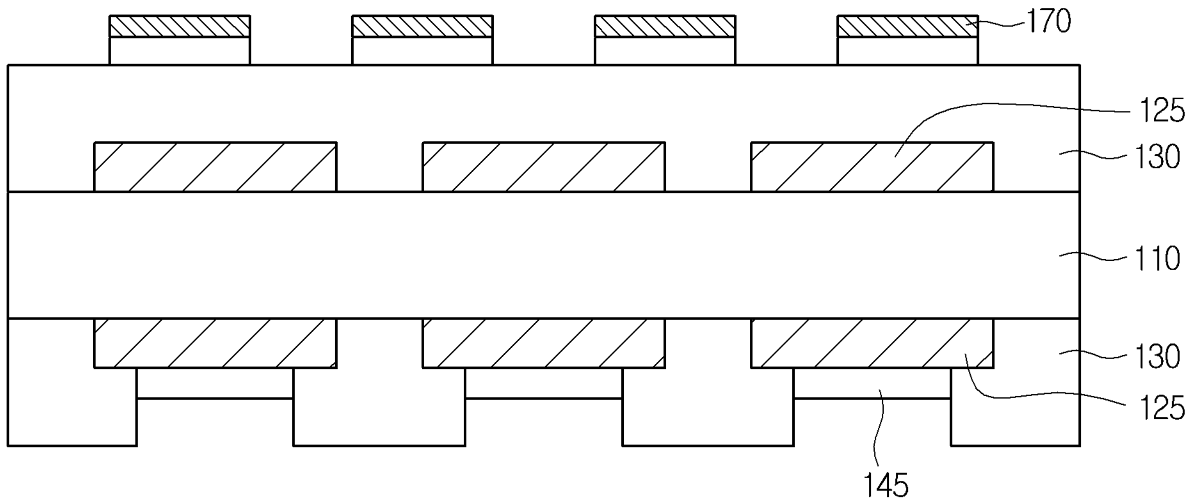
[Fig. 10]



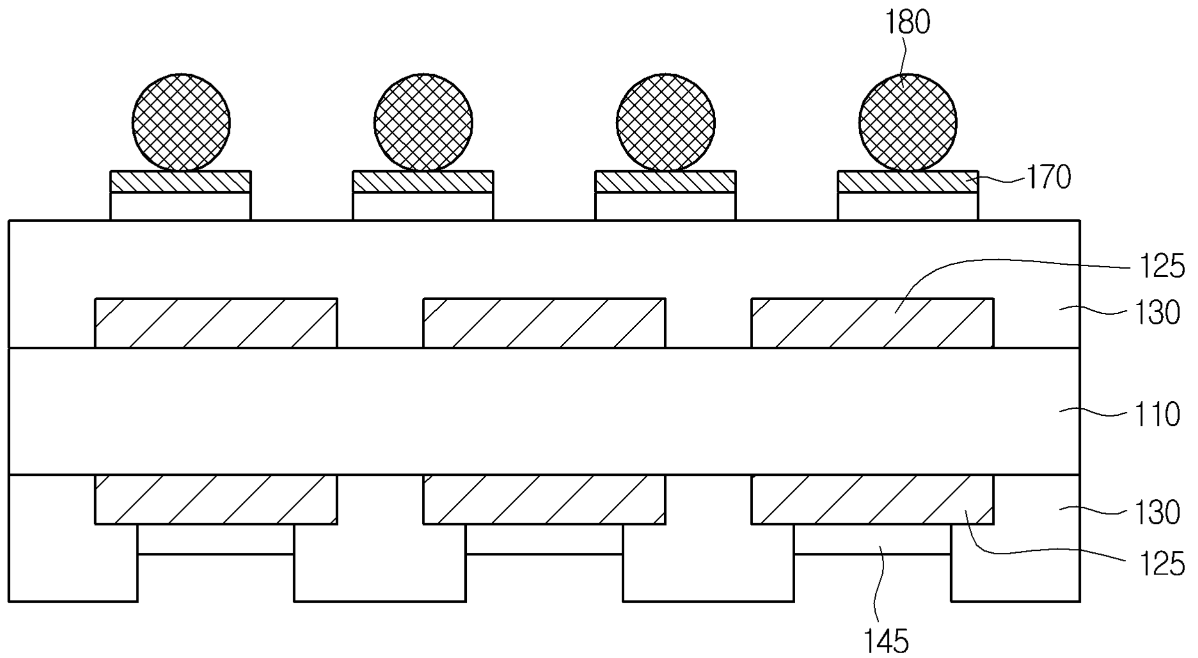
[Fig. 11]



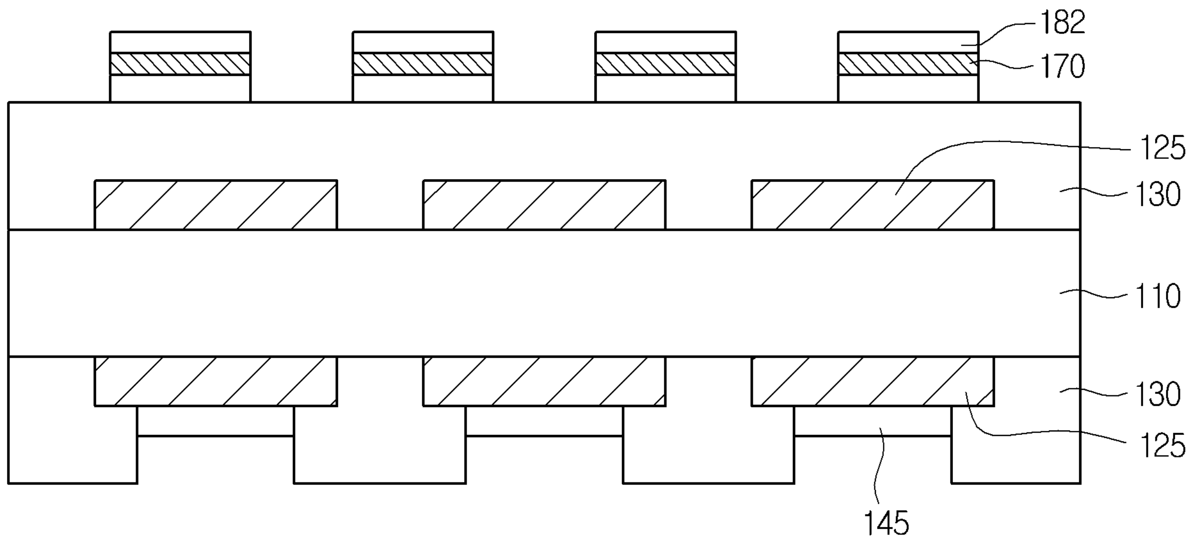
[Fig. 12]



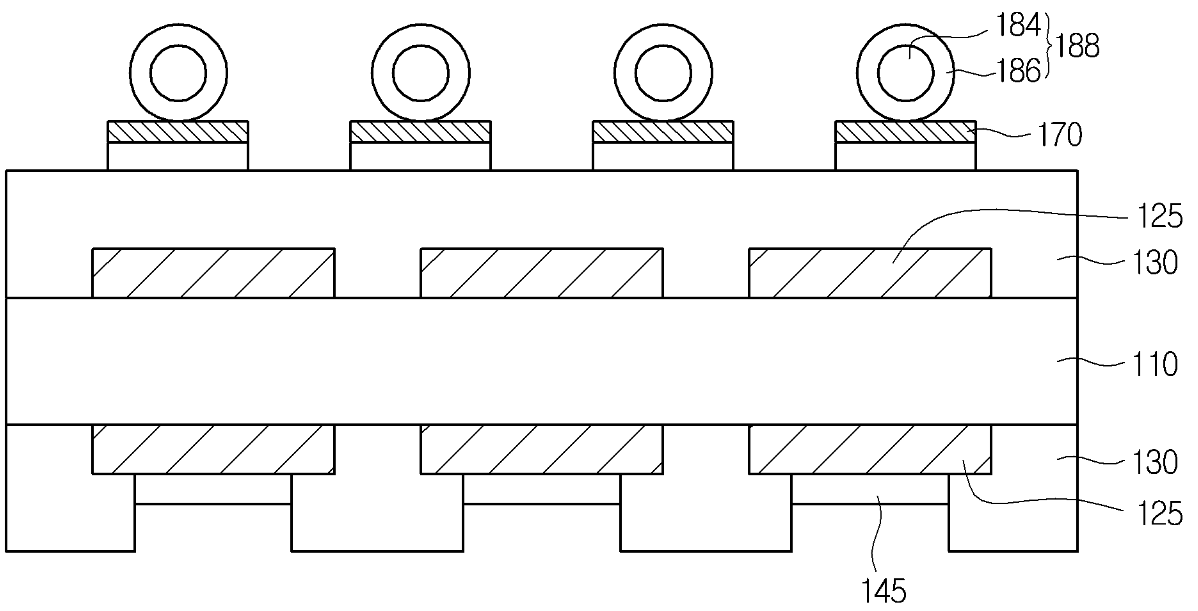
[Fig. 13]



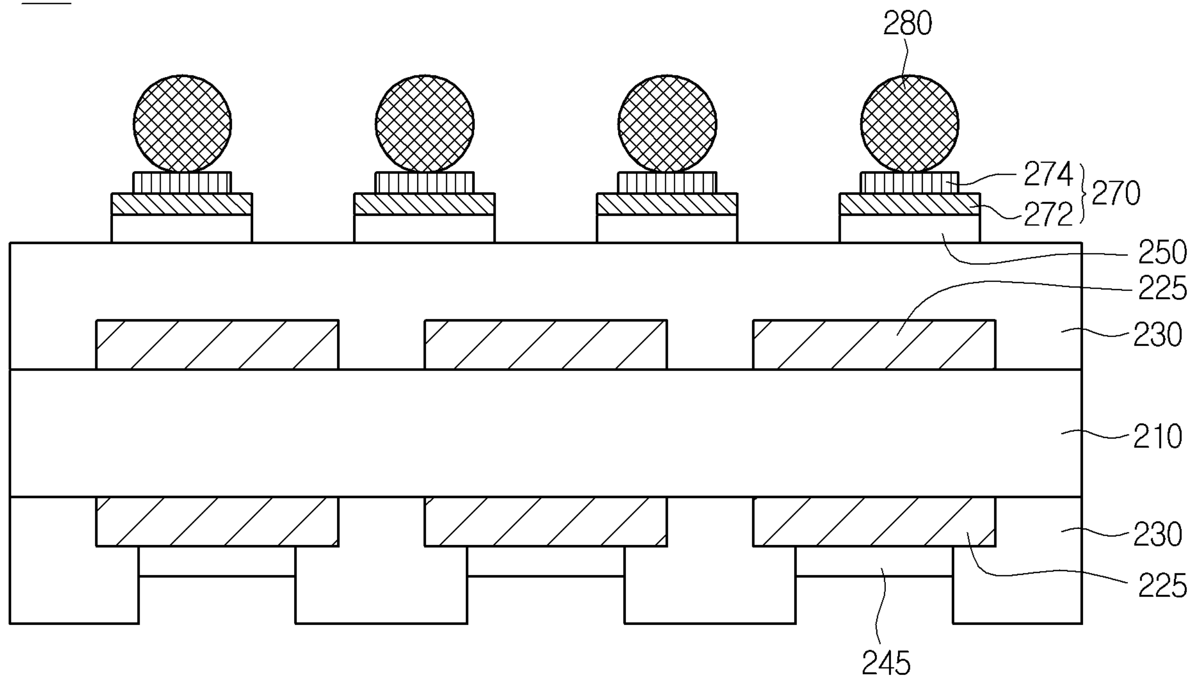
[Fig. 14]



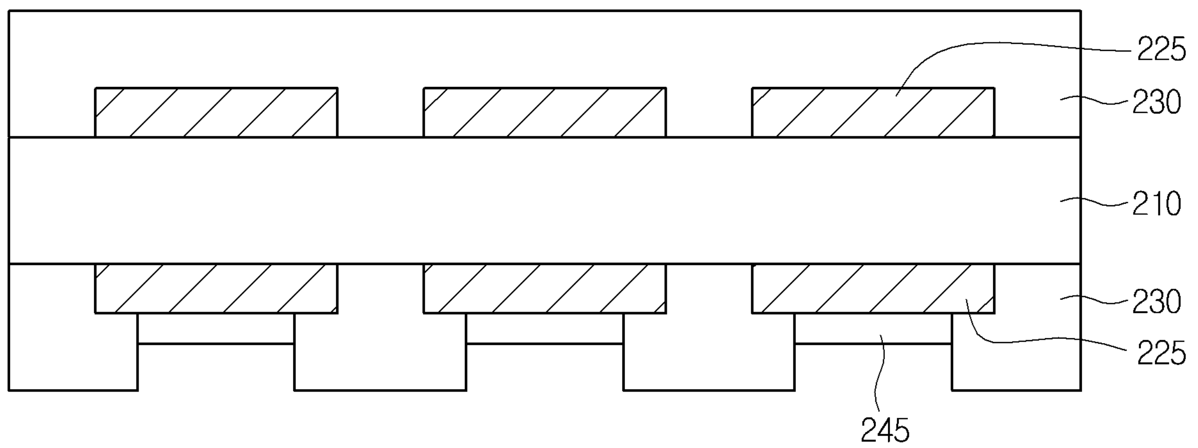
[Fig. 15]



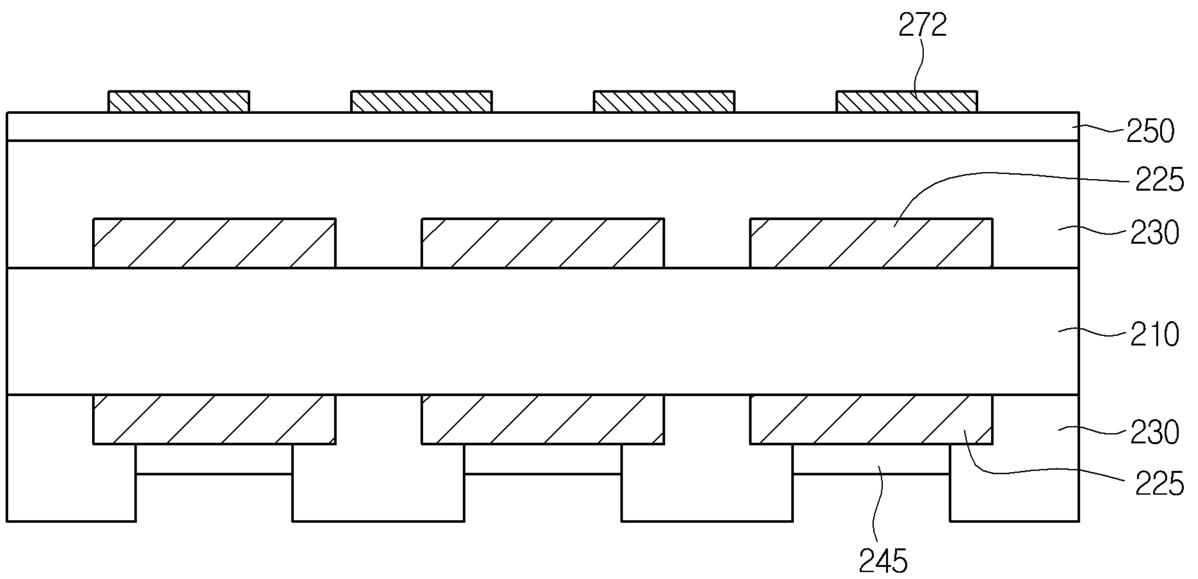
[Fig. 16]



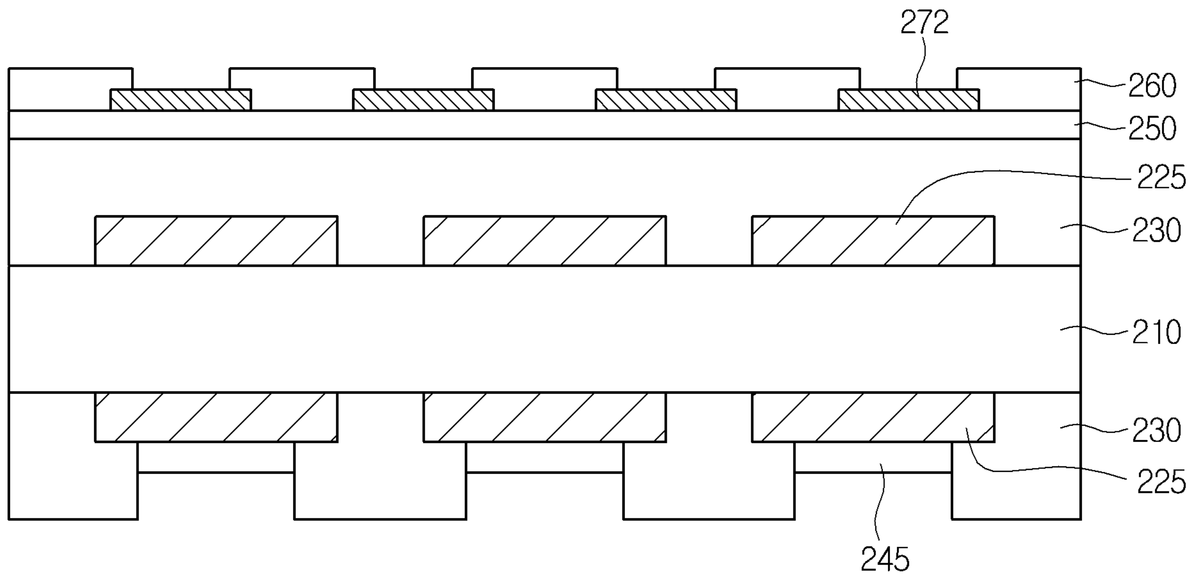
[Fig. 17]



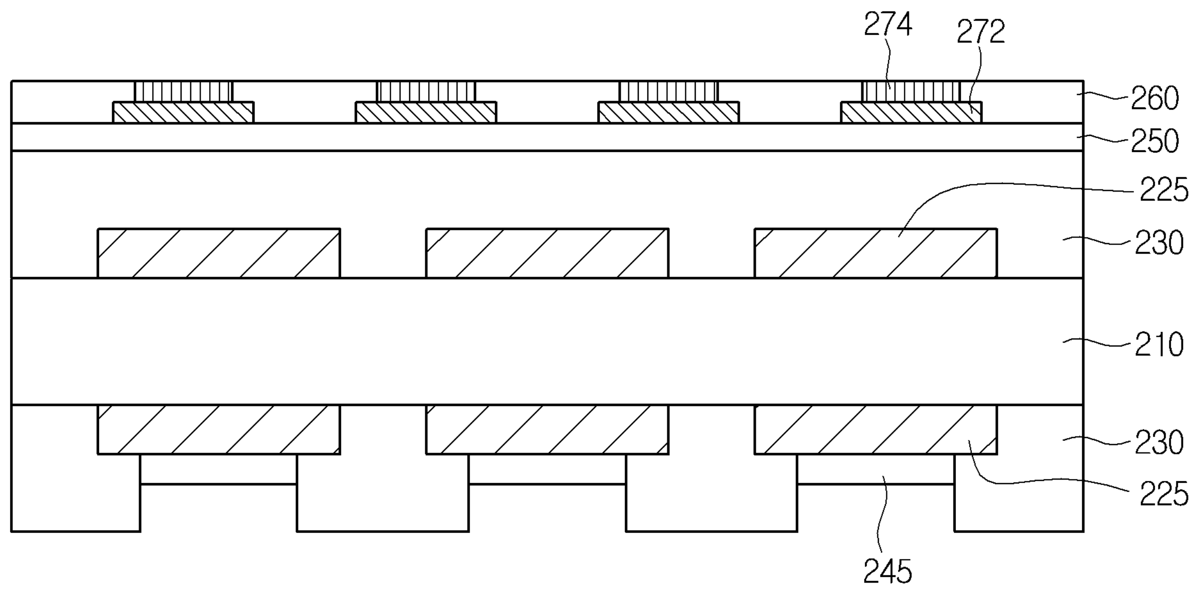
[Fig. 18]



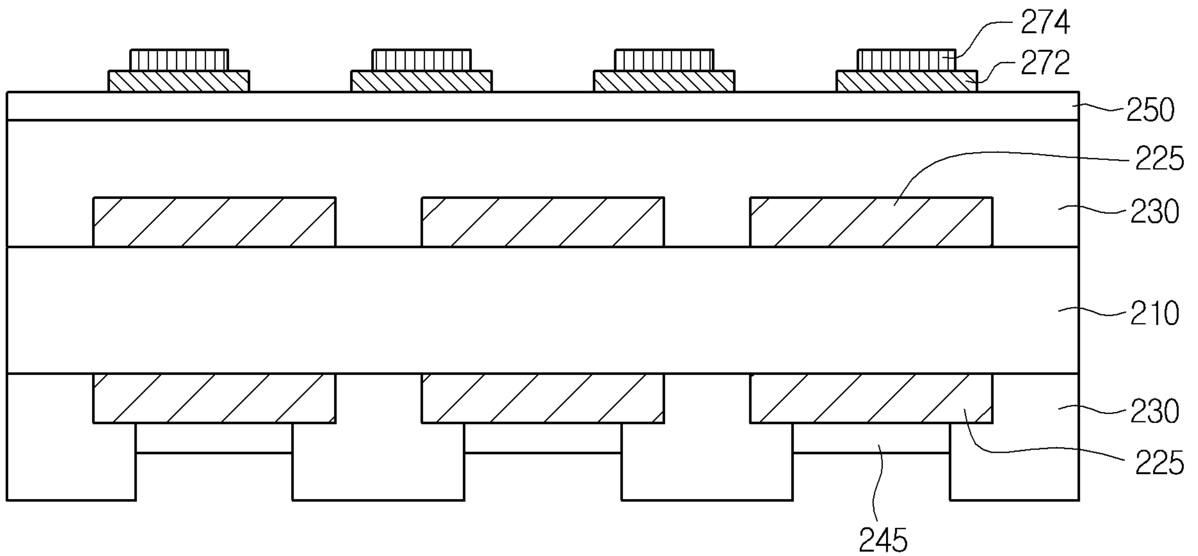
[Fig. 19]



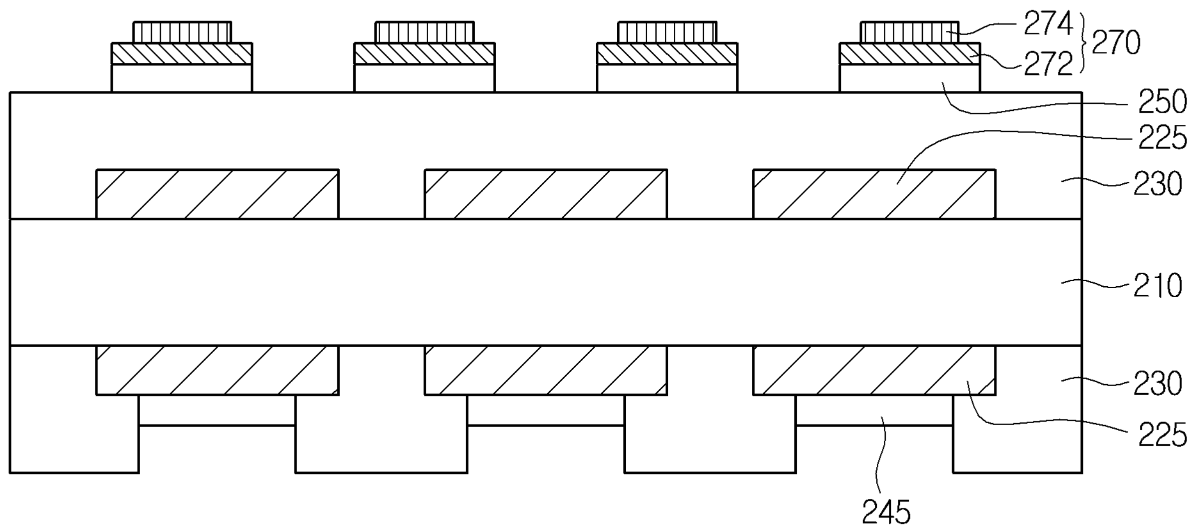
[Fig. 20]



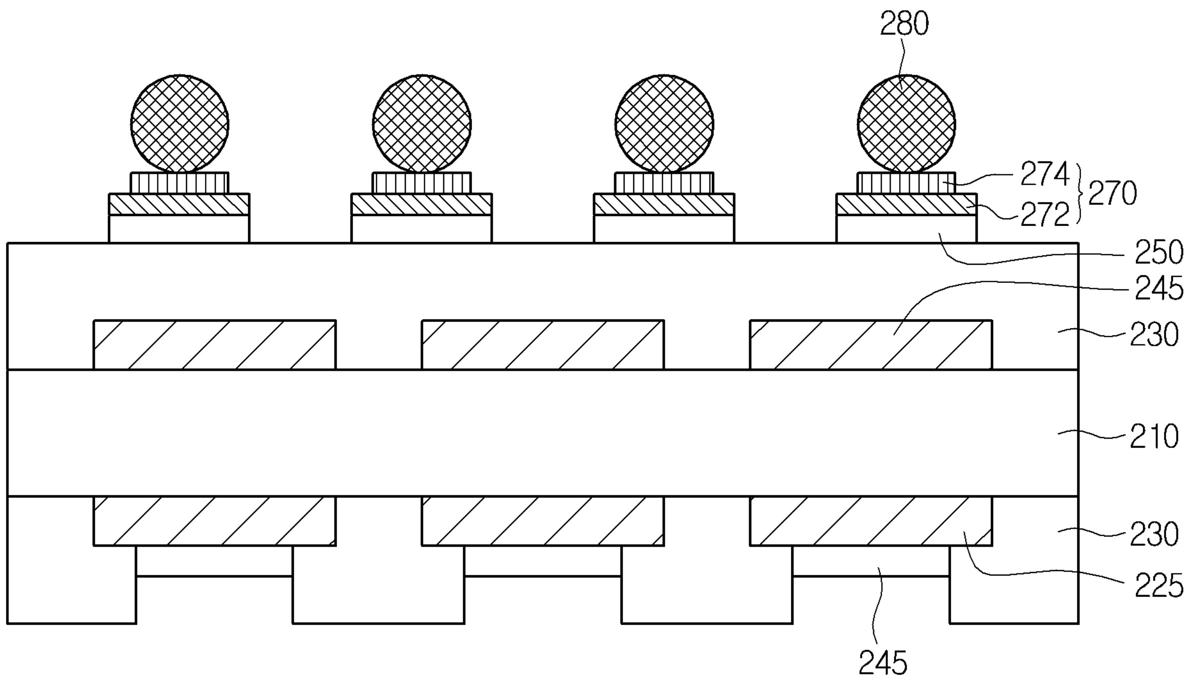
[Fig. 21]



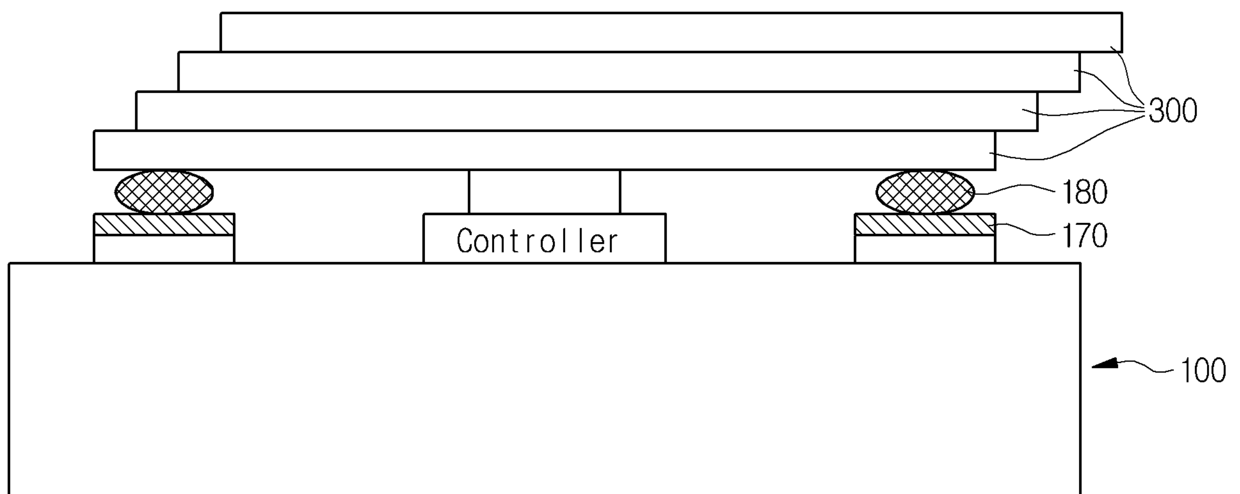
[Fig. 22]



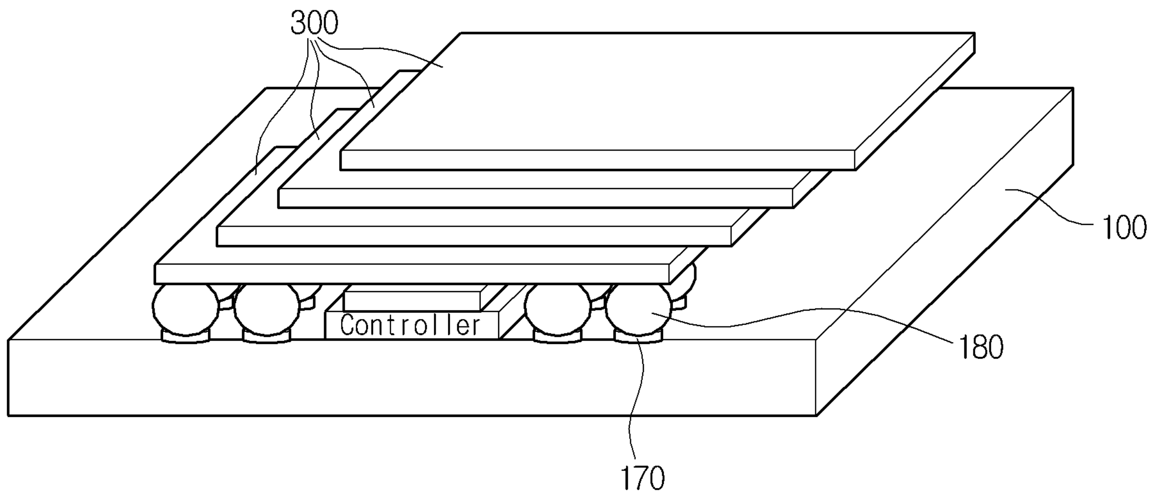
[Fig. 23]



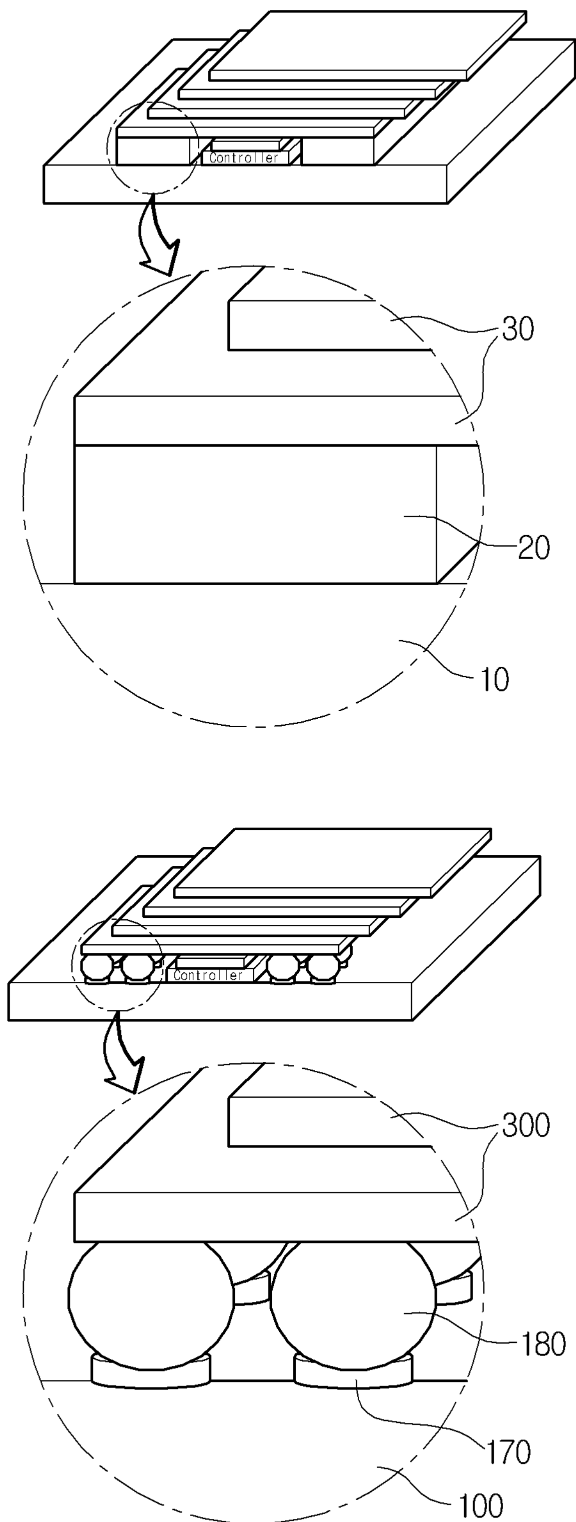
[Fig. 24]



[Fig. 25]



[Fig. 26]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2013/004578

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/12(2006.01)i, H01L 23/15(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/12; H01L 21/50; H05K 1/02; H01L 21/00; H01L 21/44; H01L 23/15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: substrate, protective layer, circuit pattern, package, pad width

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	JP 2003-110052 A (NEC TOPPAN CIRCUIT SOLUTIONS INC.) 11 April 2003 See abstract, paragraphs [0009]-[0012], claim 1 and figures 1-4.	1-3,7-11,14-15 4-6,12-13,16-23
A	KR 10-1067216 B1 (SAMSUNG ELECTRO-MECHANICS CO., LTD.) 22 September 2011 See abstract, paragraphs [0026]-[0036], claim 1 and figure 1.	1-23
A	US 2011-0003431 A1 (CHENG-TANG HUANG) 06 January 2011 See abstract, paragraphs [0047]-[0049] and figures 11, 21.	1-23
A	US 2006-0223230 A1 (SHIH-PING HSU et al.) 05 October 2006 See abstract, paragraphs [0054]-[0058] and figures 4-7.	1-23
A	US 2005-0095836 A1 (CHIA-HUNG LAI et al.) 05 May 2005 See abstract, paragraphs [0032]-[0037] and claim 1.	1-23

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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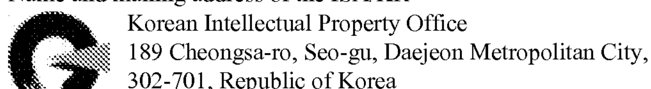
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 September 2013 (27.09.2013)	**27 September 2013 (27.09.2013)**

Name and mailing address of the ISA/KR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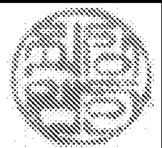
Authorized officer

CHOI Sang Won



Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2013/004578

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2003-110052 A	11/04/2003	None	
KR 10-1067216 B1	22/09/2011	US 2011-0286191 A1	24/11/2011
		US 8253034 B2	28/08/2012
US 2011-0003431 A1	06/01/2011	TW 200952092 A	16/12/2009
		TW I387014 B	21/02/2013
		US 2009-0302465 A1	10/12/2009
US 2006-0223230 A1	05/10/2006	JP 2005-064498 A	10/03/2005
		JP 4682294 B2	11/05/2011
		TW 286372 B	01/09/2007
		TW I286372 B	01/09/2007
		US 2005-0037601 A1	17/02/2005
		US 2006-0226544 A1	12/10/2006
		US 7081402 B2	25/07/2006
		US 7485970 B2	03/02/2009
US 2005-0095836 A1	05/05/2005	CN 1574321 A	02/02/2005
		CN 1574321 B	28/04/2010
		CN 1574321 C	28/04/2010
		CN 1574321 C0	02/02/2005
		CN 2720634 Y0	24/08/2005
		SG 115593 A1	28/10/2005
		TW 222710 A	21/10/2004
		TW 222710 B	21/10/2004
		TW I222710 B	21/10/2004
		US 2004-0235223 A1	25/11/2004
		US 6844626 B2	18/01/2005
		US 7015129 B2	21/03/2006