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(12) **Reissued Patent**
Nakano

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(54) **SEMICONDUCTOR DEVICE**

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(72) Inventor: **Yuki Nakano**, Kyoto (JP)

(73) Assignee: **ROHM CO., LTD.**, Kyoto (JP)

(*) Notice: This patent is subject to a terminal disclaimer.

(21) Appl. No.: **15/933,357**

(22) Filed: **Mar. 22, 2018**

Related U.S. Patent Documents

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Issued: **Mar. 22, 2016**
Appl. No.: **13/364,416**
Filed: **Feb. 2, 2012**

U.S. Applications:
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(30) **Foreign Application Priority Data**

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Dec. 26, 2008 (JP) 2008-334480
Dec. 24, 2009 (JP) 2009-293361

(51) **Int. Cl.**
H01L 29/16 (2006.01)
H01L 29/45 (2006.01)
H01L 29/78 (2006.01)
H01L 29/66 (2006.01)
H01L 29/06 (2006.01)
H01L 29/417 (2006.01)
H01L 29/423 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/7813*** (2013.01); ***H01L 29/45*** (2013.01); ***H01L 29/66068*** (2013.01); ***H01L 29/7802*** (2013.01); ***H01L 29/7803*** (2013.01); *H01L 29/0696* (2013.01); *H01L 29/41766* (2013.01); *H01L 29/42368* (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/7813; H01L 29/7802; H01L 29/7803; H01L 29/7805; H01L 29/66068; H01L 29/1095; H01L 29/45; H01L 29/16; H01L 23/544
USPC 257/77, 330, 382; 438/326, 330
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,278,099 A 1/1994 Maeda
5,466,971 A 11/1995 Higuchi
(Continued)

FOREIGN PATENT DOCUMENTS

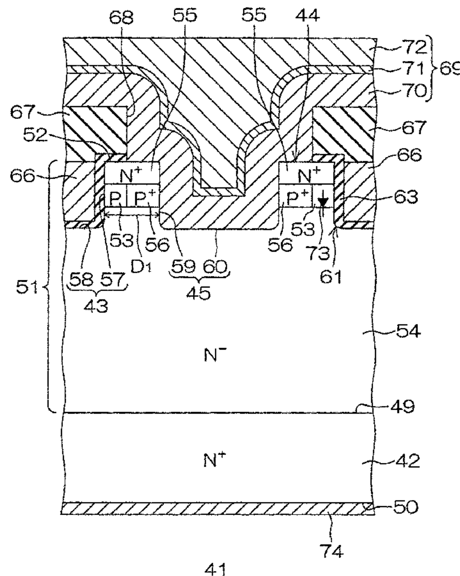
CN 101174569 A 5/2008
JP 60-123060 7/1985
(Continued)

Primary Examiner — Tuan H. Nguyen
(74) *Attorney, Agent, or Firm* — Hamre, Schumann, Mueller & Larson, P.C.

(57) **ABSTRACT**

The semiconductor device according to the present invention includes: a semiconductor layer made of SiC; an impurity region formed by doping the semiconductor layer with an impurity; and a contact wire formed on the semiconductor layer in contact with the impurity region, while the contact wire has a polysilicon layer in the portion in contact with the impurity region, and has a metal layer on the polysilicon layer.

21 Claims, 49 Drawing Sheets



(56) References Cited

U.S. PATENT DOCUMENTS

Number	Kind	Date	Name	Class
5,614,749	A	3/1997	Ueno	
5,719,409	A *	2/1998	Singh	H01L 29/1095 257/77
5,831,288	A *	11/1998	Singh et al.	257/77
5,905,294	A	5/1999	Kushida	
6,124,144	A	9/2000	Watanabe	
6,159,839	A	12/2000	Jeng et al.	
6,228,720	B1	5/2001	Kitabatake et al.	
6,342,709	B1	1/2002	Sugawara et al.	
6,362,495	B1 *	3/2002	Schoen et al.	257/77
6,599,644	B1 *	7/2003	Zekentes et al.	428/627
6,649,973	B2	11/2003	Takaishi	
6,822,288	B2	11/2004	Hshieh et al.	
7,645,658	B2	1/2010	Nakamura et al.	
7,714,352	B2	5/2010	Shimoida et al.	
7,824,995	B2	11/2010	Endo et al.	
8,035,112	B1 *	10/2011	Cooper et al.	257/77
8,044,434	B2	10/2011	Ohta et al.	
8,415,250	B2	4/2013	Alptekin et al.	
8,487,318	B2	7/2013	Nakano	
8,623,752	B2	1/2014	Fujikawa et al.	
8,872,263	B2 *	10/2014	Nakano	H01L 29/1608 257/330
2002/0132473	A1 *	9/2002	Chiang et al.	438/643
2002/0175383	A1 *	11/2002	Kocon et al.	257/376
2004/0079989	A1	4/2004	Kaneko et al.	
2004/0145011	A1 *	7/2004	Hsu et al.	257/330
2004/0217358	A1	11/2004	Kaneko	
2005/0012143	A1 *	1/2005	Tanaka et al.	257/328
2005/0045892	A1 *	3/2005	Hayashi et al.	257/77
2005/0062048	A1 *	3/2005	Hayashi et al.	257/77
2005/0077569	A1	4/2005	Yamashita et al.	
2005/0133794	A1	6/2005	Hayashi et al.	
2005/0167742	A1 *	8/2005	Challa et al.	257/328
2005/0173739	A1 *	8/2005	Kusumoto et al.	257/263
2005/0199873	A1 *	9/2005	Tanaka et al.	257/20
2005/0199953	A1 *	9/2005	Kawamura et al.	257/341
2005/0218472	A1	10/2005	Okada et al.	
2006/0178016	A1	8/2006	Zhang	
2006/0267090	A1	11/2006	Sapp et al.	
2006/0273382	A1 *	12/2006	Hshieh	H01L 24/26 257/330
2007/0007537	A1	1/2007	Ogura et al.	
2007/0034901	A1	2/2007	Lui et al.	
2007/0114574	A1	5/2007	Onose	
2007/0138545	A1	6/2007	Lin et al.	
2007/0138548	A1	6/2007	Kocon et al.	
2007/0181886	A1	8/2007	Shimoida et al.	
2007/0241338	A1	10/2007	Yamamoto et al.	
2007/0262324	A1 *	11/2007	Kaneko	257/77
2008/0029812	A1	2/2008	Bhalla	
2008/0081422	A1 *	4/2008	Kobayashi et al.	438/270
2008/0099768	A1 *	5/2008	Scarsbrook et al.	257/77
2008/0102585	A1	5/2008	Nakamura et al.	
2008/0197361	A1 *	8/2008	Ueno	257/77
2008/0197407	A1	8/2008	Challa et al.	
2008/0197411	A1	8/2008	Korec et al.	
2008/0203402	A1	8/2008	Endo et al.	
2008/0246086	A1	10/2008	Korec et al.	
2009/0032821	A1	2/2009	Onose et al.	
2009/0066589	A1	3/2009	Yamazaki et al.	
2009/0072301	A1	3/2009	Bhalla et al.	H01L 29/407 257/328
2009/0140262	A1 *	6/2009	Ohki et al.	257/76
2009/0140326	A1	6/2009	Konstantinov et al.	
2009/0140327	A1	6/2009	Hirao et al.	
2009/0179264	A1	7/2009	Korec et al.	
2009/0212359	A1 *	8/2009	Hsieh	257/331
2009/0225578	A1	9/2009	Kitabatake	
2009/0272982	A1 *	11/2009	Nakamura et al.	257/77
2009/0283776	A1 *	11/2009	Iwamuro	257/76
2009/0315106	A1 *	12/2009	Hsieh	257/334
2009/0315107	A1 *	12/2009	Hsieh	257/334
2010/0006861	A1	1/2010	Yamamoto et al.	
2010/0025730	A1 *	2/2010	Heikman et al.	257/194
2010/0044796	A1	2/2010	Hshieh	
2010/0052014	A1	3/2010	Matsushita	
2010/0075474	A1	3/2010	Kudou et al.	
2010/0102331	A1	4/2010	Fujikawa et al.	
2010/0118455	A1	5/2010	Kusunoki	
2010/0193796	A1	8/2010	Nakano	
2010/0193799	A1	8/2010	Nakano et al.	
2010/0224884	A1 *	9/2010	Seki et al.	257/77
2010/0224886	A1	9/2010	Iwamuro	
2011/0042727	A1	2/2011	Pan et al.	
2011/0175111	A1 *	7/2011	Harada et al.	257/77
2011/0207321	A1 *	8/2011	Fujiwara et al.	438/663
2011/0284874	A1	11/2011	Miura et al.	
2012/0012861	A1	1/2012	Nakano et al.	
2012/0049202	A1	3/2012	Nakano	
2013/0026568	A1	1/2013	Bhalla	
2013/0119483	A1	5/2013	Alptekin et al.	
2013/0234159	A1	9/2013	Tsuchiya	
2013/0285072	A1	10/2013	Iwamuro	
2014/0015019	A1 *	1/2014	Okamoto et al.	257/288

FOREIGN PATENT DOCUMENTS

Country	Number	Kind	Date
JP	60-169169		9/1985
JP	63-229852		9/1988
JP	H1-094672	A	4/1989
JP	H01-094672	A	4/1989
JP	03-163832		7/1991
JP	H03252166		11/1991
JP	H06-77163	A	3/1994
JP	H06232074	A	8/1994
JP	H0864802	A	3/1996
JP	H08204179	A	8/1996
JP	H10-98188	A	4/1998
JP	2000-312003	A	11/2000
JP	2000332239	A	11/2000
JP	2001-119025	A	4/2001
JP	2002261275	A	9/2002
JP	2003174167		6/2003
JP	2003-318388	A	11/2003
JP	2003318396		11/2003
JP	2004-031471	A	1/2004
JP	2005-101255	A	4/2005
JP	2005-183563	A	7/2005
JP	2005-285913	A	10/2005
JP	2006024880	A	1/2006
JP	2006-066770	A	3/2006
JP	WO-2006086636	A2	8/2006
JP	2006-332358	A	12/2006
JP	2007180118	A	7/2007
JP	2007-214355	A	8/2007
JP	2007-258465	A	10/2007
JP	2008-017237	A	1/2008
JP	2008-117923	A	5/2008
JP	2008-530800	A	8/2008
JP	2008227441	A	9/2008
JP	2008-244455	A	10/2008
JP	2008270656		11/2008
JP	2009-088326	A	4/2009
JP	2009-135360	A	6/2009
JP	2010-171417	A	8/2010
WO	WO-2006/086636	A2	8/2006

* cited by examiner

FIG. 1

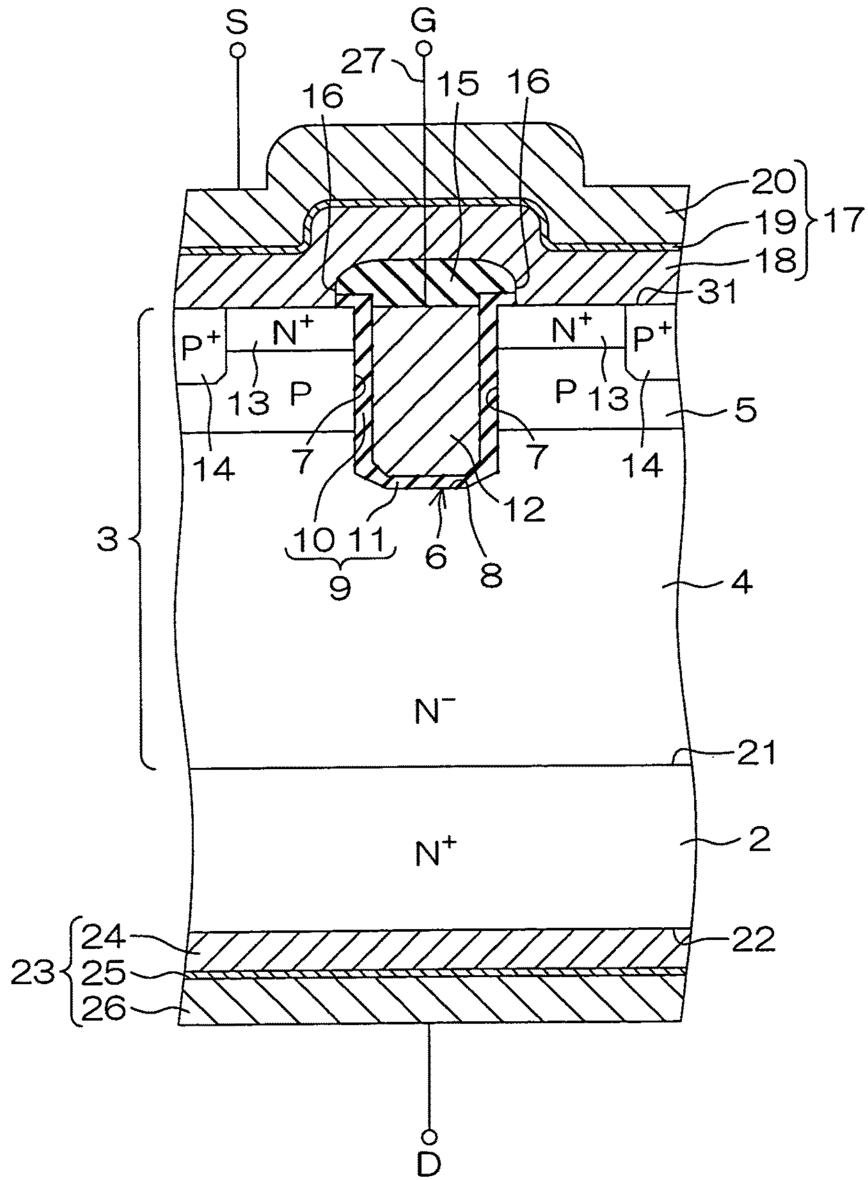


FIG. 2A

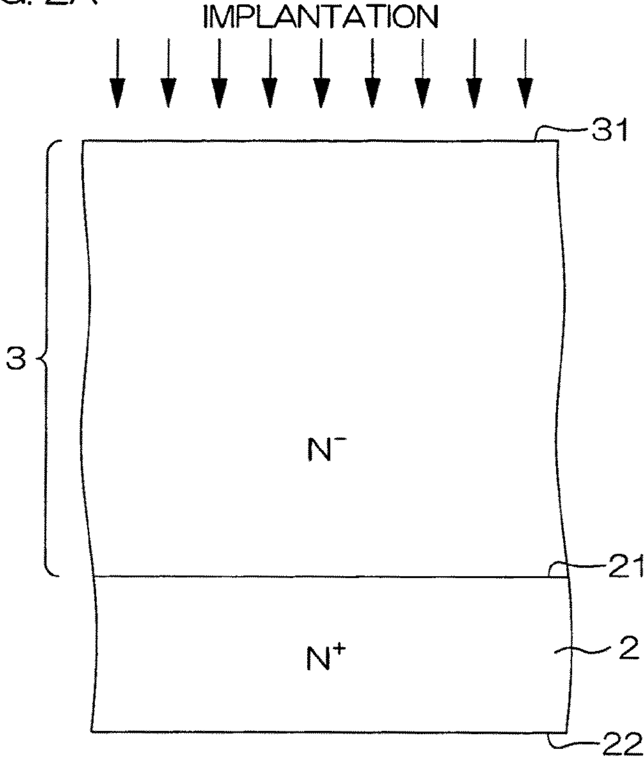


FIG. 2B

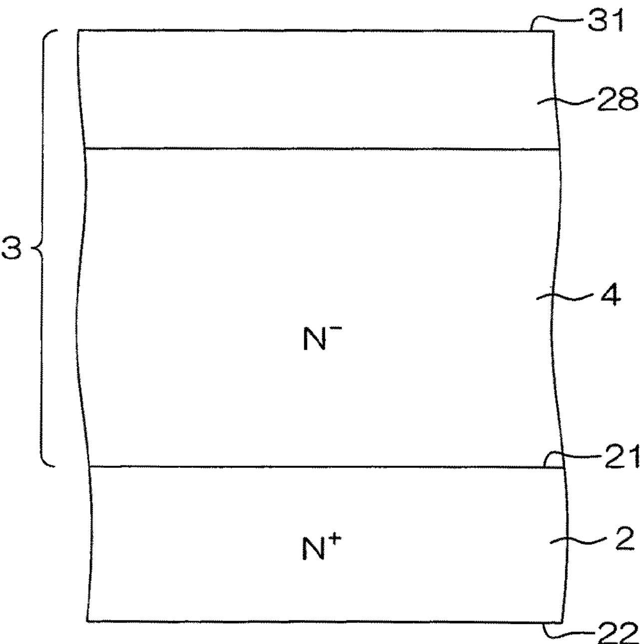


FIG. 2C

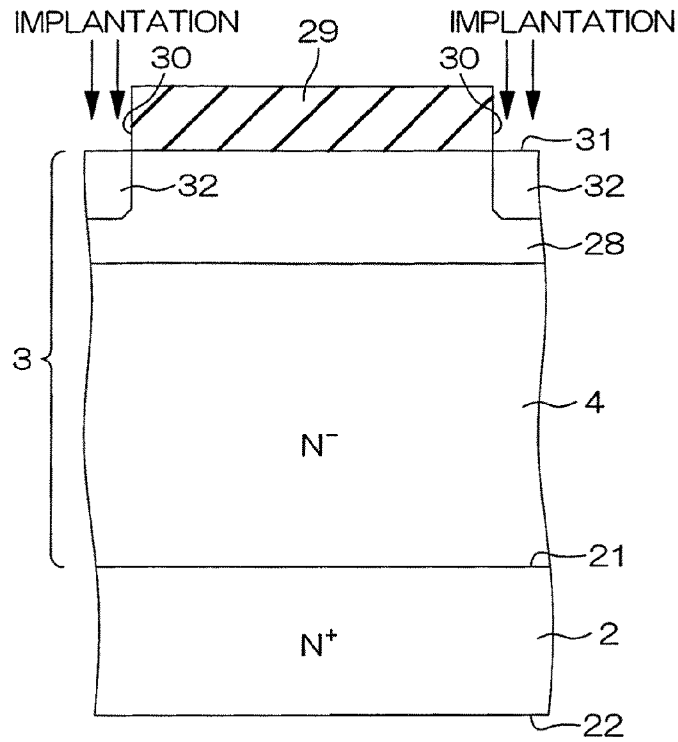


FIG. 2D

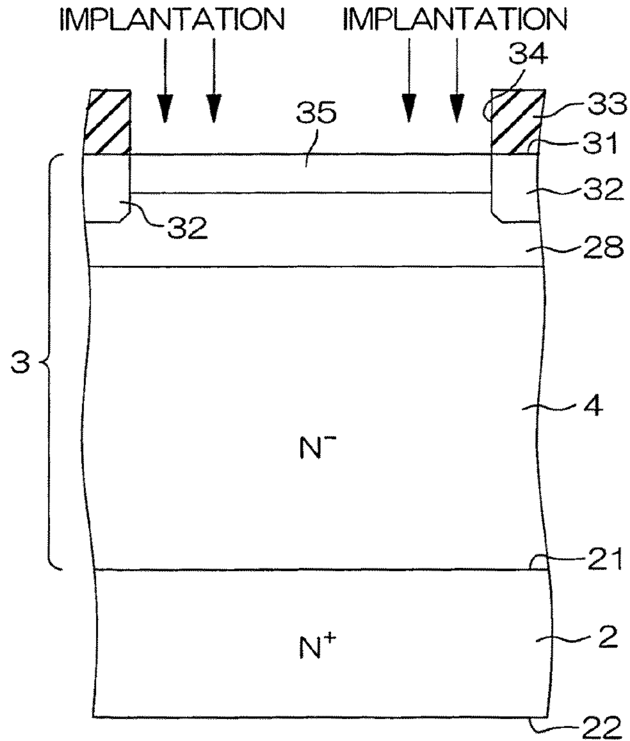


FIG. 2E

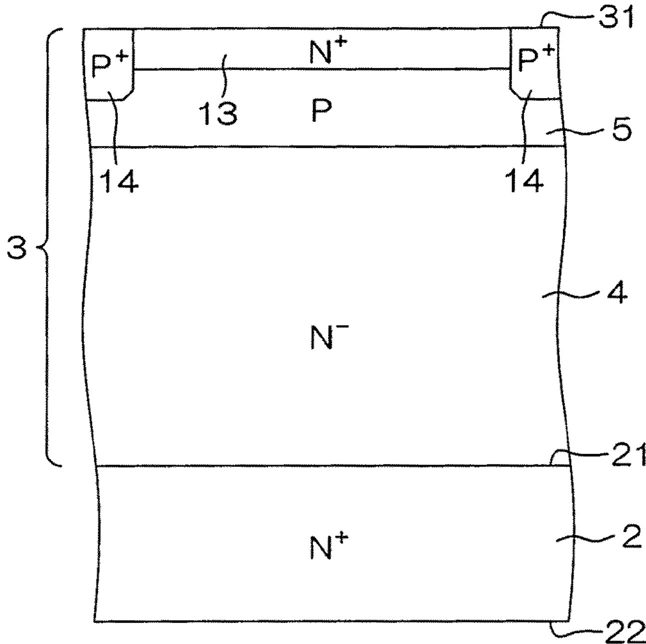


FIG. 2F

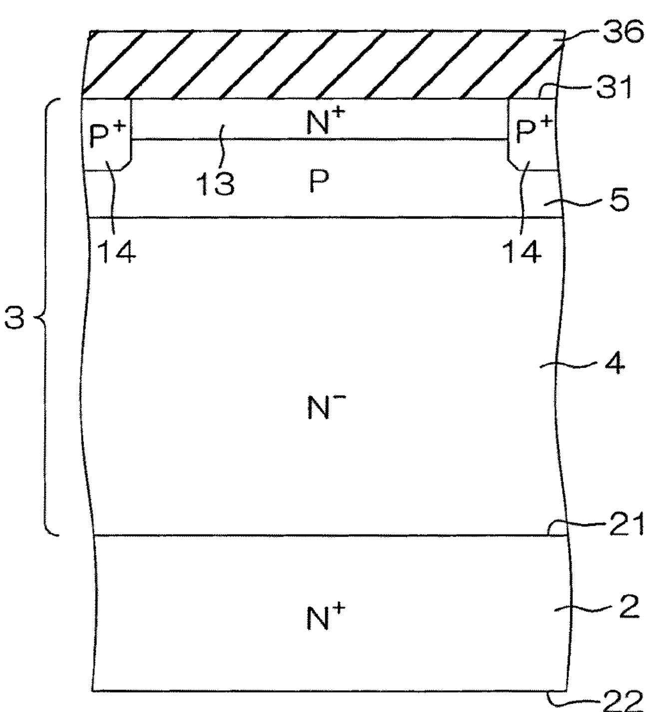


FIG. 2G

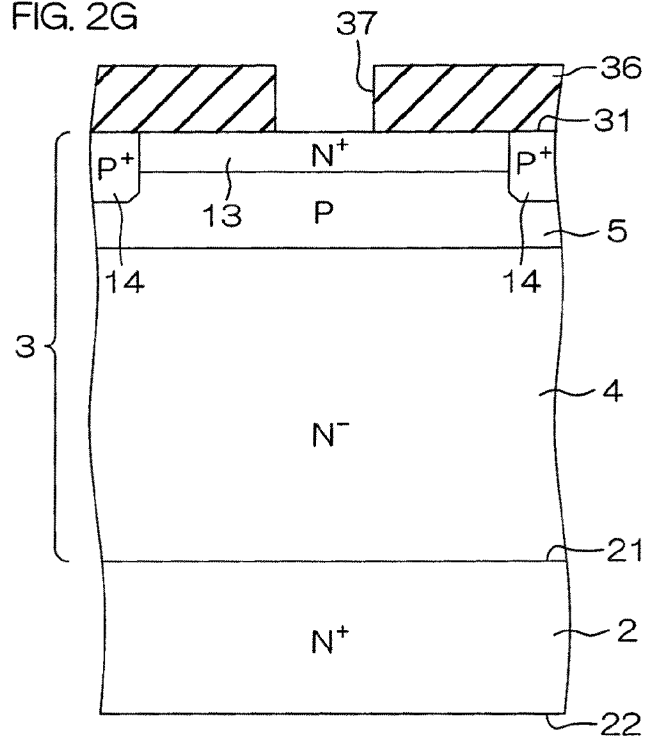


FIG. 2H

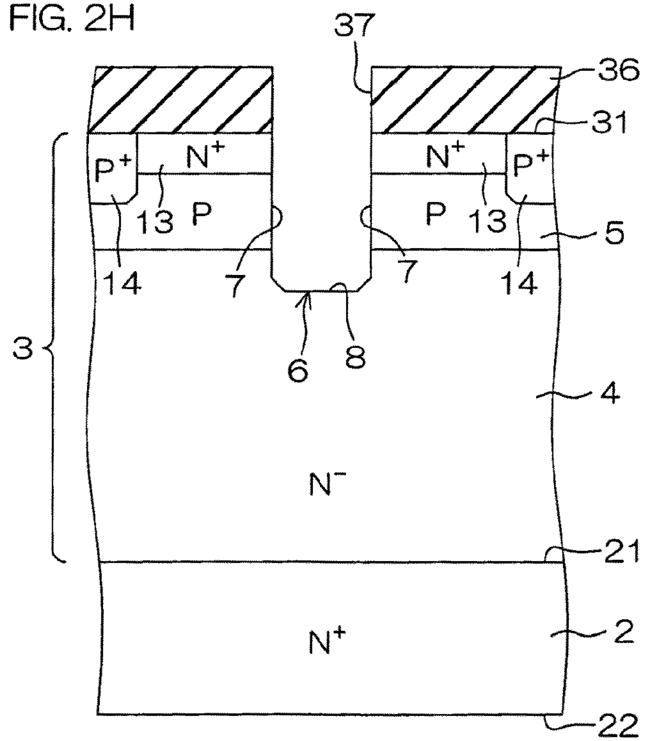


FIG. 2I

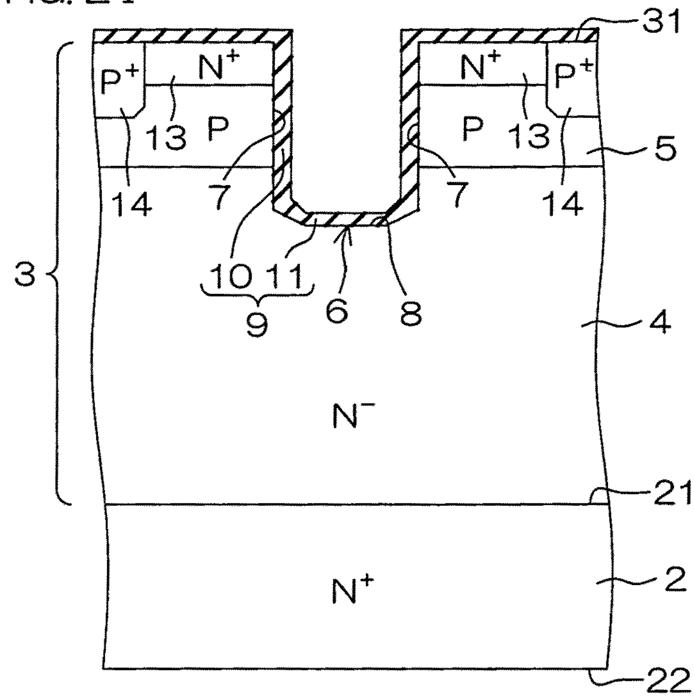


FIG. 2J

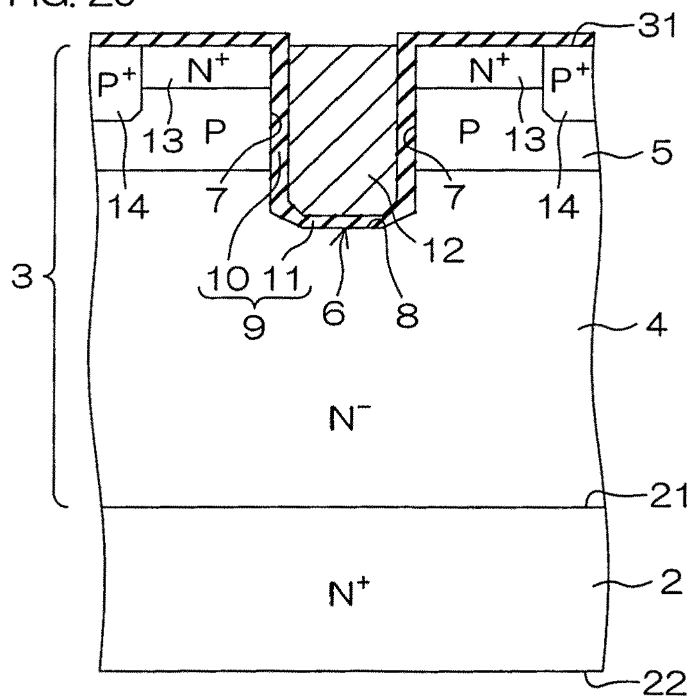


FIG. 2K

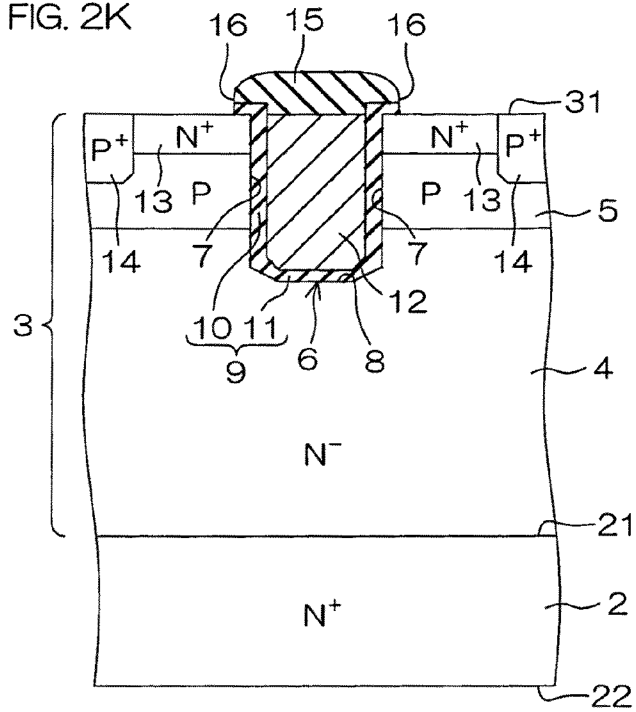


FIG. 2L

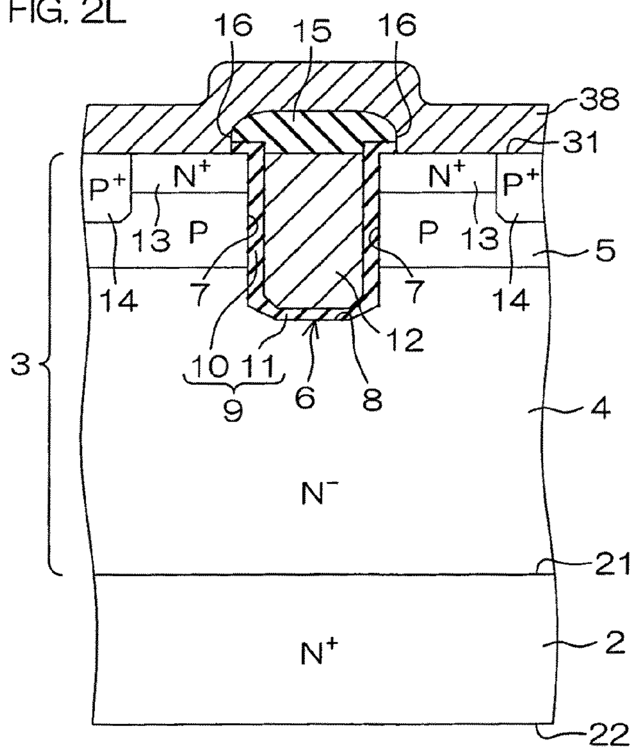
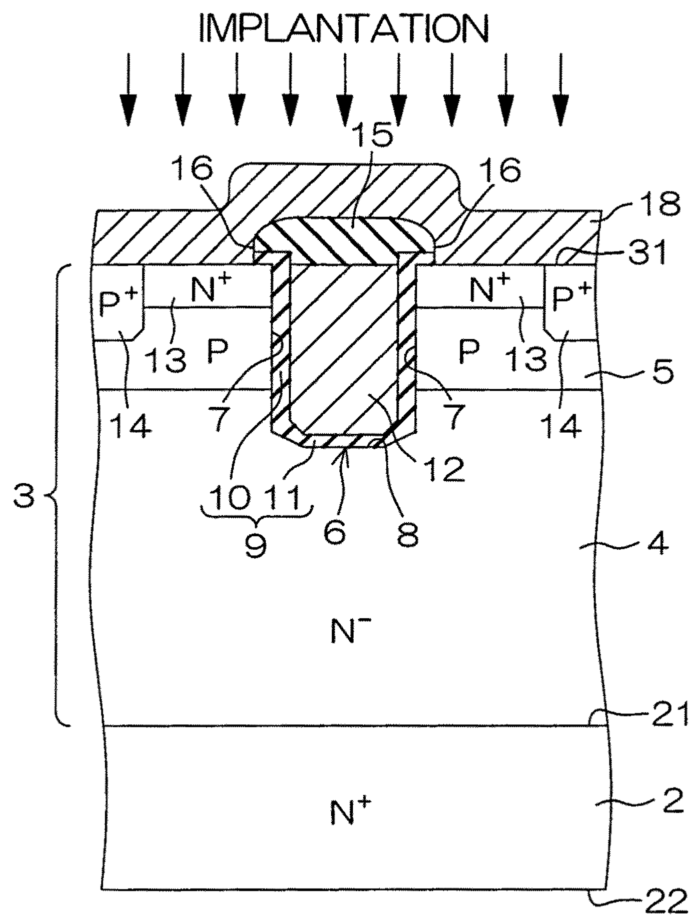


FIG. 2M



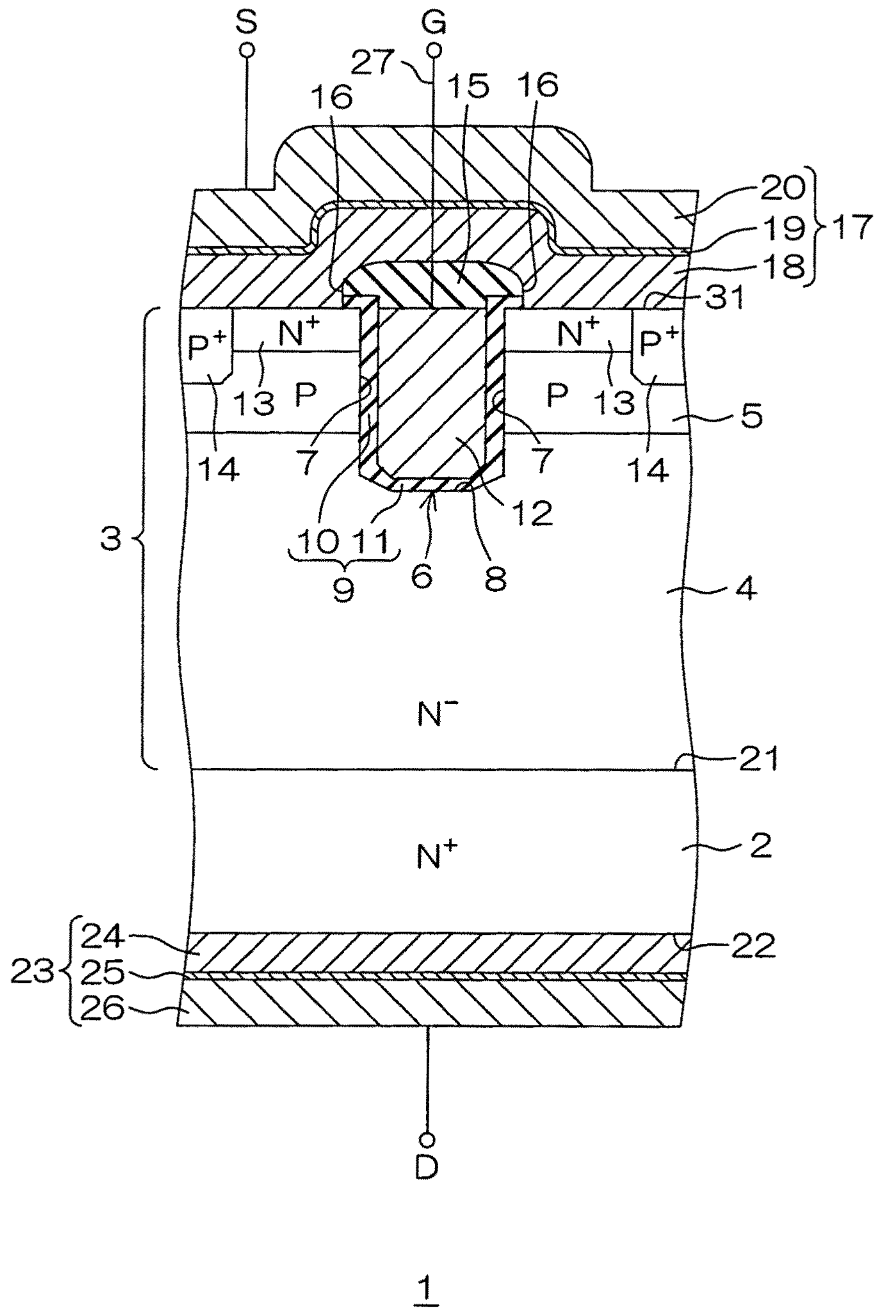


FIG. 2N
S
G
27
16
15
16
20
19
17
18
31
N+
P+
N+
P+
13
P
P
13
5
14
7
7
14
12
3
10 11
9
6
8
4
N−
21
N+
2
24
22
23
25
26
D
1

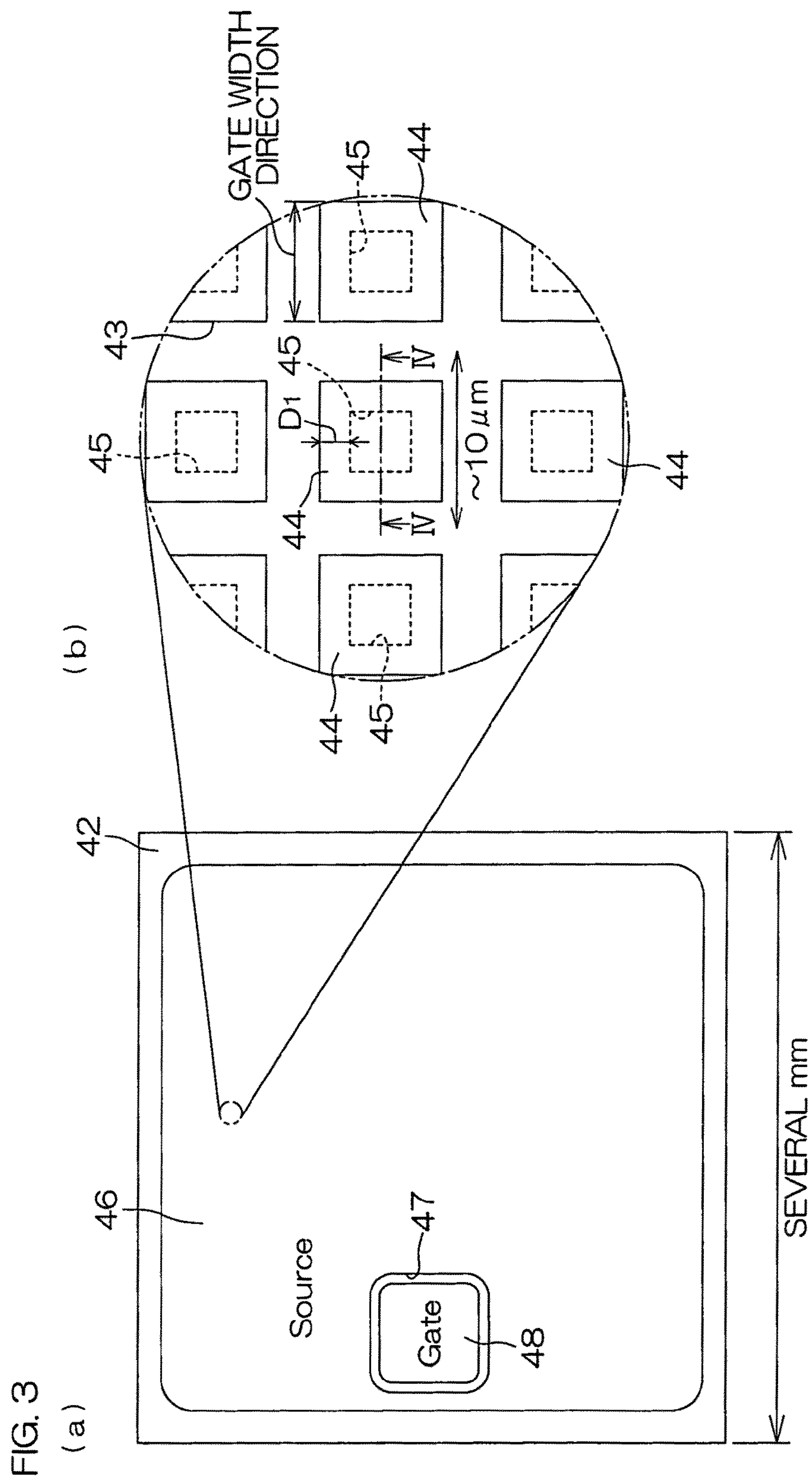


FIG. 3
(a)
(b)
GATE WIDTH DIRECTION
43
44
45
D1
IV
~10μm
42
46
Source
47
Gate
48
SEVERAL mm
41

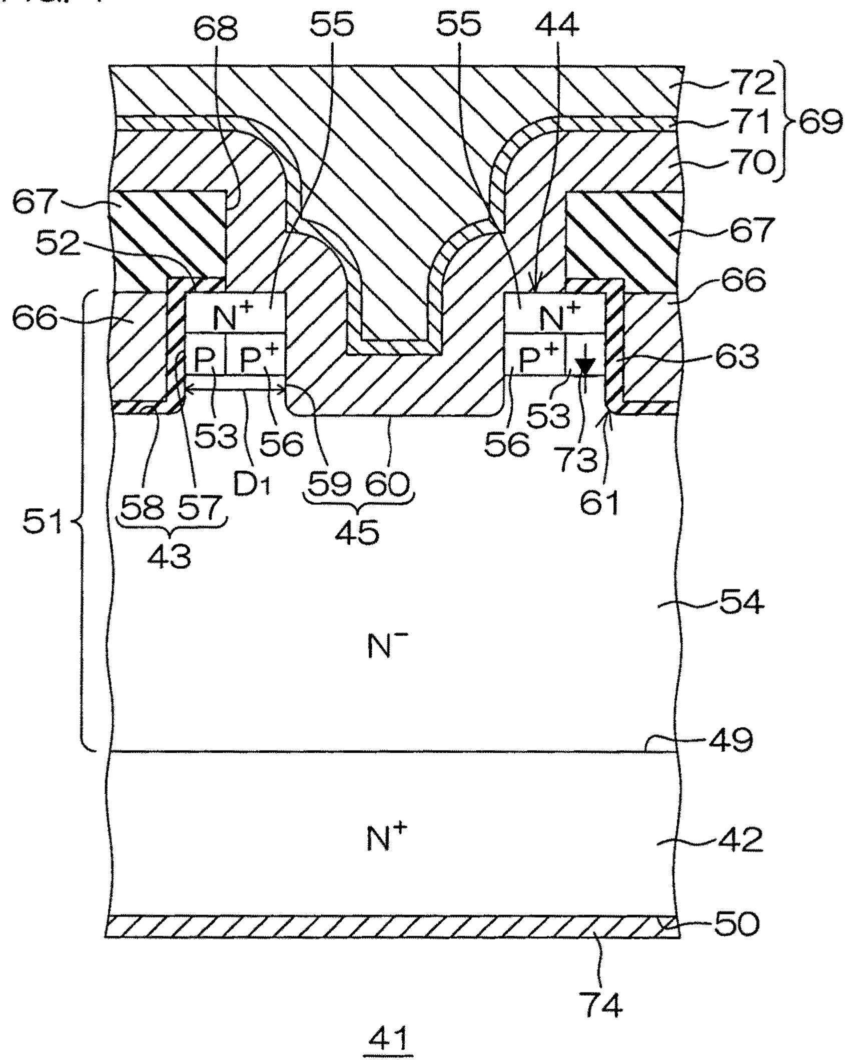


FIG. 4
68
55
55
44
72
71
69
70
67
67
52
66
66
N+
N+
P
P+
P+
63
53
56
53
56
73
D1
59 60
61
58 57
51
43
45
54
N−
49
N+
42
50
74
41

FIG. 5A

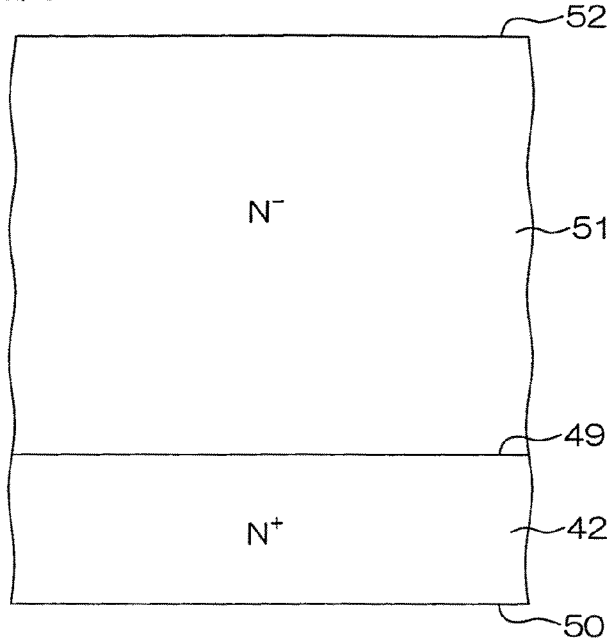
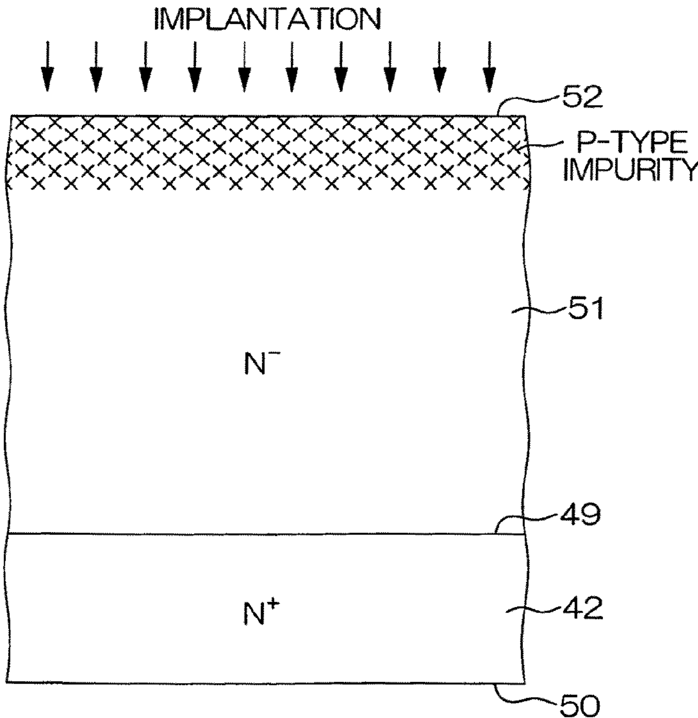


FIG. 5B



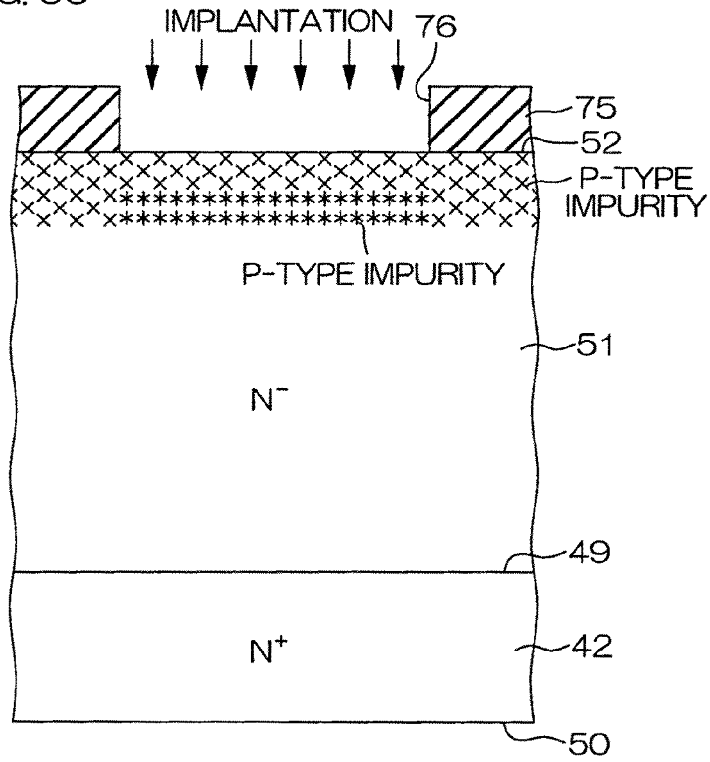


FIG. 5C
IMPLANTATION
76
75
52
P-TYPE IMPURITY
P-TYPE IMPURITY
51
N⁻
49
N⁺
42
50

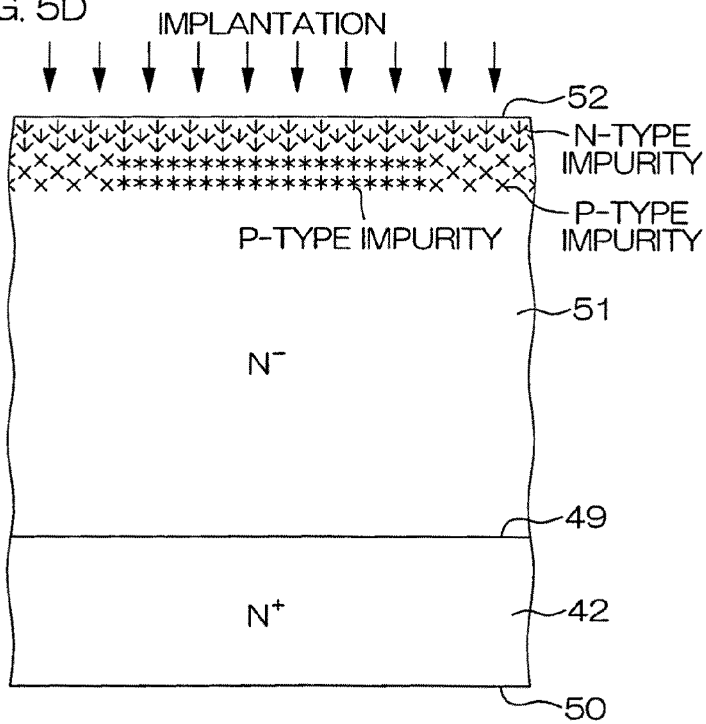


FIG. 5D
IMPLANTATION
52
N-TYPE IMPURITY
P-TYPE IMPURITY
P-TYPE IMPURITY
51
N⁻
49
N⁺
42
50

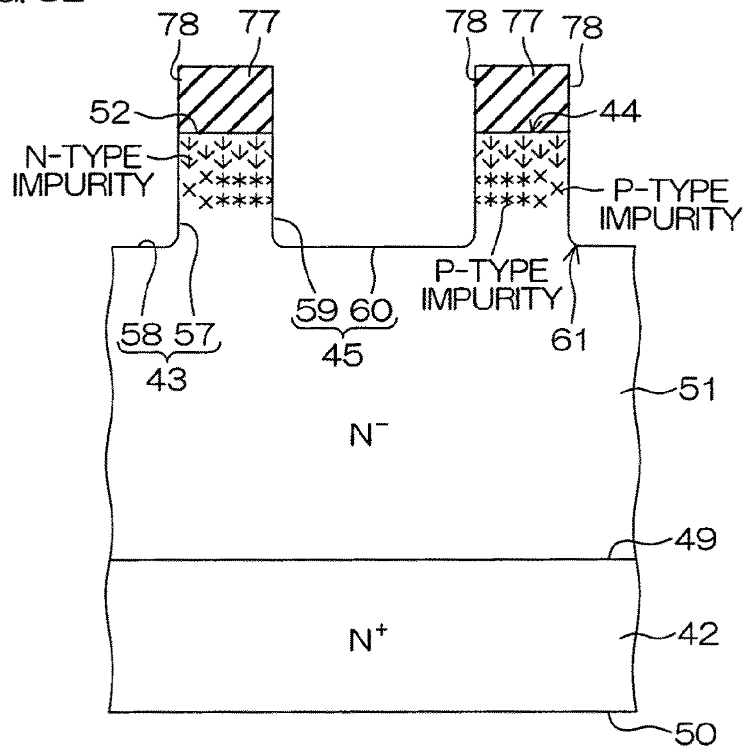


FIG. 5E
78
77
78
77
78
52
44
N-TYPE IMPURITY
P-TYPE IMPURITY
P-TYPE IMPURITY
58 57
43
59 60
45
61
51
N⁻
49
N⁺
42
50

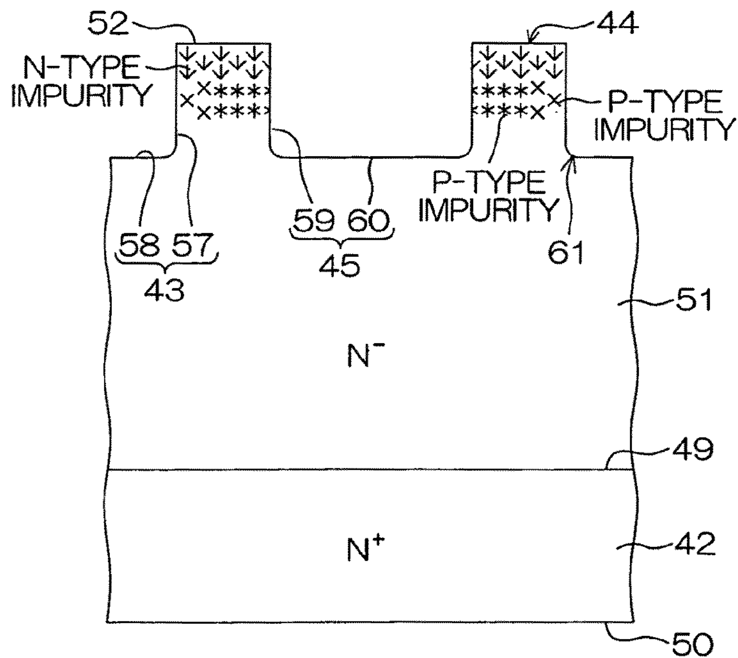


FIG. 5F
52
44
N-TYPE IMPURITY
P-TYPE IMPURITY
P-TYPE IMPURITY
58 57
43
59 60
45
61
51
N⁻
49
N⁺
42
50

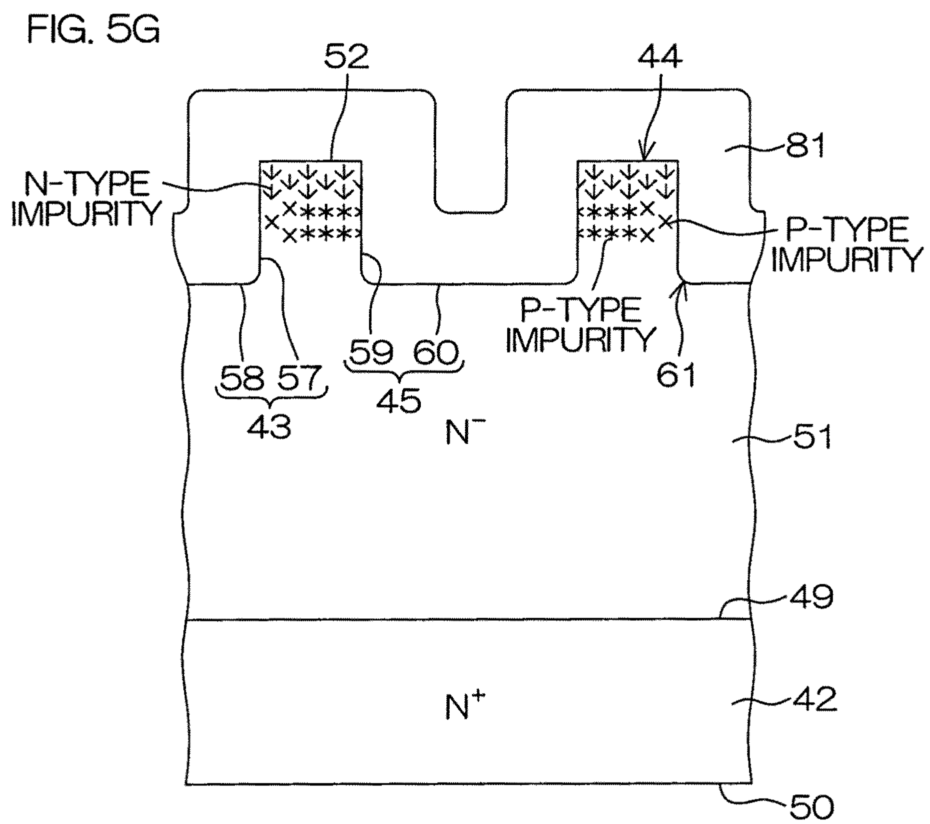


FIG. 5G
52
44
81
N-TYPE IMPURITY
P-TYPE IMPURITY
P-TYPE IMPURITY
59 60
45
58 57
43
61
N⁻
51
49
N⁺
42
50

FIG. 5H

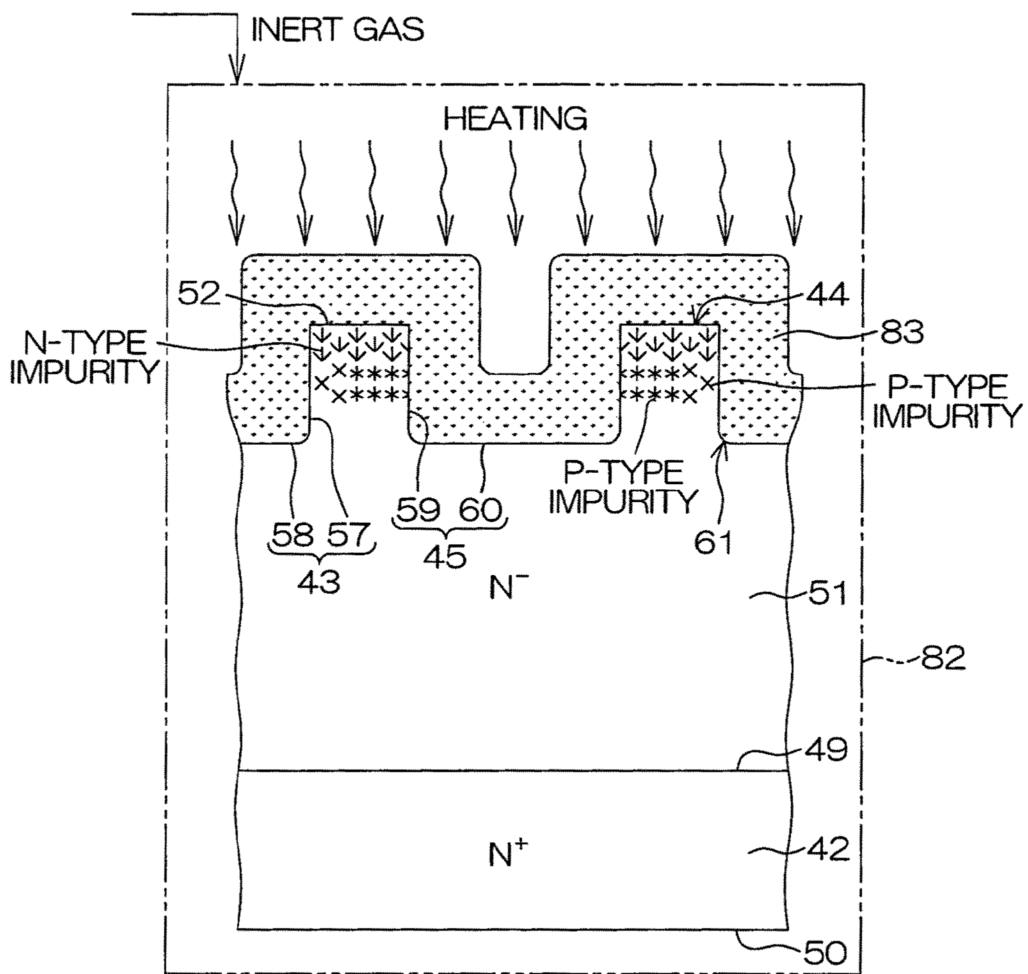


FIG. 5 I

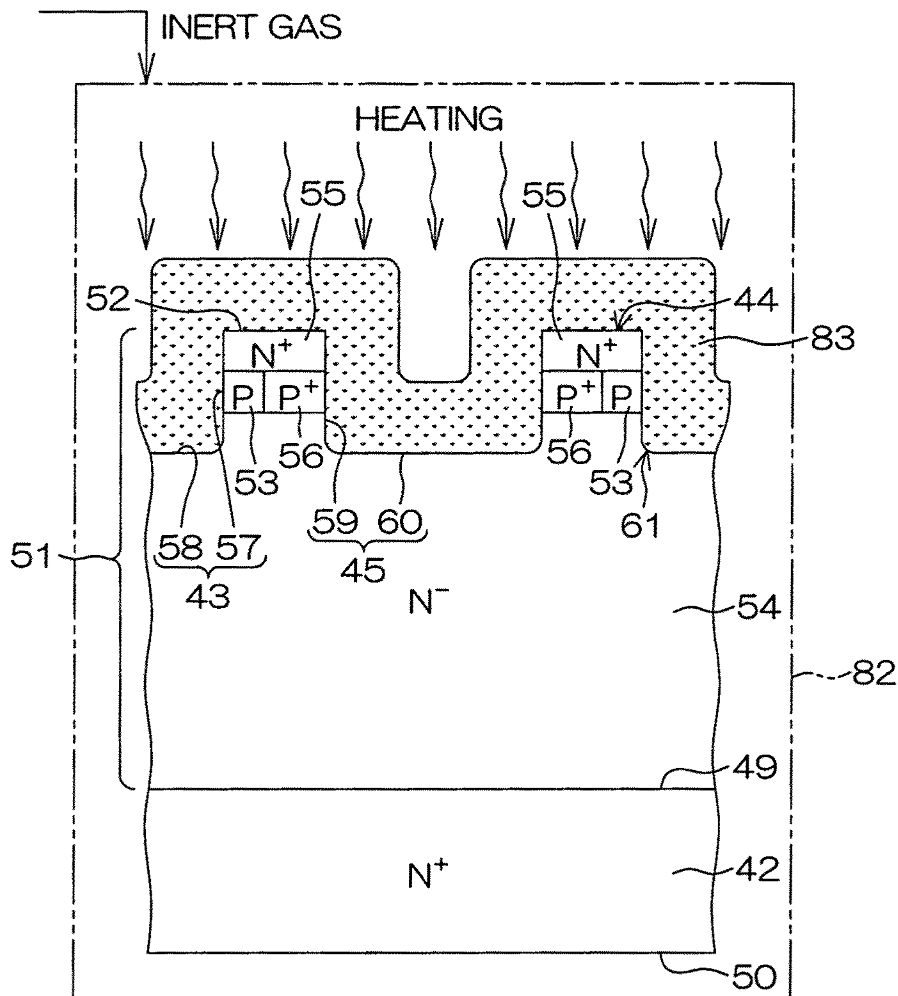


FIG. 5J

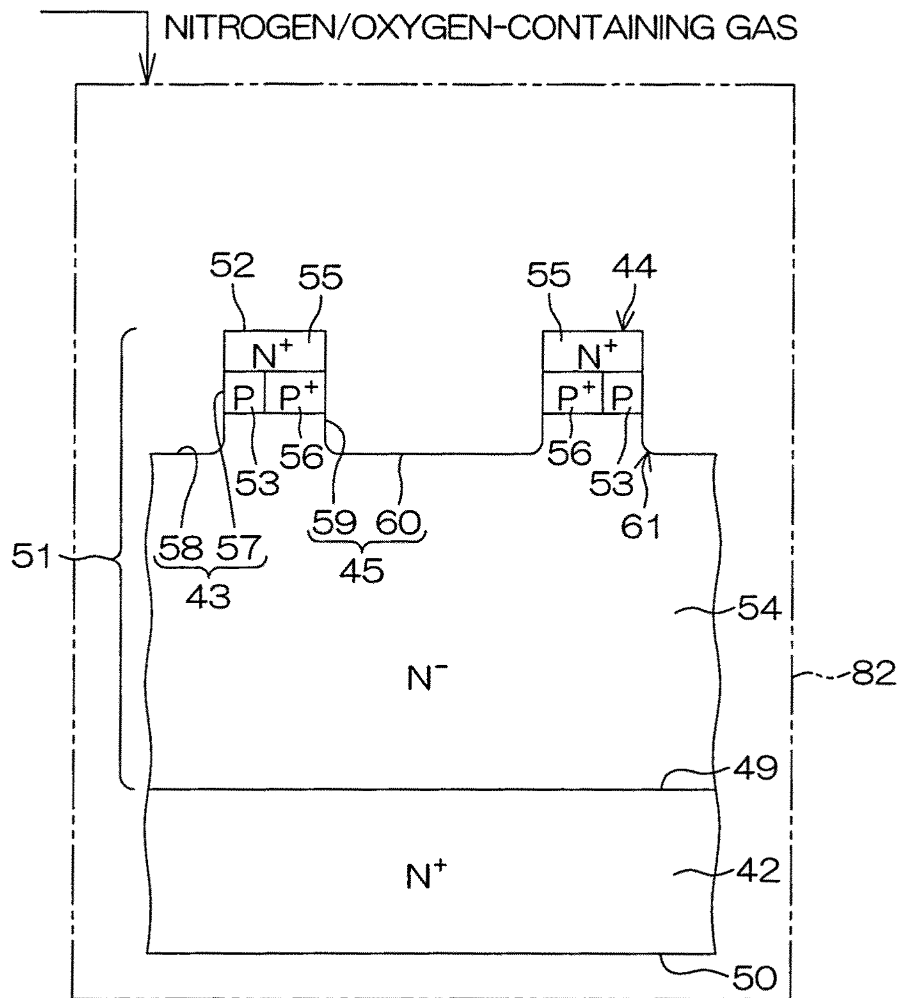


FIG. 5K

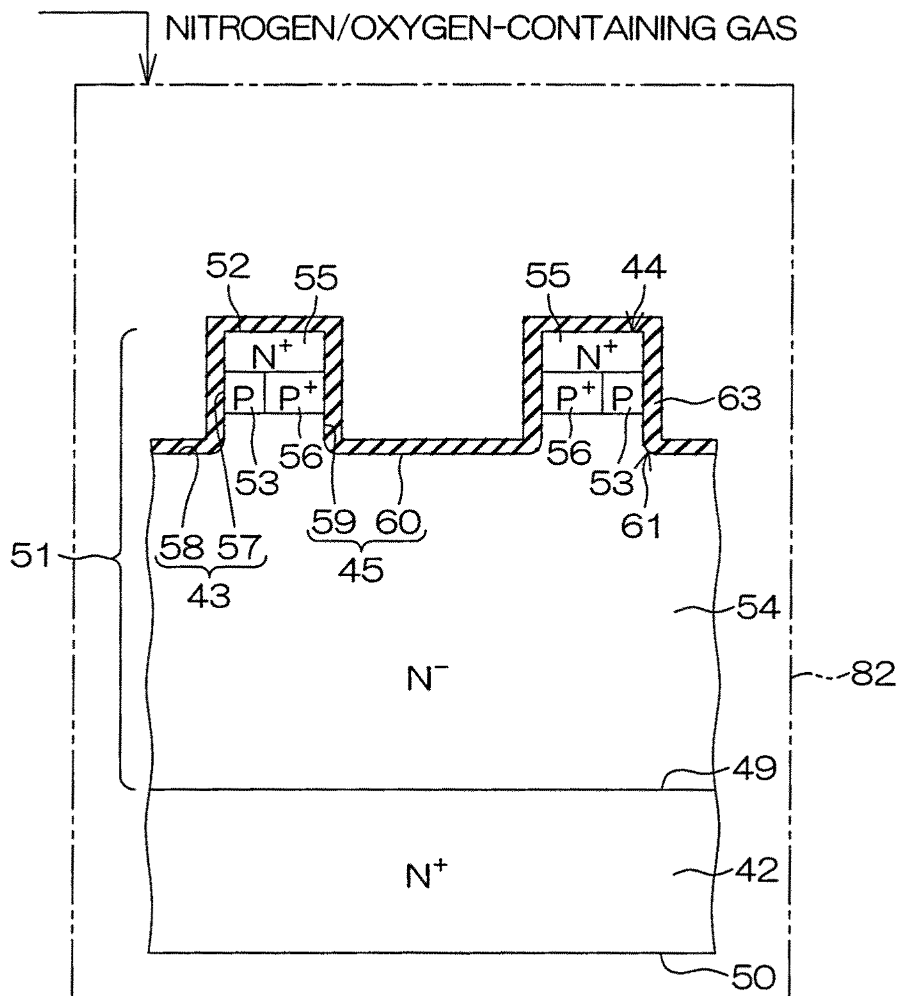


FIG. 5L

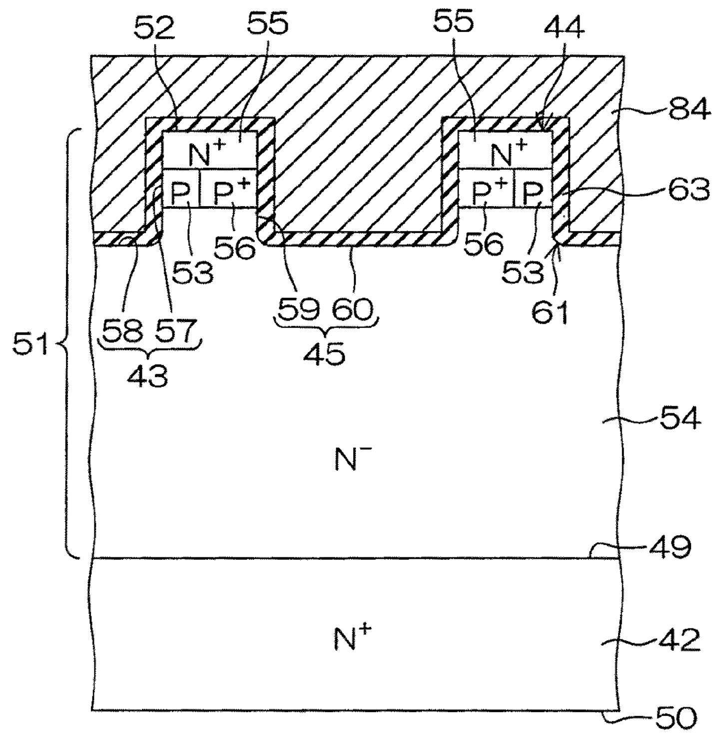


FIG. 5M

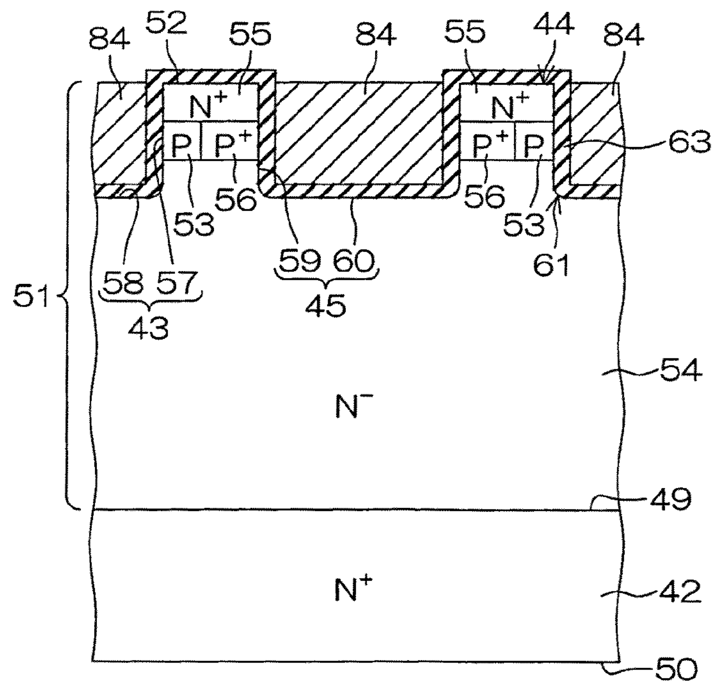
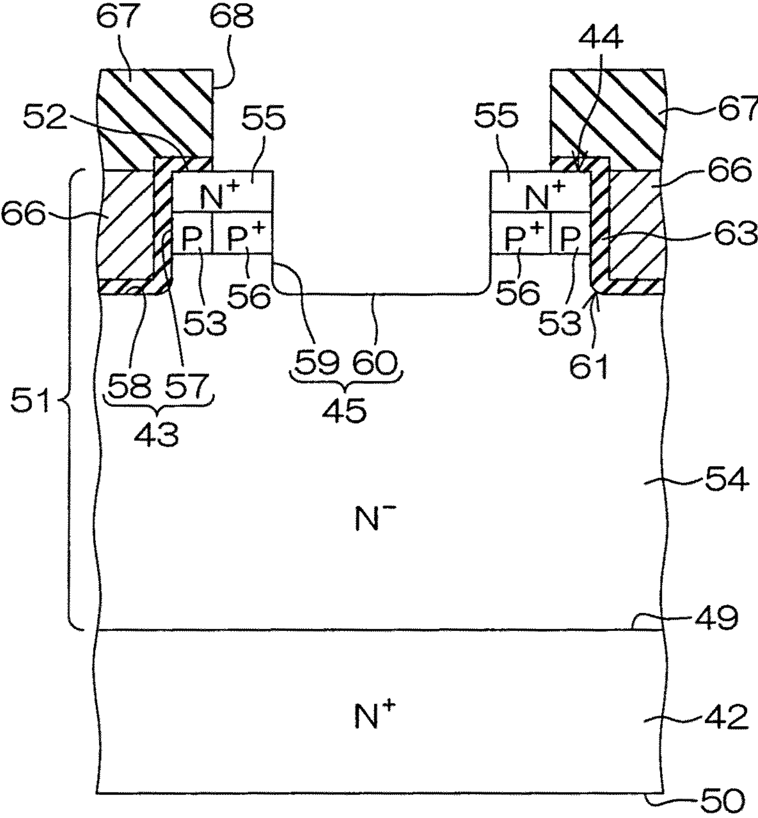


FIG. 5N

FIG. 5O

FIG. 5P



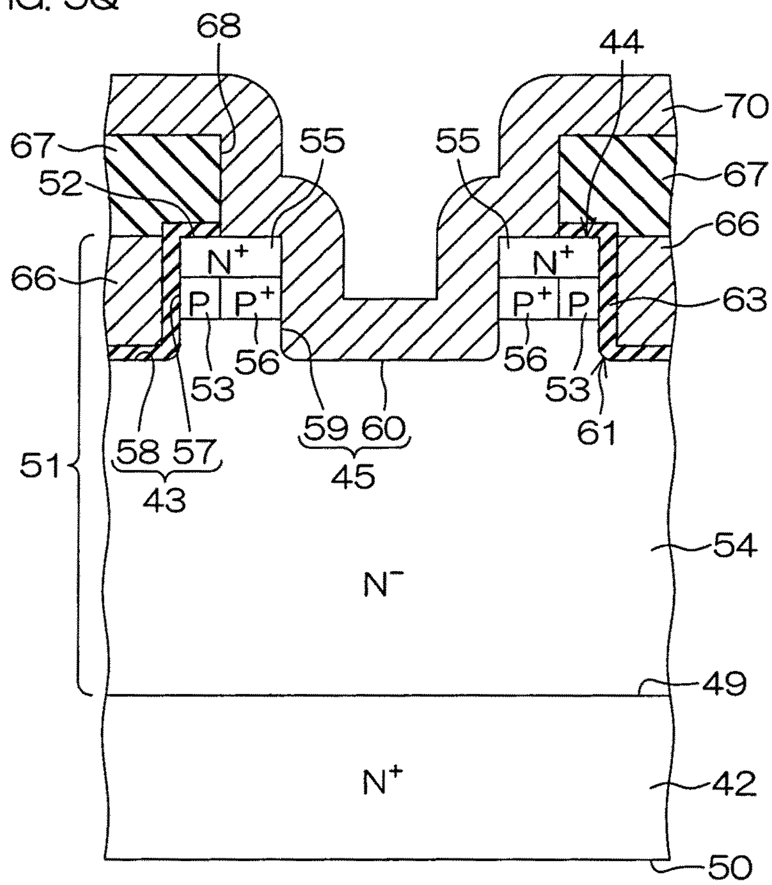


FIG. 5Q
68
44
70
67
55
55
67
52
66
N+
N+
66
P
P+
P+
P
63
56
56
53
53
59 60
61
58 57
45
51
43
54
N−
49
N+
42
50

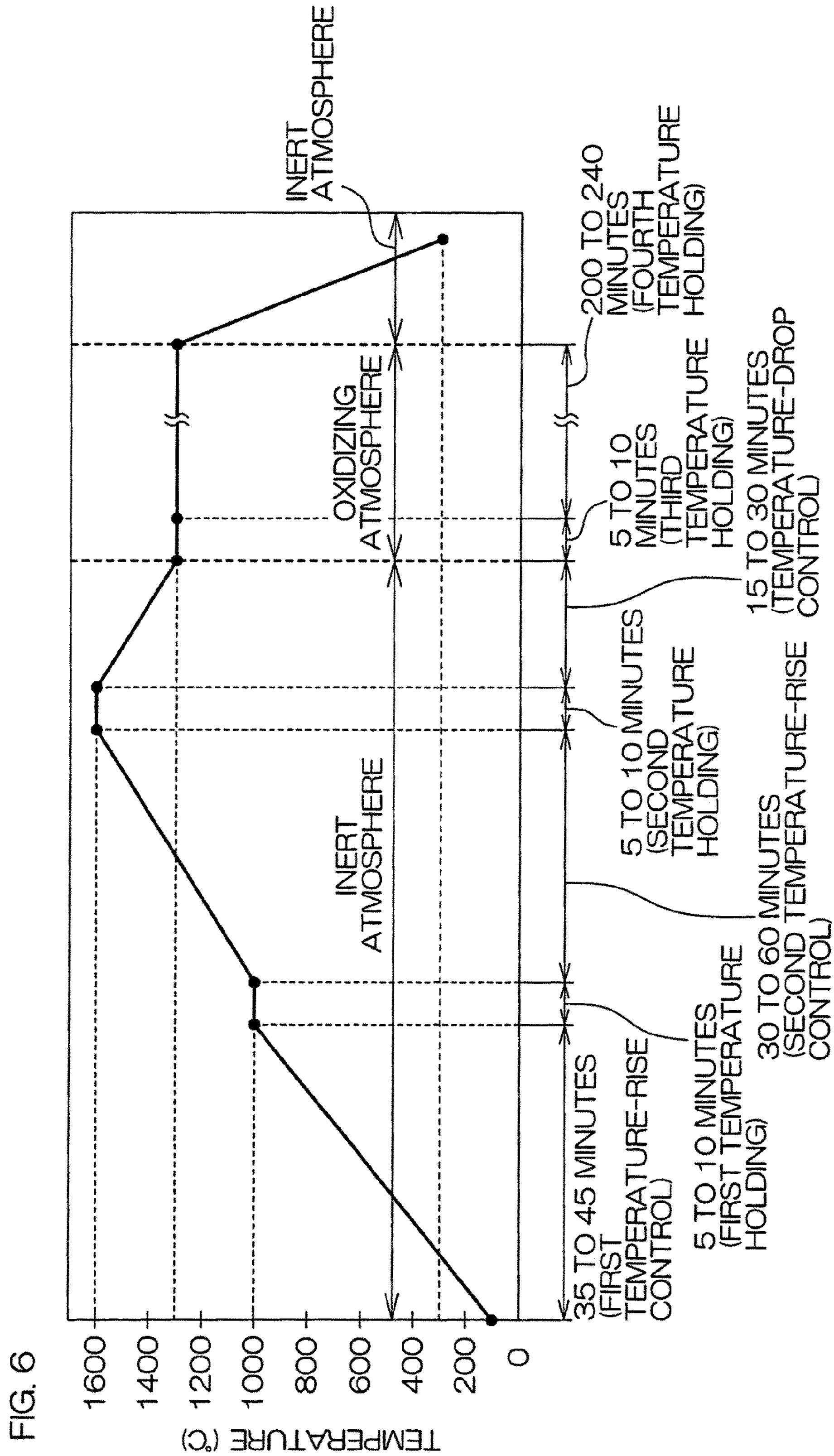
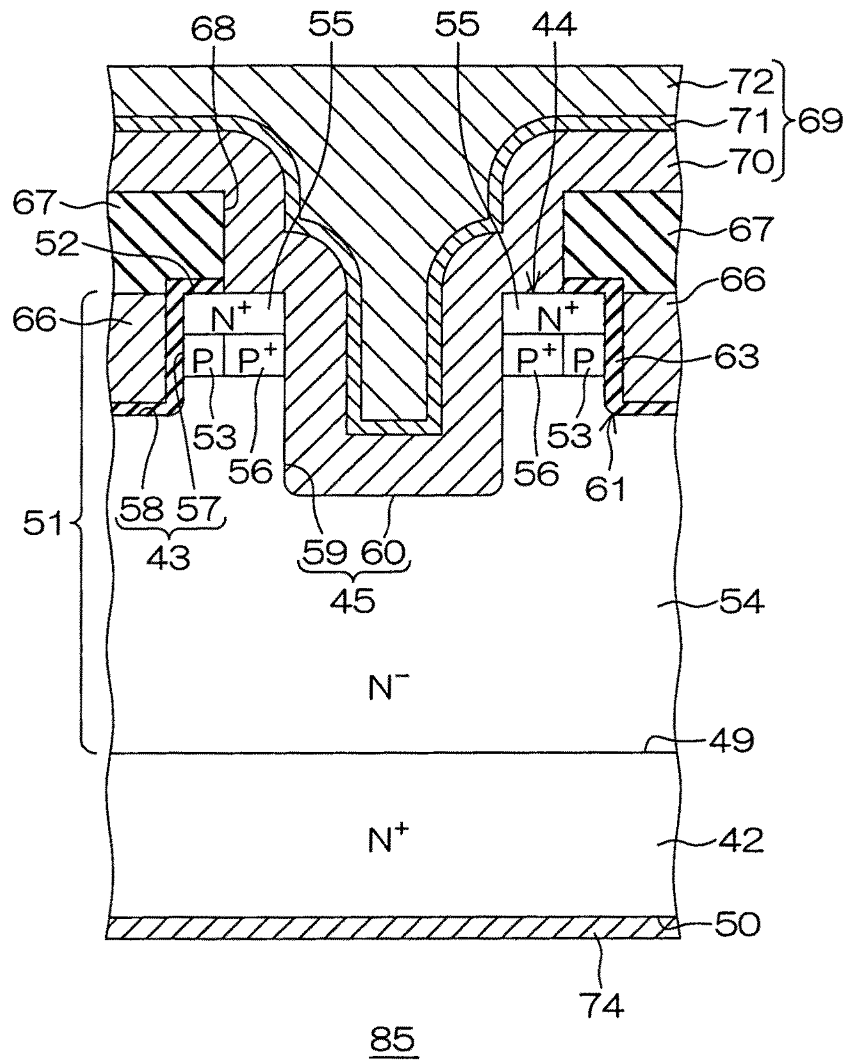


FIG. 6
TEMPERATURE (°C)
1600
1400
1200
1000
800
600
400
200
0
INERT ATMOSPHERE
OXIDIZING ATMOSPHERE
INERT ATMOSPHERE
35 TO 45 MINUTES (FIRST TEMPERATURE-RISE CONTROL)
5 TO 10 MINUTES (FIRST TEMPERATURE HOLDING)
30 TO 60 MINUTES (SECOND TEMPERATURE-RISE CONTROL)
5 TO 10 MINUTES (SECOND TEMPERATURE HOLDING)
15 TO 30 MINUTES (TEMPERATURE-DROP CONTROL)
5 TO 10 MINUTES (THIRD TEMPERATURE HOLDING)
200 TO 240 MINUTES (FOURTH TEMPERATURE HOLDING)

FIG. 7



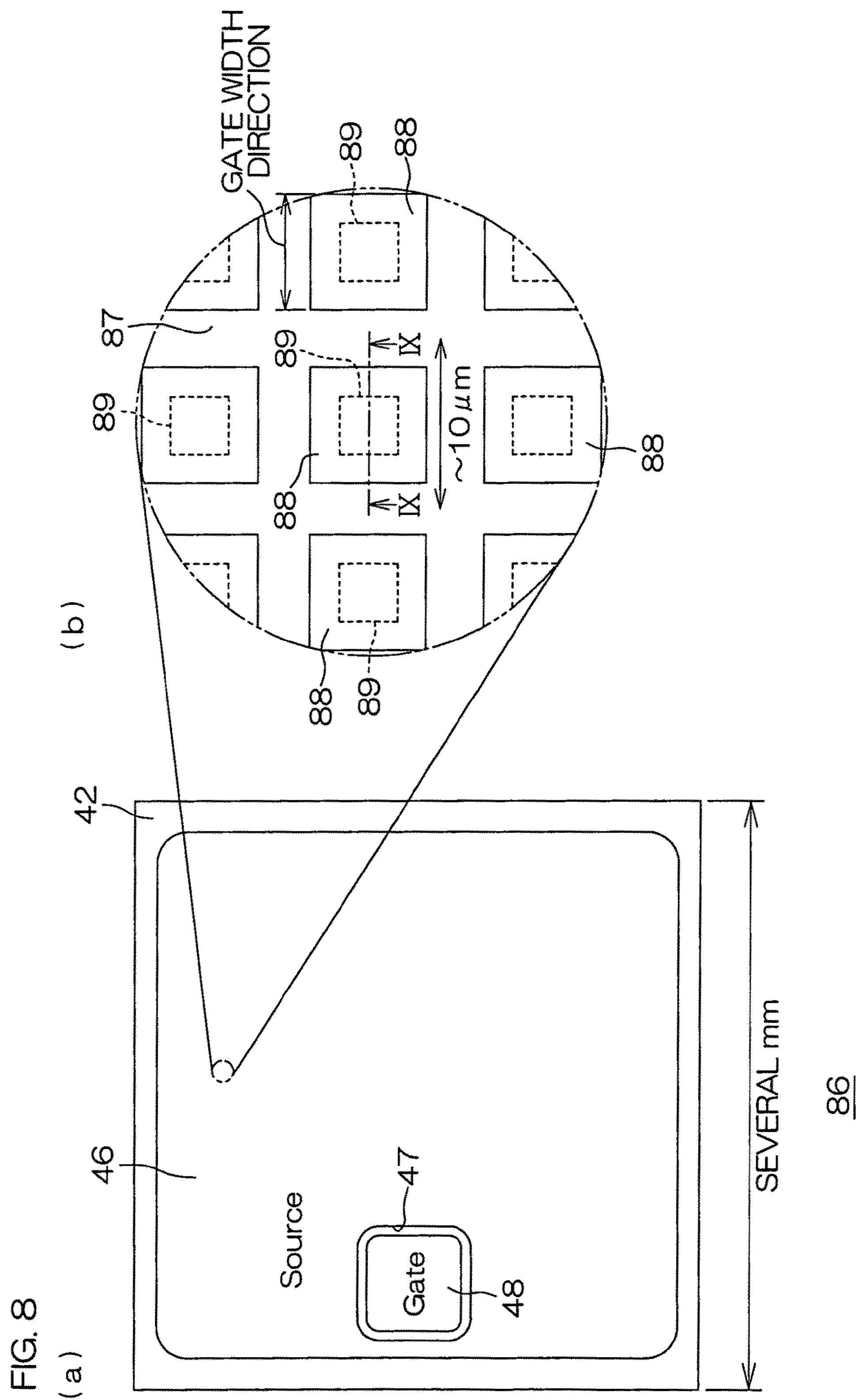


FIG. 8
(a)
(b)
GATE WIDTH
DIRECTION
87
88
89
~10 μm
IX
IX
42
46
Source
Gate
47
48
SEVERAL mm
86

FIG. 9

88 96 99 98 89 97 95 95 87 87 52 94 94 N+ P+ N+ P 92 93 92 90 51 91 N− 49 N+ 42 50 74

86

FIG. 10A

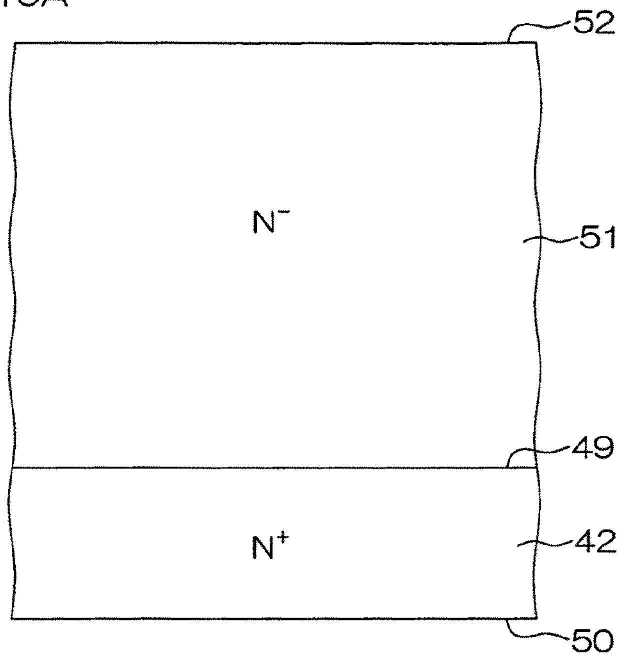


FIG. 10B

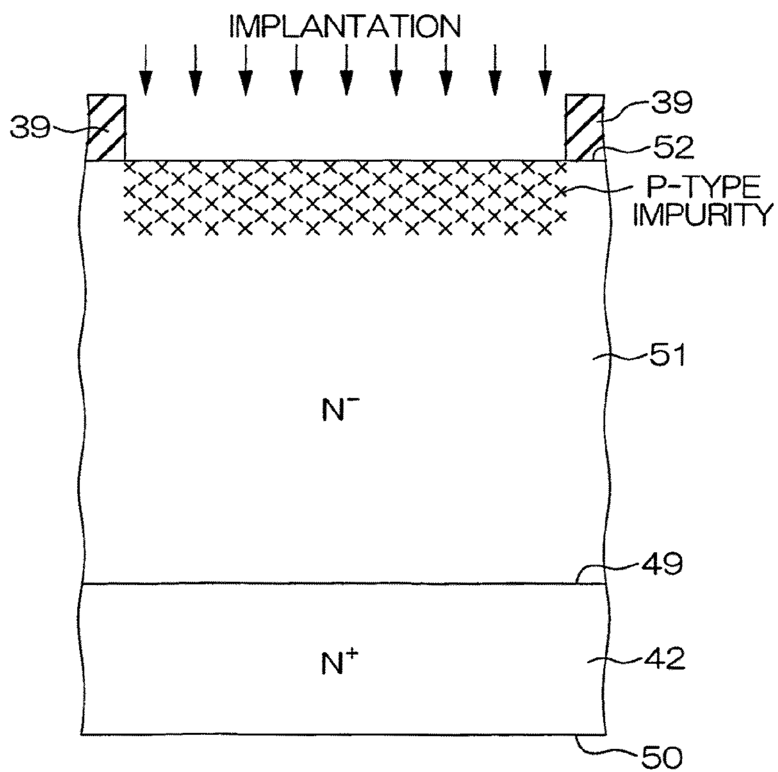


FIG. 10C

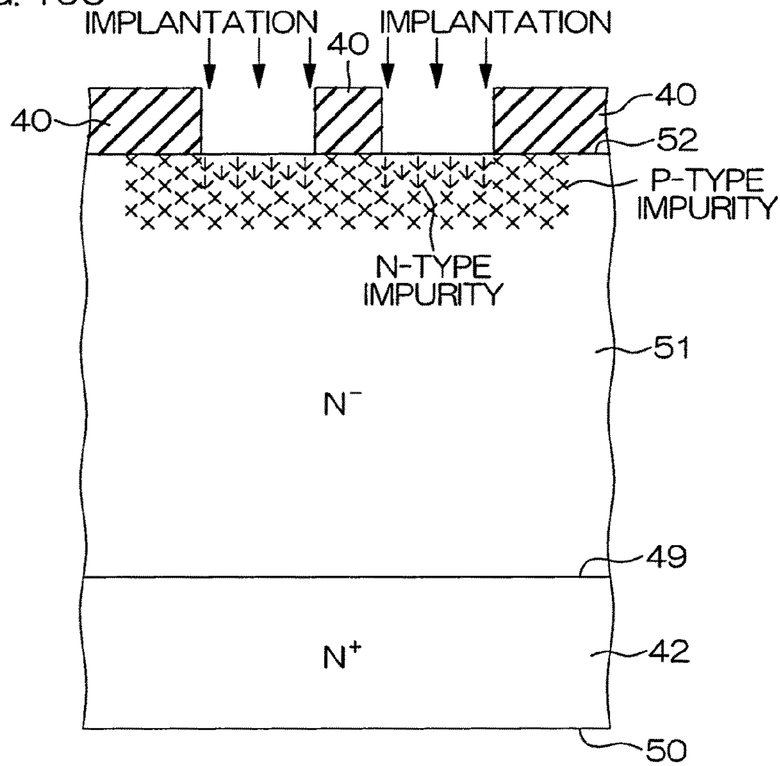
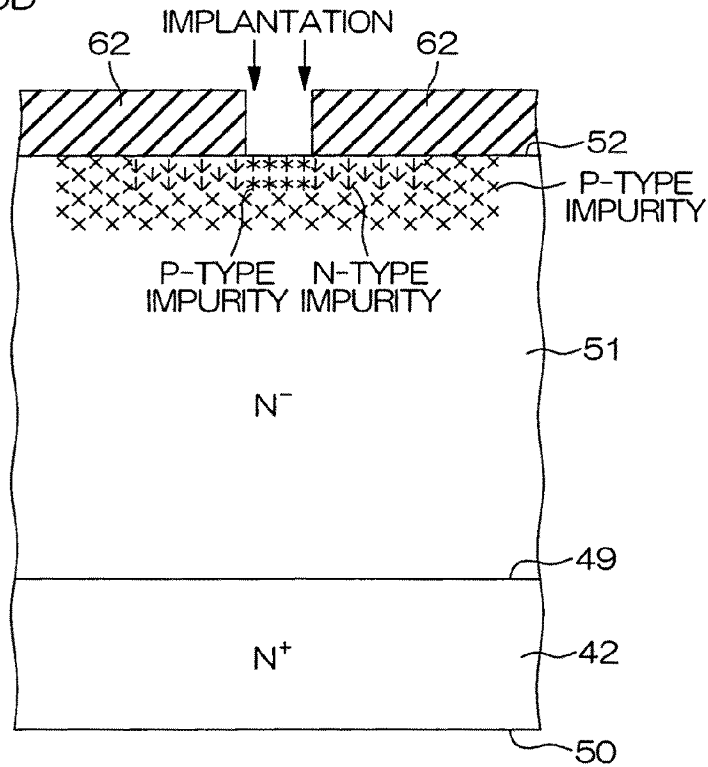


FIG. 10D



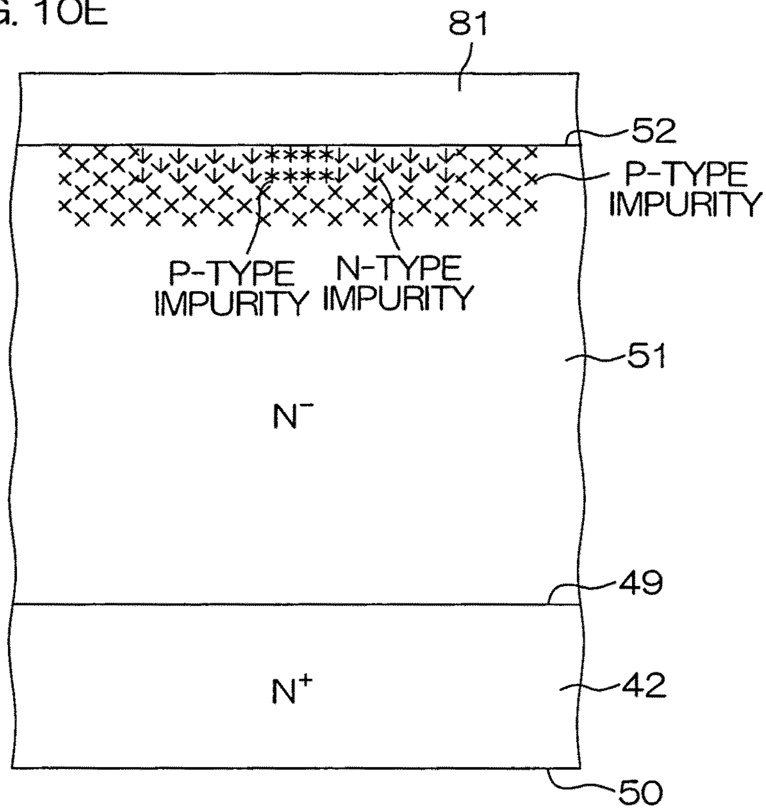


FIG. 10E
81
52
P-TYPE IMPURITY
P-TYPE IMPURITY
N-TYPE IMPURITY
51
N⁻
49
N⁺
42
50

FIG. 10F

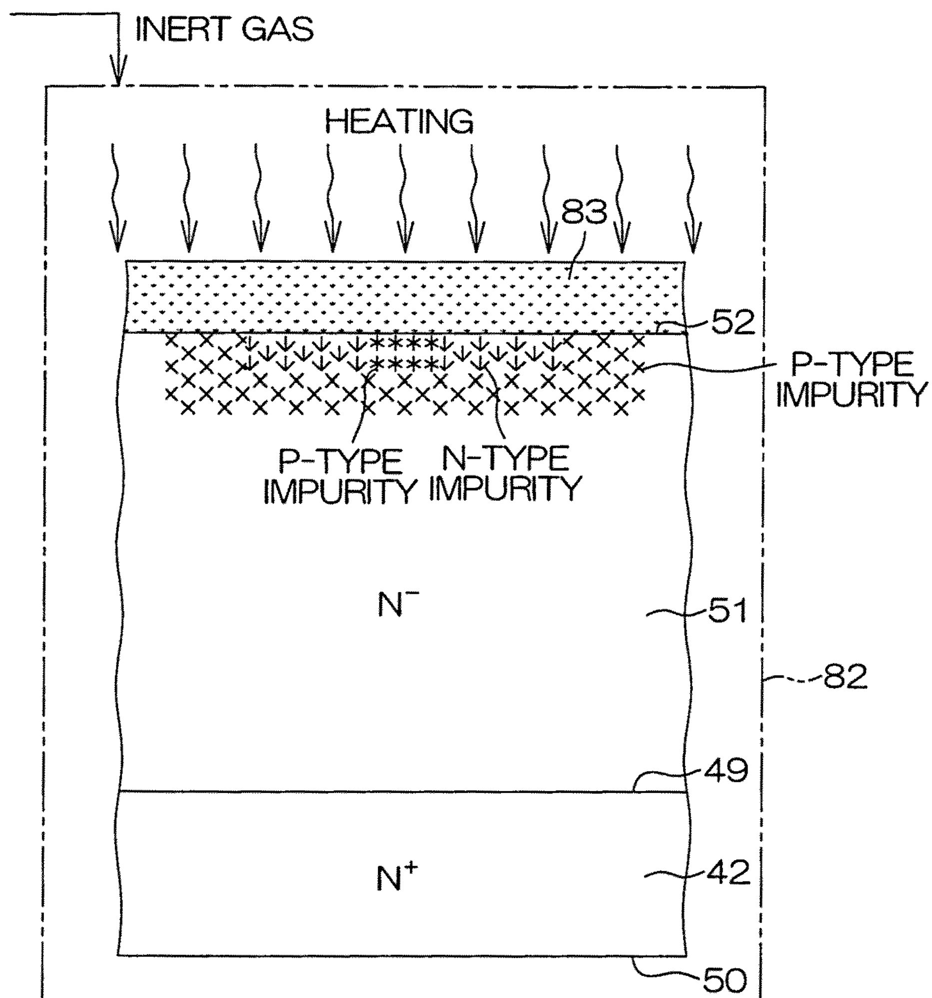


FIG. 10G

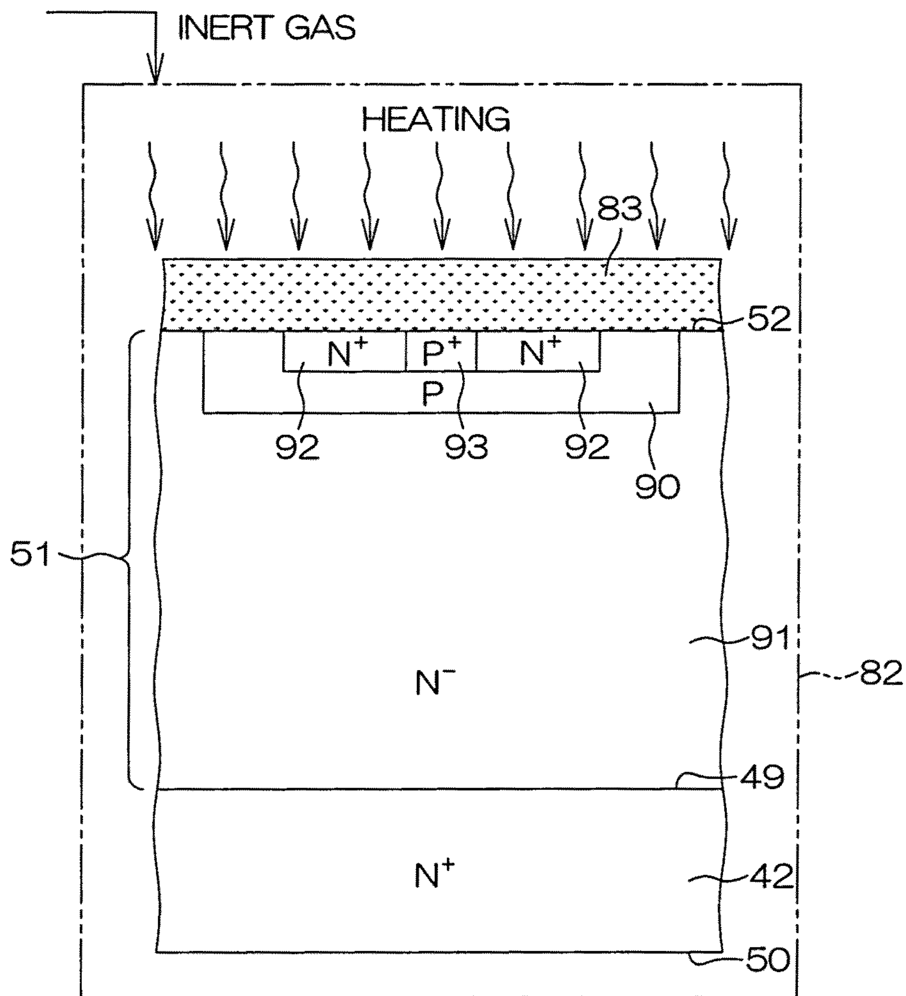
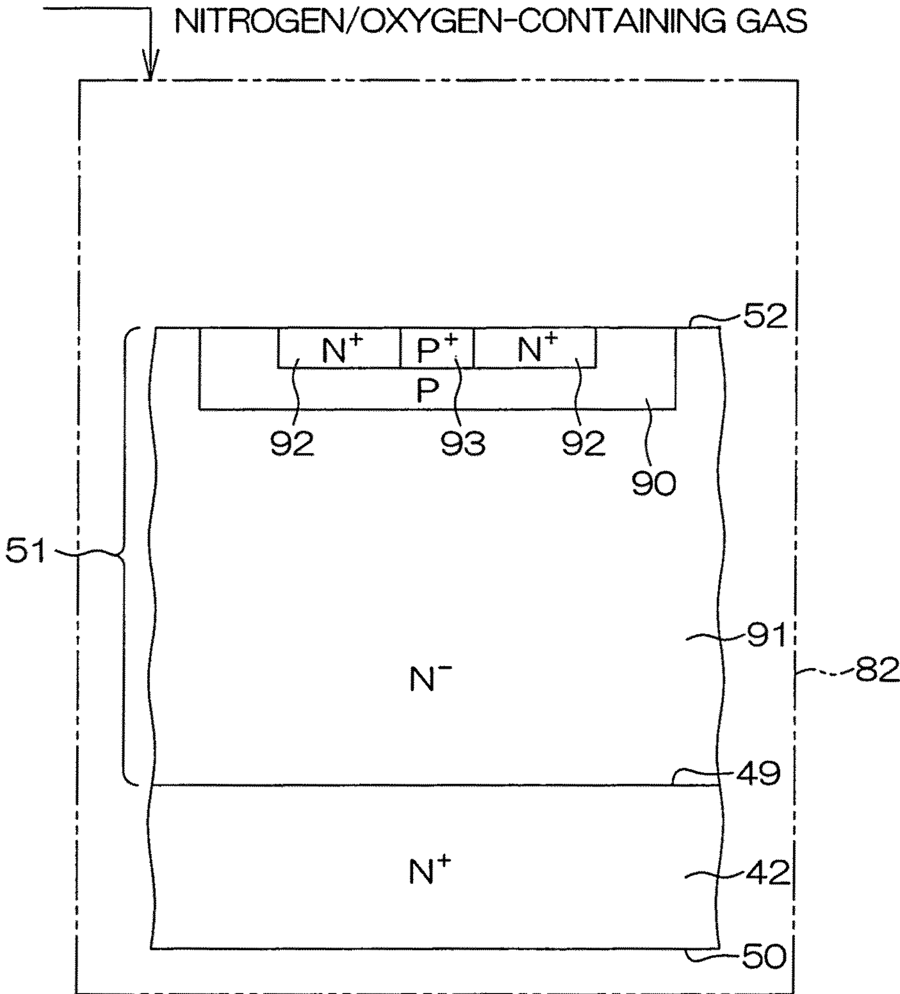


FIG. 10H



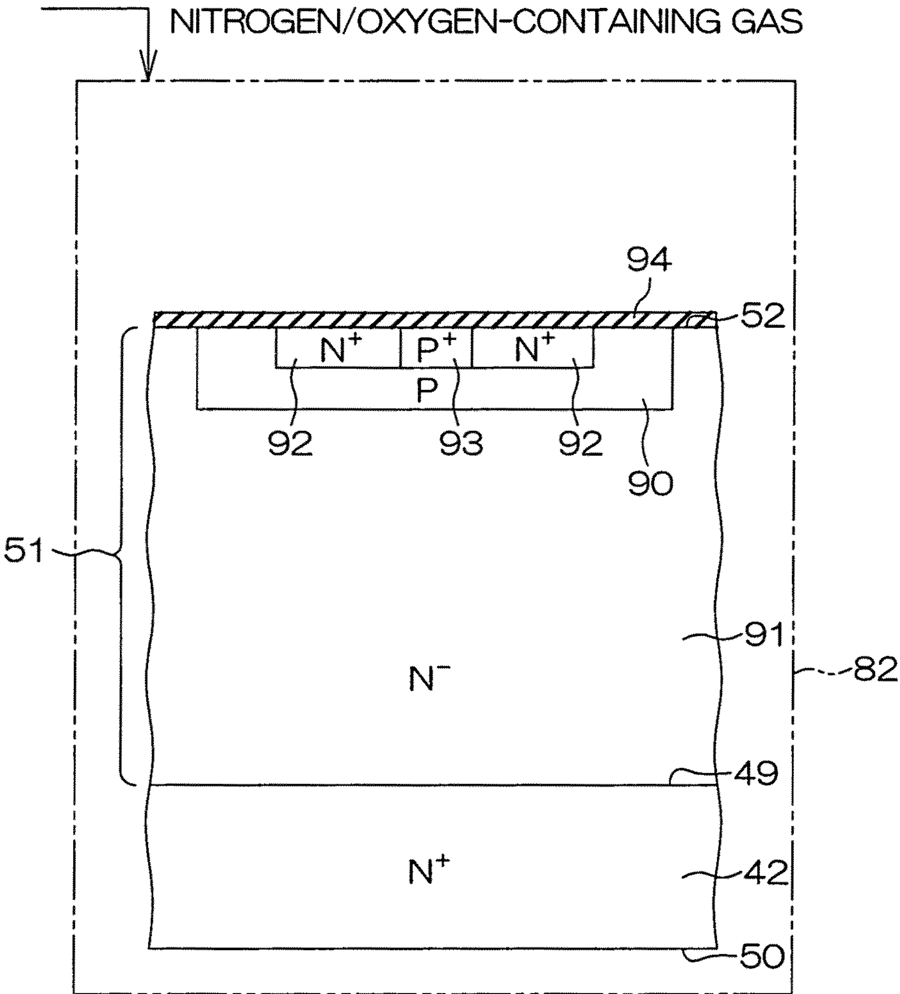


FIG. 10I
NITROGEN/OXYGEN-CONTAINING GAS
94
52
N+
P+
N+
P
92
93
92
90
51
91
N−
82
49
N+
42
50

FIG. 10J

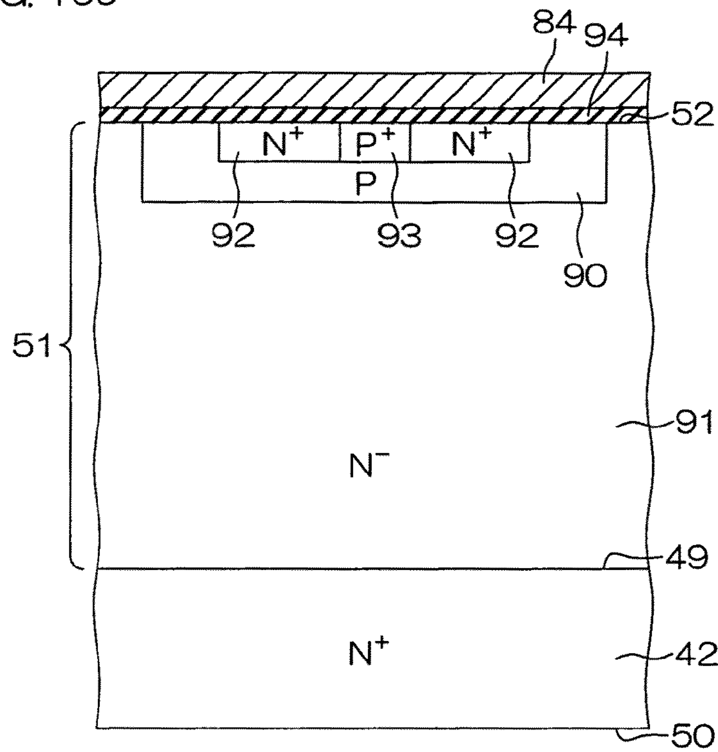


FIG. 10K

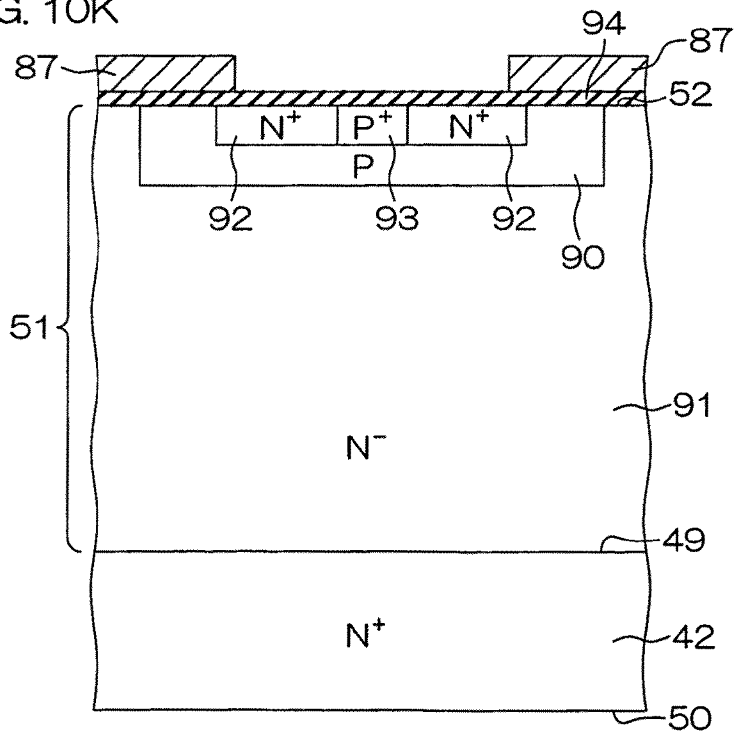


FIG. 10L

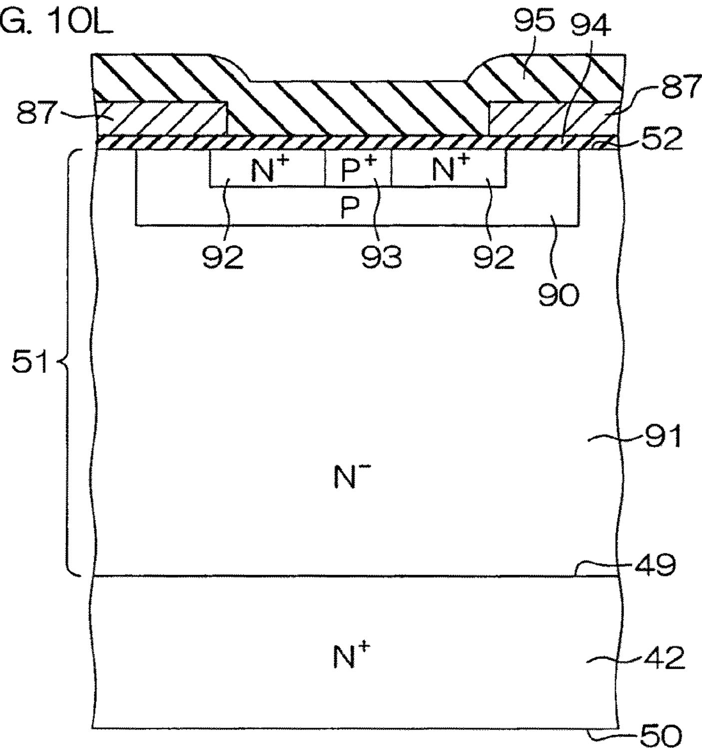


FIG. 10M

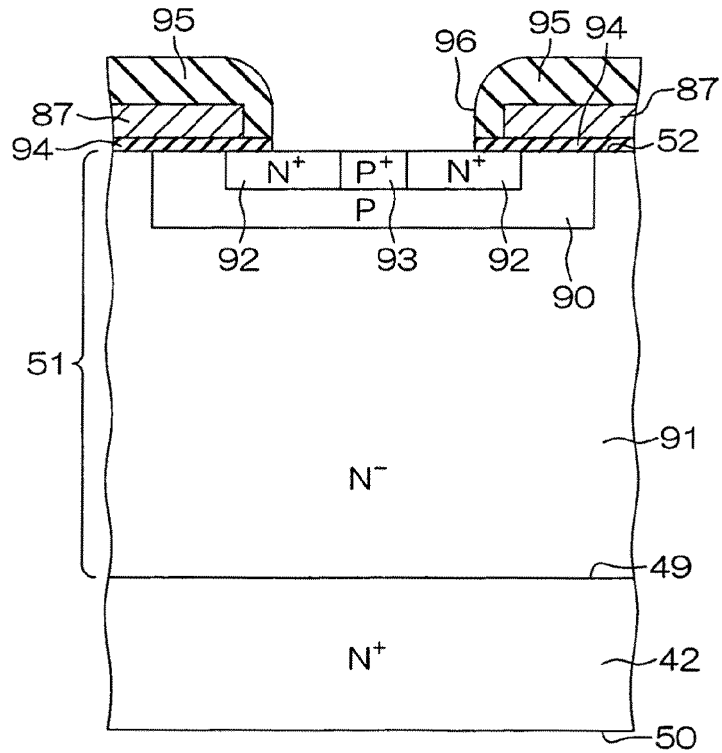


FIG. 10N

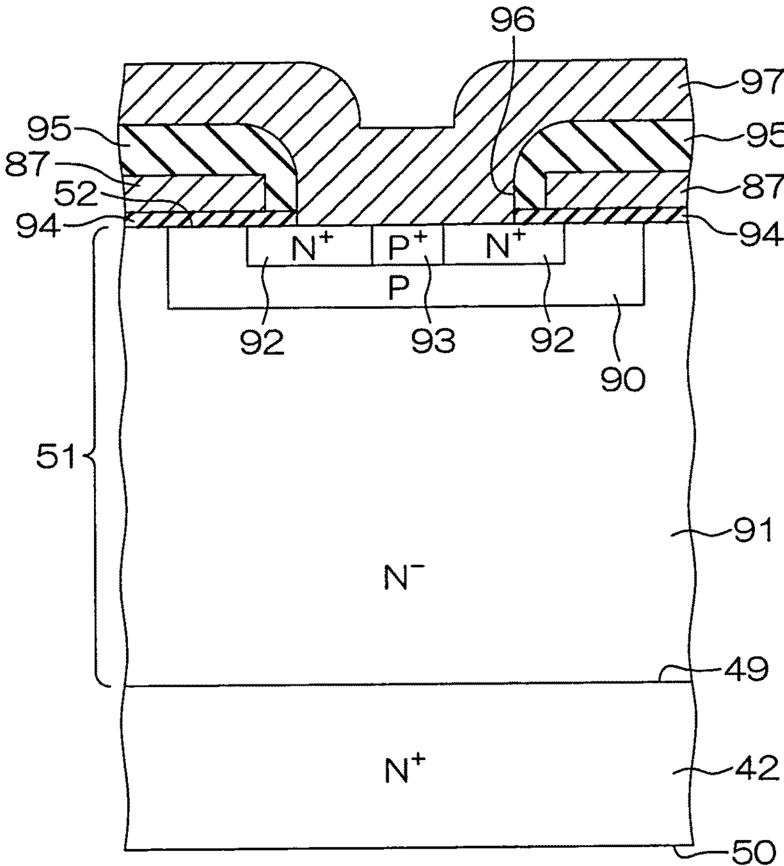
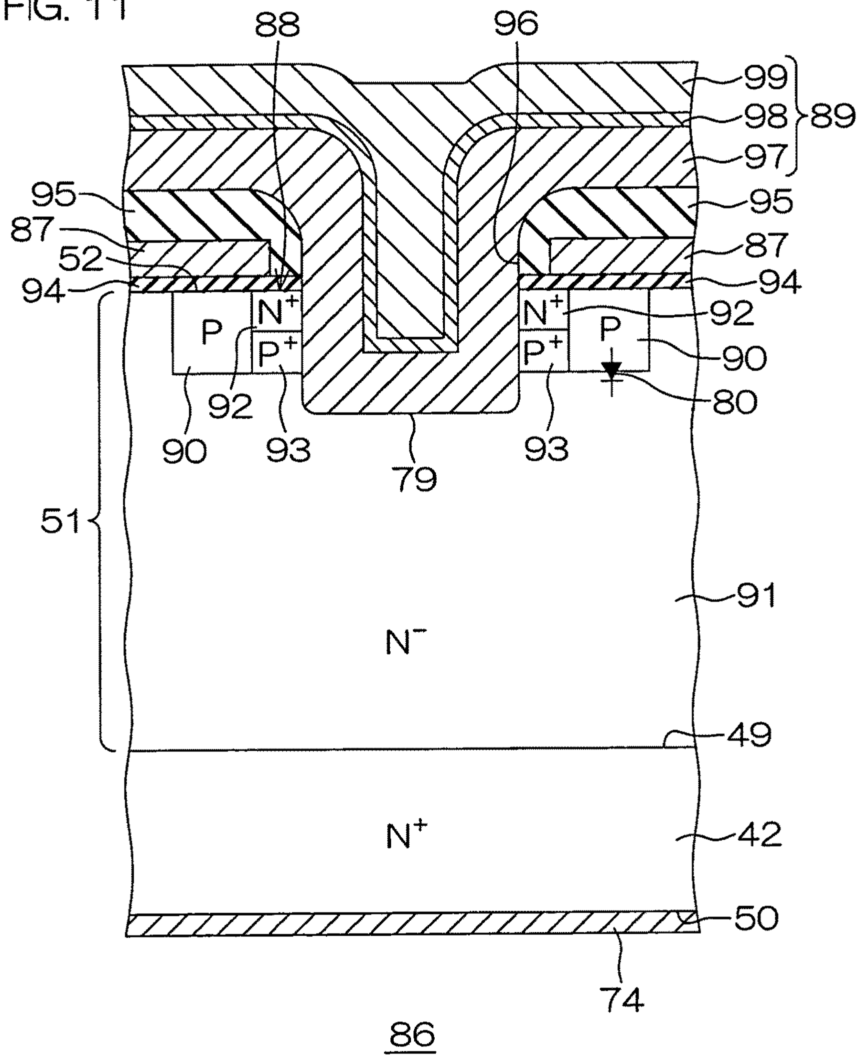


FIG. 11



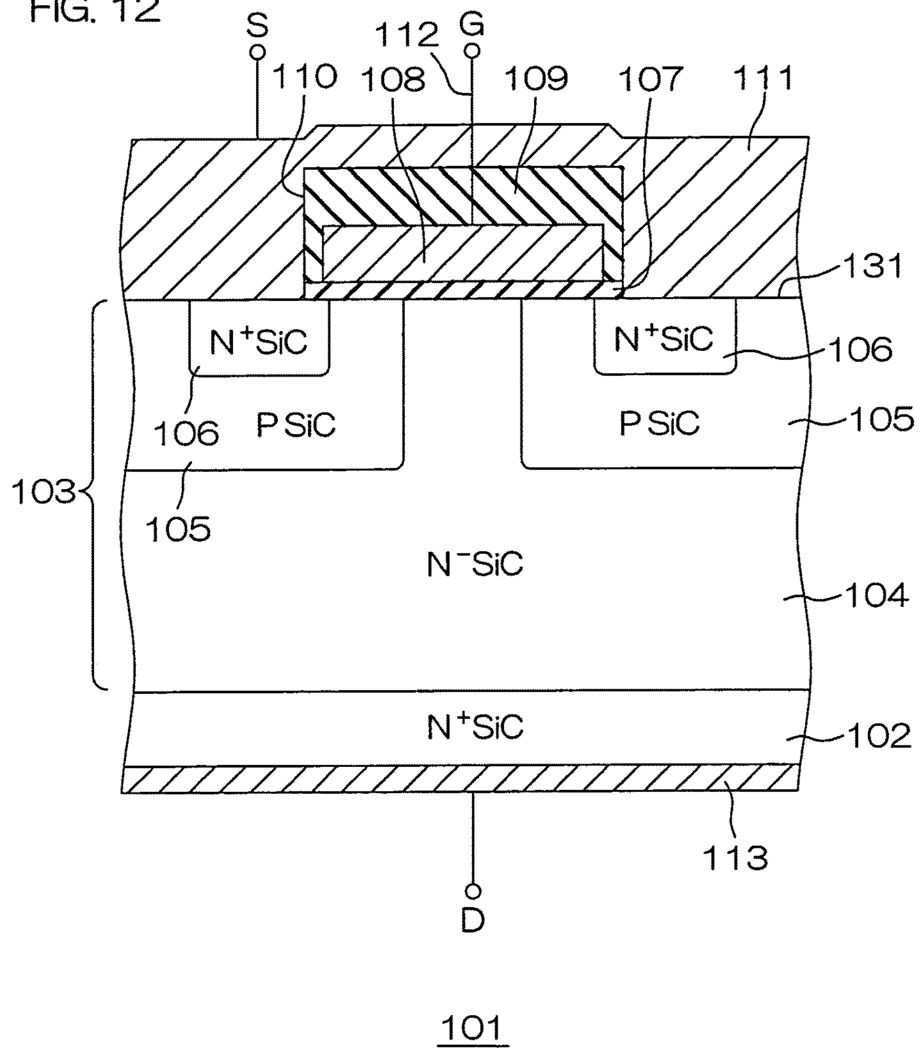


FIG. 12
S
G
112
110
108
109
107
111
131
N+SiC
N+SiC
106
106
P SiC
P SiC
105
105
103
N−SiC
104
N+SiC
102
113
D
101

FIG. 13A

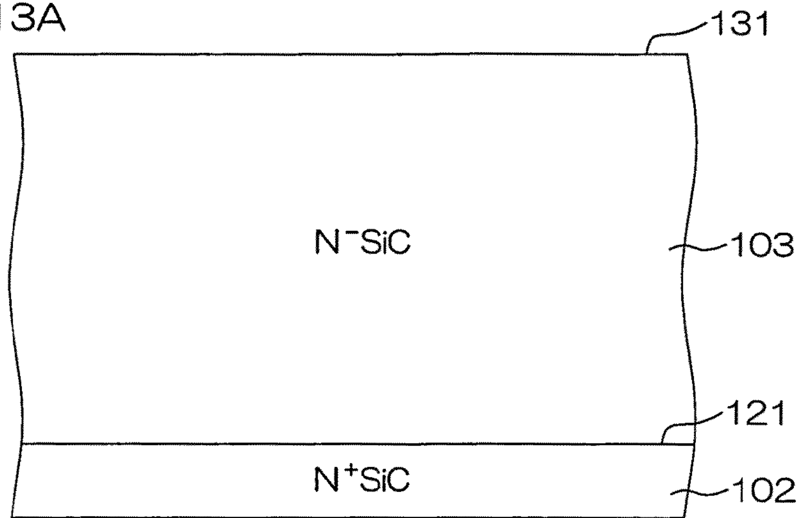


FIG. 13B

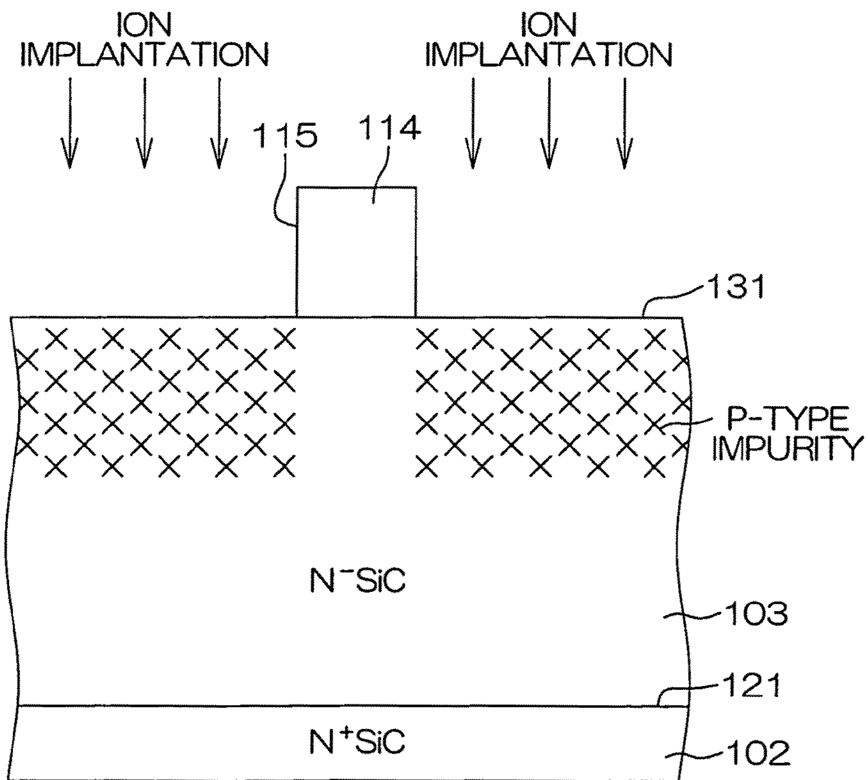


FIG. 13C

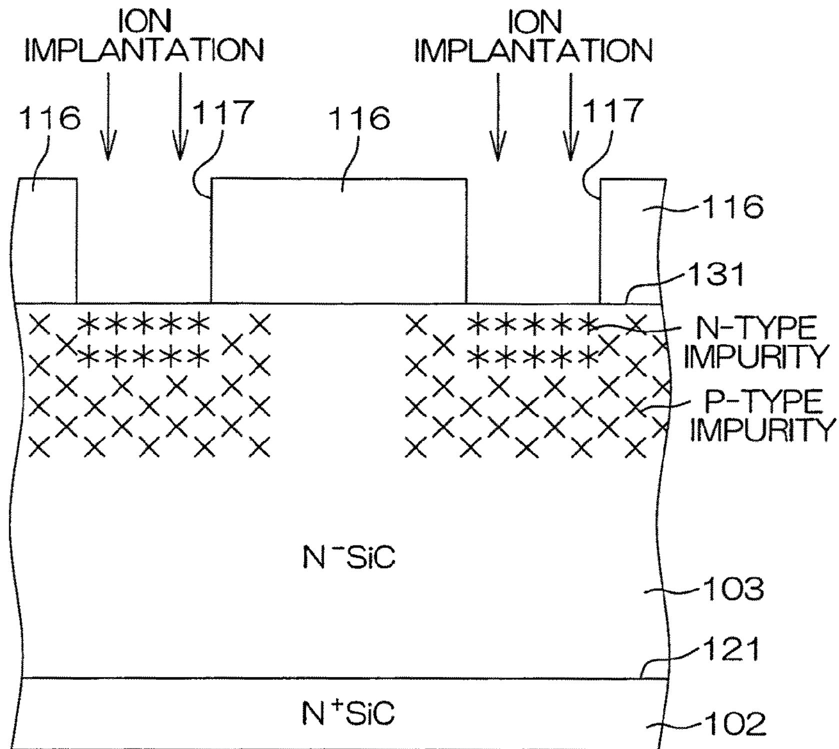


FIG. 13D

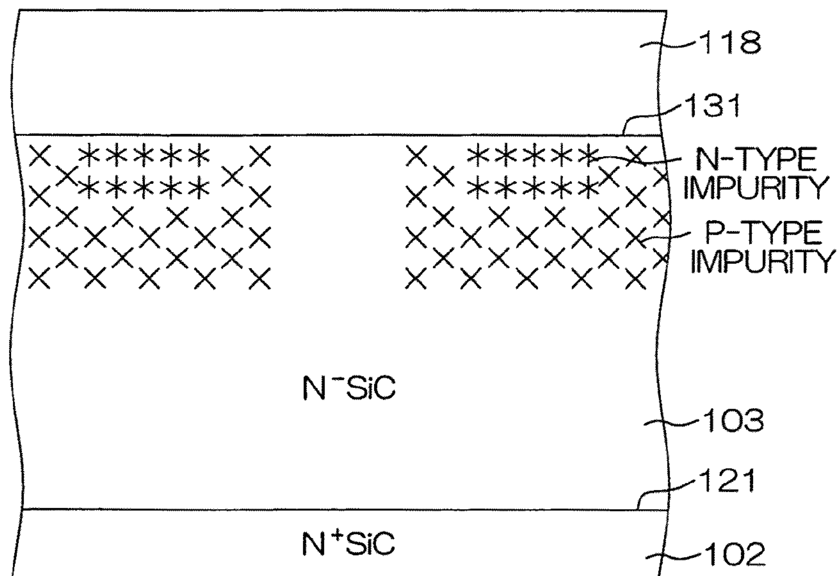


FIG. 13E

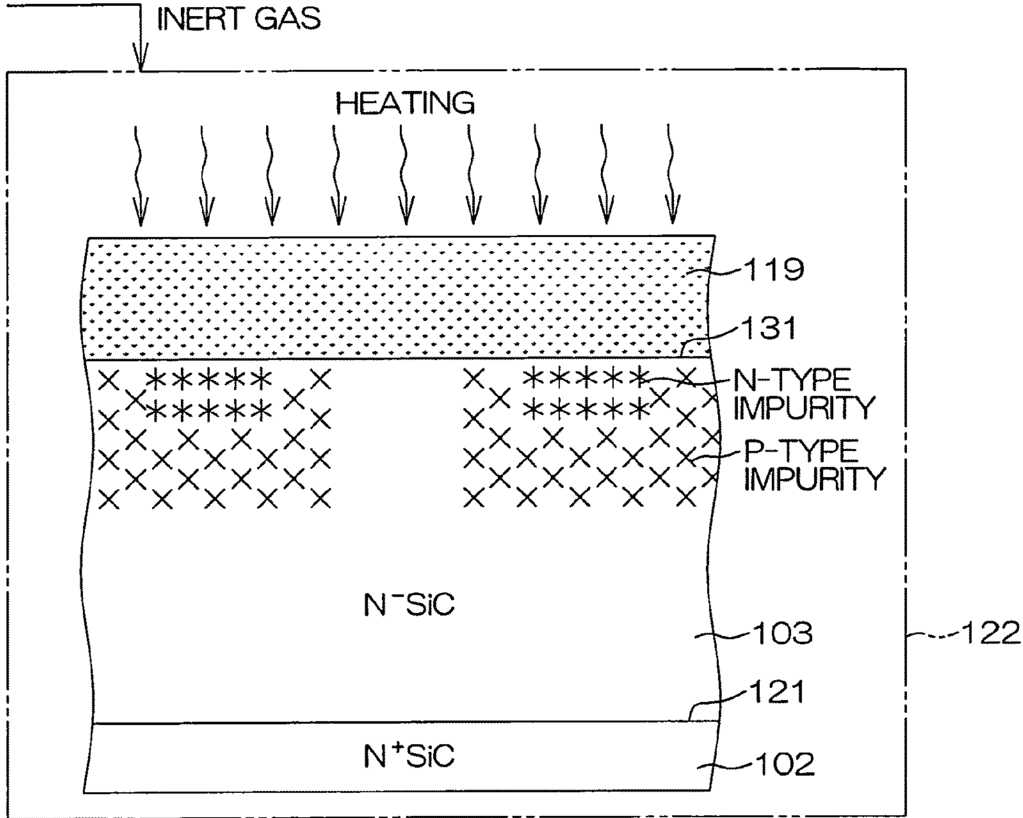


FIG. 13F

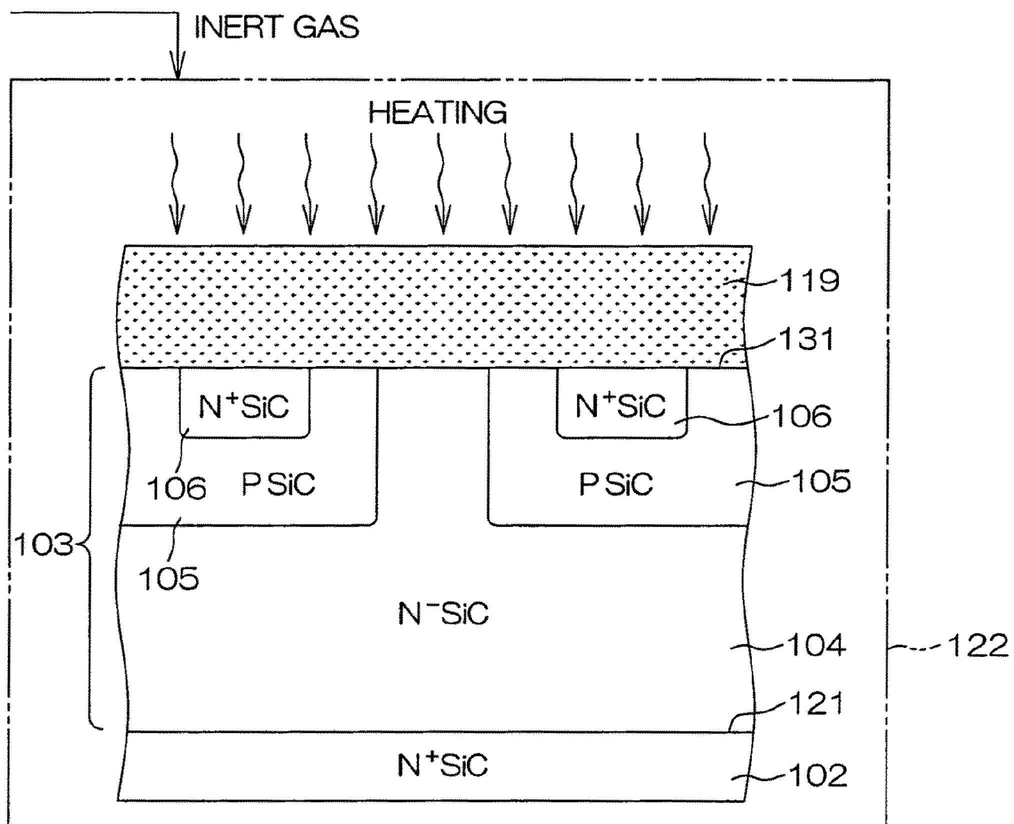


FIG. 13G

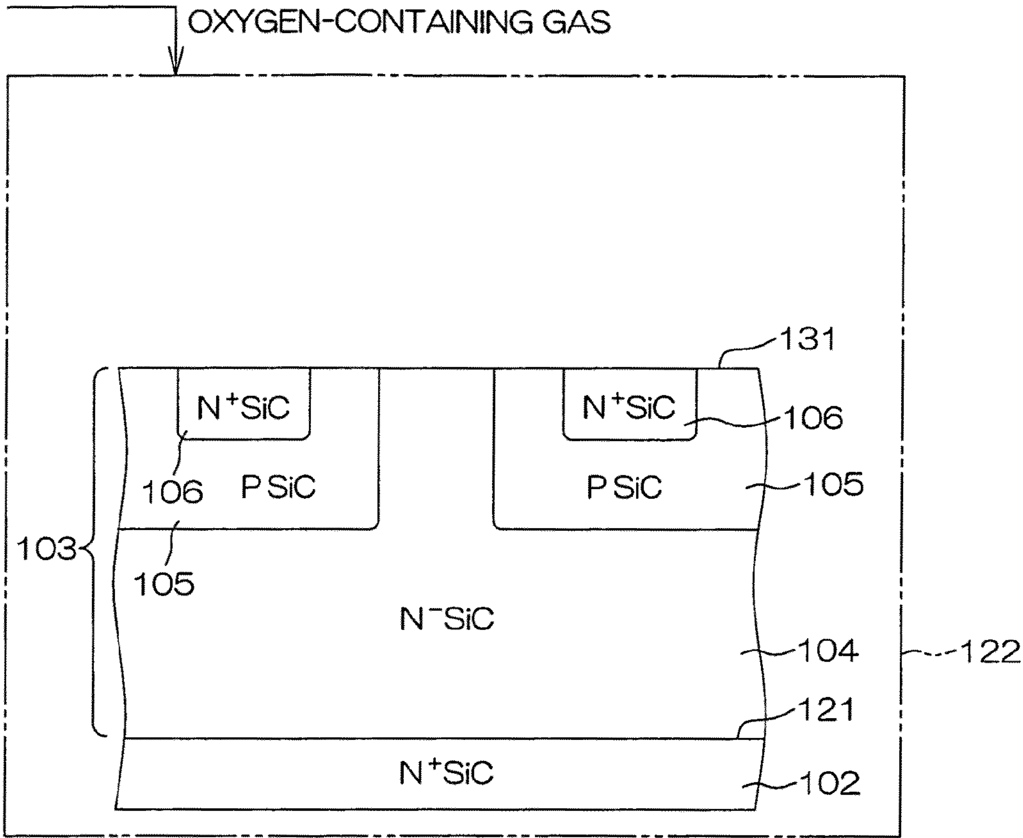


FIG. 13H

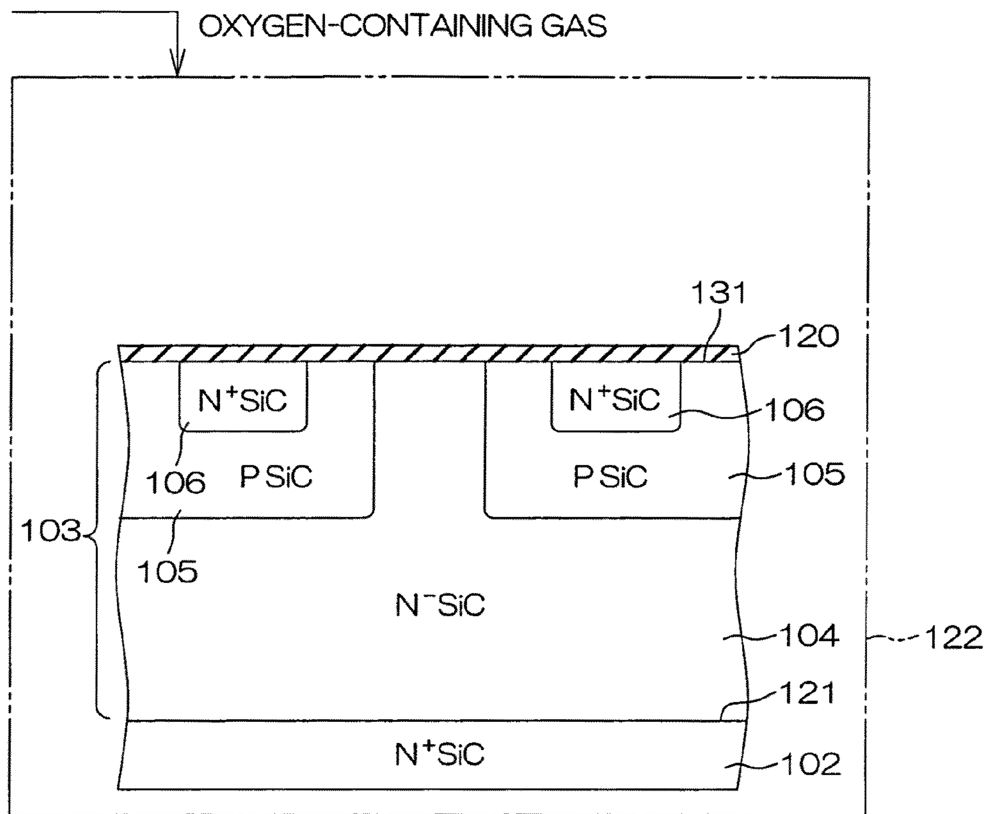


FIG. 13 I

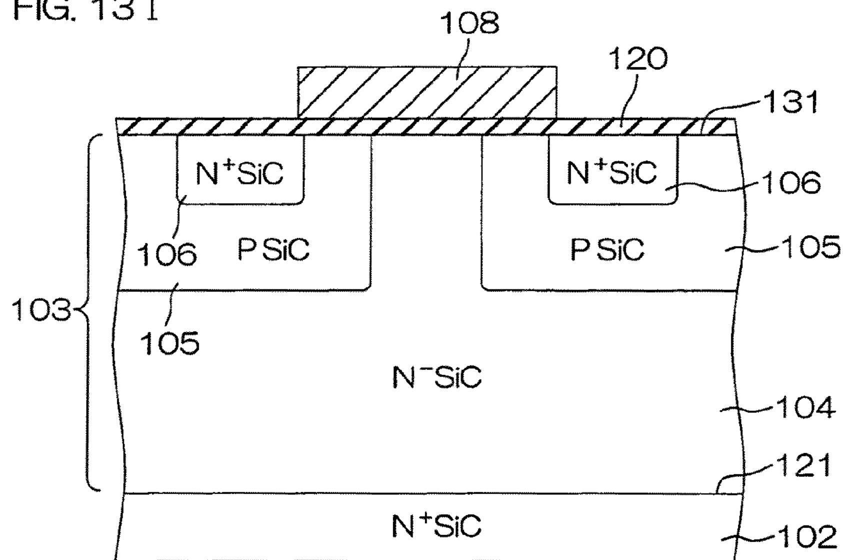


FIG. 13J

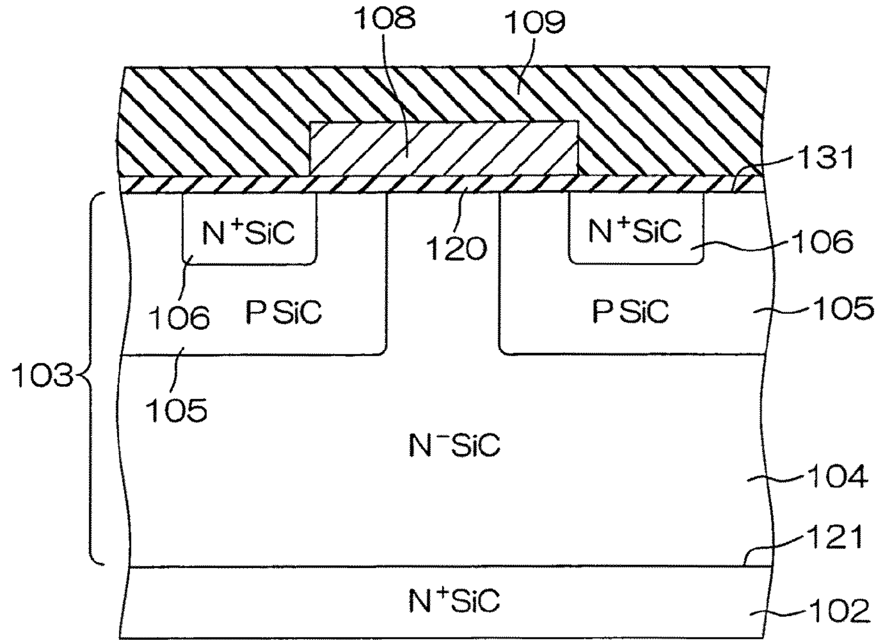


FIG. 13K

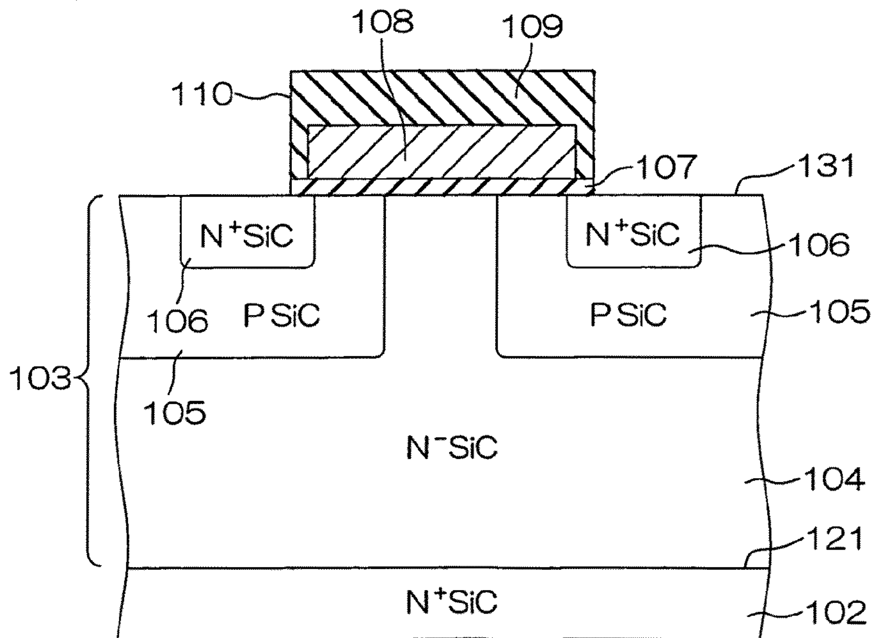


FIG. 13L

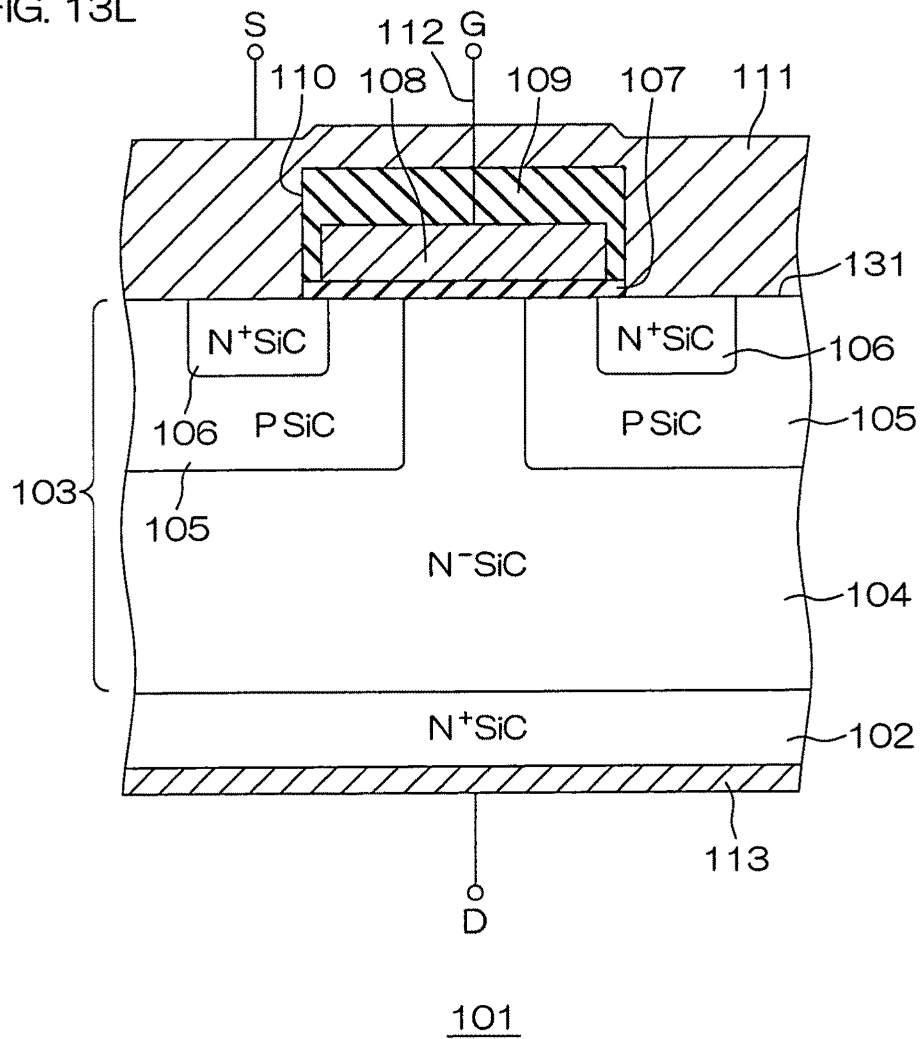
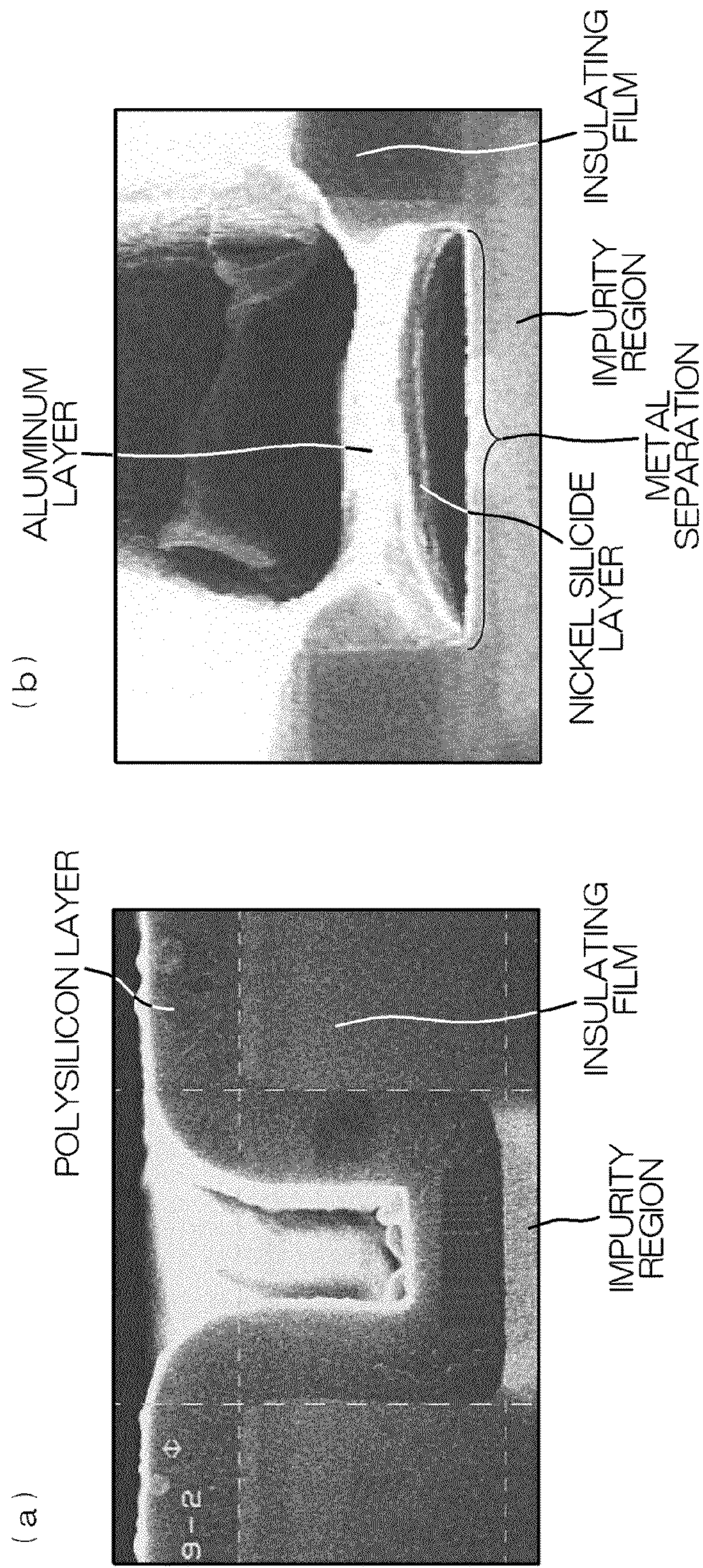


FIG. 14



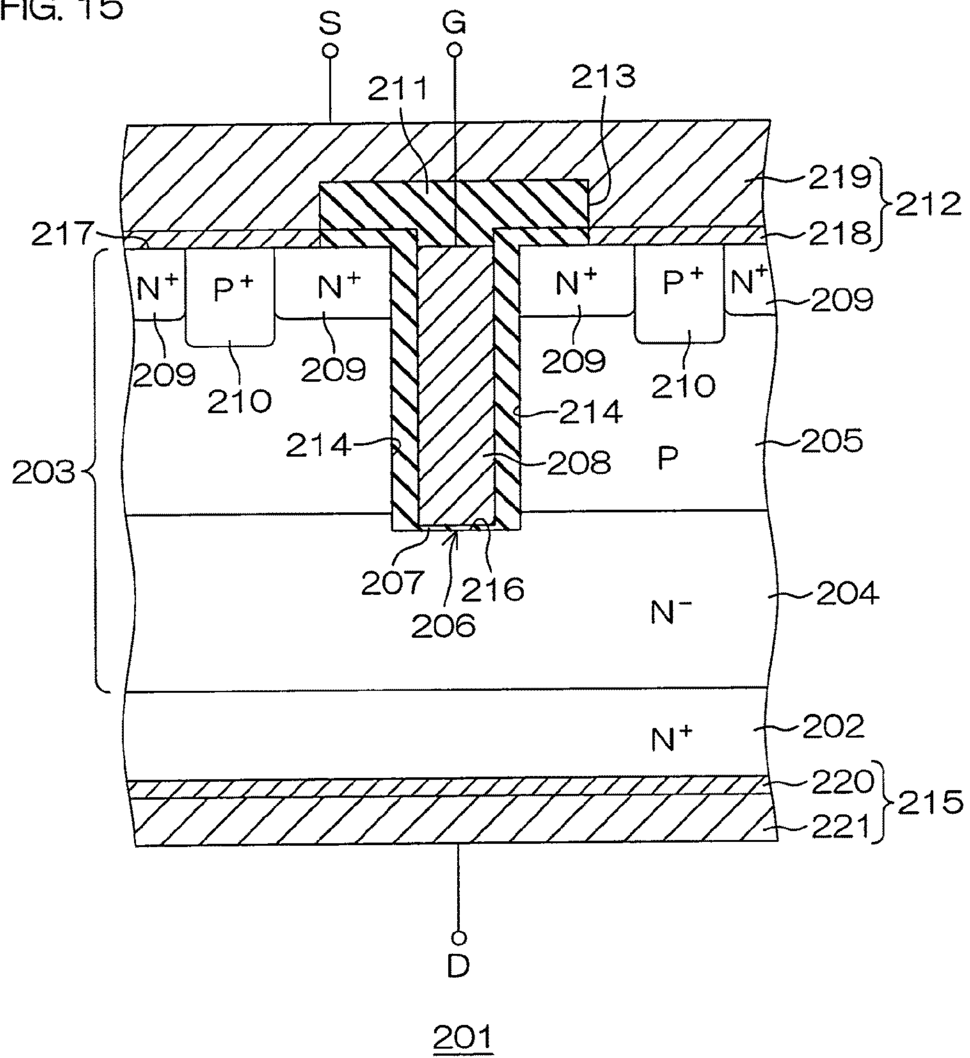


FIG. 15
S
G
211
213
219
212
218
217
N+
P+
N+
N+
P+
N+
209
209
210
209
209
210
214
214
203
208
P
205
207
216
206
N−
204
N+
202
220
215
221
D
201

SEMICONDUCTOR DEVICE

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

CROSS-REFERENCE TO RELATED APPLICATION

This application is a *reissue of U.S. patent application Ser. No. 13/364,416 (U.S. Pat. No. 9,293,575), issued on Mar. 22, 2016, which is a* divisional of application Ser. No. 12/654,621 filed on Dec. 24, 2009. Furthermore, this application claims the benefit of priority of Japanese applications 2008-330317 filed on Dec. 25, 2008, 2008-334480 filed on Dec. 26, 2008, and 2009-293361 filed on Dec. 24, 2009. The disclosures of these prior U.S. and Japanese applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device employing SiC.

2. Description of Related Art

In recent years, employment of SiC (silicon carbide) as the next-generation power device material implementing low on-resistance has been examined.

A trench gate structure is known as a structure for refining a power device and reducing on-resistance. For example, a power MOSFET employing the trench gate structure is increasingly forming the mainstream.

FIG. **15** is a schematic sectional view of a conventional SiC semiconductor device having a trench gate VDMOSFET.

A semiconductor device **201** includes an N^+-type SiC substrate **202** forming the base of the semiconductor device **201**. An N^--type epitaxial layer **203** made of SiC (silicon carbide) doped with an N-type impurity in a lower concentration than the SiC substrate **202** is laminated on an Si surface (a silicon surface) of the SiC substrate **202**. A base layer portion of the epitaxial layer **203** forms an N^--type drain region **204** maintaining a state after epitaxy. In the epitaxial layer **203**, a P-type body region **205** is formed on the drain region **204** in contact with the drain region **204**.

A gate trench **206** is dug down in the epitaxial layer **203** from a surface **217** (an Si surface) thereof. The gate trench **206** passes through the body region **205** in the thickness direction, and the deepest portion (a bottom surface **216**) thereof reaches the drain region **204**.

A gate insulating film **207** made of SiO_2 is formed in the gate trench **206**, to cover the overall regions of the inner surfaces of the gate trench **206**.

A gate electrode **208** is embedded in the gate trench **206** by filling up the inner side of the gate insulating film **207** with a polysilicon material doped with an N-type impurity in a high concentration.

On a surface layer portion of the epitaxial layer **203**, N^+-type source regions **209** are formed on both sides of the gate trench **206** in a direction (the right-and-left direction in FIG. **15**) orthogonal to the gate width. The source regions

209 extend along the gate trench **206** in a direction along the gate width, and bottom portions thereof are in contact with the body region **205**.

The epitaxial layer **203** is further provided with P^+-type body contact regions **210** passing through central portions of the source regions **209** in the direction orthogonal to the gate width from the surface **217** thereof to be connected to the body region **205**.

An interlayer dielectric film **211** made of SiO_2 is laminated on the epitaxial layer **203**. A source wire **212** is formed on the interlayer dielectric film **211**. The source wire **212** has a nickel silicide layer **218** in contact with the source regions **209** and the body contact regions **210** through a contact hole **213** formed in the interlayer dielectric film **211** and an aluminum layer **219** formed on the nickel silicide layer **218**.

A drain wire **215** is formed on the rear surface (a carbon surface: a C surface) of the SiC substrate **202**. The drain wire **215** has a nickel silicide layer **220** in contact with the SiC substrate **202** and an aluminum layer **221** formed on the nickel silicide layer **220**.

In order to form the source wire **212**, Ni is first deposited by sputtering on the surfaces (the surfaces of the source regions **209** and the body contact regions **210**) of regions (impurity regions) of the epitaxial layer **203** doped with impurities. Then, Ni is silicified by reacting with Si contained in SiC through a heat treatment at a high temperature (about 1000° C., for example), to be brought into ohmic contact with the impurity regions. Thus, the nickel silicide layer **218** is formed. Thereafter Al is deposited on the nickel silicide layer **218** by sputtering. Thus, the aluminum layer **219** is formed, to form the source wire **212**. The drain wire **215** is also formed by a method similar to that for the source wire **212**.

SUMMARY OF THE INVENTION

When the nickel silicide layer **218** is formed, carbon (C) remaining in SiC is deposited on the surface of the nickel silicide layer **218** and in the vicinity of the interfaces between the nickel silicide layer **218** and the impurity regions, to form a carbon layer containing a large quantity of C. The carbon layer is so poor in adhesiveness to a metal or SiC that the nickel silicide layer **218** is easily peeled from the aluminum layer **219** or the impurity regions. Such a disadvantage also applies to the drain wire **215**.

An object of the present invention is to provide a semiconductor device capable of improving connection reliability of a contact wire while ensuring ohmic contact between the contact wire and an impurity region in SiC.

The foregoing and other objects, features and effects of the present invention will become more apparent from the following detailed description of the embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic sectional view of a semiconductor device according to a first embodiment of the present invention.

FIGS. **2**A to **2**N are schematic sectional views for illustrating a method of manufacturing the semiconductor device shown in FIG. **1** in step order.

FIGS. **3**(a) and **3**(b) are schematic plan views of a semiconductor device according to a second embodiment of the present invention, with FIG. **3**(a) showing the overall semiconductor device and FIG. **3**(b) showing an inner portion thereof in an enlarged manner.

FIG. **4** is a schematic sectional view of the semiconductor device according to the second embodiment of the preset invention, taken along a line IV-IV in FIG. **3**(b).

FIGS. **5**A to **5**Q are schematic sectional views for illustrating a method of manufacturing the semiconductor device shown in FIG. **4** in step order.

FIG. **6** is a graph showing temperature changes in a resistance heating furnace.

FIG. **7** is a schematic sectional view for illustrating a modification of the semiconductor device shown in FIG. **4**.

FIGS. **8**(a) and **8**(b) are schematic plan views of a semiconductor device according to a third embodiment of the present invention, with FIG. **8**(a) showing the overall semiconductor device and FIG. **8**(b) showing an inner portion thereof in an enlarged manner.

FIG. **9** is a schematic sectional view of the semiconductor device according to the third embodiment of the pre sent invention, taken along a line IX-IX in FIG. **8**(b).

FIGS. **10**A to **10**N are schematic sectional views for illustrating a method of manufacturing the semiconductor device shown in FIG. **9** in step order.

FIG. **11** is a schematic sectional view for illustrating a modification of the semiconductor device shown in FIG. **9**.

FIG. **12** is a schematic sectional view of a planar gate semiconductor device.

FIGS. **13**A to **13**L are schematic sectional views for illustrating a method of manufacturing the semiconductor device shown in FIG. **12** in step order.

FIGS. **14**(a) and **14**(b) are SEM images of contact wires according to Example 1 and comparative example 1 respectively.

FIG. **15** is a schematic sectional view of a conventional SiC semiconductor device having a trench gate VDMOSFET.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A semiconductor device according to an embodiment of the present invention includes: a semiconductor layer made of SiC; an impurity region formed by doping the semiconductor layer with an impurity; and a contact wire formed on the semiconductor layer in contact with the impurity region, while the contact wire has a polysilicon layer in the portion in contact with the impurity region, and has a metal layer on the polysilicon layer.

According to the structure, the impurity region is formed in the semiconductor layer made of SiC by doping the semiconductor layer with the impurity. The contact wire is in contact with the impurity region. The contact wire has the polysilicon layer in the portion in contact with the impurity region, and has the metal layer on the polysilicon layer.

Polysilicon can form excellent ohmic contact with the region (the impurity region) of SiC doped with the impurity. Therefore, silicification indispensable for a structure having a metal layer directly in contact with an impurity region can be omitted. Thus, formation of a carbon layer can be prevented on the surface of the polysilicon layer and in the vicinity of the interface between the polysilicon layer and the impurity region.

Consequently, layer peeling can be suppressed between the polysilicon layer and the metal layer as well as between the polysilicon layer and the source region. Thus, connection reliability of the source wire can be improved.

Preferably, the semiconductor device further includes a gate trench dug down from the surface of the semiconductor layer, a first conductivity type body region formed in the semiconductor layer on a side portion of the gate trench, a gate insulating film formed on the inner surface of the gate trench, and a gate electrode embedded in the gate trench through the gate insulating film, the impurity region is a second conductivity type source region formed on a surface layer portion of the body region adjacently to the gate trench, and the contact wire is a source wire in contact with the source region.

According to the structure, the gate trench is dug down from the surface of the semiconductor layer. In the semiconductor layer, the first conductivity type body region is formed on the side portion of the gate trench. On the surface layer portion of the body region, the second conductivity type source region is formed adjacently to the gate trench. The source wire is in contact with the source region. The gate insulating film is formed on the bottom surface and the side surface of the gate trench. The gate electrode is embedded in the gate trench through the gate insulating film.

Thus, a trench gate VDMOSFET (Vertical Double Diffused MOSFET) having such a MOS (Metal Oxide Semiconductor) structure that the gate electrode (Metal) is opposed to the body region (Semiconductor) through a portion of the gate insulating film located on the side surface of the gate trench is formed in the semiconductor device.

In the semiconductor device, the source region is the impurity region, and the source wire is the contact wire. In other words, the source wire has the polysilicon layer in the portion in contact with the source region. Polysilicon is so excellent in coverage that coverage of the source wire can be improved by forming the polysilicon layer to fill up a contact hole. Consequently, the connection reliability of the source wire can be improved.

The semiconductor layer may further include a first conductivity type body region formed on a surface layer portion of the semiconductor layer, a gate insulating film formed on the surface of the semiconductor layer, and a gate electrode formed on the gate insulating film and opposed to the body region through the gate insulating film, the impurity region may be a second conductivity type source region formed on a surface layer portion of the body region, and the contact wire may be a source wire in contact with the source region.

The semiconductor device is the so-called planar gate VDMOSFET, in which the gate electrode is not embedded in a trench but formed on the gate insulating film formed on the surface of the semiconductor layer and opposed to the body region through the gate insulating film.

In the semiconductor device, the source region is the impurity region, and the source wire is the contact wire. In other words, the source wire has the polysilicon layer in the portion in contact with the source region. Polysilicon is so excellent in coverage that coverage of the source wire can be improved by forming the polysilicon layer to fill up a contact hole. Consequently, the connection reliability of the source wire can be improved.

Preferably, the polysilicon layer is a high-concentration doped layer doped with an impurity in a concentration of 10^{19} to 10^{21} cm^{-3}.

According to the structure, the polysilicon layer is the high-concentration doped layer, whereby resistance in the contact wire can be reduced.

Preferably in the semiconductor device, a layer containing titanium is interposed between the polysilicon layer and the metal layer.

A material containing titanium has excellent adhesiveness with respect to both of a polysilicon material and a metal material. In the semiconductor device having the layer

containing titanium interposed between the polysilicon layer and the metal layer, therefore, adhesiveness between the polysilicon layer and the metal layer can be improved. Consequently, the connection reliability of the contact wire can be further improved.

Preferably in the semiconductor device, the metal layer has a layer containing Al, and the layer containing titanium has a structure obtained by laminating a Ti layer and a TiN layer in this order from the side closer to the polysilicon layer.

While Al can be utilized as an impurity for providing the polysilicon layer with conductivity, the resistance of the polysilicon layer utilized as the source wire may be unstabilized unless Al is mixed into the polysilicon layer in a proper quantity.

In the structure of the semiconductor device, therefore, the TiN layer is interposed between the layer containing Al and the polysilicon layer, as a barrier layer for preventing diffusion of Al into the polysilicon layer. Thus, no excessive Al diffuses into the polysilicon layer, whereby the impurity concentration in the polysilicon layer can be stabilized. Consequently, the resistance of the polysilicon layer can be stabilized.

The polysilicon layer may be doped with at least one type of conductive impurity selected from a group consisting of B, P, Al and N.

In activation of the body region and the source region or formation of the gate insulating film, the semiconductor layer made of SiC may be heated to a temperature of not less than 1200° C., and the following is known as the background technique related to heating of a semiconductor layer made of SiC, for example:

More specifically, a MOSFET having a MOS (Metal Oxide Semiconductor) structure formed by an SiC layer having an activated ion region on a surface layer portion thereof, a gate oxide film formed on the surface of the SiC layer and a gate electrode formed on the gate oxide film and opposed to the ion region through the gate oxide film, for example, is known as a semiconductor device employing SiC.

In order to prepare such a MOS structure, impurity ions are first implanted into the surface layer portion of the SiC layer, for example. Then, the SiC layer is heated in a resistance heating furnace, whereby the implanted ions are activated. After the activation of the ions, the gate oxide film is formed on the surface of the SiC layer by feeding oxygen-containing gas in a CVD (Chemical Vapor Deposition) apparatus. Then, the gate electrode is formed on the gate oxide film by sputtering. Thus, a layered structure (the MOS structure) of the gate electrode (Metal), the gate oxide film (Oxide) and the SiC layer (Semiconductor) is produced.

In order to activate the ions in the SiC layer, the SiC layer must be annealed at a temperature of 1600 to 1700° C., for example. In the resistance heating furnace, it takes a long time to heat the SiC layer up to a high temperature range, and hence Si sublimates from the surface of the SiC layer by the so-called Si escape, to roughen the surface of the SiC layer. Consequently, the interface between the SiC layer and the gate oxide film is irregularized, to reduce channel mobility of the MOSFET.

Therefore, a technique of suppressing surface roughening of the SiC layer by utilizing a high-frequency induction heater for reducing the time for heating the SiC layer up to the high temperature range and thereafter forming the gate oxide film through a gate oxidation furnace is employed.

However, such a technique separately requires two apparatuses, i.e., the high-frequency induction heater and the gate oxidation furnace, and hence the device cost is disadvantageously increased.

Another technique of forming a carbon film on the surface of the SiC layer in advance of the activation of the ions and preventing the Si escape with the carbon film thereby maintaining planarity on the surface of the SiC layer is proposed.

The carbon film is prepared by forming a film containing carbon on the surface of the SiC layer and heating the film containing carbon in the high-frequency induction heater thereby evaporating elements other than carbon from the film, for example.

According to studies made by the inventors, however, a heating temperature for forming the carbon film may be about 1000° C., which is lower than the temperature (1600 to 1700° C.) for activating the ions. Therefore, the heating temperature must be controlled in two stages, while it has been recognized difficult to precisely temperature-control the high-frequency induction heater.

After the activation of the ions, the carbon film is no longer required. The unrequited carbon film is oxidized and removed with oxidizing gas in an apparatus different from the high-frequency induction heater. While the oxidizing gas may be introduced into the high-frequency induction heater to remove the carbon film subsequently to the activation of the ions, a carbon material is used for a heating element of the high-frequency induction heater and hence the carbon material is oxidized when fed with the oxidizing gas. Therefore, a carbon film removing apparatus is inevitably additionally required, to unavoidably increase the device cost.

In order to attain an object of providing a method of manufacturing a semiconductor device capable of suppressing roughening on the surface of an SiC layer through simple temperature control without increasing the device cost, the inventors have provided the following invention:

More specifically, the method of manufacturing a semiconductor device according to the invention includes the steps of forming an organic material film on the surface of an SiC layer having a surface layer portion into which ions have been implanted, altering the organic material film into a carbon film by heating the organic material film in a resistance heating furnace after the formation of the organic material film, activating the ions in the SiC layer by heating the SiC layer provided with the carbon film in the resistance heating furnace, oxidizing and removing the carbon film by introducing oxygen-containing gas into the resistance heating furnace, and forming an oxide film by oxidizing the surface of the SiC layer with the oxygen-containing gas in the resistance heating furnace continuously after the removal of the carbon film.

According to the method, the organic material film is heated in the resistance heating furnace after the formation of the organic material film, whereby the organic material film is altered into the carbon film, and the carbon film is formed on the surface of the SiC layer. After the formation of the carbon film, the SiC layer is heated in order to activate the ions in the SiC layer. Thereafter the carbon film is oxidized and removed by introducing the oxygen-containing gas into the resistance heating furnace. After the removal of the carbon film, the surface of the SiC layer is oxidized with the oxygen-containing gas continuously in the resistance heating furnace, so that the surface of the SiC layer is oxidized with the oxygen-containing gas and the oxide film is formed.

The carbon film is formed on the surface of the SiC layer in advance of the heating for activating the ions, whereby Si escape from the surface of the SiC layer can be prevented when the SiC layer is heated. Therefore, roughening on the surface of the SiC layer can be suppressed, and planarity on the surface of the SiC layer can be maintained. Consequently, the interface between the SiC layer and the oxide film can be smoothed, whereby channel mobility of the semiconductor device can be improved.

Further, the four steps of altering the organic material film into the carbon film by heating the same, activating the ions by heating the SiC layer, oxidizing and removing the carbon film with the oxygen-containing gas, and forming the oxide film by oxidizing the surface of the SiC layer can be continuously carried out in a single resistance heating furnace. No apparatus for removing the carbon film or the like is additionally required, whereby increase in the device cost can also be suppressed. Further, the resistance heating furnace is so employed that the heating temperature for forming the carbon film and that for activating the ions can be precisely and simply controlled.

The oxygen-containing gas may be gas containing oxygen and nitrogen. When the oxygen-containing gas for forming the oxide film contains oxygen and nitrogen, the channel mobility of the semiconductor device can be further improved.

Gas containing NO (nitrogen monoxide), N_2O (dinitrogen oxide) or the like, for example, can be employed as the gas containing oxygen and nitrogen.

Preferably, the surface of the SiC layer is defined by a (0001) plane, i.e., an Si surface.

As hereinabove described, the inventors have provided the invention utilizing the resistance heating furnace as the invention related to heating of the semiconductor layer made of SiC.

When the aforementioned invention utilizing the resistance heating furnace is applied in the activation of the body region and the source region as well as the formation of the gate insulating film, therefore, functions/effects of the aforementioned invention utilizing the resistance heating furnace can be attained in addition to those of the present invention.

Embodiments of the present invention are now described in detail with reference to the attached drawings.

FIG. **1** is a schematic sectional view of a semiconductor device according to a first embodiment of the present invention.

A semiconductor device **1** has a structure obtained by arranging a plurality of unit cells of a trench gate VDMOSFET in the form of a matrix. FIG. **1** shows only part of the plurality of unit cells.

The semiconductor device **1** includes an SiC substrate **2** forming the base thereof. The SiC substrate **2** is doped with an N-type impurity in a high concentration (10^{18} to 10^{21} cm^{-3}, for example). The SiC substrate **2** has a surface **21** (an upper surface) formed by an Si surface and a rear surface (a lower surface) **22** formed by a C surface.

An N^--type epitaxial layer **3** made of SiC (silicon carbide) doped with an N-type impurity in a lower concentration than the SiC substrate **2** is laminated on the surface **21** of the SiC substrate **2**. The epitaxial layer **3** formed on the surface **21**, i.e., the Si surface, is grown with a major growth surface formed by an Si surface. Therefore, the epitaxial layer **3** has a surface **31** formed by the Si surface.

A portion (a base layer portion) of the epitaxial layer **3** opposite to a portion (a surface layer portion) on the side of the Si surface forms an N^--type drain region **4** entirely maintaining a state after epitaxy. The drain region **4** has an N-type impurity concentration of 10^{15} to 10^{17} cm^{-3}, for example.

On the other hand, a P-type body region **5** is formed on the surface layer portion of the epitaxial layer **3**. The body region **5** is in contact with the drain region **4**. The body region **5** has a P-type impurity concentration of 10^{16} to 10^{19} cm^{-3}, for example.

A gate trench **6** is dug down in the epitaxial layer **3** from the surface **31** thereof. A plurality of such gate trenches **6** (not shown in FIG. **1**) are formed at regular intervals to parallelly extend in the same direction (a direction parallel to the plane of FIG. **1**: the direction may hereinafter be referred to as a "direction along the gate width"), thereby forming a striped structure, for example.

Each gate trench **6** has planar side surfaces **7** opposed to each other at an interval and orthogonal to the surface **31** respectively and a bottom surface **8** having a portion parallel to the surface **31**. The gate trench **6** passes through the body region **5** in the thickness direction, and the deepest portion (the bottom surface **8**) thereof reaches the drain region **4**.

A gate insulating film **9** made of SiO_2 is formed on the inner surfaces of the gate trench **6** and the surface **31** of the epitaxial layer **3**, to cover the overall regions of the inner surfaces (the side surfaces **7** and the bottom surface **8**) of the gate trench **6**. In the gate insulating film **9**, the thickness of a portion (an insulating film bottom portion **11**) located on the bottom surface **8** is smaller than that of portions (insulating film side portions **10**) located on the side surfaces **7**. For example, the ratio (thickness of insulating film bottom portion **11**/thickness of insulating film side portion **10**) of the thickness of the insulating film bottom portion **11** to that of the insulating film side portions **10** is 0.1 to 0.8. More specifically, the thickness of the insulating film side portions **10** is 400 to 600 Å and that of the insulating film bottom portion **11** is 200 to 300 Å, for example.

A gate electrode **12** is embedded in the gate trench **6** by filling up the inner side of the gate insulating film **9** with a polysilicon material doped with an N-type impurity in a high concentration.

On a surface layer portion of the body region **5**, N^+-type source regions **13** are formed on both sides of the gate trench **6** in a direction (the right-and-left direction in FIG. **1**) orthogonal to the gate width. The source regions **13** are doped with an N-type impurity in a higher concentration than the drain region **4**. The source regions **13** have an N-type impurity concentration of 10^{18} to 10^{21} cm^{-3}, for example. The source regions **13** extend in the direction along the gate width on positions adjacent to the gate trench **6**, and the bottom portions thereof are in contact with the body region **5** from the side of the surface **31** of the epitaxial layer **3**.

The epitaxial layer **3** is provided with P^+-type body contact regions **14** pas sing through central portions of the source regions **13** in the direction orthogonal to the gate width from the surface **31** thereof to be connected to the body region **5**. The body contact regions **14** are doped with a P-type impurity in a higher concentration than the body region **5**. The body contact regions **14** have a P-type impurity concentration of 10^{18} to 10^{21} cm^{-3}, for example.

In other words, the gate trench **6** and the source regions **13** are alternately provided in the direction orthogonal to the gate width, and extend in the direction along the gate width respectively. Boundaries between the unit cells adjacent to one another in the direction orthogonal to the gate width are set on the source regions **13** along the source regions **13**. At least one or more body contact regions **14** are provided over

two unit cells adjacent to each other in the direction orthogonal to the gate width. The boundaries between the unit cells adjacent to one another in the direction along the gate width are so set that the gate electrode **12** included in each unit cell has a constant gate width.

An interlayer dielectric film **15** made of SiO_2 is laminated on the epitaxial layer **3**. A contact hole **16** exposing the surfaces of the source regions **13** and the body contact regions **14** is formed in the interlayer dielectric film **15** and the gate insulating film **9**.

A source wire **17** is formed on the interlayer dielectric film **15**. The source wire **17** is in contact (electrically connected) with the source regions **13** and the body contact regions **14** through the contact hole **16**. The source wire **17** has a polysilicon layer **18** in the portion in contact with the source regions **13** and the body contact regions **14**, and has a metal layer **20** on the polysilicon layer **18**.

The polysilicon layer **18** is a doped layer made of doped polysilicon doped with an impurity, and preferably a high-concentration doped layer doped with the impurity in a high concentration of 10^{19} to 10^{21} cm^{-3}, for example. The impurity for forming the polysilicon layer **18** as the doped layer (including the high-concentration doped layer) can be prepared from an N-type impurity such as P (phosphorus) or As (arsenic) or a P-type impurity such as B (boron). The polysilicon layer **18** fills up the contact hole **16**. The thickness of the polysilicon layer **18** is 5000 to 10000 Å, for example, depending on the depth of the contact hole **16**.

The metal layer **20** is made of aluminum (Al), gold (Au), silver (Ag) or copper (Cu), an alloy thereof, or a metal material containing the same, for example. The metal layer **20** forms the outermost layer of the source wire **17**, and a metal wire or the like, for example, is connected (bonded) thereto. The thickness of the metal layer **20** is 1 to 5 μm, for example.

In the source wire **17**, an intermediate layer **19** containing titanium is interposed between the polysilicon layer **18** and the metal layer **20**. The intermediate layer **19** is formed by a single layer containing titanium (Ti) or a plurality of layers including the layer. The layer containing titanium can be prepared from titanium, titanium nitride or the like. The thickness of the intermediate layer **19** is 200 to 500 ∈, for example.

The aforementioned source wire **17** having the polysilicon layer **18**, the intermediate layer **19** and the metal layer **20** preferably has a multilayer structure (Poly-Si/Ti/TiN/Al) obtained by successively laminating polysilicon (the polysilicon layer **18**), titanium (the intermediate layer **19**), titanium nitride (the intermediate layer **19**) and aluminum (the metal layer **20**).

A drain wire **23** is formed on the rear surface **22** of the SiC substrate **2**. The drain wire **23** is in contact (electrically connected) with the SiC substrate **2**. The drain wire **23** has a polysilicon layer **24** in the portion in contact with the SiC substrate **2**, and has a metal layer **26** on the polysilicon layer **24**.

The polysilicon layer **24** can be made of a material similar to that constituting the aforementioned polysilicon layer **18**. The thickness of the polysilicon layer **24** is 1000 to 2000 Å, for example.

The metal layer **26** can be made of a material similar to that constituting the aforementioned metal layer **20**. The metal layer **26** forms the outermost layer of the drain wire **23**, and is bonded to a die pad of a lead frame when the SiC substrate **2** is bonded to the die pad, for example. The thickness of the metal layer **26** is 0.5 to 1 μm, for example.

In the drain wire **23**, an intermediate layer **25** containing titanium is interposed between the polysilicon layer **24** and the metal layer **26**. The intermediate layer **25** can be made of a material similar to that constituting the aforementioned intermediate layer **19**.

A gate wire **27** is in contact (electrically connected) with the gate electrode **12** through a contact hole (not shown) formed in the interlayer dielectric film **15**.

A prescribed voltage (a voltage of not less than a gate threshold voltage) is applied to the gate wire **27** while a prescribed potential difference is caused between the source wire **17** and the drain wire **23** (between a source and a drain), whereby a channel is formed in the vicinity of the interface between the body region **5** and the gate insulating film **9** due to an electric field from the gate electrode **12**. Thus, a current flows between the source wire **17** and the drain wire **23**, and the VDMOSFET is turned on.

FIGS. **2**A to **2**N are schematic sectional views for illustrating a method of manufacturing the semiconductor device **1** shown in FIG. **1** in step order.

First, an SiC crystal is grown on the surface **21** (the Si surface) of the SiC substrate **2** by epitaxy such as CVD (Chemical Vapor Deposition), LPE (Liquid Phase Epitaxy) or MBE (Molecular Beam Epitaxy) while doping the same with an impurity, as shown in FIG. **2**A. Thus, the N^--type epitaxial layer **3** is formed on the SiC substrate **2**. Then, a P-type impurity is implanted into the epitaxial layer **3** from the surface **31** thereof. While the implantation conditions vary with the type of the P-type impurity, acceleration energy is 200 to 400 keV, for example.

Thus, a region (a P-type implantation region **28**) into which the P-type impurity has been implanted is formed on the surface layer portion of the epitaxial layer **3**, as shown in FIG. **2**B. Due to the formation of the P-type implantation region **28**, the drain region **4** isolated from the P-type implantation region **28** while maintaining the state after the epitaxy is formed on the base layer portion of the epitaxial layer **3**.

Then, a mask **29** made of SiO_2 is formed on the epitaxial layer **3** by CVD, as shown in FIG. **2**C. Then, the mask **29** is etched through a photoresist film (not shown) into a pattern having openings **30** in regions for forming the body contact regions **14**. After the formation of the openings **30**, a P-type impurity is implanted into the epitaxial layer **3** from the surface **31** thereof. While the implantation conditions vary with the type of the P-type impurity, acceleration energy is 30 to 200 keV, for example. Thus, regions (P^+-type implantation regions **32**) into which the P-type impurity has been implanted in a high concentration are formed on a surface layer portion of the P-type implantation region **28**. After the implantation of the P-type impurity, the mask **29** is removed.

Then, a mask **33** made of SiO_2 is formed on the epitaxial layer **3** by CVD (Chemical Vapor Deposition), as shown in FIG. **2**D. Then, the mask **33** is etched through a photoresist film (not shown) into a pattern having openings **34** in regions for forming the source regions **13**. After the formation of the openings **34**, an N-type impurity is implanted into the epitaxial layer **3** from the surface **31** thereof. While the implantation conditions vary with the type of the N-type impurity, acceleration energy is 30 to 200 keV, for example. After the implantation of the N-type impurity, the mask **33** is removed. Thus, a region (an N^+-type implantation region **35**) into which the N-type impurity has been implanted in a high concentration is formed on the surface layer portion of the P-type implantation region **28**.

Then, the epitaxial layer **3** is heat-treated at a temperature of 1400 to 2000° C., for example, as shown in FIG. **2**E.

Thus, the implanted N- and P-type impurities are activated, whereby the body region **5** is formed on the surface layer portion **3** of the epitaxial layer **3**, while the source regions **13** and the body contact regions **14** are formed on the surface layer portion of the body region **5**.

Then, a mask **36** made of SiO_2 is formed on the overall region of the surface **31** of the epitaxial layer **3** by CVD or thermal oxidation, as shown in FIG. **2**F. The mask **36** may alternatively be made of SiN or the like through CVD.

Then, the mask **36** is etched through a photoresist film (not shown) into a pattern having an opening **37** in a region for forming the gate trench **6**, as shown in FIG. **2**G.

Then, mixed gas (SF_6/O_2 gas) containing SF_6 (sulfur hexafluoride) and O_2 (oxygen) is introduced into the surface **31** of the epitaxial layer **3** through the opening **37**, as shown in FIG. **2**H. Thus, the epitaxial layer **3** is dry-etched from the surface **31** (the Si surface), and the gate trench **6** having the bottom surface **8** having the portion (the Si surface) parallel to the surface **31** and the side surfaces **7** orthogonal to the Si surface is formed. After the formation of the gate trench **6**, the mask **36** is removed.

Then, the inner surfaces (the side surfaces **7** and the bottom surface **8**) of the gate trench **6** and the surface **31** of the epitaxial layer **3** are oxidized by thermal oxidation, as shown in FIG. **2**I. The gate trench **6** is formed in the epitaxial layer **3** made of SiC, and hence the oxidation of the inner surfaces of the gate trench **6** progresses under the condition that the oxidation rate for the bottom surface **8** having the Si surface and that for the side surfaces **7** orthogonal to the Si surface satisfy the following relational expression:

Oxidation rate for bottom surface 8/oxidation rate for side surface 7<0

Thus, the gate insulating film **9** is formed so that the thickness of the portion (the insulating film bottom portion **11**) located on the bottom surface **8** is smaller than that of the portions (the insulating film side portions **10**) located on the side surfaces **7**.

Then, a doped polysilicon material is deposited on the epitaxial layer **3** by CVD, as shown in FIG. **2**J. The deposited polysilicon material is etched back until the etched-back surface is flush with the surface **31** of the epitaxial layer **3**. Thus, portions of the polysilicon layer located outside the gate trench **6** are removed, and the gate electrode **12** is formed by the polysilicon material remaining in the gate trench **6**.

Then, the interlayer dielectric film **15** made of SiO_2 is laminated on the epitaxial layer **3** by CVD, as shown in FIG. **2**K. Then, the interlayer dielectric film **15** and the gate insulating film **9** are so patterned that the contact hole **16** exposing the source regions **13** and the body contact regions **14** is formed in the interlayer dielectric film **15** and the gate insulating film **9**.

Then, a polysilicon material **38** is laminated by CVD to fill up the contact hole **16**, as shown in FIG. **2**L.

Then, an N- or P-type impurity is implanted into the deposited polysilicon material, as shown in FIG. **2**M. While the implantation conditions vary with the type of the impurity, acceleration energy is 10 to 100 keV, for example. Thus, the polysilicon layer **18** doped with the impurity in a high concentration is formed.

Then, titanium and titanium nitride are deposited in this order on the surface of the polysilicon layer **18** by a method such as sputtering or vapor deposition to form the intermediate layer **19**, as shown in FIG. **2**N. Then, aluminum is deposited on the surface of the intermediate layer **19** by a method such as sputtering or vapor deposition, to form the metal layer **20**. Then, the metal layer **20**, the intermediate layer **19** and the polysilicon layer **18** are worked into a prescribed pattern, to form the source wire **17**. Then, the gate wire **27** connected to the gate electrode **12** is formed. Thereafter the drain wire **23** having the polysilicon layer **24**, the intermediate layer **25** and the metal layer **26** is formed on the rear surface **22** of the SiC substrate **2** by a method similar to that for the source wire **17**.

The semiconductor device **1** shown in FIG. **1** is obtained through the aforementioned steps.

In the semiconductor device **1**, as hereinabove described, the source wire **17** in contact with the source regions **13** and the body contact regions **14** has the polysilicon layer **18** in the portion in contact with the source regions **13** and the body contact regions **14**, and has the metal layer **20** on the polysilicon layer **18**.

Polysilicon can form excellent ohmic contact with a region (an impurity region) of SiC doped with an impurity. Therefore, ohmic contact can be formed between the polysilicon layer **18** and the source regions **13** as well as the body contact regions **14** by depositing the polysilicon material **38** by CVD as hereinabove described and bringing the polysilicon layer **18** into contact with the source regions **13** and the body contact regions **14**.

Therefore, silicification indispensable for a structure having a metal layer directly brought into contact with an impurity region can be omitted. Thus, formation of a carbon layer can be prevented on the surface of the polysilicon layer **18** and in the vicinity of the interface between the polysilicon layer **18** and the source regions **13** and the body contact regions **14**.

Consequently, layer peeling can be suppressed between the polysilicon layer **18** and the metal layer **20** as well as between the polysilicon layer **18** and the source regions **13** and the body contact regions **14**. Thus, connection reliability of the source wire **17** can be improved.

The source wire **17** is in contact with the source regions **13** and the body contact regions **14** through the contact hole **16** of the interlayer dielectric film **15**. In the source wire **17**, the polysilicon layer **18** made of the polysilicon material excellent in coverage is formed with the thickness filling up the contact hole **16**. Therefore, coverage of the source wire **17** can be improved. Consequently, the connection reliability of the source wire **17** can be further improved. Further, planarity of the metal layer **20** formed on the polysilicon layer **18** can be improved. Consequently, bondability can be improved when the metal wire is bonded to the metal layer **20**.

The polysilicon layer **18** is a high-concentration doped layer doped with the impurity in the high concentration of 10^{19} to 10^{21} cm^{-3}, whereby the resistance of the source wire **17** can be reduced.

Further, the intermediate layer **19** having the multilayer structure of the titanium layer and the titanium nitride layer is interposed between the polysilicon layer **18** and the metal layer **20**. A material containing titanium has excellent adhesiveness with respect to both of a polysilicon material and a metal material. Therefore, the adhesiveness between the polysilicon layer **18** and the metal layer **20** can be improved. Consequently, the connection reliability of the source wire **17** can be further improved.

Functions and effects attained by the drain wire **23** having the polysilicon layer **24**, the intermediate layer **25** and the metal layer **26** are similar to those attained by the source wire **17**, and hence redundant description is omitted.

FIGS. **3**(a) and **3**(b) are schematic plan views of a semiconductor device according to a second embodiment of

the present invention, with FIG. 3(a) showing the overall semiconductor device and FIG. 3(b) showing an inner portion thereof in an enlarged manner.

A semiconductor device 41 according to the second embodiment of the present invention is a trench gate power VDMOSFET (an individual device) employing SiC, in the form of a chip square in plan view, for example. The chip-like semiconductor device 41 has a length of about several mm in the right-and-left (vertical) direction in the plane of FIG. 3(a).

The semiconductor device 41 has an SiC substrate 42 and a large number of unit cells 44 formed on the SiC substrate 42 and partitioned by a gate trench 43 latticed in plan view. In other words, the unit cells 44 in the form of rectangular parallelepipeds arranged in window portions of the latticed gate trench 43 respectively are aligned on the SiC substrate 42 in the form of a matrix. Each unit cell 44 has a length of not more than 10 μm in the right-and-left (vertical) direction in the plane of FIG. 3(b), for example, and a source trench 45, square in plan view, dug down from the surface side toward the side of the SiC substrate 42 is formed at the center thereof.

A source pad 46 is formed on the surface of the semiconductor device 41. The source pad 46 is generally in the form of a square having outwardly bent four corners in plan view, and formed to generally cover the overall region of the surface of the semiconductor device 41. A removed region 47 is formed in the source pad 46 by partially removing the same in a generally square manner in plan view, on a position slightly leftward in the right-and-left direction in the plane of FIG. 3(a).

A gate pad 48 is arranged on the removed region 47. An interval is provided between the gate pad 48 and the source pad 46, which are insulated from each other.

FIG. 4 is a schematic sectional view of the semiconductor device 41 according to the second embodiment of the preset invention, taken along a line IV-IV in FIG. 3(b).

The sectional structure of the semiconductor device 41 is described with reference to FIG. 4. The semiconductor device 4 includes the SiC substrate 42 of an N^+-type (having a concentration of 10^{18} to 10^{21} cm^{-3}, for example). The SiC substrate 42 has a surface 49 (an upper surface) formed by an Si surface and a rear surface 50 (a lower surface) formed by a C surface.

An N^--type epitaxial layer 51 made of SiC having a lower concentration (10^{15} to 10^{17} cm^{-3}, for example) than the SiC substrate 42 is laminated on the SiC substrate 42. The epitaxial layer 51 as a semiconductor layer is formed on the SiC substrate 42 by the so-called epitaxy. The epitaxial layer 51 formed on the surface 49, i.e., the Si surface, is grown on a major growth surface formed by an Si surface. Therefore, a surface 52 of the epitaxial layer 51 formed by the growth is an Si surface, similarly to the surface 49 of the SiC substrate 42.

On the side of the epitaxial layer 51 closer to the surface 52 (the Si surface), a P-type body region 53 is provided in the form of a well over a wide range, with a concentration of 10^{16} to 10^{19} cm^{-3}, for example. A region of the epitaxial layer 51 closer to the SiC substrate 42 (the C surface) than the body region 53 forms an N^--type drain region 54 (a drift region) maintaining the state after the epitaxy.

In the body region 53, an N^+-type source region 55 (having a concentration of 10^{18} to 10^{21} cm^{-3}, for example) is formed generally on the overall region of the side closer to the surface 52, while a P^+-type body contact region 56 (having a concentration of 10^{18} to 10^{21} cm^{-3}, for example) is formed on a side (the lower side) closer to the SiC substrate 42 than the source region 55. A large number of such body contact regions 56 are provided in the form of a matrix.

Source trenches 45 are formed in the same number as the body contact regions 56 so that each source trench 45 passes through each body contact region 56, and the latticed gate trench 43 is formed to surround each body contact region 56 provided with the source trench 45. Thus, the large number of unit cells 44 functioning as field-effect transistors respectively are formed on the epitaxial layer 51. In other words, the body contact region 56 is formed to surround the corresponding source trench 45 and the body region 53 is formed to surround the body contact region 56 in each unit cell 44. A side of the body region 53 opposite to the side closer to the body contact region 56 is exposed on the side surfaces of the gate trench 43. In the unit cell 44, the depth direction of the gate trench 43 corresponds to a gate length direction, and the peripheral direction of each unit cell 44 orthogonal to the gate length direction corresponds to a gate width direction.

Both of the source trench 45 and the gate trench 43 pass through the body region 53 from the surface 52 of the epitaxial layer 51 to reach the drain region 54, and the depths thereof are identical to each other in the second embodiment. The distance D_1 between side surfaces 59 and 57 of the source trench 45 and the gate trench 43 is 0.5 to 3 μm, for example. When the distance D_1 is in this range, increase in resistance (on-resistance) can be suppressed when each unit cell 44 is turned on, and an electric field applied to the bottom portion of the gate trench 43 can be relaxed.

The gate trench 43 is U-shaped in section, such that both end corner portions 61 of the bottom portion thereof in a direction (a direction opposed to the adjacent unit cell 44) orthogonal to the gate width are bent toward the side of the drain region 54 and the side surfaces 57 opposed to each other and a bottom surface 58 are continuous through bent surfaces. The source trench 45 is also U-shaped in section similarly to the gate trench 43, such that the side surfaces 59 opposed to each other and a bottom surface 60 are continuous through bent surfaces. When the unit cell 44 is turned off, therefore, the electric field applied to both end corner portions 61 of the bottom portion of the gate trench 43 can be dispersed to portions other than both end corner portions 61, whereby a portion of the gate insulating film 63 located on the bottom surface 58 can be prevented from dielectric breakdown.

A gate insulating film 63 is formed on the inner surfaces of the gate trench 43, to cover the overall regions thereof. The gate insulating film 63 consists of an oxide film containing nitrogen, such as a silicon oxynitride film formed by thermal oxidation with gas containing nitride and oxygen, for example. The nitrogen content (the nitrogen concentration) in the gate insulating film 63 is 0.1 to 10%, for example.

A gate electrode 66 is embedded in the gate trench 43 by filling up the inner side of the gate insulating film 63 with a polysilicon material doped with an N-type impurity in a high concentration.

An interlayer dielectric film 67 made of SiO_2 is laminated on the epitaxial layer 51. A contact hole 68 exposing the surfaces of the source trench 45 and the source region 55 of each unit cell 44 is formed in the interlayer dielectric film 67 and the gate insulating film 63.

A source wire 69 is formed on the interlayer dielectric film 67. The source wire 69 collectively enters the source trench 45 of every unit cell 44 through each contact hole 68, and is in contact with the drain region 54, the body contact region

56 and the source region 55 successively from the bottom side of the source trench 45 in each unit cell 44. In other words, the source wire 69 is common to all unit cells 44. An interlayer dielectric film (not shown) is formed on the source wire 69, which in turn is electrically connected to the source pad 46 (see FIG. 3(a)) through the interlayer dielectric film (not shown). On the other hand, the gate pad 48 (see FIG. 3(a)) is electrically connected to the gate electrode 66 through a gate wire (not shown) drawn onto the interlayer dielectric film (not shown).

The source wire 69 has a polysilicon layer 70, an intermediate layer 71 and a metal layer 72 successively from the side in contact with the epitaxial layer 51.

The polysilicon layer 70 is a doped layer made of doped polysilicon doped with an impurity, such as a high-concentration doped layer doped with the impurity in a high concentration of 10^{19} to 10^{21} cm^{-3}, for example. The impurity for forming the polysilicon layer 70 as the doped layer (including the high-concentration doped layer) can be prepared from an N-type impurity such as N (nitrogen), P (phosphorus) or As (arsenic)or a P-type impurity such as Al (aluminum) or B (boron). The thickness of the polysilicon layer 70 is 5000 to 10000 Å, for example.

According to the second embodiment, the polysilicon layer 70 is formed to cover the overall region of the surface of the unit cell 44 exposed in the contact hole 68, and in contact with the drain region 54, the body contact region 56 and the source region 55 in the source trench 45.

The layer of the source wire 69 in contact with the drain region 54, the body contact region 56 and the source region 55 is made of polysilicon, whereby the source wire 69 can be brought into ohmic contact with both of the body contact region 56 and the source region 55, which are high-concentration impurity regions. On the other hand, a heterojunction having a smaller junction barrier than the diffusion potential of a body diode 73 (a PN diode formed by junction between the body region 53 and the drain region 54) intrinsic in the semiconductor device 41 can be formed with respect to the low-concentration drain region 54.

When a current flows to the body diode 73 intrinsic in the semiconductor device 41, positive holes (holes) moving from the body region 53 to the drain region 54 recombine with electrons in the drain region 54, and a defect of an SiC crystal in the epitaxial layer 51 may spread in the plane due to the resulting recombination energy. The resistance of the crystal defect is so high that the crystal defect may hinder an ordinary transistor operation to increase on-resistance when spreading toward the side of the gate trench 43.

When the heterojunction is formed due to the contact between the polysilicon layer 70 and the drain region 54 as in the second embodiment, on the other hand, a current can be fed to the side of the heterojunction in preference to the side of the body diode 73, even if a reverse voltage is applied between the source and the drain and the current can flow to the aforementioned body diode 73. Consequently, the crystal defect of SiC can be prevented from spreading, and increase in the on-resistance can be suppressed.

The intermediate layer 71, laminated on the polysilicon layer 70, is formed by a single layer containing Ti (titanium) or a plurality of layers including the layer. The layer containing Ti can be prepared from Ti, TiN (titanium nitride) or the like. The thickness of the intermediate layer 71 is 200 to 500 nm, for example.

The metal layer 72, laminated on the intermediate layer 71, is made of Al (aluminum), Au (gold), Ag (silver), Cu (copper) or Mo (molybdenum), an alloy thereof, or a metal material containing the same, for example. The metal layer 72 forms the outermost layer of the source wire 69. The thickness of the metal layer 72 is 1 to 5 μm, for example.

More specifically, the polysilicon layer 70, the intermediate layer 71 and the metal layer 72 may be combined in a multilayer structure (Poly-Si/Ti/TiN/Al) obtained by successively laminating Poly-Si (the polysilicon layer 70), Ti (the intermediate layer 71), TiN (the intermediate layer 71) and Al (the metal layer 72).

A drain electrode 74 is formed on the rear surface 50 of the SiC substrate 42, to cover the overall region thereof. The drain electrode 74 is common to all unit cells 44. The drain electrode 74 has a multilayer structure (Ti/Al) obtained by laminating Ti and Al successively from the side of the SiC substrate 42, for example.

A prescribed voltage (a voltage of not less than a gate threshold voltage) is applied to the gate pad 48 while a prescribed potential difference is caused between the source pad 46 (the source wire 69) and the drain electrode 74 (between a source and a drain), whereby a channel is formed in the vicinity of the interface between the body region 53 and the gate insulating film 63 due to an electric field from the gate electrode 66. Thus, a current flows between the source wire 69 and the drain wire 74, and the VDMOSFET is turned on.

FIGS. 5A to 5Q are schematic sectional views for illustrating a method of manufacturing the semiconductor device 41 shown in FIG. 4 in step order.

First, an SiC crystal is grown on the surface 49 (the Si surface) of the SiC substrate 42 by epitaxy such as CVD (Chemical Vapor Deposition), LPE (Liquid Phase Epitaxy) or MBE (Molecular Beam Epitaxy) while doping the same with an impurity, as shown in FIG. 5A. Thus, the N^--type epitaxial layer 51 is formed on the SiC substrate 42.

Then, a P-type impurity is implanted into the epitaxial layer 51 from the surface 52 thereof, as shown in FIG. 5B. While the implantation conditions vary with the type of the P-type impurity, acceleration energy is 200 to 3000 keV, for example.

Then, a mask 75 made of SiO_2 is formed on the epitaxial layer 51 by CVD, as shown in FIG. 5C. Then, the mask 75 is etched through a photoresist film (not shown) into a pattern having an opening 76 in a region for forming the body contact region 56. After the formation of the opening 76, a P-type impurity is implanted into the epitaxial layer 51 from the surface 52 thereof. While the implantation conditions vary with the type of the P-type impurity, acceleration energy is 30 to 400 keV, for example. After the implantation of the P-type impurity, the mask 75 is removed.

Then, an N-type impurity is implanted into the epitaxial layer 51 from the surface 52 thereof, as shown in FIG. 5D. While the implantation conditions vary with the type of the N-type impurity, acceleration energy is 30 to 400 keV, for example.

Then, a mask 77 made of SiO_2 is formed on the overall region of the surface 52 of the epitaxial layer 51 by CVD or thermal oxidation, as shown in FIG. 5E. The mask 77 may alternatively be made of SiN or the like through CVD. Then, the mask 77 is etched through a photoresist film (not shown) into a pattern having openings 78 in regions for forming the gate trench 43 and the source trench 45. After the formation of the openings 78, mixed gas (SF_6/O_2 gas) containing SF_6 (sulfur hexafluoride) and O_2 (oxygen) or mixed gas ($SF_6/O_2/HBr$ gas) containing SF_6, O_2 and HBr (hydrogen bromide), for example, is introduced into the surface 52 of the epitaxial layer 51 through the openings 78. Thus, the epitaxial layer 51 is dry-etched from the surface 52 (the Si surface), and the gate trench 43 and the source trench 45 are

formed at the same time. Further, the large number of unit cells **44** are formed on the epitaxial layer **51**.

Then, the mask **77** is removed by wet etching, as shown in FIG. **5**F.

Thereafter an organic material film **81** is formed on the overall region of the surface **52** of the epitaxial layer **51**, as shown in FIG. **5**G. The organic material film **81** is made of a material containing carbon, to which an organic material (polyimide or the like, for example) employed as a photoresist material or the like can be applied, for example. The organic material film **81** is formed with a spin coater or the like, for example.

After the formation of the organic material film **81**, the SiC substrate **42** is charged into a resistance heating furnace **82**. The resistance heating furnace **82** is not particularly restricted, so far as airtightness in the resistance heating furnace **82** in which a heated object is set can be ensured and gas can be introduced thereinto. Further, the heating system of the resistance heating furnace **82** may be either direct heating or indirect heating.

When the SiC substrate **42** is set in the resistance heating furnace **82**, inert gas (N_2, Ar or the like, for example) is introduced into the resistance heating furnace **82**, which in turn is subjected to temperature-rise control (first temperature-rise control).

In the first temperature-rise control, the heating temperature is controlled to rise from 100° C. to 1000° C. over 35 to 45 minutes, for example, and thereafter held at 1000° C. (first temperature holding) for 5 to 10 minutes, for example, as shown in FIG. **6**. Due to the temperature rise and the temperature holding, elements other than carbon evaporate from the organic material film **81**, which in turn is altered into a carbon film **83**, as shown in FIG. **5**H. Therefore, the overall region of the surface **52** of the epitaxial layer **51** is covered with the carbon film **83**.

Then, the resistance heating furnace **82** is subjected to further temperature-rise control (second temperature-rise control) while the inner portion thereof is kept in the inert atmosphere.

In the second temperature-rise control, the heating temperature is controlled to rise from 1000° C. to 1600° C. over 30 to 60 minutes, for example, as shown in FIG. **6**. After the temperature rise, the heating temperature is held at 1600° C. (second temperature holding) for 5 to 10 minutes, for example. Due to the temperature rise and the temperature holding, ions of the individual N- and P-type impurities implanted into a surface layer portion of the epitaxial layer **51** are activated, and the body region **53**, the source region **55** and the body contact region **56** are formed in response to the implanted portions respectively, as shown in FIG. **5**I. Further, the drain region **54** maintaining the state after the epitaxy is formed on a base layer portion of the epitaxial layer **51**.

Then, the resistance heating furnace **82** is subjected to temperature-drop control while the inner portion thereof is kept in the inert atmosphere.

In the temperature-drop control, the heating temperature is controlled (temperature-drop-controlled) to drop from 1600° C. to 1300° C. over 15 to 30 minutes, for example, as shown in FIG. **6**. After the temperature drop, nitrogen/oxygen-containing gas is introduced into the resistance heating furnace **82** for 5 to 10 minutes, for example, while the heating temperature is held at 1300° C. (third temperature holding). Due to the introduction of the nitrogen/oxygen-containing gas, the carbon film **83** is oxidized and removed by reacting with oxygen contained in the gas, as shown in FIG. **5**J. The introduced nitrogen/oxygen-containing gas can be prepared from gas containing at least N_2O (dinitrogen oxide), and may contain NO (nitrogen monoxide). The N_2O gas is fed at a flow rate of not more than 30%, preferably 1 to 30% with respect to the total flow rate of the introduced gas.

Thereafter the heating temperature is further held at 1300° C. (fourth temperature holding) for 200 to 240 minutes, for example, while the nitrogen/oxygen-containing gas is introduced into the resistance heating furnace **82** at the same flow rate. Thus, the surface **52** of the epitaxial layer **51** is oxidized, and a silicon oxynitride film (the gate insulating film **63**) covering the overall region of the surface **52** is formed, as shown in FIG. **5**K.

After the formation of the gate insulating film **63**, the inert gas (N_2, Ar or the like, for example) is reintroduced into the resistance heating furnace **82**, while the heating temperature is controlled to drop from 1300° C. to 300° C. After the temperature drop, the SiC substrate **42** is taken out from the resistance heating furnace **82**.

Then, a doped polysilicon material **84** is deposited from above the epitaxial layer **51** by CVD, as shown in FIG. **5**L. The polysilicon material **84** is continuously deposited until at least the gate trench **43** and the source trench **45** are filled up therewith.

Thereafter the deposited polysilicon material **84** is etched back until the etched-back surface is flush with the surface **52** of the epitaxial layer **51**, as shown in FIG. **5**M.

Then, only the portion of the polysilicon material **84** remaining in the source trench **45** is removed by dry etching, as shown in FIG. **5**N. Thus, the gate electrode **66** is formed by the polysilicon material **84** remaining in the gate trench **43**.

Then, the interlayer dielectric film **67** made of SiO_2 is laminated on the epitaxial layer **51** by CVD, as shown in FIG. **5**O.

Then, the interlayer dielectric film **67** and the gate insulating film **63** are continuously patterned, whereby the contact hole **68** is formed in the interlayer dielectric film **67** and the gate insulating film **63**, as shown in FIG. **5**P.

Then, a polysilicon material is deposited by CVD to fill up the contact hole **68**, as shown in FIG. **5**Q. Thereafter an N- or P-type impurity is implanted into the deposited polysilicon material. While the implantation conditions vary with the type of the N- or P-type impurity, acceleration energy is 10 to 100 keV, for example. Thereafter the impurity is diffused at a temperature of 900° C. for 20 minutes, for example. Thus, the polysilicon layer **70** doped with the impurity in a high concentration is formed. Then, Ti and TiN are deposited in this order on the surface of the polysilicon layer **70** by a method such as sputtering or vapor deposition, and the intermediate layer **71** is formed. Then, a metal such as Al is deposited on the surface of the intermediate layer **71** by a method such as sputtering or vapor deposition, and the metal layer **72** is formed. Thus, the source wire **69** is formed. Then, the drain electrode **74** is formed on the rear surface **50** of the SiC substrate **42**.

Thereafter the semiconductor device **41** shown in FIG. **4** is obtained by forming the interlayer dielectric film (not shown), the source pad **46** and the gate pad **48**.

In the semiconductor device **41**, as hereinabove described, the source wire **69** has the polysilicon layer **70** in the portion in contact with the source region **55** and the body contact region **56** similarly to the semiconductor device **1** according to the first embodiment, whereby the source wire **69** can be brought into ohmic contact with both of the body contact region **56** and the source region **55**, which are high-concentration impurity regions.

When the semiconductor device **41** is manufactured, therefore, a step of forming an Ni layer on the surface **52** of the epitaxial layer **51** can be omitted dissimilarly to a case where a layer made of only a metal such as Al is directly brought into contact with the impurity regions, and a step of silicifying such an Ni layer can also be omitted. Thus, the surface **52** of the epitaxial layer **51** can be prevented from formation of a carbon layer.

Consequently, layer peeling can be suppressed between the source wire **69** and the epitaxial layer **51**. Thus, connection reliability of the source wire **69** can be improved.

Further, the layer (the polysilicon layer **70**) entering the source trench **45** to come into contact with the drain region **54**, the body contact region **56** and the source region **55** is made of polysilicon excellent in coverage, whereby coverage of the source wire **69** can be improved. Consequently, the connection reliability of the source wire **69** can be further improved.

In addition, the polysilicon layer **70** is the high-concentration doped layer doped with the impurity in the high concentration of 10^{19} to 10^{21} cm^{-3}, whereby the resistance of the source wire **69** can be reduced.

Further, the intermediate layer **71** having the multilayer structure of the Ti layer and the TiN layer is interposed between the polysilicon layer **70** and the metal layer **72**. A material containing Ti has excellent adhesiveness with respect to both of a polysilicon material and a metal material. Therefore, adhesiveness between the polysilicon layer **70** and the metal layer **72** can be improved. Consequently, the connection reliability of the source wire **69** can be further improved.

In the semiconductor device **41**, the source trench **45** is formed at the center of each unit cell **44** surrounded by the gate trench **43**, whereby congestion of equipotential lines can be suppressed in the vicinity of both end corner portions **61** of the gate trench **43**. Consequently, the electric field applied to both end corner portions **61** on the bottom portion of the gate trench **43** can be relaxed, whereby the portion of the gate insulating film **63** located on the bottom surface **58** can be prevented from dielectric breakdown.

The source trench **45** may be deeper than the gate trench **43**, as in a semiconductor device **85** shown in FIG. **7**. Thus, the electric field applied to both end corner portions **61** on the bottom portion of the gate trench **43** can be further relaxed.

FIGS. **8**(a) and **8**(b) are schematic plan views of a semiconductor device according to a third embodiment of the present invention, with FIG. **8**(a) showing the overall semiconductor device and FIG. **8**(b) showing an inner portion thereof in an enlarged manner. Referring to FIGS. **8**(a) and **8**(b), portions corresponding to those shown in FIGS. **3**(a) and **3**(b) are denoted by the same reference numerals. In the following, redundant description on the portions denoted by the same reference numerals is omitted.

A semiconductor device **86** according to the third embodiment of the present invention is a planar gate power VDMOSFET (an individual device) employing SiC in the form of a chip square in plan view, for example. The chip-like semiconductor device **86** has a length of about several mm in the right-and-left (vertical) direction in the plane of FIG. **8**(a).

The semiconductor device **86** has an SiC substrate **42** and a large number of unit cells **88** formed on the SiC substrate **42** and partitioned by a gate electrode **87** latticed in plan view. In other words, the unit cells **88** in the form of squares in plan view arranged in window portions of the latticed gate electrode **87** respectively are aligned on the SiC substrate **42** in the form of a matrix. Each unit cell **88** has a length of not more than 10 μm the right-and-left (vertical) direction in the plane of FIG. **8**(b), for example, and a source wire **89** is connected to the center thereof from the surface side.

FIG. **9** is a schematic sectional view of the semiconductor device **86** according to the third embodiment of the present invention, taken along a line IX-IX in FIG. **8**(b). Referring to FIG. **9**, portions corresponding to those shown in FIG. **4** are denoted by the same reference numerals. In the following, redundant description on the portions denoted by the same reference numerals is omitted.

The sectional structure of the semiconductor device **86** is described with reference to FIG. **9**. The semiconductor device **86** includes the SiC substrate **41** of an N^+-type (having a concentration of 10^{18} to 10^{21} cm^{-3}, for example) and an epitaxial layer **51** laminated on the SiC substrate **42**.

A large number of well-shaped P-type body regions **90** are formed on the side of the epitaxial layer **51** closer to a surface **52** (an Si surface), with a concentration of 10^{16} to 10^{19} cm^{-3}, for example. A region of the epitaxial layer **51** closer to the side of the SiC substrate **42** (the side of a C surface) than each body region **90** is an N^--type drain region **91** (a drift region) maintaining a state after epitaxy.

An N^+-type source region **92** (having a concentration of 10^{18} to 10^{21} cm^{-3}, for example) and a P^+-type body contact region **93** (having a concentration of 10^{18} to 10^{21} cm^{-3}, for example) surrounded by the source region **92** are formed in each body region **90**.

The latticed gate electrode **87** is formed over the adjacent body regions **90**, and a gate insulating film **94** is interposed between the gate electrode **87** and the epitaxial layer **51**. The gate electrode **87** extends over the source region **92** and the drain region **91**, to control formation of an inversion layer (a channel) on the surface of the body region **90**. The gate insulating film **94** consists of an oxide film containing nitrogen, such as a silicon oxynitride film formed by thermal oxidation with gas containing nitride and oxygen, for example. The nitrogen content (the nitrogen concentration) in the gate insulating film **94** is 0.1 to 10%, for example.

An interlayer dielectric film **95** made of SiO_2 is laminated on the epitaxial layer **51**, to cover the gate electrode **87**. In the interlayer dielectric film **95** and the gate insulating film **63**, a contact hole **96** is formed in a central region of the body region **90**.

A source wire **89** is formed on the interlayer dielectric film **95**. The source wire **89** collectively enters every contact hole **96**, and is in contact with the drain region **91**, the body contact region **93** and the source region **92** in each unit cell **88**. In other words, the source wire **89** is common to all unit cells **88**. An interlayer dielectric film (not shown) is formed on the source wire **89**, which in turn is electrically connected to a source pad **46** (see FIG. **8**(a)) through the interlayer dielectric film (not shown). On the other hand, a gate pad **48** (see FIG. **8**(a)) is electrically connected to the gate electrode **87** through a gate wire (not shown) drawn onto the interlayer dielectric film (not shown).

The source wire **89** has a polysilicon layer **97**, an intermediate layer **98** and a metal layer **99** successively from the side in contact with the epitaxial layer **51**.

The polysilicon layer **97** is a doped layer made of doped polysilicon doped with an impurity, such as a high-concentration doped layer doped with the impurity in a high concentration of 10^{19} to 10^{21} cm^{-3}, for example. The impurity for forming the polysilicon layer **97** as the doped layer (including the high-concentration doped layer) can be prepared from an N-type impurity such as N (nitrogen), P (phosphorus) or As (arsenic) or a P-type impurity such as Al

(aluminum) or B (boron). The thickness of the polysilicon layer **97** is 5000 to 10000 Å, for example.

According to the third embodiment, the polysilicon layer **97** is formed to cover the overall region of the surface of each unit cell **88** exposed in the contact hole **96**, and in contact with the body contact region **93** and the source region **92**.

The layer of the source wire **89** in contact with the body contact region **93** and the source region **92** is so made of polysilicon that the source wire **89** can be brought into ohmic contact with both of the body contact region **93** and the source region **92**, which are high-concentration impurity regions.

The intermediate layer **98**, laminated on the polysilicon layer **97**, is formed by a single layer containing Ti (titanium) or a plurality of layers including the layer. The layer containing Ti can be prepared from Ti, TiN (titanium nitride) or the like. The thickness of the intermediate layer **98** is 200 to 500 nm, for example.

The metal layer **99**, laminated on the intermediate layer **98**, is made of Al (aluminum), Au (gold), Ag (silver), Cu (copper) or Mo (molybdenum), an alloy thereof, or a metal material containing the same, for example. The metal layer **99** forms the outermost layer of the source wire **98**. The thickness of the metal layer **99** is 1 to 5 μm, for example.

More specifically, the polysilicon layer **97**, the intermediate layer **98** and the metal layer **99** may be combined in a multilayer structure (Poly-Si/Ti/TiN/Al) obtained by successively laminating Poly-Si (the polysilicon layer **97**), Ti (the intermediate layer **98**), TiN (the intermediate layer **98**) and Al (the metal layer **99**).

A drain electrode **74** is formed on a rear surface **50** of the SiC substrate **42**, to cover the overall region thereof.

A prescribed voltage (a voltage of not less than a gate threshold voltage) is applied to the gate pad **48** while a prescribed potential difference is caused between the source pad **46** (the source wire **89**) and the drain electrode **74** (between a source and a drain), whereby a channel is formed in the vicinity of the interface between the body region **90** and the gate insulating film **63** due to an electric field from the gate electrode **87**. Thus, a current flows between the source wire **89** and the drain electrode **74**, and the VDMOSFET is turned on.

FIGS. **10**A to **10**N are schematic sectional views for illustrating a method of manufacturing the semiconductor device **86** shown in FIG. **9** in step order. Referring to FIGS. **10**A to **10**N, portions corresponding to those shown in FIGS. **5**A to **5**Q are denoted by the same reference numerals. In the following, redundant description on the portions denoted by the same reference numerals is omitted.

First, an SiC crystal is grown on a surface **49** (an Si surface) of the SiC substrate **42** by epitaxy such as CVD (Chemical Vapor Deposition), LPE (Liquid Phase Epitaxy) or MBE (Molecular Beam Epitaxy) while doping the same with an impurity, as shown in FIG. **10**A. Thus, the N^--type epitaxial layer **51** is formed on the SiC substrate **42**.

Then, a mask **39** made of SiO_2 is formed on the epitaxial layer **51** by CVD, as shown in FIG. **10**B. Then, the mask **39** is etched through a photoresist film (not shown) into a pattern having an opening in a region for forming the body region **90**. After the formation of the opening, a P-type impurity is implanted into the epitaxial layer **51** from the surface **52** thereof. While the implantation conditions vary with the type of the P-type impurity, acceleration energy is 200 to 3000 keV, for example. After the implantation of the P-type impurity, the mask **39** is removed.

Then, a mask **40** made of SiO_2 is formed on the epitaxial layer **51** by CVD, as shown in FIG. **10**C. Then, the mask **40** is etched through a photoresist film (not shown) into a pattern having an opening in a region for forming the source region **92**. After the formation of the opening, an N-type impurity is implanted into the epitaxial layer **51** from the surface **52** thereof. While the implantation conditions vary with the type of the N-type impurity, acceleration energy is 30 to 400 keV, for example. After the implantation of the N-type impurity, the mask **40** is removed.

Then, a mask **62** made of SiO_2 is formed on the epitaxial layer **51** by CVD, as shown in FIG. **10**D. Then, the mask **62** is etched through a photoresist film (not shown) into a pattern having an opening in a region for forming the body contact region **93**. After the formation of the opening, a P-type impurity is implanted into the epitaxial layer **51** from the surface **52** thereof. While the implantation conditions vary with the type of the P-type impurity, acceleration energy is 30 to 400 keV, for example. After the implantation of the P-type impurity, the mask **62** is removed.

Thereafter an organic material film **81** is formed on the overall region of the surface **52** of the epitaxial layer **51**, as shown in FIG. **10**E.

After the formation of the organic material film **81**, the SiC substrate **42** is charged into a resistance heating furnace **82**. When the SiC substrate **42** is set in the resistance heating furnace **82**, inert gas (N_2, Ar or the like, for example) is introduced into the resistance heating furnace **82**, which in turn is subjected to temperature-rise control (first temperature-rise control), similarly to the step shown in FIG. **5**H (see FIG. **6**). Due to the temperature rise and temperature holding, elements other than carbon evaporate from the organic material film **81**, which in turn is altered into a carbon film **83**, as shown in FIG. **10**F.

Then, the resistance heating furnace **82** is subjected to further temperature-rise control (second temperature-rise control) while the inner portion thereof is kept in the inert atmosphere, similarly to the step shown in FIG. **5**I (see FIG. **6**). Due to the temperature rise and temperature holding, ions of the individual N- and P-type impurities implanted into a surface layer portion of the epitaxial layer **51** are activated, and the body region **90**, the source region **92** and the body contact region **93** are formed in response to the implanted portions respectively, as shown in FIG. **10**G. Further, the drain region **91** maintaining the state after the epitaxy is formed on a base layer portion of the epitaxial layer **51**.

Then, the resistance heating furnace **82** is subjected to temperature-drop control while the inner portion thereof is kept in the inert atmosphere, similarly to the step shown in FIG. **5**J (see FIG. **6**). Due to the temperature-drop control introducing nitrogen/oxygen-containing gas, the carbon film **83** is oxidized and removed by reacting with oxygen contained in the gas, as shown in FIG. **10**H.

Thereafter the heating temperature is further held at 1300° C. (fourth temperature holding) for 200 to 240 minutes, for example, while the nitrogen/oxygen-containing gas is introduced into the resistance heating furnace **82** at the same flow rate (see FIG. **6**). Thus, the surface **52** of the epitaxial layer **51** is oxidized, and a silicon oxynitride film (the gate insulating film **94**) covering the overall region of the surface **52** is formed, as shown in FIG. **10**I.

After the formation of the gate insulating film **94**, the inert gas (N_2, Ar or the like, for example) is reintroduced into the resistance heating furnace **82**, while the heating temperature is controlled to drop from 1300° C. to 300° C. After the temperature drop, the SiC substrate **42** is taken out from the resistance heating furnace **82**.

Then, a doped polysilicon material **84** is deposited from above the epitaxial layer **51** by CVD, as shown in FIG. **10**J.

Thereafter the deposited polysilicon material **84** is removed by dry etching, as shown in FIG. **10**K. Thus, the gate electrode **87** is formed.

Then, the interlayer dielectric film **95** made of SiO_2 is laminated on the epitaxial layer **51** by CVD, as shown in FIG. **10**L.

Then, the interlayer dielectric film **95** and the gate insulating film **94** are continuously patterned so that the contact hole **96** is formed in the interlayer dielectric film **95** and the gate insulating film **94**, as shown in FIG. **10**M.

Then, a polysilicon material is deposited by CVD to fill up the contact hole **96**, as shown in FIG. **10**N. Thereafter an N- or P-type impurity is implanted into the deposited polysilicon material. While the implantation conditions vary with the type of the N- or P-type impurity, acceleration energy is 10 to 100 keV, for example. Thus, the polysilicon layer **97** doped with the impurity in a high concentration is formed. Then, Ti and TiN are deposited in this order on the surface of the polysilicon layer **97** by a method such as sputtering or vapor deposition, and the intermediate layer **98** is formed. Then, a metal such as Al is deposited on the surface of the intermediate layer **98** by a method such as sputtering or vapor deposition, and the metal layer **99** is formed. Thus, the source wire **89** is formed. Then, the drain electrode **74** is formed on the rear surface **50** of the SiC substrate **42**.

Thereafter the semiconductor device **86** shown in FIG. **9** is obtained by forming the interlayer dielectric film (not shown), the source pad **46** and the gate pad **48**.

In the semiconductor device **86**, as hereinabove described, the source wire **89** has the polysilicon layer **97** in the portion in contact with the source region **92** and the body contact region **93**, whereby the source wire **89** can be brought into ohmic contact with both of the body contact region **93** and the source region **92**, which are high-concentration impurity regions, similarly to the semiconductor device **1** according to the first embodiment.

When the semiconductor device **86** is manufactured, therefore, a step of forming an Ni layer on the surface **52** of the epitaxial layer **51** can be omitted dissimilarly to a case where a layer made of only a metal such as Al is directly brought into contact with the impurity regions, and a step of silicifying such an Ni layer can also be omitted. Thus, the surface **52** of the epitaxial layer **51** can be prevented from formation of a carbon layer.

Consequently, layer peeling can be suppressed between the source wire **89** and the epitaxial layer **51**. Thus, connection reliability of the source wire **89** can be improved.

Further, the layer (the polysilicon layer **97**) entering the contact hole **96** to come into contact with the drain region **91**, the body contact region **93** and the source region **92** is made of polysilicon excellent in coverage, whereby coverage of the source wire **89** can be improved. Consequently, the connection reliability of the source wire **89** can be further improved.

In addition, the polysilicon layer **97** is the high-concentration doped layer doped with the impurity in the high concentration of 10^{19} to 10^{21} cm^{-3}, whereby the resistance of the source wire **89** can be reduced.

Further, the intermediate layer **98** having the multilayer structure of the Ti layer and the TiN layer is interposed between the polysilicon layer **97** and the metal layer **99**. A material containing Ti has excellent adhesiveness with respect to both of a polysilicon material and a metal material. Therefore, adhesiveness between the polysilicon layer **97** and the metal layer **99** can be improved. Consequently, the connection reliability of the source wire **89** can be further improved.

When the body contact region **93** is formed on a side (a lower portion) closer to the SiC substrate **42** than the source region **92** and a source trench **79** is formed to pass through each body contact region **56** as shown in FIG. **11** similarly to the second embodiment, the polysilicon layer **97** can be brought into contact with the drain region **91**, the body contact region **93** and the source region **92** in the source trench **79**. In other words, a current can be fed to the side of a hetero junction in preference to the side of a body diode **80** (a PN diode formed by junction between the body region **90** and the drain region **91**), even if a reverse voltage is applied between the source and the drain and the current flows to the body diode **80**.

An embodiment related to the invention of a method of manufacturing an SiC semiconductor device through a resistance heating furnace is now described.

FIG. **12** is a schematic sectional view of a planar gate semiconductor device.

A semiconductor device **101** has a structure obtained by arranging a plurality of unit cells of a planar gate VDMOSFET in the form of a matrix. FIG. **12** shows only part of the plurality of unit cells.

The semiconductor device **101** includes an N^+-type SiC substrate **102** forming the base of the semiconductor device **101**. An N^--type epitaxial layer **103** made of SiC (silicon carbide) doped with an N-type impurity in a lower concentration than the SiC substrate **102** is laminated on a surface **121** of the SiC substrate **102**. A surface **131** of the epitaxial layer **103** is constituted of a (0001) plane of SiC, for example.

An N^--type drain region **104** maintaining a state after epitaxy is formed on the epitaxial layer **103**.

A P-type body region **105** is formed on a surface layer portion of the epitaxial layer **103**. A plurality of such body regions **105** (not shown in FIG. **12**) are formed at regular intervals to parallelly extend in the same direction (a direction perpendicular to the plane of FIG. **12**), and arranged in a striped manner or in the form of a matrix, for example. The drain region **104** is exposed between two body regions **105** adjacent to each other.

On a surface layer portion of the body region **105**, an N^+-type source region **106** is formed at an interval from the peripheral edge thereof.

A gate insulating film **107** extending over the drain region **104**, the body region **105** and the source region **106** is formed on the surface **131** of the epitaxial layer **103**. The gate insulating film **107** is made of SiO_2.

A gate electrode **108** made of polysilicon doped with an N-type impurity in a high concentration is formed on the gate insulating film **107**. The gate electrode **108** is opposed to the drain region **104**, the body region **105** and the source region **106** through the gate insulating film **107**.

An interlayer dielectric film **109** made of SiO_2 is laminated on the epitaxial layer **103**. A source wire **111** is formed on the interlayer dielectric film **109**. The source wire **111** is electrically connected to the body region **105** and the source region **106** through a contact hole **110** formed in the interlayer dielectric film **109**.

A gate wire **112** is electrically connected to the gate electrode **108** through a contact hole (not shown) formed in the interlayer dielectric film **109**.

A drain electrode **113** is formed on the rear surface of the SiC substrate **102**.

When the source wire **111** is grounded and the potential of the gate electrode **108** is controlled while applying a positive voltage of a proper level to the drain electrode **113**, a channel can be formed in the vicinity of the interface between the body region **105** and the gate insulating film **107** due to an electric field from the gate electrode **108**. Thus, a current can be fed between the source wire **111** and the drain electrode **113**.

FIGS. **13**A to **13**L are schematic sectional views for illustrating a method of manufacturing the semiconductor device **101** shown in FIG. **12** in step order.

First, the epitaxial layer **103** is formed on the surface **121** of the SiC substrate **102** by epitaxy, as shown in FIG. **13**A. At this time, a major growth surface (the surface **121**) of the SiC substrate **102** is defined by a (0001) plane. Due to the surface **121** of the SiC substrate **102** defined by the (0001) plane, the epitaxial layer **103** formed on the SiC substrate **102** by epitaxy is grown also with a major surface defined by a (0001) plane. Therefore, the surface **131** of the epitaxial layer **103** parallel to the surface **121** of the SiC substrate **102** is defined by the (0001) plane.

Then, a photoresist film **114** having an opening **115** in a portion opposed to a region for forming the body region **105** is formed on the surface **131** of the epitaxial layer **103** by well-known photolithography. Then, ions (boron ions, for example) of a P-type impurity are introduced into the surface **131** of the epitaxial layer **103** from above the photoresist film **114**. Thus, the P-type impurity is implanted into surface layer portions of portions of the epitaxial layer **103** exposed from the opening **115**, as shown in FIG. **13**B.

Then, a photoresist film **116** having an opening **117** in a portion opposed to a region for forming the source region **106** is formed on the surface **131** of the epitaxial layer **103** by well-known photolithography. Then, ions (arsenic ions, for example) of an N-type impurity are introduced into the surface **131** of the epitaxial layer **103** from above the photoresist film **116**. Thus, the N-type impurity is implanted into a surface layer portion (closer to the surface **131** than the portions into which the P-type impurity has been implanted) of a portion of the epitaxial layer **103** exposed from the opening **117**, as shown in FIG. **13**C.

After the implantation of the impurity ions into the surface layer portion of the epitaxial layer **103**, an organic material film **118** is formed on the overall region of the surface **131** of the epitaxial layer **103**, as shown in FIG. **13**D. The organic material film **118** is made of a material containing carbon, to which an organic material (polyimide or the like, for example) employed as a photoresist material or the like can be applied, for example. The organic material film **118** is formed with a spin coater or the like, for example.

After the formation of the organic material film **118**, the SiC substrate **102** is charged into a resistance heating furnace **122**. The resistance heating furnace **122** is not particularly restricted, so far as airtightness in the resistance heating furnace **122** in which a heated object is set can be ensured and gas can be introduced thereinto. Further, the heating system of the resistance heating furnace **122** may be either direct heating or indirect heating.

When the SiC substrate **102** is set in the resistance heating furnace **122**, inert gas (N_2, Ar or the like, for example) is introduced into the resistance heating furnace **122**, which in turn is subjected to temperature-rise control (first temperature-rise control).

In the first temperature-rise control, the heating temperature is controlled to rise from 100° C. to 1000° C. over 35 to 45 minutes, for example, and thereafter held at 1000° C. (first temperature holding) for 5 to 10 minutes, for example, as shown in FIG. **6**. Due to the temperature rise and the temperature holding, elements other than carbon evaporate from the organic material film **118**, which in turn is altered into a carbon film **119**, as shown in FIG. **13**E. Therefore, the overall region of the surface **131** of the epitaxial layer **103** is covered with the carbon film **119**.

Then, the resistance heating furnace **122** is subjected to further temperature-rise control (second temperature-rise control) while the inner portion thereof is kept in the inert atmosphere.

In the second temperature-rise control, the heating temperature is controlled to rise from 1000° C. to 1600° C. over 30 to 60 minutes, for example, as shown in FIG. **6**. After the temperature rise, the heating temperature is held at 1600° C. (second temperature holding) for 5 to 10 minutes, for example. Due to the temperature rise and the temperature holding, ions of the N- and P-type impurities implanted into the surface layer portion of the epitaxial layer **103** are activated, and the body region **105** and the source region **106** are formed on the surface layer portion of the epitaxial layer **103**, as shown in FIG. **13**F. Further, the drain region **104** isolated from the body region **105** while maintaining the state after the epitaxy is formed on a base layer portion of the epitaxial layer **103**.

Then, the resistance heating furnace **122** is subjected to temperature-drop control while the inner portion thereof is kept in the inert atmosphere.

In the temperature-drop control, the heating temperature is controlled (temperature-drop-controlled) to drop from 1600° C. to 1300° C. over 15 to 30 minutes, for example, as shown in FIG. **6**. After the temperature drop, oxygen-containing gas is introduced into the resistance heating furnace **122** for 5 to 10 minutes, for example, while holding the heating temperature at 1300° C. (third temperature holding). Due to the introduction of the oxygen-containing gas, the carbon film **119** is oxidized and removed by reacting with oxygen contained in the oxygen-containing gas, as shown in FIG. **13**G. The oxygen-containing gas introduced into the resistance heating furnace **122** is preferably prepared from gas containing oxygen and nitrogen. More specifically, gas containing NO (nitrogen monoxide) or N_2O (dinitrogen oxide) can be employed.

Thereafter the heating temperature is further held at 1300° C. (fourth temperature holding) for 200 to 240 minutes, for example, while the oxygen-containing gas is introduced into the resistance heating furnace **122**. Thus, the surface **131** of the epitaxial layer **103** is oxidized, and an oxide film **120** covering the overall region of the surface **131** is formed, as shown in FIG. **13**H.

After the formation of the oxide film **120**, the inert gas (N_2, Ar or the like, for example) is reintroduced into the resistance heating furnace **122**, while the heating temperature is controlled to drop from 1300° C. to 300° C. After the temperature drop, the SiC substrate **102** is taken out from the resistance heating furnace **122**.

Then, a conductive material film is formed by sputtering. Then, the conductive material film is patterned by well-known photolithography and etching, and the gate electrode **108** is formed on the oxide film **120**, as shown in FIG. **13**I.

Thereafter the interlayer dielectric film **109** is laminated on the epitaxial layer **103** by CVD (Chemical Vapor Deposition), as shown in FIG. **13**J.

Then, the contact hole **110** is formed in the interlayer dielectric film **109** and the oxide film **120** by well-known photolithography and etching, as shown in FIG. **13**K. The remaining portion of the oxide film **120** forms the gate insulating film **107**.

Then, a film of a conductive material is formed on the epitaxial layer **103** by sputtering. The conductive material is bonded (deposited) to fill up the contact hole **110** and form a thin film on the interlayer dielectric film **109**. Then, the conductive material film formed on the interlayer dielectric film **109** is patterned by well-known photolithography and etching. Thus, the source wire **111** is formed, as shown in FIG. **13**L. Further, the gate wire **112** electrically connected with the gate electrode **108** is formed. In addition, the drain electrode **113** is formed on the rear surface of the SiC substrate **102**.

The semiconductor device **101** shown in FIG. **12** is obtained through the aforementioned steps.

According to the aforementioned method, the organic material film **118** is heated in the resistance heating furnace **122** by the first temperature-rise control after the formation of the organic material film **118** to be altered into the carbon film **119**, which is formed on the surface **131** of the epitaxial layer **103**.

After the formation of the carbon film **119**, the epitaxial layer **103** is heated due to the second temperature-rise control in the resistance heating furnace **122** while the inner portion thereof is kept in the inert atmosphere, thereby activating the ions of the N- and P-type impurities in the epitaxial layer **103**.

Then, the temperature-drop control (temperature drop from 1600° C. to 1300° C., for example) is executed while maintaining the resistance heating furnace **122** in the inert state. Thereafter the oxygen-containing gas is introduced for 5 to 10 minutes, for example, while the heating temperature is held at 1300° C. (the third temperature holding). Thus, the carbon film **119** is oxidized and removed, and the surface **131** of the epitaxial layer **103** is exposed.

After the removal of the carbon film **119**, the resistance heating furnace **122** is subjected to the temperature holding (the fourth temperature holding) while the oxygen-containing gas is continuously introduced thereinto, whereby the exposed surface **131** is oxidized and the oxide film **120** is formed.

The carbon film **119** is formed on the surface **131** of the epitaxial layer **103** in advance of the heating (the second temperature-rise control) for activating the ions, whereby Si escape from the surface **131** can be prevented when the epitaxial layer **103** is heated. Therefore, roughening of the surface **131** of the epitaxial layer **103** can be suppressed, and planarity of the surface **131** can be maintained. Consequently, the interface between the epitaxial layer **103** and the gate insulating film **107** can be smoothed, whereby channel mobility of the semiconductor device **101** can be improved.

Further, the four steps of altering the organic material film **118** into the carbon film **119** by heating the same (the first temperature-rise control), activating the ions by heating the epitaxial layer **103** (the second temperature-rise control), oxidizing and removing the carbon film **119** with the oxygen-containing gas (the temperature-drop control and the third temperature holding) and forming the oxide film **120** by oxidizing the surface **131** of the epitaxial layer **103** (the fourth temperature holding) can be continuously carried out in the single resistance heating furnace **122**. No apparatus for removing the carbon film **119** or the like is additionally required, whereby increase in the device cost can also be suppressed. Further, the resistance heating furnace **122** is so employed that the first temperature-rise control, the second temperature-rise control, the temperature-drop control as well as the third temperature holding, and the fourth temperature holding can be precisely and simply executed.

In addition, the surface **131** of the epitaxial layer **103** on which the oxide film **120** is formed is defined by the (0001) plane, and the oxygen-containing gas introduced into the resistance heating furnace **122** is prepared from the gas containing oxygen and nitrogen.

When oxide films are formed by oxidizing (0001) planes of SiC layers with O_2 gas, H_2O gas (water vapor) and N_2O gas respectively, for example, MOSFETS including the SiC layers exhibit channel mobility values of 1 to 5 $cm^2/V·s$, 5 to 15 $cm^2/V·s$ and 15 to 25 $cm^2/V·s$ respectively, for example. In other words, the MOSFET including the SiC layer having the oxide film formed with the N_2O gas is most excellent in channel mobility.

In the semiconductor device **101** according to the embodiment, the oxide film **120** is formed by oxidizing the (0001) plane (the surface **131**) of the epitaxial layer **103** with NO gas or N_2O gas, whereby the channel mobility of the semiconductor device **101** can be further improved.

EXAMPLES

While the present invention is now described with reference to Example and comparative example, the present invention is not restricted by the following Examples.

Example 1

First, an epitaxial layer made of SiC was formed by growing an SiC crystal on an Si surface of a wafer-shaped SiC substrate (by Cree Inc.). Then, an N-type impurity was multistage-implanted from the surface (the Si surface) of the epitaxial layer with acceleration energy of 30 to 200 keV. Thus, an N-type impurity region (having a concentration of 10^{20} cm^{-3}) was formed on a surface layer portion of the epitaxial layer.

Then, an insulating film made of SiO_2 was formed on the surface of the epitaxial layer by CVD. Then, a contact hole was formed in the insulating film, to expose the aforementioned impurity region.

Then, a contact wire was obtained by forming a polysilicon layer by depositing a polysilicon material in the contact hole by CVD.

Comparative Example 1

Steps similar to those in Example 1 were carried out up to a step of forming a contact hole. After the formation of the contact hole, nickel was deposited in the contact hole by sputtering. Then, a nickel silicide layer was obtained by silicifying nickel through a heat treatment at a temperature of 1000° C. Finally, a contact wire was obtained by forming an aluminum layer by depositing aluminum on the nickel silicide layer by sputtering.

1) Photography with Scanning Electron Microscope (SEM)

The contact wires formed according to Example 1 and comparative example 1 were scanned with electron beams through a scanning electron microscope. SEM images were obtained by image-processing information detected by the scanning with the electron beams. FIGS. **14**(a) and **14**(b) show the SEM images obtained according to Example 1 and comparative example 1 respectively.

2) Presence or Absence of Layer Peeling

The presence or absence of layer peeling in the contact wires was confirmed by visually recognizing the SEM images shown in FIGS. **14**(a) and **14**(b).

Referring to FIG. **14**(a), the polysilicon layer was in close contact with the impurity region, and it was confirmable that

the polysilicon layer was excellently in contact with the impurity region. Thus, it has been confirmed that connection reliability of the contact wire can be improved while forming ohmic contact between the contact wire and the impurity region according to Example 1.

Referring to FIG. **14**(b), on the other hand, a void was formed between the nickel silicide layer and the impurity region, and layer peeling was clearly confirmed therebetween. In other words, a contact failure was confirmed between the contact wire and the impurity region.

While the embodiments of the present invention have been described, the present invention may be embodied in other ways.

For example, the conductivity types of the semiconductor portions of the semiconductor device **1**, **41**, **85** or **86** may be reversed. In other words, the P-type portions may be replaced with N-type portions and vice versa in the semiconductor device **1**, **41**, **85** or **86**.

In the semiconductor device **1**, only either the source wire **17** or the drain wire **23** may be employed as the contact wire having the polysilicon layer.

In the semiconductor device **41**, **85** or **86**, the contact wire having the polysilicon layer may be applied to the drain electrode **74**.

The crystal planes of the surface **21** or **49** and the rear surface **22** or **50** of the SiC substrate **2** or **42** may be reversed. In other words, the surface **21** or **49** may be a C surface and the rear surface **22** or **50** may be an Si surface in the SiC substrate **2** or **42**.

While the contact wire according to the present invention has been shown as the source wire **17** or **69** and the drain wire **23** of the trench gate MOSFET or the source wire **89** of the planar gate VDMOSFET in each of the aforementioned embodiments, the present invention is also applicable to a wire brought into contact with an impurity region of a diode, a thyristor or a bipolar transistor, for example.

While the present invention has been described in detail by way of the embodiments thereof, it should be understood that these embodiments are merely illustrative of the technical principles of the present invention but not limitative of the invention. The spirit and scope of the present invention are to be limited only by the appended claims.

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor layer made of SiC;

a source region of a first conductivity type formed in the semiconductor layer, the source region forming a surface of the semiconductor layer;

a body region of a second conductivity type formed in the semiconductor layer, the body region being in contact with the source region from a side of a back surface of the semiconductor layer;

a drain region of a first conductivity type formed in the semiconductor layer, the drain region being in contact with the body region from the side of the back surface of the semiconductor layer;

a gate trench dug down in the semiconductor layer from the surface thereof, the gate trench passing through the source region and the body region **[**and the deepest portion thereof reaching**]** *to reach* the drain region;

a gate insulating film formed on an inner surface of the gate trench;

a gate electrode embedded in the gate trench on the gate insulating film;

a source trench dug down in the semiconductor layer from the surface thereof, the source trench passing through the source region and the body region**[**, and the deepest portion thereof reaching**]** *to reach* a first conductivity type part of the drain region; and

a conductive material embedded in the source trench, the conductive material having a first layer conforming to a side surface and a bottom surface of the source trench and a second layer formed on the first layer;

wherein the body region includes a first portion exposed from a side surface of the gate trench and a second portion exposed from the side surface of the source trench,

wherein a high-concentration impurity region is formed in the second portion of the body region and is in contact with the drain region,

wherein the second layer includes at least a lower layer conforming to the first layer to define a space inside the source trench, and an upper layer embedded in the space,

wherein an ohmic contact is selectively formed between the first layer and a high-concentration impurity region of the body region in an ohmic contact area,

wherein a non-ohmic contact is selectively formed between the first layer and the drain region in a non-ohmic contact area, and

wherein the ohmic contact area and the non-ohmic contact area are adjacent.

[2. The semiconductor device according to claim **1**, wherein the source trench passes through the source region and the body region and the deepest portion thereof reaches the drain region.**]**

[3. The semiconductor device according to claim **1**, wherein an ohmic contact is selectively formed between the first layer and the semiconductor layer.**]**

[4. The semiconductor device according to claim **1**, wherein an non-ohmic contact is selectively formed between the first layer and the semiconductor layer.**]**

5. The semiconductor device according to claim **1**, wherein the upper layer includes a surface layer made of Al.

6. The semiconductor device according to claim **5**, wherein the lower layer includes an intermediate layer between the first and surface layers.

7. The semiconductor device according to claim **6**, wherein the intermediate layer contains Ti.

8. The semiconductor device according to claim **6**, wherein the intermediate layer contains TiN.

9. The semiconductor device according to claim **6**, wherein the intermediate layer has a laminating structure of Ti and TiN.

10. The semiconductor device according to claim **1**, the gate trench and the source trench have the same depth.

11. The semiconductor device according to claim **1**, wherein the source trench is deeper than the gate trench.

12. The semiconductor device according to claim **1**, wherein

the source region is an n^+-type source region,

the drain region is an n-type drain region, and

the body region has a p-type region forming **[**a**]** *the* side surface of the gate trench, and a p^+-type region forming the side surface of the source trench and having an impurity concentration larger than that of the p-type region.

13. The semiconductor device according to claim **12**, wherein an ohmic contact is selectively formed between the first layer and the n^+-type source region.

14. The semiconductor device according to claim **1**, wherein the first layer is made of polysilicon.

15. The semiconductor device according to claim **1**, wherein the gate trench is formed to surround the source trench in plan view.

16. A semiconductor device, comprising:

a semiconductor layer made of SiC;

a source region formed in the semiconductor layer, the source region forming a surface of the semiconductor layer;

a body region formed in the semiconductor layer, the body region being in contact with the source region from a side of a back surface of the semiconductor layer;

a drain region formed in the semiconductor layer, the drain region being in contact with the body region from the side of the back surface of the semiconductor layer;

a gate trench dug down in the semiconductor layer from the surface thereof, the gate trench passing through the source region and the body region [and the deepest portion thereof] *to reach* the drain region;

a gate insulating film formed on an inner surface of the gate trench;

a gate electrode embedded in the gate trench on the gate insulating film;

a source trench dug down in the semiconductor layer from the surface thereof*, the source trench passing through the source region and the body region to reach the drain region*; and

a conductive material embedded in the source trench, the conductive material having a first layer conforming to a side surface and a bottom surface of the source trench and a second layer formed on the first layer;

wherein the body region includes a first portion exposed from a side surface of the gate trench and a second portion exposed from the side surface of the source trench,

wherein a high-concentration impurity region is formed in the second portion of the body region and is in contact with the drain region,

wherein the first layer selectively forms an ohmic contact and a first junction with respect to the semiconductor layer, the first junction having a smaller junction barrier than the diffusion potential of a body diode [intrinsic in the semiconductor device] *which is a PN diode formed by junction between the body region and the drain region*, [and]

wherein the second layer includes at least a lower layer conforming to the first layer to define a space inside the source trench, and an upper layer embedded in the space*,*

wherein the ohmic contact is selectively formed between the first layer and the high-concentration impurity region of the body region in an ohmic contact area,

wherein a non-ohmic contact is selectively formed between the first layer and the drain region in a non-ohmic contact area, and

wherein the ohmic contact area and the non-ohmic contact area are adjacent.

17. The semiconductor device according to claim **16**, wherein the source trench passes through the source region and the body region [and the deepest portion thereof reaches] *to reach* the drain region.

[**18**. The semiconductor device according to claim **16**, wherein a non-ohmic contact is selectively formed between the conductive material and the semiconductor layer.]

19. The semiconductor device according to claim **16**, the gate trench and the source trench have the same depth.

20. The semiconductor device according to claim **16**, wherein the source trench is deeper than the gate trench.

21. The semiconductor device according to claim **16**, wherein

the source region is an n^+-type source region,

the drain region is an n-type drain region, and

the body region has a p-type region forming a side surface of the gate trench, and a p^+-type region forming the side surface of the source trench and having an impurity concentration larger than that of the p-type region.

22. The semiconductor device according to claim **21**, wherein an ohmic contact is selectively formed between the conductive material and the n^+-type source region.

23. The semiconductor device according to claim **16**, wherein the gate trench is formed to surround the source trench in plan view.

24. The semiconductor device according to claim 1, wherein the non-ohmic contact is a heterojunction.

25. The semiconductor device according to claim 16, wherein the non-ohmic contact is a heterojunction.

* * * * *