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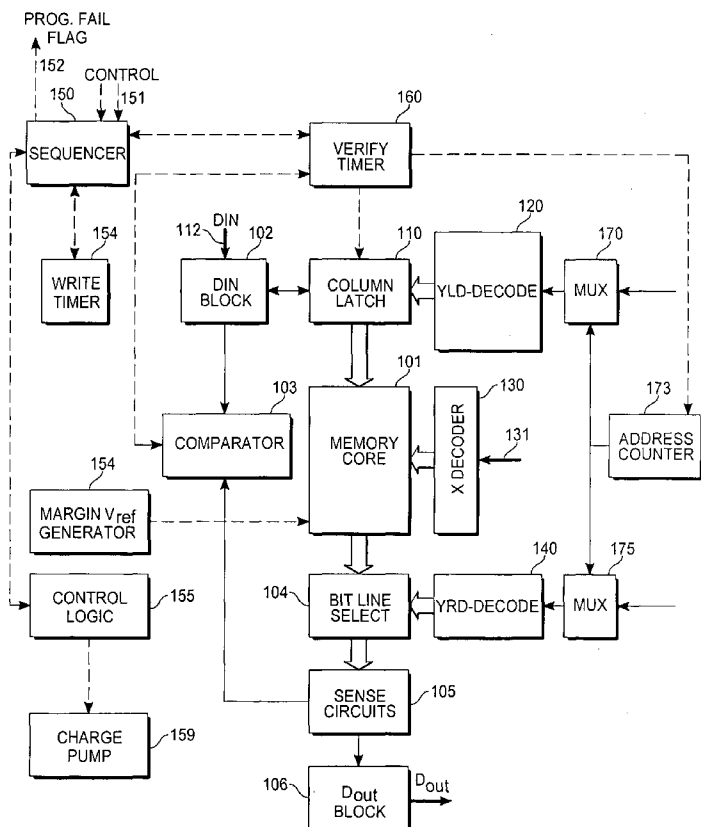
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Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) Title: SELF-ADAPTIVE PROGRAM DELAY CIRCUITRY FOR PROGRAMMABLE MEMORIES



(57) Abstract: A self-adaptive programming circuit (150, 160, 173, 170, 175, 154, 103) for EEPROM (Fig. 2) is used to automatically tune an erase or write delay, providing an improved programming window. The programming circuit may also provide improvements in data retention for programmed memory cells. The invention can be applied more particularly in the field of EEPROM memories capable of page mode writing operations.

WO 2006/023146 A3



— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/24187

A. CLASSIFICATION OF SUBJECT MATTER

IPC: G11C 7/06(2006.01)

USPC: 365/189.07,230.06,189.09,185.2,189.05,239

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/189.07, 230.06, 189.09, 185.2, 189.05, 239

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,829,181 B1 (SEITOH) 7 DECEMBER 2004	1-19
A	US 6,418,054 B1 (HOLLMER) 9 JULY 2002	1-19
A	US 6,191,976 B1 (SMAYLING ET AL.) 20 FEBRUARY 2001	1-19
A	US 5,537,358 (FONG) 16 JULY 1996	1-19

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