

Jan. 14, 1964

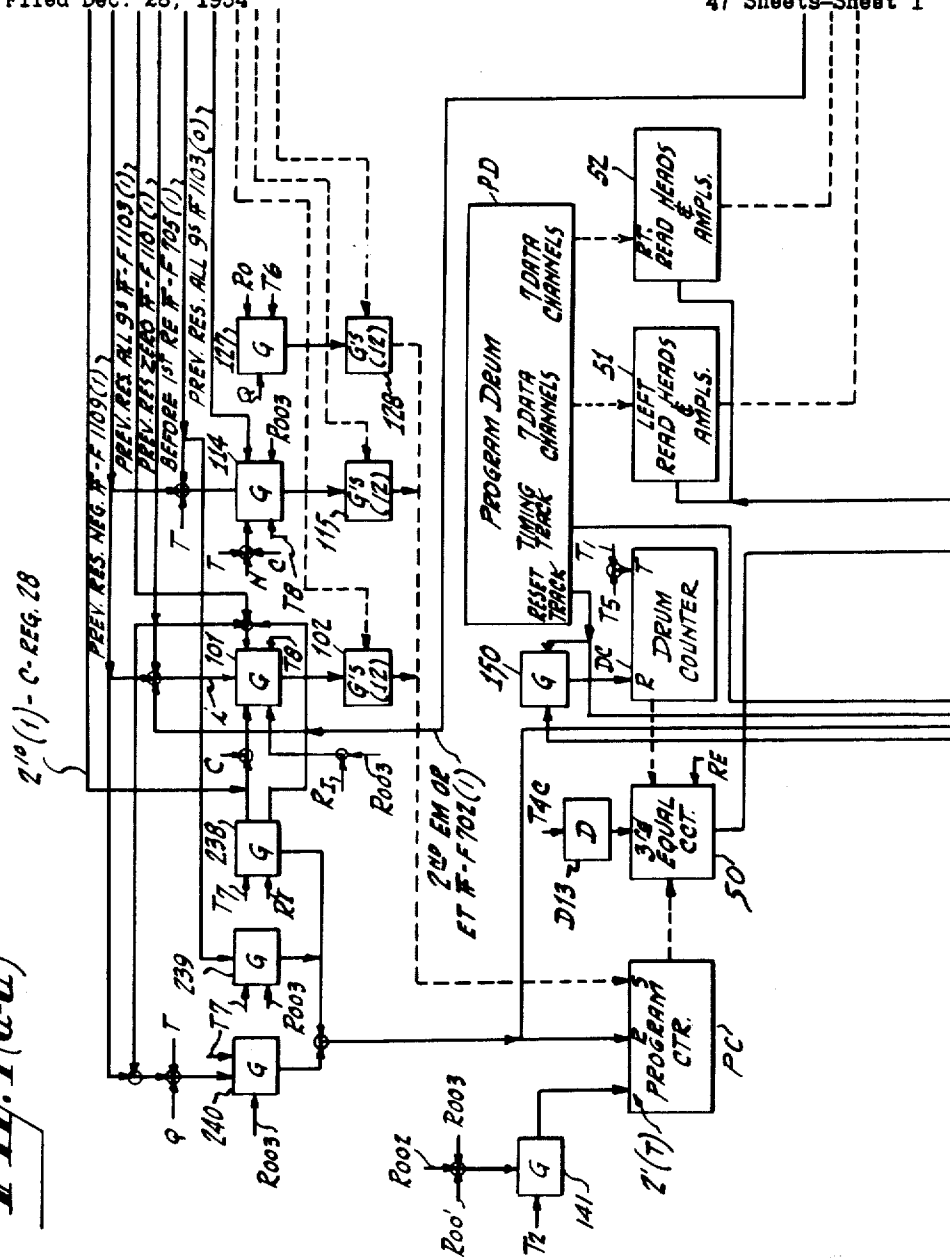
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Fig. 1(a-d)



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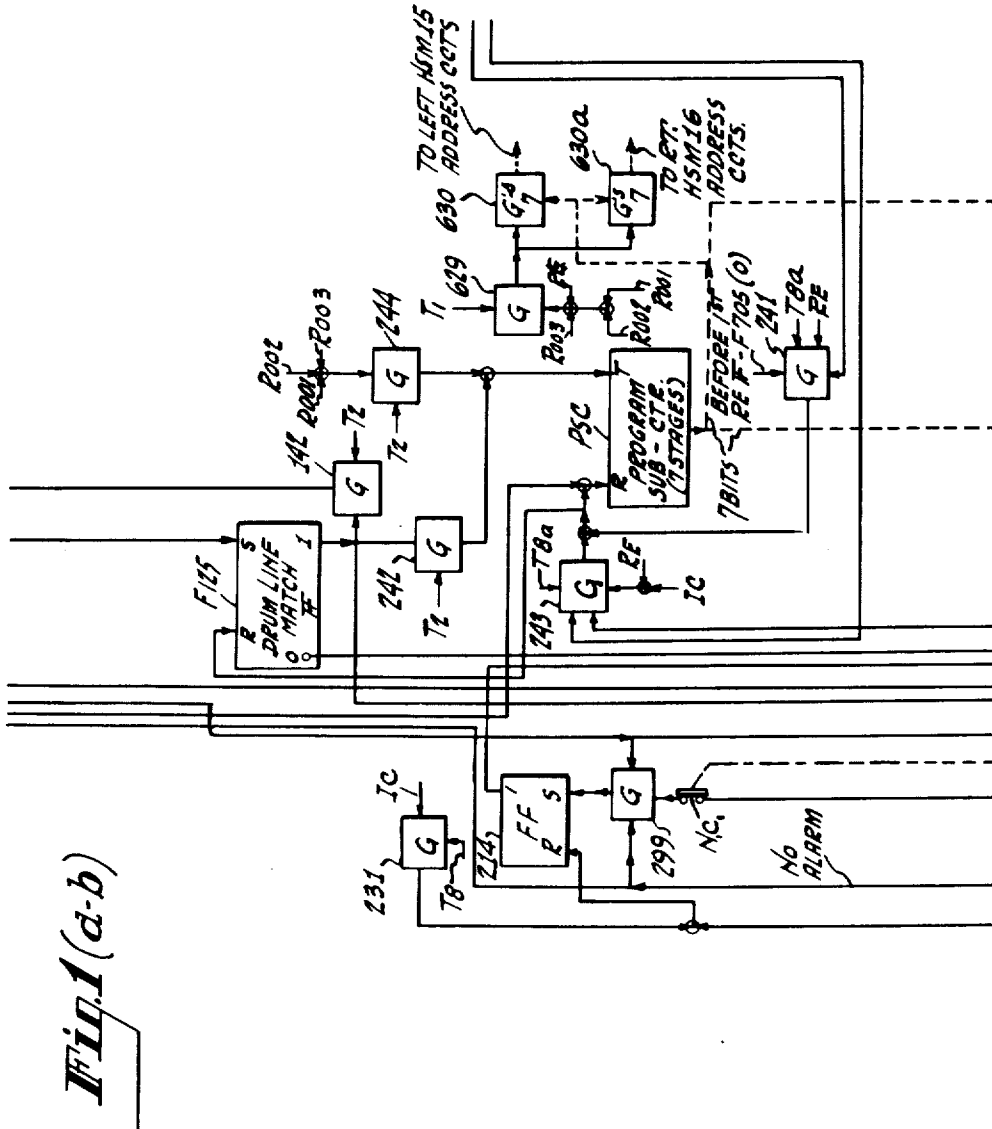


Fig. 1(a-b)

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LOWELL S. BENSKY
BY *Milton S. Winter*
ATTORNEY

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Fig. 1(a-c)

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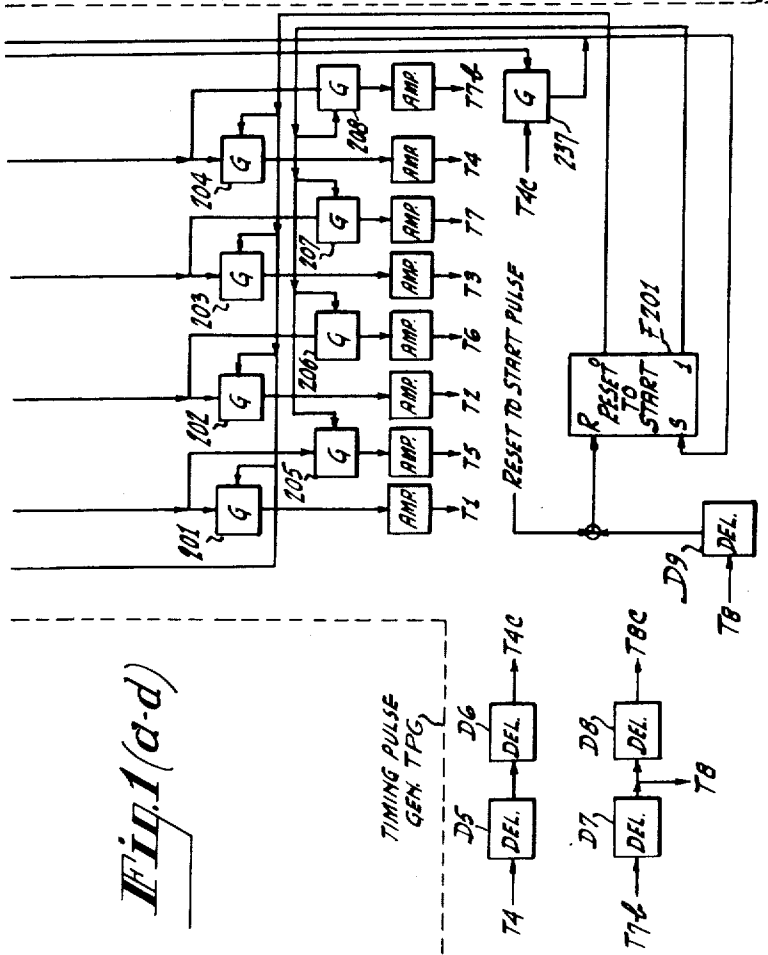
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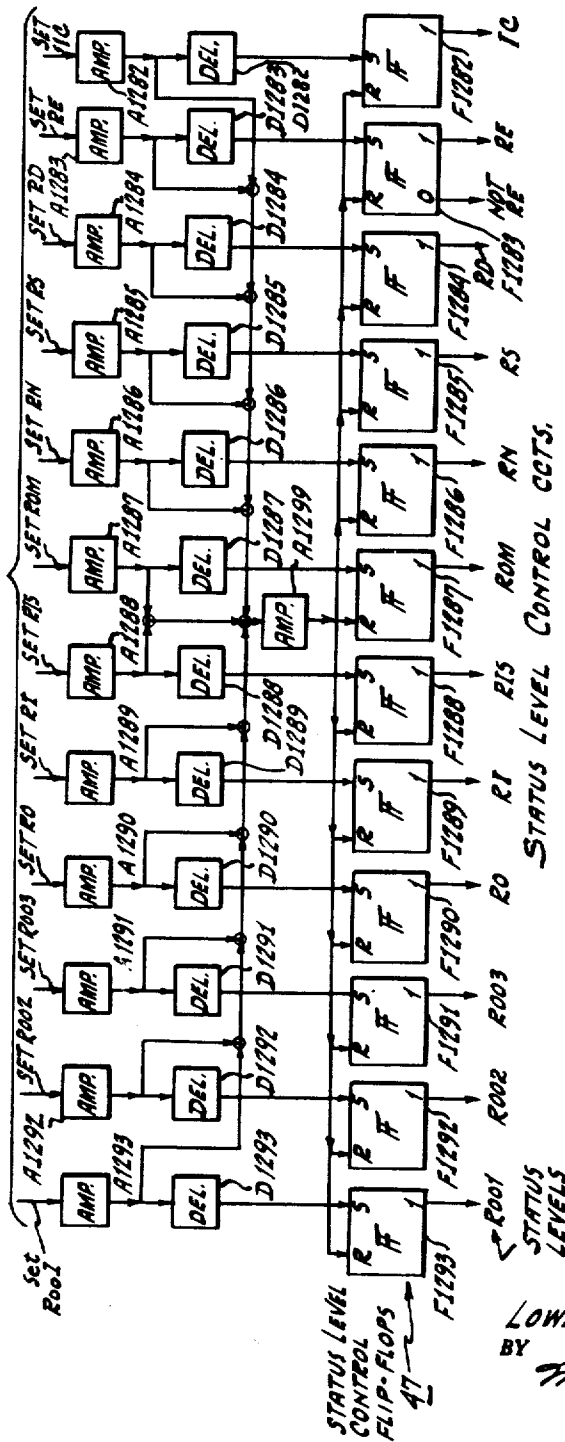
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Fig. 1(a-e)

INPUTS FROM STATUS TRANSITION GATES
FIGS 1G & 1H



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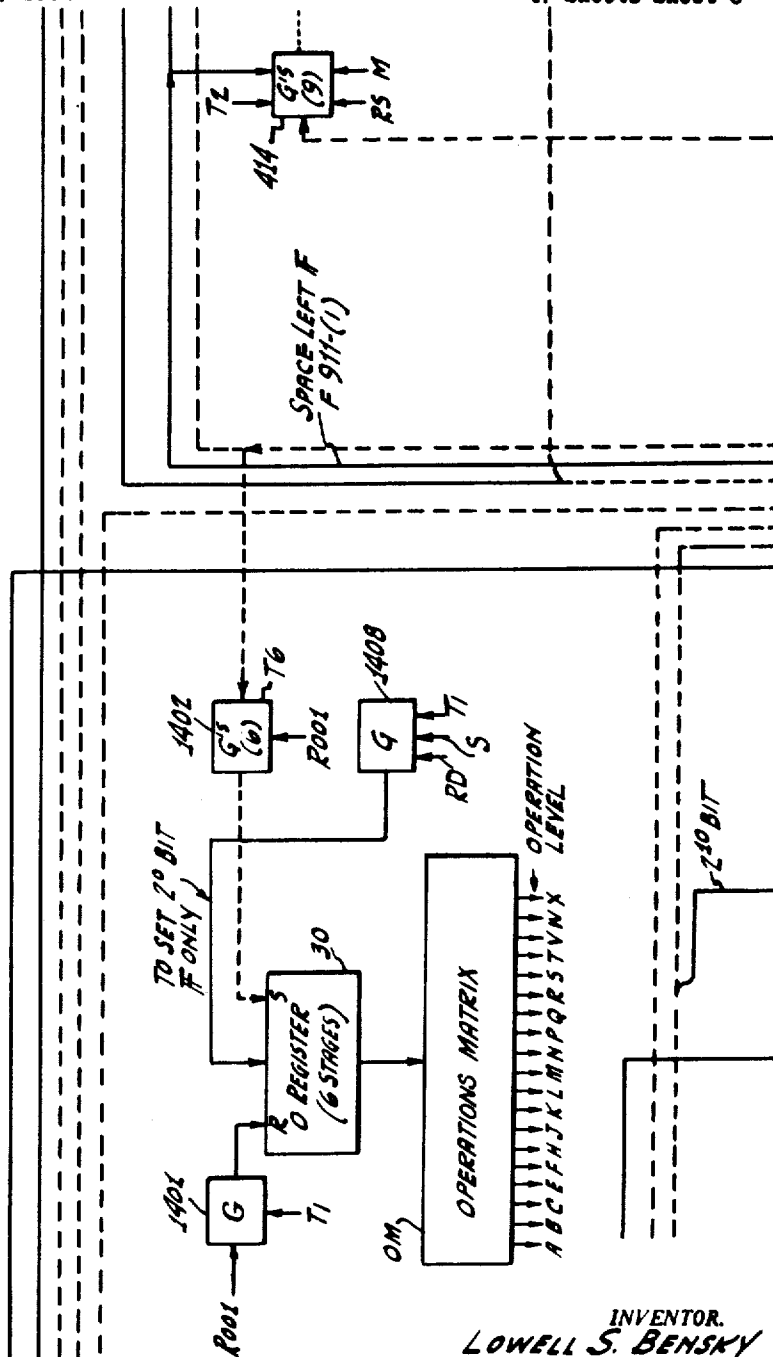
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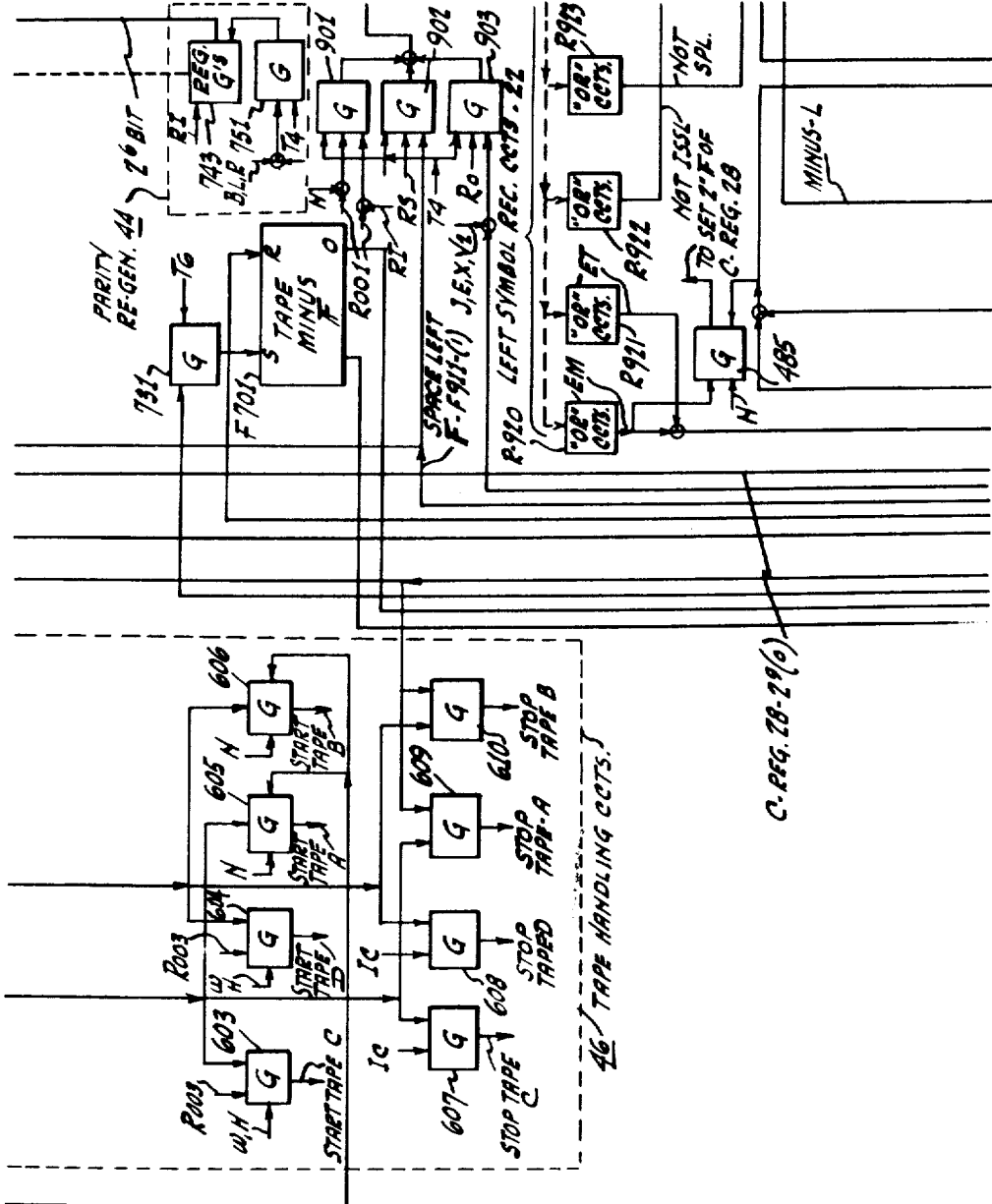


Fig. 1(b-d)

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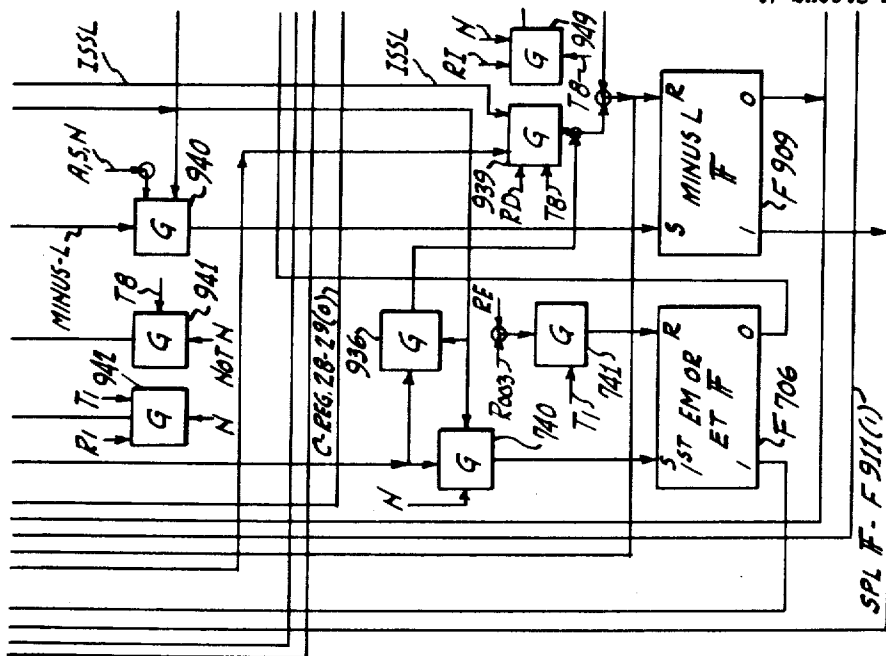


Fig. 1(b-e)

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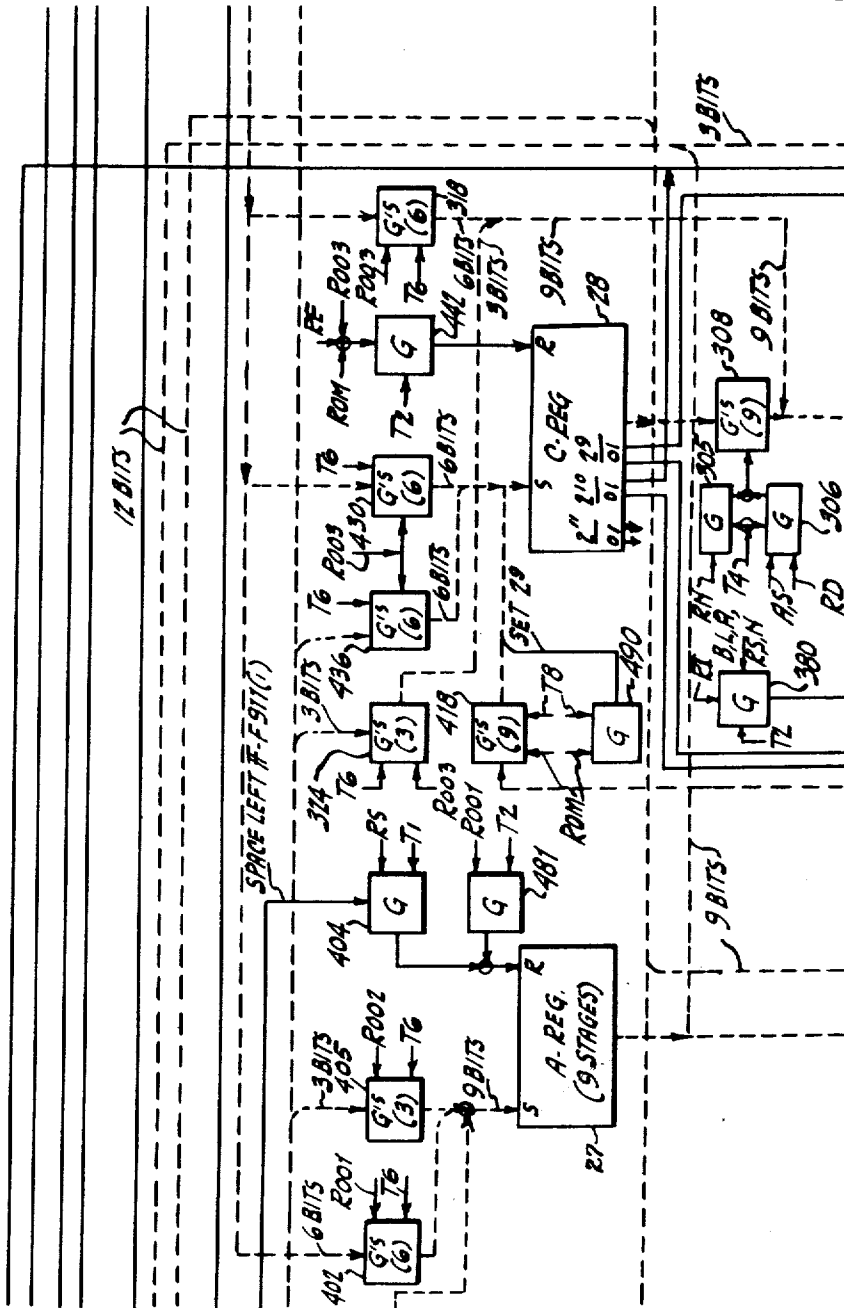
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47 Sheets-Sheet 11

Fig. 1(c-d)



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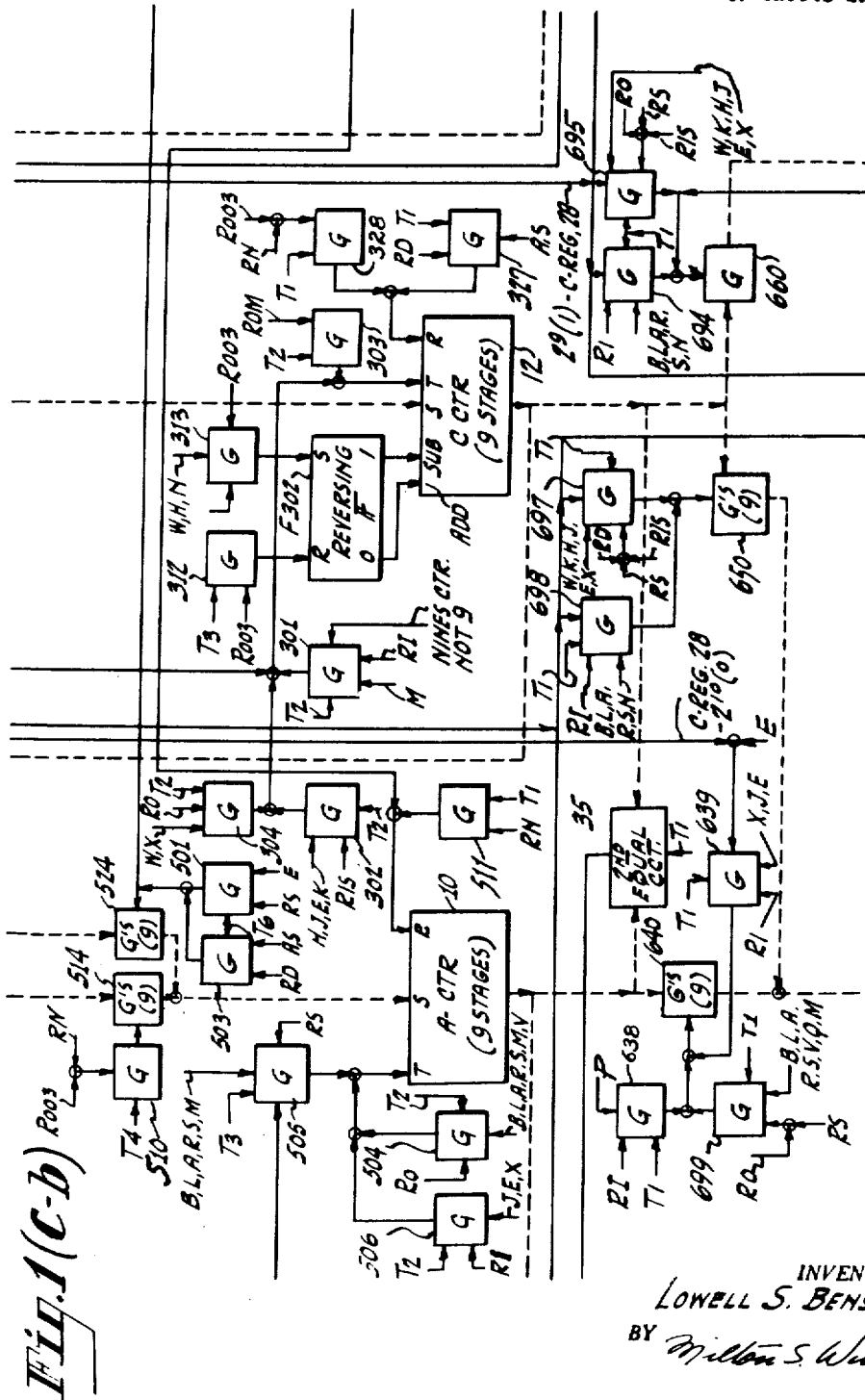
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Fig. 1(c-c)

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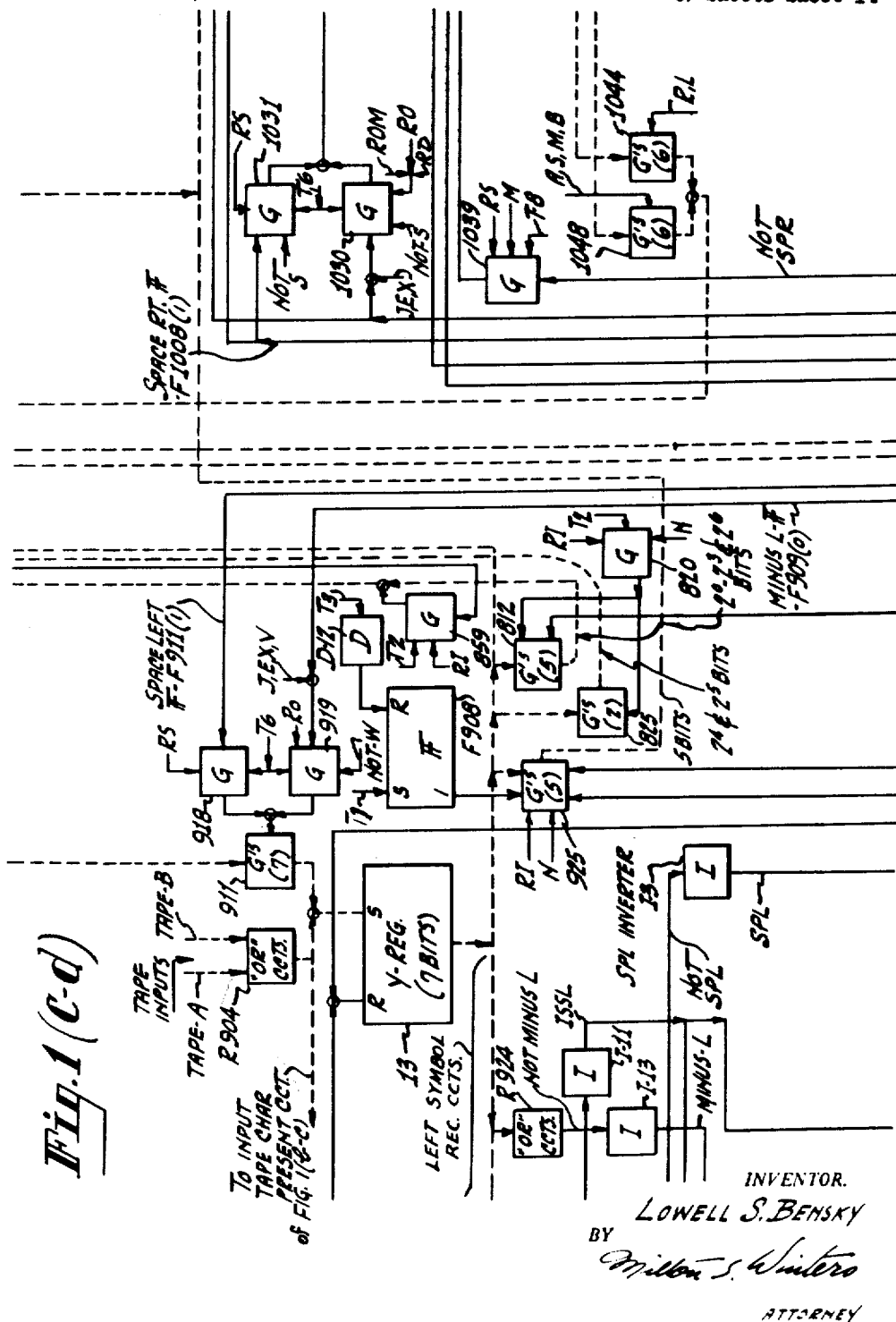
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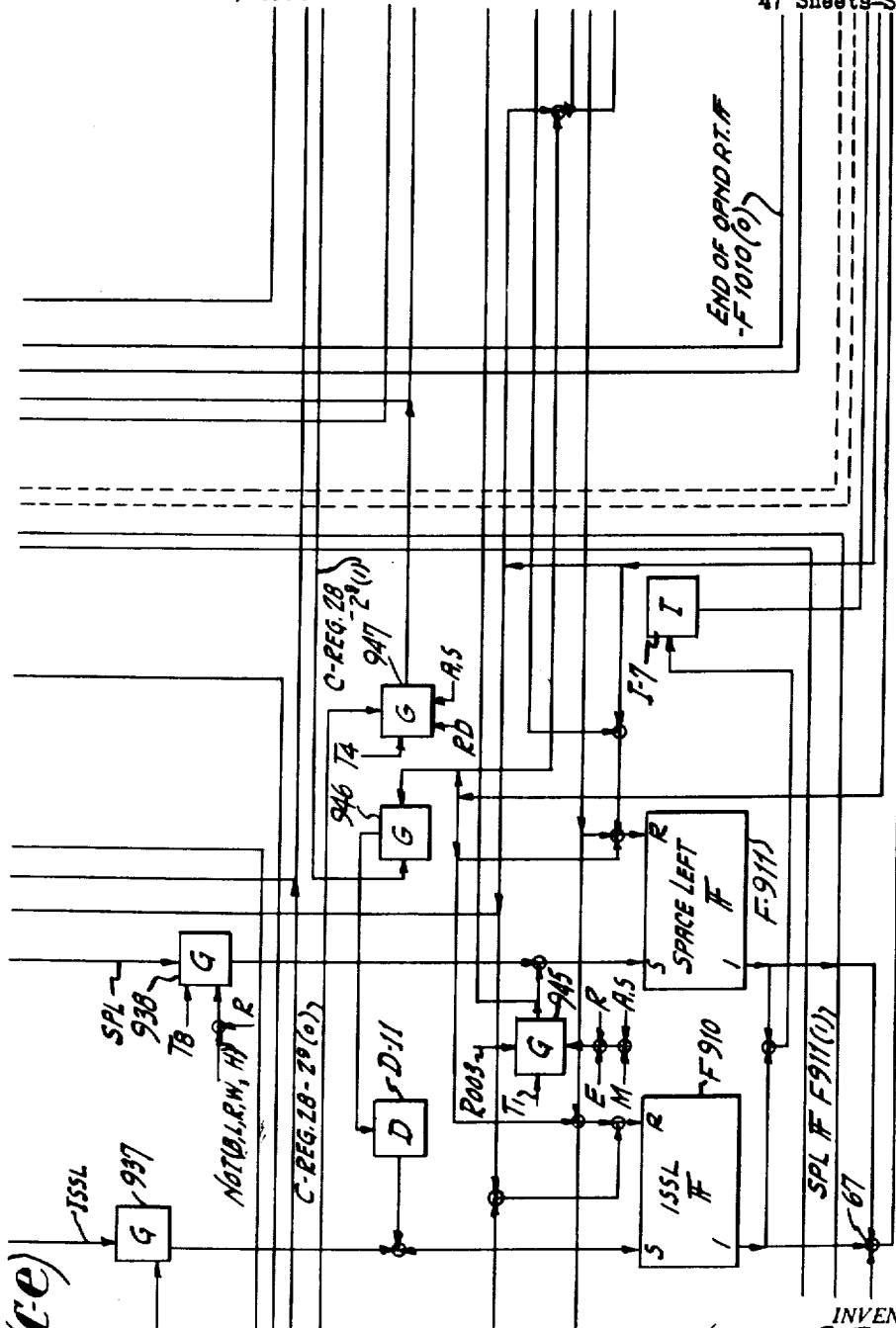
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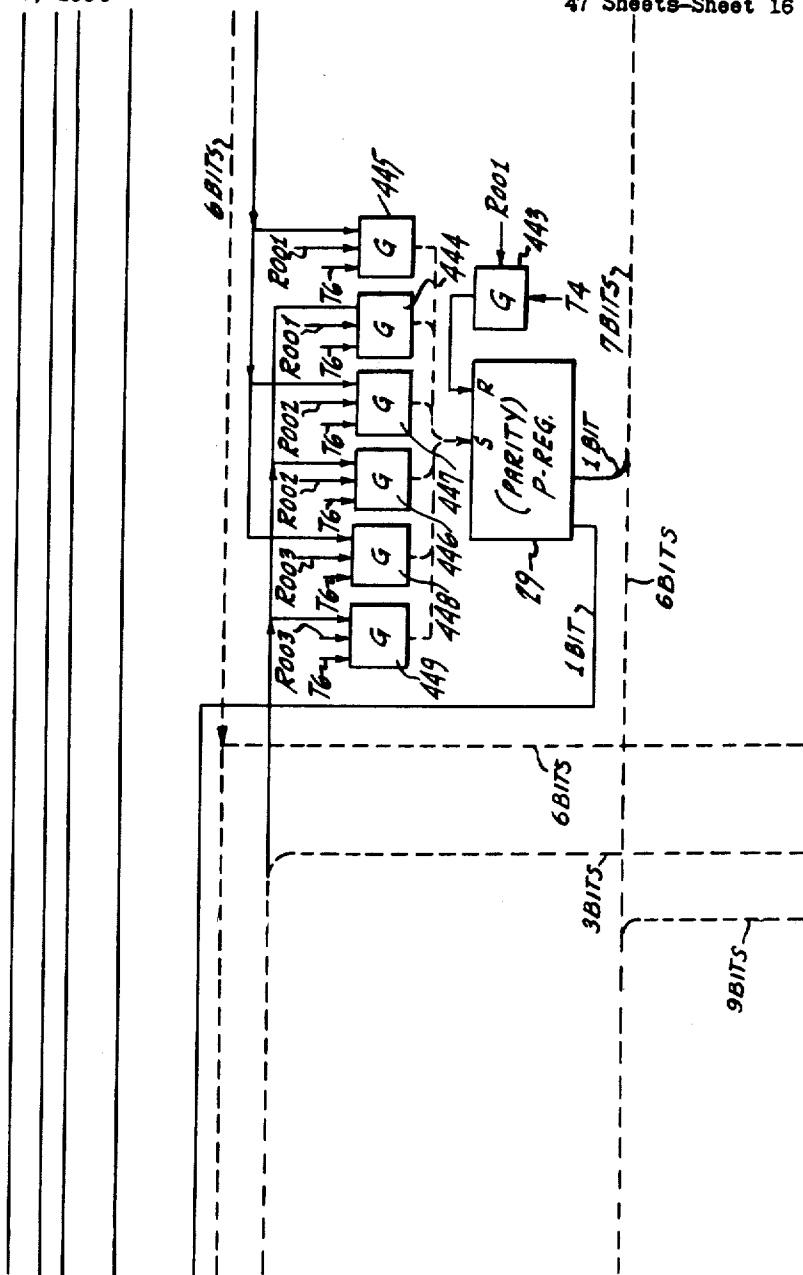


Fig. 1.(d-a)

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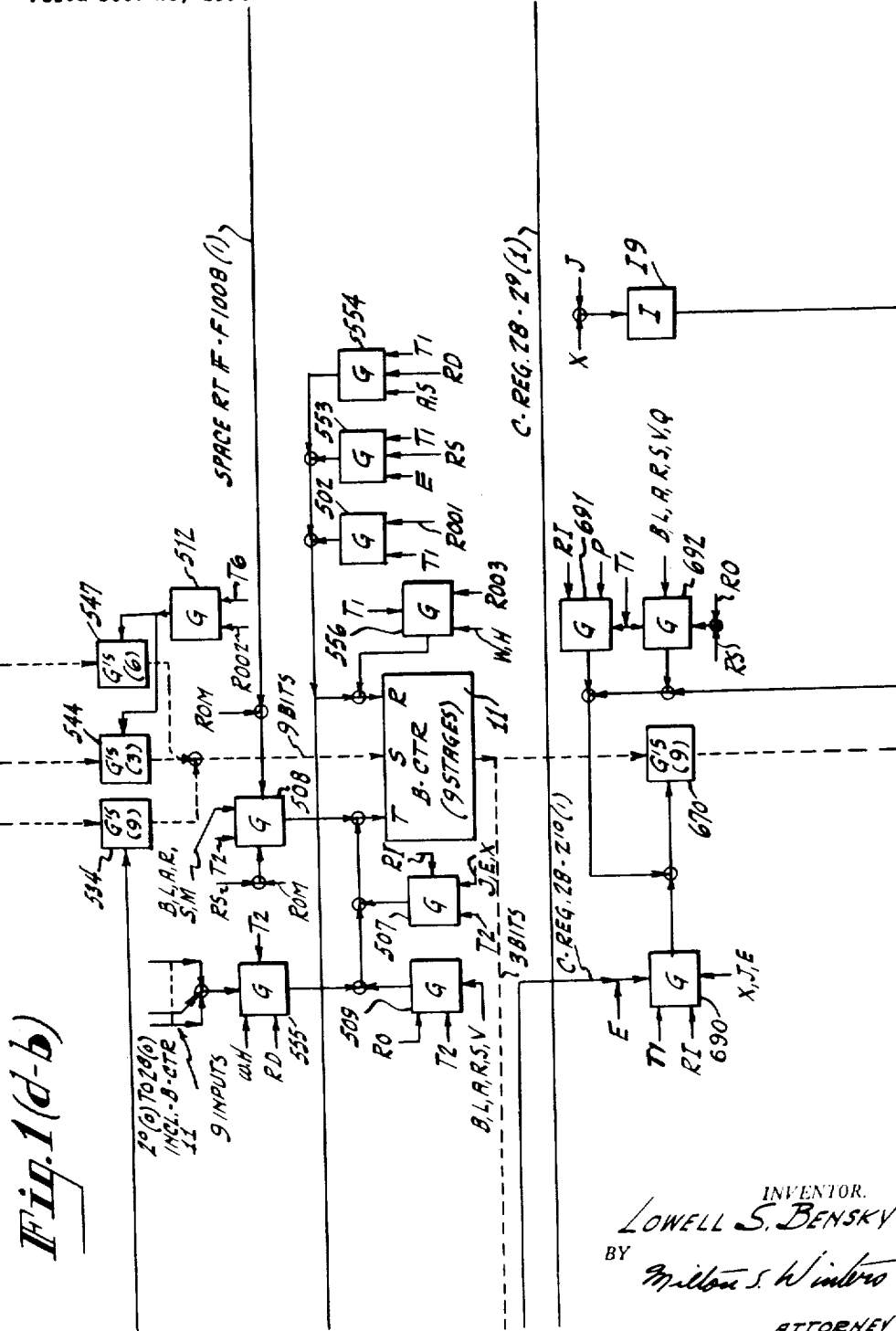
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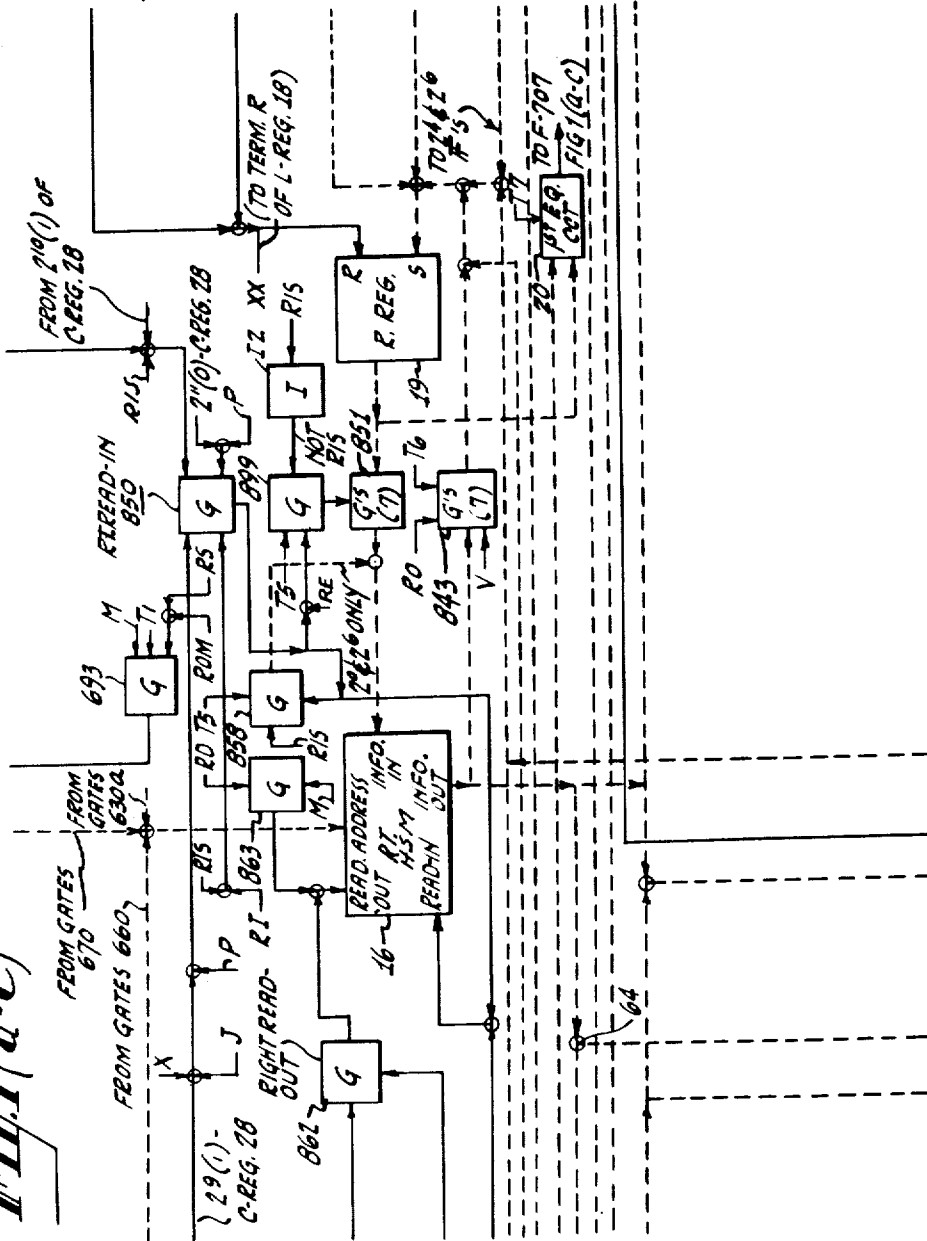
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Fig. 1(d-c)



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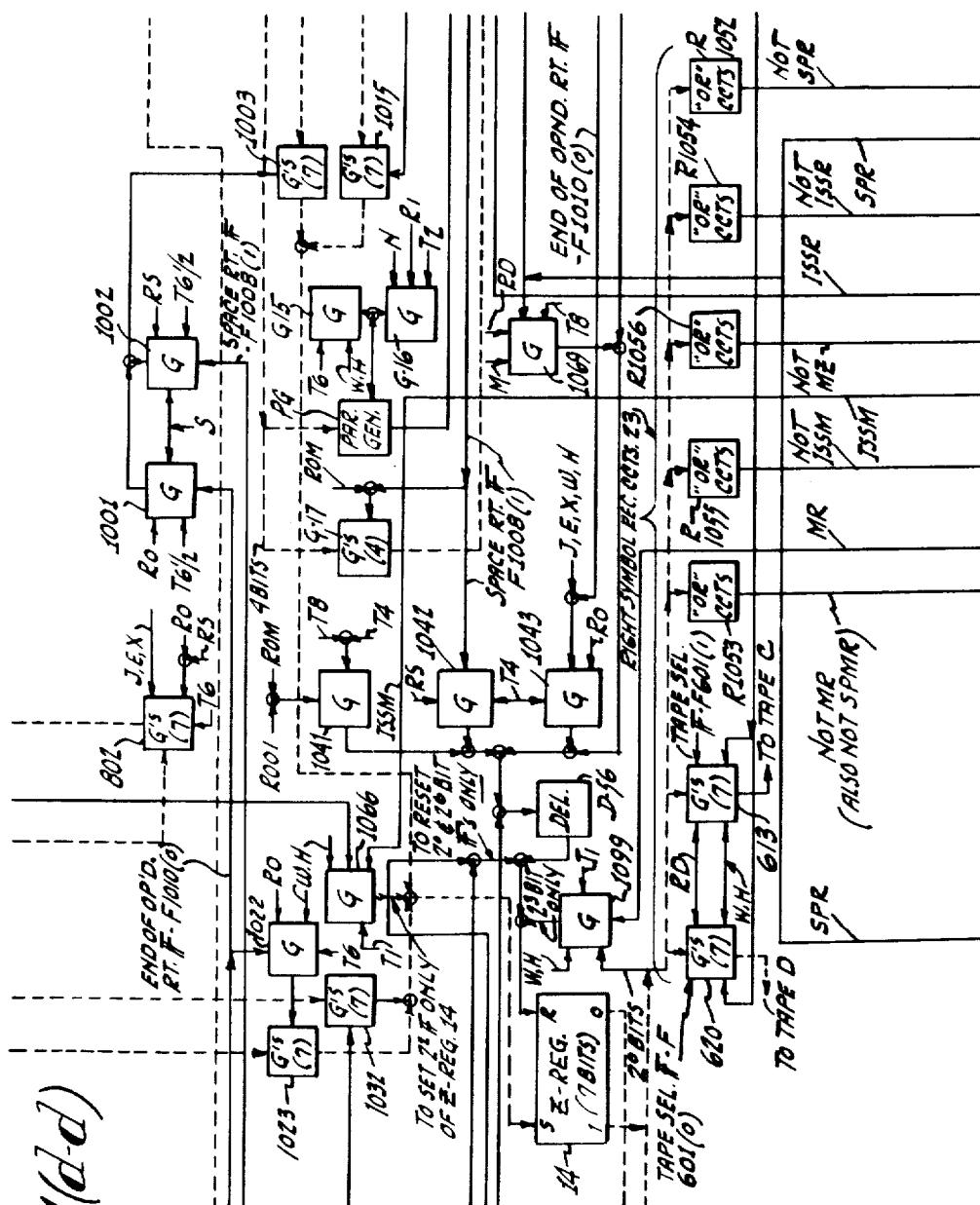


Fig. 1(d-d)

INVENTOR.
LOWELL S. BENSKY
BY *Milton S. Winters*
ATTORNEY

ATTORNEY

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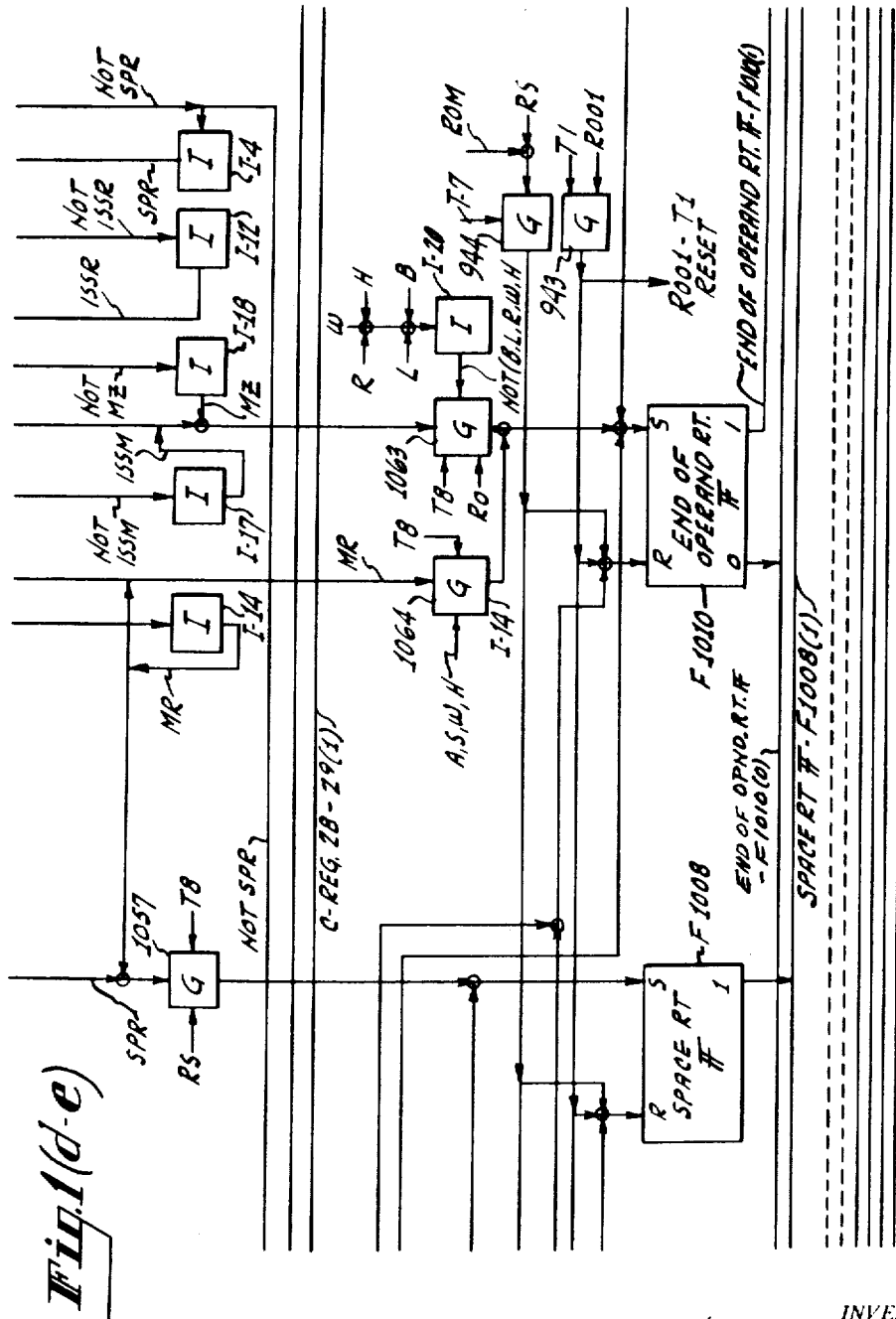


Fig. 1(d-e)

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Jan. 14, 1964

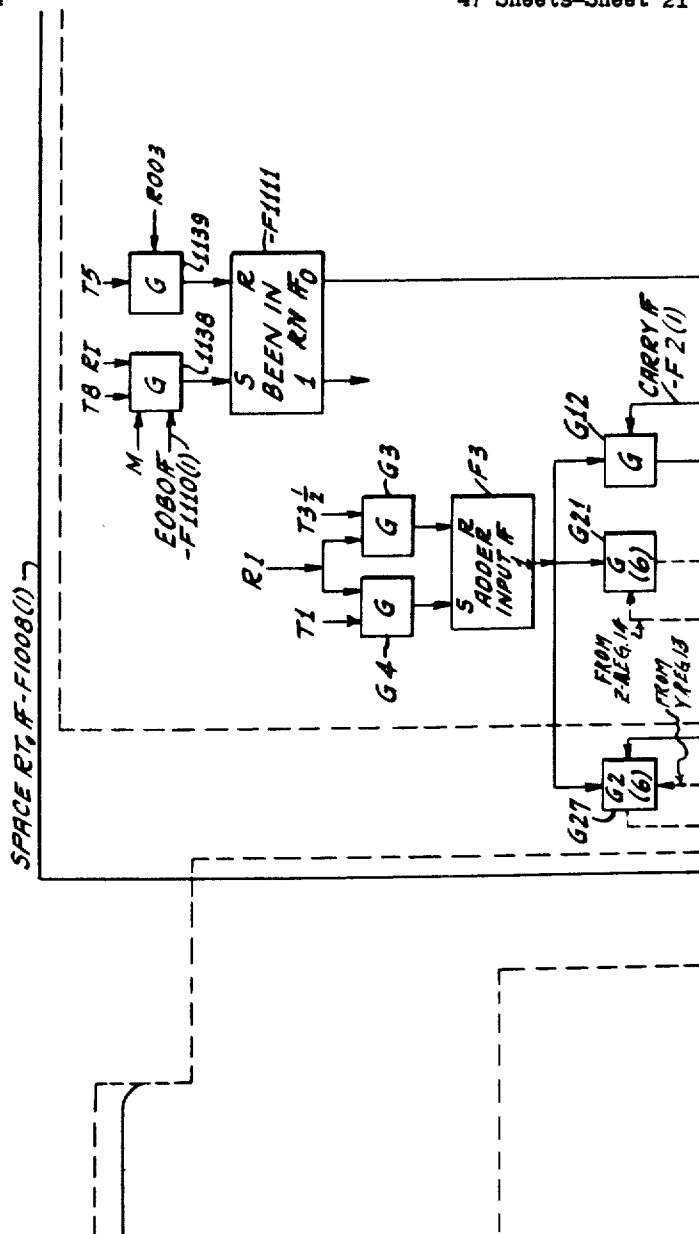
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Fig. 1(e-a)



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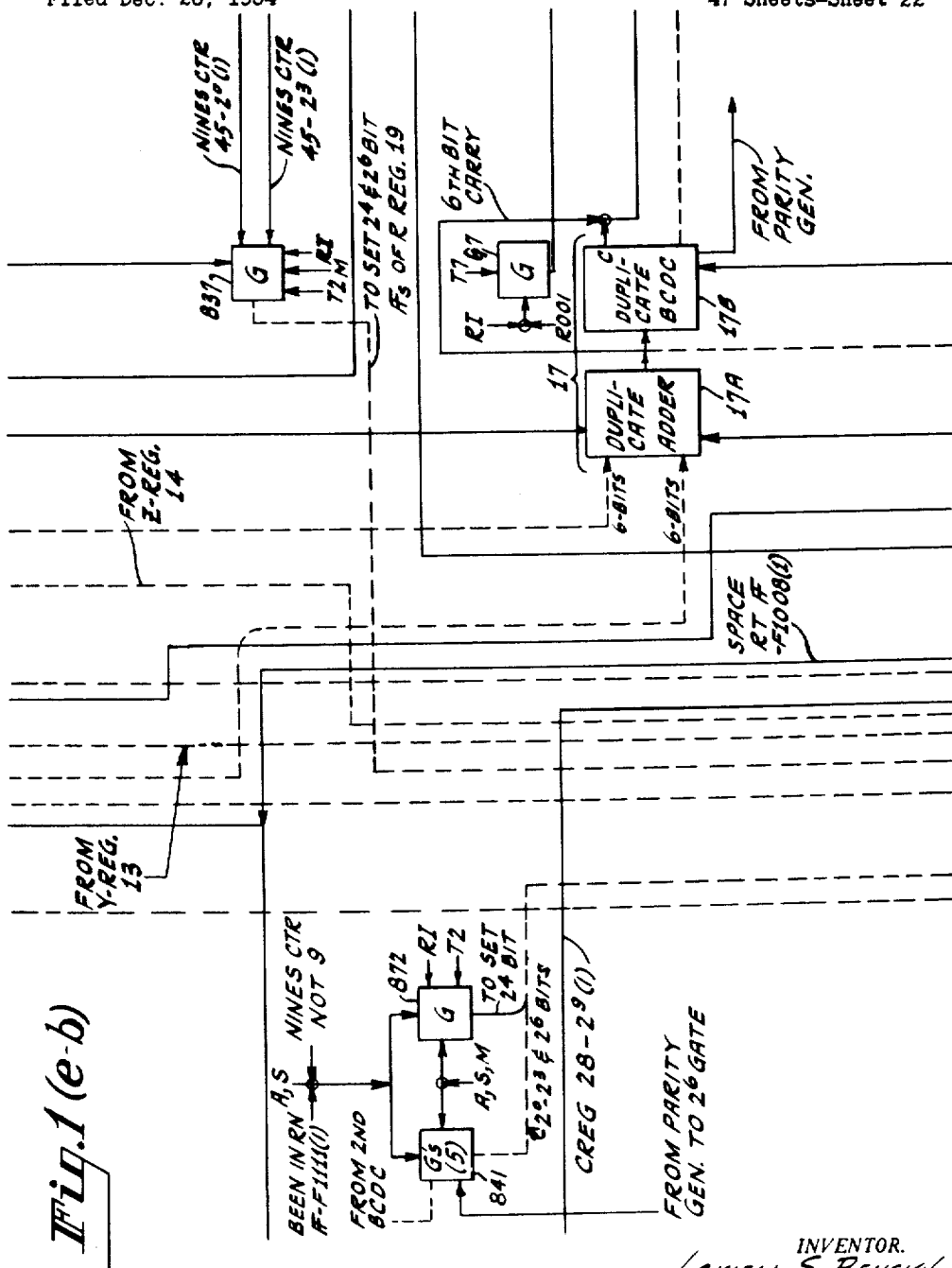


Fig. 1(e-b)

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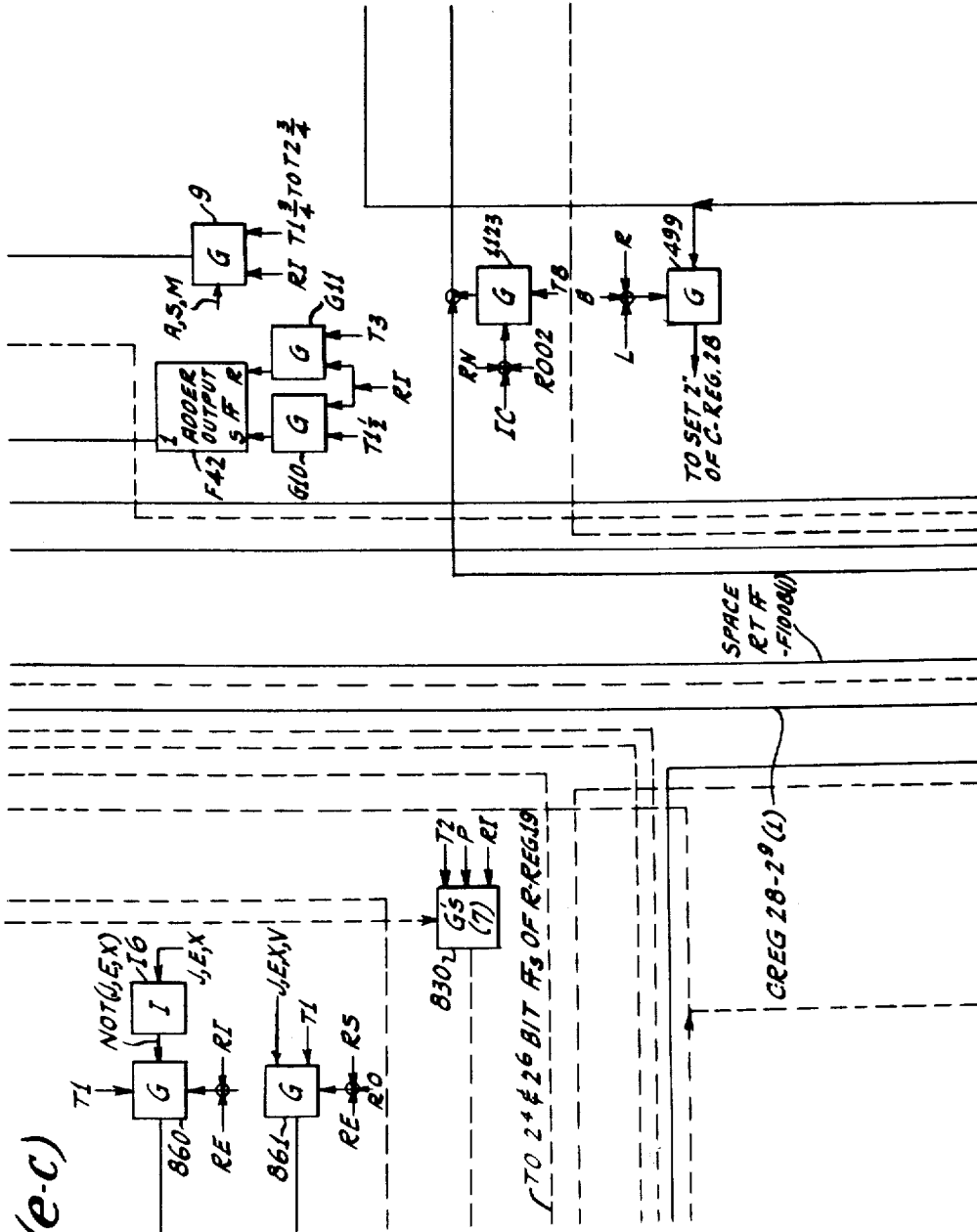
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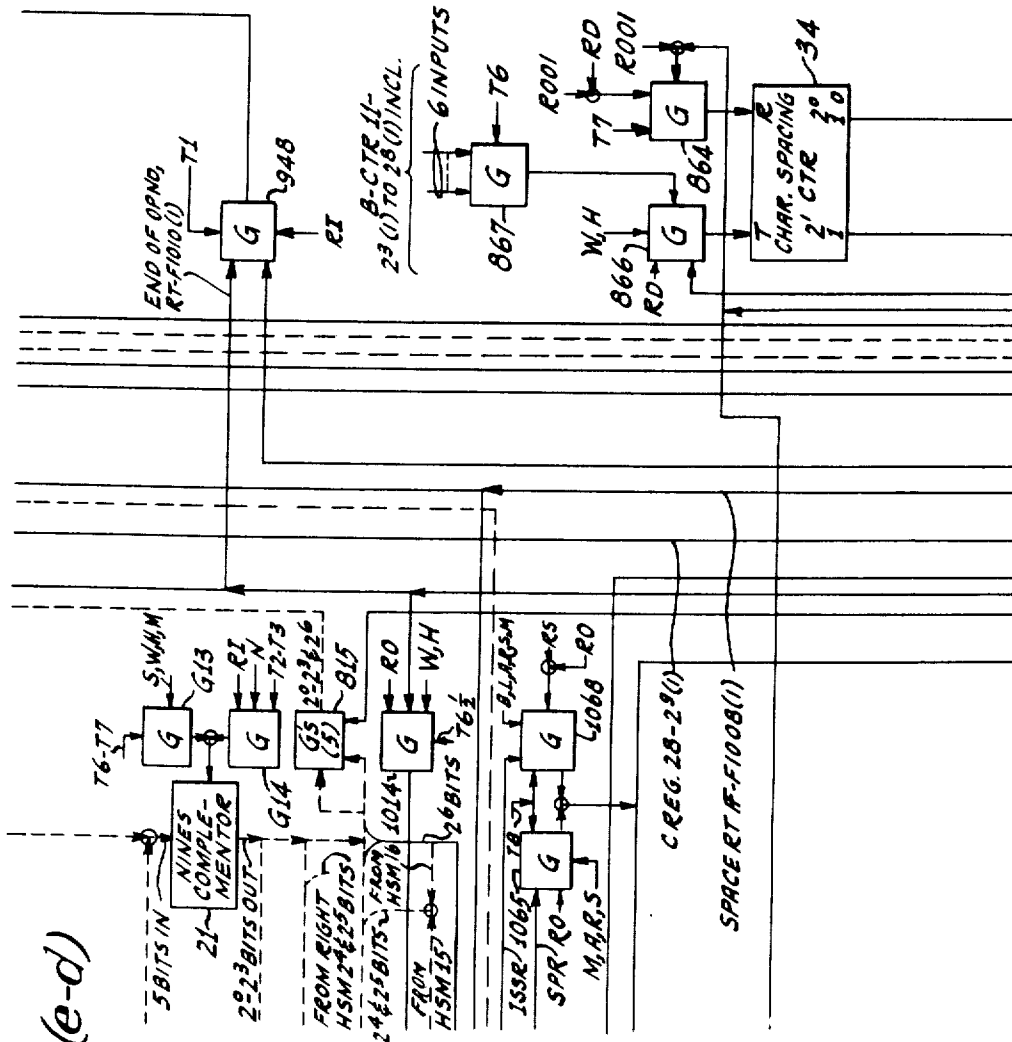


Fig. 1(e-d)

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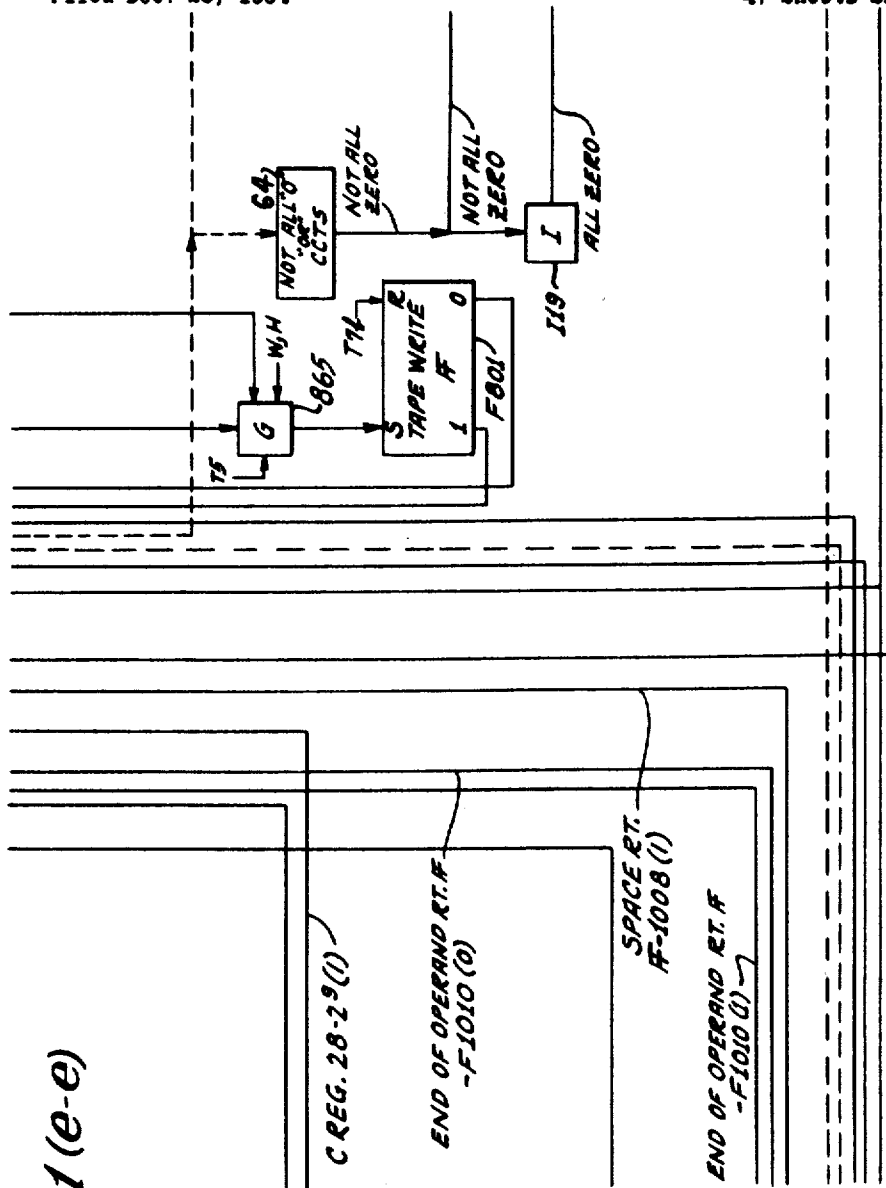


Fig. 1(e-e)

INVENTOR.
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BY *Milton S. Winthro*
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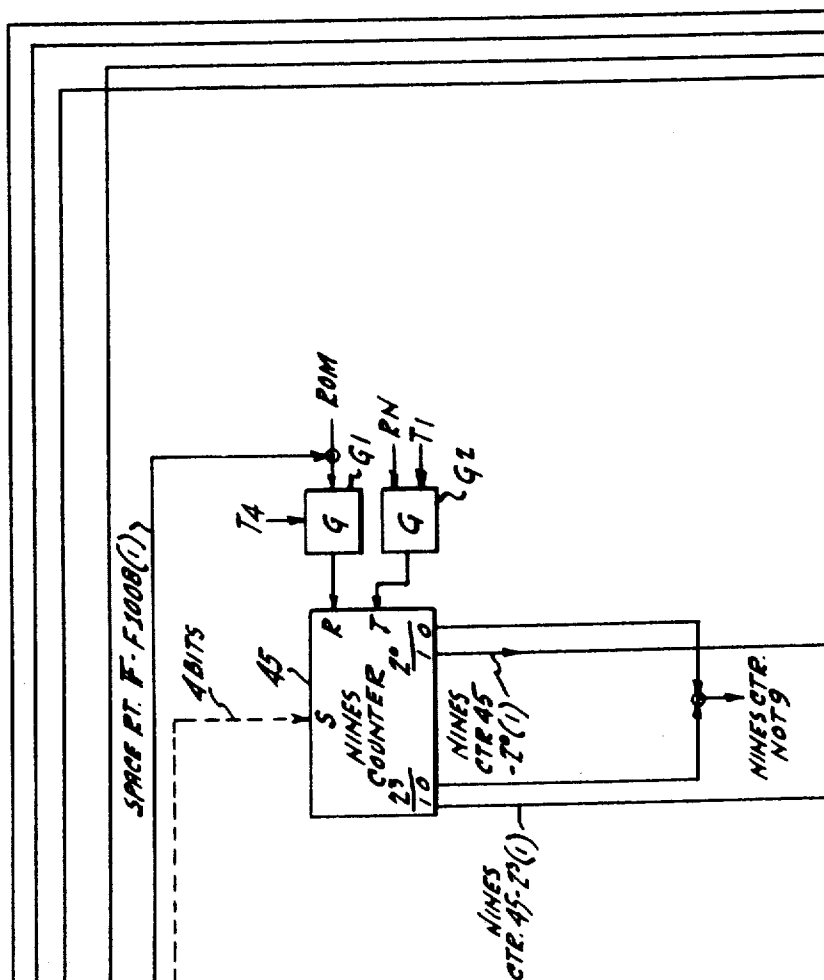
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Fig. 1(f-d)



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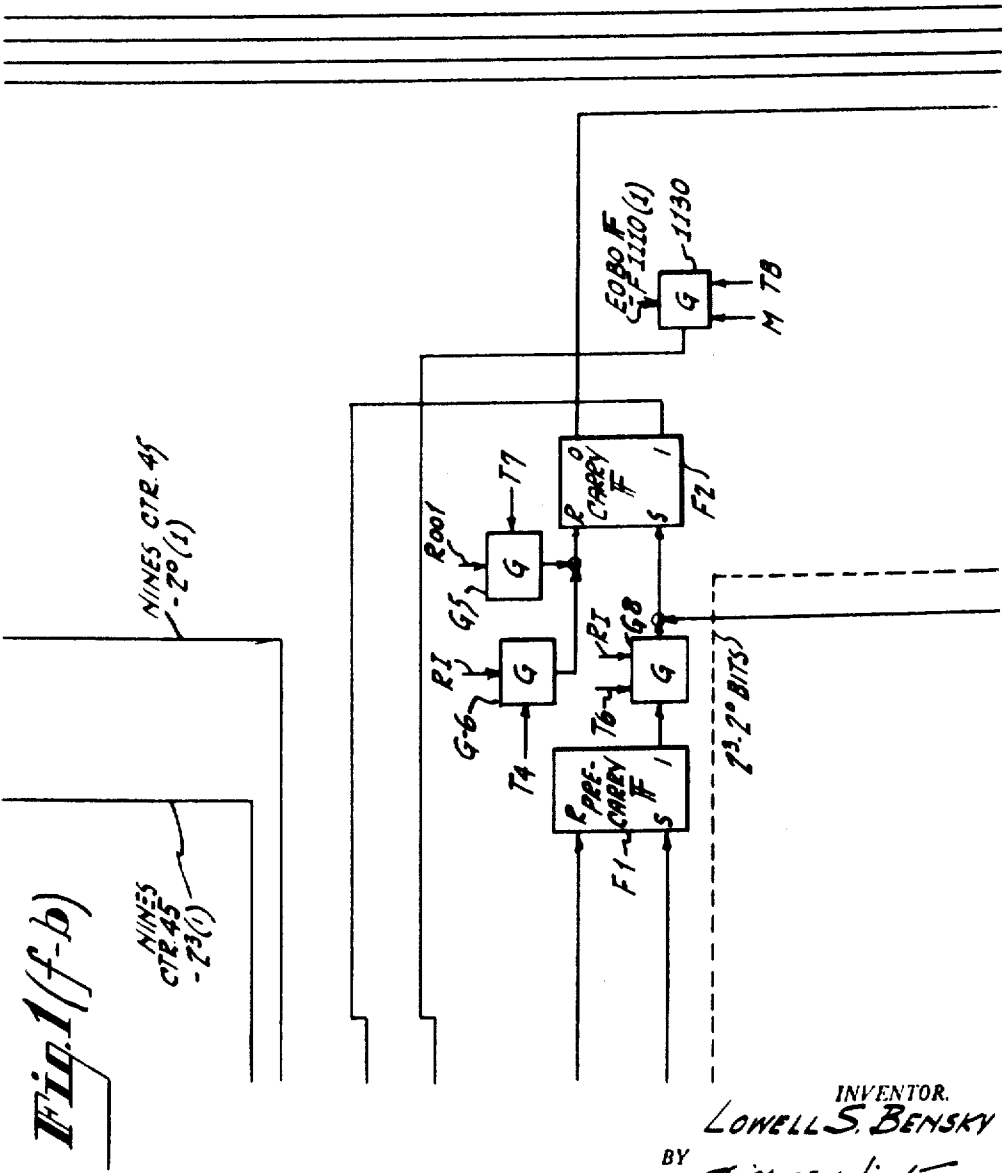
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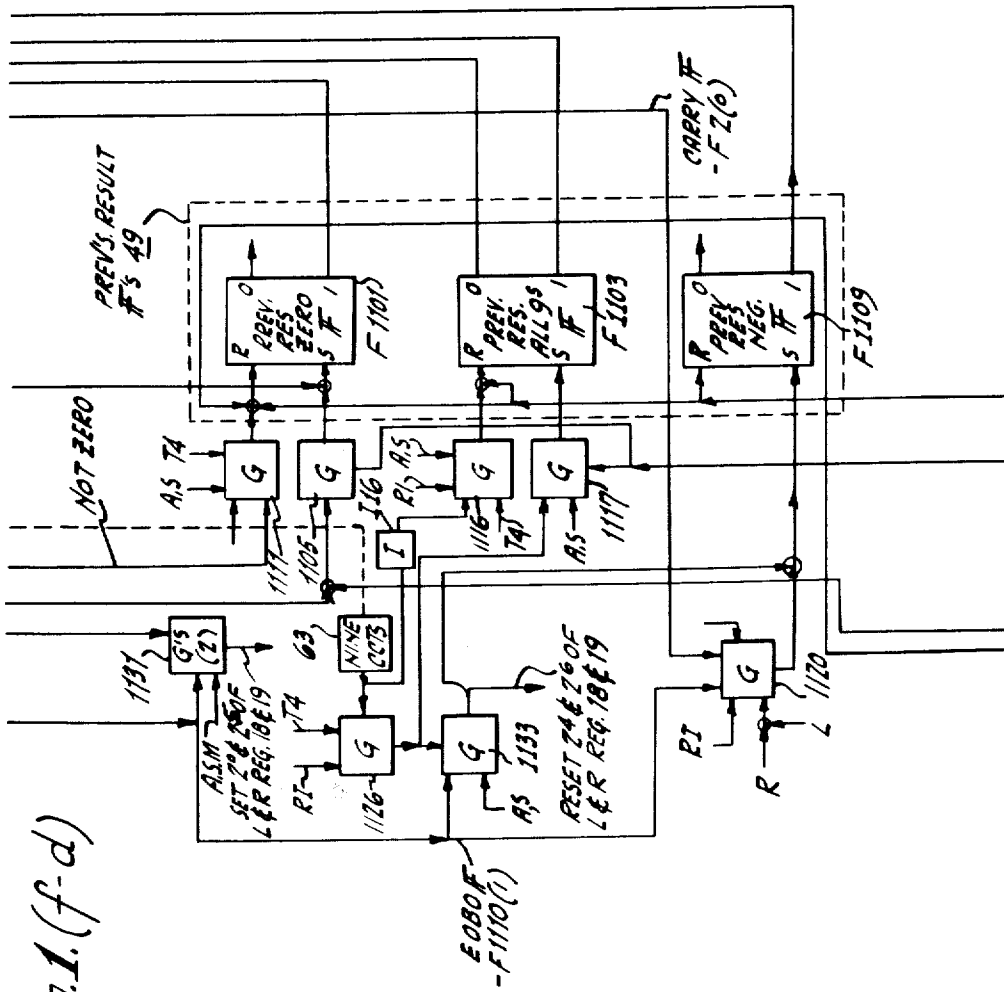


Fig. 1(f-d)

INVENTOR.
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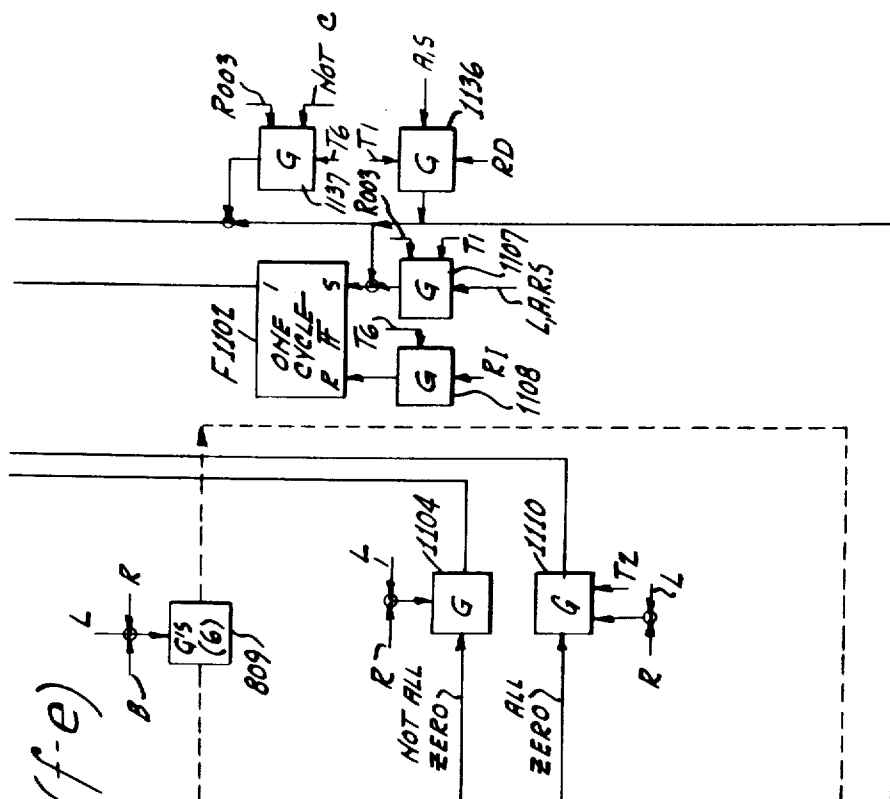


Fig. 1(f-e)

INVENTOR.
LOWELL S. BENSKY
BY
Millan S. Waters
ATTORNEY

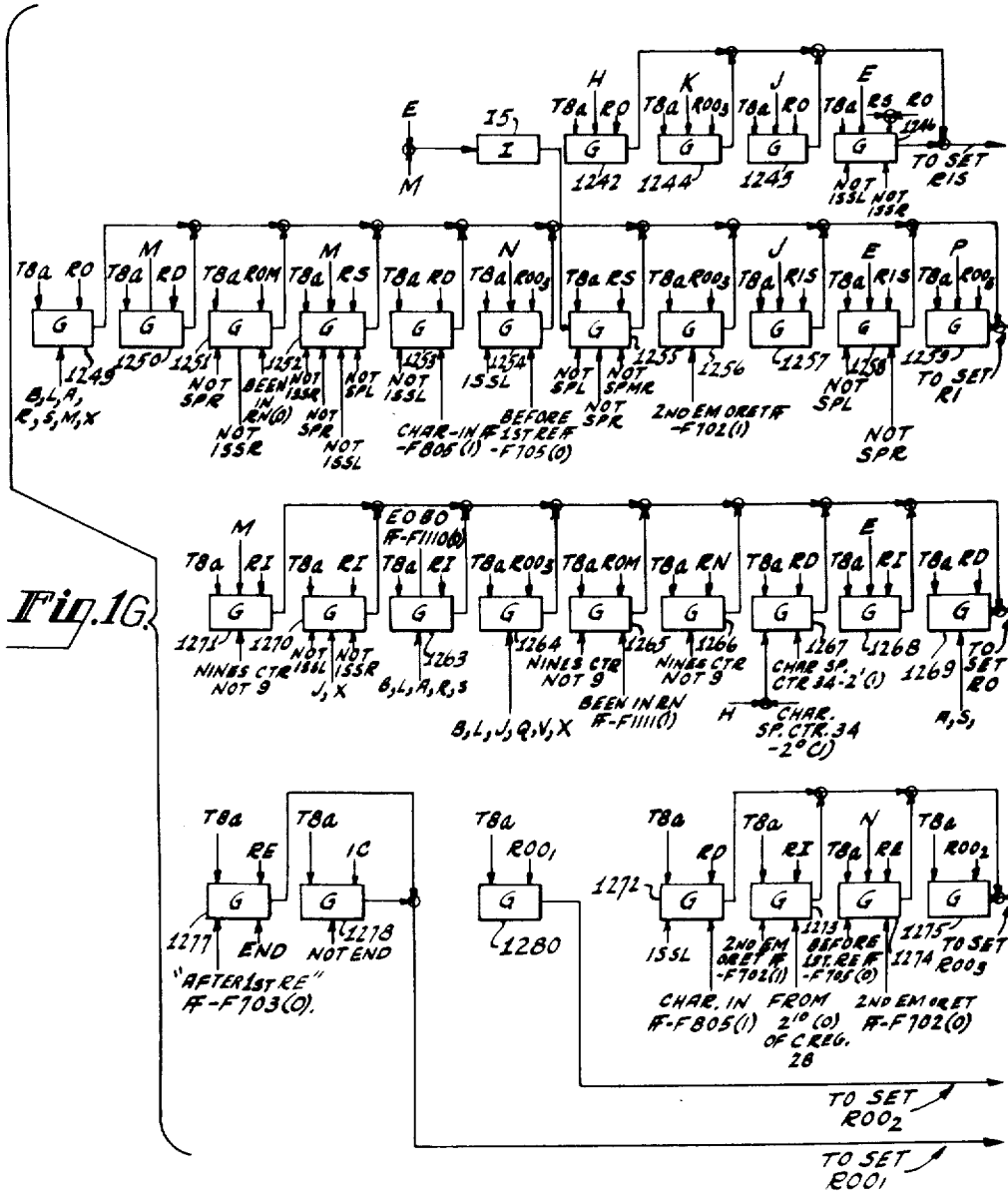
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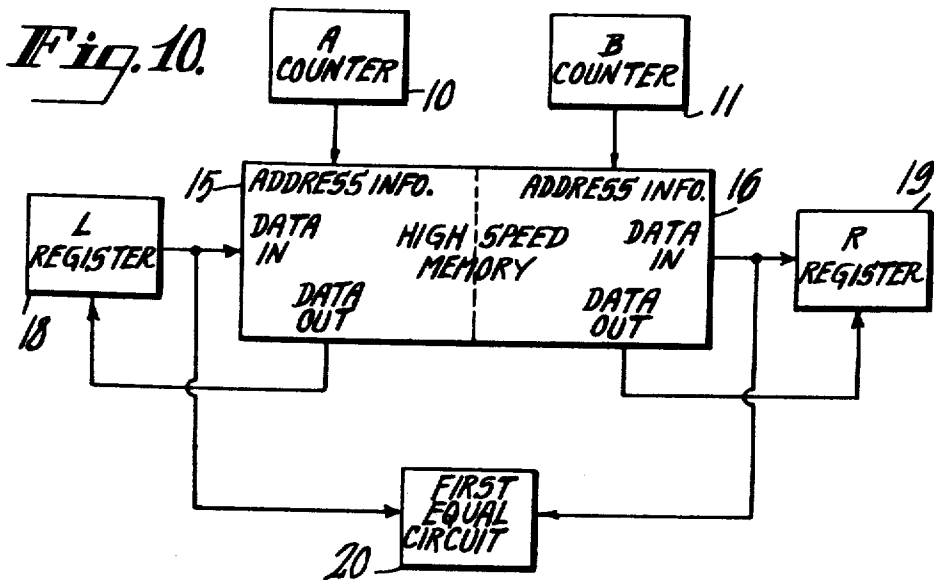
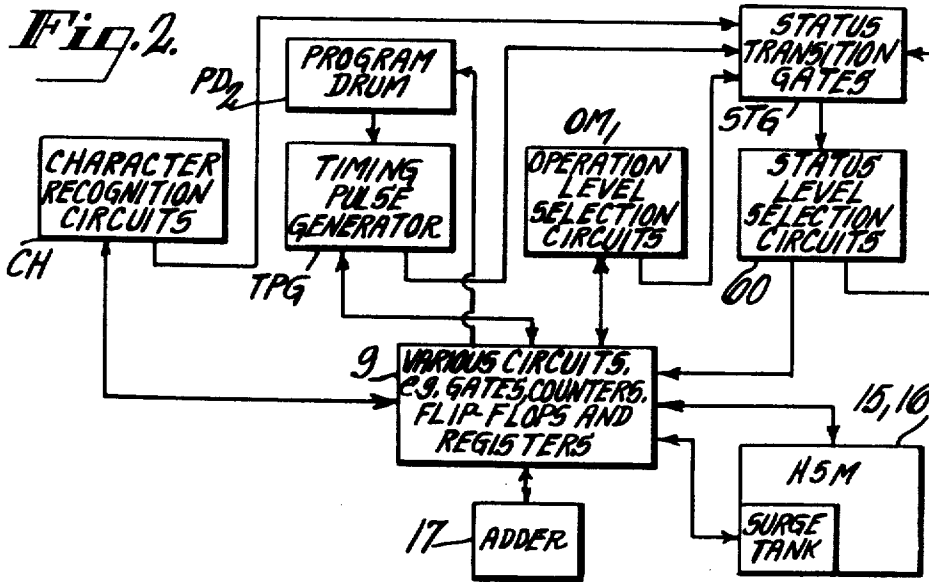
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47 Sheets-Sheet 33



VERIFY (OPER. V)

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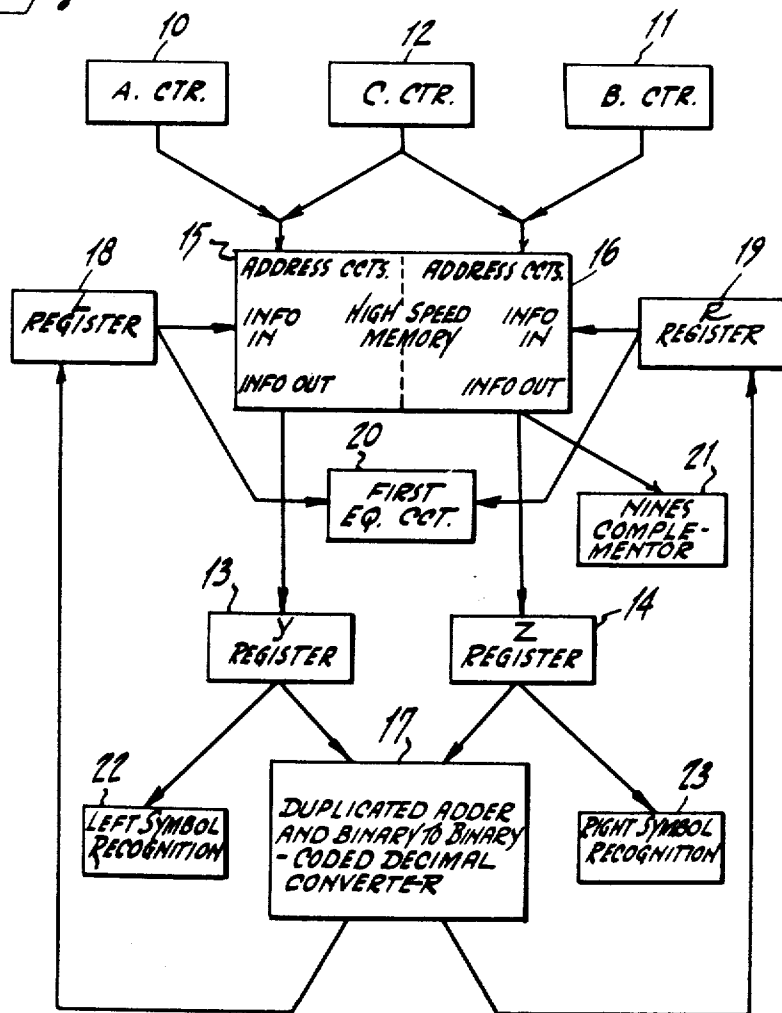
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Filed Dec. 28, 1954

47 Sheets-Sheet 34

Fig. 3.



DECIMAL ADDITION AND SUBTRACTION (OPER. A & S)

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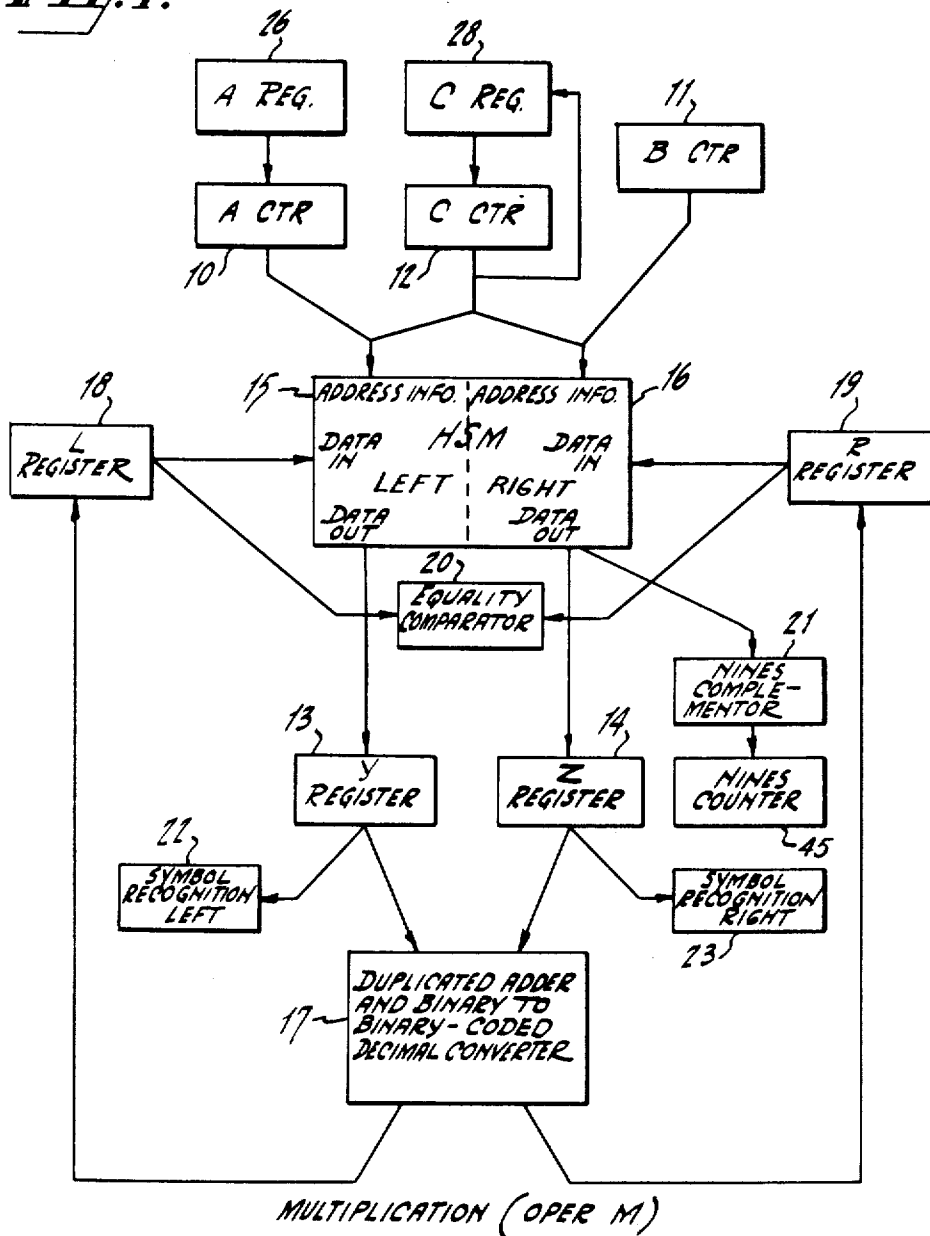
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Fig. 4.



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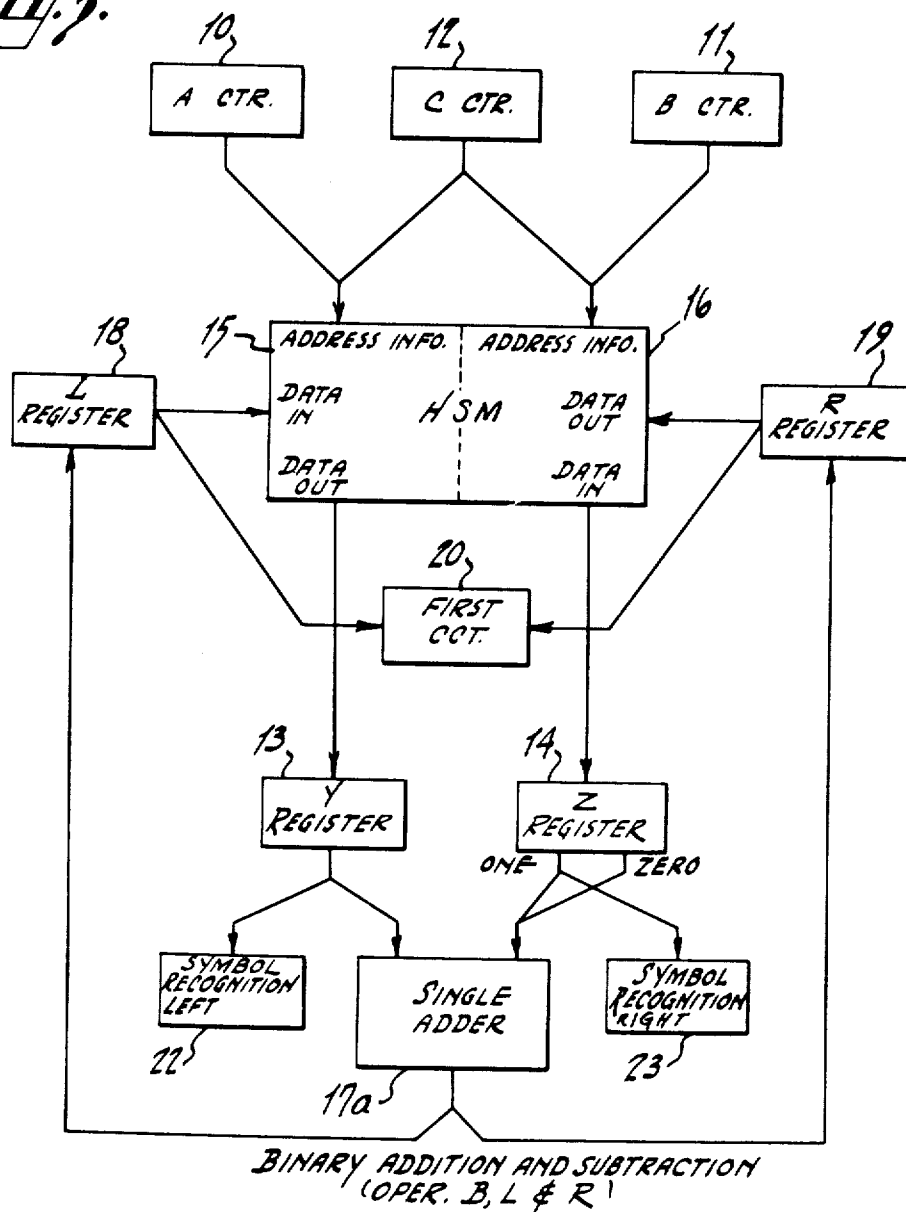
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Fig. 5.



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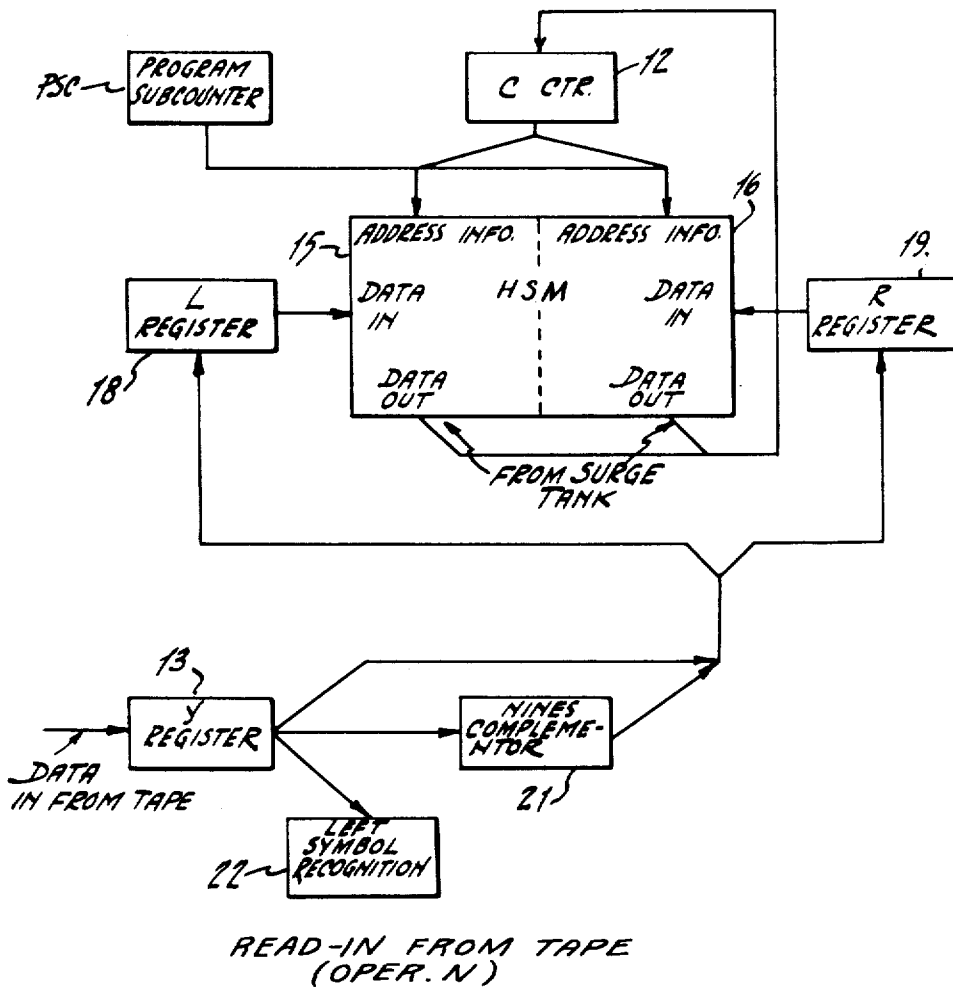
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Fig. 6



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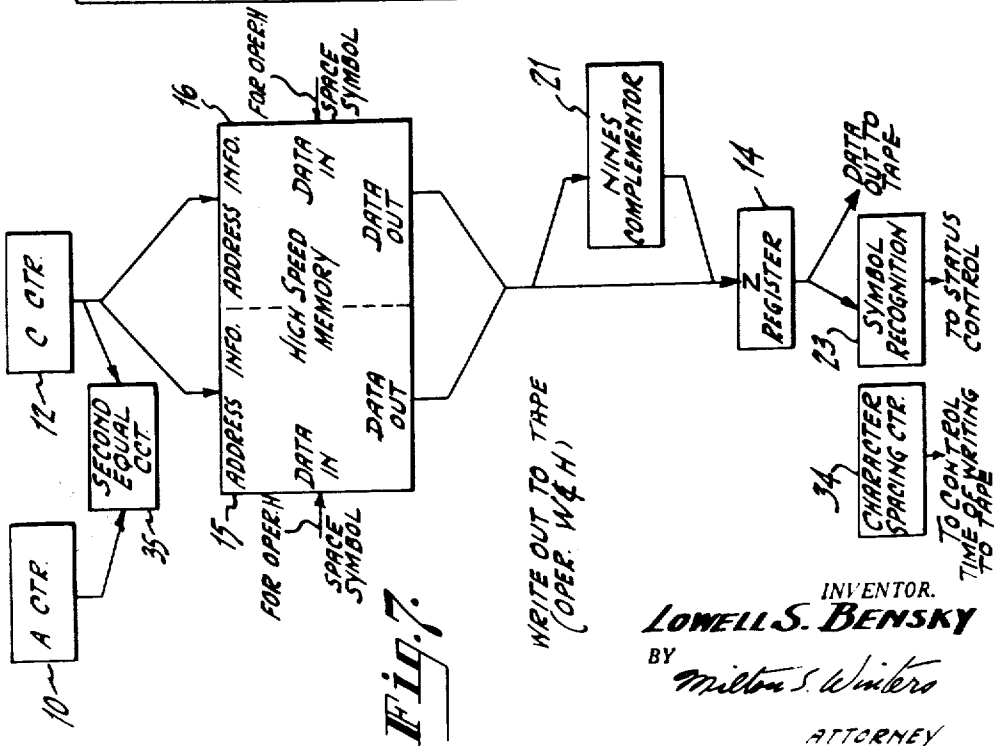
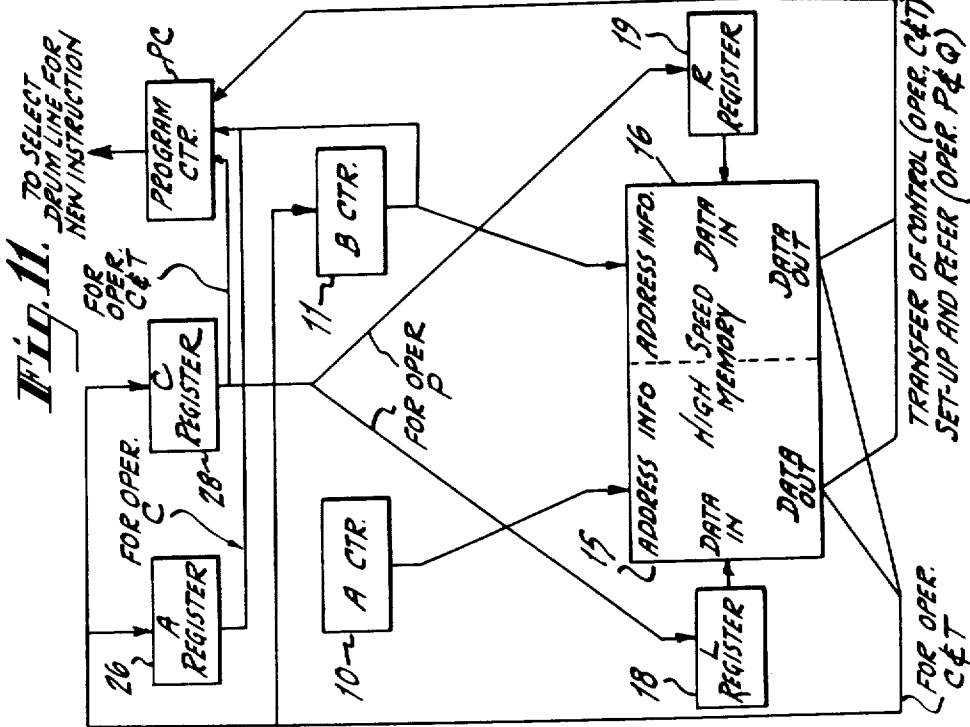
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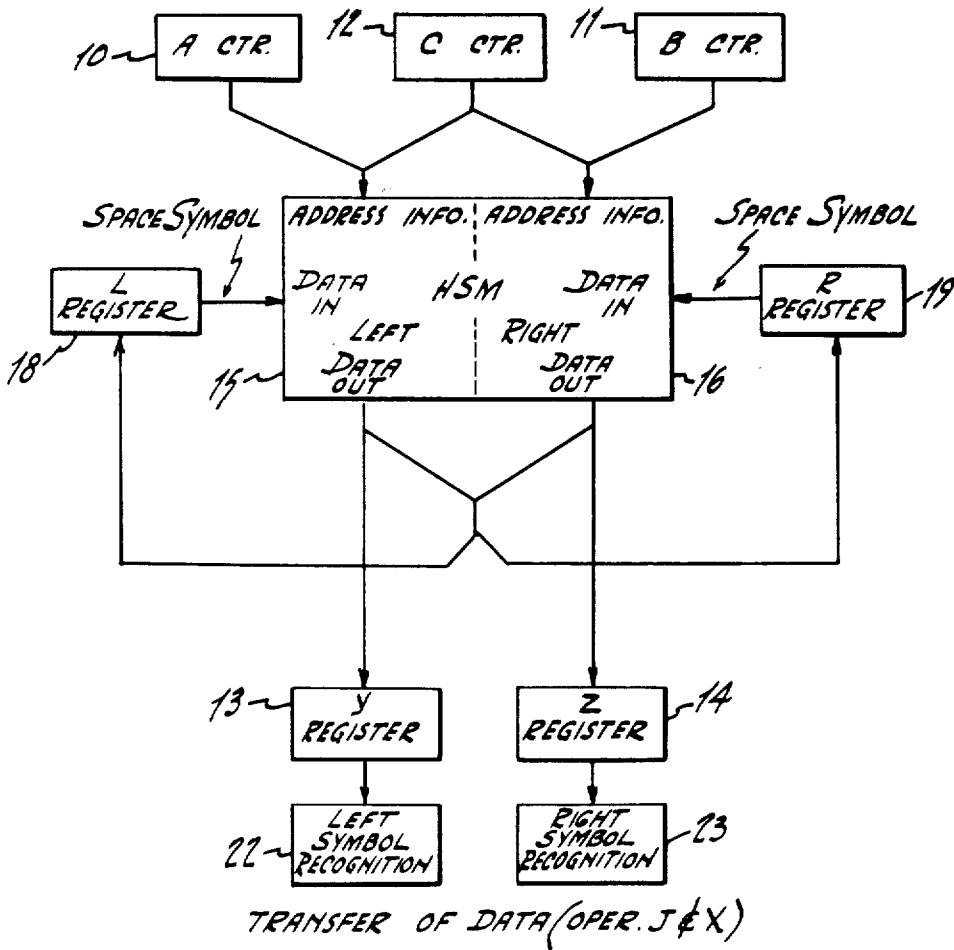
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Fig. 8.



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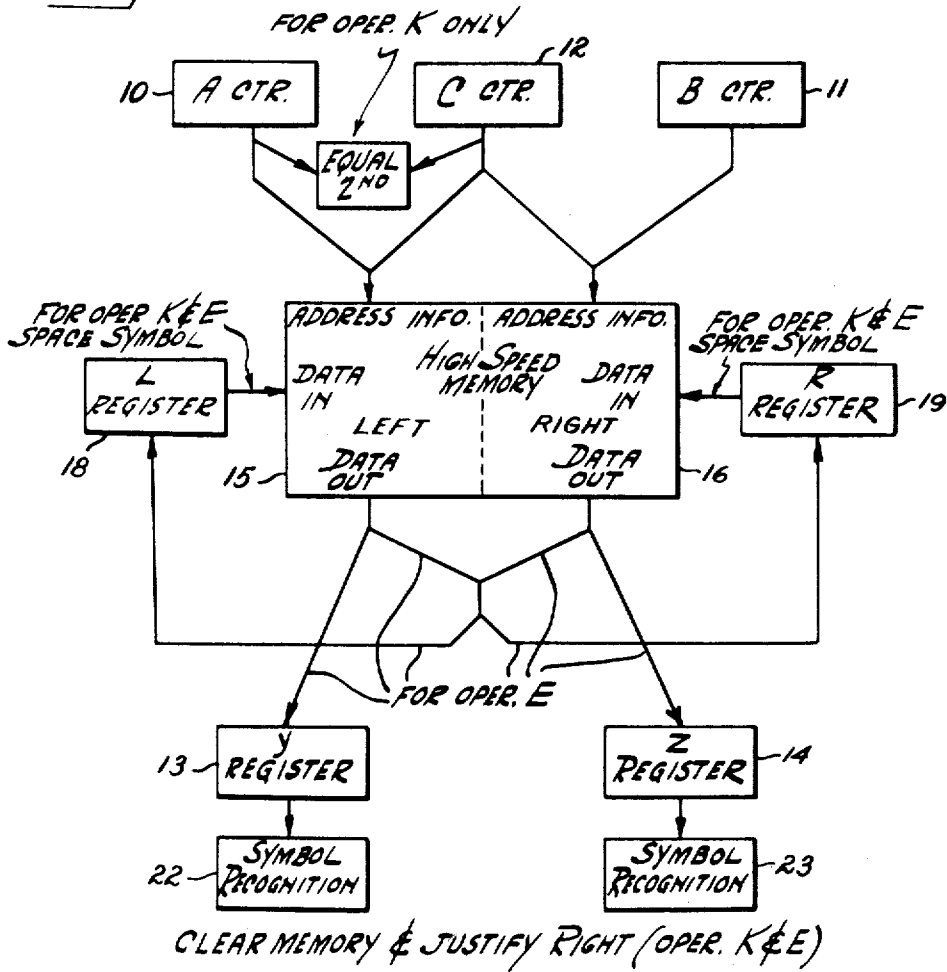
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Fig. 9.



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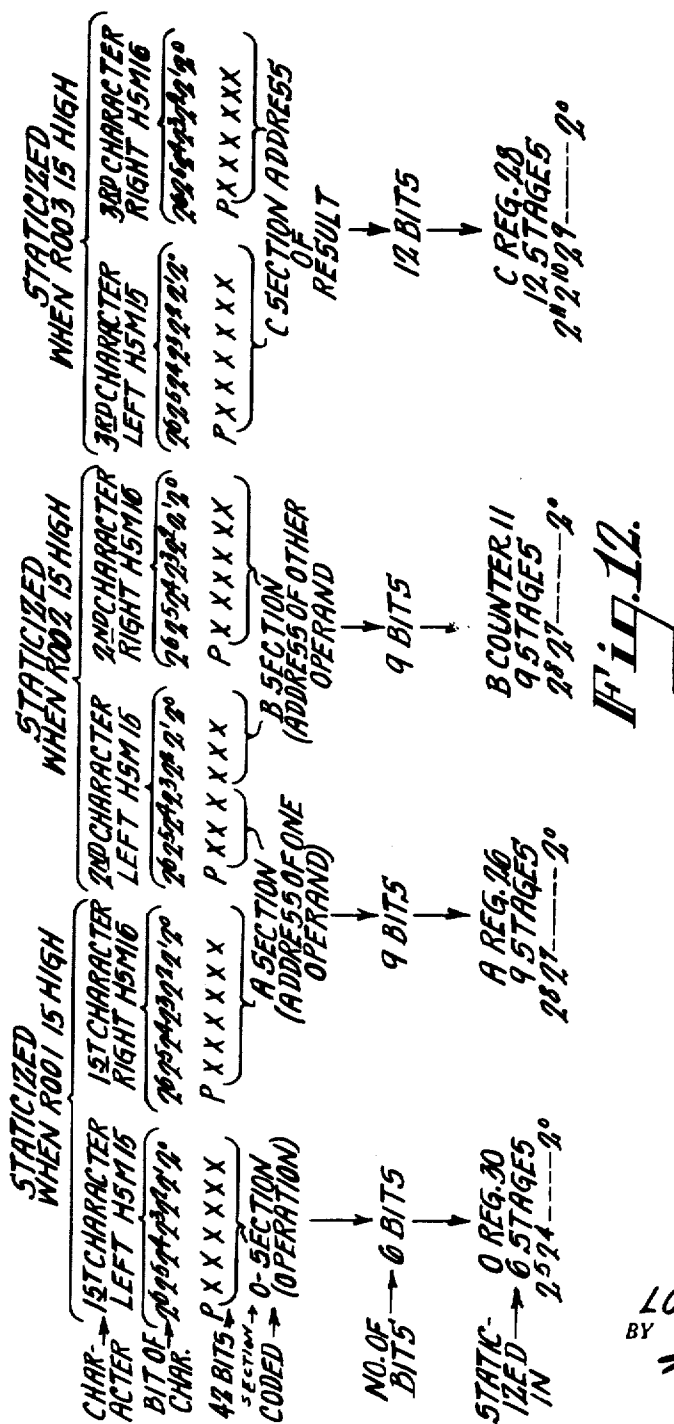
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3,118,055

Filed Dec. 28, 1954

47 Sheets-Sheet 42

Fig. 13.

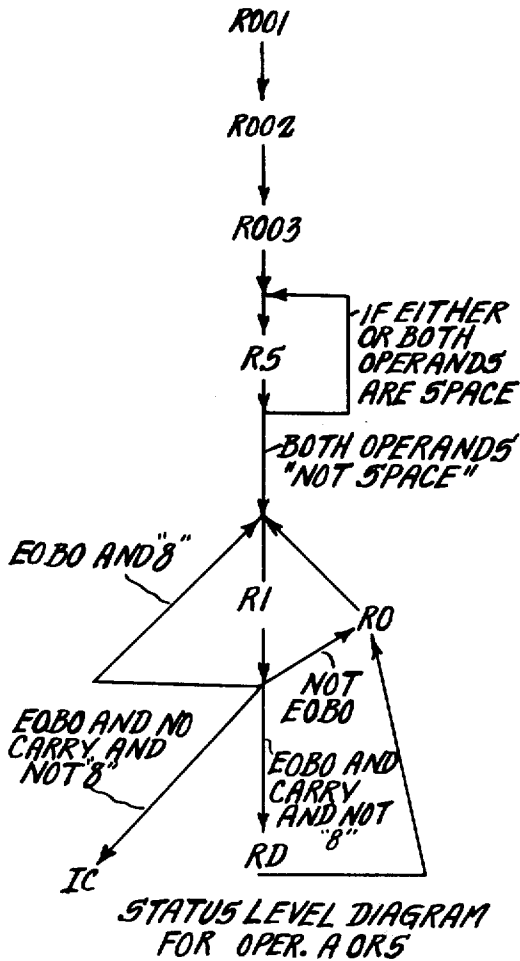


Fig. 15.

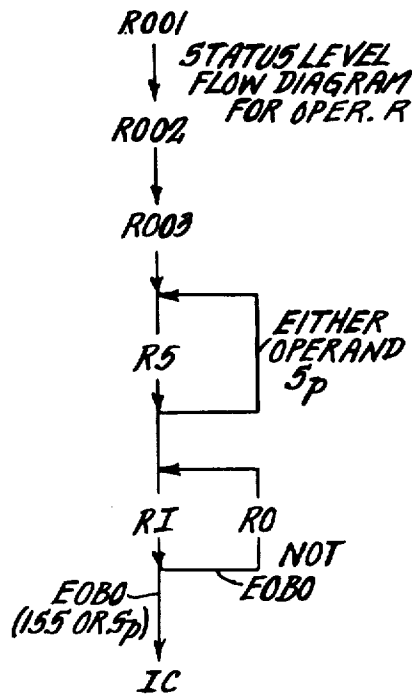
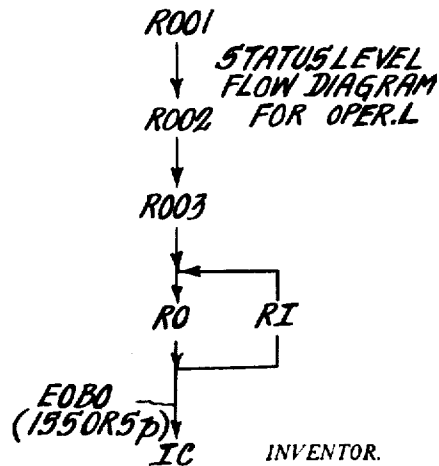


Fig. 16.



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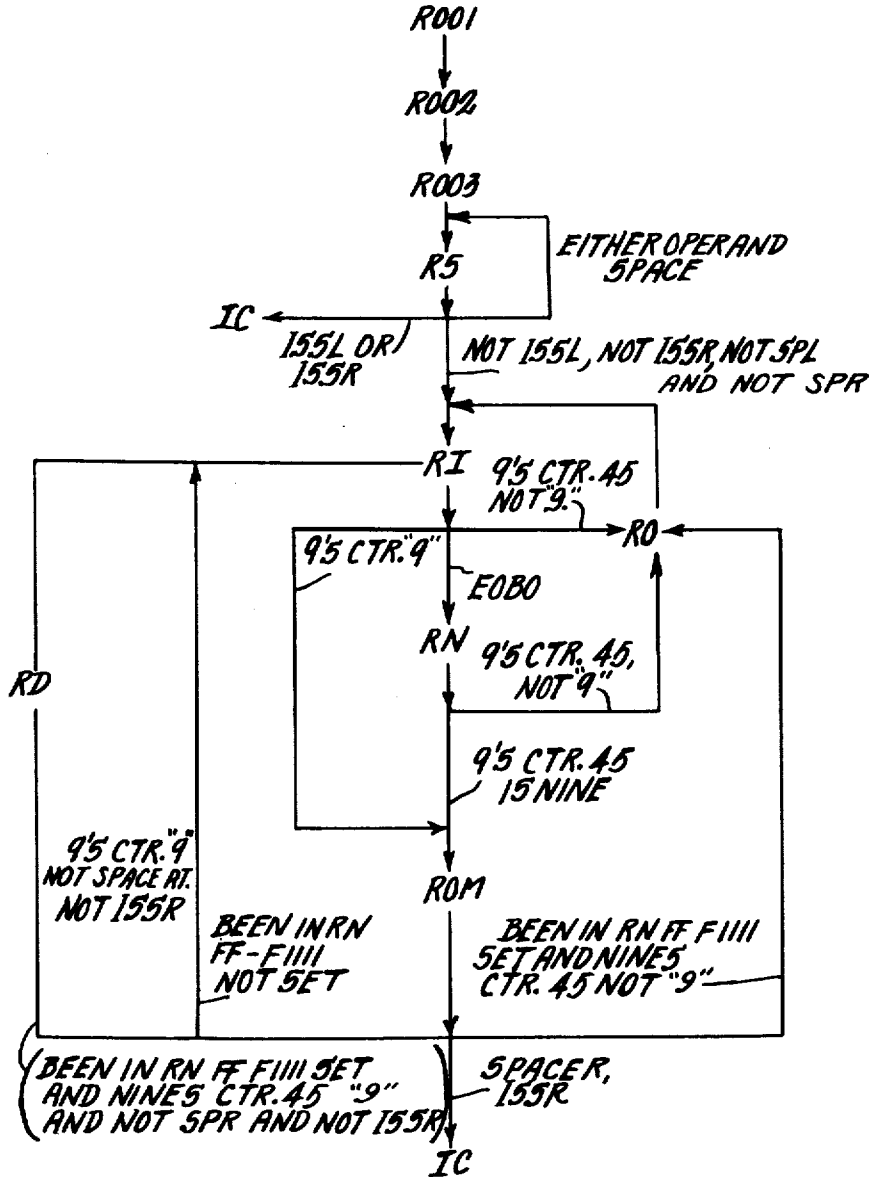
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47 Sheets-Sheet 43

Fig. 14.



STATUS LEVEL FLOW
DIAGRAM FOR OPER. M.

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47 Sheets-Sheet 44

Fig. 17.

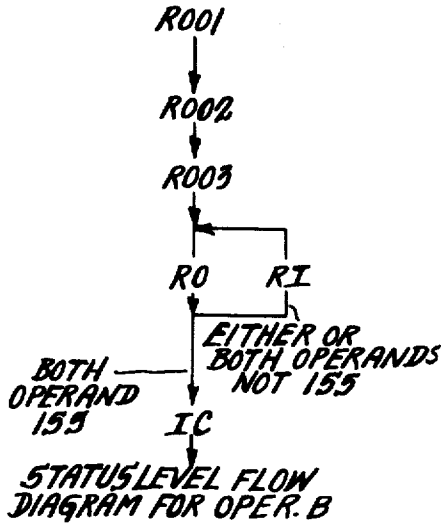


Fig. 19.

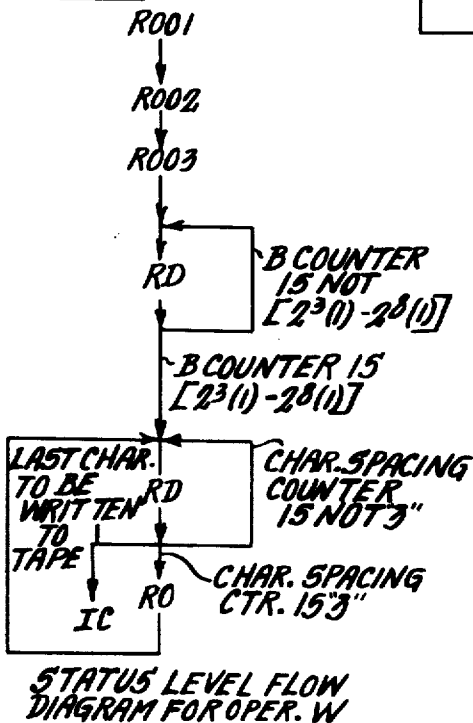


Fig. 20.

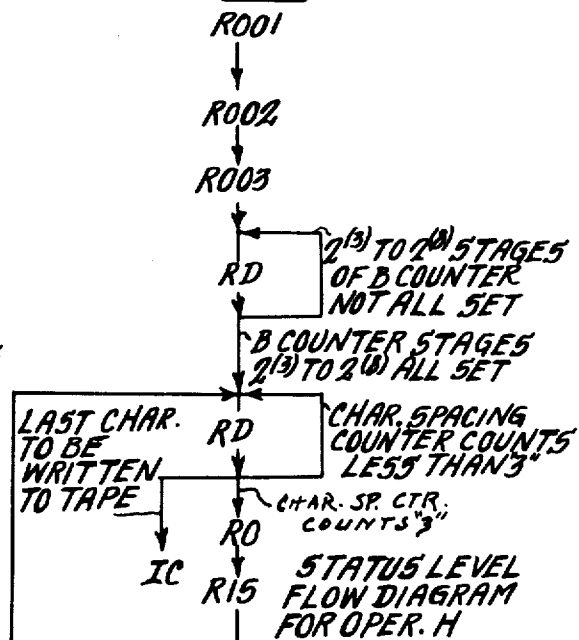
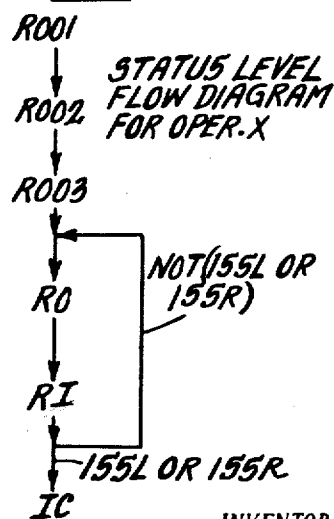


Fig. 21.



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BY

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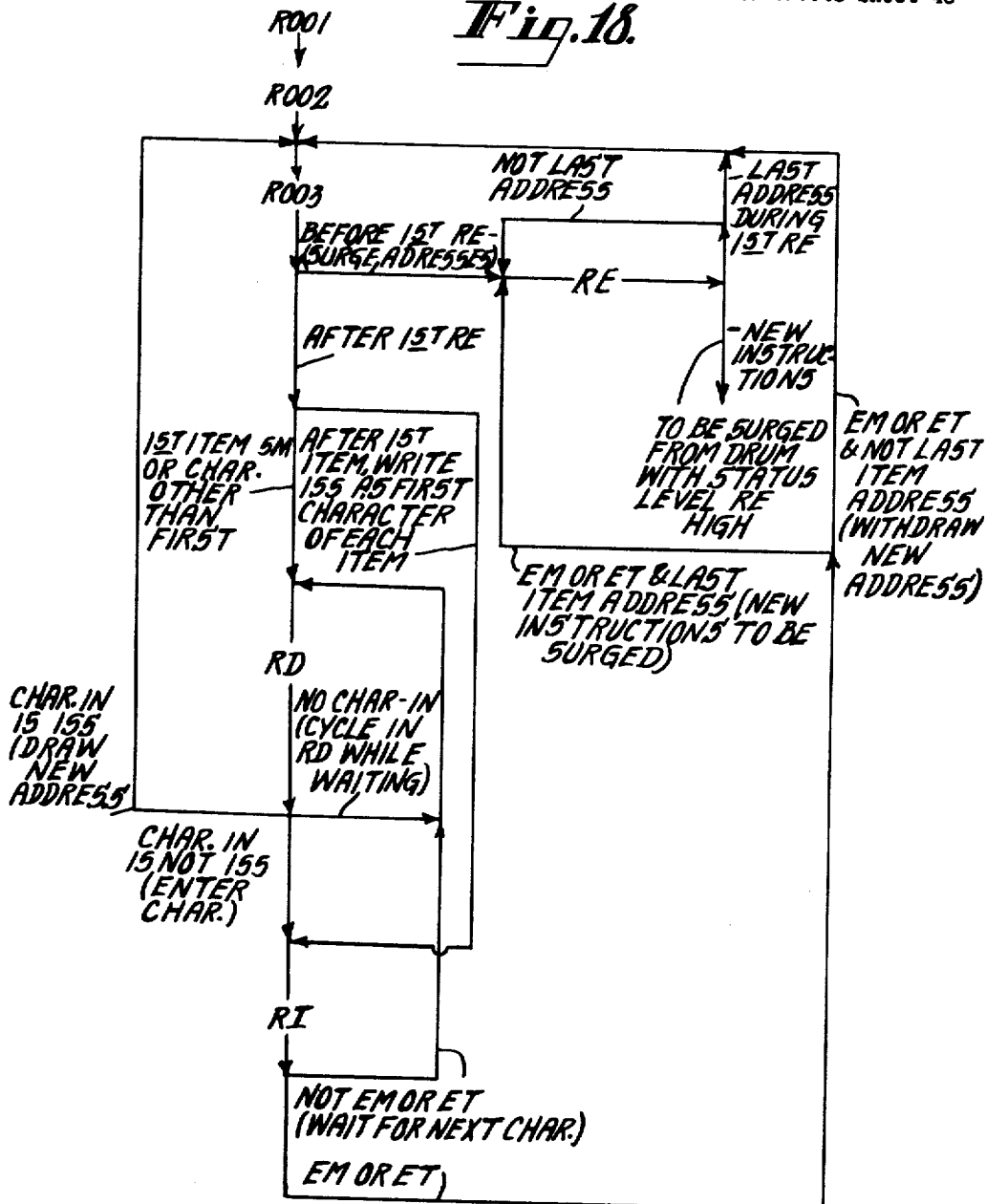
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47 Sheets-Sheet 45

Fig. 18.



STATUS LEVEL FLOW DIAGRAM
FOR OPER. N

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47 Sheets-Sheet 46

Fig. 22.

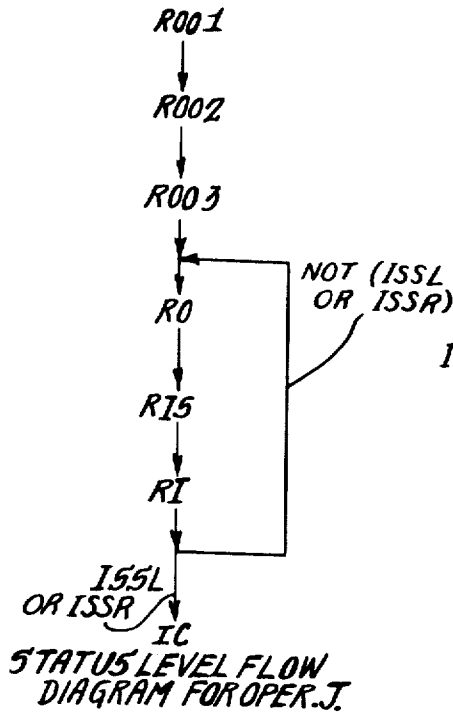


Fig. 24.

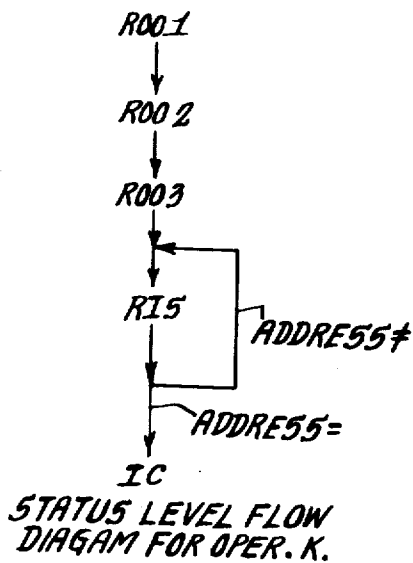


Fig. 23.

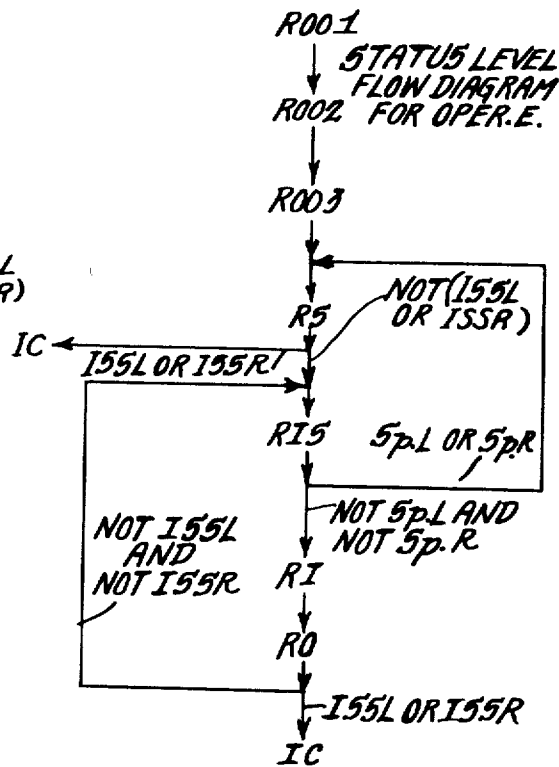
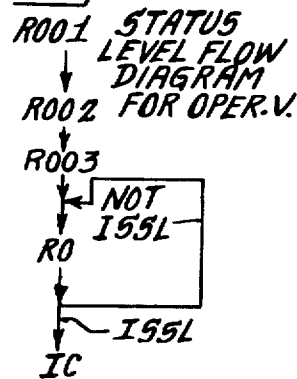


Fig. 25.



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3,118,055

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Fig. 26.

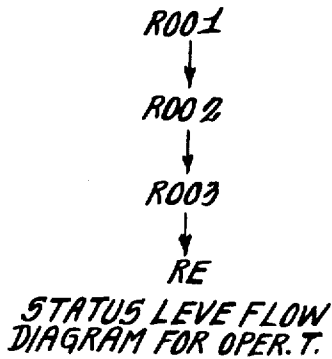


Fig. 27.

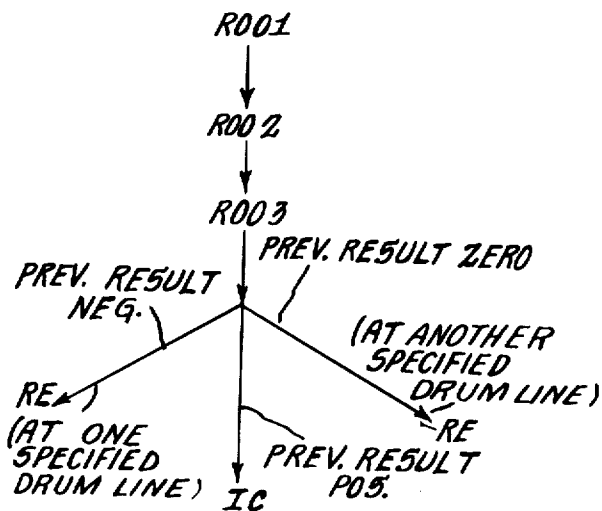


Fig. 28.

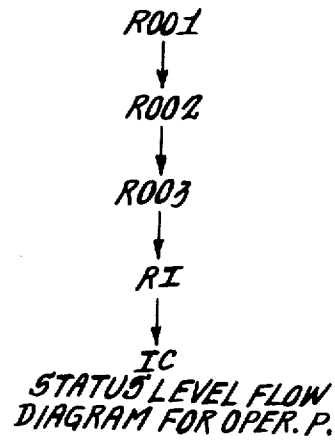
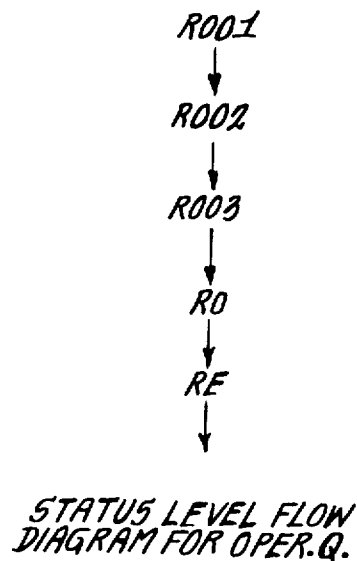


Fig. 29.



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ELECTRONIC DIGITAL INFORMATION HANDLING SYSTEM WITH CHARACTER RECOGNITION FOR CONTROLLING INFORMATION FLOW

5

Lowell S. Bensky, Levittown, Pa., assignor to Radio Corporation of America, a corporation of Delaware

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Table of Contents

Column

1. Introduction.....	4
2. General Considerations.....	8
2.1 Coding.....	8
2.2 Data on Tape.....	9
2.3 "Non-Standard Maximum" and "Variable" Item Lengths.....	10
2.4 Form of Data.....	10
2.5 Type of Data Item.....	10
2.6 Types of Storage.....	10
2.7 Internal Data Storage.....	11
2.8 Instruction Storage.....	11
2.9 Form of Instructions.....	11
2.10 Sequencing of Status Levels.....	11
2.11 Surging of Instructions.....	12
3. "Wired-In" Operations.....	13
3.1 Decimal Addition and Subtraction (Operations A and B).....	13
3.2 Decimal Multiplication (Operation M).....	14
3.3 Binary Addition and Subtraction (Operations B, L, and R).....	15
3.4 Read-In From Tape (Operation N).....	15
3.5 Write-Out To Tape (Operations W and H).....	17
3.6 Transfer of Data (Operations J and X).....	17
3.7 Justify Right (Operation E).....	18
3.8 Clear (Operation K).....	18
3.9 Verify (Operation V).....	18
3.10 Conditional and Unconditional Transfer of Control (Operations C and T).....	19
3.11 Set-Up and Refer (Operations P and Q).....	19
3.12 Stop (Operation F).....	20
4. The Computer In Detail.....	20
4.1 Major Components of the Detailed Diagram—Fig. 1.....	20
4.1.1 Magnetic Program Drum PD—Fig. 1(a-a).....	21
4.1.2 Program Counter PC—Fig. 1(a-a).....	21
4.1.3 Drum Counter DC—Fig. 1(a-a).....	21
4.1.4 Program Subcounter PSC—Fig. 1(a-b).....	21
4.1.5 Timing Pulse Generator TPG—Fig. 1(a-d).....	21
4.1.6 High Speed Memory (HSM) 15, 16—Fig. 1(c-c) and Fig. 1(d-e).....	22
4.1.7 L (for left) and R (for right) Registers 18 and 19—Figs. 1(b-c) and 1(d-e), respectively; and Y and Z Registers 13 and 14—Figs. 1(c-d) and 1(d-e) respectively.....	22
4.1.8 Operation Matrix OM—Fig. 1(b-a).....	23
4.1.9 A and C Registers 26 and 28—(Fig. 1(c-a)); O Register 30—Fig. 1(b-a); P Register 29—Fig. 1(d-a).....	23
4.1.10 A and C Counters 10 and 12—Fig. 1(c-b) and B Counter 11—Fig. 1(d-b).....	23
4.1.11 Left Symbol Recognition Circuits 22—Figs. 1(b-d), 1(b-e), and 1(c-e); and Right Symbol Recognition Circuits 23—Figs. 1(d-d) and 1(d-e).....	23
4.1.12 Nines Complementor 21—Fig. 1(e-d).....	23
4.1.13 Nines Counter 46—Fig. 1(f-a).....	23
4.1.14 Duplicated Adder 17A and Duplicated Binary to Coded Decimal Converter (BCDC) 17B—Fig. 1(c-b).....	23
4.1.15 Tape Handling Circuits 46—Fig. 1(b-c) and 1(b-d).....	24
4.1.16 Status Level Control Flip-Flops 47—Figs. 1(a-a); and Status Transition Gates—Figs. 1G and 1H.....	24
4.1.17 Alarm Circuits 48—Fig. 1(a-c).....	24
4.1.18 Parity Regenerator 44—Fig. 1(b-d).....	24
4.1.19 Previous Result Flip-Flops 49—Fig. 1(f-d).....	24
4.2 Staticizing Instruction.....	24
4.2.1 Staticizing Instructions—Status Level RO01 High.....	24
T1.....	24
T2.....	25
T4.....	25
T6.....	26
T8a.....	27
4.2.2 Status Level RO02 High.....	27
T1.....	27
T2.....	27
T6.....	27
T8a.....	28
4.2.3 Status Level RO03 High.....	28
T1.....	28
T2.....	28
T4.....	29
T6.....	29
4.2.4 Analysis of Staticized Instruction.....	30
4.3 Start of Machine and Generation of Timing Pulses.....	31
4.4 Surge of Instructions.....	35
4.4.1 Initiation of Surge of Instructions.....	35
T1.....	35
T2.....	35
T6.....	36
4.4.2 End of Surge Instructions.....	36
4.5 Typical Selection of New Status Level.....	39
4.6 Instruction Complete—Status Level IC High.....	40
5. Detailed Description and Operations of the Computer.....	40

Table of Contents—Continued

Column

5.1 Decimal Addition (Operation A)—Operation Level A High.....	41
5.1.1 Status Level RS High.....	41
T1.....	41
T2.....	42
T4.....	43
T6.....	43
T7.....	44
T8.....	44
T8a.....	46
5.1.2 Status Level RI High, First Cycle.....	46
T1.....	46
T1-4-T3.....	47
T3.....	50
T4.....	50
T6.....	51
T7.....	52
T8.....	52
T8a.....	52
5.1.3 Status Level RO High, First Cycle.....	53
T1.....	53
T2.....	53
T4.....	53
T6.....	54
T8a.....	55
5.1.4 Status Level RI High, Second Cycle.....	55
5.1.5 Status Level RO High Second and Succeeding Cycles, and End of Both Operands—Succeeding Digits—Two Item Separation Symbols (ISS's) and New Status Level.....	55
5.1.6 End of Both Operands, Status Level RI High.....	57
5.1.7 End of Both Operands and No Carry, Special Cases.....	58
5.1.8 Review of Decimal Addition, Positive Numbers—Sequence of Status Levels.....	60
5.1.9 Decimal Addition, Negative Numbers.....	61
5.1.9.1 End Around Carry or EAC.....	62
Case 1a Status Level RI High.....	63
Case 1b Status Level RD High.....	63
Case 2 Modified Nine and ISS and a Sum Nine.....	65
Case 3 Modified Nine plus Modified Nine and No Carry.....	67
Case 4 Modified Nine and Modified Nine and Carry.....	67
5.1.10 Operands of Different Lengths.....	68
Case a.....	68
Case b.....	68
Case c.....	69
5.1.11 Review of Decimal Addition and Sequence of Status Levels.....	69
5.1.12 Previous Results Circuits, Description.....	69
5.1.13 Previous Results Circuits, Operation.....	72
5.2 Decimal Subtraction—(Operation S)—Operation Level S High.....	73
5.2.1 Additional Circuits.....	73
5.2.2 Operation Level S High and Operation.....	74
5.2.3 Special Cases.....	75
5.3 Multiplication (Operation M)—Operation Level High.....	76
5.3.1 Additional Components.....	76
5.3.2 Detailed Operation.....	80
5.3.2.1 Status Level RS High.....	80
5.3.2.1a One or Both Characters.....	82
5.3.2.1b ISS Before Other Character.....	82
5.3.2.1c Non-Space Characters.....	83
5.3.2.2 Status Level RI High (For First Multiplier Digit Zero).....	83
5.3.2.3 Status Level RI High (For Non-Zero Multiplier Digit).....	84
5.3.2.4 Status Level RO High.....	85
5.3.2.5 RI-RO-RI Sequence.....	86
5.3.2.6 Status Level RN High (Renew Multiplier and Partial Product Address).....	86
5.3.2.7 Status Level ROM High.....	87
5.3.2.8 Status Level RD High.....	89
5.3.2.9 Status Level ROM High Again.....	89
5.3.2.10 Status Level RI High with a Zero Multiplier Digit After a Non-Zero Multiplier Digit.....	90
5.3.2.11 Completion.....	91
5.3.3 Sequence of Status Levels.....	91
5.3.4 Zeros in the Multiplier.....	93
5.4 Binary Subtraction, Right Hand Justification (Operation R) Operation Level R High.....	94
5.4.1 Description of Additional Components.....	94
5.4.2 Machine Operation—Binary Subtraction, Right Hand Justification.....	96
5.4.2.1 Status Level RS High.....	96
5.4.2.2 First Status Level RI High.....	96
5.4.2.3 Succeeding High Status Levels RO-RI.....	97
5.4.2.4 Special Cases.....	97
5.4.2.5 End of Both Operands.....	98
5.4.2.6 Condition of Previous Result Flip-Flops.....	99
5.4.2.7 Parity Regeneration.....	100
5.4.3 Sequence of Status Levels.....	100
5.5 Binary Subtraction, Left Hand Justification (Operation L) Operation Level L High.....	101
5.5.1 Status Level RO High.....	102
5.5.2 Sequence of Status Levels.....	103
5.6 Binary Addition (Operation B)—Operation Level B High.....	103
5.6.1 Status Level RO High.....	103
5.6.2 Status Level RI High.....	104
5.6.3 Succeeding Status Levels.....	105
5.6.4 Sequence of Status Levels.....	105
5.7 Read-In From Tape (Operation N)—Operation Level N High.....	106
5.7.1 Additional Components.....	106
5.7.2 Machine Operation—Read-In From Tape.....	112
5.7.2.1 Status Level RO01 High.....	112
5.7.2.2 Status Level RO02 High.....	112

Table of Contents—Continued

	Column
5.7.2.3 Status Level RO03 High.....	113
5.7.2.4 Status Level RE High—Start Surge of Ad- dresses.....	113
5.7.2.5 Address Surge—Status Level RI High.....	114
5.7.2.6 Continuation of Address Surge.....	114
5.7.2.7 Status Level RO03 High After Address Surge.....	116
5.7.2.8 Status Level RD High—Cycling.....	117
5.7.2.9 Status Level RI High—First Character From Tape.....	117
5.7.2.10 RD—RI Sequence.....	118
5.7.2.11 Status Level RD High—Item Separation Symbol (ISS).....	119
5.7.2.12 Status Level RO03 High—After ISS Recog- nition.....	119
5.7.2.13 Status Level RI High—Entry of Next Mes- sage Started.....	119
5.7.2.14 Negative Items.....	119
5.7.2.14.1 Status Level RD High—Minus Symbol From Tape.....	119
5.7.2.14.2 Status Level RI High—Negative Items From Tape.....	120
5.7.2.14.3 Cycling in RD—Digits of Nega- tive Item.....	120
5.7.2.14.4 Status Level RI High—Negative Item From Tape.....	120
5.7.2.14.5 Status Level RD High—ISS from Tape after Negative Symbol.....	121
5.7.2.15 Status Level RD High—Successive ISS's.....	122
5.7.2.16 Status Level RD High—End Message Sym- bol EM.....	122
5.7.2.17 Status Level RI High—After End of Message Symbol EM.....	122
5.7.2.17.1 EM or ET and Last Address.....	122
5.7.2.17.2 EM or ET and NOT Last Ad- dress.....	123
5.7.2.17.3 Status Level RO03 High—After Status Level RI High and After EM or ET and NOT Last Item Address.....	124
5.7.2.17.4 Status Level RI High—After Status Level RI High and After EM or ET and NOT Last Item Address.....	124
5.7.2.18 Status Level RI High with End of Tape Symbol.....	125
5.7.3 Sequence of Status Levels—Operation N.....	126
5.8 Write-Out to Tape (Operation W)—Operation Level W High.....	129
5.8.1 Additional Components.....	129
5.8.2 Detailed Operation—Write Out to Tape.....	132
5.8.2.1 Status Level RO02 High (staticizing).....	132
5.8.2.2 Status Level RO03 High (staticizing).....	133
5.8.2.3 Status Level RD High.....	133
5.8.2.4 Status Level RO High.....	134
5.8.2.5 Status Level RD High.....	134
5.8.2.6 Negative Numbers.....	135
5.8.3 Sequence of Status Levels.....	137
5.9 Write-Out to Tape and Clear (Operation H)—Operation Level H High.....	137
5.9.1 Additional Components.....	138
5.9.2 Detailed Operation.....	138
5.9.2.1 Initiating Operation.....	138
5.9.2.2 Status Level RIS High.....	138
5.9.3 Sequence of Status Levels.....	139
5.10 Transfer Data Within HSM 15, 16 (Operation X) Opera- tion Level X High.....	139
5.10.1 Additional Components.....	140
5.10.2 Detailed Operation.....	141
5.10.2.1 Status Level RO High.....	141
5.10.2.2 Status Level RI High.....	142
5.10.3 Sequence of Status Levels.....	142
5.11 Transfer and Clear Data Within HSM 15, 16 (Operation J)—Operation Level J High.....	143
5.11.1 Additional Components.....	143
5.11.2 Detailed Operation.....	143
5.11.2.1 Status Level RO High.....	143
5.11.2.2 Status Level RIS High.....	143
5.11.2.3 Status Level RI High.....	144
5.11.3 Sequence of Status Levels—Operation J.....	144
5.12 Justify Right (Operation E)—Operation Level E High.....	144
5.12.1 Additional Components.....	145
5.12.2 Detailed Operation.....	145
5.12.2.1 Status Level RS High.....	146
5.12.2.2 Status Level RIS High.....	147
5.12.2.3 Status Level RI High.....	148
5.12.2.4 Status Level RO High.....	148
5.12.3 Sequence of Status Levels.....	149
5.13 Clear (Operation K)—Operation Level K High.....	150
5.13.1 Additional Components.....	150
5.13.2 Machine Operation.....	150
5.13.3 Sequence of Status Levels.....	152
5.14 Verify (Operation V)—Operation Level V High.....	152
5.14.1 Additional Components.....	152
5.14.2 Machine Operation.....	152
5.14.3 Sequence of Status Levels.....	155
5.15 Transfer of Control (Unconditional) (Operation T) Opera- tion Level T High.....	155
5.15.1 Additional Components.....	155
5.15.2 Machine Operation.....	155
5.15.3 Sequence of Status Levels.....	156
5.16 Conditional Transfer of Control (Operation C)—Operation Level C High.....	156
5.16.1 Additional Components.....	156
5.16.2 Detailed Operation.....	157
5.16.2.1 Previous Result Positive.....	157
5.16.2.2 Previous Result Zero Positive.....	157
5.16.2.3 Previous Result Zero Negative.....	157
5.16.2.4 Previous Result Negative.....	158
5.16.3 Sequence of Status Levels.....	158
5.17 Set Up—Operation Level P High.....	158
5.17.1 Additional Components.....	153

Table of Contents—Continued

	Column
5.17.2 Machine Operation.....	159
5.17.3 Sequence of Status Levels.....	160
5.18 Refer (Operation Q)—Operation Level Q High.....	160
5.18.1 Additional Components.....	160
5.18.2 Machine Operation.....	161
5.18.3 Sequence of Status Levels.....	161
5.19 Stop (Operation F)—Operation Level F High.....	162
5.20 Various Alarm Circuits.....	162
6. Conclusion.....	163

I. INTRODUCTION

The present invention is related to information handling systems.

In information handling systems, for example, digital computers, the information to be handled is coded and stored. When a computer is designed for business use, the computations to be made are usually simple. Computations for business use are ordinarily restricted to addition, multiplication, subtraction, and occasionally division. However, the amount of information subject to the computations may be great. For example, in a day's transactions, charges (additions) may have to be made to hundreds of accounts. Thus, the situation is quite different from that found in digital computers for theoretical calculations, as in physics. In the computers designed for theoretical work, the information subject to computation, in most instances at least, is substantially less than those found in business problems. In theoretical work, the computer operations or computations may be long and complex, involving integration, differentiation, summation of series, and the like, or approximations thereto. Therefore, a large internal storage is desired. In business machines, the computations, although possibly repetitious, are simple. The information to be handled is extensive. Therefore, especially in business machines, a large external information storage is desirable.

One of the most efficient forms of external information storage is on tapes, either magnetic or punched. Where a large amount of information is to be stored, either on tape or otherwise, for business purposes, another problem is entering the information into the storage. The longer the entries, the greater the attention required of an operator and the greater are the chances for errors. Also, the difficulties of checking increase. For these reasons, it is desirable to minimize the length of each item (or group of characters) and to minimize the length of each message (or group of items). Accordingly, non-standard items or messages may be terminated when the information to be stored is completed without adding spaces and without standardizing item or message lengths. Further, non-standard message and item lengths provide a higher density of storage than may be achieved with standard lengths. Tests show that the average business item and message are appreciably less than the maximum. To provide a standard length to accommodate this maximum, therefore, would be wasteful of storage space, especially where tape memories or storages are used.

The use of non-standard item lengths in a standard type computer would involve conversion from non-standard to standard lengths in the computer. The results would then be reconverted for efficient tape storage. Such conversion and re-conversion would require extensive apparatus in addition to the computer proper, or a computer greater than needed for the computation itself.

Digital computers may be of the "serial" or "parallel" type. In the "serial" type of computer heretofore proposed, the operations are performed a digit or a character at a time, for example, in addition, starting with the least significant digit. In the performance of an operation serially, it has been usual, heretofore, to complete the operation for all possible entries of the operands in the registers involved. By way of example, consider an addi-

5

tion operation. The capacity of the registers (or memories) holding the augend and addend (the two operands) may be eight digits each. Assuming each operand to have a decimal point in a corresponding place, the operation is repeated for each digital place, starting from the least significant, for eight places. However, the numbers to be added may be three digit numbers each, or may have three characters, for example, in the hundreds. Then, for five or four (depending on whether a carry is required) digital places, the operations are superfluous and wasted. The computer is made to perform extra work. There is also a loss in computational time which may be trivial for one operation. Such loss of time may be serious when totalled over the thousands of operations which a modern computer may execute in the course of solving a single problem. This loss, however, may be neglected for the present, assuming that the computer nevertheless performs faster than information may be read from or applied to the tape.

Unfortunately, to employ one of the previous standard length item computers with a storage tape of non-standard message items involves an undesirable increase in internal random access memory within the computer. This increase is required so that each item may be stored, preparatory to a computation, in a register with enough storage spaces to receive the maximum length item. Similarly, provisions must be made for each maximum length message.

It is an object of the invention to provide a novel program control for an information handling system especially suited for non-standard length items.

Another object of the invention is to provide a novel program control for an information handling system of the serial type.

A further object of the invention is to provide a novel program control especially suitable for a computer of the serial type for non-standard length items.

A further object of the invention is to provide a novel method of operation for an information handling system of the serial type having greater flexibility and adaptability than heretofore available.

A further object of the invention is to provide a novel method of computer operation for operating arithmetically digit by digit, or character by character, or item by item, without operating on unused parts in the operands.

Another object of the invention is to improve the program control of an information handling system in the sequencing of the operations thereof.

According to one feature, the invention takes advantage of the character (or characters) which mark the end of items. The program control of the system is improved by selecting a succession of status levels in response to the operation being performed, the current status level, and the operand character upon which the computer is operating.

The status levels allow the use of sub-operation steps common to different operations. Thus new, or different, or modified operations having some sub-operations steps in common with those of some other operations are readily provided, without extensive equipment additions. Moreover, the sequential selection of such steps responds, in the system of the invention, also to the operand characters, for example to terminate an operation as the end of the operand or operands is reached. By means of suitable status transition gates, the proper sequence of status levels for any operation is obtained. Hence, for a new or different operation employing a new or different sequence of sub-operation steps, additional status transition gates provides the proper sequencing. Even if a new sub-operation is required for the performance of the new operation, advantage may be taken of the already available sub-operation steps by proper sequencing by the status transition gates.

6

Note that the invention contemplates a sub-programming by sub-operation steps digit by digit, or character by character. However, this sub-programming is preset or predetermined for each operation the computer performs. By thus following the instructions item by item or character by character, with the sub-operation steps, depending upon the characters, and possibly the previous sub-operation steps, the operation may be ended after all the significant digits of the operands have been operated upon. Thus the program control of the computer is increased in efficiency, as no time is wasted in operating on unnecessary characters.

The feature of the invention just described may be described in another way. On selection of an instruction to be performed, one of a set of operation levels (or leads) is selected to be at an enabling level. The selected operation level, in conjunction with the status levels and the operand or operands, controls the machine to perform the instruction. The operands are operated upon character by character. On recognition of the end of both operands, where such recognition is required, or on whatever other occurrence indicates completion of the operation, the appropriate status transition gate passes the final timing pulse to select an "instruction complete" level. Again, by suitable status transition gates, the next status level selected may be one withdrawing a new instruction from the machine memory, or surging new instructions into the machine memory, or terminating the operations, as circumstances may require.

An important feature of the invention resides in the employment of certain status levels and status transition gates. A gate is a logical "and" circuit. The computer internally generates cycles of timing pulses (sometimes called clock pulses) applied to the various status transition gates, as well as to other gates throughout the system. A status transition gate passes a final pulse of a sequence of pulses to select a status "level." A "level" refers to a particular one of two possible voltage levels or voltage values on a lead with respect to the reference voltage or ground of the system. The voltage on a lead is bivalued, in conformity with binary or Boolean algebra. When speaking of a level as "selected," in common with engineering parlance, the meaning is that that lead is selected to be an enabling level for a gate, or to pass a signal through an "or" circuit. Thus a level may be considered as a binary unit of information, that is, a "bit." On leads carrying the coded characters, in the present machine, a high level is taken as the enabling level, and when carrying information, as a binary "one."

On conclusion of a sequence of timing pulses, the same status level is retained as the selected one, or another status transition gate, "primed" or enabled by the then current status level or the equivalent, or by another level, passes the final pulse of a sequence of timing pulses, to cause selection of the succeeding status level, etc. These status levels then control a sub-operation step during an operation, as already mentioned. The high level is taken throughout as an enabling level when applied to gates, or to pass "or" circuits. However, either the high or low of the levels could be employed for the purpose.

As an example of the use of sub-operation steps and the status levels, consider the operation of addition as performed in this machine. On selection of an operation level corresponding to addition, a first status level may cause a search of the memory for the least significant digit of each of two operands. When both are encountered, a second status level may be selected to cause the first digit of each operand to be read out and staticized in registers. Then a third status level is selected to cause the two digits to be added and stored again in the memory. Next the second and third status levels are selected in sequence for succeeding operand digit char-

acters. Finally, when the addition is complete, and the ends of both operands are reached, a final status level is selected to cause a new instruction to be withdrawn or new instructions to be surged. Note that the second status level, for example, may well be useful as a sub-operation step in common with other operations.

Another feature of the invention employs certain circuits which detect the results of the handling of information by the machine, and uses these results to control or determine the sequence of the programming thereafter.

Another feature of the invention resides in the detection and setting up in a circuit of a determination of a previous mode of operation, and using the output of the circuit to control the sequence of status levels. For example, a flip-flop or bi-stable circuit may be used so that its state indicates whether the machine, during the course of a particular operation, has, or has not, selected a particular status level. The succession of status levels may be controlled in part by the status of this flip-flop.

The system described has advantageous and novel features which afford flexibility of program control and programming of a type especially useful in accounting. Note that a different transition gate and a different status control level is, in many cases, selected for each cycle of timing pulses. This feature assists in the desired digit by digit or character by character operation.

Certain other important features of the present invention are more fully disclosed hereinafter. Further, certain features described herein are also described in certain other applications, as follows:

Title: Information Handling Device. Inventors: Ivan H. Sublette, Arthur D. Beard, Lowell S. Bensky (the present applicant), Linder C. Hobbs, and Stephen M. Filebrown, Serial No. 478,022; now Patent No. 2,877,446, issued March 10, 1959;

Title: Digital Computing Systems. Inventors: Lowell S. Bensky, and Ivan H. Sublette, Serial No. 478,098; now Patent No. 3,023,964, issued March 6, 1962;

Title: Digital computing Systems. Inventors: Edward J. Schmitt, and James G. Smith, Serial No. 477,975; now Patent No. 3,023,963, issued March 6, 1962; all filed concurrently herewith.

The foregoing and other objects, advantages, and novel features of the invention will be more fully apparent from the following description, when read in connection with the accompanying drawing, in which like reference characters refer to similar parts, and in which:

FIG. 1, comprising the thirty sheets from FIG. 1(a-a) to FIG. 1(f-e), each sheet being designated by one of the combinations of a first letter from a to f inclusive (identifying the column for these assembled sheets), a second letter from a to e inclusive (identifying the row for these assembled sheets, and the two further sheets designated FIG. 1G and FIG. 1H (those leads of which interconnect with the remainder of FIG. 1 being suitably labeled) is a schematic diagram, in block form, of a computer according to the present invention;

FIG. 2 is a highly abbreviated block diagram illustrating the control of the computer of FIG. 1 by the operation levels and status levels mentioned above;

Each of FIGS. 3 to 11 inclusive, is a highly abbreviated schematic diagram showing the flow of information between certain major units of the computer for various computer operations;

FIG. 12 illustrates in a diagrammatic way the flow of information in staticizing an instruction in the computer of FIG. 1; and

Each of FIGS. 13 to 29, inclusive, is a status level flow diagram showing, for a different computer operation, the sequence of status levels as tabulated below:

Tabulation of Status Level Flow Diagrams
Figs. 13-29, Inclusive

Fig.	Operation	Letter Designation for Corresponding Operation and Operation Level
13	Decimal Addition (A) and Decimal Subtraction (S).	A and S
14	Multiplication	M
15	Binary Subtraction—"right hand justification."	R
16	Binary Subtraction—"left hand justification."	L
17	Binary Addition	B
18	Read-in from Tape	N
19	Write-out to Tape	W
20	Write-out to Tape and Clear	H
21	Transfer Data within HSM 15, 16	X
22	Transfer Data and Clear	J
23	Justify Right	E
24	Clear	K
25	Verify	V
26	Unconditional Transfer of Control	T
27	Conditional Transfer of Control	C
28	Set-up	P
29	Refer	Q
No status level flow diagram included.	Stop	F

2. GENERAL CONSIDERATIONS

2.1 Coding

In this computer, a seven-bit, alpha-numeric code is employed for the data which is to be transmitted from one unit of the system to another. Six of these bits, called "information" bits and providing sixty-four possible combinations, are used to designate the ten numerals, the twenty-six letters, and other special symbols, any one of which is called a character. A character may be defined as a letter, digit, or symbol. A character also may be defined as a pattern of binary digits representing a letter, digit, or symbol. A character may be represented by a pattern of binary-valued electrical pulses or voltages. The seventh bit in each of these coded characters is a parity bit chosen as 1 or 0 to make the total number of 1's in each character even. Checking for this "evenness" (parity check) at various points in the system guards against errors—transient and otherwise. In the ten numerals, the four least-significant digits code the decimal values into binary equivalents (binary coded decimal).

The following code table provides an example of a code which may be used:

CODE TABLE

Character	Code
Minus zero	0 000 000
Space	1 000 001
Space minus	1 001 001
Numerics:	
zero	1 010 000
one	0 010 001
two	0 010 010
three	1 010 011
four	0 010 100
five	1 010 101
six	1 010 110
seven	0 010 111
eight	0 010 100
nine	1 011 001
Minus	0 001 001
Alphabetics:	
A	1 100 000
B	0 100 001
C	0 100 010
D	1 100 011
E	0 100 100

CODE TABLE—Continued

Alphabets:—Continued

Character		Code
F-----	1	100 101
G-----	1	100 110
H-----	0	100 111
I-----	0	101 000
J-----	1	101 001
K-----	1	101 010
L-----	0	101 011
M-----	1	101 100
N-----	0	101 101
O-----	0	101 110
P-----	1	101 111
Q-----	0	110 000
R-----	1	110 001
S-----	1	110 010
T-----	0	110 011
U-----	1	110 100
V-----	0	110 101
W-----	0	110 110
X-----	1	110 111
Y-----	1	111 000
Z-----	0	111 001
Item Separation Symbol-----	0	111 100
Item Separation Symbol Minus-----	0	111 001
Start Message-----	1	111 110
End Message-----	1	111 101
End Data-----	1	111 011
Quote-----	1	000 010
Dollar Sign-----	1	000 100
Comma-----	1	001 110
Period-----	1	011 010
Apostrophe-----	0	000 011

2.2 Data on Tape

Magnetic tape is the external storage medium used to carry and retain data throughout the system. The data is recorded on magnetic tape either by an input operator using one of several known input devices. Successive characters are recorded serially along the tape, spaced approximately 100 per inch. The tapes are intended to move past read or write heads at 100 inches per second. Characters are received from reading heads or presented to writing heads every 100 microseconds. The seven bits of each character are recorded across the width of the tape so that these seven bits are handled simultaneously by seven read or seven write heads. This series-parallel handling of characters is present on incoming magnetic tapes to the computer and is also maintained on outgoing tapes from the computer.

For the present example it is assumed that:

- (1) a group of characters and a special symbol known as an item separator symbol (abbreviated ISS) make up an item; and
- (2) a group of items comprise a message with a special symbol, start message (SM), at the beginning of the group, and a special symbol, end message (EM), at the end of the group.

The structure, or item arrangement, of messages in a particular tape, are preferably constant throughout the tape. For example, the first item in each message of the tape carries the same information, as the customer's account number in a billing operation; the second item of each message may indicate amount due from the customer; and similarly for other items in the messages. To minimize various operation times and computer storage requirements, the number of characters per item (item length), the number of items per message (message length), and the number of messages per tape have not been standardized.

2.3 "Non-Standard Maximum" and "Variable" Item Lengths

For use in further discussion of the computer two definitions which differentiate between two types of variation in item lengths are accepted. Each item (sometimes called a word) in a message has an assigned maximum length equal to one more than the maximum number of characters this item can ever have, the extra character is an item separator symbol (abbreviated ISS). For example, $7+1=8$ characters would suffice in billing to the nearest cent when amounts are \$9999.99 (the decimal point is not written in) or less. In a like fashion, all the items in a message are assigned maximum lengths which depend on the item usage. Since these assigned maximum lengths are not necessarily equal, the phrase "non-standard maximum" item lengths is used to connote the variation in maximum lengths of each of the items of a message. Flexibility and resulting economy in data handling is carried one further step. Recalling the example above of an eight-character maximum item length for billing to the nearest cent of amounts less than \$100,000, it is evident that the actual number of characters needed in a particular billing can range from one (ISS alone) up to the maximum of eight. Item lengths on tape in the present system are the actual lengths needed, with no extra blanks or spaces inserted to fill out the assigned lengths to the maxima. To connote the variation in length of a given item in a group of messages, the phrase "variable" item length is used. In the present system both variable and non-standard maximum item lengths are used.

2.4 Form of Data

Series-parallel handling of data is used on the magnetic tapes in this system. Registers enable transformations in time, where desired, from sequential flow of information characters to simultaneous flow; and in space, from one information flow path to parallel paths or to a single path.

2.5 Type of Data Item

The present computer avoids transformation of the input data to standard length items, and avoids a waste of high-speed memory stage. Original analysis has shown that the maximum item lengths in business usages are considerably longer than the average item lengths.

The use of a variable, non-standard maximum item length in the computer, with a search for the least-significant digit and an end-of-operand indication, is employed to save considerable time and memory space.

2.6 Types of Storage

For purposes of discussion, storage devices may be divided into two groups: cyclic and static. Cyclic storage devices are those which allow retrieving of stored information or the writing of new information to be stored only at prescribed instants, which may occur periodically at a fixed rate. For instance, information written onto a magnetic drum reappears at the reading station once every drum revolution. By the same token, writing information on a specified section of a rotating magnetic drum is possible once every revolution. An acoustic delay line with output connected to input is another example of a cyclic memory device.

Static memory devices accomplish storage spatially rather than in time, as in cyclic devices. Spatial coordinates serve to identify the section of the memory to be written into or read-out of. For instance, an electron beam can be positioned electrostatically on a special storage surface to read or write information at a given point on this surface. An array of flip-flops, radecchons, type SB-256 tubes, and magnetic core arrays are examples of static memories. Again, from this brief description, handling of variable length items in static devices ordinarily is simpler than in cyclic memories. Basically, this greater

simplicity is attributable to the random access possible in static devices.

2.7 Internal Data Storage

Because of adaptability to variable item length, rapid random access, and convenience when used in conjunction with magnetic tapes, a static form of storage for data internally of the computer is employed. Radechon, SB-256 memories, or magnetic core arrays may be employed to advantage. A random access, high speed memory (HSM) is used illustratively, as more fully described hereinafter.

2.8 Instruction Storage

As the system is applied to cyclic accounting problems, the same program may be used repeatedly for many batches of input data, thus diminishing the effects of loading information, new programs, etc. into a cyclic memory. A magnetic drum memory is employed for instruction storage. Access time is reduced over normal drum access time by surging the instructions, briefly explained in sec. 2.11 and more fully hereinafter.

2.9 Form of Instructions

As has been mentioned previously, instructions contain the information necessary to control the manipulation of data items from and to magnetic tapes and within the computer. Control circuitry serves to interpret these instructions by converting the information contained in an instruction into control voltages and pulses distributed to activate the several parts of the computer at proper times during the instruction execution. This control is more fully described hereinafter.

The form for most instructions is a coded three-address instruction. Two addresses specify high-speed memory locations of the operands entering into the operation, and a third address specifies the high-speed memory location for storing the result of the operation. The third address allows storage of the result of arithmetic operations at desired places in the high-speed memory, eliminating the need for a maximum length accumulator.

To take full advantage of a three-address instruction code in this asynchronous, serial machine, the three addresses together with the operation code are staticized, or stored in suitable registers. Since characters are to be handled serially, the memory address staticizers are counters which may be preset and then increased by one as each successive character of an item is handled. In the use of a three-address code, from the standpoint of the time necessary per operation, it is desirable that two operands, such as the addend and augend in an addition, be simultaneously available. In the present machine, the high speed memory is divided into two banks, left and right, with each bank independent of the other. The two operands are then simultaneously available where desired, as in addition, by taking one operand from each memory bank.

2.10 Sequencing of Status Levels

To operate serially with items of variable, non-standard length both within the computer as well as in the input and output equipment, a selective sequencing of status levels of the computer, cycle by cycle of clock pulses, is provided. Each cycle consists of a sequence of sub-operation steps upon a single character of an item as needed.

FIG. 2 is a highly abbreviated block schematic illustrating control of the computer by the instructions. The timing track pulses of a program drum PD are applied as synchronizing pulses to a timing pulse generator TPG. A high-speed memory (HSM) 15, 16 has a portion employed as a surge tank to receive the coded instructions from the program drum PD. The coded instructions, as called for, are staticized in a register 9 of various gates, registers, and counters. The output of this register controls the operations level selection circuits, a matrix OM.

Status transition gates STG, indicated in FIG. 2, are provided having outputs applied to status level selection circuits 60. A status transition gate typically receives inputs from certain flip-flops, character recognition circuits, status levels, and the last timing pulse of the cycle. The various registers and flip-flops may also be employed for the temporary storage of information.

A large number of gates among the circuits 9 are under the control of the operation levels, the status levels, the timing pulses, and a set of character recognition circuits CH, and the timing pulses from the timing pulse generator TPG. These gates of circuits 9 control the flow of information between the computer input and output (from tapes) and the arithmetic unit, in this case an adder 17.

In operation, the operation levels, the status levels, and the outputs from the recognition circuits CH jointly with the timing pulses control the circuits 9 and thus effect the program control, that is, control the flow of information within the computer. Timing within each cycle is provided by a series of pulses from the timing pulse generator, TPG. Most of the timing pulses are, for example, one-microsecond each. Each cycle of timing pulses is synchronized with the timing track upon the magnetic program drum PD. The timing pulses are distributed as clock pulses throughout the machine. All other inputs than timing pulses are considered "levels," which are considerably longer than a clock pulse, for example, the 20-microsecond status levels.

A selected operation level is high for any selected operation. A 20-microsecond status level is also applied to the various circuits 9 appropriate to the execution of the given operation or portion thereof. The operation levels, status levels, and outputs from the recognition circuits determine the sequence, that is, the selection, of successive status levels. Sometimes this sequence is modified by the nature of the preceding sequence of status levels. At the end of a status level, the succeeding particular status level is selected by a clock pulse or timing pulse passed through one of the status transition gates STG. A particular status transition gate is typically "primed" by one or more operation levels, by the current status level, and by an input directly or indirectly from the recognition circuits. The sequence of the status levels may depend on the prior sequence during the instruction execution, which, however, depends on the nature of the operand or operands. Only one status level is "selected" or "high" at a time (except for the brief transition period). The next status level is selected to be high in accordance with the state of the machine as determined by the operation level selection circuits OM, the current status level, and various internal conditions which may be staticized in flip-flops; (for example, end of both operands). This mode of operation involving successive status levels amounts to wired-in rules for transitions from one status level to another, these rules being consistent with the execution of a given instruction. However, the rules may be flexible to allow a different sequencing for different operands.

Thus, any given operation usually involves a series of status levels. The length of the series of status levels is determined by the operation and by the lengths (and sometimes the nature) of a given set of variable-length operands. Therefore, execution time of an instruction is variable, and the machine operates asynchronously with respect to a specific program, or instruction, depending on the operand or operands.

After the execution of any instruction, a new instruction is withdrawn from a section (surge tank) of the memory by a sequence of certain status levels. As the new instruction is staticized, the operation level selection circuits OM, select the new operation level, as called for by the new instruction.

2.11 Surging of Instructions

The instructions are entered in the surge tank, either initially or after all have been withdrawn, by a surge as

described in the patent to Bensky and Beard, No. 2,679,638. In the method of instruction surging, a block of several instructions is read from the drum at one time, and stored in a section (called the surge tank) of the internal static memory. The instructions are then withdrawn for execution as needed until exhausted, whereupon a new surge, if required for the program, takes place. Thus, without attempting an exact definition, a "surge" may be defined, for the purposes of the present application, as the withdrawal from a drum or other cyclic memory of a group of character signals as they are read, without the intervention of other extraneous steps by the machine and in time sequence, for storage in a random access memory.

The effectiveness of surging in reducing drum access time depends, among other things, upon the sequential use of all the instructions surged. It may be desired to execute the entire list of instructions sequentially as written on the drum and surged into the memory only conditionally. It is possible that a portion of the surged instructions may not be used. Conditional and unconditional transfers of control, more fully described hereinafter, make available to the programmer program branch points so that the computer may deviate from the sequential execution of the program instructions. At a branch point, the next instruction to be executed may not be in the surge tank in which event another surge starting at the next desired instruction may be employed. The surge is described in greater detail hereinafter.

3. "WIRED-IN" OPERATIONS

3.1 Decimal Addition and Subtraction (Operations A and B)

Decimal addition and subtraction is included as a wired-in operation. By a "wired-in" operation is meant one in which an entire instruction to perform that operation is executed in response to a single coded entry in the machine, so that additional programming is not necessary. "End-around" carry and the nines-complement system, is employed.

With reference to the abbreviated diagram of FIG. 3, counters 10, 11 and 12 are provided having their outputs applied to the high speed memory (abbreviated HSM) having left and right banks 15 and 16. The counters are connected to the addressing circuits of the HSM 15, 16. The outputs from the left and right HSM 15 and 16 are connected respectively to registers (designated Y and Z) 13 and 14 respectively. The outputs of the Y and Z registers 13 and 14 are applied to a duplicated adder and binary to binary-coded decimal converter 17. The output of the duplicated adder and binary to binary-coded decimal converter 17 is applied to an L register 18 and to an R register 19. The output of the L register 18 is applied to the data input of the left HSM 15 and the output of the R register 19 is applied to the data input of the right HSM 16. The outputs of the L and R registers 18 and 19 are also compared in a comparator 20. Left and right symbol recognition circuits 22 and 23 are connected respectively to the outputs of the Y and Z registers 13 and 14.

In decimal addition or subtraction, the first phase of the operation is a search for the least significant digits of the operands. This search is made because all operands are "justified left" as they are read into the high speed memory (HSM) 15, 16, while the address specified in the instruction is that of the least possible significant digit of the variable-length item. The search is performed by addressing the memory from the A and B counters 10 and 11 and reading out successive characters to the Y and Z registers 13 and 14. Addition is now performed by repeated cycles of read-out of operands from the HSM 15, 16 as addressed by the A and B counters 10 and 11; and passing the operands through the duplicated adder and binary to binary-coded decimal converter 17. The sum is entered in both the left and right (L and R) regis-

ters 18 and 19. The sum in the L register 18 and the R register 19 (from the different duplicated adder and converter 17) is compared in the equality comparator 20. If no error has been made, the sum is read into the memory 15, 16 at the address specified by the C counter 12. As will appear more fully hereinafter, the sum is stored only in one of the left or right HSM 15 or 16. Symbol recognition circuits left and right, 22 and 23 respectively, for the Y and Z registers 13 and 14, respectively, recognize the symbol for the end of operand. Upon recognition of an end of operand symbol in both operands, the operation is terminated, with suitable provision for the carry, if any.

Subtraction resembles addition, except that the subtrahend is always located in the right bank 16 of the memory. Also, the subtrahend is read through a nines complementor 21 after which it is treated as an augend and added to the minuend.

3.2 Decimal Multiplication (Operation M)

Multiplication involving negative numbers is not included in the wired-in instructions. On the other hand, ordinary decimal multiplication, involving only positive numbers, is wired-in the computer. Round-off is left to programming as is algebraic multiplication. Decimal multiplication is accomplished by repeated additions and shifts. Note that division is not included as a wired-in instruction. Division may be accomplished by programming suitable operations.

With reference to FIG. 4, means are provided (a nines counter 45) for recording the number of additions which have been made. The nines counter 45 is set from the complementor with the complement of each multiplier digit, and the "overflow" of the nines counter later recognized. In order that repeated serial additions may be made, A and C registers 26 and 28 are employed for restoring the addresses of the least significant digits of the operands—multiplicand and partial product—in the addressing counters after counting away from these addresses to perform the serial addition.

The first phase of the multiplication operation is a search for the least-significant digits of both operands, the multiplicand and multiplier. The multiplicand is always located in the left bank of the memory. The multiplicand is addressed by the A counter 10. The multiplier is always located in the right bank of the memory 16 and is addressed by the B counter 11. The least-significant multiplier digit is read through the nines complementor 21 to the nines counter 45; thereby the nines counter is preset with the nines complement of the multiplier digit. When the least significant digits of both operands have been located, the first series of additions is begun. The multiplicand is added to the partial product (normally zero at the start) located in the right bank 16 of the HSM (the right HSM) and addressed by the C counter 12, by means of successive cycles of read-out and read-in, digit by digit, as in decimal addition, until the end-of-item symbol of the multiplicand is recognized. The resulting sum is read back into the partial product location as addressed by the C counter 12. When the end of the multiplicand is recognized, the nines counter 45 is increased by one and a check is made for overflow (when the nines counter reaches 9). If no overflow has occurred, a further addition is necessary. The A and C counters 10 and 12, however, have been increased during the previous addition and are now returned to their original addresses. This original address information is stored in A and C registers 26, 28. The original addresses are now read into the A and C counters 10, 12 respectively. A number of additions is performed until the nines counter 45 overflows. At this point, a new multiplier digit is read from the right HSM 16 of the memory through the nines complementor 21 into the nines counter 45. In effect, a shift is now accomplished by increasing by one the address of the least-significant digit of the partial sum and setting the C regis-

15

ter 28 and the C counter 12 with this increased address. A new series of additions is now performed until the nines counter 45 again overflows.

A shift is again accomplished and another series of additions begins. This process of adding until the nines counter overflows, shifting and adding again, proceeds until an end of operand symbol is recognized during the multiplier read-out. Upon such recognition, the operation is terminated. The product is now found in the HSM 15, 16 with the least-significant digit at the address (stored in the C counter 12) of the original multiplication instruction.

3.3 Binary Addition and Subtraction (Operations B, L and R)

In order fully to handle items made up of alpha-numeric characters of the code employed, certain arithmetic operations over and above the decimal operations mentioned above are included. For instance, the alphabetical arranging of a list of names or stock numbers involves subtractions with alpha-numeric characters. Primarily for such alphabetical listing, binary subtraction with "left hand justification" is included as a wired-in instruction, and requires little additional equipment. Further, only little more equipment provides binary subtraction with "right hand justification" and binary addition. These three binary operations are more fully explained hereinafter. A further use of these instructions is the modification of original program instructions, mainly for the purpose of modifying the addresses of these instructions. These addresses may be considered as alpha-numeric characters and therefore are not ordinarily handled by the decimal operations.

The binary operations wired into the computer thus facilitate comparisons and also facilitate the modification of instructions within the high-speed memory. All six information-carrying bits of the characters are operated upon; negative operands are not permitted.

With reference to FIG. 5, in binary addition (Operation B) and binary subtraction with left hand justification (Operation L), there is no search for the least significant digit; spaces are admissible characters. Binary addition is performed by repeated cycles of reading out a single pair of characters from the memory as addressed by the A and B counters 10 and 11, to the Y and Z registers 13 and 14. The characters are read through only one adder 17a of the duplicated adder to the L and R registers 18 and 19. The contents of either the L or the R input register 18 or 19 is then read into the appropriate left or right bank of the memory 15 or 16 as addressed by the C counter 12. The six-bit adder 17a, however, is not duplicated. Therefore, the comparison in comparator 20 between the memory input L and R registers 18 and 19 serves only to check the transfer from the single adder 17a to the L and R registers 18 and 19. The operation is terminated by the recognition of end of operand symbols in both Y and Z adder input registers 13 and 14 by the left and right recognition circuits 22 and 23. In the operations of binary addition and subtraction B and L, the only admissible end of operand symbol is the ISS.

In binary subtraction with right hand justification (Operation R), spaces are not admissible characters in an item and a search for the least-significant digit is necessary. A space as well as an item separator symbol serves as an end of operand symbol. The necessary complementing for the subtraction operations B or L, is effected by taking the subtrahend input from each "zero" terminal of flip-flop stages of the Z register 14, which is a flip-flop register.

3.4 Read-In From Tape (Operation N)

By the operations read-in from and read-out to tape, messages of "raw" data from magnetic tapes are entered into the computer internal memory and messages

16

containing final data are removed from the computer memory to magnetic tapes in an efficient manner.

Missing items in a message on tape may be:

- (1) represented by two consecutive item separator symbols; or
- (2) entirely absent if part of a consecutive group of items at the end of a message.

Density of storage is thus enhanced. In either case, discontinuous placement of items during read-in (a new memory location for the start of each item coming from tape) is provided.

Negative items in the computer are represented by a coded minus sign followed by the nines complement of the positive magnitude. On the tape, negative numbers maintain the form of a minus sign followed by a positive magnitude. Two input and two output tapes are used in the illustrated embodiment.

The computer is provided with a feature for random composition during read-in of data from the magnetic tape. By virtue of this feature, each item may be read into any address of the memory 15, 16 as specified by the program. The items of a message are read into the memory sequentially. With reference to FIG. 6, the address information is first surged into the memory from the magnetic drum in a manner similar to that used in the surge of instructions. This address surge is the first phase of the read-in operation. The tape is then started. When an ISS, which precedes an item, is read into the Y register 13 from the tape, it is recognized. The memory 15, 16 surge tank section is then addressed by the program subcounter PSC to withdraw an address from the surge tank of the HSM 15, 16 from those addresses which were previously surged into the section. The address stored in the memory 15, 16 surge tank is entered in the C counter 12. The item separator symbol is now read from the L and R registers 18 and 19 into one or the other left or right HMS 15 or 16 of the address now in the C counter 12, to complete the cycle.

The computer then waits for the next character to be read to the Y register 13 from the tape and then reads this next character into the left and right registers 18 and 19. The count in the C counter 12 is decreased one to determine the place to store the new character in the Y register 13, to complete another cycle. These cycles continue until another ISS is recognized in the Y register 13 by the left symbol recognition circuit 22. The program subcounter PSC then addresses the memory to withdraw a new address for this item. The next surge tank address is entered into the program subcounter PSC. The item address is entered in the C counter 12, and the fore-going procedure is repeated.

The procedure is repeated until an end message symbol is recognized in the Y register 13 by the left symbol recognition circuit 22. No further characters then are read from the tape and the tape is stopped. If all the addresses required by the program have not been used, a further feature artificially reads ISS into each of the remaining addresses. When the last address of the group of addresses surged in from the drum is recognized, in a manner to be described hereinafter, the operation is terminated.

All items which are preceded by a minus sign are read from the Y register 13 through the nines complementor 21 into the L and R registers 18 and 19 and, thence, to the memory. Therefore, negative numbers are stored in their complemented form. Since no spaces are recorded on the tape when items are of less than their maximum allowable length as determined by the program, all items which are read from the tape are stored in the memory with left hand justification.

At the end of the operation, the new instruction surge is started by entering the drum line for the start of the surge into the program counter PC from the C register

8, where this first instruction drum line was recorded as part of the operation instruction.

3.5 Write Out to Tape (Operations W and H)

In writing to tape, two memory addresses are specified, one where read-out is to begin (in the C counter 12) and the other where read-out is to end (in the A counter 10). All characters including spaces between the two addresses are then read to tape.

With reference to FIG. 7, in addition to the components already described, a second "equal" circuit 35 is provided which may be connected between the A and C counters 10 and 12. A character spacing counter 34 is also provided having an output which controls the time of writing each character on the tape, and thus the character spacing on uniformly moving tape. Successive characters are read from the memory 15, 16 as addressed by the C counter 12 to the Z register 14. From the Z register 14 the characters are recorded on an output tape, each at a time determined by the state of the character spacing counter 34.

When a minus sign is recognized in the Z register 14 by symbol recognition circuit 23, succeeding characters are read from the memory 15, 16 through the nine's complementor 21 to the Z register 14, until an item separator symbol is recognized in symbol recognition circuit 23. Therefore, negative numbers which have been stored in their complemented form are now read out in their true representation, preceded by a minus sign.

The C counter 12 is advanced one count for each character read out. An indication from the second equal circuit 35 of equality of contents of the A and C counters 10 and 12 causes the operation to terminate. Use of the operation H rather than the operation W, causes the area in the memory from which the data has been read, to be cleared to spaces. This clearing is accomplished in a positive manner by following each character read-out by a read-in of the space symbol to the same address.

3.6 Transfer of Data (Operations I and X)

Note that transfer of data may be programmed using one of the addition operations to add the desired item to zero and place the result in the location to which it is desired to transfer the original item. However, wired-in transfer of data instructions are provided for the convenience of the programmer with little additional equipment over that already provided for other purposes. The principal components are already provided.

A transfer-and-clear operation (Operation J) is included to simplify transferring an item out of one place and clearing this location. Transfer-and-clear (Operation J) is an instruction especially useful when the problem being solved is cramped for high-speed memory space.

With reference to FIG. 8, transfer of data is accomplished by successive cycles of reading-out from and read-in to the HSM 15, 16. The item address during read-out is supplied from the C counter 12. The item is read out to both the L and R registers 18 and 19. The item is also read out into either the Y and Z registers 13 or 14, respectively, depending on whether the item came from the left or right HSM 15 or 16. The contents of the L or R registers 13 or 14 are then read into the left HSM 15 or the right HSM 16 at the new address. During read-in, the memory 15, 16 is addressed from the A or B counters 10 or 11. The operation is terminated when an item separator symbol is recognized in the Y or Z registers by symbol recognition circuits 22 and 23.

Two types of transfer are provided; one in which the location from which the data has been read is not cleared (Operation X) and one in which the location from which the data has been read is cleared (Operation J).

Clearing is accomplished by following each read-out with a read-in of a space symbol to the location from which the character has just been read.

3.7 Justify Right (Operation E)

If, for some reason, the programming of a shift in either direction by a specified number of digits is desired, it may be simply accomplished by using the transfer and clear operation. The operation justify right shifts a variable length operand to the right end of the space allotted to the maximum length this operand could occupy, and is very useful in the present machine. This operation, justify right, is difficult to program using wired-in instructions and at the same time occurs fairly often in accounting routines. For instance, when a number is originally written into the system, it is justified left, for example, .372 - - - - . The dot at the middle of the line represents an ISS. When this same number passes through the computer to an output tape in preparation for printing, in a column of figures where right hand justification is wanted, the justify right order is more desirable. By this instruction, the right hand justification may be accomplished before the read-out.

With reference to FIG. 9, the A and B counters 10 and 11 are set to the specified address and a search for the least significant digit is instituted by reading successive characters from the memory, as addressed by the A or B counters 10 or 11, to the Y or Z registers 13 or 14. As the characters are read out of the memory, they are also read into both the L and R registers 18 or 19. As long as spaces are read out, each read-out is followed by a read-in of a space symbol to the same address.

When a non-space character is recognized in either the Y or Z registers 13 or 14, by symbol recognition circuits 22 and 23, that character, which also is stored in the L and R registers 18 and 19, is read into the memory as addressed by the C counter 12 to the space first addressed. The cycle then proceeds with read-out addressed by the A or B counters 10 or 11, read-in of a space to that address, and read-in of the character just read-out to the memory location addressed by the C counter 12 advanced one in count, etc. Recognition of an item separator symbol in the Y or Z registers by symbol recognition circuits 22 or 23 terminates the operation.

3.8 Clear (Operation K)

The computer memory employed in this computer, in the process of writing new information into locations destroys previously stored information at those locations. In writing the corresponding items in successive messages into the same memory locations, in the system herein disclosed, a shorter item written over a longer item (both having the same maximum length) does not obliterate (that is, erase) part of the longer item. The clear operation before writing accomplishes this erasure. Although the clear operation may be programmed using instructions otherwise provided, only few additional components provide the clear operation as a wired-in instruction.

In order to insure a more positive clearing operation, the "clear" instruction clears to space symbols.

With reference to FIG. 9, in executing the instruction for clear (Operation K), the characters or entries between any two specified addresses is cleared to spaces. Normally the clear operation is the first instruction of a program. The beginning address is specified in the C counter 12 and the ending address in the A counter 10. The memory is addressed from the C counter 12 and the space symbol read into this location. The C counter 12 count is increased by one, the memory is addressed again, and the space symbol read into the succeeding location. This cycle continues until an equality is recognized between the A and C counters 10 and 12 in the second equal circuit 35. The operation clear is then terminated.

3.9 (Verify Operation V)

The verify instruction facilitates program checks.

With reference to FIG. 10, two addresses are specified in the A and B counters 10 and 11 and the correspond-

ing two characters are read-out of the HSM 15, 16. After entry in the L and R registers 18 and 19 respectively, the two characters are compared in the first equal circuit 20. If the two characters are identical, the instruction is continued by proceeding to similarly compare characters at succeeding addresses. If the characters compared are not identical, an alarm is given and the machine stops. The operation is terminated on reading two ISS's.

3.10 Conditional and Unconditional Transfer of Control (Operations C and T)

In order to exploit fully the power of high-speed large-scale digital computers, it is desirable to include the decision-making functions usually referred to as conditional transfer of control. In the phrase "transfer of control," "control" refers to the sequencing of the computer operation by instructions of a program one after the other. By the inclusion of the operation of conditional transfer of control, the computer may make a decision regarding the instruction which is to control the next computer operation, this decision depending on the result of a previous computation. The conditional transfer of control allows a modification in the sequence of executing these instructions, on the basis of a specified criterion. The criterion in this machine, is the sign of the result of a previous operation. Depending upon whether a given arithmetic operation produces a negative, positive, or zero result, the succeeding instruction is taken from one of three possible paths. There are two paths, or sequences of instructions, out of the original program sequence, and one path following the original sequence.

There may be a loss in efficiency of surging due to the branch points generated by the transfer of control. This loss may be reduced by proper programming. If the path which most probably is to be followed is made the straight-through path, that is, the same sequence as though there were no transfer of control, the surge is as effectively used as the statistics of the problem allow. Further, if the programmer arranges to have the conditional transfer of control the last instruction in a surge group, the effectiveness of surging is little, if any, reduced, even for the two paths leading to instructions out of the original line.

Unconditional transfer of control is included as a wired-in instruction. In the execution of unconditional transfer of control, the sequence of instructions is interrupted to jump to a specified instruction. The jump or interruption is independent of the results of a previous operation.

With reference to FIG. 11, a transfer of control is accomplished by surging a new group of instructions into the surge tank of the HSM 15, 16. The drum line address information is read from the high-speed memory 15, 16 and staticized, and transferred to the program counter PC. The new surge is initiated beginning with the drum line specified in the program counter PC.

In unconditional transfer of control (Operation T) there is only one setting of the program counter PC determined by the information stored in the C register 28. In conditional transfer of control (Operation C) there are two ways of setting the program counter PC, either from the A register 26 and the three most significant digits of the B counter 11, or the C register 28. One of these two ways is selected based on information as to whether the previous result is zero or negative. In addition, if the previous result is positive, the program counter PC count is not altered, and the program proceeds as though the operation for conditional transfer of control had not intervened. Consequently, there are three possible instruction paths available after a conditional transfer of control, one of which is a normal continuation and two of which are transfers to new parts of the program.

3.11 Set-up and Refer (Operations P and Q)

A pair of instructions respectively called set-up and refer, are included to allow the entering of a subroutine,

that is, a minor sequence of instructions, from any place in a main routine (that is, the main sequence of instructions) and returning to any place in the main routine after having completed the subroutine. The use of subroutines in this manner may save considerable instruction storage by enabling the repeated use of the same subroutine readily at several points along the main routine. To utilize a subroutine in a program, a means of entering a subroutine and, upon completion of the subroutine, returning to the main program is provided. The set-up and refer instructions are designed to fulfill this function.

The set-up instruction (Operation P) is used to store within the HSM 15, 16 the program line which is to be used following the completion of the subroutine.

Referring to FIG. 11, the instruction set-up is staticized by setting an address for one character in the A counter 10 and an address for the other character in the B counter 11. The characters representing the program line are set into the C register 28. From the C register 28, one character is read to the L register 18 and one character to the R register 19. These two characters are then read into the locations specified by the A and B counters 10 and 11 respectively. The desired storage is thereby accomplished.

The "refer" instruction (Operation Q) specifies the same two addresses used in a previous set-up instruction (Operation P). The characters are read-out from the memory 15, 16 to the program counter PC, and a new instruction surge is begun. Control is thus returned from the subroutine to the desired program. Thus, for example, one subroutine may be used many times within a program by using the set-up and refer instructions.

3.12 Stop (Operation F)

The machine is stopped by this instruction. It may be started, as described hereinbefore (and in greater detail hereinafter) to staticize the next instruction.

4. THE COMPUTER IN DETAIL

4.1 Major Components of the Detailed Diagram—FIG. 1

FIG. 1 is a complete diagram of the computer and shows, in block form, substantially all the gates, flip-flops, registers, and other components required to execute all the operations of this machine. The thirty sheets of FIG. 1(a-a) to FIG. 1(f-e) may be assembled in a rectangular array, with the first letter of the pair in parenthesis indicating the column position of that sheet, and the other, second letter, the row position. It is helpful to trim the sheets so that those leads in register at the margins between sheets intended to be continuous join each other as nearly as possible without hiatus. Some of the lines may have to be extended to join in a way which will be apparent after assembly. The interconnections of FIG. 1(a-e), showing the status level control circuits, and of FIG. 1G and 1H showing the status transition gates, each with the other sheets of FIG. 1, are indicated by labelled leads.

A few drafting conventions are peculiar to this diagram. Arrowheads converging at the center of a small circle indicate an "or" circuit. "Or" circuits are described, for example, in "High Speed Computing Devices" by Engineering Research Associates, published by McGraw-Hill Book Company, Inc., 1950, for example, at pp. 44-45. Many "gates" are shown in block form with an inscribed G (or G's for a plurality of gate). These gates are all logical "and" circuits unless otherwise specified. "And" circuits are described in different publications, for example, the volume just cited, at pp. 37 et seq. Some "or" circuits are shown in rectangles, and when so shown the rectangle is suitably labelled. A D.C. (direct current) inverter is indicated by a rectangle inscribed with an I. Multiple signal lines are usually indicated with dotted lines.

In the drawing, the "one" (1) and "zero" (0) are Boolean tags given to the output of the set and reset ter-

minals, respectively, of a binary device or circuit which is here typified by flip-flops (that is, bistable multivibrators). A flip-flop may assume the set condition by application of a pulse on its set or "S" input terminal, or may be triggered to the set condition by a pulse on a trigger or T terminal. The flip-flop may assume its other, or reset, condition, by a pulse on its reset or R terminal. The convention adopted herein is that, if the flip-flop is set, the "one" output voltage is higher than the "zero" output voltage, but if the device is reset, the "one" output voltage is lower than the "zero" output voltage. This convention accords with that generally adopted by the art. Further the higher output voltage is often referred to as being "high" since it is then at the higher or more positive voltage of its two stable voltages. A different convention may be adopted, if desired, consistent with Boolean algebraic circuits.

The major units are described below, and their location on FIG. 1 of the drawing is indicated for each one. Familiarity with these locations increases the ease of following the detailed description. Note again that in FIG. 1, the sheets designated with two letters appended in parentheses are to be paid in rows and columns, and the first letter indicating the column and the second letter indicating the row. If the sheets are suitably trimmed, and thus laid, with their length horizontal, the lines extending to other sheets join. Note also that certain lines are indicated as the same, or as bearing the same signal, without being extended across the schematic, to save confusion. The outputs from the status transition gates of FIGS. 1G to 1H, inclusive, are applied to certain inputs of FIG. 1(a-e), which shows the status level selection circuits. The outputs from FIG. 1(a-e), including all the status levels, are suitably labelled, rather than being extended to the many places on the remainder of FIG. 1 which receives the status levels.

4.1.1 Magnetic Program Drum PD—FIG. 1(a-a)

This drum carries the programs which have been selected for particular groups of messages on one or more magnetic data tapes. The drum PD contains 16 tracks: A reset track has a fiducial pulse recorded thereon from which the count of lines recorded on the drum is taken. A timing track on the drum is used in the generation of the timing pulses. The drum has two sets of tracks on each of which are recorded, in lines, characters of seven bits each. The seventh bit of each character is a parity bit.

4.1.2 Program Counter PC—FIG. 1(a-a)

The program counter holds a binary number which indicates the drum line of the instruction next to be executed, and is advanced in count as the instruction is withdrawn. It is also employed for recording the drum line number for a new surge of instructions.

4.1.3 Drum Counter DC—FIG. 1(a-a)

The drum counter counts the lines on the magnetic drum PD as they pass under the read heads. The count in the drum counter DC is usually equal to the number of the next drum line about to pass under the drum reading heads.

4.1.4 Program Subcounter PSC—FIG. 1(a-b)

The program subcounter PSC counts the number of instructions being surged, so that the surge is stopped at the proper time. It also counts the number of instructions staticized so that the machine "knows" when it needs a new surge. Its count is used to address the HSM 15, 16 during the surge and during instruction staticizing as explained hereinafter.

The three counters just described (PC, DC, and PSC) may be binary counters made up of flip-flop stages.

4.1.5 Timing Pulse Generator TPG—FIG. 1(a-d)

This generator includes a group of gates and flip-flops.

Its function is to generate timing pulses for use throughout the machine. Timing pulses are designated by the prefix T. There are eight timing pulses T1 to T8, equally spaced in time, and others. The relative position of the timing pulses in a cycle is identified by the number following the prefix. Thus T1½ indicates a timing pulse occurring after the first timing pulse T1, by a time one half the time between the first timing pulse T1 and the second timing pulse T2 of the cycle. The timing pulse generator is indicated by a dotted line enclosure on FIGS. 1(a-d) and 1(a-c).

4.1.6 High Speed Memory (HSM) 15, 16—FIG. 1(c-c) and FIG. 1(d-c)

There are two blocks 15 and 16 representing the internal, high-speed memory. Each block represents a bank of seven memory matrices. Each matrix is a plane array capable of storing 512 bits. Thus, the left HSM 15 (FIG. 1(c-c)) has a storage capacity of 512 seven-bit characters. So also has the right HSM 16 (FIG. 1(d-c)) a capacity of 512 seven-bit characters. Each of the locations of the 512 characters has an address number so that a particular character may be stored at a specified location in the HSM 15, 16. Such memory devices, as with magnetic matrices, are known. For example, see the article by Jay W. Forrester, published in the Journal of Applied Physics, vol. 22, No. 1, January 1951.

The two banks are designated, respectively, the left HSM 15 and the right HSM 16. Each memory bank may be of the type employing magnetic cores and may be assumed to include address circuits. Each memory bank also includes read-out and read-in circuits, which may be respectively actuated by pulses or high levels. On the occurrence of a pulse, at the appropriate circuit, the memory is placed in condition and thus receives information applied thereto at its information-in circuits or supplies information at its information-out circuits. The information in or out is in the form of binary digits of information or bits each represented by the level on one of several leads. Several bits, in this instance seven, may be stored at each address, and written in or read out in parallel. For this purpose, each bank may have seven "memory planes" connected in known fashion. One of these seven bits is a parity bit. As will appear more fully hereinafter, a series of timing (that is, clock) pulses are provided in cycles of approximately twenty microseconds. It is assumed that the read-in and read-out circuits, although actuated, are further actuated internally only upon occurrence of a timing pulse designated T5. Information may be received or fed out of the memory throughout the period from timing pulse T5 to timing pulse T6. A memory of magnetic cores may be employed, or a vacuum tube memory, such as a type SB256, for example, may be employed.

Circuits are provided internally of each memory bank for regenerating and re-entering information at the same address from which withdrawn, if, as is now usual, the reading-out process would otherwise erase information at the read-out address.

It may be noted that the employment of two banks of the memory, rather than a single larger bank, and the use of other certain details involved are not essential to the invention described and claimed herein, but these details are shown and described by way of clear, explicit, and full example.

4.1.7 L (for Left) and R (for Right) Registers 18 and 19—FIGS. 1(b-c) and 1(d-c), Respectively; and Y and Z Registers 13 and 14—FIGS. 1(c-d) and 1(d-d), Respectively

(a) L and R registers 18 and 19 receive and store characters which are to be read into the left HSM 15 or right HSM 16, respectively.

(b) Y and Z registers 13 and 14 receive characters from the left HSM 15 or the right HSM 16 respectively, or from external tapes.

4.1.8 Operation Matrix OM—FIG. 1(b-a)

The operation matrix OM receives information, for example, from a suitable register, the operation called for in the instruction. This matrix then raises the level on the proper output operation level (or lead) which is then applied to enable the gates concerned in the specified operation. One and only one operation level (or lead) is high at any one time. Matrices which respond in this fashion are known.

4.1.9 A and C Registers 26 and 28—FIG. 1(c-a); O Register 30—FIG. 1(b-a); P Register 29—FIG. 1(d-a)

These registers are represented by labelled blocks. They are used for storing various parts of an instruction and occasionally for other purposes. These registers may be made up of flip-flop stages.

4.1.10 A and C Counters 10 and 12—FIG. 1(c-b) and B Counter 11—FIG. 1(d-b)

These counters may be made up of flip-flop stages. At least in some instances, they are also used as registers, and have stages which may be set or reset individually.

4.1.11 Left Symbol Recognition Circuits 22—FIGS. 1(b-d), 1(b-e), and 1(c-e); and Right Symbol Recognition Circuits 23—FIGS. 1(d-d) and 1(d-e)

These recognition circuits receive the output of the Y and Z registers 13 and 14 respectively. The recognition circuits "recognize" the nature of the character stored in the registers. The recognition circuit responds by a suitable signal. Such recognition is employed to afford control by the characters, jointly with the current status and operation levels, of the next status level to be high. Thus the characters of the operands join in determining the sequence of status levels which are to be raised and thus control the flow of the information through the information paths of the machine. These groups of circuits are only indicated in a general manner as a group by brackets above them. The individual recognition circuits are fully shown in block form and are more fully described hereinafter.

4.1.12 Nines Complementor 21—FIG. 1(e-d)

The nines complementor 21 accepts a binary coded decimal digit and produces the nines complement of the digit. This complementor 21 is used particularly in the subtraction operation, and in the handling of negative numbers. The nines complementor 21 may be of the kind described, for example in the application of Spielberg and Sublette, Ser. No. 337,572, filed February 18, 1953, entitled "A Code Converter," now U.S. Patent 2,798,677, issued July 9, 1957.

4.1.13 Nines Counter 45—FIG. 1(f-a)

The nines counter 45 is used in the operation multiplication to keep track of the number of times the multiplicand has been added to the partial product. A desired count may be entered on the nines counter 45, for example from the nines complementor 21.

4.1.14 Duplicate Adder 17A and Duplicate Binary to Coded Decimal Converter (BCDC) 17B—FIG. 1(e-b)

These units receive as inputs the addend and the augend, in binary coded decimal form and the previous carry, and produce, as output, a sum in the form of a binary coded, decimal digit and a carry (if any). The duplicated adders and BCDC (duplicated) together are the unit 17. The duplication provides for arithmetical checking. The unit 17 is the computer arithmetic unit.

4.1.15 Tape Handling Circuits 46—FIGS. 1(b-c) and 1(b-d)

The tape handling circuits include certain gates and a flip-flop enclosed in a dotted line. These circuits are used to control the tapes for both the read-in from tape and write-out to tape operations.

4.1.16 Status Level Control Flip-Flops 47—FIG. 1(a-e); and Status Transition Gates—FIGS. 1G and 1H

Status level changes are controlled by a set of flip-flops F1282 to F1293, and by a large number of status transition gates which are separately shown as the gates in FIGS. 1G to 1H. These circuits are an important feature of the present machine. From the fact that only one of the status level control flip-flops 47 is set at one time, it is apparent that a matrix driven by a register which register is under control of the status transition gate pulses to raise the level or voltage on a selected one only of the status levels could be used to perform the function of the status level flip-flops 47. The various status levels used in this machine are tabulated in section 4.5 below.

4.1.17 Alarm Circuits 48—FIG. 1(a-c)

The machine has certain protections against continued operation after certain errors have been made. The circuits which may be used to raise an alarm in such event are shown here.

4.1.18 Parity Regenerator 44—FIG. 1(b-d)

This circuit reads the contents of the L register 18 during certain operations and generates a parity bit if required. Other similar circuits are used.

4.1.19 Previous Result Flip-Flops 49—FIG. 1(f-d)

In certain programs, the sequence of operations depends upon the nature of the previous result. Three previous results flip-flops by their conditions indicate the nature of the results that affect the later program. The different conditions of the previous results flip-flops 49 is affected by certain associated circuitry including gates, the output of which responds to the result of an arithmetic operation.

4.2 Staticizing Instruction

The machine may be started manually, as more fully described hereinafter. In operation, instructions are then read out of the HSM and staticized (that is, temporarily stored), as required.

It is convenient to describe, at this point, the machine and its operation relating to the staticizing of instructions in a typical fashion which is accomplished by making a certain subset of the status levels successively high. It should be understood, however, that the order of succession of the status levels to be high is determined by the status transition gates. Also, certain preparations are made for subsequent operations during the high status levels RO01, RO02, and RO03 many of which are described in connection with the subsequent operations.

4.2.1 Staticizing Instructions—Status Level RO01 High

Assume that the status level or lead RO01 is high, that is has a high voltage. In other words, the status level control flip-flop F1293 (FIG. 1(a-e)) is in its set condition.

T1

A gate 502 (FIG. 1(d-b)) is provided which is primed by the high status level RO01 (from F1293 of FIG. 1(a-e)) to pass the first timing pulse T1 to reset the A and B counters 10 and 11 of FIGS. 1(c-b) and 1(d-b) respectively. Note that the terminal designated R (reset) where shown, for various counters and registers is connected to all the counter or register stages to reset all the stages at once unless otherwise indicated or stated.

Note that the gate 502 is connected through an "or" circuit to the reset terminal R of the B counter 11. The

25

very numerous "or" circuits are designated on the drawing only by the arrow and circle convention hereinbefore mentioned, or by legend, and ordinarily are not numbered. Moreover, their function is apparent from the schematic of FIG. 1.

A two-input gate 1401 (FIG. 1(b-a)) has as one input the status level RO01 and as the second input, the first timing pulse T1. The output of the gate 1401 is applied to the reset terminal R of the O register 30. Accordingly, all stages of the O register 30 are reset.

The count in the program subcounter PSC, FIG. 1(d-b), may be assumed a zero count. This zero count is passed in parallel through two sets of two-input gates 630, 630a, each set comprising seven gates. The gates in each set are connected respectively to receive as one input the outputs (from the "one" terminal) of the program subcounter PSC flip-flop stages. Each gate of the two sets has as its second input the first timing pulse T1 passed through a gate 629 which is primed by the high level RO01 applied through "or" circuits (as shown) to the last mentioned gate 629. Also applied through these "or" circuits to the gate 629 are status levels RO02, RO03, and RE.

The outputs from each set of gates 630 and 630a, respectively, are applied through suitable "or" circuits to the address circuits of the left HSM 15 and to the address circuits of the right HSM 16, respectively (see FIG. 1(c-c) and FIG. 1(d-c)). The left and right HSM 15 and 16 are respectively addressed at a location which may be designated zero. For this purpose, the remaining, higher order bits required for complete addressing of the HSM 15 or 16 may be considered zero. The addressing circuits corresponding to these higher order bits may be reset by a pulse whenever the gates 630, 630a are opened. One address suffices to read or write at one time, in one bank, a seven bit character.

T2

A two-input gate 141 (FIG. 1(a-a)) is provided having as one input the output of an "or" circuit receiving the status levels RO01, RO02, and RO03. The second input to the gates 141 is the second timing pulse T2. The output of the gate 141 is applied to the set terminal of the next to the lowest order (2^1 bit) flip-flop of the program counter PC. Accordingly, the count of the program counter PC is advanced by two, to keep step with the alternate drum lines corresponding to each portion of the instruction staticized. The program counter PC thus has the count of the drum line corresponding to the portion of an instruction next following that portion being staticized.

A two-input gate 244 (FIG. 1(a-b)) is provided which has its output applied to the trigger terminal T of the program subcounter PSC and which is primed by the high status level RO01, RO02, or RO03 through a suitable "or" circuit. The second input of the gate 244 is the second timing pulse. Thus, the gate 244 passes the second timing pulse to the program subcounter PSC. This trigger input is to the stage storing the least significant digit (lowest order stage) of the program subcounter PSC. The program subcounter PSC is thus advanced one count to contain the address of a second portion of the instruction to be withdrawn from the memory 15, 16. Each of these portions is (for most instructions) one-third of an instruction.

A two-input gate 481 (FIG. 1(c-a)) has as one input the status level RO01 and as the second input the second timing pulse T2. The output of the gate 481 is applied to the reset terminal of the A register 26. All stages of the A register 26 are thus reset.

T4

A two-input gate 443 (FIG. 1(d-a)) has as one input the status level RO01, and as a second input the fourth timing pulse T4. The output of the gate 443 is applied

26

to the reset terminal R of the parity register 29. Accordingly, the parity register 29 is now cleared (reset).

T6

A memory composed of magnetic elements is assumed. If a memory utilizing storage tubes is employed, preparation is preferably made for activating the cathode ray beam of the storage tubes. This preparation is omitted in the present description, but the requisite modification for use of storage tubes may be made by one skilled in the art.

A pair of two-input gates 730 (FIG. 1(c-c)) and 862 (FIG. 1(d-c)) are provided designated left and right read-out gates respectively. The outputs of this pair of gates are applied respectively to activate the read-out circuits of the left and right HSM 15 and 16. A first input of each of the left and right read-out gates 730 and 862 receives, through "or" circuits as shown, the status levels RO01, RO02, RO03, RS, RO, and ROM. The second input to each of the left and right read out gates receives, through "or" circuits as shown, the status levels RO01, RO02, and RO03, and the operation levels Q, M, V, and also operation levels B, L, A, R, or S, the latter group through "or" circuits indicated (but not shown) by the commas between the designating letters. In addition, the second input to the left read-out gate 730 receives the output from the "zero" terminal of the 2^9 bit (tenth order) flip-flop of the C register 28, applied through an "or" circuit; and the right read-out gate 862 receives the output from the "one" terminal of the 2^9 bit flip-flop of the C register 28 applied through an "or" circuit. At or shortly after the fifth timing pulse T5, and through the sixth timing pulse T6 the bits of the instruction addressed (in this case zero address) from the program subcounter PSC address are read out of the HSM 15, 16 information-out circuits. Six gates 1402 (FIG. 1(b-a)) are provided which are primed by the high status level RO01. Six bits from the left HSM 15 pass through the gates 1402 into the O register 30. The terminal indicated set (S) on the O register 30, as in the other flip-flop registers or counters herein, indicates, in reality, connections of the individual, multiple leads to the individual set terminals of the different flip-flop stages of the register. Therefore, the O register 30 receives the six bits coded to correspond to the operation to be performed. The O register 30 therefore responds to the coded instruction and controls the operation matrix OM to set high only the one corresponding output of the operation matrix, the other operation levels are low.

A three-input gate 444 (FIG. 1(d-a)) has as one input the status level RO01, as a second input, the parity bit from the left HSM 15, and as the third input, the sixth timing pulse T6. The output of the gate 444 is applied to the next to the lowest order (2^1) stage of the parity register 29. Thus, the single parity bit of the first portion of the instruction being read out from the program subcounter PSC is passed by the gate 444 into the parity or P register 29 (FIG. 1(d-a)).

The right HSM 16 (FIG. 1(d-c)) is also prepared for reading out by the high status level RO01 applied through the right read-out gate 862 (FIG. 1(d-c)). A set of six, three-input gates 402 (FIG. 1(c-a)) each has as one input status level RO01, and as a second input the sixth timing pulse T6. The six gates 402 receive, respectively, as the third input the various six bits, excluding the parity bit, from the right HSM 16. The outputs of the gates 402 are applied to the respective six higher order set terminals S of the A register 26 (FIG. 1(c-a)), respectively. A three-input gate 445 receives as one input the parity bit from the right HSM 16 as a second input the status level RO01, and as the third input the sixth timing pulse T6. The output of the gate 445 is applied as input to the set terminal S of the lowest order (2^0) stage of the parity register 29.

27

Accordingly, the seven bits stored in the right HSM 16 at the program subcounter PSC zero address are now passed in parallel into the six stages (2^0 - 2^5 stages) of the A register 26. The seventh bit from the right HSM 16 is the parity bit which is passed into the parity register 29 through a gate 445 which is also primed by the status level RO01 and the sixth timing pulse T6.

T8a

A two-input status transition gate 1280 (located on FIG. 1G) is provided which is primed by, that is, receives the status level RO01 and also receives an eighth delayed timing pulse designated T8a. This delayed pulse occurs before initiation of the succeeding cycle of timing pulses. From the status transition gate 1280, the eighth delayed timing pulse T8a is applied to the "set RO02" lead (of FIG. 1(a-e)) to reset all of the status level control flip-flops 47 through an amplifier 1292 and an amplifier A1299. Before start of the next cycle of timing pulses, the second status level control flip-flop F1292 (FIG. 1(a-e)) is set by the same pulse T8a from amplifier A1292, after passing through a fractional microsecond delay circuit D1292 to the set terminal S of a status control flip-flop 1292. Accordingly, the status level RO01 is lowered, and the status level RO02 is now high.

The O register 30 now contains the six bits of the binary code for the operation to be performed, and the A register 26 contains six bits of a nine bit address (the A address) of one of the operands.

4.2.2 Status Level RO02 High

T1

On the first timing pulse T1, the program subcounter PSC of FIG. 1(a-b) now applies to gates 630 and 630a levels which represent the address of the second portion (one-third) of the instruction now being read out and formerly surged into the HSM 15, 16. The gate 629 is primed by the status level RO02 to pass the first timing pulse T1 to open the gates 630 and 630a. The program subcounter PSC address is now applied to the address circuits of the left and right HSM 15 and 16 respectively.

T2

The second timing pulse T2 passes through the gate 244 which is primed by the status level RO02, to trigger the program subcounter PSC. The count in the program subcounter PSC is thus advanced to the address of the last portion (one-third) of the instruction to be read from the HSM 15, 16.

The gate 141 (FIG. 1(a-a)) passes the second timing pulse T2 to advance the count of the program counter PC by two.

The left and right HSM 15, 16 are respectively placed in read-out condition by the high level passed from the left and right read-out gates 730 (FIG. 1(c-c)) and 862 (FIG. 1(d-c)) respectively. Each of the read-out gates 730 and 862 is primed by the high status level RO02 passing through appropriate "or" circuits. Accordingly, the left and right HSM 15 and 16 are each addressed to the address (in this case "one") corresponding to the second portion of the stored instruction, and each HSM is conditioned for read-out.

T6

The sixth timing pulse T6 and the high status level RO02 together are applied to each gate of a set of three, three-input gates 405 (FIG. 1(c-a)). The three gates 403 also receive, respectively, the three lowest order bits of the seven bits from the output of the left HSM 15. The outputs of the gates 405 are applied, respectively, to the three lowest order stages of the A register 26.

Accordingly, the A register 26 now has stored in it nine bits which are the A address of the one operand of an operation about to be performed.

The sixth timing pulse T6 passes through a gate 512

28

(FIG. 1(d-b)), primed by the high status level RO02, and is applied to open a set of three gates 544. The gates 544 pass three more bits (which may be indicated as 2^0 - 2^2 bits) of information of the seven bits from the left HSM 15 output to the three set terminals of the most significant (that is, highest order) stages of the B counter 11. The seventh bit from the left memory HSM 15 is a parity bit. Note that the B counter 11 receives its initial count as a register.

Six, two-input gates 547 are provided (FIG. 1(d-b)) which receive the sixth timing pulse T6, passed through the gate 512, mentioned above. Gates 547 also receive respectively the six information bits from the right HSM 16. The outputs of the gates 547 are applied to the six least significant stages of the B counter 11. The seventh bit is a parity bit. Accordingly, the B counter 11 now holds the complete address of the other operand of the operation being staticized.

The sixth timing pulse T6 and the high status level RO02 also prime a gate 446 (FIG. 1(d-a)) to admit the parity bit from the left HSM 15, into the parity register 29. Similarly, a gate 447 (FIG. 1(d-a)) is primed by the sixth timing pulse T6 and the status level RO02 admits the parity bit from the right HSM 16. Accordingly, two more parity bits are entered in the parity register 29.

T8a

A status transition gate 1275 (FIG. 1G) is primed by the high status level RO02, and also receives the eighth delayed timing pulse T8a. This status transition gate 1275 passes the eighth delayed timing pulse T8a to the "set RO03" lead. The eighth delayed timing pulse T8a is then passed through amplifier A1291 and through amplifier 1299 to reset all of the status control level flip-flops 47. After further delay by delay circuit D1291 the eighth delayed timing pulse T8a sets the third status level control flip-flop F1291. Accordingly, status level RO03 is now high.

4.2.3 Status Level RO03 High

T1

With status level RO03 now high, the gate 629 (FIG. 1(a-b)) is primed to pass the first timing pulse T1, which in turn primes the gates 630 and gates 630a. The gates 630 pass the contents of the program subcounter PSC to the address circuits of the left HSM 15, and the gates 630a pass the contents of the program subcounter PSC to the address circuits of the right HSM 16, as before. Thus the left and right HSM 15 and 16 are addressed to corresponding addresses for the last portion (one-third) of the instruction stored in the HSM 15, 16.

The C counter 12 (FIG. 1(c-b)) is cleared or reset (all stages simultaneously) by the first timing pulse T1 passing through a gate 328 primed by the high status level RO03 and thence through an appropriate "or" circuit, as shown. The C counter 12 is now cleared preparatory to receiving the address for the result of the operation to be performed.

A gate 945 (FIG. 1(c-e)) is provided primed by the high status level RO03 to pass the first timing pulse T1 to the set terminal S of a space left flip-flop F911 (FIG. 1(a-e)) and a space right flip-flop F1008 (FIG. 1(d-e)). Accordingly, the space left and space right flip-flop F911 and F1008 are placed in the set condition. The reason for providing these two flip-flops and placing them in set condition will become apparent hereinafter.

T2

A gate 442 (FIG. 1(c-a)) is provided which receives the high status level RO03, ROM, or RE applied through a suitable "or" circuit. The gate 442 also receives the second timing pulse T2. The output of the gate 442 is applied to the reset terminal R (thus to reset all stages) of the C register 28.

29

The gate 141 (FIG. 1(a-a)) passes the second timing pulse T2 to advance by two the count of the program counter PC.

The program subcounter PSC (FIG. 1(a-b)) count is advanced by the second timing pulse T2 applied to its trigger terminal T through the gate 244 primed by the high status level RO03 applied through the "or" circuit shown. The program subcounter PSC is thus advanced to the HSM address of the first portion (one-third) of the following instruction stored in the HSM, if one is to be withdrawn.

T4

A set of nine gates 514 (FIG. 1(c-b)) are provided. The "one" outputs of the A register 26 (FIG. 1(c-a)) stages are connected respectively through the nine gates 514 (FIG. 1(c-b)) to the respective set terminals S of the A counter 10 of FIG. 1(c-b)). In other words the nine bits of information stored in the A register 26 are now applied to the set terminals S of the corresponding nine flip-flops of the A counter 10. A gate 510 is provided primed by the high status level RO03 or the high status level RN through a suitable "or" circuit to pass the fourth timing pulse T4 to open the gates 514.

T6

As with status levels RO01 and RO02 high, with status level RO03 high, a high level is applied through suitable "or" circuits to both inputs of each of read-out gates 730 and 862 (FIGS. 1(c-c) and 1(d-c)) to activate the left and right HSM 15 and 16 respectively. The information out is available at the sixth timing pulse T6.

The sixth timing pulse T6 and the high status level RO03 are applied to prime each of a set of six gates 436 and a set of six gates 430 of FIG. 1(c-a). These gates 436 and 430 now pass respectively the six bits from the read-out (or information out) circuits of the left HSM 15 and the right HSM 16 respectively into the six higher order and six lower order stages of the C register 28. The stages of the C register 28, as in the other registers or counters herein, may be considered to correspond to binary digits of a binary number. The least significant digit of the binary number is identified as 2⁰. The second significant digit each corresponding to the 2¹, etc. The C register 28 has a capacity for twelve binary digits and the six digits applied from the right HSM 16 are considered to be entered into the places designated as 2⁰ to 2⁵. The six bits of information from the left HSM 15 are entered into stages designated 2⁶ to 2¹¹.

In this way the digits corresponding in some operations, to the address of the result of the operation are entered into the C register 28. At the same time, the same six binary digits which are passed by the gates 430 to the C register 28 are applied by a set of six gates 318 (FIG. 1(c-a)) to the corresponding set terminals S of the six least significant stages of the C counter 12. The gates 318 are primed by the high status level RO03 and the sixth timing pulse T6. The three next significant bits in the C register 28 (2⁶ to 2⁸ bits) are at the same time entered by a set of three, three-input gates 324 into the C counter 12. One input to each of the gates 324 is from the 2⁶ to 2⁸ bit from the left HSM 15. The other two inputs to each of the gates 324 are, respectively, the status level RO03 and the sixth timing pulse T6. The same nine binary digits corresponding to the nine least significant digits of the result address are thus entered in the C counter 12 and in the C register 28.

Note that if desired the gates 430 and 318 could be primed through a single gate, because the "logic" is the same for these gates, with a resultant saving of equipment. This equipment saving, however, is often not shown in the schematic because such a single gate could not have a sufficiently high energy output, and sometimes because the description is simpler when shown separately.

Gates 448 and 449 are provided (see FIG. 1(d-a)) each primed by the sixth timing pulse T6 and the high

30

status level RO03. Gate 449 passes the parity digit of the left HSM 15 character and gate 448 passes the parity digit of the right HSM 16 character to the parity register 29.

Of the three most significant digits of the number now stored in the C register 28, that designated as the 2⁹ bit (10th bit) is employed to determine (in some operations) which side, left or right, of the HSM 15 or 16 is to be addressed for a result location. The 2¹⁰ bit stored in C register 28 is used in the operations read-in from tape (Operation N) and transfer data (Operations X and J). The 2¹¹ bit stored in the C register 28 is used in some operations to prevent reading into the HSM 15, 16.

The next status level selected depends upon the operation level which is high, and upon which status transition gate is opened.

Note that the status level RO01 is followed by status level RO02 which, in turn, is followed by status level RO03. However, after RO03 the status level which next becomes high is under control of the status transition gates. The next status level to be high depends on which operation level (from the operations matrix OM) is high.

4.2.4 Analysis of Staticized Instruction

During these three status levels the machine enters the HSM 15, 16 at specified addresses. These addresses are in a portion of the HSM 15, 16 reserved for program instructions, that is, the surge tank. A coded instruction representing an operation and three addresses is withdrawn and staticized.

With reference to FIG. 12, a complete coded instruction for this machine for most of the operations consists of forty-two binary digits of information (that is, "bits") of which six serve as parity check bits of the six, seven-bit characters which make up the instruction. The remaining thirty-six bits (for identification purposes called information bits, although the term at first seems tautological) serve to designate the operation to be performed and the addresses in the HSM 15, 16 where the operands are located or to be located. Some instructions do not need all three addresses, some use more addresses, and some require that the address bits be interpreted in a special way. However, these variations from most cases will be apparent from the description which follows.

Those bits of the forty-two bits which relate to different parts of an instruction have been denoted in FIG. 13 by O for operation, A address, B address, and C address. The twelve bits indicated as C address actually carry some additional information, as noted above, in that the 2⁴ and 2⁵ bits of the third character of the left HSM 15 (which are the 2¹⁰ and 2¹¹ bits of the C address of the instruction) carry special information.

The six information bits designated 2⁰ to 2⁵ of the first character in the left HSM 15 are the operation section O of the instruction. These six bits are staticized respectively in the stages designated 2⁰ to 2⁵ (in ascending order) of the O register 30. In the binary counters and registers, the stages are considered ordered as for a binary number. This O section of the instruction serves to "instruct" the machine what operation is to be performed.

The A register 26 receives nine information bits. The three A register stages designated 2⁰ to 2² receive respectively the 2³, 2⁴, and 2⁵ bits of the second character of the left HSM 15. The 2⁰ to 2⁵ bits of the first character of the right HSM 16 are staticized respectively in the 2³ to 2⁸ stages of the A register 26. The 2⁰ to 2⁵ bits of the second character of the right HSM 16 are staticized respectively in the 2⁰ to 2⁵ stages of the B counter 11, and the 2⁰ to 2² bits of the second character of the left HSM 15 are staticized in the remaining three B counter 11 stages 2⁶ to 2⁸ respectively.

The 2⁰ to 2⁵ bits of the third character of the right HSM 16 and the 2⁰ to 2⁵ bits of the third character of

the left HSM 15 are staticized respectively in the 2⁰ to 2¹¹ stages of the C register 28.

The parity bits are stored in the parity register 29 in the 2⁰ to 2⁸ stages respectively.

Starting from the 2⁰ stage and proceeding to "more significant" (higher order) stages up to the 2¹¹ stage, the six bits from the third character of the right HSM 16 designated 2⁰ to 2⁵ and the six bits from the third character of the left HSM 15 designated 2⁰ to 2⁵ are staticized in the twelve stages of the C register 28.

When the status level RO01 is high, the first one-third portion of the instruction is staticized. The instruction has previously been stored in the surge tank of the HSM 15, 16. It is now withdrawn in accordance with the address in the program subcounter PSC. This address is taken as zero for purposes of illustration, but any appropriate address may have been selected. The first one-third portion of the instruction includes the O section coded in the first character withdrawn from the left HSM 15. Also, the six most significant bits of the A address are withdrawn from the right HSM 16 and staticized in the corresponding six most significant or highest order stages of the A register 26. The two parity bits are stored in the parity register.

When the status level RO02 is high, the second character of the left HSM 15 and the second character of the right HSM 16 are withdrawn. The three most significant bits of the second character of the left HSM 15 are entered as the three least significant bits in the A register 26. The three least significant bits of the second character of the left HSM 15 are entered as the three most significant bits in the B counter 11, and the six information bits of the second character of the right HSM 16 are entered as the six least significant bits in the B counter 11. Again the parity bits are stored in the parity register.

The six information bits of the third character from the left HSM 15 and the six information bits of the third character from the right HSM 16 are entered respectively as the most significant six bits and the least significant six bits of the twelve bit C register 28. Again, the two parity bits are stored in the parity register 29.

It will be apparent that the so-called information bits of the coded instruction are staticized as follows: Six bits in the O register 30 which indicate the operation to be performed; nine bits in the A register 26 (also in the A counter 10) which give the address of one operand (in the left memory bank); nine bits in the B counter 11 which give the address of the other operand (in the right memory bank); and twelve bits in the C register 28, nine bits of which give the address of the result in a memory bank, one bit (2⁰ bit) indicates which memory bank, and the other two bits of which are employed for special purposes in certain operations.

4.3 Start of Machine and Generation of Timing Pulses

It is assumed that coded instructions are stored on the magnetic program drum PD (FIG. 1(a-a)) which has suitable timing tracks. It is known to thus load the drum with instructions. A set of timing pulses are generated under control of a reset track pulse and timing track pulses from the program drum PD. The reset (index) pulse occurs only once in a drum revolution and, at the rate of rotation of the drum, approximately 50 microseconds before the first pulse from a timing track and 50 microseconds after the last pulse from a timing track. The first timing track pulse is generated at the same time that the first line of the drum is read, in known manner. After the first timing track pulse is generated one timing track pulse is generated for each line of the drum.

In this computer, an instruction employs three drum lines. However, alternate, rather than consecutive, drum lines are used for each portion (one-third) of an instruction. One series of instructions uses all the even numbered lines, and another series of instructions uses all the odd numbered lines on the program drum PD. At

the beginning of an instruction surge, the desired instruction may start on an even numbered drum line or an odd numbered drum line. Therefore, each drum line (odd and even) is checked until the first line carrying the desired instruction is found. A count is manually set (by means not shown) in the program counter PC (FIG. 1(a-a)) to correspond to the drum line on which is coded the first one-third of the first instruction desired. Also, the status level RE is manually set high (by means not shown), if not high already. The various flip-flops and registers are assumed in appropriate initial condition, most being reset, and suitable means may be provided to insure such condition.

A manual "reset to start" switch (FIG. 1(a-c)) is provided. Before the machine is started, this manual "reset to start" switch is actuated to set or reset various flip-flops to their initial condition, and in particular to reset a pair of flip-flops F201 FIG. 1(a-d) and F202 FIG. 1(a-e). The zero terminal of one flip-flop F201 of this pair is applied to prime each of a group of gates 201, 202, 203, and 204 of FIG. 1(a-d) and 235 of FIG. 1(a-c). The "one" output or terminal of flip-flop F201 is applied as one input of each of another group of gates 205, 206, 207, and 208 of FIG. 1(a-d). The four timing pulses designated first to fourth (T1 to T4) are gated by the gates 201 to 204 respectively and then passed through suitable amplifiers as indicated in FIG. 1(a-d). The fifth (T5), sixth (T6), seventh (T7), and seven-b (T7b) timing pulses are gated respectively by gates 205 to 208.

A manual start switch (FIG. 1(a-c)) is provided having two sets of contacts, one set normally open, indicated NO, and one set normally closed indicated NC. When one set of contacts of the manual start switch is closed the other is open, and vice versa. The reset pulse from the reset track of the program drum PD (which occurs once each drum revolution) is applied to a two-input gate 227 and a three-input gate 299, and also to a gate 150. Gate 227 is primed by a positive voltage (as indicated) from the normally open contacts NO closed when the switch is actuated. The output of the gate 227 is applied to the reset terminal R of a flip-flop F212 (FIG. 1(a-c)). The output taken from the zero terminal of the flip-flop F212 passes through the switch contacts NC (FIG. 1(a-b)) when the switch is not actuated, to the gate 229 which, when suitably primed, then passes the reset track pulse, to the set terminal S of a flip-flop F214. The "one" terminal of the flip-flop F214 is connected to prime a three-input gate 235 (FIG. 1(a-c)) through which pass the timing track pulses from the timing track on the program drum PD. The reset terminal R of the flip-flop F214 (FIG. 1(a-b)) is connected to receive a suitable pulse from a gate 228 (FIG. 1(a-c)) through a suitable "or" circuit (FIG. 1(a-b)) for reasons explained more fully hereinafter. These gated pulses each applied to the reset terminal of flip-flop F214 prevent the passage of timing pulses and halt the operations of the machine.

In the operation of the surging circuits to start to fill the surge tank, that is, to start to surge the instructions into the HSM 15, 16, the "manual start" switch is actuated and the contacts NO are closed, and the contacts NC are opened. The reset pulse from the program drum PD passes the gate 227 (FIG. 1(a-c)) primed by the voltage through the "manual start" switch. The flip-flop F212 is reset by this pulse from gate 227. As the contacts NC are open, nothing further happens until the manual start switch is released and the switch contacts NC (FIG. 1(a-b)) are closed. Then the high level from the zero output from the flip-flop F212 (FIG. 1(a-b)) is passed to the gate 229. One input to gate 229 (also FIG. 1(a-b)) comes from an inverter I10 connected in the alarm circuit 48; the output voltage of this inverter on a "no alarm" lead is high when there is no alarm. When this "no alarm" voltage primes the gate 229 to

gether with the voltage from the zero terminal of flip-flop F212 and the next pulse from the reset track of the program drum PD appears at gate 229, the gate 229 passes this pulse from the reset track to set flip-flop F214 (FIG. 1(a-b)). The "no alarm" voltage is applied to the gate 150 as a priming voltage. The output of the gate 150 is applied to the reset terminal R of the drum counter DC. The output of flip-flop F214 partially primes the gate 235 (FIG. 1(a-c)) which receives a second priming input from the zero terminal of flip-flop F201 (FIG. 1(a-d)), as already mentioned.

Therefore, on the occurrence of the first synchronizing pulse from the timing track (distinguish from the first timing pulse T1) following the reset (that is, index or fiducial) pulse from the reset track of the program drum PD, the gate 235 (FIG. 1(a-c)) passes the first timing track pulse through the gate 201 (FIG. 1(a-d)) and an amplifier to become the first timing pulse T1. This first timing pulse T1 sets the flip-flop F212 (FIG. 1(a-c)). Accordingly, the gate 229 (FIG. 1(a-d)) is closed to the pulses from the reset track of the program drum PD. At the same time the condition of the flip-flop F214 (FIG. 1(a-b)) is unchanged even though its set terminal voltage has gone low. Accordingly, the gate 235 (FIG. 1(a-c)) remains primed insofar as the "one" input from the flip-flop F214 is concerned. This first timing track pulse followed the fiducial pulse (after a suitable delay in a delay circuit D1) is passed by the gate 202 (FIG. 1(a-c)) through another amplifier to become the second timing pulse T2. Similarly, the gates 203 and 204 (FIG. 1(a-d)) pass this first timing track pulse after suitable delays in delay circuits D2 and D3 and amplification to become third and fourth timing pulses T3 and T4.

The fiducial (that is, index) pulse from the reset track of the program drum PD passing through the gate 150 resets the drum counter DC. With the occurrence of the first timing pulse T1 after the index pulse the count of the drum counter DC (FIG. 1(a-d)) is advanced by one because the first timing pulse T1 is applied to the trigger terminal T (of the lowest order stage) of the drum counter DC. The count of the drum counter DC is now advanced in like manner for each drum line, one of which parallels each timing track recorded pulse, which passes under the drum heads. A comparison circuit indicated as the third equal circuit 50 compared each bit of the information previously entered in the various flip-flops of the program counter PC with the corresponding ones in the drum counter DC. The equal circuit 50 may be a group of "and" gates and "or" circuits arranged to have a high output if and only if the two binary numbers, one from the drum counter DC and the other from the program counter PC, are equal. Besides, the output "and" gate receives the high status level RE, and a timing pulse T4c.

Accordingly, when the count previously set into the program counter PC (for example, manually by means not shown) corresponds to that in the drum counter DC and the status level RE is also high, the third equal circuit 50 passes a pulse T4c delayed in delay circuit D13 but occurring between the fourth and fifth timing pulses T4 and T5. When the pulse leaves the third equal circuit 50, it sets a drum line match flip-flop F125 (FIG. 1(a-b)). A gate 142 is primed by the "one" output of the drum line match flip-flop F125 to pass the second timing pulse T2 of the succeeding cycle of timing pulses to the reading heads and amplifiers 51 and 52 (FIG. 1(a-a)). Thus when the drum line match flip-flop F125 (FIG. 1(a-b)) is set by the delayed pulse T4c so passed from the third equal circuit 50, amplifiers of the reading heads and amplifiers 51 and 52 may be considered gated to read-out the seven bits read from each of the two information channels of the program drum PD. The disposition of this information is described hereinafter.

The high "one" output from the drum line match flip-flop F125 (FIG. 1(a-b)) also primes a gate 242 through which the second timing pulse on each occurrence triggers

the program subcounter PSC to advance its count one. The drum line match flip-flop F125 "one" output also primes a gate 232 (FIG. 1(a-c)) to which has applied to it the second timing pulse T2. The gate 232 now passes the second timing pulse T2 to set the flip-flop F202 which primes the gate 237 (FIG. 1(a-d)). When the gate 237 is thus primed a delayed fourth timing pulse T4c is passed to set the flip-flop F201. Setting the flip-flop F201 primes the gates 205 to 208 and thus to pass fifth, sixth, seventh, and seventh delayed timing pulses T5, T6, T7 and T7b, as shortly explained more fully.

A delayed fourth timing pulse T4c is formed (see FIG. 1(a-d) toward lower left) by applying the fourth timing pulse T4 to a delay circuit D5 to generate, first, a delayed fourth pulse T4b. The timing pulse T4b is passed through another delay circuit D6 to form another delayed fourth timing pulse T4c.

The gate 237 passes the fourth delayed timing pulse T4c to a delay circuit D4 (FIG. 1(a-c)) through the "or" circuit shown to the delay circuits D1, D2 and D3. Note that, in effect, the timing track pulse is recirculated. At the same time, the fourth delayed timing pulse T4c is applied to the set terminal S of the flip-flop F201. Accordingly, the gates 201 to 204 are closed. The "one" output of the flip-flop F201 is high to open the gates 205 to 208.

The recirculated pulse is now delayed in delay circuit D4 and in the same delay circuits D1 to D3 used to delay the first pulse, and the pulses then pass through the gates 205 to 208 respectively, and after amplification are used as the 5th, 6th, 7th, and 7bth timing pulses T5, T6, T7, and T7b.

Note (FIG. 1(a-2) at left) that the timing pulse T7b is also applied to a delay circuit D7 to make available an eighth timing pulse T8, and then to a further delay circuit D8 to make available an eighth delayed timing pulse T8c.

The eighth timing pulse T8 is applied to a delay circuit D10 (FIG. 1(a-c)) and then through a gate 1301 to provide a delayed eighth timing pulse designated T8a. The gate 1301 is primed by the high "no alarm" voltage to pass the eighth delayed timing pulse T8a. This eighth delayed timing pulse T8a is used as one input on the status transition gates.

The eighth timing pulse T8 is now applied through a delay circuit D9 to reset flip-flop F201. The gates 201 to 204 are now open again and gates 205 to 208 are closed. One drum line has meanwhile passed the drum heads. Accordingly, with the next pulse, occurring when the alternate line passes the drum heads, from the timing track of the program drum PD another first timing pulse T1 is passed by gate 201 and the cycle of the timing pulses recurs unless a different action occurs to stop the passage of these pulses, as may be the case, as will appear more fully hereinafter. Therefore, as every other drum line passes the read heads and every other timing track pulse occurs, a new series of timing pulses occurs, and the second timing pulse T2 is used to gate the read amplifiers on the alternate drum lines.

Note that when the flip-flop F201 (FIG. 1(a-d)) is set by the timing pulse T4c passed by the gate 237, the gate 235 is closed, because the zero output of the reset to start flip-flop F201 is low. The timing is such, however, that at slightly after this time, for example when T5 is generated, the next line on the drum passes under the reading heads. However, as the gate 235 is closed, no new first timing pulse is generated, as when the gate 235 is open and the flip-flop F201 is in reset condition. Further, the drum reading heads and amplifiers 51 and 52 are closed. The drum counter count, however, is advanced one by the timing pulse T5 applied through an "or" circuit to the trigger terminal T of the drum counter DC. Thus the drum counter DC keeps the proper count of the drum line arriving under the reading heads.

35

The arrangement of the timing pulse generator described allows substantially twice as much information to be packed on the drum and used in a highly efficient manner as would be possible without this arrangement. Recall that the HSM 15, 16 can respond to information only at twenty microsecond intervals. The drum may be packed with information on lines distant at ten microsecond intervals, at its proper rotational rate. Therefore, the arrangement of the timing pulse generator allows alternate lines to be read from the drum at a rate to which the memory can properly respond. At the same time, the drum may be packed with information solidly.

The drum counter DC keeps proper count of the drum lines, because of the input to its trigger circuit from the "or" circuit having the T1 or T5 input. The rapidity of access to any drum line is not reduced by virtue of the slower read-out, since any drum line is still accessible in not more than one revolution of the drum. Thus the timing pulse generator arrangement provides means whereby, when a complete cycle of timing pulses are generated, only certain drum lines start each cycle, and intermediate drum lines between these certain (in this instance alternate) lines, for the current cycle, are ignored. A novel means of reducing the read-out or pulse rate and still maintaining density of packing and rapidity of access is thus provided.

The program drum and its timing track may be considered as part of the timing pulse generator. The program storage of the drum may be considered as part of the entire internal memory of the computer.

4.4 Surge of Instructions

The surge of information into the surge tank may now be described. The status level RE is high. The description of the machine and its operation for the surge of instructions may now be followed in accordance with the sequence of the timing pulses. The surge is similar to that described in the Bensky et al. Patent 2,679,638.

4.4.1 Initiation of Surge of Instructions

T1

A three-input gate 860 (FIG. 1(e-c)) is provided having as one input the status levels RE or RI applied through a suitable "or" circuit, as a second input the output of an inverter I6 indicated as NOT (J, E, X), and as the third input the first timing pulse T1. The input to the inverter is from an "or" circuit having as inputs the operation levels J, E, and X. These operation levels are all low, so that the NOT (J, E, X) lead is high. The output of the gate 860 is applied through "or" circuits (FIG. 1(d-c)) to reset the R register 19 and also the L register 18 (FIG. 1(b-c)) by the lead XX.

A three-input gate 861 is provided having as one input the output of an "or" circuit receiving the status levels RE, RO, and RS. A second input to the gate 861 is from an "or" circuit receiving the operation levels J, E, X, and V. The third input to the gate 861 is from the first timing pulse T1. The output of the gate 861 is applied through "or" circuits to the lead XX.

Accordingly, the L register 18 and the R register 19 are reset, so that they will not affect through "or" circuits from the respective register outputs the read-in from the drum to the HSM 15, 16.

The gate 629 (FIG. 1(a-b)) is primed by the high status level RE applied through an "or" circuit with the status levels RO01, RO02, and RO03. Accordingly, the first timing pulse T1 is passed through the gate 629 to prime the gates 630 and 630a. The gates 630 and 630a are therefore open and pass the program subcounter PSC count to the address circuits of the left and right HSM 15 (FIG. 1(c-c)) and 16 (FIG. 1(a-c)).

T2

The status levels RE, and ROM, as well as RO03, are applied through the "or" circuit, as shown, to the gate

36

442 (FIG. 1(c-a)). Accordingly, the second timing pulse T2 is applied to reset the C register 28.

The gate 142 (FIG. 1(a-b)) primed by the "one" terminal of the drum line match flip-flop F125, passes the second timing pulse T2 to open the read heads and amplifiers 51 and 52 (FIG. 1(a-a)). The amplifiers of the read heads and amplifiers may be considered as gated or opened to pass information through various "or" circuits as indicated to the L and R registers 18 (FIG. 1(b-c)) and 19 (FIG. 1(d-c)) respectively.

The drum line match flip-flop F125 (FIG. 1(a-b)) "one" output is applied to prime the gate 242. The second timing pulse T2 is passed by the gate 242 through an "or" circuit to trigger the program subcounter PSC. The program subcounter PSC is thus advanced one in count for each line read from the program drum PD. Therefore, the program subcounter PSC records the number of one-third portions of instructions surged into the HSM 15, 16. Note that because the gates 630 and 630a to the memory address circuits are opened only during the first timing pulse T1, the memory address for any drum line to be stored in the memory corresponds to the count in the program subcounter PSC before the latter count is advanced by the second timing pulse T2 to correspond to the address of the next line to be stored.

T5

A set of seven, two-input gates 722 (FIG. 1(c-c)) is connected between the L register 18 (FIG. 1(b-c)) and the information receiving circuits of the left HSM 15 (FIG. 1(c-c)). A three-input gate 799 has its output applied to the gates 722. The three-input gate 799 receives one input from an inverter I1 (FIG. 1(b-c)). The input to the inverter I1 is from the status level RIS now low.

A second input to the gate 799 (FIG. 1(c-c)) is from the status level RE through a suitable "or" circuit, as shown. The third input to the gate 799 is from the fifth timing pulse T5.

A set of seven, two-input gates 851 (FIG. 1(d-c)) is connected between the R register 19 (FIG. 1(d-c)) and the information receiving circuits of the right HSM 16. A gate 899 has its output applied to open the gates 851. The three-input gate 899 receives one input from an inverter I3. The input to the inverter I3 is from the status level RIS now low. A second input to the gate 899 (FIG. 1(d-c)) is from the status level RE applied through a suitable "or" circuit. The third input to the gate 899 is the fifth timing pulse T5.

In operation, the gates 799 (FIG. 1(c-c)) and 899 (FIG. 1(d-c)) are open because of the high status level RE and, respectively, the high outputs from the inverters I1 and I3. Note that the input to each of the inverters is low and when inverted is high. Therefore the gates 799 and 899 pass the fifth timing pulse T5 to the gates 722 (FIG. 1(c-c)) and 851 (FIG. 1(d-c)) respectively. The information from the left read heads and amplifiers 51 (FIG. 1(a-a)) which was staticized in the L register 18 (FIG. 1(b-c)) is now entered into the left HSM 15 at the address from the program subcounter PSC (FIG. 1(a-b)); the information from the right read heads and amplifiers 52 (FIG. 1(a-a)) which was staticized in the R register 19 (FIG. 1(d-c)) is now entered into the right HSM 16 at the address from the program subcounter PSC (FIG. 1(a-b)). The addresses from the program subcounter PSC were entered in the address circuits of the HSM 15, 16 when the timing pulse T1 of the current cycle of timing pulses occurred.

On the next series of timing pulses T1, T2, etc., an alternate drum line containing one-third of the instruction is entered into the HSM 15, 16 and a cycle of timing pulses are again generated.

4.4.2 End of Surge of Instructions

The number of instructions to be read into the HSM 15 and 16 during any one surge is determined by the pro-

grammer. The number may be 4, 8, 16, or 32, as desired, in this apparatus. The desired number is manually set in a "manual switch for surge length" 54.

The ganged manual switch 54 (FIG. 1(a-c)) is arranged with contacts which come off the "one" and "zero" terminals of certain of the program subcounter flip-flop stages. The arrangement of this switch is best understood by way of example. The seven stages of the program subcounter PSC (FIG. 1(a-b)) correspond respectively to the digits of a seven digit binary number. In a first position of the manual switch for surge length 54 (FIG. 1(a-c)) the "one" terminals of the third and fourth stages, which correspond to the 2^2 and 2^3 binary digits of information or bits, are connected to an "and" gate 245. The zero terminals of these same 2^2 and 2^3 stages are connected to an "or" circuit 55. The terminal labeled "NOT END" is the output of the "or" circuit 55. The "end" terminal is the output of the "and" gate 245. With the switch 54 in this first position, the "Not End" terminal is high so long as the count (expressed decimally) 12 is not reached, whereas the "End" terminal first becomes high when the count 12 is first reached.

If the contacts are now switched to the 2^4 and 2^3 bits or stages of the program subcounter PSC, the "End" terminal is first high when the program subcounter PSC first reaches the count 24. The "Not End" terminal is high until the count 24 is reached. Thus, the "Not End" terminal of the manual switch is high until the count inserted or called for by the switch 54 is reached. As soon as the count called for by the manual switch for surge 54 is reached by the program subcounter PSC, the "End" terminal becomes high and the surge of instructions ceases, as will appear more fully hereinafter.

When the count 12 is inserted in the manual switch for surge 54, twelve lines are to be surged from the drum. In this machine, three lines of 14 bits each are required for each instruction and therefore the count 12 set in the manual switch 54 corresponds to calling for four instructions by the programmer. If the count 24 is set into the manual switch for surge 54, then eight instructions will be surged into the HSM 15, 16 from the program drum PD.

The program subcounter PSC (FIG. 1(a-b)) counts the lines being surged, and this count corresponds to the address in each memory bank left HSM 15 and right HSM 16 where the lines are stored. When the count in the program subcounter PSC is the same as the surge length entered in the manual switch for surge length 54 (FIG. 1(a-c)), the level at the output of the gate 245 rises, that is, a high level is placed on the terminal designated "END." A four-input gate 243 (FIG. 1(a-b)) receives the voltage from this "End" terminal. The gate 243 is also primed by the voltage from the "zero" output terminal of an "after first RE" flip-flop F703 (FIG. 1(b-b)) which is, for the surge and most operations, in the reset condition. The "after first RE" flip-flop F703 is reset by the first timing pulse T1 passed through a gate 943 (FIG. 1(d-e)). The gate 943 receives two inputs, one the status level RO01 and the other the first timing pulse T1. The output lead from the gate 943 is designated RO01-T1 reset. The gate 243 (FIG. 1(a-b)) also receives the status level RE. Therefore, the gate 243 passes the eighth timing pulse T8 (delayed) through suitable "or" circuits to reset the program subcounter PSC and also reset the drum line match flip-flop F125.

The zero terminal of the "after first RE" flip-flop F703 (FIG. 1(b-b)) is applied to prime a status transition gate 1277 (FIG. 1G). The status transition gate 1277 is also primed by the high status level RE and by the high "End" terminal (FIG. 1(a-c)). Therefore, the status transition gate 1277 (FIG. 1G) now passes the eighth delayed timing pulse T8a to a lead designated "set RO01" (FIG. 1(a-e)). The "set RO01" lead passes the pulse through an amplifier A1293 and a delay circuit D1293 to reset all of the status level control flip-flops 47; and after a delay

in delay circuit D1293 to set the RO01 flip-flop F1293. Accordingly, the machine is now ready to read-out the first one-third of the first instruction from the HSM 15, 16, as already described.

As each one-third instruction is staticized with successive high status levels RO01, RO02, and RO03, the program subcounter PSC (FIG. 1(a-b)) keeps count, being triggered by pulses from the gate 244. The program subcounter PSC count is again compared to the count set into the manual switch for surge length 54 (FIG. 1(a-c)). So long as no equality is reached, the "NOT END" terminal is high. This "NOT END" terminal primes status transition gate 1278 (FIG. 1G). Every time an instruction is completed, for most instructions, the status level IC is high. Therefore, in most instances, status transition gate 1278 is primed by the "NOT END" terminal and the instruction complete status level IC to pass the eighth delay timing pulse T8a to the "set RO01" lead, and the next instruction is read-out in the manner heretofore described.

Finally, when the count in the program subcounter PSC (FIG. 1(a-b)) equals the count set into the manual switch for surge 54 (FIG. 1(a-c)), the "End" terminal is high and the "NOT END" terminal is low. When the "End" terminal level is high and the instruction complete status level IC is high, these are both applied to the status transition gate 1220 (FIG. 1H) to pass the eighth delayed timing pulse T8a to the "set RE" lead (FIG. 1(a-e)). After passing through amplifiers A1283 and A1299 to reset all of the status level control flip-flops, this pulse from status transition gate 1220 is effective through a delay circuit D1283 to set the status level control flip-flop F1283. The status level RE calling for a new surge is now high. However, the status level RE is also used in a special way for the operation read-in-from-tape (Operation N), as described hereinafter.

Note also that after the machine is started by the reset-to-start switch (FIG. 1(a-c)) to reset flip-flop F202, that the pair of flip-flops F201 (FIG. 1(a-d)) and F202 (FIG. 1(a-c)) are reset automatically instead of manually. The flip-flop F201 (FIG. 1(a-d)) is reset by the eighth timing pulse T8 delayed in a delay circuit D9. The other flip-flop F202 (FIG. 1(a-c)) is reset from a gate 246 which is primed first by the high status level RE, second by the high "zero" terminal of the drum line match flip-flop F125 (FIG. 1(a-b)), to pass the first timing pulse T1. But the "zero" output of the drum line match flip-flop F125 is high in response to the delayed eighth timing pulse T8a passed through gate 243 when either the instruction complete IC or surge RE status levels respectively are high, and the "after first RE" flip-flop F703 (FIG. 1(b-b)) is in its reset condition (which is assumed here). However, with the flip-flop F202 (FIG. 1(a-c)) thus in reset condition, only the timing pulses T1 to T4 are generated, and timing pulses T5 to T8 are blocked. Therefore, the timing pulses T1 to T4 are repeated as for the first surge with status level RE high until the drum line carrying the desired instruction is located. Recall (see sec. 4.2) that the program counter PC (FIG. 1(a-a)) has the count of the next alternate drum line in the series in the program. Thus the next set of alternate lines are ready to be surged when the third equal circuit 50 passes a pulse indicating equality between the count in the program counter PC and in the drum counter DC. The program counter count PC is also set to a desired drum line in certain operations such as a "refer" operation (Operation Q) and others, as will appear more fully hereinafter.

Thus, in operation, the programmer sets into the manual switch for surge 54 the number of instructions to be surged into the HSM 15, 16. The operator then actuates the reset-to-start switch. The first four timing pulses are then generated until the proper drum line corresponding to the count in the program counter PC is matched by the count in the drum counter DC. Thereupon the instruc-

tions are surged from the program drum PD into the HSM 15, 16. Immediately thereafter the first instruction is read-out of the HSM 15, 16 and staticized as described above. Thereupon the operation called for by this and other instructions withdrawn is accomplished as described hereinafter. On completion of the instructions, status level RE is high and only the timing pulses T1 to T4 are generated again. Then another surge of instructions follows, etc., until the machine stops on completion of the program.

4.5 Typical Selection of New Status Level

Although the manner of selection of new status levels is apparent from what has already been said, a typical change of status level is described. Assume that the operation level A (for decimal addition) from the operation matrix OM (FIG. 1(a-a)) is high. Also assume that the status level RO is high (FIG. 1(a-e)). A status transition gate 1249 (FIG. 1G) is primed by any one of the high operation levels X, A, S, M, B, L, or R. It may be understood that these levels are applied to the status gate 1249 through a suitable "or" circuit (not shown). Therefore, the status transition gate 1249 is primed by the high operation level A and the high status level RO to pass the eighth delayed timing pulse T8a. This eighth delayed timing pulse T8a is passed to the lead designated "set RI" (FIG. 1(a-e)) which is the input to an amplifier A1289. The output of the amplifier is applied through suitable "or" circuits to the amplifier A1299 which amplifies the pulse to reset all of the status control level flip-flops 47. In this same manner, a pulse applied to any one of the twelve amplifiers A1282 to A1293 is amplified by amplifier A1299 and applied to reset all the status level control flip-flops 47 (F1282 to F1293). Any existing status level is thus removed (that is, the status level becomes low).

The pulse output of amplifier A1289 is also delayed by a delay circuit D1289 and applied to set the selected flip-flop F1289 of the status level control flip-flops 47. In this case the selected flip-flop F1289 provides from its "one" terminal the high read-in or RI level when high.

Thus, in each case, when a status level is to be selected by a status transition gate, the output of the status transition gate is first applied to reset all the status level control flip-flops 47 and thereafter is applied to set the selected status level control flip-flop 47. When a pulse is applied to any "set" lead of FIG. 1(a-e), this pulse is passed through the appropriate one of amplifiers A1282 to A1293, and through the amplifier A1299 to reset all the status level control flip-flops 47 (F1282 to F1293). The pulse from the appropriate amplifier A1282 to A1293 also passes through the appropriate delay circuit D1282 to D1293 and "sets" the corresponding flip-flop F1282 to F1293 (that is, causes the flip-flop to assume the "set" condition). The selected status level is thus made high.

The various status levels are listed in the following tabulation, with an indication of the sub-operation usually performed when that status level is high.

Tabulation of Status Levels

Status Level:	Usual Sub-Operation
RO01-----	Staticize one-third of an operation.
RO02-----	Staticize one-third of an operation.
RO03-----	Staticize last third of operation.
RO-----	Read operand or operands from HSM.
ROM-----	Read out multiplier digit from HSM.
RS-----	Search for least significant digit or digits.
RE-----	Refill surge tank of HSM.
RI-----	Write into HSM.
RIS-----	Write a space into HSH.

Status Level:	Usual Sub-Operation
RN-----	Renew multiplicand and partial product address.
RD-----	Various facilities.
IC-----	Instruction complete.

The sub-operations are not always identical for different operations. The sub-operation itself may vary depending on the operand or the operand characters. The status levels may be thought of as affording an additional degree of freedom to the computer.

4.6 Instruction Complete—Status Level High

The instruction complete status level is high at the completion of most of the instruction. There are then two possibilities, first that instructions are still stored in the HSM 15, 16 so that a new instruction may be staticized; or second that no instructions are left in the HSM 15, 16 so that a new surge with the high status level RE is required, as described previously.

If the instruction just completed is not the last instruction, and another remains in the HSM 15, 16, the "NOT END" lead from the "or" circuit 55 of the manual switch for surge 54 (FIG. 1(a-c)) is high. A status transition gate 1278 is provided which is primed by the high "NOT END" output from the "or" circuit 55 and also by the high status level IC, to pass the eighth delayed timing pulse T8a which is applied to the status transition gate 1278. The output of the status transition gate 1278 is applied to the "set RO01" lead (FIG. 1(a-e)). The status level RO01 therefore becomes high. The new instruction is staticized in the manner previously described.

In the event that the instruction just completed is the last instruction stored in the HSM 15, 16, the "END" lead from the manual switch for surge 54 is high. A status transition gate 1220 (FIG. 1H) has applied to it this "END" lead and the status level IC. The eighth delayed timing pulse T8a is also applied to the status transition gate 1220. Accordingly, under this condition, the status transition gate 1220 passes the eighth delayed timing pulse T8a to the "set RE" lead (FIG. 1(a-e)). Then the status level RE is selected to be high. A new surge of instructions is then received from the program drum PD, as explained above.

5. DETAILED DESCRIPTION AND OPERATIONS OF THE COMPUTER

In what follows each of the circuits for different operations as determined by the high levels from the operation matrix OM are detailed. The various operation levels are identified by single capital letters. The particular letters and the corresponding operation called for by the level being high are as follows:

Operation Level:	Operation
A-----	Decimal addition.
S-----	Decimal subtraction.
M-----	Multiplication.
B-----	Binary addition.
R-----	Binary subtraction, with "right-hand justification."
L-----	Binary subtraction, "left-hand justification."
N-----	Read-in from tape.
W-----	Write out to tape.
H-----	Write out to tape and clear.
X-----	Transfer data within HSM 15, 16.
J-----	Transfer data and clear.
E-----	Justify right.
K-----	Clear.
V-----	Verify.
T-----	Unconditional transfer of control.

Operation Level:	Operation
C-----	Conditional transfer of control.
P-----	Set up.
Q-----	Refer.
F-----	Stop.

5.1 Decimal Addition—Operation A

The instruction has been staticized with the successive status levels RO01, RO02, and RO03, the instruction is staticized (in binary code) as follows (see also FIG. 12):

O Section	A Section	B Section	C Section
Instruction Code No. for Addition.	Address of Addend.	Address of Augend.	Address of Sum.

A three-input status transition gate 1234 (FIG. 1H) has applied to it the high status level RO03. The operations matrix OM is set to have the high operation level A because of the instruction now in the O register 30. The operation level A, S, E, M, or R (whichever operation level is high) by means of "or" circuits, as indicated, is a second input to the status transition gate 1234. Note on the lead legended A, R, S, M, E, the commas, by convention, indicate the output from an "or" circuit having the legended levels. This convention is used herein frequently. The third input is the eighth delayed timing pulse T8a. The output of the gate 1234 is applied to the "set" RD lead. (FIG. 1(a-e)). Therefore, the status level RS is high.

5.1.1. Status Level RS High

T1

With the status level RS high there is a search for the least significant digit of each operand, in the case of addition, of the addend and of the augend. A three-input gate 945 (FIG. 1(c-e)) has its output applied through "or" circuits as shown to the set terminals of the space left and space right flip-flops F911 (FIG. 1(c-e)) and F1008 (FIG. 1(d-e)) respectively. One input to the gate 945 (FIG. 1(c-e)) is received from the output of a group of "or" circuits to which is applied the status levels E, R, M, A, or S. Note that the operation levels A, and S are passed through an "or" circuit not shown but indicated by the use of commas by the convention mentioned above. A second input to the gate 945 is the status level RO03. The first timing pulse T1 is applied as the third input to the gate 945. The operation level A was high when the O register received the information during RO01 while the instruction was being staticized. Accordingly, during the status level RO03 while the operation A was being staticized, the first timing pulse T1 was passed through the gate 945 to set both the space left and space right flip-flops F911 (FIG. 1(c-e)) and F1008 (FIG. 1(d-e)). Thus space left and space right flip-flops are set preparatory to starting the search for the least significant digits of the addend and augend.

A three-input gate 699 (FIG. 1(c-b), lower left) is primed by any one of the high operation levels B, L, A, R, S, V, Q, or M from a suitable "or" circuit (indicated by the operation level letters with commas interposed). The gate 699 receives as a second input the high status level RS or RO applied through the "or" circuit shown. Also the first timing pulse T1 is applied to 699. The output of the gate 699 is applied through "or" circuits to a set of nine two-input gates 640. Each of the nine gates 640 are opened simultaneously by the application of a pulse from the output of the gate 699. The second input for each of the gates 640 is from the output of each of the nine stages, respectively, of the A counter 10 (that is, from each of the "one" terminals thereof). The output of the gates 640 are applied through suitable "or" circuits, as indicated to the address circuits of the left HSM 15 (FIG. 1(c-c)).

Therefore, on occurrence of the first timing pulse T1,

the count in the A counter 10 (FIG. 1(c-b)) is passed to the address circuits of the left HSM 15 (FIG. 1(c-c)).

A three-input gate 692 (FIG. 1(d-b)) receives either of the high status level RS or RO applied through an "or" circuit. Another input of the gate 692 is from "or" circuits to which are applied the various operation levels B, L, A, R, S, V, and Q, as indicated. The third input to the gate 692 is from the first timing pulse T1. The output of the gate 692 is applied through "or" circuits to each of a set of nine, two-input gates 670. The gates 670 have inputs connected to receive respectively the different outputs of the stages of the B counter 11, in the same manner that the gates 640 are connected to the A counter 10. The output of the gates 670 are connected to the address circuits of the right HSM 16 (FIG. 1(d-c)). Therefore, in operation, on occurrence of the first timing pulse T1, the gates 670 pass the count in the B counter 11 (FIG. 1(c-b)) to the address circuits of the right HSM 16 (FIG. 1(d-c)).

A three-input gate 404 (FIG. 1(c-a)) is connected to be primed by the output from the "one" terminal of the space left flip-flop F911 (FIG. 1(c-e)). Recall that the space right and space left flip-flops F911 and F1008 are set. The gate 404 is also primed by the high status level RS. The third input for the gate 404 is the first timing pulse T1. The output of the gate 404 is applied to the reset terminal R of the A register 26. Accordingly, in operation, the A register 26 is reset by the first timing pulse T1.

T2

A four-input gate 508 (FIG. 1(d-b)) has as one input the operation levels A, S, M, B, R, or L applied through a suitable "or" circuits. The gate 508 has a second input the high status level RS or ROM applied through an "or" circuit. A third input to the gate 508 is from the high status level ROM or the high "one" terminal of the space right flip-flop F1008 (FIG. 1(d-e)) now in set condition, applied through an "or" circuit. The second timing pulse T2 is applied as the fourth input to the gate 508. The output of the gate 508 is applied to the trigger terminal T of the B counter 11. The trigger terminal T is that of the lowest order stage of the B counter 11. Therefore, on occurrence of the second timing pulse T2 the B counter 11 count is advanced one.

A four-input gate 505 (FIG. 1(c-b)) has as one input the high "one" terminal of the space left flip-flop F911 (FIG. 1(c-e)). The gate 505 (FIG. 1(c-b)) receives as its second input any of the high operation levels B, L, A, R, S, or M applied through "or" circuits. The gate 505 also receives the status level RS. The gate 505 receives as the fourth input the third timing pulse T3. The output of the gate 505 is applied through an "or" circuit to trigger the first ((that is, lowest order) stage of the A counter 10 corresponding to the least significant binary digit (2⁰ bit) of its binary count, this trigger terminal being designated by T. Accordingly, with the third timing pulse T3, the A counter 10 is advanced one count.

The A and B counters 10 and 11, respectively, originally contained an address of the first six-bit character (supposedly), of two operands, that is, the address of the least significant place of the addend and augend items respectively. However, the machine is arranged to operate with variable as well as with non-standard maximum item lengths. The digits actually present in an item therefore may be less than the maximum number of locations allowed by the programmer for that item, for example 374—, the period in the middle of the line representing an item separator symbol (ISS). Because only the address of the least significant place in the item is employed, it may be necessary to perform several RS (searching) cycles before the actual least significant digit is located. These counters (A and B counters 10 and 11) have now been advanced to the address of the next significant digit of the memory places allotted by the programmer for the items.

43
T4

A three-input gate 902 (FIG. 1(b-d)) receives as one input the output from the "one" terminal of the space left flip-flop F911, which is in its set condition as mentioned before. The gate 902 also receives the high status level RS. The fourth timing pulse T4 is applied as the third input to the gate 902. The output of the gate 902 is applied through an "or" circuit to the reset terminal R (all of the reset terminals) of the Y register 12. Accordingly, the Y register 13 (FIG. 1(c-d)) is reset by the fourth timing pulse T4.

A three-input gate 1042 (FIG. 1(d-d)), is primed by the high "one" terminal of the space right flip-flop F1008, in set condition as pointed out before. The gate 1042 also receives the status level RS. The gate 1042 receives as the third input the fourth timing pulse T4. The output of the gate 1042 after passing through certain "or" circuits, is applied to a delay circuit D56. The delay of the delay circuit D56 is less than the time between the fourth and fifth timing pulses T4 and T5. The output of the delay D56 is applied through various "or" circuits to the reset terminal R (the reset terminals of all the flip-flops) of the Z register 14. Accordingly, the Z register 14 is now reset.

T6

Note that the two-input left read-out gate 730 (FIG. 1(c-c)) is associated with the read-out circuits of the left HSM 15. This read-out gate 730 has been mentioned before. The output of the left read-out gate 730 is now high, because the operation level A and the status level RS are high. The output of the gate 730 is applied to the read-out circuits of the left memory HSM 15. Accordingly, the left HSM 15 is in condition for read-out. Similarly, the right HSM 16 (FIG. 1(d-c)) has associated with it a right read-out gate 862, previously described. The output of the right read-out gate 862 is high in a manner similar to that of the left read-out gate 730 (note inputs from FIG. 1(c-c)) to right read-out gate 730 of FIG. 1(d-c)). The output of the right read-out gate 862 is applied to the read-out circuits of the right HSM 16 through an "or" circuit. Accordingly, the right HSM 16 is in condition for read-out.

A three-input gate 918 (FIG. 1(c-d)) is primed by the space left flip-flop F911 "one" terminal. A second input to the gate 918 is from the status level RS, which is high. A third input from the gate 918 is from the sixth timing pulse T6. The output of the gate 918 is applied to each of a set of seven gates 911. The other input to each of the gates 911 is from the different "one" terminals of the seven addressed elements of the left HSM 15. Therefore, on the occurrence of the sixth timing pulse T6 a pulse is passed through the gate 918. Corresponding pulses for the seven elements of the left HSM 15 currently being addressed apply pulses (when "ones" are stored in the corresponding memory elements) to the corresponding stages or flip-flops of the Y register 13. Accordingly, those stages or flip-flops of the Y register 13 are now set if the corresponding "bits" from the left HSM 15 are "ones," and remain reset if the corresponding bits are zeroes. It is in this same fashion that the characters are transferred into the various registers and counters in their binary coded groups.

A four-input gate 1031 (FIG. 1(c-d), near right-hand margin) has one input connected to receive the output from the "one" terminal of the space right flip-flop F1008. Another input to the gate 1031 is designated "NOT S." Such an input can be obtained by passing the operation level S through a direct current inverter. Then, when the operation level S (subtract) is high, the level "not S" is low, and when the operation level S is low, the operation level "not S" is high. Since the operation level A is high, and all the other operation levels are low, the "not S" level is high, and the gate 1031 is primed by the "not S" input. A third input to the

44

gate 1031 is from the status level RS. The gate 1031 also receives as its fourth input, the sixth timing pulse T6. The output of the gate 1031 is applied through an "or" circuit to each of a set of seven gates 1032 (FIG. 1(d-d), near left margin). The gates 1032 each receive one input from the right HSM 16 elements being read-out from the right HSM 16 (FIG. 1(d-c)). Accordingly, the seven "bits" of information from the right HSM 16 pass through the gates 1032 (FIG. 1(d-d)). The outputs of these gates 1032 are connected to the various corresponding set terminals of the Z register 14.

Accordingly, with the occurrence of the sixth timing pulse T6, there are entered in the Y and Z registers 13 (FIG. 1(c-d)) and 14 (FIG. 1(d-d)), respectively, the seven bits read out of the left HSM 15 at the lowest possible address of the addend item, and the seven bits read out of the right HSM 16 at the lowest possible address of the augend item.

T7

A two-input gate 944 (FIG. 1(d-e)) has as one input the status level RS or ROM applied through an "or" circuit, and as the second input the seventh timing pulse T7. Therefore, the seventh timing pulse T7 is passed by gate 944 through suitable "or" circuits to reset both the space-right and space left flip-flops F1008 (FIG. 1(d-e)) and F911 (FIG. 1(c-e)).

T8

Various of the output terminals of the Y register 13 (FIG. 1(c-d)) are connected to a group of logical "or" circuits 923 (FIG. 1(b-d)) indicated by a rectangle, in the left symbol recognition circuits 22. The output of these "or" circuits R923 are labelled NOT SPL (not space left). The symbol, or group of bits, or binary number of seven digits, indicating a space, are assigned according to code. The seventh, parity bit may be ignored, since it is a redundant check bit. The logical "or" circuits R923 are a group of "or" circuits so connected that if and only if the six, significant outputs from the Y register 13 stages correspond to the code symbol for a space, the output of the "or" circuits R923 is at a low level. For example, reference may be made to the Harvard Annals for Computation, vol. 27, entitled "Synthesis of Electronic Computing and Control Circuits" published by Harvard University Press, from which such recognition circuits may be synthesized by those skilled in the art. On the other hand, if the symbol coded by the "output" terminals from the Y register 13 are any other than a space symbol, the output of the not space left "or" circuits R923 is high. Accordingly, the output NOT SPL of the not space left circuits is applied to a direct current inverter, the SPL inverter 13. The output level of the inverter may be designated space-left, indicated SPL. This space left inverter output is high if, and only if, the output from the Y register 13 contents are a space character, in code.

A three-input gate 938 (FIG. 1(c-e)) receives as one input the output from the lead SPL of the space left inverter 13. Also applied to a gate 938 is a group of levels designated "NOT (B, L, R, W, H)." This designation indicates that the operation levels B, L, R, W, and H have been applied to an "or" circuit and the output of this "or" circuit has been passed through a direct current inverter (not shown). Accordingly, the output of this last-named inverter may be termed "NOT (B, L, R, W, and H)," and is high only if none of the operation levels B, L, R, W, or H is high. The operations matrix level that is high is operation A. Thus, the lead "NOT (B, L, R, W, H)" is high, and the gate 938 is primed from this second input. The eighth timing pulse T8 is applied as the third input to the gate 938. The output of gate 938 is applied to the set terminal S of the space left flip-flop F911. Therefore, the eighth timing pulse T8 sets the space left flip-flop F911 in the event, and only in the event, that a space character is stored in the

Y register 13 and therefore recognized in the left symbol recognition circuits 22.

Among the right symbol recognition circuits 23 is a "not space right" group of "or" circuits designated R1052 in a rectangle (FIG. 1(d-d)). The "or" circuits R1052, the output of which may be designated not space right (NOT SPR) is applied to an inverter I4 (FIG. 1(d-e)) which may be termed the space right inverter. The not space right "or" circuits R1052 (FIG. 1(d-d)) are similar to the not space left "or" circuits R923 (FIG. 1(b-d)). The input to the not space right "or" circuits R1052 (FIG. 1(d-d)), however, is received from the outputs of the Z register 14. Accordingly, the space right lead SPR from the space right inverter I is high if and only if a space character, or coded symbol, is recognized in the Z register 14 by the right symbol recognition circuits 23. The output of the SPR lead is applied through a suitable "or" circuit to a three-input gate 1057 (FIG. 1(d-e)), which is also primed by the status level RS. The eighth timing pulse T8 is applied as the third input to the gate 1057, and accordingly is passed by the gate 1047 through an "or" circuit to set the space right flip-flop F1008 if a space character is stored in the Z register 14.

At this point the apparatus is substantially in the same condition as when the status level RS together with the operation level A was high, and the first timing pulse T1 was applied, with the exception that: The A counter 10 and the B counter 11 contain respectively the addresses of the second spaces reserved for the addend and augend items, respectively, reading from the least significant place.

Note that if the left symbol recognition circuits 22 and the right symbol recognition circuits 23 each finds a space, the cycle of high status level RS is repeated. Status level RS is high and no status transition gate is activated. However, if a digit that is not a space character is read out of the Y register 13, for example, the space left lead SPL, applied to the input of the gate 938 (FIG. 1(c-e)) is low, and not high, when the eighth timing pulse T8 is applied to the gate 938. Consequently at the eighth timing pulse T8, the space left flip-flop F911 remains in its reset condition, to which condition it was placed by the preceding seventh timing pulse T7 from the gate 944 (FIG. 1(d-e)). With the space left flip-flop F911 (FIG. 1(c-e)) in the reset condition, the "one" output of this last-named flip-flop is low. Therefore the gate 902 (FIG. 1(b-d)) cannot pass the fourth timing pulse T4 to reset the Y register 13 (FIG. 1(c-d)). Also the sixth timing pulse T6 cannot pass the gate 918 (FIG. 1(c-d)) to set the Y register 13 (FIG. 1(c-d)). Consequently, the least significant digit of the addend from the left HSM 15 is held in the Y register 13. Furthermore, the gate 505 (FIG. 1(c-d)) associated with the A counter 10 is not primed by the "one" output of the space left flip-flop F911. Therefore the A10 counter holds the address of the second least significant digit of the addend until, as appears hereinafter, a digit is recognized in the Z register 14 by the right recognition circuits 23.

On the other hand, if a digit is recognized in the right symbol recognition circuits 23, a similar action occurs. The space right lead SPR from inverter I4 of FIG. 1(d-e) is low, so that the gate 1057 (FIG. 1(d-e)) cannot pass the eighth timing pulse T8. The "one" output of the space right flip-flop F1008 is low. Therefore, the gate 1042 (FIG. 1(d-d)) does not pass the succeeding fourth timing pulse T4 to reset, after passing through the delay circuit D56, the Z register 14. Therefore, the Z register 14 retains the digit recognized in the right symbol recognition circuits 23. At the same time, the count in the B counter 11 is not advanced because the low level on the "one" lead of the space right flip-flop F1108 leaves the gate 508 (FIG. 1(d-b)) associated with the B counter 11 closed, and a unit is not added to the count in the B counter 11.

Accordingly, the machine now follows one of four courses: First, the search continues with RS cycles for each memory; second the Y register 13 retains the first digit of the addend and the high status level RS persists until a digit is recognized by the right symbol recognition circuits 23; or, third, the first digit of the augend is retained by the Z register 14, and the high status level RS persists and the search continues for the least significant digit in the addend; or, fourth, the least significant digit of the addend and of the augend are recognized in the same RS cycle by the left symbol recognition circuits 22 and the right symbol recognition circuit 23. In the first three cases, the operation is clear from what has been said heretofore.

At the time that the least significant digit of both addend and augend is found in the Y and Z registers 13 and 14, respectively, the A counter 10 holds the address of the next succeeding least significant digit of the addend, and the B counter 11 holds the address of the next least significant character of the augend.

When a non-space character is thus recognized in each of the Y and Z registers 13 and 14, a status transition gate 1255 (FIG. 1G) is actuated.

The status transition gate 1255 is a six-input gate. Two of the inputs are from the "not space left" NOT SPL and "not space right" NOT SPR leads respectively. A third input to the status transition gate 1255 is from the output of an "or" circuit R1053 (FIG. 1(d-d)) among the right symbol recognition circuits 23. The output of the "or" circuit R1053 is designated NOT SPMR. The lead designated "NOT SPMR" is at a high level, so far as the present operation A is concerned.

The operation level E (for justify right) and the operation level M (for multiplication) through an "or" circuit are applied to an inverter I5 (FIG. 1G). The output of the inverter is representative of "neither M nor E," that is, this output is at a high level if, and only if, both operation levels E and M are low. The output of the inverter I5 is then applied as the fourth input to the status transition gate 1255, the output of this inverter I5 is high since operation level A is high. A fifth input to the status transition gate 1255 is from the status level RS (for search). The sixth input to the status transition gate 1255 is from the eighth delayed timing pulse T8a.

Accordingly, the eighth delayed timing pulse T8a is passed by the status transition gate 1255 to the "set RI" lead to set the status level control flip-flop F1289, in the manner explained heretofore. The status level RS (for search) is now low, and the status level for RI (for read-in) is high.

As will appear more fully, the addend and the augend are to be added digit by digit. The addition of the least significant digits of the addend and the augend is now to occur.

5.1.2 Status Level RI High, First Cycle

T1

Whether the result is to be stored in the left HSM 15 or the right HSM 16 depends on the 2⁹ (10th) bit stored in the C register 28 (FIG. 1(c-a)). If the flip-flop corresponding to the 2⁹ (10th) bit of C register 28 is set so that the "one" output is high, then a four-input gate 694 (FIG. 1(c-b)) is primed from the "one" terminal of the 2⁹ bit flip-flop of the C register 28. This terminal may be designated 2⁹ (1) of the C register 28. Status level RI is a second input to the gate 694. A third input to the gate 694 is the output of an "or" circuit having as inputs the status levels B, L, A, R, S, or M. The fourth input to the gate 694 is the first timing pulse T1.

Accordingly, the first timing pulse T1 is passed by the gate 694 to prime a set of nine, two-input gates 660. The second input to the gates 660 are the respective outputs of the C counter 12. Accordingly, the address stored

in the C counter 12 passes through these gates 660 and an "or" circuit to the address circuits of the right HSM 16 (FIG. 1(d-c)).

On the other hand, the "zero" output of the 2⁹ bit flip-flop of the C register 28 is applied to a four-input gate 698 (FIG. 1(c-b)), with the same inputs, except for the input from the C register 28, as that of the gate 694. Therefore, if the "zero" output of the 2⁹ bit flip-flop of the C register 28 is reset, the first timing pulse T1, is passed by the gate 698 to each of a set of nine, two-input gates 650. The gates 650 are connected to pass, when thus opened, the address from the C counter 12 to the left HSM 15.

Accordingly, the left or right HSM 15, or 16 is addressed by the information stored in the C counter 12, according as the 2⁹ flip-flop is reset or set respectively.

The gate 860 (FIG. 1(e-c)) passes the first timing pulse T1 through an "or" circuit to the lead xx and thus to reset terminals R of the R register 19 (FIG. 1(d-c)) and also the L register 18 (FIG. 1(b-c)). The R register 19 and the L register 18, all stages, are reset and in effect cleared.

A gate G4 (FIG. 1(e-a)) is primed by the high status level RI to pass the first timing pulse T1 to the set terminal of an adder input flip-flop F3. The "one" output of the adder input flip-flop F3 is applied as a first input to a set of six, three-input gates G27. The six gates G27 each receive as a second input the output of an inverter 17 (FIG. 1(c-e)). The input of the inverter 17 is from the output of an "or" circuit having two inputs, one from the "one" output of an item separation symbol left (ISSL) flip-flop F910 (FIG. 1(c-e)); and one from the space left flip-flop F911 "one" terminal. The space left (SPL) and the item separation symbol left (ISSL) flip-flops F910 and F911 are both in the reset condition at this point. Note that the R001-T1 reset output of the gate 943 (FIG. 1(d-e)) is applied through "or" circuits to the reset terminals of these flip-flops, which were therefore reset when the instruction were staticized. With both of these flip-flops F910 and F911 (FIG. 1(c-e)) reset, the inverter 17 applies a high output as the third input to the gates G27 (and G21) (FIG. 1(e-a)) and these gates are open. To the six gates G27 are applied respectively the six binary digits (bits), as levels from the corresponding "one" terminals of the Y register 13, except for the parity bit, and thence the six bits pass through these gates, when open, to the binary adder.

The six "significant" bits (so-called to exclude the redundant parity bit) of the augend from the Z register 14 (FIG. 1(d-d)) are applied through a set of six, two-input gates 1048 (FIG. 1(d-d)) each of which receives as one input the high operation level A, S, M, or B through suitable "or" circuits, as indicated. The output from the gates 1048 are applied through a set of six, two-input gates G21 to the duplicated adders 17A. The second input to the gates G21 is from the "one" output of the adder-input flip-flop F3.

Accordingly, the six bits from the Z register 14 (FIG. 1(d-d)) are passed through the gates G21 (FIG. 1(e-a)) and the six bits from the Y register 13 (FIG. 1(c-d)) are passed through the gates G27 (FIG. 1(e-d)) to the input of the duplicated adders 17A (FIG. 1(e-b)).

T1½-T3

An adder output flip-flop F4 (FIG. 1(e-c)) has a set terminal S which receives the output of a gate G10. The adder output flip-flop F4 reset terminal R receives the output of a gate G11. The gates G10 and G11 are primed by the high status level RI. The gate G10, when primed, passes a timing pulse designated T1½. The gate G11, when primed, passes a timing pulse designated T3.

Note that certain timing pulses are designated T1½. This designates, as may be supposed, that the timing pulse T1½ occurs at a time half way between the first and second timing pulses T1 and T2. Similarly, T1¾ indi-

cates that the timing pulse designated occurs with a delay after the occurrence of the first timing pulse T1 of three-quarters of the time between the first and second timing pulses T1 and T2. In like manner the timing pulse T2¾ occurs at a time after the timing pulse T2 delayed by three-fourths of the time between the timing pulses T2 and T3. Such pulses may be derived by suitable delay circuits (not shown in detail).

Accordingly, the "one" terminal of the adder output flip-flop clocks the duplicated adders 17A internally from the one and a half timing pulse T1½ to the third timing pulse T3. Note that the adder is actuated after the gates G21 and G27 (which pass information into the adder 17A) open, and close before the gates G21 and G27 close. The adder output flip-flop also illustrates (as does the adder input flip-flop F3) how a "long" pulse may be obtained.

A gate G9 (FIG. 1(e-c)) is primed through suitable "or" circuits by any one of the high operation levels A, S, or M from an "or" circuit. Another input to the gate G9 is from the high status level RI. The gate G9 is also primed by a long pulse timed from T1¾ and T2¾. This long pulse thus applied clocks the BCDC 17B (FIG. 1(e-b)) and controls certain gates (not shown) to gate the output of the adder to enter the BCDC 17B to be converted to binary coded. A long pulse from T1¾ to T2¾ gates the output of BCDC 17B and the parity generator included therein. The output of a first of the duplicated BCDC 17B is applied to a set of five gates 717 (FIG. 1(f-c)), one of which corresponds to the 2⁶ (seventh) bit and the other four respectively to the 2⁹ to 2³ bits. A set of five gates 841 (FIG. 1(e-b)) receive the corresponding five bits from the second BCDC 17B, one corresponding to the 2⁶ bit and the other four respectively to the 2⁹ to 2³ bits.

Each of the five gates (those corresponding to the 2⁹ to 2³ and 2⁶ bits) of each set of gates 717 (FIG. 1(f-c)) and 841 (FIG. 1(e-b)) has three inputs, one from the BCDC as already mentioned. A second input to each of the gates 717 and 841 is from the output of an "or" circuit having as inputs the operation levels A, S, and M. The third input to each of the five gates 717 and the five gates 841 is from an "or" circuit having as inputs: the operation levels A and S, the output from a lead designated "nines counter not nine" from the nines counter 45 (FIG. 1(f-c)), and the output from the "one" terminal of a "been in RN" flip-flop F1111 (FIG. 1(e-a)). The nines counter 45 and the been in RN flip-flop F1111 will be described more fully hereinafter. For the present, it is enough to state that the "nines counter not nine" lead and the "one" terminal of the been in RN flip-flop F1111 are at a high level.

Accordingly, the gates 817 are open to pass the four least significant bits from one of the duplicated BCDC 17B, through suitable "or" circuits to the L register 18 (FIG. 1(b-d)), to the corresponding set terminals of the four lowest order flip-flops thereof.

Accordingly, the five gates 841 are open to pass the 2⁹ to 2³ and 2⁶ bits from the auxiliary or second binary coded-decimal converter BCDC 17B, through suitable "or" circuits to the R register 19 (FIG. 1(d-c)) to the corresponding set terminals thereof.

A three gate 872 (FIG. 1(e-b)) is primed by any of the high levels from operation levels A or S, "nines counter not nine" lead, or the "one" terminal of the been in RN flip-flop F1111, through suitable "or" circuits in the same manner as the four gates of the gates 841. The gate 872 has a second input applied from the status level RI. The third input to the gate 872 is the second timing pulse T2. The output of the gate 872 is applied to set the 2⁴ bit flip-flop (which corresponds to the fifth least significant bit or fifth lowest order flip-flop) of the R register 19 (FIG. 1(d-c)).

A gate 749 (FIG. 1(b-d)) has inputs the same as those just described to the gate 872. The output of the

gate 749 is applied to set the 2⁴ bit flip-flop of the L register 18.

Among the gates 841 just described, is a 2⁶ gate. It is assumed that included in the binary to coded-decimal converter 17B (if desired, in only one of the duplicated converters) is a parity generator. Such a generator is shown and described hereinafter. The 2⁴ bit (the fifth least significant bit) in the R register 19, is always set by the second timing pulse T2 from the gate 872. This is due to the fact that in the alpha-numeric code of this machine all numerics are coded to include a binary "one" in the fifth binary place. The sixth least significant bit corresponding to the 2⁵ bit is always a binary zero for numerics in the code of this machine. Consequently, as the R register 19 (FIG. 1(d-c)) is in the reset condition, no input is applied to the 2⁵ (that is, sixth lowest order) flip-flop, and the sixth bit in the register remains as a binary "zero." In the present machine, the seventh (26) bit represents a parity check bit. An even parity code is employed. Accordingly, since the fifth and sixth bits total only one for the numbers being read into the R register 19, only the first four bits corresponding to the 2⁰ to 2³ bits are tested in a parity generator included in the BCDC 17B. If the sum of these four bits is odd, the output from the parity generator circuit included in the BCDC 17B is a low level corresponding to a "zero" clocked out with the other outputs from T1¾ to T2¾. Then the total of the fifth and sixth bits is one, and the total of all the six bits is even so that the parity or seventh bit should then be zero. However, if the first four bits add up even, then, it being known that the fifth and sixth bits add only one, the parity generator puts out a "high" output, or pulse, in the clocked interval. The parity signal thus regenerated is applied through the 2⁶ gate of the gates 871 and this parity signal is indicated as "from parity generator to 2⁶ gate." Accordingly, with the second timing pulse T2, all seven bits corresponding to any coded-decimal number, including the parity bit, is appropriately entered into the R register 19.

In the same way the parity bit generated by the parity generator in the BCDC 17B is applied to a 2⁵ gate of the gates 717 (FIG. 1(f-c)) designated, respectively, 2⁵ and 2⁰ to 2³. As already described, these gates 717 are similar to, and primed in the same way as, the gates 841 of FIG. 1(e-b) and the same description is applicable, except that the coded input is from the first BCDC 17B, and the output from gates 717 is applied through "or" circuits to the L register 18 (FIG. 1(b-c)).

Accordingly, there are entered in each of the L register 18 (FIG. 1(b-c)) and the R register 19 (FIG. 1(d-c)) seven bits properly coded according to the code employed in this machine, representing the sum digit of the two digits entered in the Y and Z registers 13 and 14 (FIGS. 1(c-d) and 1(d-d)).

As pointed out above, a parity generation is used in this fashion because the adder is only a four-input adder, but the code of this machine for a decimal number consists of six bits. The 2⁴ and 2⁵ bits (the fifth and sixth bits, by which is meant the bits of fifth and sixth order) for all decimal numbers in this code are the same, with the 2⁴ bit a "one" and the 2⁵ bit a "zero." Therefore, by setting the 2⁴ bit in the L and R registers 18 and 19, the proper binary representation for the number is set into these registers before the number is read into the HSM 15, 16.

A three-input gate 380 (FIG. 1(c-a)) has applied to it from a suitable "or" circuit (as indicated) any of the high operation level B, L, A, R, S, or N. The gate 380 also has applied to it as a second input the high status level RI. The second timing pulse T2 is applied as the third input to the gate 380. The output of the gate 380 is passed through suitable "or" circuits to a trigger input T (of the lowest order stage) of the C counter 12 (FIG. 1(c-d)).

Accordingly, the C counter 12 is advanced by one

count to the address in the HSM 15 or 16 of the next (in this case the second) least significant digit of the sum. Remember that at the first timing pulse T1, with status level RI high, the gates 650 and 660 have passed to the left or right HSM 15, 16 memory circuits, the address of the least significant digit of the sum. The C counter 12 is a reversible counter which may include, for example, a gating circuit (not shown) at its trigger input. When an "add" level or lead has a "high" voltage, applied to one gate of the gating circuit, the trigger impulse is applied in such a way as to advance the C counter 12 count. Another "subtract" level applied to the gating circuit, when high, causes the trigger pulses passed therethrough to reverse the C counter 12 count, that is, reduce the C counter 12 by one count for each trigger impulse. Such a circuit is disclosed, for example in the patent to Flory and Morton, No. 2,462,275, dated February 22, 1949.

A reversing flip-flop F302 (FIG. 1(c-b)) has its zero output applied to the "add" terminal of the C counter 12, and its "one" output applied to the subtract "sub" terminal of the C counter 12. When the "zero" output of the flip-flop F302 is high, the C counter 12 advances its count by one for each trigger impulses received at trigger terminal T. On the other hand, when the flip-flop F302 "one" output is high, the C counter 12 subtracts one from its count for each trigger T input pulse. Note that a two-input gate 312 is provided which receives as one input the status level RO03 and as the second input the third timing pulse T3. The output of the gate 312 is applied to the reset terminal R of the flip-flop F302. Therefore, when the last one-third of the last instruction was being read from the memory, the third timing pulse T3 was passed by the gate 312 to reset the flip-flop F302. The C counter 12 is thus in condition to add for each trigger impulse applied.

Note that a gate 313 is primed by any of the high operation levels W, H, or N, and also by the high status level RO03. The gate 313 also receives the eighth timing pulse T8. Therefore, the flip-flop F302 is set by the eighth timing pulse when the status level RO03 is high only for operation W, H, or N.

Accordingly, the gate 380 (FIG. 1(c-a)) passes the second timing pulse T2, applied thereto, to the trigger input T of the C counter 12 (FIG. 1(c-b)); and the C counter 12 count is advanced to hold the address of the next least significant digit of the sum now being computed. Remember that the HSM 15, 16 address circuits have already been activated to the address of the first digit of the sum.

T3

The gate G11 (FIG. 1(e-c)) is primed by the high status level RI, as already explained, to pass the third timing pulse T3. Accordingly, as heretofore explained, the adder output flip-flop F4 is placed in the reset condition. Also, the timing pulse T3½ is applied through a two-input gate G3 (FIG. 1(e-a)) primed by the status level RI and resets the adder input flip-flop F3. Accordingly, the adder input flip-flop F3 is in the reset condition.

Notice that the sum digit is now in each of the L and R registers 18 and 19 (FIGS. 1(b-c) and 1(d-c)). The left read out and the right read out gates 730 (FIGS. 1(c-c) and 1(d-c)) respectively are both closed, so that the read-out circuits of the HSM 15 and 16 are inactivated.

T4

A gate G6 (FIG. 1(f-b)) has two inputs, one from the status level RI and the other from the fourth timing pulse T4. The gate G7 output is applied through an "or" circuit to the reset terminal R of a so-called "carry" flip-flop F2, the function of which is more fully described hereinafter. Accordingly, the carry flip-flop F2 is in reset condition.

51
T6

A four-input gate 721 (FIG. 1(c-c)) called the left read-in gate receives as one input the output from the "zero" terminal of the 2⁹ bit from the C register 28 (FIG. 1(c-a)). This zero output of the 2⁹ bit flip-flop (10th order flip-flop) of the C register 28 is applied through "or" circuits to the other inputs of which (see FIG. 1(c-c)) are applied the operation levels X and J, and operation level P. A second input to the gate 721 is from an "or" circuit receiving the high status levels RI and RIS. A third input to the gate 721 is from an inverter 18 (FIG. 1(b-c)) to which is applied through an "or" circuits the operation levels J and X, and the status level RIS. The output of the inverter 18 applied to the gate 721 is therefore high if both the operation level J is low and the operation level X is low. By suitable "or" circuits, there is applied to this same third input of the gate 721 the output from the "zero" terminal of the 2¹⁰ bit of the C register 28 of FIG. 1(c-a).

The fourth input to the left read-in gate 721 of FIG. 1(c-c) is from an "or" circuit having as inputs the operation level P and the "zero" terminal of the 2¹¹ bit flip-flop of the C register 28.

The output of the left read-in gate 721 is applied through an "or" circuit to the "read-in" (write-in) circuits of the left HSM 15.

A right read-in gate 850 (FIG. 1(d-c)) is provided for the right HSM 16. The gate 850 is similar to the gate 721 for the left HSM 15 and has similar inputs except that an inverter 19 (FIG. 1(d-b)) is employed (instead of the inverter 18) but with like inputs and output; and, instead of the input from the zero terminal of the 2¹⁰ bit flip-flop of the C register 28, there is applied to that "or" circuit through which the inverter 19 output and the status level RIS are applied to the gate 850 (FIG. 1(d-c)) the output from the "one" terminal of the 2¹⁰ flip-flop of the C register 28; further, through the gate 850 input receiving through "or" circuits the operation levels J, or X, or P, there is applied, through these "or" circuits, the output from the "one" terminal of the 2⁹ bit flip-flop of the C register 28 (rather than the zero terminal). With these exceptions, the right read-in gate 850 circuit is similar to the left read-in gate 721 circuit. The output of the right read-in gate 850 (FIG. 1(d-c)) is applied to the "read-in" ("write-in") circuits of the right HSM 16.

Accordingly, the left HSM 15 (FIG. 1(d-c)) (and not the right HSM 16) is in condition to receive information of the "zero" output of the 2⁹ bit flip-flop (indicated 2⁹ (0)) of C register 28 is high. On the other hand, if the "one" output of the 2⁹ bit flip-flop (indicated 2⁹ (1)) of the C register 28 is high, then the right HSM 16 is in condition to receive information and not the left HSM 15.

Referring again to FIG. 1(e-b) and the BCDC 17B, if there is a carry, a pre-carry flip-flop F1 receives at its set terminal S the carry output, which is a pulse from terminal C of the BCDC 17B. The "one" output of the pre-carry flip-flop F1 is applied to a three-input gate G8. The gate G8 receives as its second input the high status level RI, and as the third input thereto the sixth timing pulse T6.

Accordingly, if there is a carry the sixth timing pulse T6 passes through the gate G8 to the set terminal S of the carry flip-flop F2. Thus the carry flip-flop F2 is set, if the carry from the BCDC 17B has set the pre-carry flip-flop F1.

Note that a gate G5 is provided. Gate G5 has two inputs, the high status level RO01 and the seventh timing pulse T7. Accordingly, the carry flip-flop F2 is always reset during staticizing of the instructions. The gate G6 described above, insures that the carry flip-flop F2 is reset just before it may be set by the output from gate G8.

52
T7

A two-input gate G7 (FIG. 1(e-b)) has applied to it as one input the output of an "or" circuit receiving the status level RO01 and the status level RI. The second input to the gate G7 is the seventh timing pulse T7. The output of the gate G7 is applied to the reset terminal R of the pre-carry flip-flop F1. Therefore, the seventh timing pulse T7 is applied to the reset terminal R of the pre-carry flip-flop F1. Note that in the staticizing of instructions, the pre-carry flip-flop F1 is also reset, by the output of the same gate G7, thus preparing for any new carry from the BCDC 17B. Thus, the carry flip-flop F2 (FIG. 1(f-b)) retains a "carry" indication when set. As will appear hereinafter, the carry retained in the carry flip-flop F2 is added into the adder 17A (FIG. 1(e-b)) in the next cycle of the status level RI high during which the next least significant digits of the addend and augend are being added. The pre-carry flip-flop F1 is then available to receive the carry of the second addition, if there should be such a carry.

The first equal circuit 20 (FIG. 1(d-c)) may be similar to the third equal circuit 50, already described. The equal circuit 20 receives inputs from corresponding stages of the R register 19 (FIG. 1(d-c)) and the L register 18 (FIG. 1(b-c)). Thus the same inputs are applied to the first equal circuit 20 (FIG. 1(d-c)) from each of the L and R registers 18 and 19 provided the arithmetic performed by the duplicated adder and BCDC 17 has been the same, and together with the new fifth, sixth, and seventh least significant digits supplied by the various circuits heretofore mentioned. The output of the equal circuit 20 is "clocked" at the seventh timing pulse T7. If, and only if, the inputs from the L and R registers 18 and 19 are equal, the output from the first equal circuit 20 applies a pulse at the seventh timing pulse T7 to the reset terminal R of the compare flip-flop F707 (FIG. 1(a-c)) of the alarm circuits 48. Note that prior to the application of the pulse from the first equal circuit 20, a gate 748 primed by the high operation level RI and by any one of the high operation levels B, L, A, R, S, or M, (applied through an "or" circuit) passes the sixth timing pulse T6 to the set terminal of the compare alarm flip-flop F707.

Accordingly the flip-flop F707 of the alarm circuit is in the set condition after the sixth timing pulse T6. On the seventh pulse T7, if the results from the adder and BCDC 17B are the same, the compare alarm flip-flop F707 is reset.

T8

Recall that the eighth delayed timing pulse T8a is generated from the eighth timing pulse T8 and passes the gate 1301 (FIG. 1(a-c)) only in the absence of an alarm. The "no alarm" lead, already described, is taken from the output of an inverter 110. One input to the inverter comes from the "one" output terminal of the compare alarm flip-flop F707. Therefore, if the compare alarm flip-flop F707 fails to be reset by reason of the binary coded sum digit entered in the L and R registers 18 and 19 being unequal, the input to the inverter 110 in the alarm circuit 51 from flip-flop F707 becomes high, the "no alarm" lead goes low, due to the inversion in inverter 110, and the "no alarm" lead input to the gate 1301 in the timing pulse generator TPG is low.

Accordingly, the eighth delayed timing pulse T8a cannot be generated, and an alarm is indicated. The machine then stays in the status level at the time of the detection of the error, which in this instance is the status level RI.

T8a

A four-input status transition gate 1263 (FIG. 1G) receives the high status level RI at one input. At a second input the status transition gate 1263 receives any one of the high operation levels B, L, A, R or S. A

53

third input to the status transition gate 1263 is from the "zero" output of a flip-flop F1110 (FIG. 1(f-c)) identified as EOBO (which may be read as a coined word with long "E" and long "O," and is an abbreviation for "end of both operands"). The reaching of the ends of both operands is indicated by the set condition of the EOBO flip-flop F1110. The fourth input to the status transition gate 1263 is the eighth delayed timing pulse T8a. Therefore, as long as the EOBO flip-flop F1110 remains in its reset condition, and the end of both operands has not been detected or reached, then the status transition gate 1263 passes the eighth delayed timing pulse T8a to the lead "set RO" (FIG. 1(a-e)). Thereupon, in a manner similar to that described heretofore, the status level control flip-flops 47 are reset and the flip-flop F1290 is set. Accordingly, the status level RO now becomes high.

5.1.3 Status Level RO High, First Cycle

T1

With the status level RO high, the gate 699 (FIG. 1(c-b)) is primed to pass the first timing pulse T1 to open the gates 640 to pass the address of the next least significant digit of the addend from the A counter 10 into the address circuits of the left HSM 15 (FIG. 1(c-c)).

Similarly, the gate 692 (FIG. 1(d-b)) is primed by the high operation level RO through the "or" circuit shown, (instead of by the high operation level RS, as before) to pass the first timing pulse T1 to open the gates 670. Thereupon the gates 670 pass the address from the B counter 11 to the address circuits of the right HSM 16 (FIG. 1(d-c)).

T2

The output of a three-input gate 504 (FIG. 1(c-b)) is applied by way of "or" circuits to the trigger terminal T of the A counter 10. One input to gate 504 from any one of the high operation levels B, L, A, R, S, M, or V through an "or" circuit. The gate 504 receives as a second input the high status level RO. The third input to the gate 504 is the second timing pulse T2.

Accordingly, the gate 504 passes the second timing pulse T2 to the trigger terminal T of the A counter 10. The count of the A counter 10 is now advanced to the next digit character of the addend. Note that when the operation level RS was high, the gate 505 passed the pulse to advance the count of the A counter 10.

A three-input gate 509 (FIG. 1(d-b)) receives at one input, through a suitable "or" circuit, any one of the high operation levels B, L, A, R, S, or V. A second input to the gate 509 is the status level RO. The gate 509 receives as the third input the second timing pulse T2. The gate 509 passes the second timing pulse T2, through various "or" circuits, to the trigger terminal T of the B counter 11.

The count of the B counter 11 is thus advanced to the address of the next digit character of the augend.

T4

By way of the left symbol recognition circuits, a minus L flip-flop F909 (FIG. 1(b-d)) is set if a minus character, that is, a character indicating a minus sign, is detected at the output of the Y register 13 (FIG. 1(c-d)). Assume for the present that no such minus sign is detected. This flip-flop F909 (FIG. 1(b-e)) is designated the "minus L" flip-flop.

Note that a two-input gate 943 (FIG. 1(d-e)) is provided having inputs from the high status level RO01, and the first timing pulse T1. The output of this gate 943 is designated "RO01-T1 reset," and is used to "clear" or reset various flip-flops. Thus, through "or" circuits, the "minus L" flip-flop F909 is reset by the output of the gate 943 in the staticizing instructions. So also are the ISSL flip-flop F910 (FIG. 1(c-e)), the space left

54

flip-flop F911, the right flip-flop F1008 (FIG. 1(d-c)), and others.

The "zero" terminal of the "minus L" flip-flop F909 is high. The high "zero" output of the "minus L" flip-flop F909 is applied through suitable "or" circuits (which also apply the high operation levels, V, J, E, or X) to a first input of a three-input gate 903 (FIG. 1(b-d)). The gate 903 has applied to a second input the operation level RO. The third input to the gate 903 is the fourth timing pulse T4. The output of the gate 903 is applied through "or" circuits to the reset terminal R of the Y register 13 (FIG. 1(c-d)).

Accordingly, the Y register 13 is reset (all stages simultaneously).

An "End of Operand Right" flip-flop F1010 (FIG. 1(d-e)) is set by the right symbol recognition circuits 23 only if an end of operand symbol has been recognized. As it has been assumed that no end of operand is recognized, the "End of Operand Right" flip-flop F1010 is in the reset condition. Note that the "End of Operand Right" flip-flop F1010 was reset by the output from the RO01-T1 reset lead (FIG. 1(d-e)), or by the output of the gate 944. The high voltage from the "zero" terminal of the "End of Operand Right" flip-flop F1010 is applied through an "or" circuit to a three-input gate 1043 (see FIG. 1(d-d)). The last-mentioned "or" circuit also passes to the input of the gate 1043 any one of the high operation levels J, E, X, W, or H. A second input of the gate 1043 is the high status level RO. The fourth timing pulse T4 is the third input to the gate 1043.

Accordingly, the gate 1043 passes the fourth timing pulse T4 through various "or" circuits and the delay circuit D56 to the reset terminal R of the Z register 14. Accordingly, all of the flip-flop stages of the Z register 14 are in the reset condition, and thus the Z register 14 is cleared.

T6

The left read-out gate 730 (FIG. 1(c-c)) output is now high due to the high operation level A and the high status level RO, and so also is the right read-out gate 862 (FIG. 1(d-c)), to activate the read-out circuits for the left HSM 15 (FIG. 1(c-c)) and the right HSM 16 (FIG. 1(d-c)) respectively.

A four-input gate 919 (FIG. 1(c-d)) has an output applied through an "or" circuit, as shown, to the gates 911. One input to gate 919 is designated "Not W." This input may be derived through a suitable inverter from the operation level W (write-out-to-tape). Accordingly, the "Not W" input to gate 919 is high. A second input to the gate 919 is applied from the output of a group of "or" circuits passing any one of the high operation levels J, E, X, or V, or the high "zero" terminal of the "minus L" flip-flop F919 (FIG. 1(b-e)). A third input to the gate 919 (FIG. 1(c-d)) is the high status level RO. The fourth input to the gate 919 is from the sixth timing pulse T6.

Accordingly, the sixth timing pulse is passed by the gate 919 through a suitable "or" circuit to the gates 911 to open the latter gates and pass the currently addressed digit character from the left HSM 15 to the Y register 13.

The right symbol recognition circuits 23, if an End of Operand is recognized in the Z register 14 (FIG. 1(d-d)), as will appear more fully hereinafter, cause the "End of Operand Right" flip-flop F1010 (FIG. 1(d-e)) to be set. Assume there is no end of operand character in the Z register 14. Accordingly, the End of Operand Right flip-flop F1010 is in the reset condition. The "zero" output of this End of Operand Right flip-flop F1010 is therefore high and is applied through a suitable "or" circuit which receives also any one of the high operation levels J, E, or X, to one input of a four-input gate 1030 (FIG. 1(c-d)). A second input to the gate 1030 is designated "not S." The "NOT S" lead may be the output of the operation level S passed through an inverter. Ac-

cordingly, the "Not S" input to the gate 1030 is high. A third input to the gate 1030 is derived from an "or" circuit passing any one of the high status levels ROM, RO, or RD. The fourth and final input to the gate 1030 is from the sixth timing pulse T6. The high output of the gate 1030 is applied (through the same "or" circuit receiving also the output of the gate 1031) to the seven gates 1032 when high.

Accordingly, the sixth timing pulse T6 passes by the gate 1030 opens the gates 1032 to enter the currently addressed significant digit character (of seven bits) from the right HSM 16 (FIG. 1(d-e)) into the Z register 14 (FIG. 1(d-d)).

T8a

A three-input status transition gate 1249 (FIG. 1G) has applied to it any one of the operation levels B, L, A, R, S, M, or X, through a suitable "or" circuit. A second input to the status transition gate 1249 is the operation level RO. The third input to the status transition gate 1249 is the eight delayed timing pulse T8a. The output of the status transition gate 1249 is applied the "set RI" lead (FIG. 1(a-e)). In the manner described heretofore, all of the status level control flip-flops 47 are now reset, and the output of the amplifier A1289 is applied to set the RI flip-flop F1289. The status level RI is now high.

The condition of the machine now is that the A counter 10 (FIG. 1(c-b)) contains the address of the third least significant memory location assigned to the addend operand. The B counter 11 (FIG. 1(d-b)) contains the address of the third least significant memory location assigned to the augend operand. The L and R registers 18 and 19 (FIGS. 1(b-d) and 1(d-c)) contain the least significant digit of the sum. Note, however, that the least significant digit of the sum has already been written during the last previous high status level RI into the last or right HSM 15 or 16 (FIG. 1(c-d) or (d-c)) as called for by the instruction. The Y register 13 (FIG. 1(b-c)) contains the second least significant digit or character of the addend operand, and the Z register 14 (FIG. 1(d-c)) contains the second least significant digit or character of the augend operand.

The carry flip-flop F2 is set if there was a carry from the addition of the least significant digits of the operands, and is reset if there was no such carry.

5.1.4 Status Level RI High—Second Cycle

The connections for the second cycle of RI (read-in to the HSM 15, 16) are the same as the previously described cycle for high status level RI (section 5.1.2 supra). The only exception is that the carry is added into the duplicated adder 17A from the carry flip-flop F2 (FIG. 1(f-b)) provided a carry is present from the previously added digits, along with the second, third, etc. least significant digits of the addend and augend, as they are entered. Again, at the occurrence of the eighth delayed timing pulse T8a, the status transition gate 1263 (FIG. 1G) sends its output to the set RO (read-out) lead (FIG. 1(a-e)). Accordingly, the status level control flip-flop F1290 is set, and all the other status level control flip-flops 47 are in the reset condition. Therefore, the status level RO is again high.

5.1.5 Status Level RO High, Second and Succeeding Cycles, and End of Both Operands

The third least significant characters of the addend and augend, are now read from the left HSM 15 and the right HSM 16 (FIGS. 1(c-c) and 1(d-c)) to the Y and Z registers 13 and 14 (FIGS. 1(c-d) and 1(d-d)) respectively in the same manner as described for the first status level RO high cycle with the operation level A high (section 5.1.3). It is apparent now that the succession of high status levels RO-RI continues, for as many digits as remain in the longest operand. The manner of handling

the carry, if any remains when the end of both operands is reached, will be clear from what follows.

Assume, however, by way of example, that the third least significant characters of the addend and augend are each as ISS (item separation symbol) signifying the end of an item. Accordingly, the end of both operands has been reached.

With the status level RO now high, the machine performs as it did in the preceding cycle during which status level RO high, (section 4.7.1.3 supra) until after the sixth timing pulse T6 occurs. Note, however, that the ISS's are read into the Y and Z registers 13 and 14 (FIGS. 1(c-d) and 1(d-d)) respectively through gates 911 and gates 1032 on the occurrence of the sixth timing pulse T6, with status level RO high.

A two-input gate 941 (FIG. 1(b-e)) has as one input the level NOT-N. The level NOT-N is secured by the output of an inverter which inverts the operation level N. Accordingly, the operation level NOT-N is high, because the operation level N is low. The gate 941 receives as its second input the eighth timing pulse T8. The output of the gate 941 is applied through an "or" circuit (FIG. 1(b-d)) to various gates in the left symbol recognition circuits 22, including a two-input gate 937 (FIG. 1(c-e)). The gate 937 receives as its second input the level from a lead designated ISSL, which is the output of an inverter I11 (FIG. 1(c-d)). This inverter I11 receives its input from a group of "or" circuits R922 (FIG. 1(b-d)). If, and only if, the Y register 13 has stored in it some symbol other than an item separation symbol (ISS), is the output of the "or" circuits R922 (FIG. 1(b-d)) high. The manner of connecting the "or" circuits R922 for securing the desired output will be apparent to those skilled in the art from the previous discussion of the "or" circuits R923 (section 5.1.1 supra). The output of the ISSL inverter I11 (FIG. 1(c-d)) is therefore low, because the Y register 13 has registered in it an item separation symbol, ISS. The output ISSL of the ISSL inverter I11 is applied to prime the gate 937 (FIG. 1(c-e)). The output of the gate 937 is applied to the set terminal S of the ISSL (item separation symbol, left) flip-flop F910.

Accordingly, the eighth timing pulse T8 is passed through the gate 941 (FIG. 1(b-e)) and then through the gate 937 to the set terminal S of the ISSL (item separation symbol left) flip-flop F910 (FIG. 1(c-e)). Note that prior to the occurrence of this eighth timing pulse T8 which sets the ISSL flip-flop F910, that this flip-flop was in its reset condition.

Among the right symbol recognition circuits 23, is a group of "or" circuits R1054 (FIG. 1(d-d)) the output of which is designated NOT ISSR (Not item separation symbol right). The input of the "or" circuits R1054 are connected to receive the outputs of the Z register 14. The output of the "or" circuits R1054 is high if and only if there is other than an item separation symbol stored in the Z register 14. The manner of connection of these "or" circuits will be apparent to those skilled in the art from the description of "or" circuits R923 (FIG. 1(b-d), section 5.1.1-T8). The output of the "or" circuits R1054 (NOT ISSR) is inverted by an inverter I12 (FIG. 1(d-e)). The inverter I12 has an output, therefore, that is high if and only if an item separation symbol is stored in the Z register 14. The output (designated ISSR) of the inverter I12 is applied to a three-input gate 1068 (FIG. 1(e-d)). The gate 1068 receives as a second input any one of the high operation levels B, L, A, R, S, or M applied through suitable "or" circuits. The gate 1068 is further primed by either one of the high status levels RO or RS applied to an "or" circuit, as shown. The eighth timing pulse T8 is the third input applied to the gate 1068. The output of the gate 1068 is applied through an "or" circuit to the set terminal S of the "end of operand right" flip-flop F1010.

57

Accordingly, the end of operand right flip-flop F1010 (FIG. 1(c-e)) is set.

The "one" output terminal, now high, of the end of operand right flip-flop F1010 (FIG. 1(d-e)) is applied as one input to a four-input gate 948 (FIG. 1(e-d)). A second input to the gate 948 is from a three-input "or" circuit 67 which receives as inputs the outputs from the three "one" terminals of the minus L flip-flop F909 (FIG. 1(b-e)), of the ISSL flip-flop F910 (FIG. 1(c-e)) and of the space left flip-flop F911 (FIG. 1(c-e)). The gate 948 also receives as a third input the operation level RI, now low. The first timing pulse T1 is also applied to the gate 948. The gate 948, therefore, does not pass any voltage until a later time.

The output of the gate 1068, passing the eighth timing pulse T8, not only sets the end of operand right flip-flop F1010 (FIG. 1(d-e)), but also a passed through "or" circuits and through the delay circuit D56 (FIG. 1(d-d)) to reset all stages of the Z register 14. The delay is employed because the Z register 14 is supplying the information necessary to reset itself. In order to derive a definite reset pulse that does not occur too soon, a brief delay is interposed.

Therefore the Z register 14 is cleared.

The status transition gate 1249 (FIG. 1G) passes the eighth delayed timing pulse T8a to the "set RI" lead. Application of the eighth delayed timing pulse T8a to the set RI lead, causes the selection of the status level RI to be high.

5.1.6 End of Both Operands, Status Level RI High

The gate 948 (FIG. 1(e-d)), previously described, now passed the first timing pulse T1. The output of the gate 948 is applied to the set terminal S of the EOBO flip-flop F1110 (FIG. 1(f-c)), which is therefore in set condition.

Note the provision of a two-input gate 1123 (FIG. 1(e-c)) the output of which is applied to the reset terminal of the EOBO flip-flop F1110. One input to the gate 1123 is from an "or" circuit passing any of the high status levels IC, RM, or RO02. The eighth timing pulse T8 is also applied to the gate 1123. Therefore, in the staticizing the addition instruction, the gate 1123 passed the eighth timing pulse T8 to the reset terminal R of the EOBO flip-flop F1110 (FIG. 1(f-c)). The EOBO flip-flop F1110 was therefore in reset condition before the application of the first timing pulse to set the EOBO flip-flop F1110 from the gate 948 (FIG. 1(e-d)).

Since the ISSL flip-flop F910 (FIG. 1(c-e)) is set, the input to the gates G27 (FIG. 1(e-a)) from the inverter I7 (FIG. 1(c-e)) last mentioned is low, and these gates G27 (FIG. 1(e-a)) are blocked (that is, closed).

Accordingly, the contents of the Y register 13 (FIG. 1(c-d)) cannot pass these last mentioned gates G27 into the adder 17A. The Z register 14 (FIG. 1(d-d)) has been cleared in the last RO cycle by the eighth timing pulse T8 passing through the delay circuit D56, as previously described. According, all low level "zero" "bits" (the equivalent of a zero) are read into the adder 17A (FIG. 1(e-b)) from the Z register 14 (FIG. 1(d-d)). If there is a carry from the previous addition recorded in the carry flip-flop F2 (FIG. 1(f-b)), the carry passes into the adder 17A (FIG. 1(e-b)), through a gate G12 (FIG. 1(e-a)) supplied for the purpose. The gate G12 is primed from the output of the adder input flip-flop F3, and the carry therefore passes into the duplicated adder 17A (FIG. 1(e-b)) between the first timing pulse T1 and the three and half pulse T3½, as a "one." The pulse is applied to the adder as a binary "one," which corresponds to a decimal one. The output of the adder 17A is then passed into the HSM 15, 16 through the L register 18 or the R register 19, as described in the last preceding high status level RI.

Note that the carry flip-flop F2 (FIG. 1(f-b)) is reset

58

at the fourth timing pulse T4 through the gate G6 primed by the high status level RI. The carry flip-flop F2 is then not set again, because the addend and augend are effectively zero, and the carry flip-flop F2 remains in its reset condition.

The "one" output from the EOBO flip-flop F1110 is applied to a status transition gate 1208 (FIG. 1H). A second input to the status transition gate 1208 is from the "zero" output of the carry flip-flop F2 (FIG. 1(f-b)). The high operation levels A, or S are applied through a suitable "or" circuit to a third input of the status transition gate 1208.

The eighth delayed timing pulse T8a is applied to the last input of the status transition gate 1208. The output from the status transition gate 1208 is applied to the "set IC" (instruction complete) lead.

Accordingly, the status level IC now becomes high.

5.1.7 End of Both Operands and No Carry, Special Cases

It may happen that the two most significant digits of the addend and augend are added without any carry as a result of this addition. Then, then next RO-RI sequence should produce a zero for an answer. This zero should be obtained when ISS's (item separation symbol) or spaces are read out of both the left and right HSM 15 or 16. If this zero were put in the address for this sum digit following the most significant digit of the sum, the answer could look like: . - - 0543. The period in the middle of the line, "." signifies the item separation symbol. The dashes "-" signify spaces. If this sum were to be used as an operand in another addition, an extra RO-RI sequence would be required before the space symbol is reached. In other words, the zero shown before the "5" in the example above might be the occasion for an unnecessary sequence occurring. Although the answer would be correct, an extra and unnecessary addition or cycle would have occurred. To circumvent this extra cycle occurrence, upon the end of both operands being reached, if a zero is detected in the most significant digit of the sum, the zero character is changed into a space before being stored in the HSM 15, 16, in a manner now to be described.

Assume, by way of example, that the end of the addend operand is read into the Y register 13 during the high status level RO, and that the end of the augend operand is read into the Z register 14. If there were no carry from the addition of the previous two digits of the addend and augend operands, in the beginning of the next RI cycle the adder inputs to the adder 17A are both zero. The output of the adder and binary-to-coded decimal converter (BCDC) 17B is applied to a four-stage adder output flip-flop register 62 (FIG. 1(f-c)). A two-input gate 1115 (FIG. 1(f-c)) primed by the high status level RI, passes the first timing pulse T1.

Thus, the gate 1115 output resets the adder output register at the beginning of each cycle during which the status level RI high. Note also that the output of the adder and BCDC 17 is applied through gates 717 to the L register 18, as described hereinbefore. The BCDC 17B output is available at the end of T2¾.

The adder output register 62 (FIG. 1(f-c)) is in this case thus set in accordance with the code for "zero." The output of the adder output register 62 is applied as a first input to a three-input gate 1119 through a suitable group of "zero" circuits 61 which may be similar to the recognition circuits hereinbefore described, or may consist of a group of "and" gates, connected in a manner known to the art. The output of the circuits 61 is high only if their input is a coded "zero." The input to the gate 1119 is thus assumed to be high if, and only if, a zero character occurs at the output of the BCDC 17B (FIG. 1(e-b)). The gate 1119 (FIG. 1(f-c)) receives as its second input the high operation level RI. The fourth timing pulse T4 is the third input to the gate G1119.

Accordingly, if and only if the output from the BCDC 17B (FIG. 1(e-b)) is coded a "zero" does the gate 1119 (FIG. 1(f-c)) pass the fourth timing pulse T4.

The fourth timing pulse T4 thus passed by the gate 1119 is applied as one input to each of a pair of three-input gates 1131. Each of the gates 1131 has applied to it as a second input any of the high operation levels A, S, or N. The gates 1131 are also connected to receive as the third input the output from the "one" terminal of the EOBO flip-flop F1110.

Accordingly, the fourth timing pulse T4 from the gate 1119 is passed through the two gates 1131 to be applied to set the 2⁰ bit flip-flop (lowest order stage) and to reset the 2⁴ bit flip-flop (fifth order stage) in the L register 18 (FIG. 1(b-c)). The decimal zero in the code adopted for this machine is 1010000. The application to the L register 18 from the two gates 1131 (FIG. 1(f-c)) in the manner described in effect changes this zero code from the output of the BCDC 17B (FIG. 1(e-b)) to the code for a space 1000001 as entered in the L register 18 (FIG. 1(b-c)). Accordingly, at the fifth timing pulse T5, when the gates 722 (FIG. 1(c-c)) are opened, as hereinafter described, the space character is read into the left HSM 15 (FIG. 1(c-c)). Parity is not affected.

The output of the gates 1131 (FIG. 1(f-d)) is applied in a similar manner to set the 2⁰ bit flip-flop and to reset the 2⁴ bit flip-flop in the R register 19 (FIG. 1(d-c)). If the 2⁹ bit flip-flop "zero" output of the C register 28 is high, the gates 722 (FIG. 1(c-c)) are opened and the contents of the L register 18, representing the space character, is entered into the left HSM 15. On the other hand if the 2⁹ bit flip-flop "one" output of the C register 28 is high, then the gates 851 (FIG. 1(d-c)) are opened to pass the contents of the R register 19 into the right HSM 16.

Accordingly, the space character is read into one or the other memory bank, left or right HSM 15 or 16 in accordance with the programming.

A four-input gate 1065 (FIG. 1(e-d)) receives as one input the space right lead SPR, as a second input the status level RO, and as a third input any one of the high operation levels M, A, R, or S. The eighth delayed timing pulse T8a is applied as the fourth input to the gate 1065. The output of the gate 1065 is applied, through "or" circuits, to the set terminal S of the end of operand right flip-flop F1010 (FIG. 1(d-e)), and through "or" circuits and the delay circuit D56 (FIG. 1(d-d)) to the reset terminal R of the Z register 14.

Accordingly, if a space is read out in the second or subsequent high status level RO from only one of either the left or right HSM 15 or 16 respectively into the Y register 13 (FIG. 1(c-d)) or the Z register 14 (FIG. 1(e-d)), the space left flip-flop F911 (FIG. 1(c-e)) or the end of operand right flip-flop F1010 (FIG. 1(d-d)), respectively, is set by the eighth timing pulse T8 passed through gate 938 (FIG. 1(c-d)) or gate 1065 (FIG. 1(e-d)). In the one instance, when the space is from the left HSM 15, the output of inverter 17 (FIG. 1(c-e)) is low, and gates 27 (FIG. 1(e-a)) are inhibited in the subsequent RI cycle. Thus the space symbol stored in the Y register 13 (FIG. 1(c-d)) is not added, or in effect, a zero is added. In the other case, the Z register 14 (FIG. 1(d-d)) is reset by the eighth timing pulse (T8) from the gate 1065 (FIG. 1(e-d)) through delay circuits D56 (FIG. 1(d-d)) before the succeeding high status level RI. Therefore, in effect, a zero is added from the Z register 14. In either case, note that one of the inputs to the gate 948 (FIG. 1(e-d)) is high.

If, however, both cases occur in the same RO cycle, then gate 948 is primed to pass the first timing pulse T1 when the status level RI is next high to set the EOBO flip-flop F1110 (FIG. 1(f-c)).

Therefore, the status level RI high is followed by other appropriate status levels than RO high (see the status level flow diagram for addition FIG. 13).

5.1.8 Review of Decimal Addition, Positive Numbers—Sequence of Status Levels

With reference to the flow diagram, FIG. 13, and to the simplified schematic of FIG. 3 (or the more complete FIG. 1), after the instruction is staticized in the manner heretofore explained, with successively high status levels RO01, RO02, and RO03 a search is commenced for the least significant digits of the addend and the augend in one or more (repeated as necessary) high status levels RS, which may be designated RS cycles. Note that the items may be of non-standard maximum length, and the digits actually present in an item may be less than the maximum number of locations allowed for that item. For example, the number may be .374—. Only the address of the least significant character of the full length item need be known. In the example just given, the least significant character of the full length item is a space. Accordingly, it may be necessary to perform several RS cycles before the least significant digit of the item is found.

After suitable search cycles of RS, the least significant characters of both the addend and the augend have been read out of the left HSM 15 and the right HSM 16 and are placed in the Y and Z registers 13 and 14 respectively. During the time that the characters are stored in the Y and Z registers 13 and 14, the left and right symbol recognition circuits 22 and 23 respectively detect what these characters are, such as a digit, item separation symbol, etc.

If both characters are a space, the machine goes through another RS search cycle (see FIG. 13) to determine what the next characters of the addend and augend are. Such search continues until the least significant digit of an actual operand is found.

Now assume that a digit is recognized in the addend but not in the augend. This could occur if the addend and augend appear as follows: .32 (addend) and .57— (Augend).

The character 2, third from the right, in the addend is read from the left HSM 15 into the Y register 13. This character is recognized as being a digit (a not-space character). The A counter 10 is then advanced by one to the address of the second significant digit of the addend.

The space character, third from right, of the augend is read from the right HSM 16 into the Z register 14. This character of the augend is recognized as a space character by the right symbol recognition circuits 23. The B counter 11 is advanced by one.

Because one of the characters identified is still a space, the machine goes through another RS search cycle. Since a digit (not-space) character was recognized in the Y register 13 in the previous search RS cycle, the A counter 10 is not advanced and the Y register 13 is not reset but retains the character read into it. The least significant digit of the addend is held in the Y register 13, and the A counter 10 holds the address of the second least significant digit of the addend until the least significant digit of the augend is found.

The sequence continues in similar manner until the least significant digit of the augend is also detected. When the least significant digits of both the addend and augend have been detected, the condition of both operands "not space" simultaneously, is satisfied. The next status level selected is RI (For read-in).

The least significant digits of the addend and augend are now transferred out of the Y and Z registers 13 and 14 respectively to the duplicated adder and binary to binary-coded decimal converter 17. The sum is read into the HSM 15, 16 and the carry, if any, is held in storage in the carry flip-flop F2 (shown only in FIG. 1(f-b), not in FIG. 3) in the RI cycle.

If the end of both operands has not been reached, (follow "NOT EOBO" line in FIG. 13 after "RI" line) the

machine selects status level RO (for read-out) to be high and reads out of the HSM 15, 16 the next least significant characters of the operands. The status level RI then becomes high again. These next least significant characters are then added, the carry if any also added, and the sum is placed or stored at the address (now advanced one) specified by the C counter 12 during the RI cycle in the HSM 15, 16. The new carry, if any, is again held in storage in the carry flip-flop F2.

The sequence of high status levels FO-RI is now continued until the ends of both operands are reached. The last carry is added, and the status level IC (instruction complete) (follow "EOBO and no carry and not 8" line in FIG. 13) is then selected. The references to "8" or "not 8" in FIG. 13 have to do with the addition of negative numbers, explained hereinafter.

If the end of one operand is reached before the end of the other operand, the machine continues in an RO-RI sequence, but a zero is placed in the adder each RI cycle for the operand the end of which was detected. For example, suppose the addend to be 37546, and the augend to be 152. In the fourth cycle, during RI, a 7 is placed in the adder for the addend digit. However, a zero is placed in the adder for the augend digit. If there were a carry from the addition in the third RI cycle, this carry would be placed in the adder 17, etc. The operation continues in this fashion until the end of both operands causes the status level IC to be selected as high.

5.1.9 Decimal Addition—Negative Numbers

In the code employed for this machine, the minus sign is "0001001." This character for a minus sign precedes before the most significant digit all negative numbers. The code for a nine is "1011001." The four least significant bits of both the minus character and the nine character are the same (1001), and correspond, it may be noted, in these four bits to the decimal number 9 expressed in the radix 2. Because the adder 17 uses only the four least significant digits in the operations add A, subtract S, and multiply M, special steps must be taken to avoid possible confusion. As will appear more fully hereinafter, when the code for a minus sign is read from a tape into the machine, the code symbol is recognized as such by the recognition circuits. The recognition has the effect of causing the negative sign to be stored in the HSM 15, 16 in its coded representation, but succeeding digits of the number are complemented with respect to nine by being passed through the nines complementor 21 (FIG. 1(e-c)). Thus a number such as -234 may be written on the tape as $\bar{9}234$, where the $\bar{9}$ represents the coded symbol for minus. This number may be stored in the HSM 15, 16 as $\bar{9}765$ — — —, assuming seven characters for the maximum length of this item. In the following discussion, the minus sign may also be termed a modified nine and written as $\bar{9}$.

In the addition process, either the addend or augend, or both, may be negative. The complements of all digits zero to nine must be nine to zero respectively. The decimal nine, however, must be distinguished from the modified nine. The distinction is accomplished in the computer by reference to the 2⁴ and 2⁵ bits. For numerical numbers, these bits are one and zero respectively. For the modified nine, these bits are both zero. Consequently, by making use of the 2⁴ and the 2⁵ bits, the recognition gates readily select between nine and modified nine. These bits are also employed in decimal subtraction to recognize what is termed herein a minus space or space minus and a minus item separation symbol or ISS minus. The recognition is accomplished by appropriate circuits. However, since the four least significant digits of the nine or modified nine or space minus of ISS minus symbols in each instance are 1001, each is treated as an ordinary nine in the addition process within the adder 17A, but the handling of the sum depends upon its na-

ture. There are four basic situations or cases: (1) modified nine plus one carry (use end around carry); (2) modified nine plus ISS (item separation symbol equal nine); (3) modified nine plus modified nine and no carry equals an incomplete eight; and (4) modified nine plus modified nine and carry equals modified nine.

5.1.9.1—Case 1 (End Around Carry or EAC)

In the first case, modified nine plus one carry, by way of example:

Example I: Add -53+67; sum equals +14

Problem : -53
 +67
 +14

On Tape : $\bar{9}53$
 67

Stored in HSM: $\bar{9}46$ --
 67 ---

To perform the addition: $\bar{9}46$ plus Sum in To tape
 67 HSM
 013 eac -14 -14

"End-around-carry" is abbreviated as "eac."

Note that the "zero" sum is recognized by the zero circuits 61 (FIG. 1(f-c)) and that the space is entered only if the EOBO flip-flop F1110 is set so that its "one" terminal primes the gate 1131 (FIG. 1(f-d)).

Among the left recognition circuit 22 is a set of "or" circuits R924 (FIG. 1(c-d)) similar to such circuits heretofore described, the output of which is low if, and only if, a modified nine character (neglecting the parity bit) is detected in the Y register 13 (FIG. 1(d-c)). An inverter I13 receives the "NOT minus L" output of the "or" circuits R924 and has an output designated "minus L" which is therefore high if, and only if, a modified nine is entered in the register 13. A three-input gate 940 (FIG. 1(b-d)) has as one input the output of the "or" circuit (FIG. 1(b-d)) which receives the output of the gate 941 (FIG. 1(b-e)). A second input to the gate 940 is from any one of the high operation levels A, S, or N. The third input to the gate 940 is from the minus L lead. The output of the gate 940 is applied to the set terminal S of the minus L flip-flop F909. Recall that the output from the "one" terminal of the minus L flip-flop F909 is applied through the three-input "or" circuit 67 (shown in FIG. 1(c-e)) to one input of the gate 948 (FIG. 1(e-d)).

Among the right recognition circuits is a set of "or" circuits R1053 (FIG. 1(d-d)) (similar to the "or" circuits R924 or FIG. 1(c-d)) which are connected to receive the output of the Z register 14 (FIG. 1(d-d)), the output of which "or" circuits R1053 is designated NOT MR. The NOT MR output is applied to an inverter I14 the output of which, designated MR, is applied to a three-input gate 1064. The MR lead is high if, and only if, a minus (modified nine) character is detected in the Z register 14 (ignoring the parity bit). The second input to the gate 1064 (FIG. 1(a-c)) is from any high operation lead A, S, W, or H. The third input to the gate 1064 is the eighth timing pulse T8. The output of the gate 1064 is applied through "or" circuits to the set terminal S of the end of operand right flip-flop F1010.

Accordingly, whether the modified nine is entered in the Y register 13 (FIG. 1(c-d)) or the Z register 14 (FIG. 1(d-d)) during an RO cycle in which a space character is entered in the other of these two registers, the gate 948 is primed to pass the first timing pulse T1 in the succeeding RI cycle, to set the EOBO flip-flop F1110 (FIG. 1(f-c)).

With the EOBO flip-flop F1110 set, and with a zero in the most significant place, the zero is changed to a space, as described in section 4.7.1.7. To make the result accurate, however, an "end around carry" must now be performed.

Case 1a—Status Level RI High

At T1, the EOBO flip-flop is set.

When there is a carry, after a positive and negative number are added to give a positive result, as in the example above, the "one" output of the carry flip-flop (FIG. 1(f-b)) is high. The "one" output of the carry flip-flop F2 is connected to one input of a six-input status transition gate 1227 (FIG. 1H). A second input to the status transition gate 1227 is from the status level RI which is high. A third input to this status transition gate 1227 is from either one of the high operation levels A, or S applied through a suitable "or" circuit. A fourth input to the status transition gate 1227 is from the EOBO flip-flop F1110 (FIG. 1(f-c)). A fifth input to the six input status transition gate 1227 is derived by passing the first order flip-flop "one" terminal ($2^0(1)$) and the fourth order flip-flop "zero" terminal ($2^3(0)$) of the adder output register 62 (FIG. 1(f-c)) through an "or" circuit, (as indicated in FIG. 1H) and applying the output of this "or" circuit to the status transition gate 1227.

Accordingly, if the adder output register 62 (FIG. 1(f-c)) is storing a number the first significant digit of which, in binary form, is a one; or a number the third least significant digit of which, in binary form is a zero, (in decimal form, not a nine) then the status transition gate 1227 (FIG. 1H) is primed by its input from the adder output register 62. The eighth delayed timing pulse T8a is also applied to the status transition gate 1227.

Accordingly, the eighth delayed timing pulse T8a is passed by the status transition gate 1227 to the "set RD" lead (FIG. 1(a-e)). All of the status level flip-flops F1282 to F1293 are in the reset condition except the status level flip-flop F1284 which is in the set condition, and the status level RD is high.

Case 1b—Status Level RD High

A three-input gate 554 (FIG. 1(d-b)) receives at one input either one of the high levels A, or S. Also applied to the gate 554 is the high status level RD. The first timing pulse T1 is the third input to the gate 554. The gate 554 output is applied through "or" circuits to the reset terminals R of the A and B counters 10 and 11 (FIGS. 1(c-b) and 1(d-b)) respectively.

Accordingly, all stages of the A and B counters 10 and 11 are now in the reset condition.

A three input gate 327 (FIG. 1(c-b)) receives as one input the output of an "or" circuit receiving the operation levels A and S, as a second input the status level RD, and as the third input the first timing pulse T1. The output of the gate 327 is applied to the reset terminals R of the C counter 12 (FIG. 1(c-b)). Accordingly, the C counter 12 is now reset.

A three-input gate 1136 (FIG. 1(f-e)) receives as one input the RD level. Also applied as a second input to the gate 1136 are either one of the high operation levels A, S. The first timing pulse T1 is applied as the third input to the gate 1136. The output of the gate 1136 is applied through "or" circuits to the reset terminals of the three previous results flip-flops 49 (FIG. 1(f-d)), namely the "previous result zero" flip-flop F1101, the "previous result all nines" flip-flop F1103, and the "previous result negative" flip-flop F1109. The output of the gate 1136 is also passed to the set terminals of a one cycle flip-flop F1102 (FIG. 1(f-e)). The output of the gate 1136 is also applied through an "or" circuit to the reset terminal of the EOBO flip-flop F1110 of (FIG. 1(f-d)). (Follow lower line, FIG. 1(f-e) through FIGS. 1(e-e), 1(e-d), 1(e-c), and finally to FIG. 1(f-d)). The output of the gate 1136 output is also applied through various "or" circuits to the reset terminals of the ISSL flip-flop F910 (FIG. 1(c-e)) and of the space-left flip-flop F911 (FIG. 1(c-e)) and to the reset terminals of the space-right flip-flop F1008 (FIG. 1(d-e)) and of operand right flip-flop F1010. (Follow

lower line FIG. 1(f-e) to FIG. 1(e-e), FIG. 1(d-e), FIG. 1(c-e) and thence through branches and "or" circuits.) Also, the output of the gate 1136 (FIG. 1(f-e)) is applied to a two-input gate 946 (FIG. 1(c-e)). The gate 946 is primed by the output from the "one" terminal of the 2^9 bit of the C register 28 (FIG. 1(c-a)). The output of the gate 946 (FIG. 1(c-e)) is passed through a delay circuit D11 to the set terminal S of the ISSL flip-flop F910.

Accordingly, on the occurrence of the first timing pulse T1, the previous results flip-flops 49 (FIG. 1(f-d)) are all reset. The EOBO flip-flop F1110 (FIG. 1(f-c)) is reset. The ISSL flip-flop F910 (FIG. 1(c-e)) the space-left flip-flop F911 (FIG. 1(c-e)), the space-right flip-flop F1008 (FIG. 1(d-e)) and the end of operand right flip-flop F1010 (FIG. 1(d-e)) are also reset. If, and only if, the 2^9 bit flip-flop of the C register 28 (FIG. 1(c-a)) is in the set condition, the ISSL flip-flop F910 (FIG. 1(c-e)) receives a set pulse from the delay circuit D11 shortly after the first timing pulse T1.

A four-input gate 947 (FIG. 1(c-e)) is provided which is primed by the output from the "zero" terminal of the 2^9 bit flip-flop (indicated $2^9(0)$) of the C register 28 (FIG. 1(c-a)). The gate 947 (FIG. 1(c-e)) also receives as a second input the status level RD. The gate 947 receives as a third input either one of the high operation levels A, or S, applied through a suitable "or" circuit. The fourth input to gate 947 is the fourth timing pulse T4. The gate 947 output is applied to the set terminal S of the end of operand right flip-flop F1010 (FIG. 1(d-e)) and also through suitable "or" circuits to the reset terminals of the Z register 14.

Accordingly, it may be noted that after the fourth timing pulse T4, with the RD level high, either the ISSL flip-flop F910 (FIG. 1(c-e)) is in the set condition, or the Z register 14 is in the reset condition and the end of operand right flip-flop F1010 (FIG. 1(d-e)) is set, depending upon whether the address stored in the C register 28 (FIG. 1(c-a)) has the 2^9 bit in the set or reset condition respectively.

A three-input gate 306 (FIG. 1(c-a)) is provided having one input from status level RD and a second from either one of the high operation levels A or S. The fourth timing pulse T4 is the third input to the gate 306. The output of the gate 306 is applied through an "or" circuit to a set of nine, two-input gates 308. The second inputs to the gates 308 are from the respective "one" outputs of the C register 28 and the outputs of the gates 308 are applied to the respective set terminals of the C counter 12 (FIG. 1(c-b)).

Accordingly, the contents of the nine lower order stages of the C register 29 are transferred to the C counter 12 (FIG. 1(c-b)) from where they will again be employed to address the least significant digit of the partial sum.

A three-input gate 503 (FIG. 1(c-b)) has applied to it either one of the high operation levels A or S. The second input to the gate 503 is the status level RD. The third input to the gate 503 is the sixth timing pulse T6.

The gate 503 output is applied, through an "or" circuit, to two sets of nine, two-input gates each, a first set 524 (FIG. 1(c-b)) and a second set 534 (FIG. 1(d-b)). These two sets of gates 524 and 534 are connected to pass the output of the nine lowest order stages of the C register 28 (FIG. 1(c-a)) to the A and B counters 10 and 11 (FIGS. 1(c-b) and 1(d-b) respectively).

Accordingly, the A and B counters 10 and 11 each holds the address of the least significant digit of the sum, which presently is the partial sum of the HSM 15, 16 without the end-around-carry.

A three-input status transition gate 1269 (FIG. 1G) receives as one input the status level RD and as a second any one of the high operation levels A, S, or R. The eighth delayed timing pulse T8a is applied as the third input to the status transition gate 1269. The output of

65

the status transition gate 1269 is applied to the set RO lead.

The status level RO now becomes high.

Accordingly, the RO-RI sequence is now repeated for all the digits of the sum to take care of any propagated carry. The end-around carry is added into the least significant digit of the partial sum from the carry flip-flop F2 (FIG. 1(f-b)) in the first high status level RI cycle. Any propagated carry is thus added as the process proceeds. The A or B counter 10 or 11 (FIG. 1(c-b) or 1(d-b)) addresses the left HSM 15 or the right HSM 16 (FIG. 1(c-c) or 1(d-c)) at the location of the least significant digit of the partial sum. The new digit of the final sum is stored starting at the same sum address first entered in the C counter 12 (FIG. 1(c-b)) from the C register 28 (FIG. 1(c-a)). The RO-RI sequence is repeated once for each digit of the sum until the final sum has been computed and stored.

Note that if the 2⁹ bit flip-flop of the C register 28 is in the reset condition, with the "zero" output high, the left read-out gate 730 (FIG. 1(c-c)) is opened at the appropriate time, and the characters are read out through the Y register 13 (FIG. 1(c-d)). Meanwhile, the "bits" from the Z register 14 (FIG. 1(d-d)) are zero, because the Z register 14 now has all stages reset by the output of the gate 947 (FIG. 1(c-e)) due to the control exerted over it by the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)), as pointed out above.

On the other hand, if the 2⁹ bit flip-flop of the C register 28 is in the set condition, the ISSL flip-flop F910 (FIG. 1(c-e)), as noted above, is in the set condition, due to a pulse from the gate 946. The high "one" output of the ISSL flip-flop F910 is then inverted in inverter 17 to inhibit the gates G27 (FIG. 1(e-a)) to prevent any output from the Y register 13 (FIG. 1(e-a)) from being read into the adder 17A (FIG. 1(e-b)).

Accordingly, when the RO-RI sequence is repeated once for each digit of the sum, as pointed out above, and the partial sum is read out of the left HSM 15 or the right HSM 16, then respectively the Y register 13 or the Z register 14 are employed, and the sum is computed as though the other register always carried a zero, that is, as though a zero was read out of the other right or left HSM 15 or 16.

The effect is as though the end-around carry has been added to the least significant digit and the sum has been stored again in the same address of the left or right HSM 15 or 16 as that from which the partial sum was read out.

Upon reaching the end of this addition, the status level IC (for instruction complete) is selected by the status transition gate 1208 (FIG. 1H). (See end of section 4.7.1.6).

Case 2—Modified Nine and ISS and A Sum Nine

Example 2: Add -54+47; sum is -7

Problem: $\begin{array}{r} -54 \\ +47 \\ \hline -7 \end{array}$

On tape: 554
-47

Stored in IISM: 545
-47

To perform the addition: $\begin{array}{r} 545 \text{ Sum In} \\ -47 \text{ IISM} \\ \hline 592 \quad 592 \quad -507 \end{array}$

When the most significant digit of a sum is nine, and the ends of both operands is indicated, and there is no carry, the sum is negative and equal to the complement of the number to the right of the "minus 9." The numeral nine is changed by the machine to the symbols for minus 9 (modified nine).

A three-input gate 1133 (FIG. 1(f-d)) receives at one input either of the high status levels A, or S. A second input to the gate 1133 is from the "one" output terminal of the EOBO flip-flop F1110 (FIG. 1(f-c)). A third

66

input to the gate 1133 (FIG. 1(f-d)) is from the output of a three-input gate 1126. One input to the gate 1126 is from the high status level RI. A second input to the gate 1126 is from the fourth timing pulse T4. The third input to the gate 1126 is from a "nine" recognition circuit 63. The "nine" recognition circuit 63 is similar to the "or" circuits such as found in the left and right symbol recognition circuits 22 and 23 already described or may be similar to the "zero" circuit 61 of FIG. 1(f-c). The "nine" recognition circuit 63 (FIG. 1(f-e)) output is high if, and only if, the input to the "nine" recognition circuit 63 from the adder output register 62 (FIG. 1(f-c)) is a binary coded nine. The output of the gate 1133 (FIG. 1(f-d)) is applied to the reset terminals of the 2⁴ and 2⁶ (fifth and seventh) stages only of the L and R registers 18 and 19 (FIGS. 1(b-c) and 1(d-c, respectively).

In operation, where an addition such as that in Example 2 above it is to be performed, the machine enters the status level RS (that is the status level RS becomes high). The machine then cycles in the RS status level until the least significant digit of both operands is read out of the HSM 15, 16 (see the flow diagram of FIG. 13). Thereupon, the digits are added, in succeeding cycles of RI and RO. Finally, in the status level RO, a modified nine is read into one of the Y and Z registers 13 and 14 from the HSM 15, 16 and a space symbol or an ISS is read into the other one of the Y or Z registers 13 or 14.

If the modified nine is read into the Y register 13 (FIG. 1(c-d)) then the NOT Minus L lead from "or" circuits R924 is low and the minus L lead is high. The gate 940 (FIG. 1(b-e)) is primed to pass the eighth timing pulse T8 from the gate 941 to set the minus L flip-flop F909. The gate 948 (FIG. 1(e-d)) is therefore primed from the "or" circuit 67 because the "one" terminal of the minus L flip-flop F909 is high.

If it is assumed that the other operand character at this point stored in the Z register 14 (FIG. 1(d-d)), is an item separation symbol the NOT ISSR lead from the "or" circuits R1054 is at a low level. Accordingly, the ISSR lead is at a high level. The gate 1068 (FIG. 1(e-d)) at the eighth timing pulse TP8 of the RO cycle passes a pulse to set the end of operand right flip-flop F1010 (FIG. 1(d-c)). Therefore, the gate 948 (FIG. 1(e-c)) has the other input primed to pass the first timing pulse T1 as soon as the status level RI is high.

On the other hand, if a minus symbol is read out of the right HSM 16 (instead of the left HSM 15) in the RO cycle, the minus symbol is stored in the Z register 14 (FIG. 1(d-d)). The NOT MR output of the set of "or" circuits R1053 in the right recognition circuits 23 is at a low level. The output of the inverter I14 (FIG. 1(d-e)) designated MR is high. The eighth timing pulse is therefore passed through the gate 1064 and through "or" circuits to the set terminal S of the end of operand right flip-flop F1010. Therefore the end of operand right flip-flop F1010 is set to prime the gate 948 (FIG. 1(e-d)) at the beginning of the following high status level RI. In this case, the Y register 13 has an ISS stored in it. Therefore the ISSL flip-flop F910 (FIG. 1(c-d)) is in the set condition. Therefore a second input to the gate 948 is primed. Accordingly, in this example, whether the minus symbol is read out of the left or right HSM 15, or 16, and an ISS from the other HSM 15 or 16 (during the high status level RO) the gate 948 is primed at the high status level RI immediately following to pass the first timing pulse T1.

As described hereinbefore, the EOBO flip-flop F1110 (FIG. 1(f-c)) is then set. The gate 1126 (FIG. 1(f-d)) is primed by the output of the "nine" circuit 63 because the four digits from the adder output register 62 (FIG. 1(f-c)) are a binary coded decimal nine. Note that the four least significant digits of the modified nine and

the numeric nine are the same, and that the four least significant digits of the space symbol are all zeroes.

Accordingly, the gate 1126 (FIG. 1(f-d)) when the status level RI is high, passes the fourth timing pulse T4 to the gate 1133, the output from which resets the 2⁴ and 2⁶ stages of both L and R registers 18 and 19 (FIGS. 1(b-c) and 1(d-c)) respectively. The effect is to alter the term stored in the last mentioned registers from a nine (coded as binary 1011001) to a modified nine or minus symbol (binary 0001001).

Case 3—Modified Nine and Modified Nine and No Carry

Example 3: Add -62+(-83)+-145

Problem: - 62
- 83
-145

On Tape: 062
083

Stored in HSM: 037
016

To perform the addition:	037 0016	plus eac	Sum in HSM	Tape
	9853	9854	5854	0145

When two negative numbers are added, the end of each operand is 0. When these are added without the presence of a carry, the result is a carry and eight. Another RI cycle is required, to add another 0 to 0 and the carry. Thus the 8 becomes 98- -.

Note that although EOBO flip-flop F1110 (FIG. 1(f-c)) is set, the status transition gate 1227 (FIG. 1H) is not primed when the adder output register stores on eight (in binary code: 1000), because the 2³ bit of this register is a "one," and the 2⁰ bit is a zero. Thus one of the inputs to the status transition gate (from an "or" circuit receiving the outputs 2³(0) and 2⁰(1) of the adder output register 62 (FIG. 1(f-c)) is low. The machine does not change status levels under these conditions, but cycles again in status level RI. Note that the Y and Z registers 13 and 14 (FIG. 1(c-d) and 1(d-d)) are not reset, when storing an end of operand symbol such as modified nine. Therefore, the "eight" sum (as in the example 3 above) is entered in the HSM 15 or 16, at the location the program requires, and at the same time the two modified nines in the Y and Z registers 13 and 14 are added, with the carry flip-flop F2 (FIG. 1(f-b)) set because of the carry. In this second RI cycle, however, the condition is like Case 2 for adding negative numbers (section 5.1.9.1), with an end-around carry. The status transition gate 1227 is open at the end of the RI cycle to pass the eighth delayed timing pulse T8a. The status level RD is then high to prepare for the end-around carry. Thus an RD-(RO-RI) series follows and the sum is correctly completed.

Case 4—Modified Nine Plus Modified Nine and Carry

Example 4: -62+(-21)+83

Problem: -62
-21
+83

One Tape: 062
021

Stored in HSM: 037
078

To perform the addition:	037 078	plus eac	Sum in HSM	Tape
	915	016	016	083

In this case the sum is negative and an end-around-carry is also required. The required addition is accomplished in an RD-(RO-RI) sequence. Note that the EOBO flip-flop F1110 (FIG. 1(f-c)) is set. Status transition gate 1227 (FIG. 1H) is primed to pass the eighth delayed timing pulse T8a to the "set RD" lead. The status level RD is high, and the end-around-carry is performed as before.

5.1.10 Operands of Different Lengths

In all the above examples the addend and augend were of equal length. There are three cases in which they are of different lengths.

- Short operand negative, other operand positive.
- Long operand negative, other positive.
- Both operands negative, one long, one short.

Case a.—The short negative operand is, in effect, filled out to the same length as other operand by "holding" the negative sign and adding it repeatedly until the end of the other operand is reached. Note that neither the Y register 13 nor the Z register 14 is reset if the recognition circuits indicate either one stores a modified nine. However, the minus L flip-flop F909 (FIG. 1(b-e)) or the end of operand right flip-flop F1010 (FIG. 1(d-e)) is in set condition due to the minus sign.

Example Case a: Add a minus 4 to a plus 1236 (-4+1236)

Problem: -4
1236

On Tape: 04
1236

Stored in HSM: 05
1236

To perform the addition:	0005 1236	Plus eac	Sum in HSM	Tape
			-1232	1232

The machine changes the zero to a space by opening gates 1131 (FIG. 1(f-d)), as before (section 5.1.9.2). Recall that a modified nine is treated in the adder as a numeric nine. When the end of both operands is reached, the EOBO flip-flop F1110 (FIG. 1(f-c)) is set. Due to the carry, the carry flip-flop F2 (FIG. 1(f-b)) is set. Thus status transition gate 1227 is open, and status level RD becomes high. Then (RO-RI) sequences as required follow up the RD level to complete the end-around carry and the addition.

Case b.—The short positive operand is added as though filled out with its end-of-operand symbol (treated numerically as zero). The usual cycles of RO and RI continue until the end of both operands, and EOBO flip-flop F1110 is set. Then status level IC is selected to be high.

Example Case b: Add +5+(-1236)

Problem: 5
-1236

On Tape: 5
01236

Stored in HSM: 5
08763

To perform the addition:	0005 08763	Sum in HSM	Tape
	08768	08768	01231

With the end of both operands and no carry, status transition gate 1208 (FIG. 1H) passes the eighth delayed timing pulse T8a to the "set IC" lead. Status level IC is selected to be high and the operation completed. Note that during this addition, if the Y register 13 holds either a space or an ISS, the space left flip-flop F911 (FIG. 1(c-e)) or ISSL flip-flop F910 is set, and thereafter remains set until the end of the operation. In this case, gates 27 (FIG. 1(e-a)) are not primed (note inverter 17 of FIG. 1(c-e)). Effectively a zero is added. However, because of the setting of the flip-flop F910 or F911 the gate 948 (FIG. 1(e-d)) is primed, to permit the EOBO flip-flop F1110 (FIG. 1(f-c)) to be set at the end of the other operand.

If the Z register 14 stores a space symbol or ISS, the end of operand right flip-flop F1010 (FIG. 1(d-e)) is set, and the Z register 14 (see FIG. 1(d-d)) is reset via gate 1065 or gate 1068. The gate 948 (FIG. 1(e-d)) is primed from the "one" terminal of the end of operand flip-flop F1010. Note that the final modified nine is treated as a numeric in the adder 17a and reconverted to

a modified nine by the gate 1133 (FIG. 1(f-d)) as explained above.

Case c.—The short negative number is, in effect, filled out with 9's to the length of the long number as adding proceeds.

Example Case c: Add $-6+(-234)$

Problem: -6
 -234
 -240

On Tape: 96
 9234

Stored in HSM: 93
 9765

To perform the addition: $\begin{array}{r} 9993 \\ 9765 \\ \hline 9758 \end{array}$ plus
 9755 eac HSM Tape
 9758 9759 9759 9240

The addition proceeds without clearing that Y or Z register 13 or 14 which holds a modified nine (minus L flip-flop F909 or end of operand right flip-flop F1010 is in set condition), until the two modified nines are added and the end-around carry performed as explained above.

5.1.11 Review of Decimal Addition and Sequence of Status Levels

The flow diagram for the status levels for addition, FIG. 13, may now be reviewed again. After the instruction is staticized in the high status levels RO01, RO02, and RO03, the machine cycles in the high status level RS if either or both of the operands are a space symbol. When both operands are not a space symbol, the status level RI is selected to be high. With the status level RI high, the addition of the least significant characters is performed. If the end of both operands is not detected, the status level RO becomes high. The next least significant characters of the operands are read out of the HSM 15, 16 and the status level RI again becomes high.

If a space symbol or item separation symbol or minus symbol is detected in only one of the operands, then this symbol is retained for that one operand either by carrying it in the appropriate register or by effectively adding zeroes and resetting the register. Otherwise the machine operates as before.

At the end of an addition with the status level RI high, if the end of both operands has been detected and an eight results from the addition, the addition must be of a kind requiring a modified nine in the next more significant digit of the sum. Accordingly, the status level RI remains high and a further addition is performed with the status level RI high. If the end of both operands is reached after the high status level RI high, and the current sum is not an eight and there is a carry, and end around carry is indicated. The sum digit may be a zero which is changed to a space. The status level RD becomes high, followed by the status level RO. With the high status level RO, the least significant character of the partial sum is withdrawn from the HSM 15, 16, the end around carry added, and the addition proceeds in repeated RO RI cycles. Eventually, in all instances, the end of both operands is reached during an RI cycle, that is when the status level RI is high, and at the same time there is no carry and the sum is not an 8. The instruction is then complete and the status level IC becomes high.

5.1.12 Previous Results Circuits, Description

It is convenient at this point to describe certain circuits having to do with the recognition of the results of an arithmetical operation. These are described as associated with the operation A, but are effective with little change for certain other operations. The purpose of these circuits is to provide a way of proceeding to new instructions depending on the previous result by means of a conditional transfer of control, described in operation C (see sec. 5.16 infra).

The one cyclic flip-flop F1102 (FIG. 1(f-e)) mentioned above, has applied to its set terminal S, through

an "or" circuit, the output from a three-input gate 1107. The gate 1107 receives as one input the high RO03 status level. The gate 1107 receives as a second input any one of the high operation levels L, A, R, or S, through suitable "or" circuits. The first timing pulse T1 is also applied to the gate 1107. Accordingly, at the start of the execution of the instruction to add, with the status level A high, the one cycle flip-flop F1102 is in its set condition.

A three-input gate 1137 receives as one input the high status level RO03. The gate 1137 receives as a second input a level designated "not C," indicating that when the operation level C for conditional transfer is low, then the input "not C" is high. This input may be derived by applying the output from the operation level C from the operation matrix OM to an inverter, the output of this inverter (not shown) being the output designated as "not C." The sixth timing pulse T6 is the third input to the gate 1137. The output of the gate 1137 is applied through an "or" circuit to the reset terminals R of the previous results flip-flops 49 (FIG. 1(f-d)) mentioned hereinbefore, namely the previous result zero flip-flop F1101, the previous result all nines flip-flop F1103, and the previous result negative flip-flop F1109. Accordingly each of these previous result flip-flops 49 is each in the reset condition.

As described hereinbefore, the status transition gate 1234 (FIG. 1H), when the operation level A high, and the status level RO03 is high, at the eighth delayed timing pulse T8a, selects the operation level RS and the search for the least significant digits of the operands ensues. Also, as described before, the least significant digits of the operands are added, and the result digit from the BCDC 17B is stored in the adder output register 62 (FIG. 1(f-e)).

If the least significant digit of the result is zero, then the output of the "zero" circuits 61 (FIG. 1(f-c)), applied to the gate 1119 is high, and the gate 1119 is primed. During the succeeding high status level RI, the fourth timing pulse T4 applied to the gate 1119 is passed therethrough. The output of the gate 1119 is applied to the gates 1131 (FIG. 1(f-d)), as described heretofore, and also as one input to a two-input gate 1105. The gate 1105 receives as its other input the "one" output of the one cycle flip-flop F1102 (FIG. 1(f-e)). Accordingly, when the status level RI is high, the gate 1105 passes the fourth timing pulse T4 from the output of the gate 1119, and this pulse is applied through an "or" circuit to the set terminal S of the previous result zero flip-flop F1101.

Accordingly, the previous result zero flip-flop F1101 is in the set condition.

A four-input gate 1111 has applied to it as one input a lead indicated "NOT zero" from an inverter 115 (FIG. 1(f-c)) which receives the output of the "zero" circuits 61. This "NOT zero" lead is high if, and only if, the output register 62 contains or stores other than a zero. The gate 1111 receives as a second input either one of the high operation levels A, or S. The gate 1111 receives as a third input the high status level RI. The fourth timing pulse T4 is applied as the fourth input to the gate 1111. The output of the gate 1111 is applied to the reset terminal R of the previous result zero flip-flop F1101. Therefore the previous result zero flip-flop F1101 is reset at the fourth timing pulse T4 if a zero is not entered in the adder output register 62. Thus only if all the sum digits successively are zero does the previous result zero flip-flop F1101 remain in set condition. Note that the previous result zero flip-flop F1101 is reset by the fourth timing pulse T4 in this fashion in the RI cycle in which or during which the result digit which is not zero is computed.

A two-input gate 1108 (FIG. 1(f-e)) has its output applied to the reset terminal of the one cycle flip-flop F1102. One input to the gate 1108 is the high status level RI. The sixth timing pulse T6 is applied as the second input to the gate 1108. Accordingly, when the

status level RI high, at the sixth timing pulse T6, the one cycle flip-flop F1102 is reset.

If the least significant digit of the result is a nine, a somewhat different kind of arrangement is employed. The gate 1126 (FIG. 1(f-d)), in the event that the digit character from the adder output register 62 is a nine, passes the fourth timing pulse T4 to a three-input gate 1117, and also to a gate 1133. The gate 1133 has been described. The gate 1117 (FIG. 1(f-d)) also receives as a second input either one of the high operation levels A, or S, and as its third input the "one" output of the one cycle flip-flop F1102 (FIG. 1(f-e)). The output of the gate 1117 is applied to the set terminal S of the previous result all nines flip-flop F1103.

Accordingly, if the status level RI is high, and the adder output register 62 stores a nine, the gate 1117 (FIG. 1(f-d)) passes the fourth timing pulse T4 to set the previous result all nines flip-flop F1103.

The one cycle flip-flop F1102 (FIG. 1(f-e)) is reset, as described hereinbefore, (by the sixth timing pulse T6 passed through the gate 1108 (FIG. 1(f-e)) during the high status level RI thereby closing the gate 1117.

A four-input gate 1116 (FIG. 1(f-d)) receives as one input either one of the high operation levels A, or S. The "nine" circuits 63 output inverted by inverter I16 is applied as a second input to the gate 1116. The third input to the gate 1116 is from either of the high operation levels A or S. The gate 1116 also receives as a fourth input the high status level RI.

Accordingly, if all the digits are nine or modified nine (which to the adder appears as a nine), the previous result all nine flip-flop F1103 is set. If any of the sum digits succeeding the first are not nine, the gate 1116 passes the fourth timing pulse T4 applied thereto, to reset the previous result all nines flip-flop F1103. In this event, the previous result all nines flip-flop F1103 is reset in the high status level RI during which the digit from the adder output register 62 is not a nine.

If an end of operand character indicating a modified nine is added, notice that so far as the adder and BCDC 17 is concerned, the four least significant digits thereof correspond to a nine. If, therefore, two end of operand characters are added and the result is a nine (due to a carry) the gate 1126 (FIG. 1(f-d)) is primed as before to pass the fourth timing pulse T4. The output of the gate 1126 is applied to the gate 1133 (FIG. 1(f-d)). However gate 1133 is primed by the "one" output from the EOBO flip-flop F1110 (FIG. 1(f-c)), and therefore the last mentioned gate 1133 is open only when the end of both operands are reached. Note also that the gate 1133 is primed only for either one of the high operation levels A, or S. Accordingly, if the end of operand characters are added and the result is a nine, then the output from the gate 1133 is applied to the set terminals of the previous result negative flip-flop F1109 to set this flip-flop, thereby indicating a negative result.

The output of the gate 1133 (FIG. 1(f-d)) at the same time is applied to the appropriate stages of the L and R registers 18 and 19 (FIGS. 1(b-c) and 1(d-c)) respectively to change the nine applied to these registers 18 and 19 to a modified nine (minus symbol).

Note that if there is an end around carry, it is implemented as in sec. 5.1.9 supra. In the RD cycle then occurring, the gate 1136 (FIG. 1(f-e)) passes the first timing pulse T1 to set the one cycle flip-flop F1102, reset the previous result flip-flops 49 and to reset the EOBO flip-flop F1110. Thereafter the same previous results circuits 49 are employed to distinguish between the previous result negative, the previous result all nines, and the previous result zero, as the "one" is added to the least significant digit of the partial sum, and each digit is added to secure any propagated carry.

5.1.13 Previous Results Circuits, Operation

After an addition or subtraction operation is sometimes desired to go to a conditional transfer of control operation (high operation level C). The next instruction is to be selected on the basis of whether the sum or difference just computed is positive, negative, or zero. Reading the sum or difference from the HSM 15, 16 to determine whether it is positive, negative, or zero is costly in time. Instead, the condition of the result is determined during computation.

There are four conditions considered:

- (1) Previous result positive.
- (2) Previous result zero (positive).
- (3) Previous result zero (negative).
- (4) Previous result negative.

The two conditions of zero are due to the use of the nines complements. A number which is zero positive, or the ordinary zero, is coded by a group of zeroes in the four least significant digits of a character. On the other hand, it is possible to obtain a number which is zero, but which is designated by a series of nines (coded) preceded by the modified nine sign. The complement of this last number is zero.

The previous result zero flip-flop F1101 (FIG. 1(f-d)) as pointed out above, is set only if a zero is detected in the first or least significant digit of the sum and if the remaining digits of the sum are also zero.

The previous result all nines flip-flop F1103 is set only if a nine is detected in the least significant digit of the sum and also if the remaining digits are all nines.

The previous results negative flip-flop F1109 is set only when the end of both operands is reached and a modified nine is detected in the sum.

The use of these previous results flip-flops 49 can best be understood by the use of sample problems:

Case I: Result is positive.

```
.342- - addend
.25- - augend
-- -367 sum
```

Since the least significant digit of the sum is seven, the previous result zero, and previous result all nines flip-flops F1101 and F1103 cannot be set. When the ends of both operands are reached, no modified minus appears as a sum digit, so that the previous result negative flip-flop F1109 is not set. This combination of states in the three flip-flops indicates that the sum is positive.

Case II: Result is zero positive.

```
.000 addend
.000- - augend
.-000- sum
```

The least significant digit of the sum is zero. The previous result zero flip-flop F1101 is set. Since the remaining sum digits are zero, this flip-flop remains set. The previous result all 9's flip-flop F1103 is not set because the least significant digit of the sum is not nine. The previous result negative flip-flop is F1109 is not set because when the end of both operands is detected, the sum digit is not a modified nine. The previous result zero flip-flop F1101 is in the set condition and indicates the sum is zero positive.

Case III: Result is zero negative.

```
  156 minuend } On Tape
- 56 subtrahend
-----
   56
  843
  ---
 899 Result
```

The previous result all 9's flip-flop F1103 is set because the least significant digit of the sum is nine; and this flip-flop F1103 remains set because the remaining digits of the sum are nine or modified nine. The previous result

zero flip-flop F1101 is not set because the least significant digit of the sum is not zero. The previous result negative flip-flop F1109 is set when the end of both operands is detected because the sum digit is modified nine.

The set condition of both previous result negative and previous result all 9's F1109 and F1103 indicates that the result is zero negative.

5.2 Decimal Subtraction (Operation S)—Operation Level S High

In performing subtraction, the minuend is always taken from the left HSM 15 (FIG. 1(c-c)) and the subtrahend from the right HSM 16 (FIG. 1(d-c)). The minuend is read into the Y register 13 (FIG. 1(c-d)) through the gates 911 (FIG. 1(c-d)) in the same manner as with the high operation level A.

5.2.1 Additional Circuits

Besides the circuits already described, a pair of four input gates 1001 and 1002 (FIG. 1(d-d)) are provided for priming gates at the output of the nines complementor 21, which receives the subtrahend from the right HSM 16, FIG. 1(d-c). The gate 1001 receives, as one input, the status level RO. The gate 1002 receives as one input the status level RS. Each of the gates 1001 and 1002 has applied to it as a second input a timing pulse between the sixth and seventh designated T6½. The zero output of the end of operand right flip-flop F1010 is applied as a third input to the gate 1001. The "one" output of the space-right flip-flop F1008 is applied as a third input to the gate 1002. Ordinarily, the end of operand right flip-flop F1010 is in its reset state, as described, and the space-right flip-flop F1008 is in its set condition, as heretofore described. The fourth input to each of gates 1001 and 1002 is the operation level S. The output of the gate 1001 and the output of the gate 1002 are applied through an "or" circuit to four gates of a set of seven, two-input gates 1003 (FIG. 1(d-d)), as described shortly. Only five bits of the output of the right HSM 16 (FIG. 1(d-c)) are applied through suitable "or" circuits the five inputs of the nines complementor 21 (FIG. 1(e-d)), as explained shortly. This nines complementor 21 converts the binary coded decimals (using the five least significant bits of the seven bit code) to their nines complements coded in four bits.

A pair of gates G13 and G14 (FIG. 1(e-d)) control the timing of the output of the complementor 21. The two-input gate G13 applies at one input a high level to the nines complementor 21 in any one of the high operation levels W, H, S, or M through suitable "or" circuits, and at a second input a pulse lasting from T6 to T7. Such a pulse may be secured from a flip-flop circuit (not shown) which is set with T6 and reset with T7, and the output taken from the "one" terminal. This long pulse, from T6 to T7, gates the output of the nines complementor 21 through gates (not separately shown here, but which may be considered as included in complementor 21.)

The output of the nines complementor 21 is only four bits, that is four leads each carrying binary digit information by its respective high or low level. These are the four least significant bits of the characters. The three most significant bits, to complete the coded number in the code for the machine, which is seven bits, are merely taken from the three most significant digits of the number being complemented. Thus the complemented number coded in the seven bit binary code employed in this machine is passed through the gates 1003 (FIG. 1(d-d)) to the Z register 14. Note that the parity bit is carried forward, but that parity is here ignored.

The circuits for the operation of subtraction are otherwise the same as for addition, and the operation is similar, with some exceptions noted hereinafter.

5.2.2 Operation Level S High and Operation

The instruction for subtraction is staticized as follows (see also FIG. 12):

O Section	A Section	B Section	C Section
Code No. for Subtraction....	Address of Minuend.	Address of Subtrahend.	Address of Difference.

Note that the characters from the subtrahend in the right HSM 16 (FIG. 1(d-c)) are always passed through the complementor 21 (FIG. 1(e-d)) before being placed in the Z register 14 (FIG. 1(d-d)). This procedure complements the digits of the space symbols, item separation symbols, and minus signs, as coded, as well as the digits of the operands. These latter complements are not always numeric. The space symbol (SP) (1000001) when complemented becomes the space-minus symbol (SPM) (1001001) the item separation symbol ISS (0111100) becomes ISS minus (ISSM) (0111001) the minus sign (0001001) when complemented becomes the minus zero (MZ) (0000000). After the instruction is staticized, the status level RS is selected by the output from status transition gate 1234 (FIG. 1 H), as in addition. The minuend characters from the left HSM 15 (FIG. 1(c-c)) are handled as the addend characters in addition. The five least significant bits of the subtrahend (designated as the 2⁴ to 2⁹ bits) are applied to the complementor. The three most significant bits (2⁴, 2⁵, and 2⁶ bits) bypass the complementor 21, as already mentioned, and are passed directly through the gates 1003 to the Z register 14.

The output of the nines complementor 21 is only four bits. Five bits are applied because the complementor distinguishes between certain symbols which otherwise would appear as numerics. For example, the ISS and space symbols. In the numerics, but not in other symbols, the 2⁴ bit is a one. After the least significant characters of the minuend and subtrahend have been stored in the Y and Z registers 13 and 14 respectively the procedure is the same as in addition, each subtrahend digit being complemented in turn.

The machine continues in RS (that is, with status level RS high) until the least significant digits of both the minuend and subtrahend are detected. The machine then selects the status level RI to be high, as in addition, by passing a pulse through the status transition gate 1255 (FIG. 1G). The machine then follows the reiterated RO-RI sequence explained in addition until the ends of both operands are reached, each subtrahend digit being passed through the nines complementor 21 in turn.

A three-input gate 1408 (FIG. 1(b-a)) is provided having three inputs, one from the status level RD, a second from the operation level S, and the third input from the first timing pulse T1. The output of the gate 1408 is applied only to the 20 bit (first bit) flip-flop of the O register 30. The coding is such that the operations add and subtract are coded the same, except that for the operation add, the first bit (the least significant bit) is "one," and for the operation subtract, the first bit is zero.

Accordingly, the 20 bit flip-flop of the O register 30 is in its set condition for the operation add, but when the operation level S, for subtract, is selected to be high, this flip-flop is placed in its reset condition when the instruction S is staticized. The gate 1408 applies the first timing pulse T1 to the set terminal of the 20 bit flip-flop only, when the status level RD becomes high. The circuit is such that the other flip-flops of the O register 30 are not affected. This application to leave the other flip-flop unaffected may be by a suitable "or" circuit (not shown).

In the operation of subtraction, (as in that of addition) an end around carry may occur, as for example where subtracting a negative number from a positive number. If the EOBO flip-flop F1110 (FIG. 1(f-c)) is in its set

condition, indicating that all the characters of both operands have been added or subtracted, note that in the status level RI, the status transition gate 1227 (FIG. 1H) is primed, if the carry flip-flop F2 is in its set condition, indicating an end around carry. If either the 2⁰ bit flip-flop of the adder output register 62 (FIG. 1(f-c)) is in set condition, or if the 2³ bit flip-flop of the adder output register 62 is in reset condition, then the status transition gate 1227 selects the status level RD to be high.

However, the gate 1408 (FIG. 1(b-a)) is primed with the high operation level S, and the high status level RD, to pass the first timing pulse T1 to change the O register 30 from a condition corresponding to the code for subtract to one corresponding to the code for add. The "one" held in the carry flip-flop F-2 is now added to the least significant character of the partial sum, as in addition, and the operation continues character by character until the end of the partial difference is reached, that is, the end of both operands. In this event, however, the carry flip-flop F-2 is now in its reset condition, and the status transition gate 1208 (FIG. 1H) causes the status level IC to be selected as high.

Two further special cases arise in the subtraction operation not present in an addition operation.

5.2.3 Special Cases

Case I: The end of the minuend operand is an ISS and the end of the complemented subtrahend is a Minus Zero (abbreviated MZ). The MZ is the result of complementing a Minus (9).

The following example shows the steps involved in such a subtraction:

871 - (-233) = 1104
 871 Minuend } on tape
 9233 Subtrahend }
 871 Minuend } in HSM 15, 16
 9766 Subtrahend }
 871 Minuend in Y register 13
 9233 Complemented Subtrahend in Z register 14
 1104 Ans. after storage in HSM

Case II: The end of the minuend operand is a minus and the end of the subtrahend operand is a minus.

An example showing steps involved in this subtraction:

871 - (-233) = -638
 871 Minuend } on tape
 9233 Subtrahend }
 9128 Minuend } After storage in HSM 15, 16
 9766 Subtrahend }
 9128 Minuend } In Y register 13
 9233 Complemented Subtrahend } In Z register 14
 9361 Ans. as stored in HSM

When this last answer is read out of the HSM to the tape it is complemented giving the answer 9638 (minus).

Because the subtrahend is complemented, its end of operand character ISS, space symbol, or zero symbol is complemented to be ISS minus, space minus, or zero minus (abbreviated respectively ISSM, SPM, or ZM) respectively. However, these last characters are recognized by the right symbol recognition circuits 23. Specifically, the "or" circuits R1053 have an output which is at a high level if and only if there is not a minus sign, as described. However, in the code of this machine, a SPM symbol and a minus symbol are the same except for the parity bit. (Recall that a minus symbol is 0001001 and a space symbol is 1000001, so that a SPM symbol is 1001001). In other words the complementor 21 so complements the non-numeric symbols as to cause certain pairs of these symbols (SPM and minus, for example) to be the same, parity bit excluded. Therefore, the NOT MR lead at the output of the "or" circuits R1053 (FIG. 1(d-d)) is also high if a NOT SPM symbol is stored in the Z register 14, as these two symbols are the same.

The "or" circuits R1055 (in a manner similar to the other recognition circuits 23) provide an output indicated as NOT ISSM only if an ISSM symbol is not recognized in the Z register 14. Similarly, a lead designated NOT MZ provides an output which is at a high level if, and only if, other than a minus zero symbol in the Z register 14 is "recognized" by a set of "or" circuits R1056. The NOT ISSM and NOT MZ leads have outputs applied through an inverter 117 (FIG. 1(d-e)) and an inverter 118 respectively. The respective inverter outputs are designated ISSM and MZ respectively, and each, respectively, is high if, and only if, the symbol ISSM or MZ, as the case may be, is stored in the Z register 14 (FIG. 1(d-d)).

Note that when any one of these ISSM, SPM, or MZ symbols are recognized during subtraction, the end of operand right flip-flop F1010 (FIG. 1(d-d)) is set, in the same manner as for ends of operands which are not complemented. For this purpose, an inverter 120 (FIG. 1(d-e)) has applied to its input the output of "or" circuits to which are applied the operation levels B, L, R, W, and H. The output of the inverter 120 (designated NOT (B, L, R, W, H)) is applied as one input to a four-input gate 1063. The gate 1063 has as a second input the status level RO, as a third input the output of the "or" circuit receiving the ISSM lead and the MZ lead. The fourth input to the gate 1063 is the eighth timing pulse T8. The output of the gate 1063 is applied to the set terminal S of the end of operand right flip-flop F1010 through "or" circuits. Therefore, note also that the Z register 14 (FIG. 1(d-d)) is not reset after one of these characters is reached, because the gate 1043 (FIG. 1(d-d)) is not primed. Therefore, the ISSM, SPM, and MZ symbols are repeated in the subtrahend until after the end of operand digit of the minuend is reached.

From the foregoing, it is apparent that the status level flow diagram of FIG. 13 is applicable to subtraction as well as to addition.

5.3 Multiplication (Operation M)—Operation Level High

For multiplication, the instruction is staticized in the usual way and arranged as follows (see also FIG. 12):

O Section	A Section	B Section	C Section
Code No. for Multiplication.	Address of the Multiplicand.	Address of the Multiplier.	Address of the Product.

At the eighth delayed timing pulse T8a, the transition is made from the high status level RO03 to select the high status level RS by the status transition gate 1234 (FIG. 1H), primed by the now high operation level M.

5.3.1 Additional Components

Certain components, other than those already described, are utilized for multiplication.

The nines counter 45 (FIG. 1(f-a)) has its various set input terminals connected, as though for a register, to receive the output of the nines complementor 21 (FIG. 1(e-c)) through a set of four, two-input gates G17 (FIG. 1(d-d)). Each of the gates G17 receive at its second input the high status level ROM or the high "one" output of the space right flip-flop F1008 (FIG. 1(d-e)).

A two-input gate G1 (FIG. 1(f-a)) is provided which receives at one input either one of the "one" output of the space-right flip-flop F1008 (FIG. 1(d-e)) or the high status level ROM through an "or" circuit. The fourth timing pulse T4 is applied as the second input to the gate G1. The output of the gate G1 is applied to all of the reset terminals of the nines counter 45.

A gate G2 has its output applied to the trigger terminal T of the lowest order (2⁰ bit) flip-flop of the nines counter 45. The gate G2 is primed by the high status level RN. The first timing pulse T1 is also applied to

the gate G2. The flip-flop stage corresponding to the 2³ bit (fourth order) of the nines counter 45 has its "one" output applied to a five-input gate 837 (FIG. 1(e-b)). The gate 837 also receives at a second input the 2⁰ bit "one" output of the nines counter 45 (FIG. 1(f-a)). The gate 837 receives as third and fourth inputs the high operation level M and the high status level RI, respectively. The second timing pulse TP2 is applied as the fifth input to the gate 837.

The "one" output of the 2³ flip-flop of the nines counter 45 is applied as one input to each of two status transition gates, a five-input gate 1239 and a four-input gate 1240, (FIG. 1H). Each of the two status transition gates 1239 and 1240 receives as a second input the high "one" output of the 2⁰ bit flip-flop of the nines counter 45 (FIG. 1(f-a)). Status transition gate 1239 (FIG. 1H) receives as third and fourth inputs the status level RI, and the operation level M, respectively. The status transition gate 1240 receives as a third input the status level RN. The status transition gates 1239 and 1240 receives as the fifth and fourth inputs, respectively, the eighth delayed timing pulse TP8a.

The output of a four-input gate 1138 (FIG. 1(e-a)) is applied to the set terminal S of the Been in RN flip-flop F1111. The gate 1138 receives as one input the "one" output of the EOBO flip-flop F1110, as a second input the high operation level M, as a third input the high status level RI, and as the fourth input, the eighth timing pulse T8. A two-input gate 1139 has its output applied to the reset R of the been in RN flip-flop F1111. The gate 1139 receives the status level RO03 and as the second input fifth timing pulse T5.

The zero output of the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is applied as one input to a five-input status transition gate 1251 (FIG. 1G). The status transition gate 1251 has its output applied through "or" circuits to the "set RI" lead. The status transition gate 1251 receives as its other four inputs the status level ROM, the NOT SPR lead, the NOT ISSR lead, and the eighth delayed timing pulse T8a.

The zero outputs of the 2⁰ and 2³ flip-flops of the nines counter 45 (FIG. 1(f-a)) are passed through a suitable "or" circuit to provide an output indicated as "nines counter not 9." If, and only if, the nines counter 45 holds a count which is not nine, is the "nines counter not 9" lead high. In this connection, as will appear more fully hereinafter, the nines counter 45 does not hold a count higher than nine at any time.

The "nines counter not 9" output (FIG. 1(f-a)) is applied as one input to a four input status transition gate 1265 (FIG. 1G) and as one input to a three-input status transition gate 1266 (FIG. 1G). The output of each of status transition gates 1265 and 1266 is applied through "or" circuits to the "set RO" lead. The status transition gate 1266 receives as a second input the status level RN, and as the third input the eighth delayed timing pulse T8a. The status transition gate 1265 receives as a second input the status level ROM, as a third input the high "one" lead from the "been in RN" flip-flop F1111 (FIG. 1(e-a)), and as a fourth input the eighth delayed timing pulse T8a.

The high "one" output of the EOBO flip-flop F1110 (FIG. 1(f-c)) is applied as one input to a four-input status transition gate 1237 (FIG. 1H). The status transition gate 1237 has as second and third inputs the status level RI and the operation level M, respectively. The eighth delayed timing pulse T8a is applied as the fourth input to the status transition gate 1237. The output of the status transition gate 1237 is applied to the "set RN" lead.

A four-input status transition gate 1207 (FIG. 1H) is provided. One input to the status transition gate 1207 is from a suitable "or" circuit (FIG. 1H) which receives as inputs the ISSL lead (FIG. 1(c-d)) and the ISSR lead (FIG. 1(d-e)). A second input to the status transition

gate 1207 is from the operation level M. A third input to the status transition gate 1207 is from the status level RS. The eighth delayed timing pulse T8a is applied as the fourth input to the status transition gate 1207. The output of the status transition gate 1207 is applied through "or" circuits to the "set IC" lead.

A seven input status transition gate 1252 (FIG. 1G) is provided. Four of the inputs to the status transition gate 1252 are respectively from the lead NOT SPR (FIG. 1(d-e)), NOT ISSL (FIG. 1(b-d)), NOT SPL (FIG. 1(b-d)), and NOT ISSR (FIG. 1(d-d)). A fifth input to the status transition gate 1252 is from the status level RS, and a sixth input is from the operation level M. The eighth delayed timing pulse T8a is applied as the seventh input to the status transition gate 1252. The output of the status transition gate 1252 is applied through "or" circuits to the "set RI" lead.

A status transition gate 1271 (FIG. 1G) is provided having four inputs. The first input is the status level RI. The second input is the operation level M. A third input is from the "nines counter not 9" lead. The fourth and final input is from the eighth delayed timing pulse T8a. The output from status transition gate 1271 is applied through "or" circuits to the "set RO" lead.

A four-input gate 696 (FIG. 1(c-c)) is provided one input of which is the operation level M. A second input is from a three input "or" circuit having applied to its three inputs respectively the three status levels RI, RO, and RD. A third input to the gate 696 is the first timing pulse T1. The fourth input to the gate 696 is from the "one" output terminal of the 2⁰ bit flip-flop of the C register 28 (FIG. 1(c-a)). The output of the gate 696 is applied through suitable "or" circuits to that same input of the gate 660 (FIG. 1(c-b)) which receive the output of the gate 694.

A four-input gate 301 (FIG. 1(c-b)) is provided having one of its inputs connected to receive the output of the "nines counter not 9" lead (FIG. 1(f-a)). A second input to the gate 301 (FIG. 1(c-b)) is from the operation level M. A third input to gate 301 is from the status level RI. The fourth input to the gate 301 is from the second timing pulse T2. The output of the gate 301 is applied through suitable "or" circuits of the trigger terminal T of the C counter 12.

A gate 1041 (FIG. 1(d-d)) has two inputs, one of which is received from an "or" circuit having applied to it the operation levels RO01 and ROM. The other input to the gate 1041 is from an "or" circuit having two inputs, to one of which is applied the fourth timing pulse T4 and to the other of which is applied the eighth timing pulse T8. The output of the gate 1041 is applied through "or" circuits and the delay circuit D56 of the reset terminals R of the Z register 14. Note that when the status level RO01 is high, the fourth timing pulse T4 and also the eighth timing pulse T8 are passed to reset the Z register 14. Further, when the status level ROM is high, the fourth timing pulse T4 and the eighth timing pulse T8 reset the Z register 14 through the gate 1041 and delay circuit D56.

A gate 510 (FIG. 1(c-b)) is primed by either one of the high status levels RO03 or RN applied through suitable "or" circuits. The fourth timing pulse T4 is also applied to the gate 510. The output of the gate 510 primes a set of nine, two input gates 514 (FIG. 1(c-b)) connected between the nine outputs respectively of the A register 26 (FIG. 1(c-a)) and the respective inputs of the A counter 10 (FIG. 1(c-b)).

A two-input gate 305 (FIG. 1(c-a)) has applied to it as one input the status level RN. The gate 305 also receives the fourth timing pulse T4. The output of the gate 305 is applied through an "or" circuit to prime a set of nine, two-input gates 308 connected between the output of the C register 28 and the input of the C counter 12.

A set of nine, five-input gates 414 (FIG. 1(b-a)) are connected to receive as one input for each of the respec-

tive binary digits (or contents) stored in the A counter 10 (FIG. 1(c-b)). The outputs of the gates 414 are applied as inputs to the A register 26 (FIG. 1(c-a)). The gates 414 each receive as the four inputs in addition to the corresponding "one" output of the A counter 10 flip-flops (FIG. 1(c-b)), first, the output of the space-left flip-flop F911 (FIG. 1(c-e)), second the operation level M, third the status level RS, and finally the second timing pulse T2.

A four-input gate 1039 (FIG. 1(c-d)) receives one input from the NOT SPR lead (FIG. 1(d-d)). A second input to gate 1039 (FIG. 1(c-d)) is from the operation level M; and a third input is from the status level RS. The fourth input to the gate 1039 is from the eighth timing pulse T8. The output of the gate 1039 is applied through "or" circuits and delay circuit D56 (FIG. 1(d-d)) to the reset terminals R of the Z register 14 (FIG. 1(d-d)).

A three-input gate 693 (FIG. 1(d-c)) has one input from the operation level M. A second input is from either one of the high status levels ROM or RS applied through an "or" circuit. The first timing pulse T1 is the third input to the gate 693. The output of the gate 693 is applied through "or" circuits to the gates 670.

A two-input gate 303 (FIG. 1(c-b)) is primed by the high status level ROM to pass the second timing pulse T2 applied thereto. The output of the gate 303 is applied through an "or" circuit to the trigger terminal T of the C counter 12.

A two-input gate 511 (FIG. 1(c-b)) is primed by the high status level RN to pass the first timing pulse T1, applied thereto, through an "or" circuit to the reset terminal R of the A counter 10.

A four-input gate 1069 (FIG. 1(d-d)) is primed by the high status level RD, the high operation level M, and the high SPR lead. The eighth timing pulse T8 is applied to the gate 1069. The output of the gate 1069 is applied through "or" circuits and the delay circuit 56 to the reset terminal R of the Z register 14.

A four-input gate 1106 (FIG. 1(f-c)) is provided which receives at one input the high status level RS. At a second input the gate 1106 receives either of the high levels from leads ISSL or ISSR (FIG. 1(c-d) and 1(d-e)) respectively from an "or" circuit (FIG. 1(f-c)) as shown. A third input to the gate 1106 is from either of the high operation levels E or M. The fourth input to the gate 1106 is from the eighth timing pulse T8.

A three-input gate 1130 (FIG. 1(e-b)) receives as one input the operation level M, and as a second input the output from the "one" terminal of the EOBO flip-flop F1110 (FIG. 1(f-c)). The third input to the gate 1130 is from the eighth timing pulse T8. The output of the gate 1130 is applied through "or" circuits to reset the ISSL and space left flip-flops F910 and F911 (FIG. 1(c-e)), the space right and end of operand right flip-flops F1008 and F1010 (FIG. 1(d-e)), and the Y register 13 (FIG. 1(c-d)).

A set of nine, three-input gates 418 (FIG. 1(c-a)) are primed by the high status level ROM as a first input. The gates 418 receive the eighth timing pulse T8 as a second input. The nine gates 418 are connected respectively between the nine "one" output terminals of the C counter 12 (FIG. 1(c-b)) as the third input, and the set terminals of the nine lowest order stages of the C register 28 (FIG. 1(c-a)).

A two-input gate 490, primed by the high status level ROM as one input, is connected to apply its output to the set terminal of the 2⁹ stage flip-flop (10th order stage) of the C register 28 (FIG. 1(c-a)).

A two-input gate 863 (FIG. 1(d-c)) has its output applied through an "or" circuit to the read-out circuits of the right HSM 16. One input to the gate 863 is from the operation level M and the second is from the status level RD.

A status transition gate 1224 (FIG. 1G) has seven inputs as follows: (1) a "been in RN flip-flop" F1111

(FIG. 1(e-a)) "one" terminal; (2) the status level ROM; (3) the NOT ISSR lead from "or" circuits R1054 (FIG. 1(d-d)); (4) the NOT SPR lead from "or" circuits R1052 (FIG. 1(d-e)); (5) the "one" terminal of the 2³ flip-flop of the nines counter 45 (FIG. 1(f-a)); (6) the "one" terminal of the 2⁰ flip-flop of the nines counter 45; and (7) the eighth delayed timing pulse T8a. Note that the concurrence of the two high levels (from the 2³ and 2⁰ flip-flops) from the counter 45 required to prime this status transition gate 1224 is equivalent to requiring the count in this counter 45 to be nine before the gate may open. The output of the status transition gate 1224 is applied through "or" circuits to the "set RD" lead.

A three-input status transition gate 1206 (FIG. 1H) has applied to one input the high status level ROM. A second input to the status transition gate 1206 is from an "or" circuit receiving inputs from the SPR lead from inverter I4 (FIG. 1(d-e)) and the ISSR lead from inverter I12 (FIG. 1(d-e)). The third input to the status transition gate 1206 is from the eighth delayed timing pulse T8a. The output of the status transition gate 1206 is applied through "or" circuits to the "set IC" lead.

A three-input status transition gate 1250 (FIG. 1G) is provided primed by the high operation level M as a first input and the high status level RD as a second input. The eighth delayed timing pulse T8a is applied as the third input of the gate 1250. The output of the gate 1250 is applied through "or" circuits to the "set RI" lead.

5.3.2 Detailed Operation

5.3.2.1 Status Level RS High

At the completion of the staticizing of the instruction for multiplication where the status level RO03 is high, the status level RS is selected to be high by the passage of the eighth delayed timing pulse T8a through the status transition gate 1234 (FIG. 1H). The operations matrix OM has caused the operation level M to become high during the status level RO01 while the instruction was being staticized.

Note that the space-left flip-flop F911 (FIG. 1(c-e)) is in the set condition because of the first timing pulse T1 passed by the gate 945 (FIG. 1(c-e)) during the high status level RO03. Also the space-right flip-flop F1008 (FIG. 1(d-e)) is in the set condition, being set by the same pulse from the same gate 945.

T1

With the operation level M high and with the status level RS high, the machine operation is very similar to that in addition. The A counter 10 addresses the multiplier location in the left HSM 15 through the gates 640 in the same manner as it addresses the addend in addition. The B counter 11 addresses the HSM 16 at the location of the multiplier through the gates 670. The A register 26 is cleared by the first timing pulse T1 passed through the gate 404.

T2

At the second timing pulse T2, the gates 414 (FIG. 1(b-a)), primed by the space-left flip-flop F911 (FIG. 1(c-e)) "one" output, pass the contents of the A counter 10 (FIG. 1(c-b)) into the A register 26 (FIG. 1(c-a)). The count in the B counter 11 (FIG. 1(d-b)) is advanced one by a pulse from the gate 508.

T3

At the third timing pulse T3, the A counter 10 (FIG. 1(c-b)) is advanced one by a pulse from the gate 505. By advance of the A and B counters 10 and 11, successively least significant digits are read-out in each RS cycle from the memory banks until a non-space character is encountered.

81

T4

The nines counter 45 (FIG. 1(f-a)) has four flip-flop stages and is so termed because it is used to count up to nine starting from the complement of each multiplier digit. The nines counter 45, if the "one" terminal of the space right flip-flop F1008 is high, is reset by the fourth timing pulse T4 passed through the gate G1, primed by the output from the "one" terminal of the space right flip-flop F1008 (FIG. 1(d-e)), preparatory to entry of the complement of the multiplier digit during the succeeding sixth to seventh timing pulses T6-T7. In other words, if a space is not recorded in the Z register 14, the nines counter 45 is reset at the fourth timing pulse T4.

The Y register 13 (FIG. 1(c-d)) is reset by the fourth timing pulse T4 applied from the gate 902 (FIG. 1(b-d)). The Z register 14 (FIG. 1(d-d)) is reset by the fourth timing pulse T4 passed through the gate 1042 and thence through the delay circuit D56.

Note that with the status level RS high and the operation level M high, the left and right read-out gates 730 (FIG. 1(c-c)) and 862 (FIG. 1(d-c)) apply a high level to activate the read out circuits respectively of the left and right HSM 15 and 16 (FIGS. 1(c-c) and 1(d-c)) respectively.

Accordingly the left and right HSM 15 and 16 are conditioned for reading out information.

T6

With the occurrence of the sixth timing pulse T6, the contents of the left HSM 15 (FIG. 1(c-c)) at the location addressed at the first timing pulse T1 from the A counter 10 (FIG. 1(c-b)) are now passed through gates 911 (FIG. 1(c-d)), primed by the sixth timing pulse T6 from the gate 918, into the Y register 13. The gate 918 is primed by the "one" output from the space-left flip-flop F911 (FIG. 1(c-e)). The contents of the right HSM 16 (FIG. 1(d-c)) as addressed by the B counter 11 (FIG. 1(d-b)) pass into the Z register 14 (FIG. 1(d-d)) through the gates 1032. The gates 1032 are opened or primed at the sixth timing pulse T6 from the gate 1031 (FIG. 1(c-d)).

T6 to T7

During the occurrence of an enlarged timing pulse T6 to T7, the gate G13 (FIG. 1(e-c)) applies a high level to the nines complementor 21 to open the output gates of the nines complementor 21. Accordingly, the four least significant bits of the least significant digit of the multiplier in the right HSM 16 (FIG. 1(d-c)) are passed through the gates G17 (FIG. 1(d-d)) primed by the space right flip-flop F1008 (FIG. 1(d-e)) "one" output. From the gates G17, (FIG. 1(d-d)) these four bits are applied to the nines counter 45 (FIG. 1(f-a)). Thus, the nines counter 45 holds the nines complement of the least significant digit of the multiplier (or of a space, as the case may be). Recall again that in the code employed in this machine the least four significant digits of the binary coded character, in the case of decimal numbers, conform to the decimal number written in binary code.

T7

At the occurrence of the seventh timing pulse T7, the gate 944 (FIG. 1(d-e)) passes the seventh timing pulse T7 to reset the space-left and space-right flip-flops F911 and F1008 (FIG. 1(c-e) and 1(d-e)) respectively.

T8

The Z register 14 (FIG. 1(d-d)) is reset by the eighth timing pulse T8 passed through the gate 1039 and the delay circuit D56 after passing along through suitable "or" circuits as shown.

The gate 1106 (FIG. 1(f-c)) insures that if, during the status level RS, when another ISS symbol is encountered

82

showing that the operand is absent, the previous result zero flip-flop F1101 (FIG. 1(f-c)) is set.

Thus far, except for the entry into the nines counter 45 (FIG. 1(f-a)), and the re-registration in the A register 26 (FIG. 1(c-a)) of the count in the A counter 10 (FIG. 1(c-d)), the operation has followed substantially the steps found in the operation for addition A, with the status level RS high. However, with the operation for multiplication, there are now presented three possibilities, as follows:

A. Either or both characters are a space, and another cycle of timing pulses follows with status level RS high.

B. An item separation symbol is recognized, in which case one of the operands is missing.

C. The least significant character of each operand is recognized, and, in status level RI, the actual multiplication begins.

In connection with the further description of the operation when changes of status levels are involved, it is suggested that reference be made to the flow diagram for multiplication, FIG. 14 as well as to the larger schematic, FIG. 1.

5.3.2.1a One or Both Characters Space

The first possibility presented is that the character recorded in either the Y register 13 or the Z register 14 or both is a space. If the character in the Z register 14 is a space, the space-right flip-flop F1008 is set because the space-right lead SPR, heretofore described, is at a high level, and the gate 1057 (FIG. 1(d-e)), having applied to it the high RS level, passes the eighth timing pulse T8 to set the space-right flip-flop F1008.

If the character in the Y register 13 is a space, the space left flip-flop F911 (FIG. 1(c-e)) is set by the eighth timing pulse T8 from gate 938.

If both characters in the Y and Z registers 13 and 14 are spaces, both space left and space right flip-flops F911 and F1008 are set.

In either situation, with the space left or the space right flip-flop F911 and F1008 set, another RS cycle is repeated, as in addition. Another character is read out of the left HSM 15 or the right HSM 16 from one or the other or both sides containing spaces. If a not-space character, other than an item separation symbol ISS, has been read out from either the left or right HSM 15 or 16, the space left flip-flop F911 (FIG. 1(c-e)) or the space right flip-flop F1008 (FIG. 1(d-e)) of that particular side is in the reset condition. Accordingly, the character is held in the Y or Z registers 13 or 14, respectively, as the case may be. If a not-space character other than the item separation symbol ISS has finally been read into both the Y and Z registers 13 and 14, the status transition gate 1252 (FIG. 1G) passes the eighth delayed timing pulse T8a to the "set RI" lead. Accordingly, the status level RI now becomes high.

5.3.2.1b ISS Before Other Character

The second possibility of the three at the end of an RS cycle is that the character in either one of the Y or Z registers 13 or 14 is an item separation symbol ISS. Accordingly, the left symbol recognition circuits 22, or the right symbol recognition circuits 23 respectively cause the output lead NOT ISSL from "or" circuits R922 (FIG. 1(b-d)) or the output lead NOT ISSR from "or" circuits R1054 (FIG. 1(d-d)) to be low as the case may be. If the item separation symbol is in the Y register 13, then the ISSL lead from the ISSL inverter I11 (FIG. 1(c-d)) is at a high level. If the item separation symbol is stored in the Z register 14, then the ISSR lead from the inverter I12 (FIG. 1(d-e)) is at a high level. In either event, the status transition gate 1207 (FIG. 1H) is primed by either one of the ISSL or ISSR leads. Consequently, the status transition gate 1207 passes the eighth delayed timing pulse T8a to the set IC lead. Therefore the status level IC is

selected to be high. A new instruction is then withdrawn or a new surge of instructions occurs. At this point the presence of the item separation symbol in coded form in either the Y or Z registers 13 or 14, indicates that one of the operands is missing. In later stages of operation, the presence of the item separation symbol in the Z register 14 indicates that the end of the multiplier has been reached and that the instruction is complete.

5.3.2.1c Non-Space Characters

The third possibility at the end of an RS cycle is that the first non-space character of a multiplier is read out of the right HSM 16, and a non-space character is read out of the left HSM 15. The status transition gate 1252 (FIG. 1G) then passes the eighth delayed timing pulse T8a to the "set RI" lead. The status level RI becomes high.

5.3.2.2 Status Level RI High (For First Multiplier Digit Zero)

T1

However, two types of operation follow depending on whether the first non-space character of the multiplier is a zero or other non-space character. First, assume it is a zero.

The R register 19 (FIG. 1(d-c)) is reset by a pulse from the gate 860 at the first timing pulse T1. The right HSM 16 (FIG. 1(d-c)) is addressed by contents of the C counter 12 (FIG. 1(c-b)) at the location of the least significant digit of the product through nine gate 660. The gates 660 are opened by the first timing pulse T1 passed through the gate 696 (FIG. 1(c-c)). Note that in multiplication in this machine, the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is set. In other words, the multiplier is always taken from the right HSM 16.

T2

Note that the "Been in RN" flip-flop F1111 (FIG. 1(e-a)) was previously reset by the output of the gate 1139. Note that the count in the nines counter 45 is at nine because the first multiplier digit is assumed zero. Therefore, the 2⁰ and 2³ stages of the nines counter 45 are set. The second timing pulse T2 is passed by the gate 837 (FIG. 1(e-b)) and is applied to set the 2⁴ and 2⁶ bit flip-flops of the R register 19 (FIG. 1(d-c)).

T5

The contents of the R register 19 are now entered into the right HSM 16 through the gates 851. Note that the 2⁹ bit of the C register 28 is set. The output of the inverter 19 (FIG. 1(d-b)) is high because neither operation level X or J are high. As the status level RI is high, all inputs of the right read-in gate 850 are primed. Accordingly, the gate 899 is primed both by the output of the gate 850 and the NOT RIS lead applied thereto. Therefore the gates 851 are open and the right HSM 16 is in condition to receive the information stored in the R register 19. The digit corresponding to zero has now been read into the right HSM 16 as the first partial product digit. The 2⁴ and 2⁶ bits have been artificially set to conform the entry to a coded numeric zero. Note that the multiplier zero read out from the right HSM 16 is artificially read in to the right HSM 16 as the product of that multiplier digit.

If the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is in reset condition, and no spaces are detected at the memory outputs, the status transition gate 1251 passes the eighth delayed timing pulse T8a to the "set RI" lead. The status level RI is then high again.

T8a

At the eighth delayed timing pulse T8a, the status transition gate 1239 selects the status level ROM to be high. Note that the nines counter 45 (FIG. 1(f-a))

count is nine. The status transition gate 1239 (FIG. 1H) is therefore primed to cause the status level ROM to become high.

5.3.2.3 Status Level RI High (For NON-zero Multiplier Digit)

The high status level RI has been selected, at the end of the last RS cycle, as mentioned above, by the status transition gate 1252 (FIG. 1G) passing the eighth delayed timing pulse T8a to the "set RI" lead.

T1-T3½

At the first timing pulse T1, the gates 660 (FIG. 1(c-b)) pass the contents of the C counter 12, to the address circuits of the right HSM 16 (FIG. 1(d-c)). The Y register 13 (FIG. 1(c-d)) now contains the least significant character of the multiplicand. The contents of the Z register 14 (FIG. 1(d-d)) is the partial product digit, which may be assumed a zero at this point. Recall that the Z register 14 was reset through the gate 1039 (FIG. 1(c-d)) in the preceding RS cycle. The contents of the Y register 13 and the Z register 14 are passed through the gates 27 and 21 (FIG. 1(e-a)) respectively, as in addition, into the duplicated adder and binary to coded decimal converter 17.

T1½

At the timing pulse T1½, the adder flip-flop F4 (FIG. 1(e-c)) is set by a pulse from the gate G10.

T1¾-T2¾

At T1¾ to T2¾, the contents of the BCDC 17B (FIG. 1(e-b)) are passed into the L register 18 and the R register 19 (FIG. 1(b-c) and 1(d-c)) through the gates 717 (FIG. 1(f-c)) and the gates 841 (FIG. 1(e-b)). The operation here is as in addition. Notice that the gates 717 (FIG. 1(f-c)) and 749 (FIG. 1(b-c)) and the gates 841 and 842 (FIG. 1(e-b)) are opened in multiplication (operation level A is low and M is high) only if the nines counter 45 is not at count nine, because in this particular cycle the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is not set.

At the second timing pulse T2 the gate 301 (FIG. 1(c-b)) causes the C counter 12 to be increased by one. The gate 872 (FIG. 1(e-b)) passes a pulse to set the 2⁴ bit in the R register 19 in the same manner as in addition and for the same reason. The gate 749 (FIG. 1(b-c)) passes a pulse to set the 2⁴ bit in the L register 18, by passing the second timing pulse T2, as in addition.

T5

The gate 899 (FIG. 1(d-c)) passes the fifth timing pulse T5, being primed by the output of the right read-in gate 850, so that the gates 851 (FIG. 1(d-c)) pass the contents of the R register 19 into the right HSM 16. Thus the least significant partial product character now stored in the R register 19 is read into the right HSM 16 at the address that was specified by the C counter 12 at the preceding first timing pulse T1.

Note that the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is always set in multiplication. The reason is, as will appear more fully hereinafter, that the multiplier is always taken from the right HSM 16 to afford easy complementation. The nines complementor 21 is associated in this particular machine only with the right HSM 16 output. Accordingly, the multiplicand is always taken from the left HSM 15. As the multiplicand and the partial product are added together the number of times specified by the multiplier digit, the partial product is stored in the right HSM 16, so that the multiplicand from the left HSM 15 may be added repeatedly to the partial product sum, different each time, from the right HSM 16. Thus in programming multiplication, the programmer arranges that the 2⁹ bit flip-flop of the C register 28 is set.

85

T8a

There are now three possibilities: (1) If the nines counter 45 (FIG. 1(f-a)) count is not nine, the status transition gate 1271 (FIG. 1G) passes the eighth delayed timing pulse T8a to the set RO lead. Accordingly, the status level RO is selected, and the cycle with the high status level RO high is next described.

(2) If, however, the nines counter 45 (FIG. 1(f-a)) count is nine, indicating that a zero was read out as the multiplier digit, the status transition gate 1239 (FIG. 1H) passes the eighth delayed timing pulse T8 to the set ROM lead. A new multiplier digit is read out.

(3) If the end of both operands has been recognized and the EOBO flip-flop F1110 is set, then the status transition gate 1237 passes the eighth delayed timing pulse T8a to the set RN lead.

Note that if the "nines counter not 9" lead is low, the multiplicand has not been added into the partial product the number of times called for by the current multiplier digit, and the end of both operands cannot have been reached.

5.3.2.4 Status Level RO High

T1

At the first timing pulse T1, the left HSM 15 (FIG. 1(c-c)) is addressed through the gates 640 (FIG. 1(c-b)), as in addition, with the address found in the A counter 10 (FIG. 1(c-b)). The right HSM 16 (FIG. 1(d-c)) is addressed by the C counter 12 (FIG. 1(c-b)) through the gates 660 (FIG. 1(c-b)), as in addition.

T2

The count of the A counter 10 (FIG. 1(c-b)) is increased by one by application of the second timing pulse T2 through the gate 504, as in addition. The A counter 10 now contains the address of the next least significant digit of the multiplicand.

T4

The Y register 13 (FIG. 1(c-d)) is reset at the fourth timing pulse T4 passed through the gate 903. The Z register 14 (FIG. 1(d-d)) is reset by the fourth timing pulse T4 passed through the gate 1043 and the delay circuit D56. In this connection, note that the minus left flip-flop F909 (FIG. 1(b-e)) is in the reset condition, as no negative numbers are employed in multiplication (except as a specially programmed subroutine). Also note that the end of operand right flip-flop F1010 (FIG. 1(d-e)) is in the reset condition until a space is recognized by the right symbol recognition circuits 23.

The read-out circuits of the left HSM 15 and the right HSM 16 are primed for read-out by the left and right read-out gates 730 and 826 (FIG. 1(c-c) and 1(d-c)) respectively.

T6

At the sixth timing pulse T6 the contents of the left HSM 15, at the location addressed during the first timing pulse T1 by the A counter 10, are read out to the Y register 13 through gates 911 (FIG. 1(c-d)), as in addition. In a similar manner, the contents of the right HSM 16, at the location addressed by the C counter 12 at the previous timing pulse T1, are read out to the Z register 14 through gates 1032 (FIG. 1(d-d)) as in addition.

Y Register Contents Space

A special case arises if the character in the Y register 13 (FIG. 1(c-d)) is a space. In this event, the gate 938 (FIG. 1(c-e)) is primed as in addition to pass the eighth timing pulse T8 to set the space-left flip-flop F911 (FIG. 1(c-e)). Note that the gate 938 is primed either by a high operation level R or when none of the operation levels B, L, R, W, or H are high, designated as NOT (B, L, R, W, H). Actually, one input could simply be NOT (B, L, W, and H) and the input R could then be omitted. However, the input NOT (B, L, W, R,

86

and H) is available in the machine for other purposes and so is more easily used. Occasional examples of such apparent redundancy may be found elsewhere. If the space left flip-flop F911 is set, note that the gates 27 (FIG. 1(e-a)) for the Y register 13 are blocked by the low output from the inverter I7. The equivalent action is to add a zero from the multiplicand through the duplicated adder and BCDC 17.

T8a

At the eighth delayed timing pulse T8a, the status transition gate 1249 (FIG. 1G), primed by the high status level RO, now passes the eighth delayed timing pulse T8a to the set RI lead. Accordingly, the status level RI is selected to be high.

5.3.2.5 RI-RO-RI Sequence

The next RI sequence is similar to that described above for the first RI sequence for operation M. The RI-RO sequence is repeated until the end of both operands (multiplicand and partial product) are recognized indicating that the entire multiplicand has been added once to the entire partial product. At this point, with status level RI high, the EOBO flip-flop F1110 (FIG. 1(f-c)) is set. The status transition gate 1237 (FIG. 1H) passes the eighth delayed timing pulse T8a to the set RN lead. In the succeeding cycle with the status level RN high, the multiplicand is added again to the partial product. The addresses of the partial product and multiplicand are renewed, as described below, during this succeeding high status level RN.

As the last of these additions in the RI-RO sequence is completed in RI, the last digit of the partial product addressed from the C counter 12, and the last digit of the multiplicand, addressed from the A counter 10, are added. Finally, as in ordinary addition, two end of operand characters are withdrawn, one from the left HSM 15 and one from the right HSM 16. The EOBO flip-flop F1110 (FIG. 1(f-c)) is set. Note that the ISSL and space left flip-flops F910 and F911 (FIG. 1(c-e)), the space right and end of operand right flip-flops F1008 and F1010 (FIG. 1(d-e)), and the Y register 13 are reset at T8 in the RI cycle, when the EOBO flip-flop is set, by a pulse from the gate 1130 (FIG. 1(f-b)).

Also note that only if the nines counter 45 count is not nine, should the multiplicand be added again to the partial product. If the nines counter were nine, as appears hereinafter the status level RI cannot become high. When the nines counter 45 count is nine, ordinarily the next status level to be high is ROM (to read out a new multiplicand) or IC.

The status transition gate 1237 (FIG. 1H) is primed by the output from the "one" terminal of the EOBO flip-flop F1110. Therefore, assuming the nines counter 45 count is not nine, the status transition gate 1237 causes selection of the status level RN to be high. The multiplicand and partial product addresses are to be renewed. The machine operation in multiplication with status level RN high is now described.

5.3.2.6 Status Level RN High (Renew Multiplicand and Partial Product Address)

At the first timing pulse T1, the count of the nines counter 45 (FIG. 1(f-a)) is increased by one by the output of the gate G2. The A and C counters 10 (FIG. 1(c-b)) and 12 are reset by the first timing pulse T1 passing through the gates 511 and 328 respectively.

T4

At the fourth timing pulse T4, the address of the least significant digit of the multiplicand is transferred from the A register 26 (FIG. 1(c-a)) to the A counter 10 (FIG. 1(c-b)) through the gates 514 (FIG. 1(c-b)) opened by a pulse from the gate 510.

87

Note that in status level RS in multiplication, the A counter contents were transferred to the A register (on occurrence of the second timing pulse T2) before the A counter is advanced (on occurrence of the third timing pulse T3). Thus the A register retains the address of the lowest digit of the multiplier. There is no shift in address on renewal of the multiplier, as for the multiplicand.

The corresponding digit of the partial product to be read out has its address stored in the C register 28 (FIG. 1(c-a)). The address from the C register 28 is passed through the gates 308 (FIG. 1(c-a)), primed by the fourth timing pulse T4 passed by the gate 305 into the C counter 12 (FIG. 1(c-b)).

T8a

At the eighth delayed timing pulse T8a, if the nines counter 45 is not nine, the status transition gate 1266 (FIG. 1G) output selects the status level RO to be high.

The RO-RI sequence is now repeated until the end of both operands (multiplier and partial product) is again reached. In effect, the multiplicand is one operand and the partial product is another operand for an addition. The EOBO flip-flop F1110 (FIG. 1(f-c)) is then set, and the RN status level is again high. This sequence of events is repeated until the nines counter 45 (FIG. 1(f-a)) registers a nine during the high status level RN, being advanced with the first timing pulse T1. When the nines counter 45 registers a nine, the multiplicand has been added to the partial product a number of times equal to the digit of the multiplier which was last read out of the right HSM 16. Accordingly, the status transition gate 1240 (FIG. 1H) during the high status level RN, passes the eighth delayed timing pulse T8a to the set ROM lead, and the status level ROM is now selected to be high.

5.3.2.7 Status Level ROM High

The B counter 11 (FIG. 1(d-b)) holds the address of the second (or next) least significant digit of the multiplier, entered by the advance of the count when the last RS (or ROM) level was high by the second timing pulse T2 passed through the gate 508. The right HSM 16 (FIG. 1(d-c)) is now addressed by the B counter 11 through the gate 670 (FIG. 1(d-b)) primed by the output of the gate 693 (FIG. 1(d-c)).

T2

The B counter 11 (FIG. 1(d-b)) count is now advanced by one by a pulse passed through the gate 508 to hold the address of the next least significant digit of the multiplier. The C counter 12 (FIG. 1(c-b)) count is advanced one by a pulse from the gate 303. In effect, this advance of the C counter 12 count causes a shift of the partial product. The advance is the equivalent of selecting the next digit to the left in the partial sum thus far computed. It is as though, in ordinary long hand multiplication, after entering the product of a multiplier digit and the multiplicand, one added the result. Then the multiplicand is multiplied, starting from the right, by the next multiplier digit, and the entry is then started one place to the left of the first entry. Thus the partial product sum is, in effect, shifted right, or the subsequent entry shifted left. The C register 28 (FIG. 1(c-a)) is reset at the second timing pulse T2 passed through the gate 442.

T4

The Z register 14 (FIG. 1(d-d)) is reset by the fourth timing pulse T4 from the gate 1041 through the delay circuit D56. The nines counter 45 (FIG. 1(f-a)) is reset by the fourth timing pulse T4 passed through the gate G1.

The right HSM 16 (FIG. 1(d-c)) is actuated for reading out by the right read out gate 862 (FIG. 1(c-c)).

88

The left HSM 15 (FIG. 1(c-c)) read-out circuits are also actuated.

T6

The gates 1032 (FIG. 1(d-d)) are opened by the sixth timing pulse T6 from the gate 1030 (FIG. 1(c-d)) to enter from the right HSM 16 (FIG. 1(d-c)) the next least significant digit of the multiplier into the Z register 14 (FIG. 1(d-d)). A long pulse T6-T7 passes through the gate G13 (FIG. 1(e-d)) to open the gates of the nines complementor 21. The next least significant digit of the multiplier, entered in the Z register 14 (FIG. 1(d-d)), is also applied from the right HSM 16 (FIG. 1(d-c)) through the nines complementor 21 (FIG. 1(e-c)) and the gates G17 (FIG. 1(d-d)) so that the four least significant binary digits of the complement are applied to the nines counter 45. Thus the nines counter 45 is set to the nines complement of the next least significant digit of the multiplier.

T7

At the seventh timing pulse T7, the gate 944 (FIG. 1(d-e)) passes a pulse to reset the space-left flip-flop F911 (FIG. 1(c-e)), the space-right flip-flop F1008 (FIG. 1(d-e)) and the end of operand right flip-flop F1010.

T8

The eighth timing pulse T8 is passed by the gate 1041 (FIG. 1(d-d)) through the delay circuit D56 to reset the Z register 14. The nine bits corresponding to the 2^0 to 2^8 bits of the binary number in the C counter 12 (FIG. 1(c-b)) are passed through the gates 418 (FIG. 1(c-a)) on the occurrence of the eighth timing pulse T8 and entered in the nine lowest order stages of the C register 28 (FIG. 1(c-a)). A tenth bit, corresponding to the 2^9 bit in the C register 28, is set by the eighth timing pulse T8 passed through the gate 490.

The high status level ROM (for read out multiplier digit) has the effect also of a partial product shift. Note that a place has been selected by the C counter 12 (FIG. 1(c-b)) in the right HSM 16 (FIG. 1(d-c)) for storage of the first partial product. The C counter 12 (FIG. 1(c-b)) is advanced one, when the new multiplier digit is read out, and its contents stored in the C register 28 (FIG. 1(c-a)). Accordingly, when the new multiplicand is repetitively added into the partial product, its least significant digit is added starting at the next least significant digit of the partial product address.

At the end of the status level ROM high, with the occurrence of the eighth delayed timing pulse T8a, four cases may be distinguished.

First the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is set and the nines counter 45 (FIG. 1(f-a)) does not have a count of nine. In this case the status transition gate 1265 (FIG. 1G) passes the pulse T8a to cause the status level RO to be high. Note that the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is set only if one or more additions have been completed. The next multiplier digit has therefore been read out. If this next multiplier digit is not a space or item separation symbol, the multiplicand must now be added to the partial product a number of times equal to the multiplier digit. This repeated addition is accomplished by another sequence of high status levels RO and RI and then RN until the nines counter 45 again equals nine. When the nines counter 45 count again equals nine, the multiplicand has been added to the partial product a number of times equal to the multiplier. Accordingly, another multiplier digit is read out in the ROM level, as just explained. This RO-RI-RN-ROM sequence is repeated until a multiplier digit is found when the status level ROM is high which is a space or item separation symbol.

Second, if the SPR lead or ISSR lead is high, and the status level ROM is high, indicating that the new multi-

plier digit is a space or item separation symbol, the multiplication is complete. The status transition gate 1206 (FIG. 1H) passes the eighth delayed timing pulse T8a to cause the status level IC to be high.

Third, if the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is reset, and the multiplier digit read out is not a space or ISS, the first addition of the current multiplier remains to be accomplished. The status transition gate 1251 (FIG. 1G) passes the eighth delayed timing pulse T8a to cause the status level RI to become high.

The fourth case which may arise at the end of the sequence with the high status level ROM, is that the next multiplier digit is a zero. If the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is set, indicating that this is not the first multiplier digit, and the nines counter 45 (FIG. 1(f-a)) count is nine, (indicating a complemented zero) then the status transition gate 1224 (FIG. 1H) passes the eighth delayed timing pulse T8a to the "set RD" lead. The high status level RD follows. The high status level RD operation is considered next.

5.3.2.8 Status Level RD High

The least significant digit of the partial product in this case (or the least significant digit to which the address counter, C counter 12, has shifted in addressing the partial product) is now to be read out of the right HSM 16. If a space is read out, the space must be replaced by a zero. If the character is not a space, but a digit, the digit must be read back, unchanged, into the right HSM 16.

T1

At the first timing pulse T1 the right HSM 16 (FIG. 1(d-c)) is addressed by the C counter 12 (FIG. 1(c-b)) through the gates 660 as in the high status level RO or RI.

The read-out circuits for the right HSM 16 (FIG. 1(d-c)) are activated through the gate 863.

T6

The least significant character of the active partial product is read from the right HSM 16 (FIG. 1(d-c)) into the Z register 14 (FIG. 1(d-d)), through the gates 1032 primed by the gate 1030. Note that the end of operand right flip-flop F1010 (FIG. 1(d-e)) is reset because with status level RD high the last character was not of the "end of operand" type.

T8

If the character now in the Z register 14 (FIG. 1(d-d)) is a space, the SPR lead (FIG. 1(d-e)) is high, and the gate 1069 (FIG. 1(d-d)) passes the eighth timing pulse T8 to reset the Z register 14. If the character in the Z register 14 (FIG. 1(d-d)) is not a space, the Z register 14 is not reset.

If the partial product character in the Z register 14 is not a zero and not a space, the status transition gate 1250 (FIG. 1G) passes the eighth delayed timing pulse T8a to select the status level RI to be high, and the character is added to the contents of the now reset Y register 13, which is therefore effectively zero, for storage again without change in the right HSM 16 (FIG. 1(d-c)).

Recall that if one or more zeroes have been found as the first least significant digits of the multiplier, zeroes are read into the memory address for the sum, as previously explained. However, after a multiplier digit other than zero has been located, the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is set, and the partial product sum is preserved by adding and entering the sum. If the partial product digit is a space character, the sum digit is entered as a numeric zero.

5.3.2.9 Status Level ROM High Again

As noted above, after the completion of the RN-RO-RI-RN sequences, the status transition gate 1240 (FIG. 1) passes the eighth delayed timing pulse T8a to cause the status level ROM to be selected as high. The action of the machine with the status level ROM (FIG. 1H) high

is now as described above. Note, however, that if the "been in RN" flip-flop F1111 is in its reset condition, at the eighth delayed timing pulse T8a, the status transition gate 1251 (FIG. 1G) is actuated to cause the selection of the status level RI to be high. The first addition (other than for one or more initial zeroes of the multiplier) of the multiplicand and the partial product then begins. If however, the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is set, the status transition gate 1256 (FIG. 1G) causes the status level RO to be high, and the partial product digit is read out of the right HSM 16, so that the partial product is preserved in the ensuing additions.

In this connection, note that the gate 1138 (FIG. 1(e-a)), the output of which "sets" the "been in RN" flip-flop F1111 (FIG. 1(e-a)), and the status transition gate 1237 (FIG. 1H) receive the same priming, or enabling voltages, except for the timing pulses, the former gate 1138 receiving the eighth timing pulse T8, and the latter gate 1237 the eighth delayed timing pulse T8a. Thus, the "been in RN" flip-flop F1111 is set if and only if the status level RN has been selected as high (as an enabling voltage) in the course of the multiplication, because the "logic" for setting this flip-flop is the same as for selecting the status level RN. The sequence of the status levels is therefore modified depending on the selection or non-selection of a previous status level in the course of the multiplication operation.

In other operations, or sequences of status levels, a similar modification may be secured. For example, in the operation read-in from tape, the before first RE flip-flop F705 (FIG. 1(b-b)) performs a similar role. The sequence of status levels is modified depending on whether the status level RE was formerly selected in the course of the operation (see sec. 5.7). Other examples may be found herein. Note also the after first RE flip-flop F703 (FIG. 1(b-b)).

However, not only may such a bistable circuit be used to modify the sequence of status levels. Also modified is the effect of the status level on the flow of information. For example, the gate 837 (FIG. 1(e-b)) is closed when the "been in RN" flip-flop F1111 is set, whether the other enabling voltages applied thereto are high or not. In a way, these flip-flops change the mode of operation or mode of response during a status level. Hence, these are termed change of mode flip-flops. In effect, the change of mode flip-flops are an important feature and provide still another set of levels for control of the computer. Thus such a flip-flop may provide an additional sub-operation which otherwise might employ an additional status level. Hence an equipment saving is effected, and more flexible operation secured.

Another example of a change of mode flip-flop is the one cycle flip-flop F1102 (FIG. 1(f-e)). It will be recalled that the gates into two of the previous result flip-flops are open by the "one" output of this one cycle flip-flop only when the one cycle flip-flop is set. Thus the information flow is modified by this change of mode flip-flop without a modification of the status level sequence during that cycle. Note that this one cycle flip-flop is reset after the first cycle of RI.

Other examples of change of mode flip-flops may be found, such as the first EM or ET flip-flop F706 (FIG. 1(b-e)). In each case, the change of mode flip-flop assumes one state on the occurrence of a contingency in the course of an operation and modifies the flow of the information either by its effect on the program control circuits, or by its effect on the status transition gates, or both.

5.3.2.10 Status Level RI High With a Zero Multiplier Digit After a Non-Zero Multiplier Digit

In the following steps under the status level RI, the contents of the Z register 14 (FIG. 1(d-d)) are read through the adder and BCDC 17 back into the right HSM 16 (FIG.

1(d-c)) at the address of the then least significant digit of the partial product. The contents of the Y register 13 (FIG. 1(c-d)) are zero, as the Y register 13 was reset in the last status level.

At the first timing pulse T1, the L register 18 (FIG. 1(f-c)) and R register 19 (FIG. 1(d-c)) are reset by a pulse from the gate 860 (FIG. 1(e-c)).

The right HSM 16 (FIG. 1(d-c)) is addressed by the C counter 12 (FIG. 1(c-b)) at the location of the then least significant digit of the partial product through the gates 660 primed by the gate 696 (FIG. 1(c-c)).

To this point, the operation is the same as for the first multiplier character a zero when status level RI is high.

The output of the adder is passed into the R register 19 through the gates 841 (FIG. 1(e-b)) primed by the "been in RN" flip-flop F1111 (FIG. 1(e-a)) "one" output. Note that in the current operation this last mentioned flip-flop is set. If the character is a zero, the 2⁴ bit flip-flop in the R register 19 (FIG. 1(d-c)) is set through the gate 872 (FIG. 1(e-b)), also primed by the "been in RN" flip-flop F1111 "one" output, now high.

The right HSM 16 (FIG. 1(d-c)) is in condition to receive information by reason of a high level from the right read-in gate 850 activating the write-in circuits. Note that status level RI primes the gate 850.

At the eighth delayed timing pulse T8a, the status transition gate 1239 (FIG. 1H) causes the status level ROM to be selected high.

5.3.2.11 Completion

As already pointed out, if any multiplier character is a space or item separation symbol, during the time that the status level ROM is high, the space or item separation symbol character is applied to the Z register 14 (FIG. 1(d-d)). The right symbol recognition circuits 23 detect the presence of the space or item separation symbol in the Z register 14, (FIG. 1(d-d)) as already described. Accordingly, the item separation symbol right lead ISSR or the space-right lead SPR applied through a suitable "or" circuit, cause the status transition gate 1206 (FIG. 1H) to be primed. Accordingly, at the eighth delayed timing pulse T8a, the status transition gate 1206 applies to the "set IC" lead the eighth delayed timing pulse T8a. Therefore the status level IC is selected to be high. The instruction is complete because the multiplier characters have now been exhausted.

An ISS may be detected in the left symbol recognition circuits 22, or in the right symbol recognition circuits 23. Note that the ISSL lead and the ISSR lead are applied through a suitable "or" circuit to the input of the gate 1106 (FIG. 1(f-d)). During the RS cycle while the status level RS is high, and before a multiplier or a multiplicand digit is found, the occurrence of the ISSR item separation symbol in the Y or Z registers 13 or 14, indicates that there is no multiplier or multiplicand, as the case may be, to be multiplied. Therefore during the high status level RS at the eighth timing pulse T8, the output of the gate 1106 sets the previous result zero flip-flop F1101. The action which may follow the setting of the previous result flip-flop F1110 in multiplication is explained hereinafter, in connection with the conditional transfer of control operation, with operation level C high.

5.3.3 Sequence of Status Levels

With reference to the flow diagram FIG. 14, the instruction is staticized during the successive status levels RO01, RO02, and RO03. After the RO03 cycle, the status level RS is selected to be high. The machine searches for the least significant digit of both the multiplier and the multiplicand. The number of RS cycles depends on the operand having the greatest number of spaces in the least significant locations of the operand. When the least significant non-space character of each operand has been found, there are two possible conditions:

(a) If the least significant character of either operand is an item separation symbol, the machine selects the status level IC (instruction complete).

(b) If the least significant character of both operands is not ISS and not space, the machine selects the status level RI to be high.

The purpose of the initial RI-RO sequences which follow is to place the multiplicand in the partial product location. The multiplicand is added to zero. Note that the RI sequence is entered after RS only if both the multiplier and multiplicand have non-zero decimal values.

Status Level RI High

The entire partial product, or the contents of the right HSM 16 at the address C, at this point should consist of space characters. The least significant digit of the multiplicand is added to the least significant character of the partial product, the latter being a zero. The result is stored in the least significant HSM location of the partial product. The stored digit is the least significant digit of the multiplicand. However, in the process of this first RI, if the machine recognizes that the multiplier is a zero, a special condition occurs. If the least significant digit of the multiplier is a zero, all that need be done is enter a zero at the location of the least significant digit of the partial product. Then the address is shifted so that the new least significant digit of the partial product is addressed next to the previous least significant digit or the zero just entered. In effect, the partial product is shifted to the right (multiplied by ten). The nines counter 45 has a nines count because the complemented zero multiplier digit is entered therein. The status level ROM now becomes high and a new multiplier digit is read out. The new digit is treated as the first.

If this special case does not occur, that is, when a non-zero multiplier digit is read out, then the machine goes from the high status level RI to the high status level RO.

RO Level High

The next least significant digit of the multiplicand and the next least significant character of the partial product are read out of the HSM. The machine then selects status level RI to be high, as before.

RI Level High

The succeeding least significant digit of the multiplicand and the succeeding least significant digit of the partial product are added and the result (the second least significant digit of the multiplicand) is placed in the second least significant HSM location of the partial product.

The machine then continues from RI to RO back to RI etc., until the end of the multiplicand is read out of the HSM. The machine then selects the status level RN to be high.

Status Level RN High

The nines counter 45 which has been set with the complement of the multiplier has one added to it. The multiplicand is now to be read out again digit by digit and added to the corresponding digits of the partial product in the succeeding RO-RI cycles. The A and C counters 10 and 12 are reset to the original addresses of the least significant digits of the multiplicand and partial product, temporarily stored in the A and C registers 26 and 28 respectively.

If the nines counter 45 count is not nine, then the multiplicand has not been added to itself the number of times required by the multiplier. Therefore the machine selects the RO level to be high.

Status Level RO High

The least significant digits of the multiplicand and of the partial product are read out of the HSM. The machine selects the level RI to be high.

Status Level RI High

The least significant digits of the multiplicand and of the partial product are added and the sum digit placed in the least significant HSM location of the partial product. The previous partial product digit is then no longer stored at this location. The machine selects RO.

The machine then continues in a reiterated or repeated RO-RI sequence until the end of both operands (multiplicand the partial product are reached). The machine then selects the status level RN to be high again as pointed out above.

Status Level RN High

The nines counter 45 count has one added to it. If the nines counter 45 has not yet reached nine, the previously described RN-(RO-RI) sequence is repeated. If, however, the nines counter 45 has reached nine, then the multiplicand has been added to itself the number of times specified by the least significant digit of the multiplier. The machine then selects ROM to read out the second least significant digit of the multiplier.

The next least significant digit of the multiplier is read out in a high status level ROM.

Status Level ROM High

In ROM, the next least significant multiplier digit, which may be considered the now least significant multiplier digit, is taken from the HSM, complemented, and the nines counter 45 set in accordance with the complement.

The next least significant digit of the original partial product is considered as the new, or now least significant digit, of the partial product. In effect the partial product is shifted. The least significant digit of the original partial product is no longer used in the additions because its value has become fixed. Therefore, the least significant digit of the final product is stored in the machine. The machine then selects the status level RO to be high.

The (RO-RI)-RN sequence previously described is now repeated, until the machine again selects the high status level ROM, and the third least significant multiplier digit is read out of the HSM, complemented, and the complement set into the nines counter 45, etc.

The general flow of status levels according to the flow diagram of FIG. 14 then continues until, instead of a multiplier digit being read out of the HSM in the high status level ROM, a space or ISS (end of operand character) is read out. The status level IC then becomes high.

5.3.4 Zeroes in the Multiplier

Zeroes in the multiplier are handled in a rather special form. There are two possibilities, reviewed as follows:

(a) The least significant digit or digits of the multiplier are zero.

(b) A zero first appears after a less significant character or characters of the multiplier is a non-zero.

For example:

(a) multiplier .2350- - or .23500- -

(b) multiplier .2035- -

Case A—Zero Appearing As Least Significant Digit of the Multiplier

Case A.—If a zero is recognized as a least significant digit of the multiplier, the machine selects status level RI to be high, and a zero is placed in the location of the least significant digit of the partial product. The machine then selects the status level ROM to be high. The second least significant multiplier digit is read out of the HSM. If the second multiplier digit is a non-zero digit, it is complemented, and sets the nines counter 45 to the complement. The address of the partial product to be stored is suitably shifted. The multiplier digit is cleared from its register and the status level RI is selected to be high.

The least significant digit of the multiplicand read out of the HSM in the previous status level RS high is added to the second least significant digit of the partial product (after the shift). The character in the partial product location of the second significant digit is a space, since the only digit in the entire partial product address is the zero in the original least significant HSM location of the partial product. The space character is treated as a zero through the use of the contents of the cleared register mentioned in the high status level ROM. The sum is placed in the partial product address and the operation is continued as in the general case.

If the second multiplier digit is also a zero, the previous RI status level high operation for a zero multiplier is again followed, and a zero is artificially placed in the second least significant location of the partial product. The machine again selects ROM, etc.

Case B—Zero Appears in The Multiplier After a Non-Zero Digit

The status level ROM is high. A zero is read out of the HSM, in status level ROM, complemented, then placed in the nines counter 45. As one or more less significant multiplier digits were non-zero, the "been in RN" flip-flop F1111 (FIG. 1(e-a)) is set, and the machine enters the high status level RD. The digit formerly stored in the partial product is read out. The least significant partial product digit associated with the current multiplier is read out of the HSM. The machine then selects RI.

In the next status level RI high period, if the character read out of the partial product address is a space, then a zero is written back into the HSM at the same location the space was taken from. If the character read out of the partial product address is a decimal digit, then the same digit is added to the artificial zero and read back into the HSM location from which it was taken. The machine then selects the status level ROM to be high. In effect, the same partial product has been reentered at its same address, and the effective shift is ready to be accomplished.

The status level ROM is now high, and the next multiplier digit is read out of the HSM, complemented, and stored in the nines counter 45. The partial product is effectively shifted (by change of the C address), and if the new multiplier digit is non-zero, the machine selects the high status level RO and proceeds as already described.

5.4 Binary Subtraction, Right Hand Justification (Operation R) Operation Level R High

Provision is made for binary subtraction with right hand justification. In this binary subtraction process, the six significant bits of a number or character in the binary code are considered as a binary number, without the parity bit. The significant binary digits of succeeding characters of the same item are considered the succeeding digits of the same binary number. The two items may be subtracted one from the other, considered as two binary numbers. The term right hand justification is employed because the significant bits of each item are aligned according to their binary order, from the least significant bit of the least significant character on up. This alignment corresponds to right hand justification in printing or writing the number in the usual English order, with the zero order digits aligned at the right.

5.4.1 Description of Additional Components

In addition to the components thus far described, certain additional components are employed for the operation of binary subtraction with right hand justification. A set of six gates 1044 (FIG. 1(c-d)) are provided connected respectively to the six "zero" output terminals of the Z register 14 (FIG. 1(d-d-)). The output of the gates 1044 (FIG. 1(c-d)) is applied through suitable "or" circuits to the inputs of the gates 21 (FIG. 1(e-a)). Note

that the parity bit is not passed by these gates. The gates 1044 (FIG. 1(c-d)) are primed by either one of the high operation levels R (for binary subtraction right-hand justification) and L (binary subtraction left-hand justification) applied through a suitable "or" circuit. The binary complement with respect to the binary number 1000000 is thus taken.

A three-input gate 1138 (FIG. 1(f-c)), is provided. The gate 1138 is primed at one input by either one of the high operation levels R or L. The gate 1138 is also primed at a second input from the high status level RO03. The third input to the gate 1138 is from the first timing pulse T1. The output of the gate 1138 is passed through an "or" circuit to the set terminal S of the carry flip-flop F2 (FIG. 1(f-b)). Accordingly, in either one of the high operation levels R or L, the carry flip-flop F2 is set during the staticizing of the instruction. Thus for binary subtraction of either kind, an end around carry is always provided.

A set of six, two-input gates 809 (FIG. 1(f-e)) are provided each of which are primed at one input by any one of three high operation levels B (for binary addition), L, or R. The gates 809 are connected between the respective outputs of the duplicated adders 17A (FIG. 1(e-b)) at their second input, and the respective inputs to the register L register 18 and R register 19 (FIGS. 1(b-c) and 1(d-c)).

The output of the duplicated adders 17A is connected through a six input "or" circuit 64 (FIG. 1(a-e)) designated "not all zero" (distinguish from the "zero" circuits), so that the lead designated "not all zero" is at a high level if any one of the outputs of the duplicated adder 17A is a "one," and is at a low level only if all are "zero" or at a low level. The "not all zero" lead is applied to an inverter I and then to a three-input gate 1110 (FIG. 1(f-e)). Accordingly, the input to the gate 1110 from this inverter I19 may be considered an "all zero" lead. The "all zero" lead being high is an indication that each and every one of the outputs from the duplicated adder 17A is a binary zero. The gate 1110 is primed at a second input by either one of the high operation levels R, or L. The second timing pulse T2 is applied as the third input to the gate 1110. The output of the gate 1110 passes through a suitable "or" circuit, which receives also the output of the gate 1119, to a gate 1105 (FIG. 1(f-d)), previously described.

The "not all zero" lead mentioned heretofore is also applied to a two-input gate 1104 (FIG. 1(f-e)). The gate 1104 is also primed at its second input by either one of the high operation levels R, or L. The output of the gate 1104 is applied through a suitable "or" circuit to the reset terminal R of the previous results zero flip-flop F1101 (FIG. 1(f-d)).

Note the three-input gate 1137 (FIG. 1(f-e)), which is primed by the high status level RO03, and by a "not C" input, and receives the sixth timing pulse T6.

A five-input gate 1120 (FIG. 1(f-d)) is provided. One input of the gate 1120 is primed by either one of the high operation levels R, or L. A second input is primed by the high status level RI. The gate 1120 is primed at a third input by the high "one" output terminal of the EOBO flip-flop F1110 (FIG. 1(f-c)). A fourth input to the gate 1120 (FIG. 1(f-d)) is from the "zero" output of the carry flip-flop F2 (FIG. 1(f-b)). The fifth input to the gate 1120 is the eighth timing pulse T8. The output of the gate 1120 is applied to the set terminal S of the previous result negative flip-flop F1109 (FIG. 1(f-d)).

A two-input gate 1118 is provided receiving at one input the output of an "or" circuit to which are applied the operation levels B, L, and R. The output of the gate 1118 is applied through an "or" circuit to set the second bit (2¹ bit) flip-flop of the adder output register 62, only (and not the other stages).

A parity regenerator 44 (FIG. 1(b-d)) is more fully described hereinafter.

A gate 499 (FIG. 1(e-c)) is provided to receive the output of the gate 948 (FIG. 1(e-d)). Note that the output of gate 948 is therefore received by the gate 949 as well as by set terminal S of the EOBO flip-flop F1110 (FIG. 1(f-c)). The gate 949 (FIG. 1(e-c)) is primed by any one of the three operation levels L, B, or R which may be high. The output of the gate 499 is applied to the set terminal of the 2¹¹ bit of the C register 28.

A four input status transition gate 1201 is provided. One input is from any one of the high operation levels B, L, or R. A second is from the high status level RI. A third is from the "one" output terminal of the EOBO flip-flop F1110 (FIG. 1(f-c)). The fourth input to status transition gate 1201 (FIG. 1H) is from the eighth delayed timing pulse T8a. The output of the status transition gate 1201 is applied through "or" circuits to the "set IC" lead.

5.4.2 Machine Operation—Binary Subtraction, Right Hand Justification

The instruction is staticized in the usual manner in the high status levels RO01, RO02, and RO03, as follows:

O Register	A Address	B Address	C Address
Code for Operation B-----	Address of Minuend.	Address of Subtrahend.	Result Address.

At the eighth delayed timing pulse T8a with the status level RO03 high and the operation level R high, the status transition gate 1234 (FIG. 1H) applied the eighth delayed timing pulse T8a to the "set RS" lead.

5.4.2.1 Status Level RS High

The status level RS is now high. The operation is the same as for decimal addition, with the high status level RS.

After the least significant digits are located in both the left and right HSM's 15 and 16, the status transition gate 1255 (FIG. 1G) passes the eighth delayed timing pulse T8a to the set RI lead.

5.4.2.2 First Status Level RI High

The status level RI is now high. The gate 698 (FIG. 1(c-b)) passes the first timing pulse T1 to prime the gates 650 or the gate 694 passes the first timing pulse T1 to prime the gates 660, respectively, in accordance with whether the 2⁹ bit flip-flop of the C register 28 is in its reset or set condition.

Note that in the last RS cycle the least significant character of the minuend and subtrahend respectively are stored in the Y and Z registers 13 and 14 (FIGS. 1(c-d) and 1(d-d)) respectively.

T1-T3½

The least significant character of the minuend is transferred from the Y register 13 (FIG. 1(c-d)) through the adder input gates G27 (FIG. 1(e-a)) during the interval between the first timing pulse T1 and the timing pulse T3½, during which interval the adder input flip-flop F3 is in the set condition.

The least significant character of the subtrahend is taken from the "zero" terminals of the Z register 14 (FIG. 1(d-d)) through the gates 1044 (FIG. 1(c-d)) and then through the adder input gates G21 (FIG. 1(e-a)) also primed by the adder input flip-flop F3 in the interval between timing pulse T1 and timing pulse T3½. Note that the input to the adder is taken from the "zero" terminals of the Z register 14, thus complementing the subtrahend with respect to a binary number $2^6 - 1 = 63$.

The "carry" from the carry flip-flop F2 (FIG. 1(f-b)) is applied through the gate G12 (FIG. 1(e-a)) to the

duplicated adder 17A (FIG. 1(e-b)), thus providing the end-around-carry. Note that the gate G12 (FIG. 1(e-a)) is also primed by the adder input flip-flop F3. Note also that when the least significant character is subtracted, that the character flip-flop F2 is in its set condition, because of the application of the first timing pulse T1 during the last high status level RO03 applied through gate 1138. Accordingly, the carry is provided for the binary operation corresponding to the carry in "tens complement" or end-around carry in decimal subtraction. Thereafter, a carry, if any, is sent forward only in the subsequent RI high status levels for binary subtraction, to propagate properly.

The output of the gate 1118 (FIG. 1(f-c)) insures that the 2^1 bit flip-flop of the adder output register 62 is set. Therefore, the adder output register 62 contents cannot be a nine and cannot be a zero. Thus the "not zero" lead from inverter 115 (FIG. 1(f-c)) and FIG. 1(f-d)) and the output from the gate 1116 (FIG. 1(f-d)) are both high. The gates 1111 and 1116 are primed. The gates 1126, and 1117 cannot have an output. Thus the previous result all nines flip-flop F1103 cannot be set. The gate 1105, for the previous result zero flip-flop F1101, can be primed only by the output of the gate 1110. Note that the previous result negative flip-flop F1109 can be set, in operations R or L, only by the output of the gate 1120.

The proper restoration of the parity bit in operations L, B, or R is taken care of by the parity regeneration circuit 44 (FIG. 1(b-d)). This circuit 44 is similar to, but not the same as, the parity generator heretofore described in connection with the 2^6 gate of the gates 841 (FIG. 1(e-b)) in addition (sec. 5.1.2, T1½-T3). The parity regeneration is described in greater detail herein after (sec. 5.4.2.7).

Between timing pulses T1½ and T3, the adder output flip-flop F4 (FIG. 1(e-c)) gates the output of the duplicated adders 17A to pass to the gates 809 (FIG. 1(f-e)). The output of the gates 809 passes to the L register 18 (FIG. 1(b-c)) and the R register 19 (FIG. 1(d-c)). Thus the result of the subtraction of the subtrahend and from the minuend is stored in each of the L and R registers 18 and 19.

T4

At the fourth timing pulse T4, the Z register 14 (FIG. 1(d-d)) is reset by the output of the gate 1043 passed through the delay circuit D56. The Y register 13 (FIG. 1(c-d)) is reset by the fourth timing pulse T4 passing through the gate 901 (FIG. 1(b-d)).

T5

At the fifth timing pulse T5, one of the read-in gates 721 (FIG. 1(c-c)) and 850 (FIG. 1(d-c)) are primed, depending respectively on whether the 2^9 bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset or set condition.

The status transition gate 1263 (FIG. 1G) passes the eighth delayed timing pulse T8a to the "set RO" lead. Accordingly, the status level RO is now high.

5.4.2.3 Succeeding High Status Levels RO-RI

The second least significant characters of the minuend and subtrahend are now read out of the left HSM 15 and the right HSM 16, into the Y and Z registers 13 and 14 respectively, as in operation L.

The machine then selects RI to be a high status level. The second least significant characters of the operands and the carry (if one exists) from the previous high status level RI are added and read into the HSM 15, 16.

The machine continues in a reiterated RO-RI sequence until the ends of both operands are detected.

5.4.2.4 Special Cases

Two special cases may be considered before describing the operation when the end of both operands is reached.

In the first of these cases, the end of only one operand, namely the subtrahend, occurs. The end of the subtrahend operand may be an item separation symbol ISS or a space symbol. Either the space symbol or ISS is to be subtracted from a binary character in the minuend as a zero. Note that the end of operand right flip-flop F1010 (FIG. 1(d-e)) is set by virtue of the gate 1065 (FIG. 1(e-d)) passing the eighth timing pulse T8. The gate 1065 is opened or primed by the SPR lead from the right recognition circuits 23. If the symbol in the subtrahend is an item separation symbol, then the gate 1068 (FIG. 1(e-d)) passes the eighth timing pulse T8 to set the end of operand right flip-flop F1010 (FIG. 1(d-e)). Whichever gate, 1065 or 1068 (FIG. 1(e-d)) passes the eighth timing pulse T8, the eighth timing pulse T8, in addition to setting the end of operand right flip-flop F1010, is also applied through the delay circuit D56 (FIG. 1(d-d)) to reset the Z register 14. Therefore, the input to the adder 17A (FIG. 1(e-b)) from the "zero" terminals of the Z register 14 are all high. However, adding all binary "ones" in all six places of the six digit binary number, is equivalent to subtracting zero.

Note that the end-around carry which may have to be taken care of, is always taken care of in advance by the flip-flop F2 (FIG. 1(f-b)) due to its having been set by the first timing pulse T1 in the previous high status level RO03 as mentioned above. The end-around carry is to propagate through the binary digits of successive characters, and any subsequent carry is staticized through flip-flops F1 and F2 (FIG. 1(f-b)). Note that the sixth bit carry output as well as the six bit sum output (FIG. 1(e-b)) from the duplicated adder 17A by-passes the binary to coded-decimal converter 17B. This sixth bit carry output passes through a suitable "or" circuit to the set terminal of flip-flop F1 (FIG. 1(f-b)). The sixth timing pulse T6 is then passed through the gate G8 (primed by the "one" terminal of the flip-flop F1) in the high status level RI to set the carry flip-flop F2. The set condition of the carry flip-flop F2 is then available as the carry for the duplicated adder 17A on the next high status level RI, the carry being reset only at the fourth timing pulse T4 of the high status level RI, after the new addition, and the set impulse being applied at the sixth timing pulse T6 with the high status level RI provided the flip-flop F1 again is set.

In the second special case, the end of operand of the minuend only is reached. The ISSL flip-flop F910 (FIG. 1(c-e)) is therefore set, by the eighth timing pulse T8 passed through the gate 941 (FIG. 1(b-e)) and thence through the gate 937 (FIG. 1(c-e)) primed by the high ISSL lead; or the space left flip-flop F911 (FIG. 1(c-e)) is set by the eighth timing pulse T8 from the gate 938. Therefore, the input of the inverter 17 (FIG. 1(c-e)) is high and its output low. The gates G27 (FIG. 1(e-a)) are inhibited, that is, closed and prevent the passage of information. Accordingly, all low levels are passed into the adder 17A, that is, the equivalent of a zero is added from the minuend.

Note that if the subtrahend is greater than the minuend in binary subtraction, there is an error in the result. However, the result itself need not be used, so far as the present machine is concerned, except to secure an indication that the result is negative and that the subtrahend is greater than the minuend.

5.4.2.5 End of Both Operands

Returning now to the end of both operands, note that the end of the operands can be either a space or an item separation symbol. If a space is stored in the Y register 13, the left symbol recognition circuits 22 cause one of the ISSL flip-flop F910 (FIG. 1(c-e)) and one of the SPL flip-flop F911 (FIG. 1(c-e)) to be set, in the manner just described. If either the ISSL flip-flop or the space-left flip-flop F911 is in its set condition, one of the inputs

to the gate 948 (FIG. 1(e-d)) is primed, as noted in connection with addition.

If a space appears in the Z register 14, the right symbol recognition circuits 23 cause the gate 1065 (FIG. 1(e-d)) to pass the eighth timing pulse T8 to set the end of operand right flip-flop F1010 (FIG. 1(d-e)). If the item separation symbol (ISS) is found in the Z register 14, the right symbol recognition circuits 23 cause the ISSR lead to be high. The gate 1068 (FIG. 1(e-d)) is then primed to pass the eighth timing pulse T8 to set the end of operand right flip-flop F1010 (FIG. 1(d-e)). The gate 948 (FIG. 1(e-d)) is also primed by the high "one" output of the end of operand right flip-flop F1010 (FIG. 1(d-e)).

Accordingly, at the selection of the status level RI to be high following the last RO cycle, the gate 948 is primed to pass the first timing pulse T1 to set the EOBO flip-flop F1110 (FIG. 1(f-c)).

Accordingly, in the high status level RI, after the end of both operands has been reached, the first timing pulse T1 is passed through the gate 948 (FIG. 1(e-d)) and in addition to setting the EOBO flip-flop F1110 (FIG. 1(f-c)) is passed through the gate 499 (FIG. 1(e-c)) to set the 2¹¹ bit of the C register 28 (FIG. 1(c-a)).

However, the "zero" output of the 2¹¹ bit flip-flop of the C register 28 is applied through that "or" circuit (see FIG. 1(b-c)) to which is also applied the operation level P to the left read-in gate 721 (FIG. 1(c-c)). Similarly, the zero output of the 2¹¹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is applied through that "or" circuit having another input from the operation level P, to prime the right read-in gate 850 (FIG. 1(d-c)). Accordingly, with the 2¹¹ bit flip-flop of the C register 28 set, the gates 721 are closed, as a result of which the left HSM 15 and the right HSM 16 have their respective "write-in" circuits inactivated. Therefore, the HSM 15, 16 cannot receive information. The input to the HSM 15, 16 is blocked. Any carry (if there is one) from the addition of the most significant character of the minuend and the complemented subtrahend is therefore discarded at this point. However, no numerical accuracy is sought in binary subtraction with right hand justification.

5.4.2.6 Condition of Previous Result Flip-Flops

In addition to storing the difference in the HSM 15, 16 for future use, the nature of the difference is "staticized." That is, whether the difference is positive, zero, or negative determines the state of the previous results flip-flops 47 (FIG. 1(f-d)).

At the staticizing of the instruction L, or R, or A, or S, when the status level RO03 is high, the first timing pulse T1 is passed through the gate 1107 to set the one cycle flip-flop F1102 (FIG. 1(f-e)). If the result of the first addition is zero, the gate 1110 is primed by the "all zero" lead (FIG. 1(f-e)), the second timing pulse T2 is passed through the gate 1110 and applied to the gate 1105 (FIG. 1(f-d)). The gate 1105 is primed by the "one" output of the one cycle flip-flop F1102. The gate 1110 (FIG. 1(f-e)) passes the second timing pulse T2 to the primed gate 1105 (FIG. 1(f-d)) through which the previous result all zero flip-flop F1101 is set. Hence, if the results are all zeroes, the previous result zero flip-flop F1101 is in the set condition at the end of the addition. If not, note that the gate 1104 (FIG. 1(f-e)) passes a high level during the time the duplicate adder 17A (FIG. 1(e-b)) is being gated open. The high level from gate 1104 then resets the previous result zero flip-flop F1101 (FIG. 1(f-d)). Therefore, if any succeeding digit of the sum of the minuend and complemented subtrahend fails to have six zero bits, the gate 1104 (FIG. 1(f-e)) passes the high level from the "not all zero" lead, and the previous result zero flip-flop F1101. The resetting of the previous result zero flip-flop F1101 (FIG. 1(f-d)) then indicates that the answer is something other than all zero.

The previous result negative flip-flop F1109 (FIG.

1(f-d)) is reset when the instruction is staticized by the passage of the timing pulse T6 through the gate 1137 (FIG. 1(f-e)). When the end of both operands is reached, the EOBO flip-flop F1110 (FIG. 1(f-c)) is set. If there is also no carry, the carry flip-flop F2 is in the reset condition, the gate 1120 (FIG. 1(f-d)) is also primed. In the last high status level RI, the gate 1120 then passes the eighth timing pulse T8 to the set terminal of the previous result negative flip-flop F1109. With the previous result negative flip-flop F1109 (FIG. 1(f-d)) in the set condition, and the previous result zero flip-flop F1101 (FIG. 1(f-d)) in the reset condition, the state of the circuit shows that the result was negative.

Observe that in binary subtraction, the absence of the last carry (when end of both operands is reached) indicates a negative result.

The condition of the previous result flip-flops in binary subtraction, may be tabulated as follows (the previous result all nines flip-flop F1103 is always reset):

TABULATION

Subtract Item B from Item A	Carry	Result	Cond. of flip-flop	
			PRZ F1101	PRN F1109
If A > B.....	(1)	not 0	reset.....	reset.....
A = B.....	(1)	0	set.....	reset.....
A < B.....	0	not 0	reset.....	set.....

The status transition gate 1201 (FIG. 1H) passes the eighth delayed timing pulse T8a, at the end of the operation, to cause the status level IC to be high.

5.4.2.7 Parity Regeneration

As noted above, the proper restoration of the parity bit in operations L, B, or R is taken care of by the parity regeneration circuit 44 (FIG. 1(b-d)). This circuit is similar to, but not the same one as, the parity generator heretofore described in connection with the 2⁶ gate of gates 841 (FIG. 1(e-b) in addition).

A gate 751 (FIG. 1(b-d)) in the parity regenerator 44 has applied to it through suitable "or" circuits the operation levels L, B, or R. The second input to the gate 751 is the fourth timing pulse T4. Accordingly, at any one of the high status levels L, B, or R, the gate 751 is primed to pass the fourth timing pulse T4. The fourth timing pulse T4 thus passed through the gate 751 is applied to a set of gates 740 connected together as a parity regenerator. The gates 743 are primed by the high status level RI. Also applied to the gates 743 are the six bits coming from the L register 18 (FIG. 1(b-c)). The gates 743 (FIG. 1(b-d)) are connected in such a fashion that if the sum of the six bits is even, the output of the gates 743 is a low level; if the sum of the six bit output of the L register 18 is odd, then the output of the parity regenerator gates 743 is at a high level. The output of the parity regenerator gates 743 is applied as the 2₆ bit (or the seventh bit or parity bit) of the L and R registers 18 and 19, that is, applied to the set terminal of the 2₆ bit flip-flop of these registers. Accordingly, the "even" parity for the coding of this machine is maintained for characters stored in the internal memory. Note that the corrected sum is stored in the right or left HSM 15 or 16 at the fifth timing pulse T5 after the regeneration.

The parity regeneration is applicable, as just described, in binary subtraction, left or right hand justification, and in binary addition. Therefore, this parity regeneration is not described again.

5.4.3 Sequence of Status Levels

The process of binary subtraction is provided primarily for comparing two items to see which one is the smaller, so that the items may be arranged in alphabetically ascending or descending order. The subtraction is per-

101

formed character by character from right to left. All six binary digits specifying each character are used in the binary subtraction as compared to only four in decimal subtraction. The instruction may be employed for ordering, for changing characters, and for other purposes. Note that in the code employed in the machine the letters of the alphabet are each given a binary number such that the number corresponding to A is less than the number corresponding to B, and so forth. Therefore, when A is subtracted from B or any other letter in the alphabet, the difference is positive. If B is subtracted from A the difference is negative.

In binary subtraction with right hand justification, the space characters to the right of the operands are not considered part of the operand in question. For example, the machine is required to compare and place in ascending order the two words ·JIM and ·JAMES, the former being in the minuend and the latter the subtrahend, i.e. ·JAMES is to be subtracted from ·JIM. The process of subtraction, right hand justification, starts with the least significant character of each item (the first non-space character of each operand) from right to left until the item separation symbol (·) of both operands are reached. In the example just given the result is negative because the subtrahend has more significant characters than the minuend. The result of the subtraction above being negative, the following order results: ·JIM precedes ·JAMES. If a number of significant characters of both operands are the same, the decision as to which item is greater depends on the most significant characters of each operand which are not the same. For example, with the words Lane and Land, the *e* and *d* would determine the order. The example above described is for an arbitrary ordering. A more usual type of problem might be to arrange the following stock numbers in ascending order:

·10B5
·10B651
·10B430

If the items are of unequal length (such as the first and second in the last example given) the item with the most characters will be the largest. If the items are of equal length (such as the second and third in the example last given) the item which is greater numerically or alphabetically will be the largest since the numbers and letters have known weights. The items in ascending order are then arranged as follows:

·10B5
·10B430
·10B651

With reference to the status level flow diagram, FIG. 15, note that in binary subtraction with right hand justification, after the instruction is staticized, there is a search for the least significant digit of both operands, until the least significant digit of both operands is found. The machine then selects the status level RI to be high. Thereafter, if the instruction has not been completed, the status level RO is selected. The status levels RI and RO are then high in sequence until the end of both operands is reached and the status level IC for instruction complete is high.

5.5 Binary Subtraction, Left Hand Justification (Operation L) Operation Level L High

In this operation, a status transition gate 1264 (FIG. 1G) that is described more fully hereinafter is employed.

The instruction is staticized in the operation levels RO01, RO02, and RO03, as follows:

O Section	A Section	B Section	C Section
Code for Operation L.....	Address of Minuend.	Address of Subtrahend.	Address of Difference.

102

During the high status level RO03, the carry flip-flop F2 (FIG. 1(f-b)) is set by the first timing pulse T1 passed through the gate 1133 (FIG. 1(f-c)). The one cycle flip-flop F1102 (FIG. 1(f-e)) is set by the first timing pulse T1 passed by the gate 1107 (FIG. 1(f-e)).

The status transition gate 1264 (FIG. 1H) is provided having three inputs. To one input is applied, through suitable "or" circuits any one of the high operation levels B, L, J, Q, V, or B. A second input to the status transition gate 1264 is from the status level RO03. The third input to the status transition gate 1264 is from the eighth delayed timing pulse T8a.

Accordingly, when the operation level L (binary subtraction left hand justification) is high from the operation matrix, and the status level RO03 is high, the eighth delayed timing pulse T8a is passed to the set RO lead. Accordingly, the status level RO is selected to be high.

Note that no search for least significant digits is employed in this operation. All characters of the item are operated upon, including spaces assigned thereto. However, the operands may be "justified left," before beginning the operation. Also, it is assumed the operands may have the same maximum standard length. The machine may thus operate, if desired, with standard length items. However, if two ISS's are detected, the status level IC follows, because the gate 944 (FIG. 1(d-e)) requires the status level RS to be high in order to pass a reset pulse to the end of operand right flip-flop F1010 or the space left flip-flop F911 (FIG. 1(c-e)).

5.5.1 Status Level RO High

T1

The gate 699 (FIG. 1(c-b)) passes the first timing pulse T1 to prime the gates 640. The address of the least significant character of the minuend is thus transferred from the A counter 10 to the address circuits of the left HSM 15 (FIG. 1(c-c)). The gate 692 (FIG. 1(d-b)) passes the first timing pulse T1 to open the gates 670, thereby to address the right HSM 16 (FIG. 1(d-c)) with the address of the least significant character of the subtrahend from B counter 11 (FIG. 1(d-b)).

T2

The gate 504 (FIG. 1(c-b)) passes the second timing pulse T2 to advance the count of A counter 10, as in addition. Similarly, as in addition, the gate 509 (FIG. 1(d-b)) passes the second timing pulse T2 to advance the count of B counter 11 (FIG. 1(d-b)) by one count.

T5

The left and right read-out gates 730 and 862 respectively pass a high level to actuate the left HSM 15 and the right HSM 16 for reading out (see FIGS. 1(c-c) and 1(d-c)) respectively.

T6

The gate 919 (FIG. 1(c-d)) primed by the "zero" output of the minus L flip-flop F909 (FIG. 1(b-e)) passes the sixth timing pulse T6 to prime the gates 911 (FIG. 1(c-d)). The gates 911 pass the character addressed in the left HSM 15 (FIG. 1(c-c)) to the Y register 13 (FIG. 1(c-d)). Similarly, the "zero" output of the end of operand input flip-flop F1010 (FIG. 1(d-e)) primes the gate 1030 (FIG. 1(c-d)) to pass the sixth timing pulse T6 to prime the gates 1032 (FIG. 1(d-d)). The gates 1030 pass the character addressed in the right HSM 16 (FIG. 1(d-c)) to the Z register 14 (FIG. 1(d-d)). Accordingly, the minuend is transferred into the Y register 13 and the subtrahend is transferred into the Z register 14 from the left HSM 15 and the right HSM 16 respectively.

103

T8a

The status transition gate 1249 (FIG. 1G) passes the eighth delayed timing pulse T8a to the set RI lead. Accordingly, the status level RI is selected to be high.

The RI-RO sequence is now continued until the end of both operands is detected and the status transition gate 1201 (FIG. 1H) passes the eighth delayed timing pulse T8a to the "set IC" lead, and the status level IC is high.

5.5.2 Sequence of Status Levels

The instruction is staticized in the usual manner.

With reference to FIG. 16, the status level flow diagram, the operation now follows the same steps as with the operation R (binary subtraction right hand justification) described above, with the exception that spaces are not recognized as end of operands. The similarly in the operations of L (binary subtraction left hand justification) and R (binary subtraction right hand justification) is apparent by a consideration of the flow diagram of FIG. 16 for the operation L, and a comparison of this flow diagram with that of FIG. 15 for R.

Note that in describing subtraction with left hand justification, it is assumed that the maximum number of characters is the same in each of the two sequence of characters to be compared. In other words, the left hand justification is presumed to have been accomplished, and the subtraction is assumed to have started with the same total number of characters for both items. Thus in comparing the following two sequences of characters:

• JIM and • JAMES

It is assumed that the comparison starts at least in the fifth place to the right from the item separation symbol. There must be at least two space symbols following the character JIM. Note that the subtraction of two space characters leaves zeroes. Also note that a space character in this machine is coded as a binary one and is therefore the lowest in sequence. The actual justifying left of the characters to be compared, in other words, if any, is taken care of by the programmer. However, note that the left justification is a natural result of the manner in which the information is applied to the memories from a tape. The items are written in the same sequence as though typed or hand written in English, and read out to the memory as written, as will appear more fully hereinafter.

5.6 Binary Addition (Operation B) Operation Level B High

In the binary addition operation, the instruction is staticized in the same manner as in most other operations. When the status level RO03 is high, then status level RO is selected to be high by the eighth delayed timing pulse T8a passing through the status transition gate 1264 (FIG. 1G). The operation is staticized as follows:

O Section	A Section	B Section	C Section
Code for Operation B-----	Address of Augend.	Address of Addend.	Address of Sum.

Note that the status level RS is not high in this operation (compare Operation L, sec. 4.7.5.1). The selection of high status level RS is not required because the addend item is to be added to the entire augend item regardless of the character present in the least significant location in either item.

5.6.1 Status Level RO High

T1

The left HSM 15 (FIG. 1(c-c)) is addressed by the A counter 10 (FIG. 1(c-b)) through the gates 640 (FIG. 1(c-b)) as in decimal addition. The right HSM 16 (FIG. 1(d-c)) is addressed by the B counter 11 (FIG.

104

1(d-b)) through the gates 670 as in decimal addition, during the first timing pulse T1.

T2

At the second timing pulse T2, the A and B counters 10 and 11 are advanced one count respectively by pulses from the gates 504 and 509 respectively, as in decimal addition (see FIGS. 1(c-b) and 1(d-b)).

T4

At the fourth timing pulse T4, the Z register 14 (FIG. 1(d-d)) is reset by a pulse from gate 1043 through delay circuit 56. Note that the gate 1043 is primed from the high "zero" output of the end of operand right flip-flop F1010 (FIG. 1(d-e)). The end of operand flip-flop F1010 has been set in the last previous high status level RO01 by the RO01-T1 reset. The Y register 13 (FIG. 1(c-d)) is reset by the fourth timing pulse T4 from the gate 903 (FIG. 1(b-d)). The gate 903 is primed by the "zero" output of the minus left flip-flop F909 (FIG. 1(c-e)) which is in a reset condition. The minus left flip-flop F909 reset in the last previous high status level RO01 by the first timing pulse T1 passed (as the RO01-T1 reset) through the gate 943 (FIG. 1(d-e)).

T5

The left HSM 15 and the right HSM 16 are placed in condition for read out by the status level applied through the gates 730 and 862 (FIG. 1(c-c)) and 1(d-c)).

T6

At the sixth timing pulse T6, the gates 911 (FIG. 1(c-d)) are primed to read out of the left HSM 15 into the Y register 13 the least significant character of the augend previously addressed in the left HSM 15. The least significant character of the addend is read out of the right HSM 16 through the gates 1032 (FIG. 1(d-d)) primed by a pulse from the gate 1030 (FIG. 1(c-d)) into the Z register 14 (FIG. 1(d-d)). The addend character and augend character are thus read out as in decimal addition.

The special characters also are treated in a manner similar to that in decimal addition. For example, if an item separation symbol ISS is read out of the right HSM 16 into the Z register 14, the NOT ISSR lead (FIG. 1(d-d)) from the "or" circuits R1054 is lowered. Accordingly, the ISSR lead (FIG. 1(d-e)) from the inverter I12 is at a high level. The gate 1068 (FIG. 1(e-d)) is primed. At the eighth timing pulse T8, the gate 1068 passes a pulse to the set terminal of the end of operand right flip-flop F1010 (FIG. 1(d-e)). At the same time, the pulse from the gate 1068 (FIG. 1(e-d)) resets the Z register 14 (FIG. 1(d-d)) after passing through the delay circuit D56. Accordingly, at the next RI, a zero character is added through the adder.

Note that if an ISS is recognized in the Y register 13, the gates G27 are closed by the high level from the "one" output of the ISSL flip-flop F910 passing through the inverter as indicated.

T8a

The eighth delayed timing pulse T8a is now passed through the status transition gate 1249 (FIG. 1G) to select the status level RI.

5.6.2 Status Level RI High

T1-T3½

The gate G4 passes the first timing pulse T1 to set the adder input flip-flop F3. The "one" output of the adder input flip-flop F3 primes the gates 27, 21, and 12. These gates pass the contents of the Y register 13 (FIG. 1(c-d)) and the Z register 14 (FIG. 1(d-d)) the contents of the latter register also pass through the gates 1048 (FIG. 1(c-d)) primed by the operation level B respectively into the two six-bit inputs of the duplicated adder 17A.

105

The address in the C counter 12 (FIG. 1(c-b)) is applied to the HSM 15, 16 (FIGS. 1(c-d)) and 1(d-d)). If the 2⁹ bit flip-flop of the C register 28 is reset, the left HSM 15 is addressed through the gates 650 (FIG. 1(c-b)), as in decimal addition. If the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its set condition, then the right HSM 16 (FIG. 1(d-c)) is addressed through the gates 660 (FIG. 1(c-b)), as in decimal addition.

At the timing pulse T1½, the gate G10 sets the adder output flip-flop F4 (FIG. 1(e-c)) to prime the adder 17A output (FIG. 1(e-b)). The output of the adder is then applied directly to the L register 18 and the R register 19 through the gates 809 (FIG. 1(f-e)) without the result passing through the binary to coded-decimal converter 17B. The carry, if any, resulting from the addition of the six bits of the operands, sets the flip-flop F1 (FIG. 1(f-b)). The carry is handled in the addition of the following characters in the same way as for decimal addition, with the difference, however, that there is no end around carry in the operation B (binary addition), and no negative operands.

At the second timing pulse T2 the count of the C counter 12 (FIG. 1(c-b)) is increased one by a pulse from the gate 380 (FIG. 1(c-a)) as in decimal addition.

T5

If the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset condition, the gate 721 (FIG. 1(c-c)) primes the gates 722 allowing the binary sum of the least significant character of the operands to flow into the left HSM 15 at the address specified by the instruction. If the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is set, so that the "one" output is high, the gate 850 (FIG. 1(d-c)) primes the gate 899 to pass the fifth timing pulse T5 to prime the gates 851 allowing contents of the R register 19 to pass into the right HSM 16.

T8a

At the eighth delayed timing pulse T8a, the status transition gate 1263 (FIG. 1G) selects RO to be a high status level.

5.6.3 Succeeding Status Levels

With the next RO status level high, the second least significant characters of the operands are read out of the HSM 15, 16 and stored in the Y and Z registers 13 and 14 respectively. Then during the next RI status level high the characters are added and the sum is stored in the HSM 15, 16. The sequence is repeated until the characters have all been added and the end of each operand has been recognized. If item separation symbols are recognized by the left symbol recognition circuits 22 and the right symbol recognition circuits 23, the gate 948 (FIG. 1(e-d)) is primed as in decimal addition. At the high RI status level immediately after such recognition, the first timing pulse T1 is passed through the gate 948 to set the EOBO flip-flop F1110 (FIG. 1(f-c)). At the same time the gate 499 (FIG. 1(e-c)) passes the first timing pulse T1 from the gate 948 to set the 2¹¹ bit flip-flop of the C register 28 (FIG. 1(c-a)). The setting of this 2¹¹ flip-flop makes the "zero" terminal of the 2¹¹ bit flip-flop return to a low level. Accordingly, the priming voltage for the right and left read-in gates 721 and 850 (FIGS. 1(c-c) and 1(d-c)), respectively, is removed, and information cannot be written into the HSM 15, 16. The set condition of the EOBO flip-flop F1110 (FIG. 1(f-c)) primes the status transition gate 1201 (FIG. 1H) to select the status level IC for instruction complete to be high.

5.6.4 Sequence of Status Levels

With reference to the flow diagram of FIG. 17 for binary addition, the instruction is staticized in RO01, RO02, RO03 in the usual manner. After the status level RO03 is high, the status level RO is selected to be high. The

106

least significant characters of the augend and addend are read out of the left and right HSM 15 and 16 respectively. A transition is made to the high status level RI and the binary equivalents of the least significant characters of the addend and augend are added together. The sum is stored in the HSM 15, 16 at the address coded in the C counter 12. The binary carry (if any) is stored for further use in the addition of the second least significant characters of the addend and augend.

When the high status level RI is complete, the machine then selects the status level RO to be high. The second least significant characters are read out of the HSM 15, 16 and in the high status level RI are added together. The sum is placed in the next higher HSM location as indicated by the C counter 12 (FIG. 1(c-b)) the count of which has been advanced one.

The successive sequence of RO-RI continues until the "end of both operands" is reached. In this operation, the end of operand symbol is limited to an item separation symbol. A carry which may be obtained from a final addition of an addend and an augend is discarded, that is, the carry is not added in when two item separation symbols have been reached. The machine simply makes the transition to, or selection of, the next high status level IC.

The instruction for binary addition is convenient for modifying instructions. For example, it may be desired to make a sequence of additions from selected places in the left and right HSM 15 and 16. It may be desired to store the result or sum of the additions successively in addresses differing by ten. For example, the address designated by the decimal number 1400 in the left HSM 15 may be assigned to receive the least significant digit of a sum representing a previous stock on hand figure and a number of items to be added or subtracted therefrom. The address 400, however, is for only one depot, say depot A.

It may be desired to form a similar sum for a B depot, a C depot, etc. The addresses, however, are coded in the binary equivalents of decimal 400, decimal 410, etc. From the foregoing, it will now be apparent to those skilled in the art, that only the first result location in the memory for the A depot need be coded in binary form. Thereafter, the remaining addresses may be secured by programming the desired binary addition, that is, by adding the binary equivalent of 10 to the memory location in a sequence of additions to derive the successive addresses.

5.7 Read-In From Tape—(Operation N)
Operation Level N High

5.7.1 Additional Components

Various components in addition to those already described are employed in this operation. A flip-flop identified as "Before first Re" flip-flop F705 (FIG. 1(b-b)) has applied to its reset terminal R a lead designated "RO01-T1 reset" from the gate 943 (FIG. 1(d-e)). The RO01-T1 reset lead receives or applies the first timing pulse T1 during status level RO01. Note that the RO01 reset lead is applied to the "Before first Re" FF F705 through an "or" circuit (FIG. 1(b-b)) the other input of which comes from a gate 735. The gate 735 is primed by the high operation level N. The other input to the gate 735 comes from the 2¹⁰ bit of the drum output. The set terminal S of the "Before first Re" flip-flop 705 receives the output of a gate 734. The gate 734 has three inputs, one from the operation level N, a second from the status level RO02, and a third from the eighth timing pulse T8.

A flip-flop designated "After first Re" flip-flop F703 (FIG. 1(b-b)) has applied to its reset terminal R the RO01-T1 reset lead (FIG. 1(d-e)) through a suitable "or" circuit (FIG. 1(b-b)). The other input to the last mentioned "or" circuit is from the output of a gate 733. The gate 733 has four inputs, a first from the

"one" terminal of the 2^{10} bit flip-flop of the C register 28. A second input to the gate 733 is from the eighth timing pulse T8. A third input to the gate 733 is from the "one" output of an EM or ET FF flip-flop F702 (FIG. 1(b-c)) to be described hereinafter; and a fourth input to the gate 733 (FIG. 1(b-b)) is from the status level R1. The set terminal S of the "After first Re" flip-flop F703 is connected to receive the output of a gate 742. The gate 742 has three inputs: a first from the high operation level N, a second from the status level RO02, and a third from the fourth timing pulse TP4. The "zero" output of the "After first Re" flip-flop F703 is applied to the gate 243 (FIG. 1(a-b)). The gate 243 is also primed by the output of the gate 245 described hereinbefore in connection with the surge of instructions. The gate 243 receives a third input from the "or" circuit passing the status levels IC, or RE. The final input to the gate 243 is the eighth timing pulse T8.

The "one" output terminal of the "After first Re" flip-flop F703 (FIG. 1(b-b)) is connected to a gate 736 and also to a gate 241 (FIG. 1(a-b)). The other inputs to the gate 241 are the "zero" terminal of the "Before first Re" flip-flop F705, (FIG. 1(b-b)) the status level RE, and the eighth delayed timing pulse T8c (which follows T8a). The output of the gate 241 (FIG. 1(a-b)) is applied through a suitable "or" circuit to the reset terminal R of the program subcounter PSC.

The gate 736 (FIG. 1(b-b)) in addition to its two inputs, one from the "one" terminal of the "After first Re" flip-flop F703 and the "zero" output of the "Before first Re" flip-flop F705, is also primed by the high status level RE, and the fourth timing pulse T4. The output of the gate 736 is applied to the set terminal of a start tape pulse flip-flop F704 (FIG. 1(b-c)). A gate 737 (FIG. 1(b-b)) has an output applied to the reset terminal R of the start tape flip-flop F704. The gate 737 is primed by either one of the high status levels RO01 or RO03 applied through an "or" circuit. The gate 737 also has applied to it the fourth timing pulse T4.

The output from the start tape flip-flop F704 (FIG. 1(b-c)) "one" terminal is connected to a gate 606 (FIG. 1(b-d)) and also to a gate 605 (FIG. 1(b-d)) in the tape handling circuits 46. The gates 605 and 606 are each primed by the high operation level N. The output of the gate 605 is applied to a pulse responsive mechanism which starts a drive to operate a tape A. The pulse responsive mechanisms and drives of the tapes are not shown. The gate 606 output is applied to a pulse responsive mechanism to start tape B. The tapes A and B are input tapes. The reset terminal of a tape selector flip-flop F601 (FIG. 1(b-c)) is connected to receive the output of a gate 602. The gate 602 has applied to it at one input the status level RO02, at a second input the output from the "one" terminal of the 2^1 bit flip-flop from the B counter 11 (FIG. 1(d-b)), and at a third and final input the eighth timing pulse T8. The output from a gate 601 (FIG. 1(b-c)) is applied to the set terminal S of the tape selector flip-flop F601. The gate 601 has three inputs, one from the "one" terminal of the 2^0 bit flip-flop of the B counter 11 (FIG. 1(d-b)); a second from the status level RO02; and a third from the eighth timing pulse T8.

A pre-character in flip-flop F806 (FIG. 1(b-c)) has its set terminal connected to a lead designated "input tape character present," to be described hereinafter. The pre-character flip-flop F806 has its reset terminal R connected to receive the output of a gate 870 (FIG. 1(b-b)). The gate 870 is primed by the high status level RO01 applied through an "or" circuit, and passes the second timing pulse T2 when so primed. The pre-character is flip-flop F806 (FIG. 1(b-c)) has its "zero" output terminal applied to prime a gate 868. The gate 868 also has applied to it the eighth timing pulse T8. The output of the gate 868 is applied to the reset terminal R of a character in flip-flop F805. The "one" output terminal of the

pre-character in flip-flop F806 is applied to a gate 869 which is also primed by the high operation level N. The sixth timing pulse T6 is also applied to the gate 869. The output of the gate 869 is applied to the set terminal S of the character-in flip-flop F805. The "one" output terminal of the character-in flip-flop F805 is applied through an "or" circuit (described before and receiving also the level RO01) to the gate 870 (FIG. 1(b-b)).

A first EM or ET flip-flop F706 (FIG. 1(b-e)) has its "one" output terminal connected to one input of a gate 609 (FIG. 1(b-d)), among the tape handling circuits 46 and also to one input of a gate 732, (FIG. 1(b-b)). Each of the gates 609 and 610 of FIG. 1(b-d) has a second input. The gate 609 has its second input from the "one" output of the tape selector flip-flop F601 (FIG. 1(b-c)). The gate 610 has its second input from the "zero" output terminal of the tape selector flip-flop F601. The output of the gate 609 is applied to a mechanism to stop the tape A drive, which responds to a high level on this output to stop tape A. The output of the gate 610 is applied to a similarly responsive mechanism to stop the tape B drive.

The gate 732 (FIG. 1(b-b)) receives the third timing pulse T3. The reset terminal R of the second EM or ET flip-flop 702 is connected to the RO01-T1 reset lead (FIG. 1(d-e)). The set terminal S of the second EM or ET flip-flop F702 (FIG. 1(b-c)) is connected to receive the output of the gate 732.

The "one" output of the second EM or ET flip-flop F702 (FIG. 1(b-c)) is also applied to a gate 238 (FIG. 1(a-a)) and through "or" circuits to two inputs of a gate 101. The gate 238 has a second input the output from the "one" terminal of the 2^{10} bit flip-flop of the C register 28 (FIG. 1(c-a)). A third input to the gate 238 is the status level R1. The final input to the gate 238 is the seventh timing pulse T7.

The gate 101 (FIG. 1(a-a)) receives through suitable "or" circuits, as mentioned before, at the input terminal marked "i" shown at the top of the gate as viewed in the drawing, the output from the "one" terminal of the second EM or ET flip-flop F702 (FIG. 1(f-c)), and at the same input terminal of the gate 101, but through an "or" circuit as shown, the output from the "one" terminal of the previous result zero flip-flop F1101 (FIG. 1(f-d)) and also the output from the "one" terminal of the previous result negative flip-flop F1109. A second input to the gate 101 (FIG. 1(a-a)) receives the output from the "one" terminal of the second EM or ET FF flip-flop F702 through an "or" circuit to which is also applied the output from the "one" terminal of the previous result all nines flip-flop F1103 (FIG. 1(f-d)) and the output from the "one" terminal of the previous results zero flip-flop F1101 (FIG. 1(f-d)). A third input to the gate 101 is from an "or" circuit the inputs to which are status levels R1 and RO03. Note that the input from the operation level C is applied through an "or" circuit to that input of the gate 101 that receives the output from the "one" terminal of the 2^{10} bit flip-flop of the C register 28.

One input to a gate 239 (FIG. 1(a-a)) is from the "one" terminal of the "Before first Re" flip-flop F705 (FIG. 1(b-b)). A second input to the gate 239 is from the status level RO03. The third input to the gate 239 is the seventh timing pulse T7.

A gate 240 (FIG. 1(a-a)) is provided having three inputs. To the first input of the gate 240, through various "or" circuits, are applied the following: The operation level Q, the operation level T, the output from the "one" terminal of the previous result negative flip-flop F1109, and the output from the "one" terminal of the previous result zero flip-flop FF1101. A second input to the gate 240 is the status level RO03. The third input to the gate 240 is the seventh timing pulse T7. The outputs of the gates 238, 239, and 240 are applied through an "or" circuit to the reset terminals R of the program counter PC;

and also through "or" circuits to the reset terminals R of the program subcounter PSC (FIG. 1(a-b)).

A gate 114 (FIG. 1(a-a)) has one input from an "or" circuit to which is applied any the high operation levels T, N, or C. A second input to the gate 214 is from a suitable "or" circuit to which are applied the output from any one of the terminals of the previous result negative flip-flop F1109 (FIG. 1(f-d)), the "Before first Re" flip-flop F705, or the lead from the high operation level T. A third input to the gate 114 (FIG. 1(a-a)) is from the "zero" terminal of the previous result all nines flip-flop F1103 (FIG. 1(f-d)). A fourth input to the gate 114 is from the status level RO03. The final input to the gate 114 is from the eighth timing pulse T8. A three-input gate 127 (FIG. 1(a-a)) has applied to it the operation level Q at one input, the status level RO at a second input, and at the third input the sixth timing pulse T6.

A set of twelve gates 115 are connected so that the "one" terminals of the C register 28 are connected between the set terminals of the corresponding flip-flops of the program counter PC. The gates 115 are opened by the output of the gate 114.

A set of twelve gates 102 (FIG. 1(a-a)) are connected so that, when these gates are opened, the set terminals of the nine most significant bit flip-flops (highest order) of the program counter PC respectively receive the output of the "one" terminals of the A register 26 flip-flops (FIG. 1(c-a)) and the set terminals of the three least significant bit flip-flops of the program counter PC respectively receive the output of the "one" terminals of the B counter 11 (FIG. 1(d-b)).

Among the left symbol recognition circuits 22 (FIG. 1(b-d)) is a set of "or" circuits R920. The output of these "or" circuits R920 is designated EM. The output of the EM "or" circuits R920 is applied to a gate 485. A second input to the gate 485 is the operation level N. A third input to the gate 485 is from the output of a two of gates, 941 and 942, through an "or" circuit as shown. The gate 941 (FIG. 1(b-e)) has been described (section 5.1.5 supra). The gate 942 (also FIG. 1(b-e)) receives as its inputs, first the operation level N, second the status level RI, and third and finally the first timing pulse T1. The output of the gate 485 (FIG. 1(b-d)) is applied to the set terminal of the 2¹¹ bit flip-flop of the C register 28. The output of the EM "or" circuits R920 are high if and only if an "end message" symbol (a unique code symbol) is stored in the Y register 13.

The output of the EM "or" circuits R920 is applied to a pair of gates 740 and 936 (FIG. 1(b-e)). Applied to the same input of the gates 740 and 936 is the output from a set of "or" circuits R921 (FIG. 1(b-d)) which is at a high level if and only if the symbol for the end of the tape ET is recognized. The manner of operation if such "or" circuits as R920 and R921 has been described hereinbefore. The gates 740 and 936 (FIG. 1(b-e)) each has a second input received from the output of the two gates 941 and 942 applied through a suitable "or" circuit (the latter "or" circuit is shown in FIG. 1(b-d)). These are the two inputs to the gate 936 (FIG. 1(b-e)) already described. The gate 740 has a third input from the operation level N. The output of the gate 740 is applied to the set terminal S of the first EM or ET flip-flop F706 (FIG. 1(b-e)). The output of the gate 936 is applied through suitable "or" circuits as shown to the reset terminal of the Minus L flip-flop F909.

A gate 741 (FIG. 1(b-e)) has an output applied to the reset terminal R of the first EM or ET flip-flop F706. The gate 741 receives as one of its inputs either one of the high status levels RO03 or RE applied through an "or" circuit as shown. A second and final input to the gate 741 is from the first timing pulse T1.

A gate 939 (FIG. 1(b-e)) receives one input from the "one" output terminal of the character-in flip-flop F805

(FIG. 1(b-c)). A second input to the gate 939 (FIG. 1(b-e)) is from the item separation symbol left ISSL lead. A third input to the gate 939 is from the high status level RD. The fourth and final input to the gate 939 is the eighth timing pulse T8. The output of the gate 939 is applied through "or" circuits as shown to the reset terminal R of the minus L flip-flop F909.

A gate 949 has applied to it three inputs, one from the status level RI, a second from the operation level N, and the third one from the eighth timing pulse T8. The output of the gate 949 is applied through "or" circuits to the reset terminal of the ISSL flip-flop F910 (FIG. 1(c-e)).

A set of "or" circuits R904 (FIG. 1(c-d)) are provided. Each of the "or" circuits R904 receives two inputs, one from each of the corresponding data channels on each tape, tape A and tape B. There are seven data channels on each tape. Accordingly, whichever tape is being driven, if a seven digit binary coded character passes under the read heads of that tape, the binary character is passed as a set of pulses to the respective seven set terminals of the Y register 13.

A tape minus flip-flop F701 (FIG. 1(b-d)) has its set terminal connected to receive the output of a gate 731 is primed by the "one" output of the minus L flip-flop F909 (FIG. 1(b-e)). The gate 731 also receives the sixth timing pulse T6. The reset terminal of the tape minus flip-flop F701 is also connected by suitable "or" circuits to receive the output of the gates 936 or 939 (FIG. 1(b-e)), or the RO01-T1 reset from gate 943 (FIG. 1(d-e)). The "one" output terminal of the tape minus flip-flop F701 (FIG. 1(b-d)) is connected as one of the inputs to each of a set of five, six-input gates 925 (FIG. 1(c-d)). The gates 925 are connected respectively to receive the six "one" output terminals of the Y register 13, excluding the parity bit, as a second input. A third input applied to each of the gates 925 is from the "one" terminal of a flip-flop F908. The flip-flop F908 provides a broad pulse lasting from the first timing pulse, T1 to a time between the third and fourth timing pulses (T3 to T4). The flip-flop F908 for this purpose has its set terminal connected to receive the first timing pulse T1 and its reset terminal connected to receive the third timing pulse T3 after a suitable short delay in a delay circuit D12 less than the time between third and fourth timing pulses T3 to T4. A fourth input to each of the gates 925 is from the "zero" output terminal of the first EM or ET flip-flop F706 (FIG. 1(b-e)). A fifth input to each of the gates 925 (FIG. 1(c-d)) is from the status level RI. The sixth input to each of the gates 925 is from the operation level N. The outputs of the gates 925 are applied to the nines complementor 21 (FIG. 1(e-c)).

Note that only the five bits of the six-bit output of the gates 925 are applied to the nines complementor 21 (FIG. 1(e-c)) when the tape minus flip-flop (FIG. 1(f-d)) is set to open gates 925 (FIG. 1(c-d)) indicating a decimal digit character. The sixth and seventh bits are restored in a manner similar to that when performing subtraction by a parity generator PG (FIG. 1(d-e)) and a set of five gates 815 (FIG. 1(e-d)). The gates 815 (FIG. 1(e-d)) are each primed by the operation level N, and also by the "one" output from the tape minus flip-flop F701 (FIG. 1(b-d)). Therefore a fifth bit (the 2⁴ or parity bit) is restored from the parity generator PG (FIG. 1(d-d)) which receives the output of the nines complementor 21. The 2⁴ bit is restored at the memory input, always being "one" as required by the code for a decimal digit. The 2⁵ bit is zero in the code for a decimal digit and therefore the corresponding flip-flop need not be set. The parity generator may be similar to the parity regenerator 44 (FIG. 1(b-d)) heretofore described. The output of the parity generator PG (FIG. 1(d-d)) is gated by the output of a gate G16 applied through an "or" circuit. The inputs to the gate G16

are the high status level RI, the high operation level N, and the second timing pulse T2.

A set of five, three-input gates 821 (FIG. 1(c-d)) is provided each primed by the high "zero" output of the tape minus flip-flop F701 (FIG. 1(b-d)). The gates 821 (FIG. 1(c-d)) are each primed at a second input by the output of a three-input gate 820. The three inputs to the gate 820 are: the high status level RI, the operation level N, and the second timing pulse T2. The gates 821 are connected to pass, when so primed, the 2⁰ to 2³ and 2⁴ bits from the Y register 13 to the corresponding set terminals S of both the L and R registers 18 and 19 (FIGS. 1(b-d) and 1(d-c)). A pair of gates 825 (FIG. 1(c-d)) are also each primed by the high output of the gate 820. The gates 825 are connected to pass, when so primed, by the gate 820 output, the 2⁴ and 2⁵ bits from the Y register 13 (FIG. 1(c-d)) to both the L and R registers 18 and 19 (FIGS. 1(b-c) and 1(d-c)).

A gate G14 (FIG. 1(e-d)) has three inputs, one from the high status level RI, one from the high operation level N, and the final one from a long pulse from the second timing pulse to the third T2 to T3. The output of the gate G14 is applied through an "or" circuit to clock, or prime, the output of the nines complementor 21.

A three input gate 859 (FIG. 1(c-d)) has as one input the "one" output of the second EM or ET flip-flop F702 (FIG. 1(b-c)). A second input to the gate 859 (FIG. 1(c-d)) is from the status level RI. The third input to the gate 859 is the second timing pulse T2. The output of the gate 859 is applied inclusive through "or" circuits to the set terminals of the 2² to 2⁶ bit flip-flops of each of the L and R registers 18 and 19 (FIGS. 1(b-c) and 1(d-c)). Note that if these L and R registers are reset, then setting the 2², 2³, 2⁴, 2⁵, and 2⁶ bit flip-flops is equivalent to entering an ISS in these registers (coded as binary 0111100 in this machine).

A four-input gate 1099 (FIG. 1(d-d)) receives as one input the "one" output of the 2⁶ bit of the Z register 14; as a second input either high operation level W or H; as a third input the MR lead; and as the fourth input the timing pulse T1. The output of the gate 1099 is applied through an "or" circuit to the reset terminal of the 2³ bit only (fourth order) flip-flop of the Z register 14. This application of the output of gate 1099 is indicated, for convenience, only by the eighth delayed timing pulse T8a.

The four-input status transition gate 1219 receives as its first input the output from the "one" terminal of the "Before first Re" flip-flop F705 (FIG. 1(b-b)); a second input from the status level RO03; a third input from the operation level N; and a fourth input from the eighth delayed timing pulse T82.

Status transition gates 1228 and 1229 (FIG. 1H) are provided each having its output applied through "or" circuits to the "set RD" lead. The four-input status transition gate 1228 receives one input from the "zero" output terminal of the second EM or ET flip-flop F702 (FIG. 1(b-c)); a second input from the status level RI; a third input from the operation level N; and a fourth input from the eighth delayed timing pulse T8a.

The six-input status transition gate 1229 (FIG. 1H) receives one input from the "zero" terminal of the "Before first Re" flip-flop F705 (FIG. 1(b-b)), a second input from the "zero" terminal of the second EM or ET flip-flop F702 (FIG. 1(b-c)); a third input from the NOT ISSL lead (FIG. 1(b-d)); a fourth input from the operation level N; a fifth input from the status level RO03; and the sixth input from the eighth delayed timing pulse T8a.

A three-input gate 313 has as one input the output of an "or" circuit receiving the operation level W, H, and N, as a second input the status level RO03, and as a third input the eighth timing pulse T8.

5.7.2 Machine Operation

The instruction is staticized as follows:

O Section	A Section	B Section	C Section
Code for read-in from tape.	Number of drum line for next instruction after current read-in is completed.	Tape identification.	Drum line where sequence of item addresses starts.

5.7.2.1 Status Level RO01 High

Note that, as the instruction is being staticized, and while status level RO01 high, the first timing pulse T1, is passed through the gate 943 (FIG. 1(d-e)) to the RO01 reset lead to reset the "Before first Re" flip-flop F705 (FIG. 1(b-b)); the "After first Re" flip-flop F703; the second EM or ET flip-flop F702 (FIG. 1(b-c)); the ISSL flip-flops F910 (FIG. 1(c-e)) and the tape minus flip-flop F701 (FIG. 1(b-d)). The O register 30 is reset by the first timing pulse T1 passed through a gate 1401 primed by the status level RO01.

T2

At a second timing pulse T2, the pre-character-in flip-flop F806 (FIG. 1(b-c)) is reset by the output of the gate F870 (FIG. 1(b-b)).

T4

The start tape flip-flop F704 (FIG. 1(b-c)) is reset by the fourth timing pulse T4 passed by the gate 737 (FIG. 1(b-b)).

T8

The character-in flip-flop F805 (FIG. 1(b-c)) is reset by the eighth timing pulse T8 passed by the gate 868.

T8a

The status transition gate 1280 by passing the eighth delayed timing pulse T8a selects the status level RO02 to be high. Note that due to the O register having received the code for operation N, the operation level N is high.

5.7.2.2 Status Level RO02 High

T4

As the instruction is being staticized, and while status level RO02 is high, the gate 742 (FIG. 1(b-b)) passes the fourth timing pulse T4 to set the "After first Re" flip-flop F702.

T8

The gate 734 (FIG. 1(b-b)) passes the eighth timing pulse T8 to set the "Before first Re" flip-flop F705. The high "one" terminal of the "Before first Re" flip-flop F705 then primes one input to the gate 114 (FIG. 1(a-a)). The gate 239 (FIG. 1(a-a)) is also primed by the high "one" terminal of the "Before first Re" flip-flop F705 (FIG. 1(b-b)).

Data may be taken from either tape A or tape B. Recall that the B counter 11 receives its portion of the instruction during the high status level RO02, at the sixth timing pulse T6. If the 2⁰ bit flip-flop in the B counter 11 (FIG. 1(d-b)) is set, the gate 601 (FIG. 1(b-c)) passes the eighth timing pulse T8 to set the tape selector flip-flop F601. The gate 605 (FIG. 1(b-d)) is then primed by the "one" terminal output of the tape selector flip-flop F601 (FIG. 1(b-c)) to start the tape A as soon as the "one" output terminal of the start tape flip-flop F704 (FIG. 1(b-c)) is high at a later time. On the other hand, if the 2¹ bit flip-flop in the B counter 11 (FIG. 1(d-b)) is set, the gate 602 (FIG. 1(b-c)) passes the eighth timing pulse T8 to reset the tape selector. The "zero" output terminal of the tape selector flip-flop F601 is high and the gate 606 is primed to pass a pulse when the start tape pulse flip-flop F704 is set,

113

to start the B tape. The programmer notes that for this instruction, the 2^0 bit flip-flop of the B counter 11 and the 2^1 bit flip-flop of the B counter 11 are not both set at the same time. Note that the gate 610 for stopping tape B is primed by the same output as that for starting tape B from the zero output of tape selector flip-flop F601 and with the same coding. Also gate 609 for stopping tape B is primed by the high "one" output from the tape selector of flip-flop F601 with gate 605. Note that the coding (B section) allows for the selection among more than two tapes. Circuits for such selection are readily devised in view of those shown illustratively herein.

T8a

The status transition gate 1275 (FIG. 1G) passes the eighth delayed timing pulse to cause the status level RO03 to be high.

5.7.2.3 Status Level RO03 High

As the instruction is being staticized, and while status level RO03 is high, the first EM or ET flip-flop F706 (FIG. 1(b-e)) is reset by the first timing pulse T1 passed by the gate 741.

T6

The sixth timing pulse passed through the gate 1137 (FIG. 1(f-e)) resets the previous result all nines flip-flop F1103 (FIG. 1(f-d)), the previous result negative flip-flop F1109, and the previous result zero flip-flop F1101. The now high "zero" output terminal of the previous result all nines flip-flop F1103 is applied to further prime the gate 114 (FIG. 1(a-a)).

T7

The gate 239 (FIG. 1(a-a)) primed by the "one" output of the "Before first Re" flip-flop F705 (FIG. 1(b-b)) to reset the program counter PC (FIG. 1(b-c)) and the program subcounter PSC (FIG. 1(a-b)). Note that the "Before first Re" flip-flop F705 (FIG. 1(b-b)) was set when RO02 was high by a pulse (T8) from the gate 734.

The gate 114 (FIG. 1(b-a)) now passes the eighth timing pulse T8 to open the gates 115. The drum line number of the first address of the item addresses to be surged into the HSM 15, 16, stored in the C register 28 (FIG. 1(c-a)), is now passed into the program counter PC (FIG. 1(a-a)).

The status transition gate 1219 (FIG. 1H) passes the eighth delayed timing pulse T8a to select the status level RE to be high.

5.7.2.4 Status Level RE High—Start Surge of Addresses

The addresses at which the items to come from the tape are to be stored are now to be surged from the program drum into the surge tank section of the HSM 15, 16. The first item address is on the drum line specified in the address portion of the instruction. The surge is similar to that described in the aforementioned Bensky, et al. Patent 2,679,638. This drum line number is presently stored in the program counter PC (FIG. 1(a-a)). All the remaining addresses of the items have been placed consecutively on alternate drum lines. The count of the drum line in the drum counter DC is compared with the drum line numbers set into the program counter PC. When equality is indicated, the drum line match flip-flop F125 is set, as in the instruction surge, as described in the said Bensky, et al. patent or in the said Bensky application, by a high level from the output of the third equal circuit 50 (FIG. 1(a-a)). The third equal circuit 50 may be a group of "or" circuits and "and" gates arranged so that a final gate is primed if and only if all the corresponding inputs are equal. This final gate is primed also by the high status level RE. The fourth delayed timing pulse T4c is applied to this final gate through

114

a suitable delay circuit D13, the delay being such that the output occurs before T5.

The drum line match flip-flop F125 "one" output terminal, now high, primes the gate 142 (FIG. 1(a-b)), the gate 242 (FIG. 1(a-b)) and the gate 232 (FIG. 1(a-c)).

Note that before the count in the program counter PC (FIG. 1(a-a)) and the drum counter DC are equal, that the machine operates as though it were in the status level RE as previously described in connection with surging instructions from the drum into the memory. In other words, only the timing pulses designated T1, T2, T3, and T4, and delayed pulses up to, but not including T5, in the timing sequence can occur, and timing pulses T5 and later in the higher sequence are inhibited (that is, prevented) by the circuitry involving the reset-to-start flip-flop F201 (FIG. 1(a-d)) as already described.

After the complete cycle of the timing pulses starts, and the drum line match flip-flop F125 (FIG. 1(a-b)) is set, the address surge from the program drum PD (FIG. 1(a-a)) may begin.

5.7.2.5 Address Surge—Status Level RI High

At the first timing pulse T1, the gate 629 (FIG. 1(d-b)) passes the first timing pulse T1 to prime the gates 630 and 630a. The HSM 15, 16 is addressed at the location corresponding to decimal zero by the program subcounter PSC (FIG. 1(a-b)) (recall that the program subcounter PSC was reset when status level RO03 was high) through these last mentioned gates. Thus the surge entry into the surge tank section of the memory starts at this zero location in both the memory banks, right and left, in this case. The first address surged is then stored at the "zero" location in the left HSM 15 and the "zero" location in the right HSM 16. The first EM or ET flip-flop F706 (FIG. 1(b-e)) is reset by the first timing pulse T1 passed through the gate 741.

Note that the Land R registers 18 and 19 (FIG. 1(b-c) and 1(d-c)) are reset by the first timing pulse passed through the gate 860 (FIG. 1(e-c)).

T2

The gate 242 (FIG. 1(a-b)) passes the second timing pulse T2 to advance the program subcounter PSC by one count beyond zero.

Accordingly, the first address stored at the drum line specified by the program counter PC entry is now read out from the program drum PD. The six bits from the left reading heads and amplifiers 51 (FIG. 1(a-a)) are entered in the L register 18 (FIG. 1(b-c)). The six bits from the right reading heads and amplifiers 52 (FIG. 1(a-a)) are entered in the R register 19 (FIG. 1(d-c)). The "read-in" circuits of the left and right HSM 15 and 16 are activated by the high "one" output terminal of the drum line match flip-flop F125.

T6

The first address is now stored, six bits in the zero location in the left HSM 15, and six bits in the zero location in the right HSM 16.

Note that the status level RE now remains high for the next cycle of timing pulses, for there is no status transition gate primed to pass the eighth delayed timing pulse T8a to select a different status level to be high.

5.7.2.6 Continuation of Address Surge

The surge now continues in the manner previously explained in connection with the detailed description of the high status level RE (section 4.4). The successive addresses are stored in the successive memory locations in the surge tank of both memory banks. Notice that the successive addresses are drawn from the alternate drum lines in succession, because the program subcounter PSC (FIG. 1(a-b)) is advanced one by reason of the drum line match flip-flop F125 being set, and the gate 242 being primed to pass the second pulse T2 as a triggering

115

pulse each time that an address is drawn off and stored. Every other drum line is not gated out. Accordingly, the drum line bearing the first address desired is itself addressed by the count entered from the C register 28 into the program counter PC. Note that because the drum line match flip-flop F125 (FIG. 1(a-b)) is set, both the left and right HSM 15 and 16 receive a high level to activate the respective "write-in" circuits from the "one" terminal of the drum line match flip-flop F125, as legended at (FIG. 1(c-c)) near the lower right hand corner. Therefore, as in the previous description herein of the surge of instructions from the magnetic program drum PD, the six information bits one parity bit from one set of seven data channels from the program drum PD is read into the left HSM 15; and the six information bits and one parity bit from the other seven data channels of the program PD are read into the right HSM 16, as each cycle of timing pulses T1 to T8 is completed.

Note that the information gated at the read heads and amplifiers 51 and 52 is at a time when one drum line is passing the heads. The next drum line passes during the period between T4 and T8 of the same cycle of timing pulses. At the eighth timing pulse T8, after passing through the delay circuit D9, (FIG. 1(a-d)), the eighth timing pulse T8 resets the reset-to-start flip-flop F201. Another cycle of timing pulses follows during which the next line is read from the drum. However, this next line is stored in the next succeeding surge tank address, that is, location, in each memory bank surge tank section after the zero. Successive addresses from the program drum PD are now stored in successive addresses in the surge tank of the memory. Each new address at which information from tape is to be stored is placed in the next succeeding higher location in the HSM 15, 16.

In the surge of instructions from the magnetic program drum PD (FIG. 1(a-a)) to the memory HSM 15, 16, the surge is terminated when a specified count entered has been reached in the program subcounter PSC (as previously described). In other words, when the number of drum lines required has been surged, the program instruction surge is terminated. However, in surging the addresses from the magnetic program drum PD (FIG. 1(a-a)) into the memory HSM 15, 16 (FIGS. 1(c-c) and 1(d-c)) at which addresses the items to be entered from the tape are to be stored, the machine recognizes by the code of the last address to be entered from the drum into the memory that the surge of addresses is complete.

The last address to be surged from the drum is indicated by a unit or binary one in the eleventh order bit (designated as the 2^{10} bit) of the twelve significant binary digits read from the program drum PD. Therefore, when the twelve bit addresses (and the two parity bits) are written into the fourteen data channels on the magnetic program drum PD, the eleventh bit of the twelve "information" bits is always written as zero except for the last address to be surged from the drum. For this last address, this eleventh bit is a one. Note on the schematic (FIG. 1(b-a)) that there is indicated a separate branch line which carries the 2^{10} bit from the output of the left read heads and amplifiers 51 of (FIG. 1(a-a)) the branch is on (FIG. 1(b-a)) to the gate 735 (FIG. 1(b-b)). Accordingly, when the last address to be surged from the drum is surged out of the drum, this eleventh bit passes through the gate 735 which is primed by the high operation level N. The "Before first RE" flip-flop F705 (FIG. 1(b-b)) is reset by the pulse from the gate 735.

With the "Before first RE" flip-flop F705 (FIG. 1(b-b)) in its reset state, the gate 736 is primed and passes the fourth timing pulse T4 to set the start tape flip-flop F704 (FIG. 1(b-c)). Accordingly, one or the other of the gates 605 or 606 (FIG. 1(b-d)) has its output at a high level, depending on the condition of the tape selector flip-flop F601. If the tape selector flip-flop F601 is in its set

116

condition, the gate 605 output level is high, and tape A is started. If the tape selector flip-flop F601 is in its reset condition, the gate 606 output is high, and the tape B is started.

T8a

The gate 241 (FIG. 1(a-b)) now passes the eighth delayed timing pulse T8a to reset the program subcounter PSC and also reset the drum line match flip-flop F125. Accordingly, the gate 142 (FIG. 1(a-b)) is closed and no further addresses can be passed from the drum through the read heads and amplifiers 51, 52 (FIG. 1(a-a)) as the output gates of the latter are not primed. Also the gate 242 (FIG. 1(a-b)) is closed so that the program subcounter PSC is not advanced at each cycle of timing pulses with occurrence of the second timing pulse T2, but holds a zero address. The eighth delayed timing pulse T8a is now also passed through the status transition gate 1274 (FIG. 1G) and the status level RO03 is selected to be high. Note that the second EM or ET flip-flop F702 (FIG. 1(b-e)) is assumed still in the reset condition. Note that the "Before first RE" flip-flop F705 has just been reset, due to the 2^{10} bit of the last address being a binary "one."

5.7.2.7 Operation N—Status Level RO03 High After Address Surge

An address is now to be withdrawn from the memory.

T1

The C counter 12 (FIG. 1(c-b)) is now reset by the first timing pulse T1 passed through the gate 328. The gate 629 (FIG. 1(a-b)) passes the first timing pulse T1 to open the gate 630 and 630a. Accordingly, the program subcounter PSC, now being in its reset condition for all stages, addresses the left HSM 15 (FIG. 1(c-c)) and the right HSM 16 (FIG. 1(d-c)) at the zero location through the gates 630 and 630a, respectively. Accordingly, the HSM 15, 16 is addressed at the surge tank location (address) where is stored the address at which the first item to be read in from the tape is to be stored.

T2

The C register 28 (FIG. 1(c-a)) is reset by the second timing pulse T2 passed through the gate 442. The gate 244 (FIG. 1(a-b)) passes the second timing pulse T2 to advance the count in the program subcounter PSC to the next memory location (the address corresponding to decimal one).

T3

The flip-flop F302 (FIG. 1(c-b)) is reset by the third timing pulse T3 passed through the gate 312. The C counter 12 is now in "add" state (but see the next T8) and ready to receive the address of the item to be read in from tape.

The left and right read-out gates 730 and 862 respectively (FIGS. 1(c-c) and 1(d-c)) pass a high level to the read-out circuits of the left and right HSM 15 and 16 respectively, to activate the read-out circuits thereof.

T6

At the sixth timing pulse T6, the gates 436 (FIG. 1(c-a)) and the gates 430 (FIG. 1(c-a)) are opened to pass, respectively, the six bits (excluding the parity bit) from the left HSM 15 (FIG. 1(c-c)) into the C register 28 (FIG. 1(c-a)); and the six bits (excluding the parity bit) from the right HSM 16 (FIG. 1(d-c)) into the C register 28, as previously described in connection with the staticizing of instructions. However, the present entry is an address withdrawn from the memory. The parity bits are stored in the parity register 29 (FIG. 1(d-a)). Also the gates 324 (FIG. 1(c-a)) and the gates 318 pass three bits and six bits respectively from the left HSM 15 (FIG. 1(c-c)) and the right HSM 16 (FIG. 1(d-c)) into the C counter 12 (FIG. 1(c-b)).

117

T8

At the eighth timing pulse T8, the flip-flop F302 (FIG. 1(c-b)) is placed in its set condition by a pulse from the gate 313. The counter 12 is now in its negative counting state, because of the high voltage applied to the "subtract" lead. Each time the C counter 12 is triggered, the address it contains is now decreased by one.

T8a

The eighth delayed timing pulse T8a is passed through the status transition gate 1229 (FIG. 1H) to cause the status level RD now to be high.

5.7.2.8 Status Level RD High—Cycling

The status level RD now remains high until a character is received from one of the tapes. Note that the start tape pulse from the gate 605 or the gate 606 (FIG. 1(b-d)) occurred during the next preceding high status level RO03. The timing required in the machine of this example between the first timing pulse T1 and the succeeding timing pulse T1 is about twenty microseconds. A considerably greater time than this is required for the tape to get up to speed. Even if at full speed, the tape requires a substantially longer time than twenty microseconds to pass succeeding characters under the read heads. The circuits are arranged so that no tape character is lost. On the other hand, the machine is able to await the occurrence or arrival of a significant character on the tape under the read heads. Accordingly, the machine stays in this status level RD high, awaiting the reading of the next character to be passed under the tape reading heads.

The first character read from either tape is passed into the Y register 13 (FIG. 1(c-d)) through the "or" circuits R904. The first character normally will correspond to a special start message symbol (SM).

The output of the "or" circuits R904 is applied to a group of circuits 66 designated "input tape character present" circuits (FIG. 1(b-c)) indicated by legend only. The "input tape character present" circuit is a single "or" circuit receiving the seven outputs of the "or" circuits R904 as seven inputs. Accordingly, if any character not all zeroes is passed through the "or" circuits R904 from either tape, the "input tape character present" circuit provides a pulse output. The output of this "input tape character present" circuit is applied to the pre-character-in flip-flop F806, which is therefore set as soon as a character is present under the heads of that input tape being driven. The gate 869 (FIG. 1(b-c)) is thus primed, when a character is present under the input tape read heads, to pass the next sixth timing pulse T6 to set the character-in flip-flop F805 (FIG. 1(b-c)). The character-in flip-flop F805 "one" output is then high.

Accordingly, the status transition gate 1253 (FIG. 1G) passes the next eighth delayed timing pulse T8a to select the status level RI to be high. Note that at the next timing pulse T2, regardless of status level, the gate 870 (FIG. 1(b-b)) resets the pre-character-in flip-flop F806 (FIG. 1(b-c)), because gate 870 (FIG. 1(b-b)) is primed by the "one" output of the same character-in flip-flop F805 (FIG. 1(b-c)).

Accordingly, the status level RI is now high.

5.7.2.9 Status Level RI High—First Character From Tape

T1

At the first timing pulse T1, the left or right HSM 15, 16 is addressed depending on whether the 2⁹ bit (tenth order) flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset or set condition respectively. If the 2⁹ bit flip-flop in the C register 28 is set, then the gate 694 (FIG. 1(c-b)) is primed from the "one" terminal of the 2⁹ bit flip-flop, and the first timing pulse T1 is passed through the gate 694 to open the gates 660 to address the right HSM 16 (FIG. 1(d-c)). On the other hand if the 2⁹ bit

118

flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset condition, the "zero" terminal of this last mentioned flip-flop is at a high level to prime the gate 698 (FIG. 1(c-b)). The gate 698 passes the first timing pulse T1 to open the gates 650 to address the left HSM 15 (FIG. 1(c-c)).

T2

The gate 380 (FIG. 1(c-a)) passes the second timing pulse T2 to trigger the C counter 12. Because the C counter 12 is in its negative or reverse counting state, as pointed out above, the address in the C counter 12 is decreased by one. Note that the character in the Y register 13 is not a negative symbol. The case in which a negative symbol is encountered, together with certain other particular cases, is discussed hereinafter. The tape minus flip-flop F701 (FIG. 1(b-d)) is assumed in its reset condition. The gates 821 (FIG. 1(c-d)) are primed by the "zero" output of the tape minus flip-flop F701. When the gate 820 passes the second timing pulse T2 to open the gates 821 and the gates 825 are opened, then the entry in the Y register 13 (FIG. 1(c-d)) is now transferred, four bits through the gates 821 (FIG. 1(c-d)), and two bits (identified as the 2⁴ and 2⁵ bits) through the gates 825 (FIG. 1(c-d)), to the L register 18 and the R register 19 (FIGS. 1(b-c) and 1(d-c)). Note that the five bits designated as 2⁰ to 2³ and 2⁶ bits are passed through the gates 821. The 2⁴ and 2⁵ bits are passed through the gates 825.

T4

The gate 901 (FIG. 1(b-d)) passes the fourth timing pulse T4 to reset the Y register 13.

If the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is reset, the gate 721 (FIG. 1(c-c)) causes the left HSM 15 to receive and store the information, that is, to be actuated for write-in. If the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its set condition, the right read-in gate 850 (FIG. 1(d-c)) applies a high level to condition the right HSM 16 to receive and store the information.

If the left read-in gate 721 output is high, and the left HSM 15 activated for write-in, the character is passed through the seven gates 722 into the left HSM 15. The gates 722 are opened by the fifth timing pulse T5 passed through the gate 799 primed by the high level from the left read-in gate 721. If the right HSM 16 is activated for write-in, the character is passed through the seven gates 851 into the memory. The gates 851 are opened by the fifth timing pulse passed through the gate 899 primed by the high level from the left read-in gate 850.

At the eighth delayed timing pulse T8a, the status transition gate 1228 (FIG. 1H) causes the status level RD to be selected as high.

5.7.2.10 RD—RI Sequence

The status level RD now is high and nothing further occurs until another character comes in from the tape. In other words, as before, the machine cycles or allows one or more cycles of about twenty microseconds to pass until the next character is read-in from the tape. There follows a repeated RD—RI sequence. As each character is read into the memory during the status level RI high, the C counter 12 count is decreased one, and the characters are read into successive places in the memory. Each item therefore is stored at an address beginning with the address withdrawn from the surge section, and including lower numbered spaces. The succeeding RD—RI cycles are the same as those just described, unless an end message (EM) or end tape (ET) or an item separation symbol (ISS) are encountered. These particular cases are described in greater detail hereinafter. It is in fact contemplated that the first character from a tape will be a start message (SM) symbol, which is to be stored at the first address. It is contemplated that the second character will be an ISS, to be stored at the second address.

5.7.2.11 Status Level RD High—Item Separation Symbol (ISS)

If a character now enters from the tape to the Y register 18 which is an item separation symbol ISS, as for example, the second character, the pre-character-in flip-flop F806 (FIG. 1(b-c)) is set as in the case of an RD high status level already described. The gate 869 passes the sixth timing pulse T6 to set the character-in flip-flop F805.

At the end of this RD cycle, the status transition gate 1272 (FIG. 1G) now passes the eighth delayed timing pulse T8a to the "set RO03" lead, and the status level RO03 becomes high. Note that the status transition gate 1272 (FIG. 1G) is primed by a high output from the ISSL lead in the left symbol recognition circuits 22.

5.7.2.12 Status Level RO03 High—After ISS Recognition

Note that the program subcounter PSC (FIG. 1(a-b)) has been advanced in the preceding high status level RO03 by a second timing pulse from the gate 244. Accordingly, the program subcounter PSC addresses (in this cycle) the memory surge section at a location one higher than that of the address last withdrawn. The address last withdrawn was at the location at which the character of the first item on the tape was to be stored. The memory surge location (address) now in the program subcounter PSC is that at of the future address of the first character of the next item on the tape. The process now is the same as that described for the high status level RO03 after the first RE as described above, and the next address is withdrawn from the surge tank location and entered in the C register 28 (FIG. 1(c-a)), and the C counter 12 (FIG. 1(c-b)).

T8a

At the eighth delayed timing pulse T8a, the status transition gate 1254 (FIG. 1G) causes the status level RI to be high.

5.7.2.13 Status Level RI High—Entry of Next Message Started

The item separation symbol (ISS) is to be read into the HSM 15, 16 at the address last staticized in the last RO03 high status level. Note that this ISS is treated as the first character of the succeeding message. The steps to be followed are the same as that described in the high status level RI, described above (section 5.7.5).

5.7.2.14 Negative Items

Negative items from tape are handled by complementation before entry into the HSM 15, 16. If a minus symbol is read at the beginning of the item, the minus symbol itself is placed directly in the assigned HSM 15, 16 address for the first character of that item, following the item separation symbol ISS. However, the remaining characters of the item are complemented before they are stored in the HSM 15, 16. A negative item that is read in from the tape is composed of binary coded decimal numbers only.

5.7.2.14.1 Status Level RD High—Minus Symbol From Tape

The minus symbol is read into the Y register 13, as in the high status level RD in the same manner as for any character following an item separation symbol. The manner of operation of the machine to complement and store the negative number including storing of the minus symbol itself, follows.

The status transition gate 1253 (FIG. 1G) passes the eighth delayed timing pulse T8a to select the status level RI to be high next, as in the case described above for high status level RD.

5.7.14.2 Status Level RI High—Negative Item From Tape

In the first RI cycle, the minus character itself is transferred from the Y register 13 into the HSM 15, 16. In greater detail:

The gate 820 (FIG. 1(c-d)) passes the second timing pulse T2 to prime the gates 821 and 825. The minus character is then transferred from the Y register 13 through these gates into the L and R registers 18 and 19.

The gate 942 (FIG. 1(b-e)) passes the first timing pulse T1 to the gate 940 (through an "or" circuit of FIG. 1(b-d)) and the pulse is passed through the gate 940 (FIG. 1(b-e)) to set the minus L flip-flop F909. Note that the gate 940 is primed by the "minus L" lead from the minus L inverter 113 (FIG. 1(c-d)).

The left HSM 15 or right HSM 16 (FIG. 1(c-c)) or 1(d-c)) is addressed through the gates 650 or 660 (FIG. 1(c-b)) respectively, according to whether the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset or set condition respectively, as in the status level RI high described just above.

The gate 901 passes the timing pulse T4 to reset the Y register 13.

At the fifth timing pulse T5, the minus character is read into the left HSM 15 or the right HSM 16 depending on whether the 2⁹ bit flip-flop of the C register 28 is in its reset or set condition.

The high "one" output terminal of the minus L flip-flop F909 (FIG. 1(b-e)) primes the gate 731 (FIG. 1(b-d)) to pass the sixth timing pulse T6 to set the tape minus flip-flop F701.

The status transition gate 1228 (FIG. 1H) passes the eighth delayed timing pulse T8a to cause the status level RD to be high.

Note that after the minus character has been read into the HSM 15, 16 the condition is the same as a high status level RI in which an ordinary character is read into the memory, except that the tape minus flip-flop F701 (FIG. 1(b-d)) is now set, and the minus L flip-flop F909 (FIG. 1(b-e)) is also set.

5.7.2.14.3 Cycling in RD—Digits of Negative Item

The machine now "cycles" in the high status level RD until the most significant digit of the negative item is read into the Y register 13, as with any other item. Thereafter at the eighth delayed timing pulse T8a, the status transition gate 1253 selects the status level RI to be high.

The RD cycle just completed is similar to those previously described in which an ordinary non-negative decimal character is entered from the tape.

5.7.2.14.4 Status Level RI High—Negative Item From Tape

The seven bits comprising the most significant digit of the negative item are now stored in the Y register 13. At the first timing pulse T1, the flip-flop F909 (FIG. 1(c-d)) is set. The flip-flop F908 is then reset between the third and fourth timing pulses, the third timing pulse T3 being applied through the delay circuit D12 to the reset terminal R of the flip-flop F908. Accordingly, the gates 925 are primed to pass the least significant five bits (2⁰ to 2⁴ bits) of the character in the Y register 13 through the gates 925 to the nines complementor 21 (FIG. 1(e-d)). The 2⁴ and 2⁵ bits (the fifth and sixth bits respectively) of the original character are transferred directly through the gates 825 (FIG. 1(c-d)) into the L register and R registers 18 and 19 (FIGS. 1(b-c) and 1(d-c)) when the gates 825 (FIG. 1(c-d)) are opened by the second timing pulse T2 passed through the gate 820. Note that the gates 821 are now closed because of the low level output from the "zero" terminal of the tape minus flip-flop F701 (FIG. 1(b-d)).

In the period between the second timing pulse T2 and the third timing pulse T3, the gate G14 clocks the nines complementor. These four bits represent the nine com-

plement of the character if the input was a decimal digit, or they represent a decimal nine if the input was an item separation symbol ISS or space SP, due to the choice of coding, as explained heretofore.

Note that the "one" terminal of the tape minus flip-flop F701 (FIG. 1(b-d)) primes the gate 815 (FIG. 1(e-c)) to pass the four bits from the nines complementor 21 to the L register 18 and the R register 19 (FIGS. 1(b-c) and 1(d-c)). The four bits from the nines complementor 21 are also applied to the parity generator PG, (FIG. 1(d-d)) which is activated at the second timing pulse T2 through the gate G16. The 2⁶ bit output of the parity generator is read into the L and R registers 18 and 19. This 2⁶ bit passes through the fifth of the five gates 819 (FIG. 1(e-d)). Thus all the seven bits are from the Y register 13 to both the L and R registers 18 and 19, (FIGS. 1(b-c) and 1(d-c)), five through gates 815 (FIG. 1(e-d)) and the 2⁴ and 2⁵ bits from gates 825 directly, these always being, respectively, "one" and "zero" for decimal digits.

The contents of the L and R registers 18 and 19 are now read into the left HSM 15 and the right HSM 16 at the fifth timing pulse T5 in accordance with whether the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset or set condition.

At the eighth delayed timing pulse T8a, the status transition gate 1228 (FIG. 1H) again selects the status level RD.

The status levels RD and RI are successively selected to be high so that the remaining significant digits of the negative item are read from the tape into the Y register 13 during the high status level RD, and from the Y register 13 (after complementing by means of complementor 21 (FIG. 1(e-d)) in their complemented form into the HSM 15, 16. Finally, an item separation symbol ISS is reached during the high RD level.

5.7.2.14.5 Status Level RD High—ISS From Tape After Negative Symbol

The ISS is read into the Y register 13 during the high status level RD, as any other character. At the eighth timing pulse T8, provided the minus L flip-flop F909 (FIG. 1(b-e)) was set (that is, if the number which was just read into the HSM 15, 16 was a negative number) the minus L flip-flop is reset by the eighth timing pulse T8 passed through the gate 939. Note that the gate 939 is primed by the high status level of the item separation symbol left lead ISSL. Also, the eighth timing pulse T8 passed by the gate 939 is applied to the reset terminal R of the tape minus flip-flop F701 (FIG. 1(b-d)). Accordingly, the gates 925 (FIG. 1(c-d)) are closed by the low level from the "one" output of the tape minus flip-flop F701 (FIG. 1(b-d)) and the output of the Y register 13 cannot pass, in the subsequent high status level RI, into the nines complementor 21 (FIG. 1(e-d)).

At the eighth delayed timing pulse T8a, the status transition gate passes the eighth delayed timing pulse T8a to select the status level RO03 to be high.

The steps which are followed if the item separation symbol is followed by an end message (EM) symbol or if the complete message has been read from tape, is described hereinafter.

A succession of similar RD-RI cycles follow (reading in characters or negative numbers in the manner described) until again an item separation symbol ISS is reached. The status level RO03 is then high and a new address for the items to be read from the tape is withdrawn from the memory location next succeeding the location of the last address withdrawn. The ISS is read into the first space, and the characters following it are then read into the memory in succeeding spaces until an ISS is again read from the tape, etc.

5.7.2.15 Status Level RD High—Successive ISS's

If there are no characters in an item, two item separation symbols follow each other from the tape.

When an ISS is detected, the high status level RD is followed by the high status level RO03 and the next item address is staticized as described above, (sec. 5.7.3), followed by the high status level RI (as in sec. 5.7.6) for reading of the ISS into the HSM 15, or 16. If, now, another ISS is detected, one of the succeeding RD cycles, without another character intervening, again the status level RO03 is made high, an RI cycle follows, etc.

Note that the status transition gate 1272 (FIG. 1G) is primed by the "one" output of the character-in flip-flop F805 (FIG. 1(b-c)), and also by the high ISSL lead. Accordingly, if an ISS is detected, immediately following reading-in the last ISS, the status level RO03 is selected immediately, without the status level RI being selected after the RD status level is high. After the new address is staticized during the high RO03 level, then the new ISS is written-in during a high RI level, etc.

5.7.2.16 Status Level RD High—End Message Symbol EM

Finally, the least significant character of the last item on the tape is followed by an end message (EM) symbol. The EM symbol is read into the Y register 13 during a high status level RD.

The pre-character-in flip-flop F806 (FIG. 1(b-c)) and the character-in flip-flop F805 are set in the usual manner as above described. As the end message symbol (EM) is entered into the Y register 13, the "or" circuits R920 (FIG. 1(b-d)) have a high level output. The status transition gate 1253 (FIG. 1G) is primed by the "one" output terminal of the character-in flip-flop F805 (FIG. 1(b-c)) and by the NOT ISSL lead from (FIG. 1(b-d)). The status transition gate 1253 (FIG. 1G) therefore passes the eighth delayed timing pulse T8a to select the status level RI to be high.

5.7.2.17 Status Level RI High—After End of Message Symbol (EM)

There are now two possibilities. The first is that the last item address was employed in entering the message just ending with EM. The second is that the end message symbol EM does not coincide with the last item address. Recall at this point that the last item address in its twelve digit binary number form has a binary "one" in the eleventh last significant digit rather than a binary zero.

The two cases are presented in order.

5.7.2.17.1 EM or ET and Last Address

The presence of the EM symbol in the Y register 13 is "recognized" or "detected" by the left recognition circuits 23, and particularly by the "or" circuits R920 (FIG. 1(b-d)) as mentioned before. The EM lead (at the output of "or" circuits R920) is therefore high. The gate 485 (FIG. 1(b-d)), the gate 740 (FIG. 1(b-e)), and the gate 936 are primed by the high level from the EM output lead of the "or" circuits R920.

T1

(The gate 485 (FIG. 1(b-d)) passes the first timing pulse T1 which was passed by the gate 942 (FIG. 1(b-e)). The output of the gate 485 is applied to the "set" terminal of the 2¹¹ (twelfth) bit flip-flop of the C register 28 (FIG. 1(c-a)). The C register 28 2¹¹ bit (twelfth order) flip-flop is therefore set.

Setting this twelfth bit flip-flop prevents read-in because the high "zero" output of this stage provides a priming voltage for the read-in gates 721 (FIG. 1(c-c)) and 850 (FIG. 1(c-c)). Therefore, the read-in gates 721 and 850 are both closed, and the write-in circuits of the left and right HSM 15, 16 are not actuated. Also, the EM symbol cannot be read into the HSM 15, 16 through the gates 722 between the L register 18 and the left HSM 15

123

(FIG. 1(c-c)); nor can the EM symbol be read from the R register 19 into the right HSM 16 through the gates 851 (FIG. 1(d-c)), as the gates 722 and 851 are also closed.

The first timing pulse T1 passed by the gate 942 (FIG. 1(b-e)) is also applied to the gate 740 (Follow the gate 740 output from (FIG. 1(b-e)) to FIG. 1(b-d) back to FIG. 1(b-e)) and through the gate 740 to the set terminal S of the first EM or ET flip-flop F706. Accordingly, the gates 609 or 610 (FIG. 1(b-d)) pass a high level to apply a pulse to stop tape A or tape B whichever was running.

T3

The "one" output of the first EM or ET flip-flop F706 (FIG. 1(b-e)) also primes the gate 732 (FIG. 1(b-b)). The third timing pulse T3 is passed by the gate 732 to set the second EM or ET flip-flop F702 (FIG. 1(b-c)).

T4

The fourth timing pulse is passed through the gate 901 (FIG. 1(b-d)) to reset the Y register 13 (FIG. 1(c-d)).

T8

As noted above, the address of the last message was staticized during the previous RO03 and has its 2^{10} (that is, eleventh order) bit a "one." Accordingly, the gate 733 (FIG. 1(b-b)) is primed by the "one" output terminal 2^{10} bit flip-flop from the C register 28 (FIG. 1(c-a)). Therefore, the eighth timing pulse T8 is passed by the gate 733 (FIG. 1(b-b)) to reset the "after first RE" flip-flop F703 (FIG. 1(b-b)). The address of the last item of the message was staticized during the previous high status level RO03 in the C register 28 (FIG. 1(c-a)). It is because this is the address of the last message, the eleventh bit (2^{10} bit) of the address is a binary "one." Accordingly, the 2^{10} bit flip-flop of the C register 28 (the eleventh bit) is set. In the operations which may follow, the "after first RE" flip-flop F703 is thus in its reset condition, in order, for example, that its "zero" output lead may prime a status transition gate 1277 (FIG. 1G) in preparation for an instruction surge. Recall that the drum line number of the next instruction to be surged from the drum was entered from the HSM 15, 16 to the A register 26 (FIG. 1(c-a)) and the B counter 11 (FIG. 1(d-b)) at the beginning of the operation read-in from tape, as part of the original instruction.

The gate 101 (FIG. 1(a-a)) is primed by the high "one" terminal of the second EM or ET flip-flop F702 (FIG. 1(b-c)) at two inputs, and by the high RI status level and the high 2^{10} bit flip-flop "one" output of the C register 28 (FIG. 1(c-a)) respectively at its other two inputs. Therefore, the gate 101 (FIG. 1(a-a)) is now open to pass the eighth timing pulse T8 to open the gates 102. The twelve bits entered in the A register 26 (FIG. 1(c-a)) and B counter 11 (FIG. 1(d-b)) are now entered in the program counter PC through the gates 102 (FIG. 1(a-a)). Accordingly, the program counter PC is set to the drum line number of the next instruction to be surged into the memory.

The status transition gate 1218 (FIG. 1H) now passes the eighth delayed timing pulse T8a to select the status level RE to be high. The next set of instructions are surged into the HSM 15, 16 in the manner described heretofore.

5.7.2.17.2 EM or ET and NOT Last Address

In this event, the end message symbol EM or end of tape symbol ET, does not coincide with the last item address. However, the EM or ET symbol is not to be read into, that is, entered into the memory. Instead, an ISS is to be read into the memory at the next address. In the same manner as for the high status level RI cycle previously described, as, for example, in sec. 5.7.2.17, the first timing pulse T1 is passed by the gate 942 (FIG. 1(b-d)) to the gate 485 to set the 2^{11} bit flip-flop of the C register

124

28 (FIG. 1(c-a)). Accordingly, the left and right HSM 15 and 16 (FIGS. 1(c-c) and 1(d-c)) cannot receive information. Note that, as before, the left read-in gate 721 (FIG. 1(c-c)) and the right read-in gate 850 (FIG. 1(d-c)) no longer receive a high voltage from the "zero" output terminal of the 2^{11} bit flip-flop of the C register 28. The gate 730 (FIG. 1(b-e)) also receives the first timing pulse T1 passed by the gate 942 (FIG. 1(b-e)). The gate 740 (FIG. 1(b-e)) passes the received pulse to set the first EM or ET flip-flop F706, as in the high status level RI cycle just described. The tapes are stopped by the pulse through the gates 609 and 610, as before. The minus L flip-flop F909 (FIG. 1(c-e)) is reset by the first timing pulse T1 passed by the gate 942 (FIG. 1(b-e)) and then the gate 936 primed by the high EM or ET lead from "or" circuits R920 to R921 (FIG. 1(b-d)). The tape minus flip-flop F701 (FIG. 1(b-d)) is also reset by the timing pulse T1 from the gate 936 (FIG. 1(b-e)).

The third timing pulse T3 passed through the gate 732 (FIG. 1(b-b)) to set the second EM or ET flip-flop F702 (FIG. 1(b-c)). Note, however, that the 2^{10} bit flip-flop of the C register 28 is in the reset condition because the last address is not entered therein. Accordingly, the status transition gate 1273 (FIG. 1G) is primed.

The status transition gate 1273 (FIG. 1G) passes the eighth delayed timing pulse T8a to select the status level RO03 to be high.

5.7.2.17.3 Status Level RO03 High—After Status Level RI and After EM or ET and NOT Last Item Address

The next item address is staticized in the same manner as in the previous high status level RO03, operation level N high. At the end of this status level RO03, the status level RI is selected to be high. Recall that the second EM or ET flip-flop F702 (FIG. 1(b-c)) is set. Status transition gate 1256 is therefore primed, and passes the eighth delayed timing pulse T8a to the "set RI" lead.

5.7.2.17.4 Status Level RI High—After Status Level RI High and After EM or ET and NOT Last Item Address

Note that when status level RI was previously high, after the EM symbol was first recognized (as in sec. 5.7.2.17.1), the gate 901 (FIG. 1(b-d)) was primed by the high status level RI and the high operation level N to pass the fourth timing pulse T4 to reset the Y register 13 (FIG. 1(c-d)). However, in the current status level RI high, the output of the "or" circuits R920 (FIG. 1(b-d)) is low, and the gate 485 (FIG. 1(b-d)) is not primed, because these "or" circuits receive the output of the register 13. Accordingly, as explained hereinbefore, the left or right HSM 15 or 16 may be activated for receiving information, since the 2^{11} bit flip-flop of the C register 28 (FIG. 1(c-a)) is in reset condition.

However, instead of receiving the contents of the Y register 13 (FIG. 1(c-d)), at the address staticized when the status level RO03 was last high, an ISS is artificially entered at this address. The gate 859 (FIG. 1(c-d)) is primed by the high "one" output of the second EM or ET flip-flop F702 (FIG. 1(b-c)). Note that this second EM or ET flip-flop F702 is set from the time an EM or ET symbol is indicated until the last address of the read-in operation is staticized and the read-in operation is completed.

The gate 859 (FIG. 1(c-d)) therefore passes the second timing pulse T2 to enter an item separation symbol (coded, for example, 0111 100) into the L and R registers 18 or 19 (FIGS. 1(b-c) and 1(d-c)) and thence into the left or right HSM 15 or 16. Note that although the gates 821 and the gates 825 are opened, they have no output because all of the Y register 13 "one" outputs are at a low level, the Y register 13 having been reset. The pulse from the gate 859 simply imposes a high level on the 2^3 to 2^5 bit leads. The write-in from the L and R registers

18 and 19 is accomplished in the same manner as in the RI cycles previously described.

After the ISS is read into the left or high HSM 15 or 16, the second EM or ET flip-flop F702 (FIG. 1(b-c)) remains in its set condition until the status level RO01 is again high. The 2¹⁰ bit flip-flop of the C register 28 is in reset condition because, as has been assumed, the EM symbol did not coincide with the last address. The RI status level is also high. Therefore, the status transition gate 1273 (FIG. 1G) is primed to pass the eighth delayed timing pulse T8a. The status level RO03 is now selected to become high.

A new address is now withdrawn from the next location in the surge section and staticized during the cycle in which the status level RO03 high. The second EM or ET flip-flop F702 (FIG. 1(b-c)) is still in its set condition. Therefore the status transition gate 1256 (FIG. 1G) is primed to pass the eighth delayed timing pulse T8a to the "set RI" lead. The status level RI now becomes high. If the new address is not the last address of the program, an ISS is again artificially read into the left or right HSM 15, 16.

Finally, in the status level RO03, the last address of the program is staticized in the C register 28 (FIG. 1(c-a)). The 2¹⁰ bit flip-flop of the C register 28 is in its set condition. The gate 101 (FIG. 1(a-a)) is primed to pass the eighth timing pulse T8 and open the gates 102 to again enter into the program counter PC the drum line number of the next instruction to be surged into the memory. The manner in which this drum line number is entered is similar to that described above, in connection with the case in which the EM symbol is recognized and at the same time the last item address is entered in the C register 28 (sec. 5.7.2.17.1).

As described before, the status transition gate 1218 (FIG. 1H) passes the eighth delayed timing pulse T8a to cause the status level RE to be high.

5.7.2.18 Status Level RI High With End of Tape Symbol

If the left symbol recognition circuits 22 detect an end tape (ET) symbol stored in the Y register 13 (FIG. 1(c-d)) the output of the "or" circuits R921 (ET lead) is high. The first timing pulse T1 passes through the gate 942 (FIG. 1(b-e)). The gate 942 output then passes through the gate 740 (FIG. 1(b-e)) to set the first EM or ET flip-flop F706. Note that the gate 485 (FIG. 1(b-d)) is not open. The third timing pulse T3 is then passed through the gate 732 (FIG. 1(b-b)) now primed, to set the second EM or ET flip-flop F702 (FIG. 1(b-c)). Note also that the status transition gate 1218 (FIG. 1H) is not primed, because the last address has not been reached and the 2¹⁰ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in reset condition. The high output of the first EM or ET flip-flop F706 "one" output is applied to the gates 609 and 610 (FIG. 1(b-d)). Therefore, the tapes are stopped. Either a new tape should be started, or the end tape ET symbol is inserted at the wrong place on the tape.

It is contemplated that the ET symbol immediately follow an EM symbol after the last message on a tape. Therefore, such a situation (resulting in the stopped tapes) normally follows immediately after a surge of addresses. After the surge, the selected tape is started in the manner already described. The high "one" output of the first EM or ET flip-flop F706 (FIG. 5), because of the pulse through gate 609 or 610 of FIG. 2, causes whichever tape is started to be stopped immediately. The 2¹¹ bit flip-flop of the C register 28 (FIG. 3) is in its reset condition because that stage was reset during the address surge. The EM symbol is now read into the memory from the Y register 13 (FIG. 5), as any character would be, in the manner already described.

The status transition gate 1273 now passes the eighth delayed timing pulse T8a to the "set RO03" lead. A new address is withdrawn, and either the last address is read

out, as described in sec. 5.7.2.7 above, or repeated cycles of status levels RI and RO03 follow, and ISS's are artificially entered at the excess addresses, if any, until the last address is withdrawn, as described in sec. 5.7.2.15, above.

After the last address is withdrawn, the status transition gate 1218 of FIG. 6 passes the eighth delayed timing pulse T8a to cause the status level RE to be high. The next set of instructions are surged into the HSM 15, 16 as previously mentioned, and may be programmed to operate upon the information just entered into the memory from the tape. If desired, a suitable recognition circuit may respond to the ET symbol, to sound an alarm, or cause the machine to stop. However, the ET symbol may also be recognized by suitable programming. For example, the subsequent instructions may be such that a conditional transfer of control to the machine instruction "stop" ensues if an ET symbol is at the first address of any group, by virtue of a suitable sub-routine.

5.7.3 Sequence of Status Levels—Operation N

It is of interest to notice that the instruction for reading in from tape may be considered as composed of one operation and $n+2$ addresses, where n is the number of addresses surged into the memory section. As the instruction is performed, the n items are stored at the n addresses of the instruction, the other two addresses serving, respectively, to indicate the drum line where the sequence of n addresses may be started and the drum line for the next instruction after the operation is completed.

If the last address at which the item is to be placed is in the right HSM 16, the tenth order (2⁹ bit) of the binary coded address is a "one." If the last address where the last item is to be placed is in the left HSM 15, then the tenth bit (2⁹ bit) is a zero.

The last of the addresses to be surged from the drum is indicated in the coding by placing a unit or binary "one" in the eleventh (ignoring parity) bit (that is, the 2¹⁰, or eleventh order information bit) of the last address. Thus this 2¹⁰ bit, redundant for addressing, is used to indicate the occurrence of the last address.

The operation "read-in from tape" (N) is employed to read into the computer messages from the magnetic tape. Any new message is to be read into the computer memory item by item, the items being placed at addresses specified on the drum and beginning with the address specified on the drum line in the C section of the instruction. It is assumed that the maximum number of items in each message is the same. A specific maximum number of characters is assumed for each item. However, this is a non-standard maximum, which is subject to choice by the operator. Thus, an address for a specific item implies that it is the location of the item separation symbol, and that the remaining characters of the item are stored in successively lower addresses. Consecutive items of the message may or may not be stored in adjacent locations in the HSM 15, 16. The maximum number of items may differ from message to message.

Refer also to the status level flow diagram FIG. 18, as well as to FIG. 1. The first step is the staticizing of the instruction read-in from tape (N) by the sequence of RO01, RO02, RO03 high status levels. The instruction for selecting the operation level N to be high is transferred to the O register 30 (FIG. 1(b-a)) during the high status level RO01. The operation level N is then made high by means of the operation matrix OM. The remainder of the instruction is entered, as previously described, in the A register 26 (FIG. 1(c-a)) the C register 28 and the A, B and C counters 10, 11 and 12 (FIGS. 1(c-b), 1(d-b), and 1(c-b)) respectively. The next status level selected as high is RE.

The machine searches for the drum line indicated by the C address of the instruction. This drum line contains the first item address. The machine locates the line and then surges that line and subsequent alternate lines on the drum into the HSM 15, 16 into the surge

tank at locations automatically prescribed by the program subcounter PSC. These locations (addresses) at which the item addresses are stored start at zero in the present machine. The surge of addresses stops when the last address code is recognized by the coding, because the address of the last item is coded with the 2^{10} bit as a binary "one."

The machine then selects the status level RO03 to be high and the tape is started. Note that there is a difference between the high status level RE with the high operation level N, and the status level RE for a surge without the status level N being high. The RE status level high with the operation level N high ends with a coded drum line. The surge of instructions (previously described) ends at a prescribed program subcounter PSC (FIG. 1(a-b)) count.

The address stored in the memory for the first character of the incoming message is staticized or stored in the various registers while the status level RO03 is high. The machine then selects the status level RD to be high and cycles (that is, the timing pulses continue their cycles without a different status level becoming high) until the first character is read from tape. The first character normally should be a start message EM symbol. The status level RI is now selected.

The start message (SM) symbol or first character is read into the HSM 15, 16 at the first address withdrawn from the memory HSM 15, 16. The status level RD is now selected to be high and the machine again cycles waiting for the next character. If another character, alphabetic or numeric, is received, it is read into the address one lower than the location of the SM symbol. If an ISS (item separation symbol) is read from the tape, then the address of the next item to be read from the tape is withdrawn from the memory surge tank section and staticized, that is, stored in the registers. When the status level RI is high, the ISS is then read into the second data item address.

The machine again selects the status level RD to be high, waits for, and receives and staticizes the next character. Then the status level RI is high and the machine reads the next character after the item separation symbol into the next address location. Note that the first item in the most significant address portion (or that corresponding to the largest number) is an item separation symbol ISS. In continuing steps of (a) cycling in RD, and (b) reading into the memory during an RI cycle, the succeeding characters are entered in successive memory places. The detection of an ISS symbol during an RD cycle indicates that the second item is completely read and another item should now be read from the tape and its characters stored at their assigned address. The machine then returns to the high status level RO03, reads an ISS into the next address location, and succeeding characters into locations successively lower in order (that is, corresponding to successively lower numbers).

If an item contains no data, two consecutive ISS's appear on the tape. The first ISS is stored in the HSM 15, 16 at the location called for by the next address, during the high status level RI, as described above. The machine then goes to the high status level RD. The next character that appears is another ISS. The status level RO03 is now selected to be high, so that the address of the next item to be stored is entered in the various registers. Thereupon an ISS is entered at the address of this item, during the succeeding high status level RI.

After the last item in the message, an end of message EM symbol occurs. The symbol is not written into the HSM 15, 16. An address is programmed for every item in a message. Therefore, the items preferably are arranged in the message so that those which most often contain data are in the most significant part of the message, and are read from the tape first. The EM symbol occurs after the last item in the message that contains

data. The tape space is thus conserved. However, it is possible for consecutive items at the end of the message to be omitted. The addresses of these items, if omitted, have been surged into the HSM 15, 16.

The end message (EM) symbol is detected in the high status level RD. The machine then selects the status level RI to be high. During the high status level RI, the end message (EM) symbol is discarded. At this point, if all the items called for in the message have been entered, the machine re-enters in the program counter PC the drum line of the next instruction, which had been held in temporary storage, and then selects the status level RE to be high. The drum line of the next instruction required in the program to operate on the various data was entered in the A register 26 and part of the B counter 11 during the staticizing of the instruction for read-in from tape, operation N. When the status level RE is now high, the machine searches the drum for the drum line of the next instruction and then surges a group of instructions into the HSM 15, 16 as in the surge operation described hereinbefore.

If however, one or more items are missing at the end of the message (that is, the program calls for various items which are not found on the tape) the machine selects the status level RO03 to be high. With the status level RO03 high, the next item address is staticized. The machine then enters the high status level RI, and an item separation symbol ISS is artificially placed in the staticized memory location of the missing data item. If the last data item address has still not appeared, the machine continues in a reiterated RO03-RI sequence. In this sequence the machine reads out consecutive data item addresses and artificially places an ISS in the memory location of each missing data item. When the last data item address is detected, the machine selects the status level RE to be high. With the high status level RE, the program instructions are surged from the program drum into the HSM 15, 16 as noted above. When the surge is completed, the machine selects the status level RO01 to be high, and begins operating on the data now in the memory in the manner heretofore described.

The instruction "read-in from tape" (Operation N) may be employed by a programmer to place as many extra item separation symbols (ISS's) as he desires by adding extra addresses for these symbols on the drum after the addresses of all the items to be read from the tape. Additional programming flexibility is thus secured.

All items on tape are preceded by an item separation symbol ISS except for the start message symbol SM. Therefore, when an item is written from the tape into the HSM 15, 16, the ISS is written also. This ISS is placed in the staticized address of the item location in the HSM 15, 16. When these items are operated upon and the results placed back in the HSM 15, 16 result locations, there is no ISS in the first character of the item. However, because the address allocated for the highest order binary coded digit or character for the result is known, an item separation symbol ISS can be artificially placed in the next higher location during the read-in operation preparatory to performing the program.

To thus obtain the entry of the desired item separation symbols ISS, note that the number of item addresses placed on the drum may correspond to the maximum number of items in the tape message. The addresses of the HSM 15, 16 locations for the ISS's of the result items may be placed after the data item addresses on the drum. The last item address to be surged from the drum into the HSM 15, 16 is indicated by the 2^{10} (eleventh) bit of the item address being a binary one. The situation is the same as that where the number of data items on the tape are less than the number of item addresses. As far as the machine is concerned, there are more data item addresses than data items, and ISS is placed in the HSM 15, 16 location specified by each address that does not have an item corresponding to it on the tape. These

entries are continued until the final address is detected by reason of the address coding, and the 2^{10} bit flip-flop of the C register 28 is set.

5.8 Write-Out to Tape (Operation W)—Operation Level W High

5.8.1 Additional Components

Certain additional components are employed in carrying out this instruction. A pair of three-input gates 603 and 604 (FIG. 1(b-d)) are assigned respectively to a pair of output tapes, tape C and tape D. Each of the gates 603 and 604 receives one input from the operation levels W or H applied through an "or" circuit (not shown). The gates 603 and 604 each receives as a second input the status level RO03. The third input to each of the gates 603 and 604 is from the "one" and "zero" terminals respectively of the tape selector flip-flop F601 (FIG. 1(b-c)). The output of the gate 603 (FIG. 1(b-d)) applies a start pulse to start the tape drive mechanism of output tape C. The output of the gate 604 applies a start pulse to the start tape mechanism of the output tape D.

A pair of two-input gates 607 and 608 are provided (FIG. 1(b-d)) respectively for each of the output tapes C and D. The outputs of the gates 607 and 608 apply stop pulses respectively to the tape drive mechanism of tapes C and D. One of the inputs to each of these gates 607 and 608 is from the high status level IC (instruction complete). The other inputs to the gates 607 and 608 are, respectively, from the "one" and "zero" output terminals of the tape selector flip-flop F601 (FIG. 1(b-c)).

A three-input gate 556 (FIG. 1(d-b)) receives as one input the status level RO03. A second input to the gate 556 is from the operation levels W and H applied through a suitable "or" circuit. The third input to the gate 556 is the first timing pulse T1. The output of the gate 556 is applied through a suitable "or" circuit to the reset terminals R of the B counter 11 to reset all the flip-flops of the B counter 11.

A three-input status transition gate 1230 (FIG. 1H) has as one input the output of an "or" circuit receiving the status levels RO03 and RIS. A second input to the status transition gate 1230 is from the operation levels W and H applied through an "or" circuit. The third input to the status transition gate 1230 is the eighth delayed timing pulse T8a. The output of the gate 1230 is applied through an "or" circuit to the "set RD" lead.

A character spacing counter 34 (FIG. 1(e-d)) is provided made up of three flip-flops, ordered from 2^0 to 2^2 bit flip-flop. The character spacing counter 34 has a trigger terminal T, for example, a trigger terminal of the 2^0 stage to which pulses may be applied to advance the counter by one for each pulse. The output of a four-input gate 866 is applied to the trigger terminal T of the character spacing counter 34. One input to the gate 866 is from the status level RD. A second input is from the operation levels W and H applied through a suitable "or" circuit. A third input is from the "zero" terminal of a tape-write flip-flop F801 (FIG. 1(e-e)). The fourth input to the gate 866 (FIG. 1(e-d)) is the output of a gate 867. The inputs to the gates 867 are seven in number. Six of the inputs to the gate 867 are from the six "one" output terminals of the 2^3 to the 2^8 bit flip-flops of the B counter 11 (FIG. 1(d-b)). The seventh input to the gate 867 (FIG. 1(e-d)) is from the sixth timing pulse T6. A three-input gate 864 has its output connected to the reset terminal R of the character spacing counter 34. A first input to the gate 864 is from either high one of the status levels RO01 or RD applied through a suitable "or" circuit. A second input to the gate 864 is from the high one of the "zero" output terminal of the tape-write flip-flop F801 (FIG. 1(e-e)), or the status level RO01 applied through a suitable "or" circuit,

as shown. The third input to the gate 864 (FIG. 1(e-d)) is the seventh timing pulse T7.

The "one" output terminal of the 2^1 bit (second order) flip-flop of the character spacing counter 34 (FIG. 1(e-d)) is connected to one input of a four-input gate 865 (FIG. 1(e-e)). A second input to the gate 865 comes from the "one" output of the first order or 2^0 bit flip-flop of the character spacing counter 34. A third input to the gate 865 is from the high operation level W or H applied through a suitable "or" circuit. The fourth input to the gate 865 is the fifth timing pulse T5.

A four-input status transition gate 1267 (FIG. 1G) is provided. Two of these inputs are received respectively from the "one" output terminals of the first and second bit flip-flops of the character spacing counter 34 (FIG. 1). These are the same two outputs of the character spacing counter 34 applied to the gate 865. However, the "one" output of the 2^0 bit flip-flop of the character spacing counter 34 is applied through an "c" circuit having an input from the operation level H. A third input to the status transition gate 1267 is from the operation level RD. The fourth input to the status transition gate 1267 is from the eighth delayed timing pulse T8a. The output of the status translation gate 1267 is applied to the "set RO" lead.

The output of the gate 865 (FIG. 1(e-e)) is applied to the set terminal S of the tape-write flip-flop F801.

The "one" output terminal of the tape-write flip-flop F801 is applied through a suitable "or" circuit to the same input of the gate 864 (FIG. 1(e-d)) which does not receive the status level RD. Accordingly, the gate 864 is primed by a high status level RO01 or by the set condition of the tape-write flip-flop F801 (FIG. 1(e-e)) in conjunction with high status level RD. The "one" output terminal of the tape-write flip-flop F801 is also connected as one input each gate of two sets each of seven gates 620 and 613 (FIG. 1(d-d)).

Each of the gates 613 and 620 is a five-input gate. The second input to each of these gates is from the status level RD. A third input to each of these gates comes from the operation levels W or H applied through a suitable "or" circuit. The set of gates 613 receives a fourth input from the "one" output terminal of the tape selector flip-flop F601 (FIG. 1(b-c)). The set of gates 620 (FIG. 1(d-d)) each has as its fourth input the "zero" output of the tape selector flip-flop F601 (FIG. 1(b-c)). The fifth input to each gate of the set of gates 613 (FIG. 1(d-d)) is from the respective "one" output terminals of the Z register 14 flip-flops. The fifth input to each of the gates of the second set 620 is also from the "one" output terminals of the flip-flops, respectively, of the Z register 14. The outputs of the first set of gates 613 are applied respectively to the seven writing heads of the output tape C. The different outputs from the gates 620 are applied respectively to the writing heads of the output tape D. Thus the sets of gates 620 and 613 are connected between the Z register 14 output and the reading heads of tape D and C respectively.

The second equal circuit 35 (FIG. 1(c-b)) has its output applied to the set terminal S of an address equal flip-flop F301 (FIG. 1(b-b)). A two-input gate 329 (FIG. 1(b-b)) is provided having as one input the status level RO03 and as the second input the fourth timing pulse T4. The output of the gate 329 is applied to the reset terminal R of the address equal flip-flop F301.

The "one" output terminal of the address equal flip-flop F301 is applied as an input to a four-input status transition gate 1204 (FIG. 1H). The status transition gate 1204 has a second input from the status level RD. A third input to the status transition gate 1204 is from the operation level W or H applied through a suitable "or" circuit. The fourth input to the status transition gate 1204 is from the eighth delayed timing pulse T8a.

131

The output of the status transition gate 1204 is applied through "or" circuits to the "set IC" lead.

A status transition gate 1225 is provided (FIG. 1H). The status transition gate 1225 has three inputs, one from the operation level W, a second from the status level RO, and the third input from the eighth delayed timing pulse T8a. The output of the status transition gate 1225 is applied to the "set RD" lead.

Two gates 695 and 697 (FIG. 1(c-b)) are provided each having four inputs. One input to each of the gates 695 and 697 is from an "or" circuit receiving the status levels W, K, H, J, E, or X. A second input to each of the gates 695 and 697 is from status levels RO, RS, or RIS applied through an "or" circuit. A third input to the gate 695 is from the "one" output of the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)), and the third input to the gate 697 (FIG. 1(c-b)) is from the "zero" output of the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)). The fourth input to each of the gates 695 and 697 is the first timing pulse T1. The output of the gate 695 is applied through an "or" circuit to prime the gates 650; and the output of the gate 695 is applied through "or" circuits to prime the gate 660.

A three-input gate 304 (FIG. 1(c-b)) has an output applied through "or" circuits to the trigger terminal T of the C counter 12. The first input to the gate 304 is the high operation levels W and X applied through an "or" circuit. The second and third inputs to the gate 304 are, respectively, the status level RO and the second timing pulse T2.

A set of five two-input gates 931 have their outputs applied through "or" circuits to those respective inputs of the nine complementor 21 which receive the outputs of the right HSM 16. The outputs of the left HSM 15 are applied respectively as one set of inputs to the gates 931. The second input to each of the gates 931 is from the output of an "or" circuit to which are applied the operation levels W and H.

A two-input gate G15 has its output applied through that "or" circuit which receives the output of the gate G16 to the parity generator PG. One input to the gate G15 is from the operation levels W and H applied to an "or" circuit, and the second input to the gate G15 is from the sixth timing pulse T6.

A four-input gate 1022 (FIG. 1(d-d)) has as one input the "zero" output of the end of operand right flip-flop F1010. A second input to the gate 1022 (FIG. 1(d-d)) is the high operation levels W or H applied through an "or" circuit. A third input to the gate 1022 is the status level RO. The fourth input to the gate 1022 is the sixth timing pulse T6. The output of the gate 1022 primes each of a set of seven, two-input gates 1023. The gates 1023 receives respectively the seven outputs from the left or right HSM 15 or 16, whichever is activated for read-out, by the left and right HSM 15 and 16 output applied through "or" circuits, indicated on FIG. 1(d-c)) by the convention adopted herein and by the reference numeral 64. The seven outputs of the gates 1023 (FIG. 1(d-d)) are applied respectively through "or" circuits to the respective set terminals S of the Z register 17.

A four-input gate 1014 (FIG. 1(e-c)) has one input from the "one" output terminal of the end of operand right flip-flop F1010 (FIG. 1(d-e)). A second input to the gate 1014 (FIG. 1(e-c)) is from the status level RO; and a third input is from the output of an "or" circuit having inputs from the two operation levels W and H. The fourth input to the gate 1014 is the timing pulse designated T6½. The output from the gate 1014 is applied to each of a set of seven gates 1015. The two-input gates 1015 correspond to the 2⁰ to 2⁶ bits of a coded character. Four bits (corresponding to the 2⁰ to 2³ bits) are received from the complementor 21. The 2⁴ and 2⁵ bits are received from "or" circuits, each of which has one input from the 2⁴ and 2⁵ bits of the left HSM 15 output and the

132

other inputs from the 2⁴ and 2⁵ bits of the right HSM 16. The 2⁶ bit input for the corresponding gate of the gates 1015 is from the parity generator PG (FIG. 1(d-d)). The outputs of the gates 1015 are applied through "or" circuits to the respective set terminals S of the Z register 14 (FIG. 1(d-d)).

A four-input gate 1066 (FIG. 1(d-d)) has one input from the ISSM lead (FIG. 1(d-e)); a second input from the end of operand right flip-flop F1010 "one" terminal (FIG. 1(d-e)); a third input from an "or" circuit receiving high operation levels W and H; and the fourth input from the first timing pulse T1. The output of the gate 1066 (FIG. 1(d-d)) is applied through "or" circuits to the reset terminals of the 2⁹ and 2⁸ bit flip-flops only of the Z register 14 (FIG. 1(d-d)) as indicated by legend, although without the legend it might appear that the output of gate 1066 is applied through the "or" circuits to reset all the stages of the Z register 14. The output of the gate 1066 is also applied to set the 2³ bit flip-flop only of the Z register 14. This application of the output of the gate 1066 is set the third order (2³ bit) flip-flop only of the Z register 14 is also indicated by legend, although without the legend it might appear that the output of the gate 1066 is applied to all the various set terminals of the Z register 14. The output of the gate 1066 (FIG. 1(d-d)) is also applied, through an "or" circuit to reset the end of operand right flip-flop F1010 (FIG. 1(d-e)).

5.8.2 Operation Level W High

After staticizing the instruction during the high status levels RO01, RO02, and RO03, the instruction "write-out to tape," W is arranged as follows:

FFR-O	A Counter	B Counter	C Counter
"Write-out" Instruction Code.	Address, minus one, of last character to be written out.	Tape Identification Number.	Address of first character to be written out.

Note however, that as soon as the entry is made to the O register in RO01, in the usual manner, the operation level W is selected by the operation matrix OM to be high. Accordingly, certain additional steps take place in RO02 and RO03 during the staticizing of the remainder of the instruction.

5.8.2.1 Status Level RO02 High (staticizing)

During the high status level RO02, in writing out to tape, note that at the eight timing pulse T8, the tape selector flip-flop F601 (FIG. 1(b-c)) is in its set or reset condition in accordance with whether the 2⁰ or 2¹ bit flip-flop in the B counter 11 (FIG. 1(d-b)) is set. If the 2⁰ bit flip-flop in the B counter 11 is set, then the gate 601 (FIG. 1(b-c)) is primed to pass the eight timing pulse T8 to the set terminal S of the tape selector flip-flop F601. If, on the other hand, the 2¹ bit flip-flop of the B counter 11 (FIG. 1(d-b)) is set, then the gate 602 (FIG. 1(b-c)) passes the eighth timing pulse T8 to reset the tape selector flip-flop F601. Therefore, the gate 603 or 604 (FIG. 1(b-d)) is primed depending on whether the tape selector flip-flop F601 (FIG. 1(b-c)) is in its set condition, and the programmer must take care to that end in coding the instruction. The tape selector flip-flop F601 (FIG. 1(b-c)) retains its initial set or reset condition throughout the entire time of the remainder of the operation write-out to tape, with the high operation level W.

Therefore, when the instruction is completed and the status level IC becomes high, the gate 608 passes the high level to stop tape C, if tape C is running; and the high level output of gate 608, when status level IC becomes high, stops tape D if tape D is running.

The status transition gate 1275 passes the eighth delayed timing pulse T8a to select the status level RO03 to be high.

5.8.2.2. Status Level RO03 High (staticizing)

The gate 603 or 604 (FIG. 1(b-d)) respectively, depending on the condition of the tape selector flip-flop F601 (FIG. 1(b-c)) passes the status level RO03 as a high level to start tape C or D.

The B counter 11 (FIG. 1(d-b)) is reset by the first timing pulse T1 passed through the gate 556. Note that the condition of the tape selector flip-flop F601 (FIG. 1(b-c)) depending on the previous condition of the 2⁰ or 2¹ bit flip-flop of the B counter 11 (FIG. 1(b-c)), now cleared. The address equal flip-flop F301 is reset by the fourth timing pulse T4 passed by the gate 329.

The gate 313 (FIG. 1) passes the eighth timing pulse T8 to the set terminal of the reversing flip-flop F302 (FIG. 1(c-b)). With the flip-flop F302 in its set condition, the C counter 12 in its negative counting state.

The status transition gate 1230 (FIG. 1H) passes the eighth delayed timing pulse T8a to the "set RD" lead. The status level RD becomes high.

5.8.2.3 Status Level RD High

The operation is such that the machine now allows time for the tape to come up to speed. Note that the characters ought to be spaced on the tape at about one-hundred microsecond intervals in time in order to suitably separate them in distance on the output tape, at the tape speeds here assumed. However, other spacings and other tape speeds could be readily accommodated with only minor variations as will be apparent to those skilled in the art, from this description.

The gate 555 (FIG. 1(d-b)) passes the second timing pulse T2 to the trigger terminal T of the B counter 11 (FIG. 1(d-b)). The count of the B counter 11, which was reset during the high status level RO03, is now advanced one. The machine keeps the status level RD high. During the next cycle of timing pulses, at T2, the B counter 11 count is again advanced one. There are five-hundred four RD cycles at twenty microseconds each between the first timing pulse after status level RD first becomes high until the 2³ to 2⁸ bit flip-flops (inclusive) in the B counter 11 are all in the set condition at the same time. Therefore, the five-hundred four cycles in RD take approximately ten milliseconds, by which time the tape is at full speed. It is clear that, if desired, other than a ten millisecond time allowance could be provided for the purpose. In the next cycle of timing pulses, with the status level RD high (this will be the five-hundred and fifth such cycle since the first unit count was added to the B counter 11 count), the gate 555 (FIG. 1(d-b)) is not primed by any input from the B counter 11. The gate 867 (FIG. 1(e-d)), however, is primed and now passes the sixth timing pulse T6 to the gate 866, which is also primed and passes the pulse T6 to the trigger terminal T of the character spacing counter 34. The count of the character spacing counter 34, which was reset in the previous RO01 cycle by the seventh timing pulse T7 applied through the gate 864, is then advanced by one. Note that the gate 866 was primed by the high status level RD and also the high level from the "zero" output terminal of the tape-write flip-flop F801 (FIG. 1(e-e)). The tape-write flip-flop F801 is reset at every time cycle at the timing pulse designated T7b between the seventh T7 and before the eighth T8.

In the next RD cycle (the five-hundred and sixth) the character spacing counter 34 (FIG. 1(e-d)) again receives the sixth timing pulse T6 passed through the gates 867 and 866. Accordingly, the character spacing counter 34 is advanced to a count of two.

During the next cycle of high status level RD (the five-hundred and seventh) the character spacing counter 34 is advanced to a count of three in the same manner.

At the count of three in the character spacing counter 34, the 2¹ and 2⁰ bit flip-flops respectively of that counter are each in the set condition. Therefore, the status transition gate 1267 passes the eighth delayed timing pulse T8a to select the status level RO to be high.

5.8.2.4 Status Level RO High

If the character to be read out of the tape is in the right HSM 16, (FIG. 1(d-c)), the 2⁰ bit flip-flop in the C register 28 (FIG. 1(c-a)) is set. Therefore, the gate 695 passes the first timing pulse T1 to open the gates 660 (FIG. 1(c-b)), so that the right HSM 16 is addressed by the contents of the C counter 12. Note that more than two output tapes could be readily accommodated (compare comment in sec. 5.7.2.2).

If the character to be read out to tape is in the left HSM 15, the 2⁰ bit flip-flop in the C register 28 (FIG. 1(c-a)) is in the reset condition. Accordingly, the gates 697 passes the first timing pulse T1 to open the gates 650, and the contents of the C counter 12 address the left HSM 15. The gate 304 passes the second timing pulse T2 to the trigger terminal T of the C counter 12. As the C counter 12 is in its negative counting state, the count in the C counter 12 is reduced by one, and the C counter 12 now holds address of next lower numbered location in the HSM 15 or 16.

The gate 1043 (FIG. 1(d-d)) primed by the high status level RO and the high operation level W, passes the fourth timing pulse T4 through the delay circuit D56 to reset the Z register 14.

The left read-out gate 730 (FIG. 1(c-c)) or the right read-out gate 862 (FIG. 1(d-c)) is opened, depending on whether the 2⁰ bit flip-flop of the C register 28 is in the reset or set condition respectively.

The sixth timing pulse T6 is passed through the gate 1022 to open the gates 1023 and pass into the Z register 14 the contents of the left HSM 15 or the right HSM 16.

The status transition gate 1226 (FIG. 1H) passes the eighth delayed timing pulse T8a to the "set RD" lead. Accordingly, the status level RD is now selected to be high.

5.8.2.5 Status Level RD High

At this point the character spacing counter 34 (FIG. 1(e-d)) still holds the count of three, with each of its 2⁰ and 2¹ bit flip-flops in the set condition. Accordingly, the gate 865 (FIG. 1(e-e)) is primed and passes the fifth timing pulse T5 to set the tape-write flip-flop F801. If the tape selector flip-flop F601 (FIG. 1(b-c)) was in its reset condition, indicating selection of tape D, then the gates 620 (FIG. 1(d-d)) are opened by the "one" high terminal of the tape write flip-flop F801 (FIG. 1(e-e)). The contents of the Z register 14 (FIG. 1(d-d)) are then applied to the write heads of tape D. If the tape selector flip-flop F601 (FIG. 1(b-c)) was in its set condition, the gates 613 (FIG. 1(d-d)) are opened to apply the contents of the Z register 14 to the write heads of tape C.

The gate 864 (FIG. 1(e-d)) is also primed by the high output from the "one" terminal from the tape-write flip-flop F801 (FIG. 1(e-e)). The gate 864 passes the seventh timing pulse T7 to reset the character spacing counter 34 (FIG. 1(e-d)). At the delayed seventh timing pulse designated T7b, the tape-write flip-flop F801 (FIG. 1(e-e)) is reset, removing the high level from the gate 620 (FIG. 1(d-d)) and the gates 613. Thus the gates 613 and the gates 620 are open from about the fifth timing pulse T5 to a little after the seventh timing pulse T7, a time of about 7½ micro-seconds.

135

The machine now continues repetitively in the following sequence:

- Three RD Cycles----- The Character Spacing Counter 34 (FIG. 1(e-d)) counts to 3.
 One RO Cycle----- The character is read out of the HSM 15, 16 into the Z register 14.
 One RD Cycle----- The character is read from the Z register 14 out to the tape.

This sequence is repeated until the status transition gate 1204 (FIG. 1H) is opened to cause the next status level to be high.

Note that the A counter 10 (FIG. 1(c-b)) holds the address, less one, of the final character to be written on the tape, staticized there when the instruction was staticized. The C counter 12 holds the address of the character that is currently being written out to the tape. When the addresses of the A counter 10 and the C counter 12 are equal, the second equal circuit 35 (also FIG. 1(c-b)) passes a pulse at the first timing pulse T1 to the set terminal S of the address equal flip-flop F201 (FIG. 1(b-b)).

The status transition gate 1204 (FIG. 1H) is then primed to pass the eighth delayed timing pulse T8a to the "set IC" lead. The status transition gate 1204 causes the selection of the status level IC to be high.

5.8.2.6 Negative Numbers

The first character of any negative item after the item separation symbol is a minus symbol. The minus symbol is written out of the HSM 15, 16 in the high status level RO to the Z register 14. The "or" circuits R1053 (FIG. 1(d-d)) causes the NOT SPMR lead to be low. The space minus right SPMR lead from the inverter I14 is therefore high, to prime the gate 1064 (FIG. 1(d-e)). The eighth timing pulse T8 is passed by the gate 1064 to set the end of operand right flip-flop F1010. The "one" output terminal of the end of operand right flip-flop F1010 is therefore high to prime gate G1014. Accordingly, the timing pulse between the sixth and seventh designated T6½ opens the gates 1015. At the same time, due to the set condition of the end of operand right flip-flop F1010 (FIG. 1(d-e)), the gate 1022 (FIG. 1(d-d)) is closed, and the gate 1023 cannot pass the contents of the left or right HSM 15 or 16 to the Z register 14. Instead, the gates 1015 (FIG. 1(d-d)) are opened by the pulse T6½ through the gate 1014 to pass the output of the nines complementor 21 into the Z register 14. Note that the output of the nines complementor 21 is five bits taken directly from the left HSM 15 or the right HSM 16, whichever is activated for read-out. The four bits of output from the nines complementor 21 is applied to the gates 1015, and particularly to the four bits designated 2⁰ to 2³ respectively of the gates. The 2⁵ and 2⁴ bits which respectively are "zero" and "one," (and the corresponding leads therefore low and high respectively) to designate (in this code) the fact that the output of the complementor is a numeral are applied from the left or right HSM 15 or 16, through "or" circuits, to the corresponding ones of the gates 1015. The seventh or parity bit is obtained from the parity generator PG and applied as the most significant bit (2⁶ bit) to the corresponding one of gates 1015. The outputs of the seven gates 1015 are applied to the respective set terminals S of the Z register 14, so that the Z register 14 holds the number ready to be written on the tape.

Note that the minus sign has been written directly on the tape from the Z register 14. In the next high status level RO, the complemented character passes through the nines complementor 21.

It should be understood that sensing of the minus sign

136

character (0001001) starts the action necessary for complementing the digits in the item which follow the minus symbol. An example of an item of this type is 0123- . . . The modified nine is utilized to represent the minus sign in the code employed. All digits following the modified nine are routed through the nines complementor 21 prior to setting the Z register 14. Note that the end of operand right flip-flop F1010 (FIG. 1(d-e)) now remains in the set condition during the time the succeeding numerals of the number are written out.

In the present machine, an EM character at the end of a negative item must be preceded by an ISS, otherwise the EM symbol is itself complemented. However, the programmer may see to it that the ISS follows a negative item preceding an EM. Also, the machine could readily be modified to avoid this possibility of complementing an EM symbol.

If a space character follows the modified nine, the complemented space symbol is not written on the tape. The space symbol (1000001) leaving the HSM 15, 16 is complemented and becomes the symbol (1001001). This latter seven bit coded symbol is called space minus, and is placed in the Z register 14. The contents of the Z register 14 are sensed by the "or" circuits R1053 which do not distinguish between the minus and space minus symbols, because they act only on the six "information" bits. The MR lead at the output of the "or" circuits R1053 is therefore at a low level. The inverter I14 causes the MR lead (FIG. 1(d-e)) to be high, to prime the gate 1099, as soon as the Z register 14 contents are entered (in high status level RO at T6½). The 2⁶ bit flip-flop "one" output terminal from the Z register 14 is also applied to the gate 1099. The last mentioned output is used to differentiate between the space minus and the minus symbol.

This seventh or 2⁶ bit is high, as prescribed by the code, for a space minus symbol. The recognition has taken place while in the status level RO. At the eighth delayed timing pulse T8a, the status level RD is selected by the status transition gate 1225 (FIG. 1H). The next first timing pulse T1 then passes through the gate 1099 and is applied (through a single "or" circuit) to reset only the 2³ bit flip-flop of the Z register 14 which contains the space minus character held therein. Thus in the high status level RD, at the first timing pulse T1, the change is made from space minus (1001001), to space (1000001), which in turn is written out to the tape just after the sixth timing pulse T6. The characters are not written out until after the change because the tape-write flip-flop F801 (FIG. 1(e-e)) is not set in order to prime the gates 620 or 613 (FIG. 1(d-d)) until the sixth timing pulse T6.

Referring back to the example of an item 0123- . . . , it would appear that the final ISS (Item separation symbol) also is complemented. The machine is arranged to inhibit the writing of this ISS minus (the complemented ISS) out to the tape, and to end the process of complementing characters following the ISS.

To prevent writing out the complement of the ISS to the tape, on the occurrence of an ISS following a minus sign, the output of the Z register 14 causes the output lead NOT ISSM of the "or" circuits R1055 (FIG. 1(d-d)) to be low. The output of the succeeding inverter I17 (FIG. 1(d-e)), the ISSM lead is high. The gate 1066 is therefore primed. Recall that the end of operand right flip-flop F1010 (FIG. 1(d-e)) is in its set condition. The gate 1066 (FIG. 1(d-d)) passes the first timing pulse T1, which is applied to set only the 2³ bit flip-flop in the Z register 14, and at the same time to reset the 2⁰ and 2⁶ bit flip-flop only of the Z register 14. The configuration of conditions of the flip-flops in the Z register 14 is now changed from that corresponding to ISS minus (0111001) to that corresponding to ISS (0111100). The gate 1066 also resets the end of operand right flip-flop F1010 (FIG. 1(d-e)).

The change in the contents of the Z register 14 occurs at the first timing pulse T1 of the high status level RD. In the high status level RD, the ISS is sensed and written out to the tape.

After the write-out, the status level RD remains high until the character spacing counter count again reaches three. The change to RO is again made for the purpose of reading out the first character of the next item, which is not read out through the complementor. If this first character is a minus symbol, the remaining characters of the item are complemented.

As the last character of the item at the last address is read out to tape with status level RD high, the status transition gate 1204 (FIG. 1H), primed by the second equal circuit 34 (FIG. 1(d-b)), passes the eighth delayed timing pulse T8a to the "set IC" lead, and the status level IC becomes high.

5.8.3 Sequence of Status Levels

The instruction for write out to tape causes data to be read out from only one side of the HSM 15, 16, that is, either the left or the right. The location of the most significant (corresponding to the highest numerical order on identification) character in the HSM 15, 16 is read out first, and then successively lower locations, until the required number of locations have been read. One of a plurality, in this instance two, tapes may receive the characters being read out, the required tape being specified in the instruction.

The tape is brought up to speed before any characters are written out. The delay is accomplished by counting the cycles of timing pulses on the B counter 11 (FIG. 1(d-b)) until all of the flip-flops corresponding to the 2⁸ to 2³ bits of the B counter 11 are in the set condition (approximately ten milliseconds) before reading out the first character. The characters are spaced approximately one-hundred microseconds apart in time after the tape has reached speed, by arranging for five status transitions to occur (approximately twenty microseconds between each transition) between the writing of one character and the writing of the next character.

Positive numbers are written directly out to tape. Negative numbers are in their nines complement form in the HSM 15, 16, and are complemented before being written out to the tape.

With reference to FIG. 19, the instruction is staticized in RO01, RO02, and RO03. The machine then selects the status level RD to be high. The machine cycles in the status level RD high for approximately ten milliseconds, as described, so that the tape may be brought up to speed. In each cycle of timing pulses with the status level RD high, one is added to the B counter 11 count. When the appropriate count is reached, a character spacing counter is employed to have one added to it in each high status level RD cycle thereafter. After counting three cycles in the high status level RD on the character spacing counter, the machine selects the status level RO to be high. The character in the most significant HSM 15, 16 location is then read out to the Z register 14. The machine then selects the status level RD to be high, the character is read out to the tape, the character spacing counter is reset, and three more cycles in RD are counted, the status level RO becomes high to staticize the next character in the Z register 14, etc.

When the last character is read out to the tape, at the program address coded in advance, the status level IC becomes high.

5.9 Write-Out to Tape and Clear (Operation H)—Operation Level H High

The operation H is substantially a duplicate of operation W, except that additional status level RIS is made high, during which spaces are read into the addresses of the HSM 15, 16 from which the contents were written out to the tape. In this manner, these addresses are left

in a cleared condition. A few other minor differences in the two operations appear hereinafter.

5.9.1 Additional Components

A three-input gate 302 (FIG. 1(c-b)) has as one input the status level RIS; as a second input the high one of the four operation levels H, J, E, or K applied through a suitable "or" circuit; and as the third and final input the second timing pulse T2. The output of the gate 302 is applied through suitable "or" circuits to the trigger terminal T of the C counter 12 (FIG. 1(c-b)).

A gate 927 (FIG. 1(c-c)) and a gate 858 (FIG. 1(d-c)) are provided. The gates 792 and 858 are each two input gates. Each of these gates 729 and 858 has the status level RIS as one input. The other input for the gate 729 is from the output of the gate 721 (FIG. 1(c-c)). The second input for the gate 858 (FIG. 1(d-c)) is from the output of the gate 850. The output of the gate 729 (FIG. 1(c-c)) and 858 (FIG. 1(d-c)) each is divided into two leads. One lead is for the (first order) and the other is for the 2⁸ (seventh order) bit of information being read into the left or right HSM 15 or 16 respectively. The first and seventh bit outputs of the gate 729 (FIG. 1(c-c)) are applied to the left HSM 15. The first and seventh bits from the gate 858 (FIG. 1(d-c)) are applied as the first and seventh bit of information into the right HSM 16. Recall that in the code of this machine a space is (1000001).

5.9.2 Detailed Operation

In the operation write out to tape and clear, operation level H high, the steps followed are the same as those in the operation write-out to tape W. The instruction is staticized during the status levels RO01, RO02, RO03, as follows (see also FIG. 12):

O Section	A Section	B Section	C Section
Code for write out to tape and clear.	Address minus one of list (least significant character) to be written out.	Tape identification.	Address of first (most significant) character to be written out.

5.9.2.1 Initiating Operation

After staticizing, 504 cycles of RD follow during which the designated tape is started and comes up to speed. After three RD cycles, in the same manner as for the operation W, the addressed character is read out of the memory to the Z register 14. The status level RO then becomes high, and operation is similar to that for operation level W high, except that the C counter 12 (FIG. 1(c-b)) does not have a pulse applied to its trigger terminal T to subtract one from the count stored therein, when the status level RO is high. At the end of the status level RO with the occurrence of the eighth delayed timing pulse T8a, the status transition gate 1242 (FIG. 1G) causes selection of the status level RIS (read-in space) to be high. At this point the character has been read out of the HSM 15, 16 and into the Z register 14, but has not been read out to the tape.

5.9.2.2 Status Level RIS High

The gate 697 (FIG. 1(c-b)) or the gate 695 passes the first timing pulse T1 depending on whether the 2⁹ bit flip-flop in the C register 28 (FIG. 1(c-a)) is in its reset or set condition respectively. If this 2⁹ bit flip-flop is reset, then the gate 697 passes the first timing pulse T1 to open the gates 650 to address the left HSM 15 (FIG. 1(c-c)). If the 2⁹ bit flip-flop of the C register 28 is set, then the gates 695 passes the first timing pulse T1 to the gates 660 to address the right HSM 16 (FIG. 1(d-c)). Note that the gates 799 (FIG. 1(c-c)) and 899 (FIG. 1(d-c)) are not primed.

The gate 302 passes the second timing pulse T2 to the

trigger terminal T of the C counter 12 to subtract one from the count in the C counter 12. The C counter 12 then holds the address of the next character of the item to be read out. Note that the count of the C counter 12 is not advanced during the status level RO because the addressing circuits should receive, at the first timing pulse during the status level RIS, the address of the character first read out to the tape.

The left read-in gate 721 (FIG. 1(c-c)) is open to activate the left HSM 15 for write-in; and the right read-in gate 850 (FIG. 1(d-c)) is open to activate the right HSM 16 for read-in, due partly to the status level RIS applied to the read-in gates through "or" circuits (FIGS. 1(b-c) and 1(d-c)) with the output of the inverters 18 and 19 of FIGS. 1(b-c) and 1(d-b) respectively.

The gate 729 (FIG. 1(c-c)), primed by the left read-in gate 721 output, applies, or the gate 858 (FIG. 1(d-c)), primed by the right read-in gate 850 output (as the case may be), applies a pulse to the first and seventh (2^0 and 2^6) bit channels only of the left HSM 15, and the right HSM 16. At the first timing pulse T1 during the last high status level RO, the L and R registers 18 and 19 (FIGS. 1(c-c) and 1(d-c)) were reset by a pulse from the gate 861 (FIG. 1(e-c)) the lead XX (FIG. 1(d-c)). The gates 722 (FIG. 1(c-d)) or the gates 851 (FIG. 1(d-c)) are opened depending on whether the left read-in gate 721 output or the right read-in gate 850 output is high. Thus the remaining 2^1 to 2^5 bits are entered in the left HSM 15 or the right HSM 16 as "zeroes." Accordingly, a space character in the machine code (1000001) has been read into the left and right HSM 15 and 16. Note that the left or right HSM 15 or 16 not addressed has a space written into its "zero" address location. This zero address, however, is vacant anyhow, because it is from this address that the first third of the first instruction of any surge is withdrawn.

The status transition gate 1230 (FIG. 1H) passes the eighth delayed timing pulse T8a to select the status level RD to be high. The machine now continues with one RD cycle in which the character is read from the Z register 14 out to the tape; three RD cycles; one RO cycle in which the character is read out of the HSM 15, 16 into the Z register 14; one RIS cycle in which a space character is read into the address in the HSM 15 or 16 from which the character was just read out into the Z register 14 (and into the zero address of the other); and an RD cycle in which the character is read from the Z register 14 to the tape. This sequence is the same as in the operation read-out to tape with status level W high, except for the insertion of the high status level RIS, and the operation is otherwise similar.

This sequence is repeated until the equality in the A and C counters 10 and 12 is reached, when the status transition gate 1204 (FIG. 1H) passes the eighth delayed timing pulse T8a and the status level IC (instruction complete) becomes high.

5.9.3 Sequence of Status Levels

Compare the status level flow diagram for operation H, FIG. 20 and the status level flow diagram for operation W, FIG. 19. The operation H (write out to tape and clear) is a duplication of the operation W (write out to tape) except for reading a space into the memory during the interposed status level RIS, and the fact that the count in the C counter 12 address, as the characters of an item are read out, is reduced by one during the high status level RIS rather than during the high status level RO. Otherwise, the operations are the same and no further description should be required.

5.10 Transfer Data Within HSM 15, 16 (Operation X) Operation Level X High

The purpose of the instruction transfer of item within the memory is to transfer an item from one address in the memory to another address in the memory.

5.10.1 Additional Components

A status transition gate 1270 (FIG. 1G) having five inputs is provided. One of these inputs is from an "or" circuit to which the operation levels J and X are applied. A second input to the status transition gate 1270 is from the status level RI. Third and fourth inputs to the status transition gate 1270 are respectively from the NOT ISSR lead (FIG. 1(e-d)) and the NOT ISSL lead (FIG. 1(b-d)). The fifth input to the status transition gate 1270 (FIG. 1G) is the eighth delayed timing pulse T8a. The output of the status transition gate 1270 is applied to the "set RO" lead.

A three input gate 861 (FIG. 1(e-c)) has as one input the output of an "or" circuit receiving the operation levels J, E, X, and V; as a second input the output of an "or" circuit receiving the status levels RE, RO, and RS; and as the third input, the eighth delayed timing pulse. The output of the gate 861 is applied through an "or" circuit to the lead XX (FIG. 1(d-c)), to three reset terminals of the L and R registers 18 and 19.

A status transition gate 1212 (FIG. 1H) is provided. One input to the status transition gate 1212 is from an "or" circuit to which is applied the operation levels J and X, indicated "J, X." A second input to the status transition gate 1212 is from the status level RI. A third input to the status transition gate 1212 is from an "or" circuit to which is applied the output of the ISSL lead (FIG. 1(c-d)) and the ISSR lead. The fourth and final input to the status transition gate 1212 is the eighth delayed timing pulse T8a. The output of the status transition gate 1212 is applied to the "set IC" (instruction complete) lead.

A set of seven, four-input gates 802 (FIG. 1(d-d)) is provided. One of the inputs to the gates 802 are respectively the seven bit output *s* of the left HSM 15 (FIG. 1(c-c)) and the right HSM 16 (FIG. 1(d-c)) applied through suitable "or" circuits as indicated. A second input to each of the gates 802 is from an "or" circuit receiving the operation levels J, E, and X. A third input to each of the gates 802 is from an "or" circuit receiving the status levels RO and RS. The fourth input to each of the gates 802 is the sixth timing pulse T6. The seven bit output of the gates 802 is applied to the seven set terminals S of the L register 18 (FIG. 1(b-c)) and to the seven set terminals S of the R register 19 (FIG. 1(d-c)).

A gate 639 (FIG. 1(c-b)) and a similar gate 690 (FIG. 1(d-b)) are provided, each being four-input gates. One input of each of the gates 639 and 690 is from a suitable "or" circuit receiving as inputs the operation levels X, J, and E.

A second input to each of the gates 639 and 690 is from the status level RI. The gate 639 (FIG. 1(c-b)) receives as its third input the output of an "or" circuit to which is applied the operation level E and the output of the "zero" terminal of the 2^{10} bit flip-flop of the C register 28 (FIG. 1(c-a)). The gate 690 (FIG. 1(d-b)) receives as its third input the output of an "or" circuit to which is applied the operation level E and the output from the "one" terminal of the 2^{10} bit flip-flop of the C register 28 (FIG. 1(c-a)). The fourth and final input to each of the gates 639 and 690 is the first timing pulse T1. The output of the gate 639 (FIG. 1(d-b)) is applied to open the gates 640 (FIG. 1(c-b)) between the A counter 10 and the address circuits of the left HSM 15 (FIG. 1(c-c)). The output of the gate 690 (FIG. 1(d-b)) is applied to open the gates 670 between the output of the B counter 11 (FIG. 1(d-b)) and the address circuits of the right HSM 16 (FIG. 1(d-c)).

A pair of gates, gate 506 (FIG. 1(c-b)) (for the A counter 10) and 507 (FIG. 1(d-b)) (for the B counter 11) are provided, the outputs of which are applied to the trigger terminals T of the A and B counters 10 and 11 respectively, through suitable "or" circuits as shown. Each of the gates 506 (FIG. 1(c-b)) and 507 (FIG. 1(d-b)) has applied to it the status level RI. A second

input to each of the gates 506 and 507 is the output of a suitable "or" circuit to which is applied the operation levels J, E, and X. The third input to each of the gates 506 and 507 is the second timing pulse T2.

5.10.2 Detailed Operation

The instruction for operation X is staticized in RO01, RO02, and RO03, as follows (see also FIG. 12):

FFR-O	A Counter	B Counter	C Counter
Instruction code for transfer of item.	Address to which item is to be transferred if 2 ¹⁰ bit of C address is "zero."	Address to which item is to be transferred if 2 ¹⁰ bit of C address is "one."	Address of item to be transferred plus 2 ¹⁰ bit designation.

At the eighth delayed timing pulse T8a, after the instruction is staticized in the high status level RO03, the status transition gate 1264 (FIG. 1G) causes the status level RO to be selected as high.

5.10.2.1 Status Level RO High

If the 2⁹ bit flip-flop of the C register 28 is in its reset condition, the gate 697 (FIG. 1(c-b)) passes the first timing pulse T1 to open the gates 650, and the left HSM 15 (FIG. 1(c-c)) is addressed by the contents of the C counter 12 (FIG. 1(c-b)). If the 2⁹ bit flip-flop of the C register 28 is in its set condition, the gate 695 passes the first timing pulse T1 to open the gates 660, and the right HSM 16 (FIG. 1(d-c)) is addressed by the C counter 12 (FIG. 1(c-b)). The gate 861 (FIG. 1(e-c)) passes the first timing pulse T1 to reset the R register 19 and to reset the L register 18.

The gate 304 (FIG. 1(c-b)) passes the second timing pulse T2 to the trigger terminal T of the C counter 12. Note that the C counter 12 is in its advance forward counting state because the flip-flop F302 was reset in the final RO03 status level high, by the third timing pulse T3 from the gate 312. Accordingly, one count is added to the count of the C counter 12. The C counter 12 now holds the address of the next character to be transferred.

The Z register 14 (FIG. 1(d-d)) is reset by the fourth timing pulse T4 passed through the gate 1043 and thence to the delay circuit D56. The Y register 13 (FIG. 1(c-d)) is reset by the fourth timing pulse T4 passed through the gate 903 (FIG. 1(b-d)).

According to whether the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset or set condition, the left or right read out gate 730 (FIG. 1(c-c)) or 862 (FIG. 1(d-c)) respectively has its output at a high level, and the left or right HSM 15 or 16 (FIG. 1(c-c)) or 1(d-c) is conditioned for read out.

The sixth timing pulse T6 is passed by the gate 919 (FIG. 1(c-d)) to open the gates 911; and the gate 1030 passes the sixth timing pulse T6 to open the gates 1032 (FIG. 1(d-d)). Accordingly, if information is being read from the left HSM 15 (FIG. 1(c-c)) it is read into the Y register 13 (FIG. 1(c-d)); if information is being read from the right HSM 16 (FIG. 1(d-c)) it is read into the Z register 14 (FIG. 1(d-d)). Furthermore, the gates 802 (FIG. 11(d-d)) are opened at the sixth timing pulse T6 to pass the character being read-out into the L register 18 (FIG. 1(b-c)) and the R register 19 (FIG. 1(d-c)).

Note that the character being read out is stored in the Y or Z register 13 or 14. The recognition circuits 22 or 23, and particularly "or" circuits R922 (FIG. 1(b-d)) and "or" circuits R1054 (FIG. 1(e-d)) associated respectively with the Y or Z register 13 or 14, therefore senses the contents of these registers to determine whether or not an ISS is present.

The status transition gate 1249 (FIG. 1G) now passes the eighth delayed timing pulse T8a to cause the status level RI to be selected as high.

5.10.2.2 Status Level RI High

If the 2¹⁰ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset condition, the gate 639 (FIG. 1(c-b)) passes the first timing pulse T1 to open the gates 670, and the left HSM 15 (FIG. 1(c-c)) is addressed by the contents of the A counter 10 (FIG. 1(c-b)). If the 2¹⁰ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its set condition, the gate 690 (FIG. 1(d-b)) passes the first timing pulse T1 to open the gates 670 and the right HSM 16 (FIG. 1(d-c)) is addressed by the contents of the B counter 11 (FIG. 1(d-b)).

The gate 506 (FIG. 1(c-b)) passes the second timing pulse T2 to the trigger terminal T of the A counter 10 to advance by one the count of the A counter 10. The gate 507 (FIG. 1(d-b)) passes the second timing pulse T2 to the trigger terminal T of the B counter 11. The A counter 10 or the B counter 11 then registers the address to which the next character is to be transferred in the left HSM 15 or the right HSM 16.

If the 2¹⁰ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset condition, the left read-in gate 721 (FIG. 1(c-c)) is opened to place the left HSM 15 in condition for read-in. If the 2¹⁰ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its set condition, the right read-in gate 850 (FIG. 1(d-c)) is open and the right HSM 16 is in condition for read-in. In this connection, note that when either the operation level J or X is high, the output of both the inverters 18 (FIG. 1(b-c)) and 19 (FIG. 1(d-b)) are low, and this low output cannot prime the left read-in gate 721 (FIG. 1(c-c)) or the right read-in gate 850 (FIG. 1(d-c)), as the case may be. Therefore which of the gates 721 and 850 are primed depends on which output ("zero" or "one") of the 2¹⁰ bit flip-flop of the C register 28 (FIG. 1(c-a)) is high. Accordingly, the contents of the L register 18 (FIG. 1(b-c)) or of the R register 19 (FIG. 1(d-b)) are read into the left HSM 15 or the right HSM 16, respectively, depending on whether the 2¹⁰ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset or set condition.

If the character just read into the left HSM 15 or the right HSM 16 is any other character than an item separation symbol, then the NOT ISSR lead (FIG. 1(d-e)) and the NOT ISSL lead (FIG. 1(c-d)) in the left symbol recognition circuits 22 and the right symbol recognition circuits 23 are both high. Accordingly, the status transition gate 1270 (FIG. 1G) passes the eighth delayed timing pulse T8a to cause the status level RO to be selected as high.

The RO-RI sequence just described is repeated until all the characters which are not ISS, are read out of the addressed locations in the HSM 15, 16 into the new locations.

If and when an item separation symbol is read out of the left HSM 15 or the right HSM 16, the item separation symbol is read into the HSM 15, 16 as the last symbol stored. However, at the termination of the status level RI, with the occurrence of the eighth delayed timing pulse T8a, one of the leads NOT ISSR or NOT ISSL is at a low level, and at least one of the leads ISSL and ISSR is at a high level. Accordingly, the status transition gate 1270 (FIG. 1G) cannot pass the eighth delayed timing pulse T8a. Instead, the status transition gate 1212 (FIG. 1H) is primed and passes the eighth delayed timing pulse T8a to select the status level IC to be high.

5.10.3 Sequence of Status Levels

With reference to the status level flow diagram FIG. 21, the machine selects the status level RO to be high, after the instruction is staticized.

During the status level RO high, the least significant character of the item being transferred is read out of the HSM 15, 16. The machine then selects the status level RI to be high.

The least significant character of the item is now read back into the HSM 15, 16 at the new location, during the status level RI high. The machine then selects status level RO to be high and continues in a reiterated RO-RI sequence. Characters in locations corresponding to succeeding higher numbered memory locations for the item are read out of the HSM 15, 16 and placed in the new locations, in the order of least significant character to most significant.

When an ISS is detected, indicating the end of the item, the machine selects the status level IC to be high.

The 2¹⁰ bit flip-flop in the C register 28 specifies to which side of the HSM 15, 16 (left or right) the item is to be transferred. If the 2¹⁰ bit flip-flop has its "one" output high, the item is transferred to the right HSM 16. If the "zero" output of the 2¹⁰ bit flip-flop is high, the item is transferred to the left HSM 15.

The 2⁹ bit flip-flop in the C register 28 specifies from which side of the HSM 15, 16 the item is to be withdrawn. If the 2⁹ bit flip-flop of the C register 28 is in its set condition, the item is withdrawn from the right HSM 16; if the 2⁹ bit flip-flop for the C register 28 is in its reset condition, the item is withdrawn from the left HSM 15.

5.11 Transfer and Clear Data Within HSM 15, 16 (Operation J)—Operation Level J High

This operation is similar to the operation for transferring data, high operation level X, just described, with certain exceptions which will be apparent hereinafter. Only a few further components are required.

5.11.1 Additional Components

A status transition gate 1245 (FIG. 1G) is provided having three inputs, one from the operation level J, a second from the status level RO, and the third from the eighth delayed timing pulse T8a. The output of the status transition gate 1245 is applied, through "or" circuits, to the "set RIS" lead.

A three input status transition gate 1257 (FIG. 1G) has as one input, the status level RIS; as a second input, the operation level J; and as the third input, the eighth delayed timing pulse T8a. The output of the status transition gate 1257 is applied through "or" circuits to the "set RI" lead.

5.11.2 Detailed Operation

The instruction is staticized in the same manner as in the transfer of item within HSM 15, 16, operation X. After the status levels RO01, RO02, and RO03, the status level RO is selected to be high.

5.11.2.1 Status Level RO High

The first part of the operation with the status level RO high for transferring clear data within HSM 15, 16, operation J, is the same as for the operation X just described with two exceptions:

First, at the second timing pulse T2, the C counter 12 does not have its count advanced, but retains its count.

Second, at the eighth delayed timing pulse T8a, the status transition gate 1245 (FIG. 1G) causes the status level RIS to be selected as the next high status level. The status transition gate 1249 (FIG. 1G) does not pass a pulse. Therefore, the status level RIS is high after the status level RO.

5.11.2.2 Status Level RIS High

The gates 650 (FIG. 1(c-b)) are opened by the first timing pulse T1 passed through the gate 697, if the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset condition. If the 2⁹ bit flip-flop of the C register 28 is in its set condition, the gate 695 (FIG. 1(c-b)) passes the first timing pulse T1 to open the gates 660. Accordingly, the left HSM 15 (FIG. 1(c-c)) or the right HSM 16 (FIG. 1(d-c)) is addressed by the contents of the C

counter 12 (FIG. 1(c-b)), respectively in accordance with whether the 2⁹ bit flip-flop of the C register 28 is in its reset or set condition. The memory bank not addressed has its address circuits set at the "zero" address.

The gate 302 (FIG. 1(c-b)) passes the second timing pulse T2 to the trigger terminal T of the C counter 12. The C counter 12 count is now (in the high status level RIS) advanced by one to contain the address of the next character to be read out of the memory.

The read-in gates, gate 721 (FIG. 1(c-c)) and gate 850 (FIG. 1(d-c)), has their outputs high due partly to the RIS status level applied through "or" circuits (FIGS. 1(b-c) and 1(d-c)), and also to the high operation level J. A space is now read into the left HSM 15 and the right HSM 16 from the gates 729 and the gate 858, with the occurrence of the fifth timing pulse T5 at the address from which the character was first read out and at the "zero" address in the other memory bank, as explained in connection with the high status level RIS under the operation write-out to tape and clear H (sec. 5.9.3 supra).

The status transition gate 1257 now passes the eighth delayed timing pulse T8a to cause the status level RI to be high.

5.11.2.3 Status Level RI High

In this status level, the operation proceeds as for the status level RI high in the transfer of item within HSM 15, 16, operation level X high (sec. 5.10.4 supra).

When an ISS is read out and recognized, the status transition gate 1212 (FIG. 1H) passes the eighth delayed timing pulse T8a, as during the operation X, to cause the status level IC to be high.

5.11.3 Sequence of Status Levels—Operation J

This operation for transfer and clear is similar to that of the operation for transfer, except that a space character is written into the HSM 15, 16 location from which the information was withdrawn or read. With reference to the flow diagram of FIG. 22, the operation instruction for transfer and clear is staticized in RO01, RO02, and RO03. The machine then selects the status level RO to be high.

The least significant character of the item to be transferred is read out or withdrawn from the HSM 15, 16. The character is stored in both the L and R registers 18 and 19, after being read out of the memory also to the Y register 13 the register 14. The machine then selects the status level RIS to be high.

In the status level RIS high, a space is inserted in the HSM 15, 16 location from which the character was read out or withdrawn. The machine then selects the status level RI to be high.

The least significant character of the item is now read into the new HSM 15 location or the HSM 16 location respectively from the L register 18 or the R register 19 depending on the program. The machine then selects the status level RO to be high.

The RO-RIS-RI sequence continues, the characters being transferred from successively higher order locations and space characters being placed in their original locations.

When an ISS (item separation symbol) is read out of the HSM 15, 16 it is also read into the new HSM 15, 16 location. However, after the status level RI is high and the ISS has been read into the new location, the machine selects the status level IC for instruction complete.

5.12 Justify Right (Operation E)—Operation Level E High

In the operation justify right, a numeric item having allotted to it certain addresses in the memory, is reentered in the memory with its least significant digit as the lowest allotted address. In English writing, the positioning of the least significant numeral at the right of a column may be termed "justifying" or lining up the figures on the right hand margin of a column. By analogy, the corresponding operation of the machine is termed "justify right."

The operation is usually employed prior to reading numbers out to tape or preparatory to printing an output in numbers, so that the numbers will be "lined up" on the right hand side. In this machine, it is contemplated that this operation is to be used only for numeric items.

5.12.1 Additional Components

A three-input gate 553 has as one input the operation level E, as a second input the status level RS, and as the third input the first timing pulse T1. The output of the gate 553 is applied through "or" circuits to the reset terminals of the A counter 10 (FIG. 1(c-b)) and of the B counter 11 (FIG. 1(d-b)).

A gate 501 (FIG. 1(c-b)) is provided having three inputs, one from the status level RS, a second from the operation level E, and the third from the sixth timing pulse T6. The output of the gate 501 is applied through the "or" circuit that also receives the output of the gate 503, to prime the gates 523 (FIG. 1(c-b)) and the gates 534 (FIG. 1(d-b)).

A status transition gate 1246 (FIG. 1G) is provided having five inputs: one input is the output of an "or" circuit having inputs from the status levels RS and RO; a second input is from the status level E; a third input is from the NOT ISSL lead (FIG. 1(b-d)); a fourth input is from the NOT ISSR lead (FIG. 1(e-d)); and the fifth input is from the eighth delayed timing pulse T8a. The output of the status transition gate 1246 is applied to the "set RIS" lead.

A status transition gate 1211 (FIG. 1H) is provided having four inputs. One input is from the operation level E. A second input is the output of an "or" circuit to which is applied the outputs from the leads ISSL and ISSR (FIGS. 1(c-e) and 1(d-e)) respectively. A third input to the status transition gate 1211 is from an "or" circuit to which is applied the status levels RI and RS. The fourth input to the status transition gate 1211 is the eighth delayed timing pulse T8a. The output of the status transition gate 1211 is applied to the "set IC" lead.

Another four-input status transition gate 1235 (FIG. 1G) is provided having as one input the output of an "or" circuit to which is applied the SPL lead (FIG. 1(c-d)) and the SPR lead (FIG. 1(d-e)). Second and third inputs to the status transition gate (FIG. 1G) are respectively from the status level RIS and the operation level E; a fourth input from the status level RIS; and the fifth input from the eighth delayed timing pulse T8a. The output of the status transition gate 1258 (FIG. 1G) is applied through "or" circuits to the "set RI" lead.

A five-input status transition gate (FIG. 1G) 1258 is provided having a first input from the NOT SPL lead (FIG. 1(b-d)) a second input from the NOT SPR lead (FIG. 1(d-d)); a third input from the operation level E; a fourth input from the status level RIS; and the fifth input from the eighth delayed timing pulse T8a. The output of the status transition gate 1258 (FIG. 1G) is applied through "or" circuits to the "set RI" lead.

A three-input status transition gate 1268 (FIG. 1G) has one input from the operation level E, a second input from the operation level RI, and the third input from the eighth delayed timing pulse T8a. The output of the status transition gate 1268 is applied through "or" circuits to the set RO lead.

5.12.2 Detailed Operation

The instruction is staticized in the status levels RO01, RO02, and RO03, as usual. The instruction is staticized as follows (see also FIG. 12):

FFR-O	A Counter	B Counter	C Counter
"Justify Right" Instruction Code Number.	Not Used...	Not Used...	Location of least-sig. char. of item after justification is complete.

During the status level RO03 high, when the instruction is staticized, the status transition gate 1234 passes the eighth delayed timing pulse T8a to cause the status level RS to be high.

5.12.2.1 Status Level RS High

If the item to be justified is in the left HSM 15, the 2⁹ bit flip-flop of the C register 28 is in its reset condition; if the item to be justified is in the right HSM 16, the 2⁹ bit flip-flop of the C register 28 is in its set condition. In the former case, the gates 650 (FIG. 1(c-b)) are opened by the first timing pulse T1 passed through the gate 697 and the left HSM 15 (FIG. 1(c-c)) is addressed by the contents of the C counter 12 (FIG. 1(c-b)). In the latter case, the gates 660 are opened by the first timing pulse T1 passed through the gate 697 and the left HSM 15 (FIG. 1(c-c)) is addressed by the contents of the C counter 12 (FIG. 1(c-b)). In the latter case, the gates 660 are opened by the first timing pulse T1 passed through the gate 695 and the right HSM 16 (FIG. 1(d-c)) is addressed by the contents of the C counter 12 (FIG. 1(c-b)).

The L and R registers 18 and 19 (FIGS. 1(b-c) and 1(d-c) respectively are cleared (reset) by a pulse from the gate 861 (FIG. 1(e-c)) to the lead XX.

Note that the gate 945 (FIG. 1(c-e)) passed the first timing pulse T1 in the preceding RO03 cycle to the space-left flip-flop F911 and also to set the space-right flip-flop F1008 (FIG. 1(d-e)). The gate 902 (FIG. 1(b-d)) is now primed by the high "one" output terminal of the space-left flip-flop F911 (FIG. 1(c-e)) to pass the fourth timing pulse T4 to reset the Y register 13 (FIG. 1(c-d)). The gate 1042 (FIG. 1(d-d)) primed by the high "one" output terminal of the space-right flip-flop F1008 (FIG. 1(d-e)) passes the fourth timing pulse T4 through the delay circuit D56 (FIG. 1(d-d)) to reset the Z register 14.

The left or right read-out gates 730 (FIG. 1(c-c)) or 862 (FIG. 1(d-c)) apply a high level to the read-out circuits of the left and right HSM 15 respectively, depending, respectively, on whether the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in reset or set condition.

If the left HSM 15 (FIG. 1(c-c)) is in condition for read-out, the addressed character is read out through the gates 911 (FIG. 1(c-d)) opened by the sixth timing pulse T6 passed through the gate 919. The character is then read into the Y register 13. If the right HSM 16 (FIG. 1(d-c)) is in condition for read out, the character is read out through the gates 1032 (FIG. 1(d-d)) opened by the sixth timing pulse T6 passed through the gate 1030 (FIG. 1(c-d)). The character from the right HSM 16 is read into the Z register 14 (FIG. 1(d-d)). The gates 524 (FIG. 1(c-d)) are opened by the sixth timing pulse T6 passed through the gate 501. The address stored in the C register 28 (FIG. 1(c-a)) is passed through the gates 524 and entered in the A counter 10 (FIG. 1(c-d)). The sixth timing pulse T6 passed by the gate 501 is also applied to the set of gates 534 (FIG. 1(d-b)) to open the latter set of gates. The gates 534 thus opened, cause the entry of the same address entered in the C register 28 (FIG. 1(c-a)) to be entered in the B counter 11 (FIG. 1(d-b)). Thus the same address is in the A counter 19 (FIG. 1(c-b)) and in the B counter 11 (FIG. 1(d-b)), and is to be used when reading in the first, not-space, least significant character in the selected left or right HSM 15 or 16. Note that the search for the least significant character starts from the address corresponding to the right-hand side to which the item is to be justified.

The gate 944 (FIG. 1(d-e)) passes the seventh timing pulse T7 to reset the space-right flip-flop F1008 (FIG. 1(d-e)) and the space-left flip-flop F911 (FIG. 1(c-e)).

If the character just read out of the memory is from the left HSM 15, (FIG. 1(c-c)) and is a space, the space character is stored in the Y register 13 (FIG. 1(c-d)).

The space-left SPL lead (FIG. 1(c-d)) in the left symbol recognition circuits 22 becomes high. The gate 938 (FIG. 1(c-e)) then passes the eighth timing pulse T8 to set the space-left flip-flop F911. If the character just read out of the HSM 15, 16 is from the right HSM 16 (FIG. 1(d-c)) and is a space, the contents of the Z register 14 (FIG. 1(d-d)) correspond to a space character. The SPR lead (FIG. 1(d-e)) of the right symbol recognition circuits 23 is at a high level. The gate 1057 (FIG. 1(d-e)) is therefore primed to pass the eighth timing pulse T8 to set the space-right flip-flop F1008.

If an ISS is read out, the status transition gate 1211 selects the status level IC to be high, and the instruction is complete.

If the character read from the left or right HSM 15 or 16 is not an item separation symbol, then both the NOT ISSL (FIG. 1(b-e)) and the NOT ISSR (FIG. 1(d-e)) leads of the left and right symbol recognition circuits 22 and 23 respectively are at a high level. The status transition gate 1246 (FIG. 1G) now passes the eighth delayed timing pulse T8a to the set RIS lead.

Note that if the character read out is a space, one of the space-left flip-flops F911 or space-right flip-flops F1008 is in the set condition. If no space has been read out, then both of these flip-flops, the space-left flip-flop F911 and the space-right flip-flop F1008, are in the reset condition.

5.12.2.2 Status Level RIS High

Either the gate 697 (FIG. 1(c-b)) passes the first timing pulse T1 to open the gates 659 and address the left HSM 15 (FIG. 1(c-c)) with the C counter 12 (FIG. 1(c-b)); or the gate 695 passes the first timing pulse T1 to open the gates 660 and address the right HSM 16 (FIG. 1(d-c)) with the contents of the C counter 12 (FIG. 1(c-b)), according, respectively, to whether the 2⁹ bit flip-flop of the C register 28 is in the reset or set, condition.

The gate 302 passes the second timing pulse T2 to advance the count in the C counter 12 by one. Note that the C counter 12 is in the forward counting state by reason of the resetting of the flip-flop F302 during the previous high status level RO03. The C counter 12 now holds the address of the next least significant character of the item after justification.

The left read-in gate 721 (FIG. 1(c-c)) applies a high level to activate the read-in circuits of the left HSM 15 and also to apply a high level to the gate 729. The gate 729 (FIG. 1(c-c)) passes the fifth timing pulse T5 to enter a space symbol in the left HSM 15. The right read-in gate 850 (FIG. 1(d-c)) applies a high level to activate the read-in circuits of the right HSM 16, and also to apply a high level to the gate 858. The gate 858 (FIG. 1(d-c)) passes the pulse thus applied to enter a space symbol in the right HSM 16. Recall that the 2¹ to 2⁹ bits are entered from the L or R register 18 or 19, cleared during the preceding RO level or RS level. If the 2⁹ bit flip-flop of the C register is set the space is written into the right HSM 16 at the address in the C counter 12 and at the "zero" address in the right HSM 15; if the 2⁹ bit flip-flop of the C register is in the reset condition, the space is written into the left HSM 15 at the address from the C counter 12 and at the "zero" address in the right HSM 16. Compare sections 5.9.3 and 5.11.3.

If a space was recognized in the preceding status level RS, the status transition gate 1235 (FIG. 1H) is opened to pass the eighth delay timing pulse T8a to the set RS lead. Accordingly, the status level RS is selected to be high.

If a space had been read out of the HSM 15, 16, then the status level RS being selected, the operation is as just described for a cycle of the status level RS high, and a cycle of status level RIS high, when another non-

space character is encountered. Note that the space between non-space characters are thus suppressed.

On the other hand, if, in the preceding RS cycle, a space was not read out from the left or right HSM 15, 16, both the NOT SPL lead (FIG. 1(b-d)) and NOT SPR lead (FIG. 1(d-d)) are high. The status transition gate 1258 (FIG. 1G) then is opened to pass the eighth delayed timing pulse T8a to select the status level RI to be high.

5.12.2.3 Status Level RI High

The first not space character is now to be written into the location of the least significant digit of the item.

The left HSM 15, (FIG. 1(c-c)) is addressed by the contents of the A counter 10 (FIG. 1(c-b)) through the gates 640 opened by the first timing pulse T1 passed through the gate 639. The right HSM 16 (FIG. 1(d-c)) is addressed by the contents of the B counter 11 (FIG. 1(d-b)) passed through the gates 670 opened by the first timing pulse T1 passed through the gate 690. Note that the address corresponds to that of the least significant character of the item stored when the justify right operation began.

The gate 506 (FIG. 1(c-b)) passes the second timing pulse T2 to advance the count of the A counter 10 by one. The gate 5007 (FIG. 1(d-b)) passes the second timing T2 to advance the count of the B counter 11 by one. Either the A counter 10 or the B counter 11 is now prepared to address the HSM 15, 16 with the address of the location into which the next character of the item is to be withdrawn.

Note that at the last status level RS high, the character read out of the memory was stored in the L and R registers 18 and 19. If the 2⁹ bit flip-flop of the C register 28 is in its reset condition, the left read-in gate 721 (FIG. 1(c-c)) primes the gates 799, which passes the fifth timing pulse T5 to open the gates 722. The contents of the L register 18 (FIG. 1(b-c)) are then written into the left HSM 15 (FIG. 1(c-c)) at the place addressed by the A counter 10 in the preceding first timing pulse T1. If the 2⁹ bit flip-flop of the C register 28 is in its set condition, the right read-in gate 850 (FIG. 1(d-c)) primes the gate 899 to pass the fifth timing pulse T5 to open the gates 851. The contents of the R register 19 are then written into the right HSM 16 at the place addressed by the B counter 11 (FIG. 1(d-b)) at the preceding first timing pulse T1.

The status transition gate 1268 (FIG. 1G) passes the eighth delayed timing pulse T8a to the set RO lead. Accordingly, the status level RO is high.

5.12.2.4 Status Level RO High

The left HSM 15 (FIG. 1(c-c)) is addressed by the C counter 12 (FIG. 1(c-b)) through the gate 650 (FIG. 1(c-b)) opened by the first timing pulse T1 passed through the gate 697.

The right HSM 16 (FIG. 1(d-c)) is addressed by the contents of the C counter 12 (FIG. 1(c-b)) through the gates 660 (FIG. 1(c-b)) opened by the first timing pulse T1 passed through the gate 695.

The L and R registers 18 and 19 are reset by the first timing pulse T1 passed through the gate 861 (FIG. 1(e-c)).

The left HSM 15 (FIG. 1(c-c)) read-out circuit or the right HSM 16 (FIG. 1(d-c)) read-out circuit is activated by the left or right read-out gates 730 or 862, respectively, depending on whether the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-b)) is in its reset or set condition respectively.

If the left HSM 15 (FIG. 1(c-c)) is activated for read-out, the contents of the left HSM 15 at the address supplied from the C counter 12 at the last occurrence of the first timing pulse T1 are read into the Y register 13 (FIG. 1(c-d)) through the gates 911 opened by the sixth timing pulse T6 passed through the gate 919. If the right

HSM 16 (FIG. 1(d-c)) is activated for read out, the contents of the right HSM 16 at the address supplied from the C counter 12 at the last occurrence of the first timing pulse T1 are read into the Z register 14 (FIG. 1(d-d)) through the gates 1032 opened by the sixth timing pulse T6 through the gate 1030. In either event, whether the left or right HSM 15 or 16 is activated for read out, the character being read out passes through the gates 802 (FIG. 1(d-d)) opened by the sixth timing pulse T6, into both the L register 18 (FIG. 1(b-c)) and the R register 19 (FIG. 1(d-c)).

If the character is not an ISS, then both the NOT ISSL and the NOT ISSR lead are high, and the status transition gate 1246 (FIG. 1G) passes the eighth delayed timing pulse T8a to the "set RIS" lead. Accordingly, the status level RIS is now high.

The RIS-RI-RO sequence of status levels is repeated until an ISS is recognized by the left or right symbol recognition circuits 22 or 23. If an ISS occurs or is stored in either the Y or Z registers 13 or 14, the ISSL or ISSR lead, one or the other, is high. Therefore, the status transition gate 1211 (FIG. 1H) selects the status level IC to be high by passing the eighth delayed timing pulse T8a to the "set IC" lead.

5.12.3 Sequence of Status Levels

The following example represents an item having an item separation symbol and numeric characters C₃, C₂, C₁ stored in the HSM 15, 16 at the addresses numbered 301 to 308 inclusive as follows:

*Example for Justifying Right—Operation E—
Before Justifying*

308 H	307 G	306 F	305 E	304 D	303 C	302 B	301 A
.	C ₃	C ₂	C ₁	-	-	-	-

In this example, the not-space characters C₃, C₂, C₁ are to be moved to the right to the addresses C, B, and A as follows:

*Example for Justifying Right—Operation E—
After Justifying*

H	G	F	E	D	C	B	A
.	-	-	-	-	C ₃	C ₂	C ₁

The "O" section of the instruction (FIG. 12) stored in the C register 28 gives the address in the HSM 15, 16 where the least-significant digit of the item is to be found. The sections for the A register 26 and the B counter 11 are not used. If the item is stored in the left HSM 15, the 2⁹ bit (the tenth bit) of the address is zero. If the item is stored in the right HSM 16, the 2⁹ bit is one. In what follows, for the sake of brevity, it is assumed that the item is stored in the left HSM 15, and that the 2⁹ bit in the C register is zero. The corresponding operation for the right HSM 16 should be clear from the detailed description already given.

Referring to the status level flow diagram for the operation justify right (E), FIG. 23, the instruction is staticized in the usual way with the status level sequence RO01, RO02, and RO03. The address of the least significant character of the item to be justified is stored in the C register 28 and in the C counter 12. The characters are now read out, starting with the first, into the L and R registers 18 and 19, starting with the least significant character from the space 301. A space character is read back into the location from which each character has just been read out. The characters are read out in the high status level RS (read out and search) and a

space is read back into the high status level RIS (read in space), these status levels being high in sequence as long as a space is recognized. Note that the first time the status level RIS is high, the address of the least significant character of the item to which the first not space character is to be transferred is entered into the A counter 10. In other words, the least significant address, in the example above numbered 301, the space initially addressed and to which the item is to be justified to the right, is stored in the A counter 10.

The RS-RIS sequence is continued until, during the high status level RS, a not space character has been read out of the left HSM 15 and stored in the Y register 13, and also in the L register 18. In this event, instead of returning to the status level RS high, after the status level RIS is high, the machine selects the status level RI to be high, and the not space character, for example, C₁, at the address 305 is read from the L register 18 into the left HSM 15 at the address 301 of the least significant character of the item, which address 301 has been stored in the A counter 10. The address in the A counter 10 is now advanced by one.

The next not-space character, C₂, at address 306, is now read out to the Y register 13 during the high status level RO, a space is read into the left HSM 15 at address 306 during the high status level RIS, and the second not-space character is now read into the HSM 15 at address 302 from the L register 18.

The RO-RIS-RI sequence is repeated until an ISS is recognized at address 308, during the high status level RO. Such recognition indicates that all the characters of the item have been shifted, and that the justify right instruction has been completed. The IC (instruction complete) level is then selected.

Note that, in the present machine, if a space is encountered following a not-space character, the spacing between the not-space characters is obliterated. Therefore, this instruction is reserved, at least in the present machine, for numbers and other items without spaces between not-space characters.

5.13 Operation Level K High

5.13.1 Additional Components

A few other components are employed, in addition to the component already described, to perform the operation clear. A three-input status transition gate 1244 (FIG. 1G) is provided. One input to the gate 1244 is from the status level RO03, a second input is from the operation level K, and the third input is from the eighth delayed timing pulse T8a. The output of the status transition gate 1244 is applied to the "set RIS" lead.

A four-input status transition gate 1203 is provided having four inputs, one from the "one" output terminal of the address equal flip-flop F301; a second from the status level RIS; a third from the operation level K; and the fourth and final input from the eighth delayed timing pulse T8a.

5.13.2 Machine Operation

The instruction for the operation clear is as follows (see also FIG. 12):

FFR-O	A Counter	B Counter	C Counter
Instruction Code Number for Clear.	Address of location where clearing stops.	Not used....	Address of location where clearing starts.

The instruction is staticized during the status levels RO01, RO02, and RO03; the O register 30 (FIG. 1(b-a)) contains the instruction code number for the operation clear; and the operation matrix selects the operation level K to be high. The A counter 10 (FIG. 1(c-b)) registers the address of the location where the last clear (space) character is to be entered. The C counter 12 contains

the address of the location where the entry of the space characters is to start.

After the status level RO03, the status transition gate 1244 (FIG. 1H) passes the eighth delayed timing pulse T8a to select the status level RIS to be high.

If the 2⁹ bit flip-flop of the C register 28 (FIG. 1(c-a)) is in its reset condition, the gate 697 (FIG. 1(c-b)) passes the first timing pulse T1 to open the gates 650. The gates 650 address the left HSM 15 with the contents of the C counter 12. If the 2⁹ bit flip-flop of the C register 28 is in its set condition, the gate 694 passes the first timing pulse T1 to open the gates 660. The gates 660 pass the contents of the C counter 12 to address the right HSM 16.

At the first timing pulse T1, the contents of the A counter 10 and the C counter 12 are compared in the second equal circuit 35. If an equality is indicated, the first timing pulse T1 passes from the equality circuit 35 to the set terminal of the address equal flip-flop F301 (FIG. 1(b-b)). Note that the address equal flip-flop F301 was reset during the preceding high status level RO03 by the fourth timing pulse T4 passed by the gate 329. The status transistor gate 1203 (FIG. 1H) is primed by the "one" output terminal of the second address equal flip-flop F301. The output of the status transition gate 1203 then selects the status level IC to be high by a pulse on the "set IC" lead.

The gate 302 passes the second timing pulse T2 to advance the count of the C counter 12 by one. Although the C counter 12 was advanced by one count at the timing pulse T2, notice that this is immaterial because the equality is indicated by the status of the C counter 12 during the first timing pulse T1. Also, the memory is addressed during the first timing pulse T1.

In the operation clear (K), the 2¹¹ bit in the C register 28 is zero, and therefore the 2¹¹ bit flip-flop of the C register 28 is in its reset condition. Therefore, the gates 729 and 858 passes the fifth timing pulse T5 to write a "one" in each of the 2⁰ and 2⁸ bits in the left HSM 15. The gate 799 is also primed, and the gates 799 and gates 899 are opened, so that the remaining 2¹ to 2⁵ bits are entered as "zeroes" from the reset L and R registers 18 and 19. Note that the read-in gates 721 and 850 also condition the HSM 15, 16 for write in. Thus a space is entered as in sec. 5.9.3 supra, when status level RIS is high. The space is entered in the memory bank, left or right, addressed during the preceding first timing pulse T1, and at the zero address of the other of the HSM 15 or HSM 16.

If there was no equality at the last preceding first timing pulse T1 between the contents of the A counter 10 and the C counter 12, the address equal flip-flop F301 (FIG. 1(b-b)) remains in its reset condition, to which condition it was reset on the fourth timing pulse T4 during the status level RO03 in which the instruction to clear was staticized. The status level RIS remains high, and the steps just described are repeated to read a space into the next location in the HSM 15, 16 which is addressed (and the space is rewritten at the "zero" address of the other).

If an equality is indicated by the second equal circuit 35 passing the first timing pulse T1, the status transition gate 1203 (FIG. 1H) is primed by the high "one" output of the address equal flip-flop F301. The eighth delayed timing pulse T8a is then passed by the status transition gate 1203 to select the status level IC to be high.

The purpose of the clear operation is to remove information stored in certain specified addresses of the HSM 15, 16. A space is to be written into each of the addresses specified. The C register 28 contains the address of the particular location where the clearing of the addresses is to begin, after the staticizing of the instruction. The programmer indicates which bank of the HSM should be cleared by means of the 2⁹ bit flip-flop of the C register 28 is reset; if the right HSM 16 is to be cleared, the 2⁹ bit flip-flop of the C register 28 is set. Thus, only one-half of the HSM 15, 16 can be cleared by one instruction. Also, since the clearing process proceeds consecutively

from one address to another, if separate groups of addresses are to be cleared, a separate instruction is provided for each group.

5.13.3 Sequence of Status Levels

The succession of status levels followed during the operation K, are indicated in the status level flow diagram of FIG. 24. The instruction is staticized in the status levels RO01, RO02, and RO03. A space character is then read into the lowest numbered address as specified in the "C" section of the instruction. This address is then compared with the last address to be cleared, which the programmer has coded in the "A" section of the instruction.

If the addresses are not equal, this means that there are still some addresses to be cleared. In that event, another RIS cycle is repeated. A space character is written into the next higher numbered address of the HSM 15, 16, and the new address is compared with the final address. The cycles of RIS status levels are repeated until the comparison indicates that the address just filled with a space equals the last address specified. The instruction has therefore been completed and the status level IC follows.

5.14 Verify (Operation V)—Operation Level V High

5.14.1 Additional Components

Only a few further components are provided for the operation verify. Two sets of gates 702 and 843 (FIGS. 1(b-c) and 1(d-c)) are provided. Each set 709 and 843 has seven gates and each gate has four inputs. A first of these four inputs is from the status level RO, a second is from the operation level V, and a third is the sixth timing pulse T6. The fourth input to each of the first set of gates 709 (FIG. 1(b-c)) is derived respectively from each of the seven outputs of the left HSM 15. The fourth input to each of the second set of gates 843 (FIG. 1(d-c)) is respectively from the seven outputs of the right HSM 16. Note that as an alternative (not shown) a single gate for each set or for both sets may provide a clock pulse on the concurrence of a high level for all three inputs of status level RO, operation level V, and timing pulse T6. The output of the first set of gates 709 is applied to the different, corresponding set terminals of the L register 18. The outputs of the second set of gates 843 are applied to the different, corresponding set terminals of the R register 19.

A three-input gate 747 (FIG. 1(a-c)) is provided having as one input the status level RO, as a second input the operation level V, and as the third input the sixth timing pulse T6.

A status transition gate 1209 (FIG. 1H) has four inputs, one from the operation level V, a second from the status level RO, a third from the item separation symbol left (ISSL) lead (FIG. 1(c-d)), and the fourth and final input from the eighth delayed timing pulse T8a. The output of the status transition gate 1209 is applied to the "set IC" lead.

5.14.2 Machine Operation

The instruction for verify is staticized in the usual manner as indicated in the following table (see FIG. 12):

O Section	A Section	B Section	C Section
Instruction Code No. for Verify.	Location in Left HSM 15 of least significant character of item to be verified.	Location in Right HSM 16 of least significant character of item to be verified.	Not used.

The status transition gate 1264 (FIG. 1G) passes the eighth delayed timing pulse T8a to the set RO lead, and the status level RO is selected to be high.

The gate 861 (FIG. 1(e-c)) passes the first timing pulse T1 to the lead XX to reset the R register 19 and to reset

the L register 18. The gate 699 (FIG. 1(c-b)) passes the first timing pulse T1 to open the gates 640. The gates 640 pass the contents of the A counter 10 (FIG. 1(c-d)) to the address circuits of the left HSM 15. The gate 692 (FIG. 1(d-b)) passes the first timing pulse T1 to open the gates 670. The gates 670 pass the contents of the B counter 11 (FIG. 1(d-b)) to the address circuits of the right HSM 16.

The gate 504 (FIG. 1(c-b)) passes the second timing pulse T2 to advance the count in the A counter 10 by one. The gate 509 (FIG. 1(d-b)) passes the second timing pulse T2 to advance the count in the B counter 11 by one. The A counter 10 and the B counter 11 now contain the addresses respectively of the next characters to be compared in the left HSM 15 and the right HSM 16.

The left read out gate 730 (FIG. 1(c-c)) and the right read out gate 862 (FIG. 1(d-c)) pass a high level to condition the left HSM 15 and the right HSM 16 respectively for read out. Note that the high operation level V is applied through "or" circuits to the left read out gate 730 (FIG. 1(c-c)) and to the right read out gate 862 (FIG. 1(d-c)) and refer also to FIG. 1(c-c)).

The gates 709 (FIG. 1(c-c)) are opened by the sixth timing pulse T6 to pass the seven binary digits out of the left HSM 15 from the address entered in the address circuits when the first timing pulse T1 of this cycle occurred into the L register 18 (FIG. 1(b-c)). The contents (the seven binary digits) of the right HSM 16 (FIG. 1(d-c)) at the address specified in the first timing pulse T1 of the current cycle are now passed through the gates 843 to the R register 19. The gate 919 (FIG. 1(c-d)) passes the sixth timing pulse T6 to open the gates 911 (FIG. 1(c-d)). The gates 911 (FIG. 1(c-d)) now pass the contents of the left HSM 15 (FIG. 1(c-c)) into the Y register 13 (FIG. 1(c-d)).

The compare alarm flip-flop F707 (FIG. 1(a-c)) is set by the sixth timing pulse T6 passing through the gate 747. If the "one" output terminal of the compare alarm flip-flop F707 is high, the "no alarm" lead is low. In this event, the gate 1301 (FIG. 1(a-c)) does not receive a high level and cannot pass the eighth delayed timing pulse T8a. No new status level can be selected by means of the status transition gates, all of which receive the eighth delayed timing pulse as one input. Also, the gate 150 (FIG. 1(a-a)) is closed when the "no alarm" lead is low, and cannot pass the index (fiducial) pulse from the reset track of the program drum PD. Further, if the "one" output of the compare alarm flip-flop F707 (FIG. 1(a-c)) remains high until after the occurrence of the eighth timing pulse T8, the gate 228 (FIG. 1(a-c)) is primed to pass the timing pulse T8c to reset the flip-flop F214 (FIG. 1(a-b)). The "one" output of the flip-flop F214 is then low, and the gate 235 (FIG. 1(a-c)) in the timing pulse generator TPG is therefore closed. The gate 235 receives also the pulses from the timing track of the program drum PC (FIG. 1(a-a)). All the timing pulses cease.

Therefore, unless the compare alarm flip-flop F707 is reset by the eighth timing pulse T8 from the first equal circuit 20 (FIG. 1(d-c)) in a timely manner, the machine stops operation in the same cycle in which the compare alarm flip-flop F707 is set. The status level then high remains high.

Note that the comparison is effective in the operations B, L, A, R, S and M during the RI cycle. With any of the operation levels B, L, A, R, S or M high, the gate 748 passes the sixth timing pulse to set the compare alarm flip-flop F707 during the high status level RI. Recall that the contents of each of the L and R registers 18 and 19 (FIGS. 1(b-c) and 1(d-c)) are derived, respectively, from the outputs of the two adders and duplicated BCDC 17 in these operations. If one of the adders and duplicated BCDC 17 makes an error, then the first equal circuit 20 does not pass the eighth timing pulse to reset the compare alarm flip-flop F707 (FIG. 1(a-e)). The ma-

chine then stops in the status level RI during that cycle in which the error occurred, as no further timing pulses are generated, as just explained above, unless the compare alarm flip-flop F707 is reset in a timely manner. Hence the check is made immediately before entry of the results of these arithmetic operations into the HSM 15, 16.

If the contents of the L register 18 (FIG. 1(b-c)) and the R register 19 (FIG. 1(d-c)) are equal, the first equal circuit 20 passes the seventh timing pulse T7 to the reset terminal R of the compare alarm flip-flop F707 (FIG. 1(a-c)) to reset this flip-flop. Accordingly, the "one" terminal of the flip-flop F707 is at a low level, and the output of the inverter I10, that is, the "no alarm" lead, is high. Therefore, after a slight delay in the delay circuit D10, the gate 1301 passes the eighth timing pulse T8 to generate the eighth delayed timing pulse T8a and a new status level can be selected through the appropriate status transition gate. Note that unless the eighth delayed timing pulse T8a is generated, no new status level is possible. Also, the pulse from the reset track of the program drum PD may be passed through the gate 150 to reset the drum counter DC. Further, the gate 228 (FIG. 1(a-c)) is closed because the compare alarm flip-flop F707 (FIG. 1(a-c)) is reset. Thus, the flip-flop F214 (FIG. 1(a-b)) remains in its set condition, the gate 235 (FIG. 1(a-c)) is open, and timing pulses can be generated.

In the operation verify, on the detection of the desired quality, and if no ISS from the left HSM 15 is detected, the machine stays in the status level RO (that is with the status level RO high) for another cycle of the timing pulses. In the next RO cycle, the next least significant characters of the two items are compared in the same manner as that just described. If these two items are equal, and no item separation symbol is encountered, the machine continues in still another RO cycle, etc.

If an ISS is read out of the left HSM 15 (FIG. 1(c-c)) into the Y register 13 (FIG. 1(c-d)), at the sixth timing pulse T6, in the manner described above, then the left symbol recognition circuits 22 respond to the ISS. The ISSL lead (FIG. 1(c-d)) is then at a high level. The status transition gate 1209 (FIG. 1H) is primed. Note that if an ISS is not read out of the right HSM 16 at the same time as from the left HSM 15 that there is no output pulse from the first equal circuit 20. In this event, the compare alarm flip-flop F707 (FIG. 1(a-c)) is not reset. Therefore, the delayed eighth timing pulse T8a cannot pass through the gate 1301 (FIG. 1(a-c)) to produce the eighth delayed timing pulse T8a, and also generation of timing pulses ceases. However, assuming that the eighth delayed timing pulse T8a is provided, the status transition gate 1209 (FIG. 1H), primed by the ISSL lead, passes this eighth delayed timing pulse T8a to cause the status level IC to be selected as high.

Although no actual alarm circuit is indicated as connected to and responsive to the "no alarm" voltage from the no alarm lead, one may be provided if desired. However, if the panel lights suggested heretofore are connected to the different status levels, the mere fact that one status level is high a sufficiently long time to be noted by a continuous lighting of the particular panel level, indicates that the eighth delayed timing pulse T8a is possibly not being produced. It would be readily ascertained whether or not this was due to a low voltage on the "not alarm" lead. A simple alarm circuit might consist of an ordinary incandescent lamp (not shown) connected between the "not alarm" lead and the low voltage level. Note that in the event of an equality, the "not alarm" lead is low only for $2\frac{1}{2}$ microseconds or so, and an ordinary incandescent lamp would not have time to flash unless the compare alarm flip-flop F707 were to remain in its set condition and failed to be reset by the output of the first equal circuit 20, or for some other cause. Note also

that the machine stops in the status level in which the error is detected, in the event of an error.

5.14.3 Sequence of Status Levels

The instruction verify is employed for comparing two items for identity. With reference to the status level flow diagram for the instruction V, FIGURE 25, the instruction is first staticized in the status levels RO01, RO02, and RO03. The machine then selects the status level RO. In the RO status level the least significant character of the item in the left HSM 15 is compared with the least significant character of the other item in the right HSM 16. If the two characters are the same, the machine enters another RO cycle. In the second RO cycle, the next least significant characters of each item are compared. The machine continues in RO cycles, unless two non-identical characters are read, indicating an error. If an error is found, the machine is stopped in the RO cycle in which the error occurs. If no error is found, the machine continues in RO cycles until the ends of the items are reached. Note that only the left symbol recognition circuits 23 are used to check for the item separation symbol. If an item separation symbol is not found in the other character, an error is indicated and the machine is stopped before selecting the next status level. On recognition of the item separation symbol, the machine selects the status level IC, instruction complete.

5.15 Transfer of Control (Unconditional) (Operation T) Operation Level T High

The operation T is staticized during the status levels RO01, RO02 and RO03 in the same manner as most of the other instructions. The operation level T is high as soon as the status level RO01 is completed. The A and B sections of the instruction are not used. Therefore, the instruction is staticized as follows:

O Section	A Section	B Section	C Section
Code No. for transfer of control operation.	Not used....	Not used....	Drum line number of first line of first instruction to be surged after transfer.

5.15.1 Additional Components

A status transition gate 1217 (FIG. 1H) is provided having three inputs, one from the operation level T, a second from the status level RO03, and a third from the eighth delayed timing pulse T8a. The output of the status transition gate 1217 is applied to the set RE lead.

5.15.2 Machine Operation

Note that when the status level RO03 is high, after the status level RO01 is high while the instruction T is being staticized, the gate 1137 (FIG. 1(f-e)) passes the sixth timing pulse T6 to reset each of the previous result flip-flops 49.

Accordingly, each of the previous result flip-flops 49 is in reset condition after the status level RO03 is high, when the instruction T is staticized. During the high status level RO03, the drum line number (in binary form) of the first instruction to be surged coded as the last one-third of the instruction T, is stored in the C register 28 (FIG. 1(c-a)) (see secs. 4.2.3 and 4.2.4 hereinabove).

The gate 240 (FIG. 1(a-a)) is primed by the high operation level T and the high status level RO03 to pass the seventh timing pulse T7 to reset the program counter PC and to reset the program subcounter PSC (FIG. 1(a-b)).

The gate 114 (FIG. 1(a-a)) is primed by the "zero" terminal of the previous result all nines flip-flop F1103 and the high operation level T to pass the eighth timing pulse T8 to open the gates 115. Remember, now, that the drum line number of the first instruction to be surged

is held in the C register 28 (FIG. 1(c-a)). This drum line binary number is now transferred through the gates 115 (FIG. 1(a-a)) into the program counter PC.

The status transition gate 1217 (FIG. 1H) now passes the eighth delayed timing pulse T8a to select the status level RE to follow the status level RO03.

While the status level RE is high, the program drum PD is searched by the machine for the drum line specified in the program counter PC and the required group of instructions starting at this specified drum line is surged into the memory. The surge in the status level RE is described hereinabove (sec. 4.4) and therefore is not again described here.

5.15.3 Sequence of Status Levels

In this instruction a new group of instructions is to be surged from the program drum PD into the HSM 15, 16 starting at a drum line specified. The instructions of this new group are then executed by the machine.

The operation unconditional transfer of control T is staticized during the status levels RO01, RO02 and RO03. See FIGURE 26, status level flow diagram for unconditional transfer of control T.

The machine then selects the status level RE to be high and surges instructions from the drum starting at the drum line specified in the T instruction currently being executed.

The instruction for unconditional transfer of control T allows the programmer to break into, or out of, a sequence of instructions, for subroutines or the like, without any condition being attached.

5.16 Conditional Transfer of Control (Operation C)— Operation Level C High

The instruction for conditional transfer of control C is staticized in the status levels RO01, RO02, and RO03 in the manner similar to other instructions, as follows (see also FIG. 12):

O Section	A Section	B Section	C Section
Code No. for conditional transfer of control operation.	Nine most significant digits of drum line number of next instruction if previous result zero.	The three highest order bits of this section are the three least significant digit of drum line number of next instruction if previous result zero (remaining bits not used).	Drum line number of next instruction if previous result negative.

There are four possibilities in the operation conditional transfer of control C, or four conditions which are recognized. The four conditions are:

- (1) Previous result positive.
- (2) Previous result zero positive.
- (3) Previous result zero negative.
- (4) Previous result negative.

The condition which prevails depends on the output of the adder. Sections 5.1.12 and 5.1.13 above, on decimal addition of numbers, describes the conditions under which the previous result flip-flops 49 (FIG. 1(f-d)) are set or reset. It is these conditions to which the conditional transfer of control differently responds.

5.16.1 Additional Components

For this operation, conditional transfer of control C, a status transition gate 1205 (FIG. 1H) is provided having five inputs, one from the operation level C; a second from the status level RO03; a third from the "zero" output of the previous result negative flip-flop F1109; a fourth from the "zero" output of the previous result zero flip-flop F1101; and the fifth input from the eighth delayed timing pulse T8a. The output of the status transition gate 1205 is applied through "or" circuits to the "set IC" lead.

A status transition gate 1216 (FIG. 1H) is provided having four inputs, one from the status level RO03; a second from the operation level C; a third from an "or" circuit having an input from the "one" terminal of the previous result zero flip-flop F1101 (FIG. 1(f-d)) and another from the "one" terminal of the previous result negative flip-flop F1109 (FIG. 1(f-d)); and the fourth input to the status transition gate 1216 (FIG. 1H) is from the eighth delayed timing pulse T8a. The output of the status transition gate 1216 is applied to the "set RE" lead.

Note that in the previous status level RO03, the gate 1137 (FIG. 1(f-e)) is not primed to reset the various previous results flip-flops, as for unconditional transfer of control.

5.16.2 Detailed Operation

Considering the four conditions successively:

5.16.2.1 Previous Result Positive

During the status level RO03, in which the conditional transfer of control operation is staticized, if the previous result was positive, the previous result negative flip-flop F1109 (FIG. 1(f-d)), and the previous result zero flip-flop F1101, are both in their reset condition. Therefore, the status transition gate 1205 (FIG. 1H) passes the eighth delayed timing pulse T8a to the set IC lead. The status level IC is then high.

5.16.2.2 Previous Result Zero Positive

If, during the status level RO03 high during which the conditional transfer of control operation is staticized, the previous result zero flip-flop F1101 (FIG. 1(f-e)) is in the set condition and the other previous result flip-flops 49 are reset. Note that the gate 240 FIG. 1(a-a)) is primed by the "one" output terminal of the previous result zero flip-flop F1101 (FIG. 1(f-e)).

The gate 240 (FIG. 1(a-a)) passes the seventh timing pulse T7 to reset the program counter PC and to reset the program subcounter PSC (FIG. 1(a-b)).

The previous result zero flip-flop F1101 "one" output terminal also primes the gate 101 (FIG. 1(a-a)) and the eighth timing pulse T8 is passed through the gate 101 and applied to the gates 102. The gates 102 are therefore opened to enter the contents of the A register 26 (FIG. 1(c-a)) and the three most significant bits of the B counter 11 (FIG. 1(d-b)) into the program counter PC.

The status transition gate 1216 (FIG. 1H) passes the eighth delayed timing pulse T8a to select the status level RE to be high.

A surge of instructions now follows with the status level RE, in the manner previously described hereinbefore, with the surge starting at the drum line specified by the present entry in the program counter PC taken from the A and B counters.

5.16.2.3 Previous Result Zero Negative

If the previous result was zero negative, the previous result all nines flip-flop F1103 and the previous result negative flip-flop F1109 are in their set condition during the status level RO03 in which the instruction for conditional transfer of control C is staticized.

The gate 240 (FIG. 1(a-a)) passes the seventh timing pulse T7 during the high status level RO03 to reset the program counter PC and the program subcounter PSC.

The gate 101 passes the eighth timing pulse T8 to open the gates 102. The twelve bits are transferred from the A register 26 and the B counter 11 as in the previous case.

The status transition gate 1216 (FIG. 1H) passes the eighth delayed timing pulse T8a to cause the status level RE to be selected as next high.

Note that the surge in the status level RE high which follows is the same as, and starts at the same drum line

as, that in which the condition was "previous result zero positive."

5.16.2.4 Previous Result Negative

With the status level RO03 high, and the operation conditional transfer of control being staticized, if the previous result was negative, the previous result negative flip-flop F1109 (FIG. 1(f-e)) is in the set condition, and the previous result all nines flip-flop F1103 is in the reset condition. The previous result zero flip-flop F1101 is also in the reset condition.

Therefore the gate 240 (FIG. 1(a-a)) passes the seventh timing pulse T7 to reset the program counter PC and the program subcounter PSC (FIG. 1(a-b)).

The gate 114 passes the eighth timing pulse T8 to open the gates 115. The twelve bits from the C register 28 are now passed through the gates 115 and entered in the program counter PC.

The status transition gate 1216 (FIG. 1H) passes the eighth delayed timing pulse T8a to cause the status level RE to be high. The surge which follows with the status level RE high is the same as the surge previously described for the previous result zero (positive or negative) except that the drum line at which the surge starts is that presently in the program counter PC, and drawn from the C register 28.

5.16.3 Sequences of Status Levels

The instruction C is used to select one of three possible sequences of instructions on the basis of whether the result of a previous operation was positive, zero, or negative. This is a so-called "branch instruction."

Refer to the status flow diagram, FIG. 27. The instruction is first staticized in RO01, RO02, and RO03. If the result of the previous operation was positive, when the instruction C is staticized, the machine selects the status level IC. The next instruction to be selected, in this event, is the next instruction listed in the program (if any). This may be considered a "straight through" path.

If a previous result was zero, at the end of the instruction for conditional transfer of control, the machine selects the status level RE to be high. Therefore a new group of instructions is surged from the drum into the HSM 15, 16. The drum line of the first instruction to be surged is stored in "A" (and part of the "B") part of the instruction, in the A and B counters 10 and 11.

If the previous result was negative, at the end of the C instruction the machine selects the status level RE. A new group of instructions is surged from the drum into the HSM 15, 16. The drum line of the first instruction to be surged in this event is contained in the C register 28. The drum line on which a surge starts if the previous result was negative, and the drum line on which a surge starts if the previous result was zero, may be different lines or the same line. If a surge of instructions is required, after this surge is completed, the machine selects the status level RO01 and begins operation on the first instruction surged.

The operation conditional transfer of control C may be employed, for example, in programming division, because division is not provided directly in this machine but must be programmed. Conditional transfer of control may be used to have the machine follow a subroutine conditionally. Other examples for the use of conditional transfer of control for solving various problems will be readily apparent from the foregoing, to those skilled in programming.

5.17 Set Up—Operation Level P High

In the course of the program, it is sometimes desired to select a group of instructions, such as a subroutine, which is not found in the main program, and then return to the main program. The two instructions "set-up" (which is the one now being described) and "refer," to be described shortly, are employed for this purpose.

The instruction set-up "stores" in the HSM 15, 16 the drum line number of the first instruction to which the machine is to return after the subroutine is completed.

5.17.1 Additional Components

A three-input status transition gate 1259 (FIG. 1G) is provided having as one input the status level RO03, as a second input the operation level P, and as the third input the eighth delayed timing pulse T8a. The output of the status transition gate 1259 is applied to the "set RI" lead.

A pair of gates 638 (FIG. 1(c-b)) and 691 (FIG. 1(d-b)) are provided. Each of the gates 638 and 691 are three-input gates, one input of which is the status level RI, second input of which is the operation level P, and the third input of which is the first timing pulse T1. The high output of the gate 638 (FIG. 1(c-b)) is applied through a suitable "or" circuit as shown to open the gates 640 between the A counter 10 and the address circuits of the left HSM 15 (FIG. 1(c-c)). The high output of the gate 691 (FIG. 1(d-b)) is applied through suitable "or" circuits as shown to open the gates 670 (FIG. 1(d-b)) between the B counter 11 and the address circuits of the right HSM 16 (FIG. 1(d-c)).

Two sets of gates 702 (FIG. 1(b-c)) and 830 (FIG. 1(e-c)) are provided, each set consisting of seven gates. Each gate of each set has four inputs. One input is from the operation level P, a second input is from the status level RI, and a third input is from the second timing pulse T2. The fourth input to each of six of the gates 702 is, respectively, from the six "most significant" (2⁶ to 2¹¹ bits), stored in the C register 28 (FIG. 1(c-a)). In other words, the different "one" output terminals of the 2⁶ to 2¹¹ bit flip-flops of the C register 28, respectively, are connected to the six gates 702 (FIG. 1(b-c)). One of the gates 702 receives its fourth input from the 2⁵ bit flip-flop of the parity register 29 (FIG. 1(d-a)). Note that the parity bit was stored in the parity register in the status level RO03 during which the instruction for "set-up," was staticized. Similarly, the fourth input to each of the gates 830 (FIG. 1(e-c)) comes from the six least significant bits, respectively, of the output of the C register 28 (FIG. 1(c-a)). The seventh or parity bit comes from the 2⁴ bit flip-flop of the parity register 29 (FIG. 1(d-a)). The output of the gates 702 (FIG. 1(b-c)) are applied to the various set terminals S of the L register 18. The outputs of the gates 830 (FIG. 1(e-c)) are applied to the various set terminals S of the R register 19 (FIG. 1(d-c)).

A status transition gate 1210 (FIG. 1H) has three inputs, the first from the status level RI, the second from the operation level P, and the third from the eighth delayed timing pulse T8a. The output of the status transition gate 1210 is applied to the "set IC" lead.

5.17.2 Machine Operation

The operation P (set-up) is staticized as follows (see also FIG. 12):

O Section	A Section	B Section	C Section
Instruction Code No. for "Set Up."	Location in left HSM 15 of the six most-significant digits of the drum line No.	Location in right HSM 16 of the six least-significant digits of the drum line No.	Drum-line number to be stored.

After the instruction for operation P is staticized, the eighth delayed timing pulse T8a that occurs during the high status level RO03 in which the instruction is staticized is passed by the status transition gate 1259. The status level RI is selected to be high.

The gate 691 (FIG. 1(d-b)) passes the first timing pulse T1 to open the gates 670. The contents of the B counter 11 are passed through the gates 670 to the address circuits of the right HSM 16 (FIG. 1(d-c)). Simi-

larly, the gate 638 (FIG. 1(c-b)) passes the first timing pulse T1 to open the gates 640 through which the contents of the A counter 10 enter the address circuits of the left HSM 15 (FIG. 1(c-c)). The gate 860 (FIG. 1(e-c)) passes the first timing pulse T1 to reset the R register 19 (FIG. 1(d-c)) and the L register 18 (FIG. 1(b-c)).

The second timing pulse T2 now opens the gates 702 (FIG. 1(b-c)) leading to the L register 18, and also the gates 830 (FIG. 1(e-c)) leading to the R register 19 (FIG. 1(d-c)). The six most significant bits recorded in the C register 28 (FIG. 1(c-a)) together with the parity bit from the 2⁵ bit flip-flop of the parity register 29 (FIG. 1(d-a)) are transferred through the gates 702 (FIG. 1(b-c)) into the L register 18. Also, the six least significant bits entered in the C register 28 (FIG. 1(c-a)) are now passed through the gates 830 (FIG. 1(e-c)) together with the parity bit from the 2⁴ bit flip-flop of the parity register 29 (FIG. 1(d-a)) into the R register 19 (FIG. 1(d-c)).

The left read-in gate 721 (FIG. 1(c-c)) applies a high level to condition the left HSM 15 read-in circuits, and also to prime the gate 799. The gate 799 passes the fifth timing pulse T5 to open the gates 722. Also, the right read-in gate 850 (FIG. 1(d-c)) applies a high level to condition the read-in circuits of the right HSM 16, and to open the gate 899. The gate 899 passes the fifth timing pulse T5 to open the gates 851. The contents of the L register 18 (FIG. 1(b-c)) are now passed through the gates 722 into the left HSM 15 (FIG. 1(c-c)) at the place addressed by the contents of the A counter 10. Similarly, the contents of the R register 19 (FIG. 1(d-c)) are now passed through the gates 851 and entered in the right HSM 16 at the place addressed by the contents of the B counter 11.

The status transition gate 1210 (FIG. 1H) passes this pulse T8a to cause the status level IC to be selected.

5.17.3 Sequence of Status Levels

As an example of the use of the "set up" and "refer" instructions, a possible program might employ the instructions as follows: The instruction to set-up is arranged to store a drum line number. Then the instruction transfer of control (T) transfers control to a subroutine. At the end of the subroutine, there is included an instruction "refer" (Operation Q) which uses the drum line stored in the HSM 15, 16 by the previous instruction set-up and thereby returns to the main program.

The combination of set-up and refer instructions allows the insertion of a given subroutine at many points in the program and then returning to these points after completing the subroutine. These instructions are therefore considerable assistance to the programmer in reducing the total number of stored instructions in the program.

Referring to the status level flow diagram of FIGURE 28, the instruction P (for set-up) is staticized in the status levels RO01, RO02, and RO03. The machine then selects the status level RI. The drum line to which reference is later to be made is then read into the HSM 15, 16 for future reference.

The machine then selects the status level IC for instruction complete.

5.18 Refer (Operation Q)—Operation Level Q High

This operation is used as explained in the preceding section.

5.18.1 Additional Components

A set of twelve, two-input gates 128 (FIG. 1(a-a)) is provided. The twelve gates 128 are connected with six of the gates 128 between the outputs (ignoring the parity bit) of the left HSM 15 (FIG. 1(c-c)) as one input and the six set terminals of the corresponding six most significant bit flip-flops (highest order) of the program counter PC; and the other six of the gates 128 (FIG. 1(a-a)) are connected between the right HSM 16 (FIG. 1(d-c)) out-

puts as one input, ignoring the parity bit, and the set terminals of the six lowest order flip-flops of the program counter PC. A three-input gate 127 has as one input the status level RO, as a second input, the operation level Q, and as a third input, the sixth timing pulse T6. The gates 128 each receive as the second input the output of the gate 127.

5.18.2 Machine Operation

The instruction is staticized as follows (see also FIG. 12):

O Section	A Section	B Section	C Section
Instruction Code No. for refer.	Location in left HSM 15 of one half the drum line.	Location in right HSM 16 of the other half of the drum line.	Not used.

Note that in the status level RO03, the gate 240 (FIG. 1(a-a)) passes the seventh timing pulse T7 to reset the program counter PC and the program subcounter PSC.

The status transition gate 1264 (FIG. 1G) passes the eighth delayed timing pulse T8a to select the status level RO to be high.

The gate 699 (FIG. 1(c-b)) passes the first timing pulse T1 to open the gates 640. The gate 692 (FIG. 1(d-b)) passes the first timing pulse T1 to open the gates 670. Accordingly, the left HSM 15 (FIG. 1(c-c)) is addressed with the contents of the A counter 10 passed through the gates 640 and the right HSM 16 (FIG. 1(d-c)) is addressed by the contents of the B counter 11 (FIG. 1(d-b)) passing through the gates 670.

The left and right read out gates 730 (FIG. 1(c-c)) and 862 (FIG. 1(d-c)) respectively apply high levels to the left HSM 15 and right HSM 16 read out circuits to condition both memory sections for reading out.

The gate 127 (FIG. 1(a-a)) passes the sixth timing pulse T6 to open the gates 128. The six most significant binary digits of the reference drum line are transferred from the left HSM 15 (FIG. 1(c-c)) through six of the gates 128 into the program counter PC (FIG. 1(a-a)). The six least significant binary digits or bits of the drum line are transferred from the right HSM 16 (FIG. 1(d-c)) through the other six gates 128 to the program counter PC. Accordingly, the drum line stored in the HSM 15, 16 at the address specified in the instruction refer is now entered in the program counter PC.

The status transition gate 1221 (FIG. 1) passes the eighth delayed timing pulse T8a to cause the status level RE to be selected as high.

During the status level RE, the search for the drum line entered in the program counter PC and the surge of instructions into the HSM 15, 16 take place as previously described.

5.18.3 Sequence of Status Levels

Referring to the flow diagram, FIG. 29, for the operation Q, the instruction is first staticized in RO01, RO02, and RO03. The machine then selects the status level RO, during which the first drum line number of the next instruction required in the program is extracted from its location in the HSM 15, 16. This drum line number, for example, may have been stored in this location in the HSM 15, 16 in a previous instruction to set-up.

The machine then selects the status level RE. In this status level, the machine searches the drum for the drum line the number of which was extracted from the HSM 15, 16. The number of instructions in the surge is determined by the programmer, as before, and set manually, preferably for the entire program. The machine then selects the status level RO01 and begins operating on the first instruction that was surged.

5.19 Stop (Operation F)—Operation Level F High

This instruction is carried out during the status level RO01 during which the instruction is staticized. Only the O section of the instruction is used.

When the status level RO01 is high, and the instruction is being staticized, the gate 629 (FIG. 1(a-b)) passes the first timing pulse T1 to open the gates 630 and the gates 630a. The entry in the program subcounter PSC is now applied to the address circuits of the left HSM 15 (FIG. 1(c-c)) and to those of the right HSM 16 (FIG. 1(d-c)).

The left and right read-out gates 730 (FIG. 1(c-c)) and 862 (FIG. 1(d-c)) respectively apply a high level to actuate the left HSM 15 and right HSM 16 read-out circuits respectively. The gates 1402 are opened by virtue of the high status level RO01 applied thereto. Therefore, at the fifth timing pulse T5, the contents of the left HSM 15 (FIG. 1(b-a)) at the address specified by the contents of the program subcounter PSC (FIG. 1(a-b)) and applied during the previous first timing pulse T1, are transferred into the O register 30 (FIG. 1(b-a)). The O register 30 then activates the operations matrix OM, causing the operation level F to become high.

The operation matrix OM reaches a quiescent value approximately four microseconds after the information bits are read into the O register 30. Note that the gate 1301 (FIG. 1(a-c)), through which the eighth delayed timing pulse T8a is generated, is primed by the "no alarm" lead from the inverter I10, the input to which is received from several "or" circuits, as shown. One of these last mentioned "or" circuits has applied to it the operation level F (see near the compare alarm flip-flop F707 in FIG. 1(a-c)). Accordingly, when the operation level F is high, the input to the no alarm inverter is high, and the "no alarm" lead is at a low level. The gate 1301 (FIG. 1(a-c)) is not primed, and no eighth delayed timing pulse T8a is generated, and no new status levels can be selected.

The gate 228 (FIG. 1(a-c)) passes an eighth delayed timing pulse T8a (applied from the delay circuit D8 of FIG. 1(a-d)) and designated T8c which is then applied to the reset terminal R of the flip-flop F214 (FIG. 1(a-b)). The gate 228 (FIG. 1(a-c)), it may be noted, is primed by the same level applied to the inverter I10 and includes the high operation level F from "or" circuits as mentioned above. The "one" output terminal of the flip-flop F214 (FIG. 1(a-b)) is thus at a low level, and the gate 235 (FIG. 1(a-c)) is thus closed. With the gate 235 closed, no further pulses can be passed from the timing track on the program drum PD (FIG. 1(a-a)). The generation of all the timing pulses is therefore blocked. The machine can now be started up again manually, as described hereinbefore, and the machine may then proceed to staticize the next instruction when so started.

The stop instruction F is used to stop the machine as a "programmed" stop. The instruction is staticized in the status level RO01. The first one-third of the instruction contains the stop information in the most significant six bits of the instruction. The machine is stopped at the end of the first RO01 cycle, at the eighth timing pulse T8.

5.20 Various Alarm Circuits

At this point it may be noted that three flip-flops F216, F217, and F218 (FIG. 1(a-c)) are provided, which may be considered respectively as a physical end of tape, HSM 15 parity, and HSM 16 parity flip-flops respectively. The left HSM 15 parity flip-flop and the right HSM 16 parity F217 and F218 respectively are employed if the parity is not correct. Circuits (not shown) are provided at the output of each of the left HSM 15 and the right HSM 16 which provide an output pulse if the parity at the seven output leads of the left HSM 15 or the right HSM 16, as the case may be, is incorrect. The output pulse

is applied to the appropriate left or right HSM 15 or HSM 16 parity flip-flop F217 or F218. Accordingly, if there is a lack of parity in the output of one section of the memory, left or right, a pulse is applied to the appropriate parity flip-flop F217 or F218 to set that parity flip-flop. The "one" output of the parity flip-flops is applied through the suitable "or" circuits, as shown, to the input of the no alarm inverter 110, these same "or" circuits receiving the output of the compare alarm flip-flop F707. The output of these "or" circuits is also applied as an input to the gate 228, as described hereinabove. Accordingly, in the event that the parity checking circuits provide an output, the "no alarm" inverter 110 input is at a high level, and the "no alarm" lead is at a low level. The gate 1301 is therefore closed and the eighth delayed timing pulse T8a cannot be generated. Also, the gate 228 passes a pulse (T8c) to reset the flip-flop F214, (FIG. 1(a-b)). The gate 235 now cannot pass pulses, and the generation of any further timing pulses is blocked. Therefore, the machine stops in the status level during which the incorrect parity output of the memory occurs.

The physical end of tape flip-flop F216 is provided in order to receive at its set terminal the output of a physical end of tape circuit (not shown). Such a circuit may sense the end of any input or output tape, as by a photocell circuit. The outputs of the end of tape circuits can be applied to suitable "or" circuits (not shown), so that if any end of tape is physically reached, a pulse is applied from such "or" circuits to the "set" terminal of the physical end of tape flip-flop F216. The "one" output terminal of the physical end of tape flip-flop F216 is applied through "or" circuits as shown to the input of the no alarm inverter 110. Accordingly if the physical end of any tape is reached, the physical end of tape flip-flop F216 is set. The input to the no alarm inverter is high, and the gate 228 (FIG. 1(a-c)) is primed. The no alarm lead is low, and the gate 1301 is closed, and the flip-flop F214 (FIG. 1(a-b)) is reset. Therefore the eighth delayed timing pulse T8a cannot be generated, and no further timing pulses can be generated, as explained above. The machine therefore stops with the status level that was high at the time the end of the tape was reached.

Note that there is a different end of tape signal from the gate 921 in the left symbol recognition circuits 22 (FIG. 1(b-d)). The operator is intended to apply a coded end of tape symbol magnetically on the magnetic tape. The physical end of tape flip-flop F216 is an additional precaution. Ordinarily, at the end of a message on the input tape, the encoded symbol for end of tape is magnetically written. The left symbol recognition circuits 22 recognize the end of the tape magnetically. The output of the ET gate 921 is high as soon as the end of tape symbol ET is entered in the Y register 13 (FIG. 1(c-d)). The output of the end of tape circuits 921 (FIG. 1(b-d)) is applied through a suitable "or" circuit to the gate 740 (FIG. 1(b-e)) in the operation N, during which information is written onto a tape. In operation N, the gate 740 receives the first timing pulse T1 from the gate 942. The first EM or ET flip-flop F706 (FIG. 1(b-e)) is therefore set. Consequently, the gates 609 and 610 (FIG. 1(b-d)) are closed. The input tape which may be running is therefore stopped. A new tape is entered, and the operation proceeds. Notice that the end of tape symbol ET cannot occur except when the beginning of a new message is expected, since the operator does not write an end of tape symbol or encode it magnetically except after the end of a message, and therefore after an end message symbol EM.

6. CONCLUSION

The information handling system of the invention has thus been described as particularly well adapted to receive information from magnetic tape, for example, and for transmitting information to magnetic tape, for example. The system gains great flexibility and opera-

tional advantages by the use of the status levels. Note that each status transition gate causes the selection of a high level, which is succeeded by another cycle in the same level or by the passing of a pulse by another status transition gate which selects still another level to be high. One and only one status level is high at any one time (except for the comparatively brief transition period). Each status level is applied to one or more of the status transition gates. Each status transition gate includes the application of a status level (or an equivalent level, as from a flip-flop) as a priming voltage. When a status transition gate passes the pulse to select a different status level, the status level applied to that transition gate is removed.

One and only one status level is high at a time. One and only one operation level is high at a time. Note that one or more status levels are employed to be high during the execution of an instruction, and during which execution only one operation level is high. Note that the only exception is in the operation for subtraction, in which the operation level for addition may be selected at the termination of the subtraction instruction. Even this, however, is not an exception to the general rule that for the execution of each instruction, one or more status levels are employed, selected by the different status transition gates; and one and only one status level is high at any one time, and one and only one operation level is high at any one time. It may be noted that, two outputs may be used for a single level. For example, two flip-flops might be used for providing a single level, each being set and reset with the other. Such a two flip-flop arrangement may be desirable to prevent overloading of a single circuit. The "one" outputs of these two flip-flops, taken together, nevertheless provide a single level in terms of logic.

The machine has great flexibility, and is readily arranged to be sequenced in partial response to the operands. The machine does not require fixed message of item lengths, and can perform a great variety of functions. Furthermore, the machine is readily modified, as by adding additional operation levels from the operation matrix, and by adding additional status levels and additional status transition gates. Also, the machine is readily modified by reducing components, for example, to use a single address system.

It is apparent that the employment of the status levels, as described, improves the program control of the computer.

What is claimed is:

1. In a computer for performing desired operations on one or more operands each having one or more characters represented by coded electrical signals, said computer comprising a generator of repeated cycles of timing pulses, a memory, an arithmetic unit, an input, an output, and program control circuits controlling the flow of information among said generator, said memory, said unit, said input, and said output, an improvement in said program control circuits comprising recognition circuits responsive to certain characters, operation level circuits for selecting at least one operation level in response to the operation to be performed, and status level circuits for selecting a sequence of status levels responsive jointly to the other of said circuits of said improvement and to said generator, said status level circuits comprising status level selection means having a set of terminals one corresponding to each said status levels, and one or more gates responsive jointly to said other of said program control circuits and to said generator, said selection means being responsive to a pulse applied to any one of said terminals to select the corresponding status level, each said terminal being connected to receive the output of at least one of said gates, certain of said terminals being connected to receive the output of more than one said gate, the outputs of said certain gates being applied to said leads through "or" circuits, said

status level selection means comprising a set of flip-flop circuits one corresponding to each said status level and having set and reset terminals, said terminals being connected through "or" circuits to said reset terminals and said "or" circuits outputs each individually to the set terminal of a corresponding one of said flip-flops through a delay circuit to delay the application of a set pulse longer than that of any reset pulse to said flip-flop circuits.

2. In an information handling system for performing desired operations on two operands each having one or more characters represented by coded electrical signals including one or more special characters indicating the end of an operand, said computer comprising a program control for controlling the flow of information in said system, said program control including means to generate repeated cycles of timing pulses, means for selecting an operation level, one for each said operation, and a memory from which said operands are withdrawn for performing the selected operation by pairs of characters, each character of a pair being that of a different one of said operands, the improvement in said program control comprising character recognition means responsive to the occurrence of said special character signals, means for selecting one of a plurality of status levels for the duration of each said cycle, and means controlling the sequence of status levels including a plurality of gates, each of the said gates receiving a said timing pulse, said gates being jointly responsive to said last-mentioned timing pulse, said recognition means, a said status level, and one of said operation levels, said selecting means including a plurality of bistable circuits one corresponding to each said status level, each said status level being provided by one output of said status level bistable circuits, said sequence controlling means comprising a set of leads, one corresponding to each said status level, means for applying a reset pulse to all of said bistable circuits from any one of said status level leads, and means for applying said pulse from any said lead to a corresponding bistable circuit after a delay.

3. In a system as claimed in claim 2, the said gates each receiving a certain one of said timing pulses.

4. In a system as claimed in claim 3, the said gates being arranged in groups, each group corresponding to a different status level, the outputs of each gate of each group being applied to said status level selecting means for causing selection of the status level corresponding to that group.

5. In an information handling system for performing desired operations on one or more operands each having one or more sequentially presented characters represented by coded electrical signals, means for generating repeated cycles of timing pulses, and means for selecting an operation level individual to each said operation, the improvement comprising means for selecting status levels, one for each component step of the operation to be performed, some said steps of some operations being in common with some said steps of other operations, each of said status levels having a duration of at least one said cycle, means for selecting the sequence of said status levels to perform the selected operation, said sequence selecting means including recognition means to which each character of each said operand is successively applied responsive jointly to the selected operation level, to the selected status level, and to the currently presented character signal, and means for modifying the sequence of status levels during a certain of said operations in response to whether or not a certain status level is for the first or for a second time selected in the performance of said certain operation.

6. In a system as claimed in claim 5, said modifying means including a bistable circuit.

7. In an information handling system for performing desired operations on one or more operands each having one or more sequentially presented characters represented by coded electrical signals, means for generating

repeated cycles of timing pulses, and means for selecting an operation level individual to each said operation, the improvement comprising means for selecting status levels, one for each component step of the operation to be performed, some said steps of some operations being in common with some steps of other operations, each said status level having a duration of at least one said cycle, means for selecting the sequence of said status levels to perform the selected operation, said sequence selecting means including recognition means to which each character of each said operand is successively applied and gates responsive jointly to the selected operation level, to the selected status level, and to the currently presented character signal, and means for modifying the said status level sequence in the performance of a specified operation in response to whether a certain status level is selected the first or a second time during said performance including a bistable circuit having an output connected to certain of said gates.

8. In an information handling system for performing desired operations on one or more operands each composed of characters represented by coded electrical signals comprising means to generate repeated cycles of timing pulses, the improvement comprising means to perform each said operation in component steps, each said step being completed during a single said cycle, and means including recognition means to which each character of each said operand is successively applied to select the succession of said steps in response to: the operation being performed, the operand character currently thus applied, and the step being performed; and means to continue said operation with one sequence of steps or another sequence of steps in response to whether or not a certain of said steps being performed occurred previously or did not occur previously in the course of the said operation being performed.

9. In an information handling system for performing desired operations on one or more operands each having one or more sequentially presented characters represented by coded electrical signals, said system having means to control the paths of flow of information therein comprising means for recognizing each character of a said operand and as thus presented, means to generate repeated cycles of timing pulses, means for selecting as an enabling level a different level one for each said operation, at least one further set of levels, and means responsive jointly to the recognizing means, the selected operation level, and the selected further level for selecting as an enabling level a level of said further set for the duration of the succeeding said cycle, the improvement in said system characterized by said information path control means including path changing means, effective in the course of performing one of said operations, for selecting a first set of paths of information flow in response to the first selection of a certain of said further levels, and for selecting a second, different set of paths of information flow in response to the second or subsequent selection of said certain of said further levels.

10. In a system as claimed in claim 9, said path changing means including a bistable circuit connected to said means to select a said further level to make the sequence of selection of said further levels during the course of said particular operation different after said second certain level selection from the sequence of selection of further levels after said first and before said second certain level selection during performance of said particular operation.

11. In a system as claimed in claim 9, said path changing means including a bistable circuit having during a performance of said particular operation one state preceding the first occurrence of said certain further level and another state after the occurrence of said certain further level.

12. In a system as claimed in claim 9, said path chang-

ing means including a bistable circuit, and means for recognizing the occurrence of said certain further level during the course of performing said particular operation, said last mentioned means controlling the state of said bistable circuit.

13. In a system as claimed in claim 12, said recognizing means including a gate receiving said particular operation level, and one of said timing pulses, the output of said gate being connected to said bistable circuit.

14. In a computer as claimed in claim 11, said further level selecting means including a gate for selecting said certain further level, said path changing means including a second gate having the same enabling levels as those for said first gate except for a timing pulse, said second gate having an output connected to said bistable circuit.

15. In an information handling machine in which an item is presented as a time sequence of characters each of coded electrical signals of a plurality of significant bits, said item having one of two or more mutually exclusive characteristics, said characteristic being indicated by each item character being of a recognizable one kind, an arrangement for recognizing and for storing recognition of said one characteristic comprising a bistable circuit having two stable states, means for initially placing said bistable circuit in one of said states, circuit means for recognizing characters of said one kind, means responsive to the concurrent presentation of the first of said characters and recognition only of said first character of an item as of said one kind by said recognizing circuit for placing said bistable circuit in its other stable state, and means responsive to the non-recognition by said recognizing means of a character of said item as being of said one kind for returning said bistable circuit to its one said stable state.

16. In an information handling machine in which an item is presented in successive characters of coded electrical signals, said item having one of two or more mutually exclusive characteristics, said one characteristic being indicated by each item character being of one certain recognizable kind, means for storing recognition of said one characteristic comprising a bistable circuit, means for placing said bistable circuit in one of its stable states before the presentation of the first said character, means responsive to the occurrence of a character of said one kind only as the first character only of said item for placing said bistable circuit in its other stable state, and means responsive to the occurrence of a character of said item of other than said one kind for returning said bistable circuit to its one state.

17. In an information handling system having means for presenting an item of successive characters each of coded electrical signals of a plurality of significant bits, said item having one and only one of two or more characteristics, said one characteristic being indicated by each item character being of a certain recognizable kind, the improvement comprising means for storing said one characteristic comprising a bistable circuit having one and another stable states, a recognition circuit for recognizing characters of said certain kind, means connecting said recognition circuit to said bistable circuit and responsive to the occurrence of a character of said certain kind as the first character only of said item for placing said bistable circuit in its said other stable state, and means connecting said recognition circuit to said bistable circuit and responsive to the occurrence of a character of said item of other than said certain kind for returning said bistable circuit to its said one state.

18. In a system as claimed in claim 17, said storing means further comprising means for placing said bistable circuit in said one of its stable states before presentation of the first said character.

19. In an information handling system having means for presenting an item of successive characters of coded

electrical signals, each character comprising a plurality of bits, said item having one of two characteristics, said one characteristic being indicated by each item character being of a certain recognizable kind, the improvement comprising means for storing said one characteristic comprising a bistable circuit having set and reset states, a recognition circuit for distinguishing between characters of said one kind and of a kind different from said one kind, gate means under control of said recognition circuit (1) for placing said bistable circuit in said set state on recognition of a character of said one kind by said recognition circuit as the first, and not as any later, character of said item presented and (2) for placing said bistable circuit in said reset state on recognition of any character of said item presented as a character of said different kind.

20. In a system as claimed in claim 19, said storing means further comprising means for placing said bistable circuit in its reset state before the first character of said item is presented.

21. In a system as claimed in claim 19, said recognition circuit having two different outputs responsive to characters of said one kind and applied to said gate means, one being in an enabling state to open a gate when the other is not, and the other being in an enabling state when the one is not.

22. In a system as claimed in claim 19, said gate means comprising two gates, the output of one of said gates being applied to set said bistable circuit and the other gate output being applied to reset said bistable circuit.

23. In a system as claimed in claim 19, said recognition circuit having two outputs one of which is selected as an enabling level on recognition of a character of said one kind, the other of which is selected as an enabling level on recognition of a character of the said other kind, said gate means comprising two gates, the output of one of said gates being applied to set said bistable circuit and the other gate output being applied to reset said bistable circuit, said one recognition circuit output being applied to said one gate and the said other recognition circuit output being applied to said other gate.

24. In a computer having means for presenting items successive in time each of numeric digit characters successive in time of coded electrical signals, the combination of a bistable circuit and means for placing said circuit in one stable state in response to all the digit characters of an item being of one digit and in the other stable state in response to any one or more digit character of an item being different from said one digit, said last-named means comprising a recognition circuit responsive in one way to signals representing said one digit and in a different way to signals representing a said different digit, said recognition circuit being connected to said bistable circuit to place said circuit in said one state if and only if the first presented numeric character signals of an item represent said one digit, and to place said bistable circuit in said other state if the first or any succeeding character signals of an item represent a said different digit, whereby after presentation of any item said bistable circuit is in one state or the other according to whether (1) each and every one of the characters of said item represented said one digit or (2) the characters of said item included one or more of a said different digit.

25. In a computer for performing desired operations on one or more operands comprising one or more characters represented respectively by a time sequence of one or more coded electrical signals, said computer having a program control for controlling the flow of information in said computer including means to select as an enabling level one of a set of operation levels in response to a said operation to be performed, means to generate respective cycles of timing pulses, and means to select as an enabling level one of a second set of status levels for the duration of any one of said cycles, each said operation being performed during cycles of said status levels, and

said computer having an arithmetic unit for performing arithmetic computations the results of which are available by successive character signals at the said arithmetic unit output, each said result signal being available during selection of one of said status levels, the improvement in said program control comprising a means for storing the information as to whether all the digits of a computation of said arithmetic unit performed in response to selection of a certain of said operation levels are a certain digit, said storing means comprising a bistable circuit, having stable set and reset states, and corresponding set and reset input terminals, a recognition circuit at the output of said arithmetic unit, a first gate connected between said recognition circuit and said set terminal, a second gate connected between said recognition circuit and said reset terminal, a second bistable circuit having set and reset states, corresponding set and reset input terminals, and corresponding "one" and "zero" output terminals, said first gate receiving the "one" enabling output of said second bistable circuit, and means responsive to said certain operation level and to said certain status level for placing said second bistable circuit in its set condition during the availability of the first character signal of the result and in its reset condition during the availability of other character signals of the result.

26. In a computer as claimed in claim 25, the last-named means therein further comprising a further gate receiving that said certain status level during which said result signal is available and one of said timing pulses, the output of said last-named gate being applied to reset said second bistable circuit.

27. In a computer for performing operations in one or more operands each having one or more characters correspondingly represented by a time sequence of one or more coded electrical signals, said computer comprising a program control to control the flow of information in said computer including means to generate repeated cycles of timing pulses, means for selecting as an enabling level a different level one for each said operation, a further set of status levels, and means for selecting as an enabling level a level of said further set for the duration of each said cycle, and an arithmetic unit having an output available at a selected timing pulse in a cycle of a chosen operation with a predetermined selected status level, the improvement in said program control comprising means to recognize a predetermined coded character signal at the output of said unit, a first bistable circuit, means to place said first bistable circuit in one state at the initiation of said operation and to place said first bistable circuit in a second state during said predetermined status level and on occurrence of a certain timing pulse later in the cycle than said selected pulse, gate means under control of said first bistable circuit and said recognition circuit, and a second bistable circuit connected to receive the output of said gate means whereby said second circuit is in one stable state only if the first and all succeeding characters of a said unit output correspond to said predetermined coded signal.

28. In an information handling system for performing operations and comprising means for generating successive cycles of timing pulses, means for presenting in time sequence items each comprising one or more serially presented characters of coded electrical signals, means for selecting as an enabling level a different level of a set of operation levels one for each of said operations to be performed, means for selecting as an enabling level one at a time for the duration of a said cycle a level of a set of status levels during a particular one of which and during a preselected operation each said character signal is presented, the combination comprising a recognition circuit having two outputs one respectively being an enabling level effective on the presentation of one kind of said character signals and the other effective on the presentation of any of said character signals different from said one kind, first and second bistable circuits each having set

and reset terminals and corresponding "one" and zero outputs, and a gate receiving the "one" output of said first bistable circuit and one of the outputs of said recognition circuit, said gate having its output applied to the set terminal of said second bistable circuit, said first bistable circuit being in its set condition only during the presentation of the first character of a said item.

29. In a system as claimed in claim 28, said gate output from said recognition circuit when available being available at a certain timing pulse in a said cycle.

30. In a system as claimed in claim 29, said combination comprising a second gate receiving said particular one status level and a later timing pulse, the output of said second gate being applied to reset said first bistable circuit.

31. In a system as claimed in claim 30, said combination further comprising means for setting said first bistable circuit before the said status level is first selected in the course of said predetermined operation.

32. In an information handling system for performing one or more operations in one or more operands of items having a time sequence of one or more characters represented by coded electrical signals and comprising means to generate repeated cycles of timing pulses, the improvement comprising means to perform each said operation in component steps, each said step being completed during a single said cycle, a first bistable circuit, and means to modify the flow of information in the system during a specified operation different ways in response to whether or not at any time previously during a single performance of said operation, a certain one of said component steps has occurred more than once in the performance of said specified operation, said flow modifying means comprising a second bistable circuit set or reset during said single performance in accordance with whether said certain one step has occurred or not during said single performance, and a gate enabled by said second bistable circuit before the occurrence of said step during said single performance and disabled thereafter throughout the course of said single performance of said operation, said gate output being connected to said first bistable circuit.

33. In an information handling system as claimed in claim 32, said improvement further comprising a recognition circuit receiving character signals serially one character signal during each said one step, the output of said circuit being applied to said gate.

34. In a system operating in different successive timed sequence and which adds or subtracts two operands of variable, non-standard maximum length, each operand being composed of characters represented by electrical signals and having at least a portion of numerical value, said operands including special signals denoting the sign and termination of an operand, an arrangement for providing control signals for initiating said successive sequences comprising means responsive to said two operands for recognizing said special terminating signals, means responsive to addition and subtraction results and to said terminating signal recognizing means for determining the sign of the results, a control signal generating network responsive to enabling signals, and gating means responsive to said terminating signal recognizing means, said sign determining means, and said control signal generating network for providing enabling signals for said control signal generating network.

35. In a system which operates in timed sequences to withdraw two characters represented by electrical signals from storage, to add operands each comprising a train of said characters in complemented and non-complemented form, and to provide a result including carry from each addition, said characters being represented in a binary-decimal code and having a part at least of numerical value, said operands also including character signals representing special sign and terminating symbol characters, an arrangement for providing control signals

for said sequences comprising means for recognizing said special terminating character signals, carry storage means responsive to said results, means responsive to the numerical value signals of said results and to said special character recognizing means for detecting sign signals, control signal generating means including a plurality of bistable elements so arranged that only one of said bistable elements is in an active state at a given time, and means including a plurality of coincidence gates coupled to said bistable elements and responsive to said recognizing means, said carry storage means, and said sign detecting means for providing conditioning signals to place desired ones of said bistable elements in the active state.

36. In an information handling system for performing desired operations on one or more operands represented by a time sequence of characters each represented by coded electrical signals and including a limit of operand character, said system comprising a program control for controlling the paths of flow of information in said system, means to generate timing pulses, the improvement in said program control comprising recognition means sequentially receiving each character of a said operand, means for sequentially selecting status levels for performing each said operation in component steps corresponding respectively to different status levels, each said step being completed during a single said cycle, said selecting means being pointily responsive to said recognition means, the current operation, and the currently selected status level, and means for causing selection of a status level sequence selected by said selecting means for continuing a specified operation on recognition of a specified character other than said limit of operand character by said recognition circuit during a specified status level to be different, in response to second or subsequent recognition by said recognition circuit of said specified character, from the sequence selected by said selecting means for con-

tinuing said specified operation in response to the first recognition of said specified character by said recognition circuit.

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