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W. S. PIKE

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REVERSIBLE COUNTER

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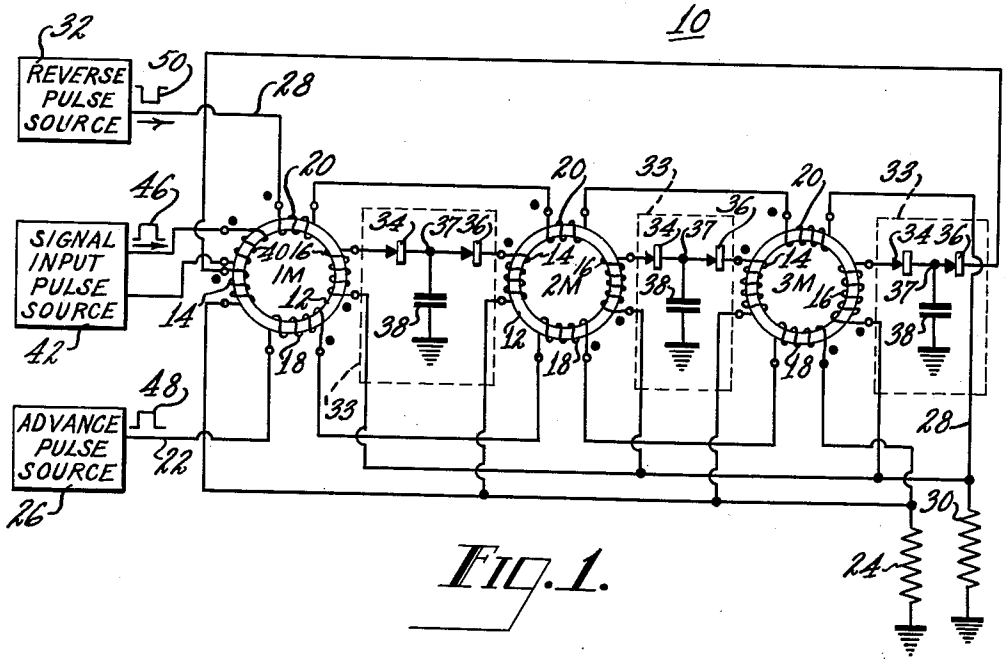


FIG. 1.

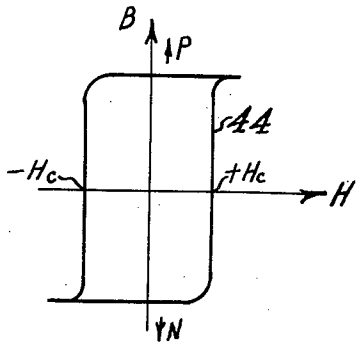


FIG. 2.

INVENTOR.
WITHROP S. PIKE
BY Morrish Rakan
ATTORNEY

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REVERSIBLE COUNTER

Winthrop S. Pike, Princeton, N.J., assignor to Radio Corporation of America, a corporation of Delaware

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This invention relates to counting circuits, and particularly to reversible counting circuits employing magnetic cores.

In the electrical art, counting circuits are used in adding and subtracting binary digits and in pulse checking circuits. Counting circuits are also used in frequency division where an unknown frequency is compared with a known frequency and an indication of the difference between the two frequencies is furnished by an output of the counter.

It is an object of the present invention to provide an improved reversible counter circuit employing magnetic cores.

Another object of this invention is to provide an improved counter circuit which can be reversed by changing the polarity of shift pulses.

Yet another object of the present invention is to provide an improved counter employing magnetic cores which can propagate information in a forward or reverse direction without undesired interaction between adjacent cores.

Still another object of the present invention is to provide an improved magnetic core ring counter which may propagate information in either direction around the ring.

According to the invention, a plurality of magnetic cores are connected in cascade by connecting adjacent cores through a transfer circuit. The transfer circuit includes a temporary storage means such as a capacitor connected between each two cores. An advance shift line connects a plurality of advance windings, one linking each of the cores, in series to a first biasing resistor. A reverse shift line connects a plurality of reversing windings, one linking each of the cores, in series to a second biasing resistor. The output of the last stage may be fed back through a transfer circuit to the input of the first stage to form a closed ring.

When positive pulses are applied to the advance shift line, information is propagated in a forward direction from a lower order core to a higher order core. When negative pulses are applied to the reverse shift line, information is propagated in the reverse direction from a higher order core to a lower order core. The same temporary storage capacitors are used in propagating the information in the forward and the reverse directions.

The invention will be more fully understood, both as to its organization and method of operation, from the following description when read in connection with the accompanying drawing, in which:

FIG. 1 is a schematic diagram of a reversible ring counter according to the invention, and

FIG. 2 is a graph, somewhat idealized, of the hysteresis loop for the magnetic material which is preferably used in constructing the magnetic cores of FIG. 1.

Referring to FIG. 1, a ring counter circuit **10**, illustratively, has three stages, 1M, 2M and 3M. Each of the stages includes a magnetic core **12**. Each core **12** is fabricated from a magnetic material having appreciable remanence. A suitable material is one exhibiting a substantially rectangular hysteresis characteristic. Each of the cores **12** is linked by an input winding **14**, an output winding **16**, an advance winding **18** and a reverse winding **20**. Each winding has its terminals indicated as marked and unmarked, respectively, in accordance with

the usual transformer convention, as explained more fully hereinafter.

An advance shift line **22** connects each advance winding **18** of the cores **12** in series, marked terminals to unmarked terminals. One terminal of the shift line **22**, at the marked terminal of the last winding **18** thereof, is connected through a first biasing resistor **24** to a common bias indicated in the drawing by the conventional ground symbol. The other terminal of the shift line **22**, at the unmarked terminal of the first winding **18**, is connected to an advance pulse source **26**.

Each of the reversing windings **20** of the cores **12** is connected in series, unmarked terminals to marked terminals, by a reverse shift line **28**. One terminal of the shift line, at the unmarked terminal of the last winding **20** thereof, is connected through a second biasing resistor **30** to ground. The other terminal of the shift line **28**, at the marked terminal of the first winding thereof, is connected to a reverse pulse source **32**. Each of the pulse sources herein may be known constant current sources such as pentode type vacuum tubes or other magnetic core circuits.

Similar transfer circuits **33** respectively connect each two adjacent cores **12**. A transfer circuit **33** includes a first unilateral conducting device, such as a diode rectifier **34**, a second unilateral device, such as a diode rectifier **36**, and a temporary storage means, such as a capacitor **38**. The anode of the first diode **34** is connected to the unmarked terminal of an output winding **16** of one stage and the cathode of the second diode **36** is connected to the marked terminal of the input winding **14** of the next higher order stage. These two diodes are series connected, the cathode of the diode **34** being connected to the anode of the diode **36**. The capacitor **38** is connected in shunt between the junction point **37** between the diodes **34** and **36** and ground.

The marked terminals of all the output windings **16** are connected together to the reverse shift line **28** at the junction between the shift line **28** and the resistor **30**. The unmarked terminals of all the input windings **14** are connected together to the advance shift line **22** at the junction between the shift line **22** and the resistor **24**.

The core **12** of the first stage **1M** also may be linked by a signal input winding **40**, for reasons described hereinafter, connected to a signal input pulse source **42**.

The magnetic cores **12** used in practicing the invention may be toroidal in shape. A hysteresis loop **44**, somewhat idealized, for a core **12** is shown in FIG. 2. Certain materials such as molybdenum-permalloy and manganese-magnesium ferrite exhibit a substantially rectangular hysteresis loop. Each core has a remanent condition of magnetic induction (B) in which the core exhibits substantial flux saturation. One remanent condition corresponds to a flux substantially oriented in one direction and the other condition corresponds to flux oriented in the opposite direction. In a toroidal core, for example, these directions may be taken along the center circular line of the figure of revolution. The one direction of magnetization is arbitrarily designated herein the "P" direction and the other direction of magnetization is designated the "N" direction.

Substantially no flux change is produced when a core is driven further into saturation along a horizontal portion of the hysteresis loop. A magnetizing force in one direction greater than a coercive force $+Hc$ is required to change the magnetization of the core from the N direction to the P direction. Similiarly, a magnetizing force in the other direction, greater than a coercive force $-Hc$ is required to change a core back to the N direction.

The relative sense of linkage of a winding to a core is indicated in FIG. 1 by a dot adjacent one of its ter-

minals (the so-called marked terminal) in accordance with the usual transformer convention, as mentioned above. A positive (conventional) current flowing into a dot marked terminal produces, or tends to produce, flux in one direction, taken herein as the P direction in the linked core. A change of flux in the core from the P direction to the other direction taken herein as the N direction induces a voltage in each winding coupled thereto, the polarity of which is such that its marked terminal is negative relative to its unmarked terminal. The polarity of the induced voltage is reversed for a flux change from the N direction to the P direction.

In operation, assume that initially the core **12** of the stage **1M** is magnetized in the P direction and the remaining cores are magnetized in the N direction. The initial condition of the counter may correspond to a reset condition. The reset condition can be achieved by applying a pulse to a reset winding (not shown) which links the core **12** of the stage **1M** in one sense and the core **12** of the remaining stages in the sense opposite the one sense. The polarity of the reset pulse is in a direction to drive the stage **1M** core **12** to the P direction of magnetization, and the remaining cores to the N-direction of magnetization. The duration of the reset pulse is made longer than the durations of any transient voltages produced by changes of flux in the respective cores **12**.

A first, positive advance pulse **48** applied to the advance shift line **22** from the source **26** flows into the unmarked terminal of each advance winding **18** and through the first biasing resistor **24** to ground. The magnetizing force generated in the cores by the advance pulse **48** drives the stage **1M** core **12** from the P to the N direction of magnetization; and drives each of the remaining cores **12** further into saturation in the N direction. The voltage induced in the output winding **16** of the first core **12** makes its marked terminal negative relative to its unmarked terminal. Thus, a current flows in the first transfer circuit **33** charging the capacitor **38** between stages **1M** and **2M**. The charging circuit for this capacitor **38** includes the second biasing resistor **30**, the output winding **16** of the first core **12**, the first diode **34** and the capacitor **38** of the first transfer circuit **33**. The voltage produced across the first biasing resistor **24** blocks each second diode **36** from passing a current while the advance pulse **48** is present. Upon the termination of the advance pulse **48** the capacitor **38** discharges through the series circuit including the second diode **36** of the first transfer circuit **33**, the input winding **14** of the second core **12** and the first biasing resistor **24**.

A signal represented by the P direction of magnetization of the stage **1M** core **12** is thus transferred from the first stage **1M** to the second stage **2M**. The voltage induced in the input winding **14** of the stage **1M** core **12** is prevented from causing a current flow by the second diode **36** of the third transfer circuit **33** being biased to cut-off. The reverse pulse source **32** and the signal input pulse source **42** can be assumed to be open while an advance pulse **48** is applied. Accordingly, no current flow is produced either in the reverse shift line **28** or through the signal input pulse source **42** during the application of an advance pulse **48**.

The next positive advance pulse **48** transfers the stored signal from the second stage **2M** to the third stage **3M** in a similar manner; and a third positive advance pulse transfers the signal from the third stage **3M** back to the first stage **1M**. The bias voltage across the first biasing resistor **24** prevents the signal from being transferred in the reverse direction by biasing each second diode **36** to cut-off.

The ring counter may be open-ended, if desired, by eliminating the transfer circuit **33** connecting the third stage **3M** and the first stage **1M**. This open-ended counter is useful in situations where it is desired to begin a count commencing with the occurrence of a specified event. In the absence of the event, all the cores are magnetized in the N direction and the advance pulses do not produce an output signal in any of the stages. Upon the occurrence of the event, an input pulse **46** is applied as by the signal input pulse source **42** and the signal input winding **40** to change the direction of magnetization of the stage **1M** core **12** to the P direction. Each subsequent advance pulse **48** then transfers a signal to a higher order stage and after a desired number of advance pulses, determined by the number of stages employed, an output signal is obtained.

When it is desired to shift the stored signal in a reverse direction, a negative reverse pulse **50** is applied to the reverse shift line **28**. For example, assume that the core **12** of the second stage **2M** is magnetized in the P direction and the remaining cores are magnetized in the N direction. When a reverse pulse **50** is applied to the shift line **28** by the reverse pulse source **32**, the stage **2M** core **12** is driven from the P to the N direction of magnetization. Each of the remaining cores is driven further into saturation in the N direction. The reverse pulse **50** produces a voltage drop across the second biasing resistor **30** which biases each first diode **34** to cut-off while the reverse pulse **50** is present. The voltage induced in the input (now output) winding **14** of the stage **2M** core **12** makes its marked terminal more negative relative to its unmarked terminal. A current flow is produced in the first transfer circuit **33** including the first biasing resistor **24**, the capacitor **38**, the second diode **36** and the input (now output) winding **14** of the stage **2M** core **12**. Upon the termination of the reverse pulse **50** the capacitor **38** is discharged through the series circuit including the first diode **34** of the first transfer circuit **33**, the output (now input) winding **16** of the stage **1M** core **12** and the second biasing resistor **30**. This current flow is into the marked terminal of the output (now input) winding **16** of the stage **1M** core **12**. Accordingly, the first core **12** is driven from the N to the P direction of magnetization. The voltage induced in the output (now input) winding **16** of the stage **2M** core **12** is blocked by the first diode **34** of the second transfer circuit **33** from changing the direction of magnetization of the stage **3M** core **12**. Thus, the signal is prevented from being propagated in the forward direction by the voltage drop across the second biasing resistor **30** which biases each first diode **34** to cut-off during the presence of a reverse pulse **50**. A second reverse pulse **50** transfers the information from the stage **1M** core **12** to the stage **3M** core **12** through the third transfer circuit **33** in a similar manner.

There has been described herein a relatively inexpensive and simply constructed counter circuit employing magnetic cores. Information can be propagated selectively in either a forward or a reverse direction depending upon the polarity of shift pulses applied to windings in the respective cores. Undesired interaction is prevented by utilizing the shifting pulses for biasing to cut-off one or the other of two diodes in each transfer circuit.

I claim:

1. A ring counter circuit comprising at least two magnetic cores, each of said cores having two directions of remanent magnetization, input, output, advance and reverse windings linked to each of said cores, a transfer circuit connecting one terminal of the output winding of one core to one terminal of the input winding of another of said cores, a first bias means, means connecting the other terminals of said input windings to said first bias means, a second bias means, means connecting the other terminals of said output windings to said second bias means, means connecting said advance windings in series to said first bias means, and means connecting said reverse windings in series to said second bias means.

2. A counter circuit comprising at least two magnetic cores each having two directions of remanent magnetization, input, output and shift windings linked to each of said cores, a transfer circuit connecting one terminal of the output winding of one of said cores to one terminal of the input winding of another of said cores, a first and

second bias means, a first and second unilateral conducting means, means connecting said shift windings in series to said first and second unilateral conducting means, means connecting said first unilateral conducting means in one sense to said first bias means, means connecting said second unilateral conducting means in the sense opposite the one sense to said second bias means, and means for applying shift pulses selectively to said shift windings.

3. A ring counter comprising a plurality of magnetic cores of substantially rectangular hystersis loop material for storing information in accordance with the one or the other directions of magnetization of said cores, input and output windings linked to each of said cores, transfer circuits connecting said cores in cascade by connecting the output winding of a lower order core to the input winding of a higher order core in a shifting sequence and including a transfer circuit connecting the output winding of the highest order core to the input winding of the lowest order core to form a closed ring, a different pair of unidirectional conducting means connected in series with each other and poled in the same direction in each transfer circuit for preventing undesired current flow in said circuits, first and second means each for applying a magnetizing force to each of said cores in a direction to change its magnetization from the one direction to the other direction, separate means connected to said magnetizing force applying means for applying a cut-off bias selectively either to the one or the other of said pair of unidirectional conducting means in each transfer circuit for shifting stored information correspondingly in either the forward or the reverse direction according to which one of said first and second means applies said magnetizing force.

4. A magnetic system comprising a plurality of magnetic cores of substantially rectangular hystersis loop material for storing information in accordance with the one or the other directions of magnetization of said cores, input and output windings linked to each of said cores, transfer circuits connecting said cores in cascade by connecting the output windings of one core to the input winding of a succeeding core in a shifting sequence, a different pair of unidirectional conducting means connected in series with each other and poled in the same direction in each transfer circuit for preventing undesired current flow in said circuits, first and second means each for selectively applying a magnetizing force to each of said cores in a direction to change its magnetization from the one direction to the other direction, and separate means each connected to a different one of said magnetizing force applying means for applying a cut-off bias selectively either to the one or the other of said pair of unidirectional conducting means in each transfer circuit for shifting stored information correspondingly in either the forward or the reverse direction.

5. A magnetic system comprising a plurality of magnetic cores of substantially rectangular hystersis loop material for storing information in accordance with one or the other directions of magnetization of said cores, input, output and a pair of shift windings linked to each core, transfer circuits connecting said cores in cascade by connecting the output winding of one core to the input winding of a succeeding core in a shifting sequence, a different pair of unidirectional conducting means connected in each transfer circuit for preventing undesired current flow in said circuits, means for applying an electrical signal selectively to either the one or the other of said pair of shift windings on each of said cores, said signal being effective to change the magnetization of a core from the one direction to the other direction, and means for applying a cut-off bias selectively either to the one or the other of said pair of unidirectional conducting means in each transfer circuit for shifting stored information correspondingly in either the forward or the reverse direction.

6. A magnetic system comprising: a plurality of magnetic cores of substantially rectangular hysteresis loop material; input, output and first and second other windings linked to each core; transfer circuits connecting said cores in cascade by connecting the output winding of one core to the input winding of a succeeding core; a different pair of unidirectional conducting means connected in each transfer circuit for preventing undesired current flow in said circuits; means for selectively applying a first electrical signal to all of said first other windings; means for applying a second electrical signal selectively to all of said second other windings; and means for applying a cut-off bias selectively to at least one unidirectional conducting means of each said pair when one of the first and second electrical signals is applied.

7. A magnetic system comprising: at least two magnetic cores each having two directions of remanent magnetization; input, output and first and second other windings linked to each of said cores; a transfer circuit connecting one terminal of the output winding of one core to one terminal of the input winding of another of said cores; first means for selectively applying an electrical signal to all of said first other windings; second means for selectively applying an electrical signal to all of said second other windings; and means for applying a bias selectively to the other terminal of each of said input windings.

8. A magnetic system comprising: a plurality of magnetic cores of substantially rectangular hysteresis loop material for storing information in accordance with the one or the other directions of magnetization of said cores; input, output and first and second other windings linked to each core; a plurality of nonmagnetic storage elements each connected effectively in parallel with the output winding of a different core; first signal means for selectively applying an electrical signal to all of said first other windings, said signal being effective to change the magnetization of a core from the one direction to the other direction; second signal means for selectively applying an electrical signal to all of said second other windings; a plurality of first unidirectional conducting devices each connected between one terminal of a different one of said storage elements and said second signal means via at least one of said second other windings; a plurality of second unidirectional conducting devices each connected between the said one terminal of a different storage element and a different one of said input windings; and means for selectively applying a cut-off bias to all of said second unidirectional conducting devices.

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