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(54) Title: ORGANIC LIGHT EMITTING DIODE DISPLAYS

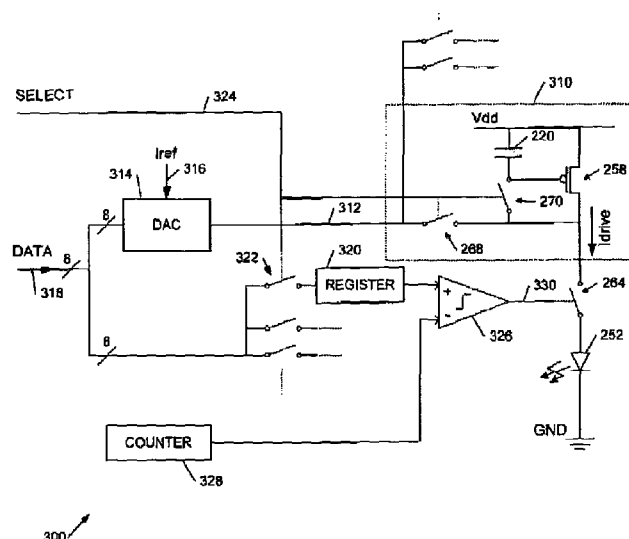


Figure 3

(57) Abstract: An organic light emitting diode (OLED) display, the display comprising: a substrate bearing a plurality of OLED pixels, each said pixel having associated control circuitry, wherein said control circuitry includes at least one memory element for storing a value to determine a luminance of an associated OLED pixel, and wherein said control circuitry has a pixel data input to receive and store, using said memory element, luminance data determining said luminance of said associated OLED pixel; wherein said control circuitry is configured to control both a current through a said OLED pixel and a duration for which said current flows through said pixel; and wherein the same luminance data controls both said current and said duration such that said luminance of the associated said OLED pixel has a non-linear response to said luminance data.



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ORGANIC LIGHT EMITTING DIODE DISPLAYS

FIELD OF THE INVENTION

- 5 This invention relates to improved drive techniques for organic light emitting diode (OLED) displays.

BACKGROUND TO THE INVENTION

- 10 Recent years have seen very substantial growth in the market for displays as the quality of displays improves, their cost falls, and the range of applications for displays increases. This includes both large area displays such as for TVs or computer monitors and smaller displays for portable devices.

- 15 The most common classes of display presently on the market are liquid crystal displays and plasma displays although displays based on organic light-emitting diodes (OLEDs) are now increasingly attracting attention due to their many advantages including low power consumption, light weight, wide viewing angle, excellent contrast and potential for flexible displays.

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- The basic structure of an OLED is a light emissive organic layer, for instance a film of a poly (p-phenylenevinylene) ("PPV") or polyfluorene, sandwiched between a cathode for injecting negative charge carriers (electrons) and an anode for injecting positive charge carriers (holes) into the organic layer. The electrons and holes combine in the organic layer generating photons. In WO90/13148 the organic light-emissive material is a conjugated polymer. In US 4,539,507 the light-emissive material is of the class known as small molecule materials, such as (8-hydroxyquinoline) aluminium (Alq₃). In a practical device one of the electrodes is transparent, to allow the photons to escape the device.

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- A typical organic light-emissive device ("OLED") is fabricated on a glass or plastic substrate coated with a transparent anode such as indium-tin-oxide ("ITO"). A layer of a thin film of at least one electroluminescent organic material covers the first electrode. Finally, a cathode covers the layer of electroluminescent organic material. The cathode is typically a metal or alloy and may comprise a single layer, such as aluminium, or a
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plurality of layers such as calcium and aluminium. In operation, holes are injected into the device through the anode and electrons are injected into the device through the cathode. The holes and electrons combine in the organic electroluminescent layer to form an exciton which then undergoes radiative decay to give light. The device may be
5 pixellated with red, green and blue electroluminescent subpixels in order to provide a full colour display. For the avoidance of doubt, "pixel" as used herein may refer to a pixel that emits only a single colour or a pixel comprising a plurality of individually addressable subpixels that together enable the pixel to emit a range of colours.

10 One way of addressing OLED displays is by use of an "active matrix" arrangement in which individual pixel elements of a display are activated by an associated thin-film transistor. In one drive technique an analogue current signal is employed to program the drive current of an active matrix OLED pixel so that the current through the pixel, and hence the luminance, is proportional to the programmed level. Another way of
15 addressing OLED displays is using a so-called passive matrix display in which there is no active thin film transistor (TFT) associated with each individual pixel. A passive matrix OLED display may be driven with a time dependent signal, for example a pulse width modulated (PWM), signal on a row or column of the display to vary the brightness of a pixel. What might be termed hybrid OLED display drive techniques have also been
20 described in, for example, US6,157,356 and KR2007/0115467A. The '467A document describes a combination of pulse amplitude modulation (PAM) and pulse width modulation (PWM), in which 6 bit digital image data is split into two portions, the upper 3 bits being employed for PWM driving and the lower 3 bits for PAM driving. However there remain significant issues to be addressed, in particular when driving large area
25 flat panel OLED displays, as explained further below.

Two major problems with OLED pixel driving for TV and related applications are dynamic range and matching at low grey levels.

The required light output from a display pixel does not depend linearly with the grey-scale signal, rather there is a gamma function which relates the grey-scale to the
30 required luminance. For the ITU Rec709 standard, used for HDTV (High Definition Television), that gamma function results in a dynamic range of 1000:1 between the maximum grey-level and the minimum non-zero grey-level where the grey-level is specified by an 8-bit value. For the sRGB standard, used for data output typically from

computer systems, an 8-bit grey-scale results in a ~200,000:1 dynamic range requirement.

5 The first problem this generates is just being able to produce an output stage capable of controlling a current over such a large range, the second is to produce the current reproducibly between different pixel drive circuits. This second problem in particular becomes extremely difficult if not impossible for the sRGB standard.

10 The problem is different depending on drive methods. For a so-called 'analogue' output, where the current level is changed in order to control the current out of the OLED, the problem is most severe as it is very hard to produce a well-matched output both at the full scale current (e.g. 3 μ A) and the minimum grey-level (3nA for Rec709, 15pA for sRGB) and would typically result in very large transistors, or possibly multiple transistors for different ranges of output (where monotonicity becomes a problem). For a digital drive method, where a fixed current reference is modulated with a set duty-cycle, the problem is one of required timing cycles (e.g. a clock rate requirement from 15 0.12MHz to 24MHz), and digital storage at the pixel. This method also ages the OLED more rapidly as it is always driven at the full scale current.

SUMMARY OF THE INVENTION

20 According to a first aspect of the invention there is therefore provided an organic light emitting diode (OLED) display, the display comprising: a substrate bearing a plurality of OLED pixels, each said pixel having associated control circuitry, wherein said control circuitry includes at least one memory element for storing a value to determine a luminance of an associated OLED pixel, and wherein said control circuitry has a pixel data input to receive and store, using said memory element, luminance data 25 determining said luminance of said associated OLED pixel; wherein said control circuitry is configured to control both a current through a said OLED pixel and a duration for which said current flows through said pixel; and wherein the same luminance data controls both said current and said duration such that said luminance of the associated said OLED pixel has a non-linear response to said luminance data. 30

Broadly speaking, in embodiments of the above described display the dynamic range requirements are reduced to the square root of what they were previously, by having both the drive level and the time for which an OLED is driven approximately

proportional to the luminance data signal: Because in embodiments, both drive current and time are substantially linearly dependent on/proportional to the luminance data signal, the luminance varies with the square of the data signal. This facilitates providing a large dynamic range, and also matching between pixel luminances at low grey-scale levels. In effect, compression of the drive signal reduces the dynamic range requirements of the data signal (the skilled person will appreciate that although references being made to grey-scale values, the same concepts apply to red, green and blue values of a colour display).

10 In embodiments of the display the luminance data signal comprises a digital signal with a plurality of data bits and one or more or all of these data bits control both the current and the duration of an OLED pixel drive. Although some preferred embodiments employ digital control techniques, alternatively the luminance data signal may comprise an analogue data signal, this analogue data (for example a voltage or current) setting
15 both a current drive to an OLED pixel and a time for which the pixel is illuminated, for example by comparison with a sawtooth wave form.

In preferred implementations the control circuitry comprises first and second programmable circuitry to program the current, and illumination duration respectively
20 for an OLED pixel of the display. More particularly in embodiments the current programming circuitry comprises a pixel drive thin film transistor (TFT) coupled to a storage capacitor, in particular to store a gate voltage for the TFT to set a drive level for the pixel. The skilled person will appreciate that depending upon whether the current is current-programmed or voltage-programmed there may be one or more switches
25 coupled to the TFT/storage capacitor to enable a desired pixel luminance level to be set by storing a voltage on the capacitor. In embodiments the current programming circuitry includes an analogue-to-digital converter to convert digital luminance data to an analogue output, and a multiplexer to selectively connect this analogue output to program the current drive level of a selected pixel.

30 In some preferred embodiments the duration programming circuitry comprises a digital register or timer which may be programmed with a timing value to define the illumination duration of a corresponding OLED pixel. Where a register is employed, a value stored by the register may be compared against an incrementing (or
35 decrementing) value from a counter in order to control a switch to switch off (or on) a current drive to the corresponding OLED pixel. In embodiments a dress circuitry, for

example a plurality of switches, is provided to allow a selected register to be programmed with a pixel duration value; in embodiments the counter may be shared between a plurality (or all) of the pixels. In other arrangements an analogue or digital timer is employed to provide a pulse of programmable duration to control current to a corresponding OLED pixel. The timer may comprise, for example, a monostable circuit, and may be implemented using either analogue or digital techniques, or both.

In some preferred implementations the control circuitry is duplicated amongst groups of pixels of the OLED display. Thus in embodiments control circuitry may be shared amongst a group of pixels within a physical boundary more particularly sharing common portions of the control circuitry such as a digital-to-analogue converter and/or counter, whilst providing separate current/duration storage elements for each pixel of the group. In embodiments some or all of the control circuitry is provided on "chipslets" mounted on the display substrate - for example a chiplet may comprise an integrated circuit carrying both the shared portion and the pixel-specific portions of the control circuitry for a group of pixels, and may have a shared input luminance data connection for programming the pixels, and separate connections to each of the pixels for controlling the individual pixels in accordance with the programmed data. Thus in embodiments the display comprises a plurality of chipslets each associated with a group of two or more pixels of the display, to provide the control circuitry for the associated pixels, the chipslets being distributed over the display substrate and having one or more common serial or parallel input data connections.

In embodiments because the luminance of a pixel is substantially proportional to the luminance signal data squared, the response of a pixel already approximates that desired, for example, for compliance with ITU (International Telecommunications Union) Recommendation 709 (which standardises the format of high definition television (HDTV)), or for the standard sRGB colour space. However in some implementations this approximation may be made more accurate, for example by modifying the response of the digital-to-analogue (DAC) converter and/or by including circuitry between the analogue output of the DAC and a current programming line of the control circuitry. In the case of Rec. 709, the accuracy of the conformance of the non-linear response to the standard may be improved by employing different responses for the current and duration luminance factors, for example providing a substantially linear duration response to the luminous data, but a non-linear current drive level response to the luminance data. In the latter case the current drive response

to the luminance data may, for example, be substantially constant or linearly increasing at low luminance values and increasing according to a power law of greater than unity (for example approximately 1.4) at higher luminance values.

5 In a related aspect the invention provides a method of driving pixels of an organic light-emitting diode (OLED) display, the display comprising: a substrate bearing a plurality of OLED pixels, each said pixel having associated control circuitry, wherein said control circuitry includes at least one memory element for storing a value to determine a luminance of an associated OLED pixel, and wherein said control circuitry has a pixel
10 data input to receive and store, using said memory element, luminance data determining said luminance of said associated OLED pixel; the method comprising using the same luminance data to control both a current through a said OLED pixel and a duration for which said current flows through said pixel such that said luminance of the associated said OLED pixel has a non-linear response to said luminance data.

15 The invention further provides a method of driving pixels of an organic light-emitting diode (OLED) display to provide increased dynamic range, wherein the method comprises: writing data to a pixel drive circuit of said OLED display; providing a drive signal from said pixel drive circuit to a said OLED pixel, wherein said drive signal has a
20 drive level and a drive duration; and controlling both said drive level and said drive duration responsive to the same data said that a luminance of said pixel exhibits a non-linear response to said data.

In preferred embodiments when averaged over a range of the input data values, for
25 example the entire input data range, the luminance varies as a value of the data raised to a power, wherein the power is equal to or greater than 2, for example 2.2 or 2.4.

In a related aspect the invention provides an OLED display having a plurality of pixels, the display comprising: means for writing data to a pixel drive circuit of said OLED
30 display; means for providing a drive signal from said pixel drive circuit to a said OLED pixel, wherein said drive signal has a drive level and a drive duration; and means for controlling both said drive level and said drive duration responsive to the same data said that a luminance of said pixel exhibits a non-linear response to said data.

35 As previously mentioned, in some preferred implementations chiplets (small integrated circuits) are distributed over the display substrate to provide control circuitry for groups

of OLED pixels. This facilitates control of both pixel drive level and pixel drive duration for individual pixels of the display (here "pixels" includes sub-pixels of a colour display).

5 Thus in a further aspect the invention provides an OLED display, the display comprising: a display substrate bearing a plurality of OLED light emitting pixels: a plurality of chiplets mounted on said substrate, wherein each said chiplet is mounted adjacent a group of said pixels and comprises a chiplet substrate bearing control circuitry for said group of pixels; and wherein said control circuitry on a said chiplet comprises first programmable circuitry to program a drive level for each pixel of said group of said pixels and second programmable circuitry to program a drive duration for each pixel of said group of pixels.

15 In embodiments the first programmable circuitry comprises a storage capacitor and thin film transistor as previously mentioned, and the second programmable circuitry a digital register and/or timer, again as previously described. In embodiments the first and second programmable circuitry share a common data input line; more particularly one or more of the same bits of a digital data line controls/programmes both the drive level and drive duration for each pixel. In this way the luminance of a pixel of the display is dependent on a power of the input, programming data value, where the power is equal to or greater than 2. In embodiments a response characteristic of one or both of the drive level and drive duration programming circuitry comprises a piecewise response having a first characteristic over a first range of input data values, and a second different characteristic over a second, higher range of input data values. Thus, for example, at low input data values the characteristic may be substantially constant or linear, and at higher values a response may exhibit a power law of approximately 1.2 or 1.4.

20 Embodiments of the above described OLED displays may also include a controller to select one or more of the chiplets and to program the selected chiplet(s) with luminance data by programming the first and second programmable circuitry to co-define pixel drive levels and durations.

5 BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will now be further described by way of example only, with reference to the accompanying Figures in which:

10 Figures 1a and 1b show, respectively, a luminance-grey-scale transfer curve for Rec. 709/sRGB, and an illustration of a portion of an OLED display including a chiplet integrated circuit;

15 Figures 2a to 2c show examples of OLED pixel drive circuits, respectively, setting a gate voltage on the drive transistor, using a current mirror, and employing a current copy technique;

Figure 3 shows control circuitry for controlling luminance of one or more OLED pixels according to an embodiment of the invention;

20 Figures 4a and 4b show portions of an OLED display incorporating chiplets bearing pixel drive circuits according to embodiments of the invention, showing, respectively, first and second example implementations;

25 Figure 5 shows a combination of an OLED display according to an embodiment of the invention and a controller for the display; and

Figure 6 shows an example of an analogue pixel drive circuit according to an embodiment of the invention.

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DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Broadly speaking we will describe how to reduce the dynamic range requirements of OLED pixel drive circuits, in embodiments by mixing analogue and digital drive methodologies. More particularly we will describe techniques in which (all) the digital luminance data goes both to an analogue pixel drive level control circuit, and to a digital drive duration control circuit. By employing a technique in which the pixel drive signal comprises a combination of a time division component and an analogue current component both proportional to the (luminance) drive signal the dynamic range requirement for a pixel may be drastically reduced, for example to of order 30:1 for Rec. 709 and of order 450:1 for sRGB. With such techniques the OLED pixels are not aged unduly and the digital storage requirements are small as compared with, for example, the approximately 19 bits per pixel which would be needed for a 200,000:1 dynamic range. We will also describe how additional non-linearity may be introduced to reduce the storage requirements still further.

Transfer curves

Figure 1a shows a generalised transfer curve relating an input grey-scale data value to a desired pixel luminance. In the example an 8 bit grey-scale value (up to 255) is assumed, but it will be appreciated that this is by way of example only. The non-linearity of the curve is expressed (approximately) by a gamma value, where luminance is proportional to the grey-scale value raised to the power gamma. For example for sRGB gamma is approximately 2.4.

For the Rec. 709 standard the transfer curve comprises a linear portion at grey-scale values near zero and a power law portion with a gamma of 2.4 at higher grey-scale values. The effect of this is that the Rec. 709 standard curve 10a differs from the sRGB curve 10b at low grey-scale values, as illustrated, thus reducing the required dynamic range for HDTV.

We will describe later how embodiments of the invention facilitate obtaining a transfer curve of the type shown in Figure 1a.

Chiplets

In some preferred implementations of the embodiments of the invention use chiplets for the pixel drive circuitry. In broad terms these comprise small silicon integrated circuits which are stuck onto the glass substrate of a display and connected to OLED pixels and to external connections of the display. To aid in understanding embodiments of the invention we will now briefly describe details of such chiplets.

Figure 1b which is taken from WO 2010/019185 shows a layout view of a group of four pixels (20a, 20b, 20c and 20d) elements of an OLED display device. Each of the four pixels can be arranged to emit a different colour, such as red, green, blue and white (RGBW). Figure 1b represents a portion of a full display where the full display would be constructed of an array of such groups of pixels arranged in many rows and columns. For example, a modern television would be constructed having 1920 rows and 1080 columns of such groups of pixels.

A chiplet 120 is arranged to control the electrical current to pixels 20a, 20b, 20c and 20d. A chiplet is a separately fabricated integrated circuit which is mounted and embedded into the display device. Much like a conventional microchip (or chip) a chiplet is fabricated from a substrate and contains integrated transistors as well as insulator layers and conductor layers which are deposited and then patterned using photolithographic methods in a semiconductor fabrication facility. These transistors in the chiplet are arranged in a transistor drive circuit to drive the electrical current to pixels of the display. A chiplet is smaller than a traditional microchip and unlike traditional microchips, electrical connections need not be made to a chiplet by wire bonding or flip-chip bonding. Instead, after mounting each chiplet onto the display substrate, deposition and photolithographic patterning of conductive layers and insulator layers continues. Therefore, the connections can be made small, for example through using vias 2 to 15 micrometers in size. The chiplet and connections to the chiplet are small enough to be placed within the area of one or more pixels which, depending on the display size and resolution, may range from approximately 50 micrometers to 500 micrometers in size. Additional details about the chiplet and its fabrication and mounting processes can be found in WO '185.

Each pixel is provided with a lower electrode, such as a lower electrode 161a in pixel 20a. The emitting area of pixel 20a is defined by an opening 163a in an insulator

formed over the lower electrode. The device includes multiple conductive elements formed in a first conductive layer which are arranged to facilitate providing electrical signals to the chiplet's transistor drive circuitry to enable the chiplet to control electrical current to the pixels. Chiplet 120 controls current to pixel 20a through a conductor 133a. For example, conductor 133a is connected to chiplet 120 through a via 143a and is also connected to lower electrode 161a through a via 153a. The device also includes a series of signal lines including, power lines, data lines, and select lines which are formed in the first conductive layer and transmit electrical signals from the edge of the display to the chiplets. Power lines are signal lines that provide a source of electrical current to operate the organic electroluminescent elements. Data lines are signal lines which transmit bright information to regulate the brightness of each pixel. Select lines are lines which selectively determine which rows of the display are to receive brightness information from the data lines. As such select lines and data lines are routed in an orthogonal manner.

Power is provided to the chiplet 120 by way of a power line 131. Two vias are provided for connection between the power line and the chiplet 120. A data line 135 is provided in the column direction for communicating a data signal containing brightness information to chiplet 120 for pixel 20a and pixel 20b. Similarly, a data line 136 is provided in the column direction for communicating a data signal containing brightness information to chiplet 120 for pixel 20b and pixel 20d. In an alternate arrangement the data lines 135 and 136 and the power line 131 can be connected to the chiplet 120 by only a single via for each line. A select line segment 137a is provided in the row direction for communicating a row select signal to chiplet 120 for pixel 20a and pixel 20b. The row select signal is used to indicate a particular row of pixels and is synchronized with the data signal for providing brightness information. Thus the row select signal and the data signals are provided in orthogonal directions. Chiplet 120 communicates the row select signal from select line segment 137a to a select line segment 137b by way of an internal pass-thru connection on the integrated circuit. Select line segment 137b then communicates the row select signal to subsequent chiplets arranged in the same row. Similarly a select line segment 138a is provided in the row direction for communicating a row select signal to chiplet 120 for pixel 20c and pixel 20d. Chiplet 120 communicates the row select signal from select line segment 138a to a select line segment 138b by way of another internal pass-thru connection on the integrated circuit. Select line segments 137a and 137b together serve to form a single select line, which is discontinuous. Connections between the select line

segments are provided by the pass-thru connections in the chiplet. While only two segments are shown, the select line can contain a series of many such segments. Select line segments 138a and 138b similarly together serve to form a single discontinuous select line. All of the select lines segments and data lines may be formed from a single metal layer. Communication across the orthogonal array is then achieved by routing either the row select signal, the data signal, or both through the pass-thru connections on the chiplet.

Active matrix pixel circuits

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It is also helpful to facilitate understanding of the operation of embodiments of the invention to describe examples of different types of analogue pixel drive circuits which may be employed in embodiments of the invention. Later we will describe a mixed analogue/digital drive circuit in which both the pixel drive level and pixel drive time are substantially proportional to a luminance data signal, and an embodiment of this circuit will be described using a current copy-type analogue pixel drive circuit. However other types of analogue pixel drive circuit which provide a variable pixel drive level to an OLED pixel may alternatively be employed including, but not limited to, those now described.

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Figure 2a shows an example of a voltage programmed OLED active matrix pixel circuit 250. A circuit 250 is provided for each pixel of the display and Vdd 252, Ground 254, row select 224 and column data 226 busbars are provided interconnecting the pixels. Thus each pixel has a power and ground connection and each row of pixels has a common row select line 224 and each column of pixels has a common data line 226.

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Each pixel has an OLED 252 connected in series with a driver transistor 258 between ground and power lines 252 and 254. A gate connection 259 of driver transistor 258 is coupled to a storage capacitor 220 and a control transistor 222 couples gate 259 to column data line 226 under control of row select line 224. Transistor 222 is a thin film field effect transistor (TFT) switch which connects column data line 226 to gate 259 and capacitor 220 when row select line 224 is activated. Thus when switch 222 is on a voltage on column data line 226 can be stored on a capacitor 220. This voltage is retained on the capacitor for at least the frame refresh period because of the relatively high impedances of the gate connection to driver transistor 258 and of switch transistor 222 in its "off" state. Driver transistor 258 is typically a TFT and passes a (drain-

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source) current which is dependent upon the transistor's gate voltage less a threshold voltage. Thus the voltage at gate node 259 controls or programs the current through OLED 252 and hence the brightness of the OLED.

5 In the voltage-programmed circuit of Figure 2a the OLED emission depends non-linearly on the applied voltage. The light output from an OLED is proportional to the current it passes, and Figure 2b (in which like elements to those of Figure 2a are indicated by like reference numerals) illustrates a pixel driver circuit which employs current control. More particularly a current on the (column) data line, set by current
10 generator 266, programs the current through thin film transistor (TFT) 260, which in turn sets the current through OLED 252, since when transistor 222a is on (matched) transistors 260 and 258 form a current mirror.

Figure 2c (which is taken from our earlier patent application WO03/038790) shows a
15 further example of a current-programmed pixel driver circuit. In this circuit the current through an OLED 252 is programmed by setting a drain source current for OLED driver transistor 258 using current generator 266, for example a reference current sink, and copying/memorising the driver transistor gate voltage required for this drain-source current. Thus the brightness of OLED 252 is determined by the current, I_{col} , flowing
20 into reference current sink 266, which may be adjustable and set as desired for the pixel being addressed. A switching transistor 264 is connected between drive transistor 258 and OLED 252 to inhibit OLED illumination during the programming phase. In general one current sink 266 is provided for each column data line. To copy the programming current, switch transistor 268 is "closed" and switch transistor 264 is
25 "opened" so that the programming current flows through drive transistor 258, and switch transistor 270 is also closed to set V_g on drive transistor 270 for the programmed current and to store this V_g value on capacitor 220.

Combined analogue and digital drive circuits

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We will now describe an embodiment of a pixel drive circuit in which an input grey-scale value, GS, is converted to a data value, DATA, which is in turn converted to a luminance value, L. In embodiments

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$$L \propto (DATA)^2 \quad (1)$$

In embodiments this is achieved by making both the pixel on-time duration approximately proportional to DATA, and the pixel (current) drive level also approximately proportional to DATA. As previously described, a desired transfer curve
 5 has

$$L \propto (GS)^\gamma \quad (2)$$

where $\gamma = 2.4$ for sRGB and also for Rec. 709 (over the majority of the curve except for
 10 the near-black region - averaged over the entire transfer curve the γ of Rec. 709 is approximately 2.2). It can be appreciated that if

$$DATA \propto (GS)^{1.2} \quad (3)$$

15 then a gamma of approximately 2.4 will be achieved via equation (1), noting equation (2).

Referring now to Figure 3, this shows a pixel driver circuit 300 in which the luminance of the driven OLED is proportional to the square of the digital input data; the circuit is
 20 also modifiable to achieve a gamma of 2.4, 2.2 or a piecewise implementation of the Rec. 709 transfer curve. In Figure 3 similar elements to those previously described are indicated by like reference numerals (although the skilled person will appreciate that the functions do not precisely correspond).

25 Broadly speaking the circuit portion within dashed line 310 enables a current drive through the OLED 252 to be programmed (by setting a voltage on capacitor 220) by a current signal on line 312. This current signal is generated by a digital-to-analogue converter (DAC) 314 in proportion to a reference current import 316, dependent on an input data value on line 318. The same data, in the example comprising 8 bits, is also
 30 provided to a register 320 via a controllable switch 322. Switch 322 is controlled by a select line 324, which also controls switches 268, 270. When the pixel drive circuit 300 is programmed data on line 318 sets a current on line 312 which in turn sets a gate voltage for transistor 258 stored on capacitor 220, and this data is also written into register 320. Switch 264 is arranged to be open during programming of the current

drive for OLED 252. As illustrated line 318 comprises a parallel data bus, that a serial or quasi serial data connection may be alternatively employed.

Register 320 provides a data output to a comparator 326, which has a second input from a counter 328, and which provides an output 330 to control switch 264, and hence to switch the current drive to OLED 252 on and off. In operation the counter counts up until the value stored in register 320 is reached at which point the comparator 326 controls switch 264 from a closed position to an open position. In this way the duration of the current drive applied is proportional to the digital value stored in register 220, which is set by the data on line 318, and the level of the current drive to the OLED is also set by the data on line 320, via DAC 314.

Consider an example where the reference current $I_{ref} = 10 \mu A$ (the full scale current), and where the DATA on line 128 has a value of 127 out of a maximum of 255. Then the drive current is given by:

$$I_{drive} = \frac{127}{255} \times 10mA \quad (4)$$

The counter resets to zero and then counts up to 255 in equal time steps (it will be appreciated that the counter could alternatively count down). Assuming a frame time of 10 ms (a 100Hz display) then for a total of 256 steps the current drive, I_{drive} is applied to OLED 252 for a duration given by:

$$I_{duration} = \frac{127}{256} \times 10ms \quad (5)$$

Therefore the total charge, Q_{pixel} , through OLED pixel 252 is given by:

$$Q_{pixel} = \frac{127^2}{255 \times 256} \times 10mA \times 10ms \quad (6)$$

It can therefore be seen that the pixel luminance L is proportional to the square of the DATA on line 318.

The skilled person will appreciate that the output 312 of DAC 314 may comprise either a voltage or a current, depending upon whether the pixel drive circuit 310 is a voltage-programmed or current-programmed circuit. The pixel drive duration is in the circuit example of Figure 3 determined by a combination of a counter, register and digital comparator, but alternative arrangements may also be employed. For example the data on line at 318 may be employed to set the duration of a pulse from an analogue or digital monostable circuit, in which case in embodiments no register is required.

Some of the circuitry of Figure 3 is pixel-specific, in particular the analogue drive circuitry within dashed box 310 and portions of the digital drive circuit in particular register 320, comparator 326 and switch 264. However for efficiency other portions of the pixel drive circuitry drive 300 of Figure 3 may be shared between groups of pixels including, for example, DAC 314 and counter 328.

In embodiments the circuitry of Figure 3 may be implemented on a chiplet 400 as shown in Figure 4a, the chiplet having portions 402 of circuitry dedicated to each of a plurality of pixels driven by chiplet 400, and also including shared circuitry 404, as previously described. Figure 4a shows, schematically, a portion of an OLED display 450 in which the pixels (or sub-pixels) are arranged in groups of 4 each served by a respective chiplet 400. Figure 4b shows another example arrangement of an OLED display 450' in which each chiplet 400' drives 6 rather than 4 pixels, and in which a serial DATA connection 318' is employed, successive chiplets being daisy chained. In each case Vdd and ground connections are provided (typically the ground connection comprises a cathode plane) together with block/pixel select lines 324. In alternative arrangements a block/pixel select line may comprise a serial or parallel address bus.

Referring now to Figure 5, this shows a combination of an OLED display 450, 450' as described above with a controller 500 for driving the display. In the example shown the controller provides one or more DATA outputs 318/318' to the OLED display, and a control signal 502 to a shift register 504 which, in embodiments, circularly rotates a single bit to provide a block (or pixel) select control signal to the OLED display. An RGB (Red, green, blue) data input 506 may optionally be mapped to a desired transfer curve using a desired transfer curve using a grey-scale look-up table 508 for each colour component. Such an arrangement can be used to adjust the response of the display to provide an average gamma of 2.2 or 2.4 taking account of the inherent gamma of 2.0 provided by the operation of the circuit. In embodiments the input data

may be mapped to increase number of bits, for example from 8 bits to 9 bits, to facilitate achieving this.

5 In more detail, and referring again to Figure 3, in embodiments the time component of the luminance variation is always substantially linear, but the variation of analogue drive level, more particularly current drive with data value may be non-linear, for example by building in non-linearity into DAC 314 and/or into a circuit between the DAC 314 and the analogue current drive pixel circuit. Thus, for example, the current drive may be held constant below a threshold data value, for example 10, and the
10 current drive may increase with a parallel exponent of 1.4 above this threshold value, giving a parallel of 2.4 above this threshold value when the proportional-to-time variation is also taken into account. In this way the Rec. 709 standard may be inbuilt into the pixel drive circuitry. Additionally or alternatively the grey-scale look up table 508 of Figure 5 may be arranged to provide a colour law modification to the common
15 input data to the analogue and digital current/duration pixel drives, for example applying the same colour law exponent of 1.2 to the common input data to give the power law exponent of 2.4 desired for sRGB.

Referring now to Figure 6 this shows an alternative arrangement of pixel drive circuitry
20 600 in which both the drive level and time for which an OLED is driven are proportional to the (same) input data signal. Again like elements to those previously described are indicated by like reference numerals.

In the circuit of Figure 6, a sawtooth voltage waveform is applied to voltage reference
25 line 602 and a voltage proportional to the pixel drive current is provided at node 604 by transistor 606, which has the same gate voltage as transistor 258, and series resistor 608. Comparator 610 compares the voltage derived from the programmed pixel drive current, V_{pgm} , with the time-dependent reference voltage to convert the pixel current drive to a corresponding duration T_{pgm} , comparator 610 controlling transistor 612 off
30 when the reference voltage exceeds the V_{pgm} .

No doubt many other effective alternatives will occur to the skilled person. It will be understood that the invention is not limited to the described embodiments and encompasses modifications apparent to those skilled in the art lying within the scope of
35 the claims appended hereto.

CLAIMS

1. An organic light emitting diode (OLED) display, the display comprising:
a substrate bearing a plurality of OLED pixels, each said pixel having
5 associated control circuitry, wherein said control circuitry includes at least one memory
element for storing a value to determine a luminance of an associated OLED pixel, and
wherein said control circuitry has a pixel data input to receive and store, using said
memory element, luminance data determining said luminance of said associated OLED
pixel;
10 wherein said control circuitry is configured to control both a current through a
said OLED pixel and a duration for which said current flows through said pixel; and
wherein the same luminance data controls both said current and said duration
such that said luminance of the associated said OLED pixel has a non-linear response
to said luminance data.
15
2. An OLED display as claimed in claim 1 wherein said luminance data comprises
digital data having a plurality of data bits, and wherein one or more or all of said data
bits control both said current and said duration.
- 20 3. An OLED display as claimed in claim 1 or 2 wherein said control circuitry
comprises first programmable circuitry to program said current and second
programmable circuitry to program said duration.
4. An OLED display as claimed in claim 3 wherein said first programmable
25 circuitry comprises a pixel drive transistor coupled to a storage capacitor to store a
programmed voltage level to program said current, and wherein said second
programmable circuitry comprises a register or timer to provide a programmed timing
value defining said duration.
- 30 5. An OLED display as claimed in claim 4 wherein said programmable circuitry
comprises a digital-to-analogue converter to receive said luminance data and to
provide an analogue output, and a multiplexer to selectively connect said analogue
output to program said voltage level on one of a plurality of said storage capacitors.

6. An OLED display as claimed in claim 4 or 5 wherein said register or timer comprises a register, and wherein said second programmable circuitry further comprises: a controllable switch to control said current through said OLED pixel, a counter, and a comparator having first and second inputs coupled respectively to said counter and to said register and having an output coupled to control said controllable switch.

7. An OLED display as claimed in any preceding claim wherein said control circuitry is provided for each said pixel and wherein a portion of said control circuitry operating to control one or both of said current and said duration is shared between a plurality of said pixels.

8. An OLED display as claimed in claim 1 wherein said luminance data comprises an analogue data signal.

9. An OLED display as claimed in any preceding claim further comprising a plurality of chiplets mounted on said substrate, wherein each said chiplet is mounted adjacent a group of said pixels and comprises a chiplet substrate bearing control circuitry for said group of said pixels.

10. An OLED display as claimed in any one of claims 1 to 9 wherein said non-linear response provides a grey-scale response of one or both of the ITU Rec. 709 and sRGB standards.

11. A method of driving pixels of an organic light-emitting diode (OLED) display, the display comprising: a substrate bearing a plurality of OLED pixels, each said pixel having associated control circuitry, wherein said control circuitry includes at least one memory element for storing a value to determine a luminance of an associated OLED pixel, and wherein said control circuitry has a pixel data input to receive and store, using said memory element, luminance data determining said luminance of said associated OLED pixel; the method comprising using the same luminance data to control both a current through a said OLED pixel and a duration for which said current flows through said pixel such that said luminance of the associated said OLED pixel has a non-linear response to said luminance data.

12. A method of driving pixels of an organic light-emitting diode (OLED) display to provide increased dynamic range, wherein the method comprises:

writing data to a pixel drive circuit of said OLED display;

providing a drive signal from said pixel drive circuit to a said OLED pixel,

5 wherein said drive signal has a drive level and a drive duration; and

controlling both said drive level and said drive duration responsive to the same data said that a luminance of said pixel exhibits a non-linear response to said data.

13. A method as claimed in claim 12 wherein, averaged over a range of said data, said luminance varies as a value of said data raised to a power, wherein the power has a value of equal to or greater than 2.

14. An OLED display having a plurality of pixels, the display comprising:

means for writing data to a pixel drive circuit of said OLED display;

15 means for providing a drive signal from said pixel drive circuit to a said OLED pixel, wherein said drive signal has a drive level and a drive duration; and

means for controlling both said drive level and said drive duration responsive to the same data such that a luminance of said pixel exhibits a non-linear response to said data.

20

15. An OLED display, the display comprising:

a display substrate bearing a plurality of OLED light emitting pixels:

a plurality of chiplets mounted on said substrate, wherein each said chiplet is mounted adjacent a group of said pixels and comprises a chiplet substrate bearing control circuitry for said group of pixels; and

25

wherein said control circuitry on a said chiplet comprises first programmable circuitry to program a drive level for each pixel of said group of said pixels and second programmable circuitry to program a drive duration for each pixel of said group of pixels.

30

16. An OLED display as claimed in claim 15 wherein said first programmable circuitry comprises, for each said pixel of said group, a storage capacitor to store said programmed drive level and a pixel drive transistor coupled to said storage capacitor, and wherein said second programmable circuitry comprises a register or timer for each said pixel of said group to provide said programmed drive duration.

35

17. An OLED display as provided in claim 16 wherein said first programmable circuitry further comprises at least one first switch for each said pixel of said group, coupled to said storage capacitor to enable selective programming of said storage capacitor; and wherein said second programmable circuitry further comprises a second switch for each said pixel of said group, coupled to control the drive to a respective said pixel to apply said drive for a duration responsive to a value from a said register or timer associated with the said pixel.

18. An OLED display as claimed in claim 17 wherein said second programmable circuitry further comprises a counter common to said pixels of said group and comparator for each said pixel of said group, wherein each said comparator has an output coupled to one of said second switches and inputs coupled to said common counter and to said register.

19. An OLED display as claimed in any one of claims 16 to 18 wherein said first programmable circuitry further comprises a digital-to-analogue converter and multiplexing circuitry coupled between said digital-to-analogue converter and said storage capacitor to selectively program a value from said digital-to-analogue converter onto a selected said storage capacitor of said chiplet.

20. An OLED display as claimed in any one of claims 15 to 19 wherein said first and second programmable circuitry share a common data input line.

21. An OLED display as claimed in claim 20 wherein a shared data value on said common data input line programs both said drive level and said drive duration such that a luminance value of a said pixel is dependent on said shared data value to a power, wherein said power is equal to or greater than 2.

22. An OLED display as claimed in any one of claims 15 to 21 wherein a response characteristic of one or both of said first and second programmable circuitry, to a value of data programming respectively said drive level and said drive duration, comprises a piecewise response wherein a first range of values of said data have a first response characteristic and a second, higher range of values of said data have a second, different response characteristic.

23. An OLED display as claimed in any one of claims 15 to 22 wherein said first programmable circuitry comprises current programmed circuitry programmed by a current flowing in a programming line of the circuitry.
- 5 24. An OLED display as claimed in any one of claims 15 to 23 further comprising a controller to select a said chiplet and to provide data to said selected chiplet to program said first and second programmable circuitry.

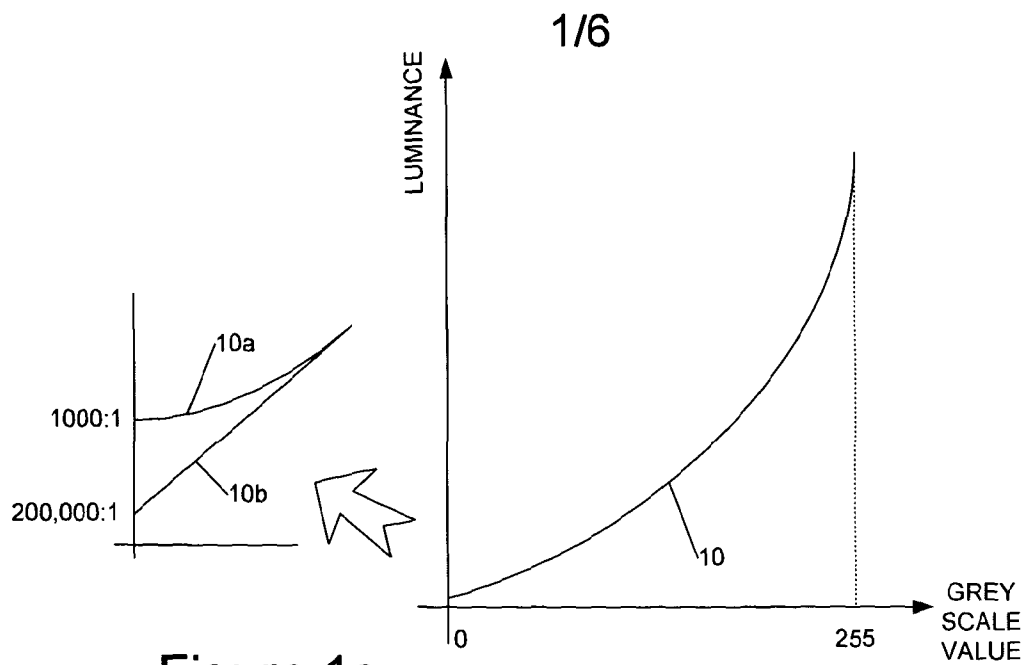


Figure 1a
(PRIOR ART)

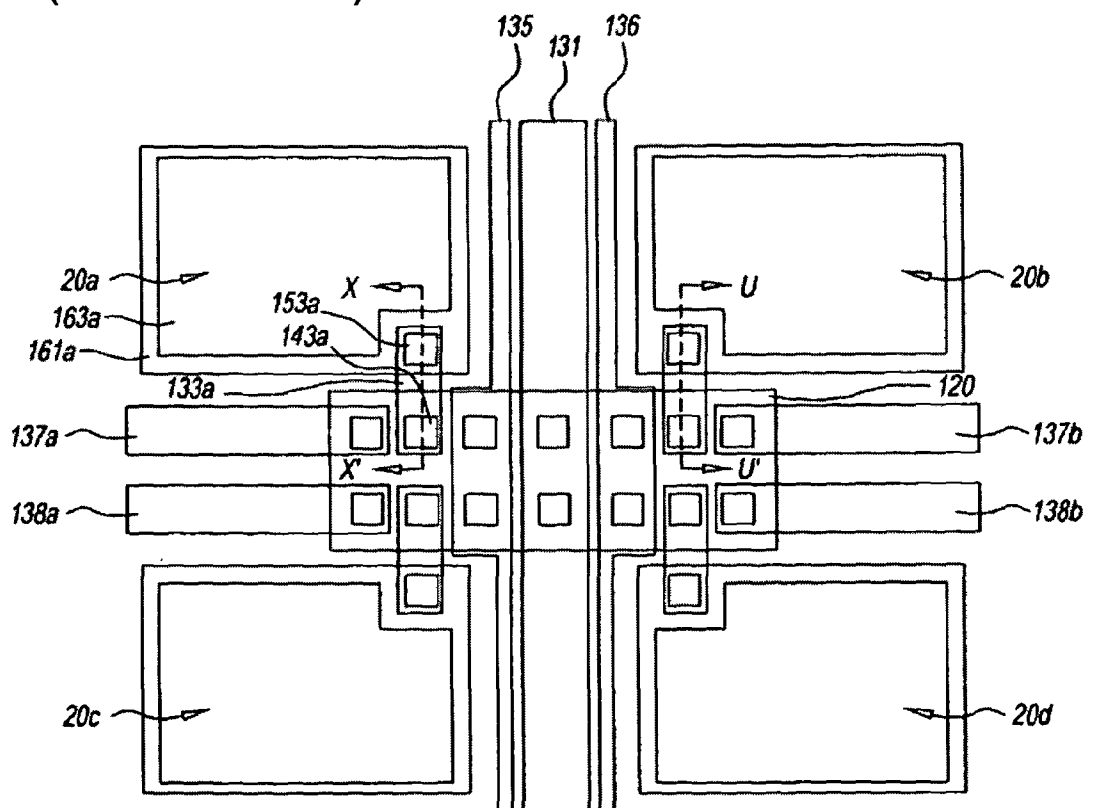


Figure 1b
(PRIOR ART)

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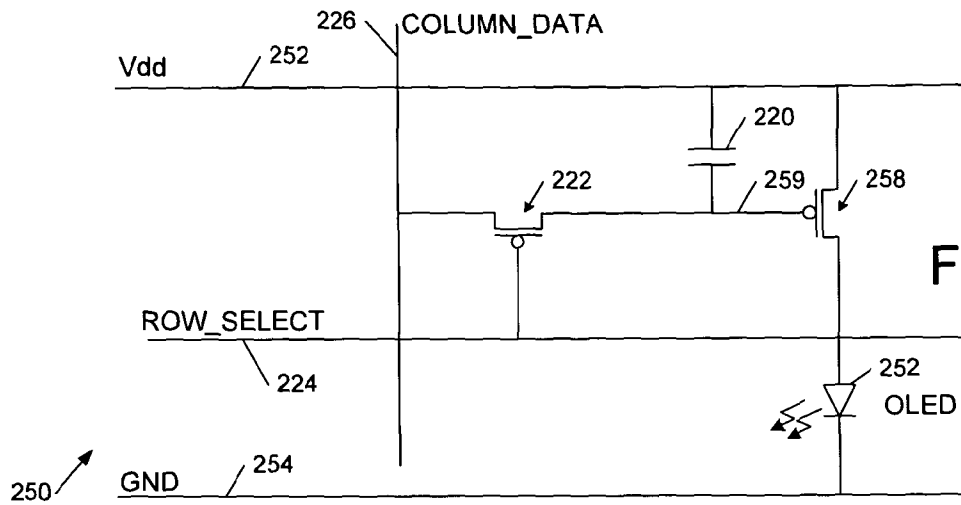


Figure 2a

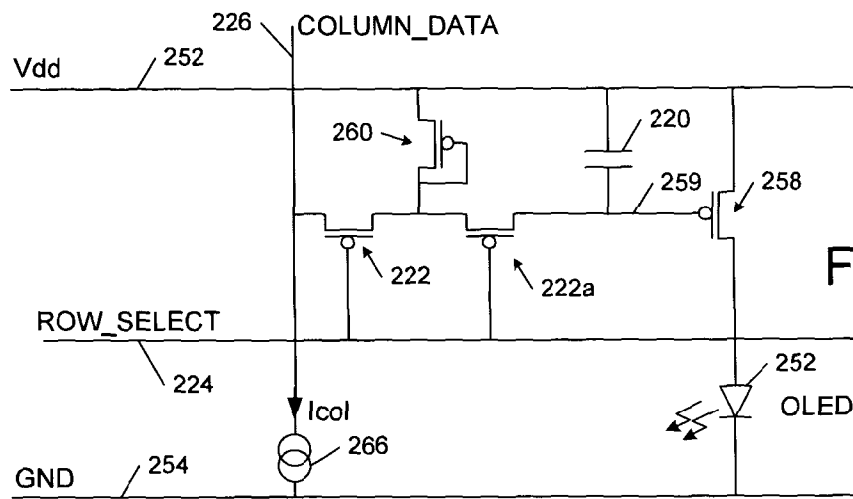


Figure 2b

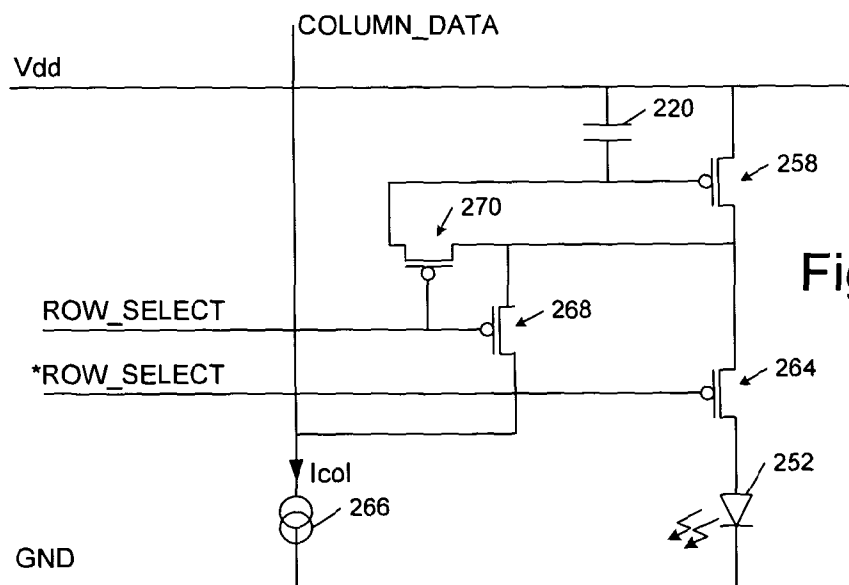


Figure 2c

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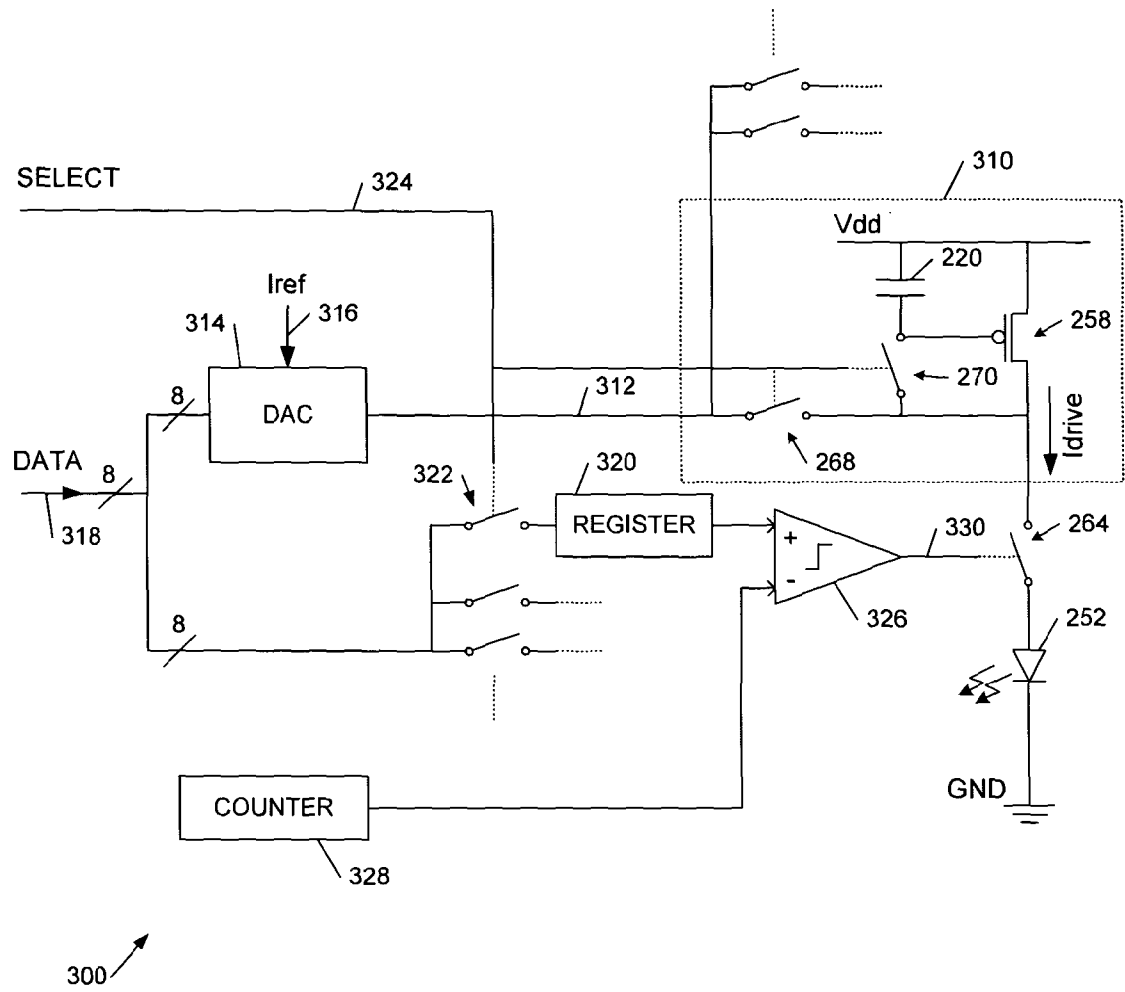


Figure 3

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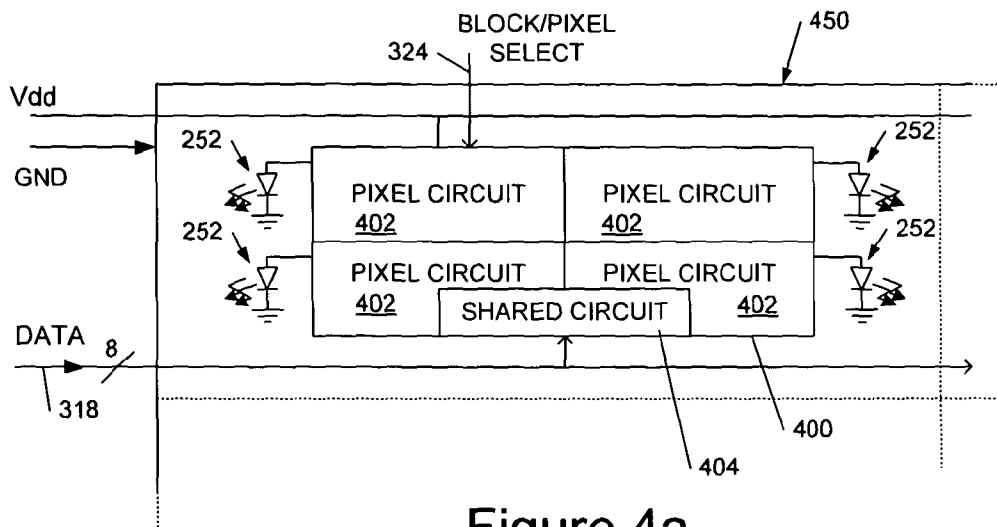


Figure 4a

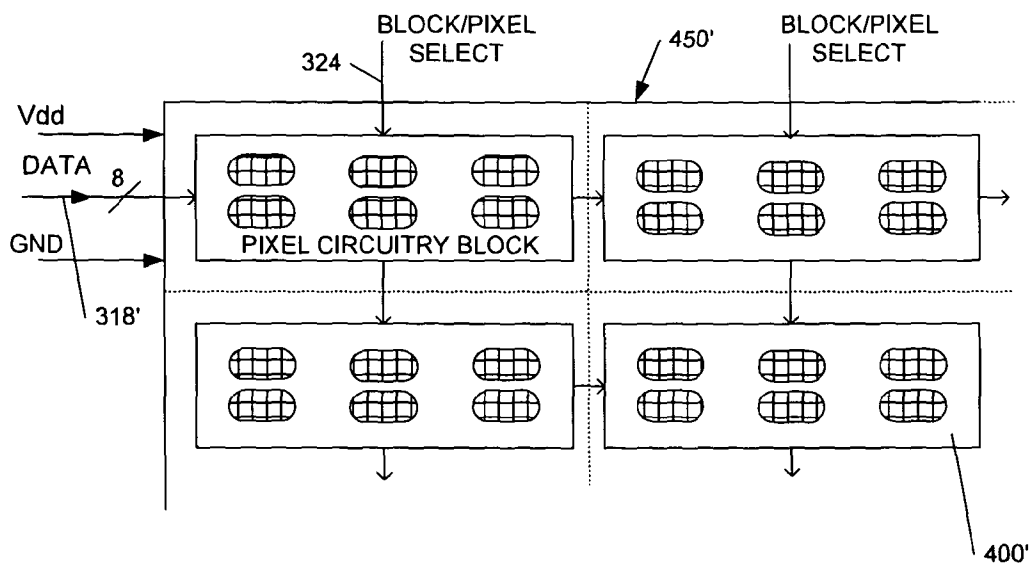


Figure 4b

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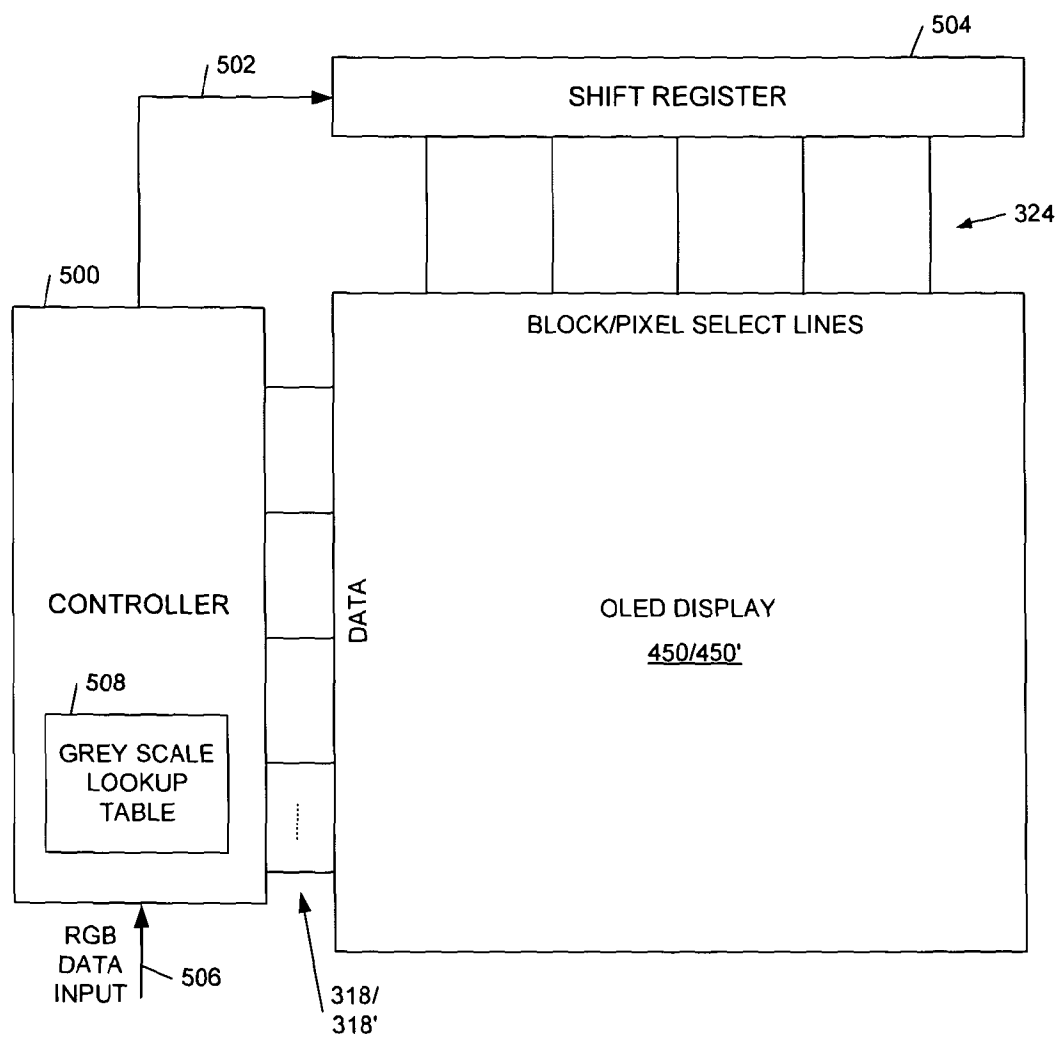


Figure 5

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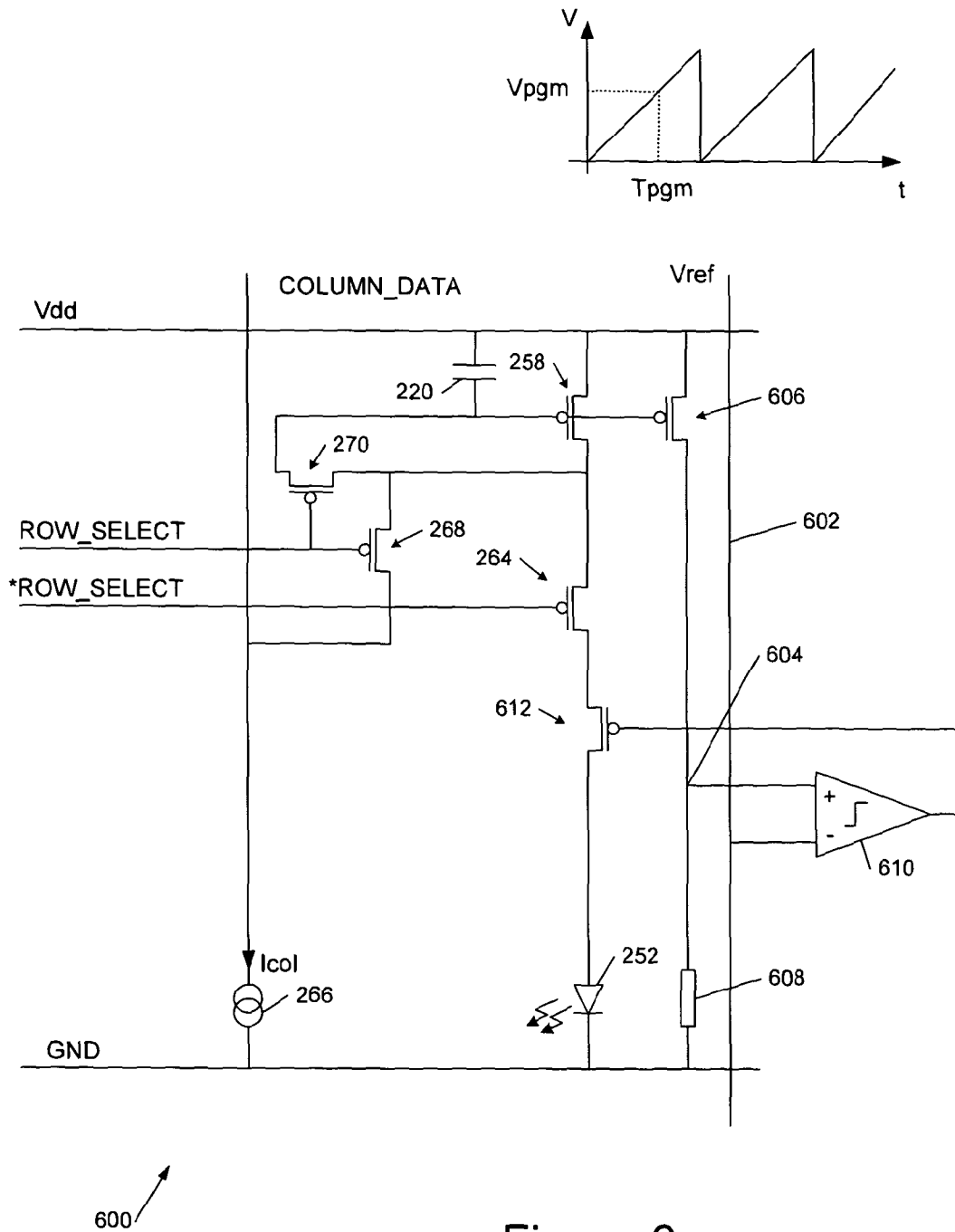


Figure 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2011/001290

A. CLASSIFICATION OF SUBJECT MATTER
INV. G09G3/32 G09G3/20 H01L27/32
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G09G H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

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Y	paragraph [0009] - paragraph [0018] paragraph [0097] - paragraph [0216] paragraph [0233] - paragraph [0234] -----	9,15-24
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Further documents are listed in the continuation of Box C.



See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

28 November 2011

Date of mailing of the international search report

02/12/2011

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2011/001290

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