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(54) Title: SULFURATION RESISTANT CHIP RESISTOR AND METHOD FOR MAKING SAME

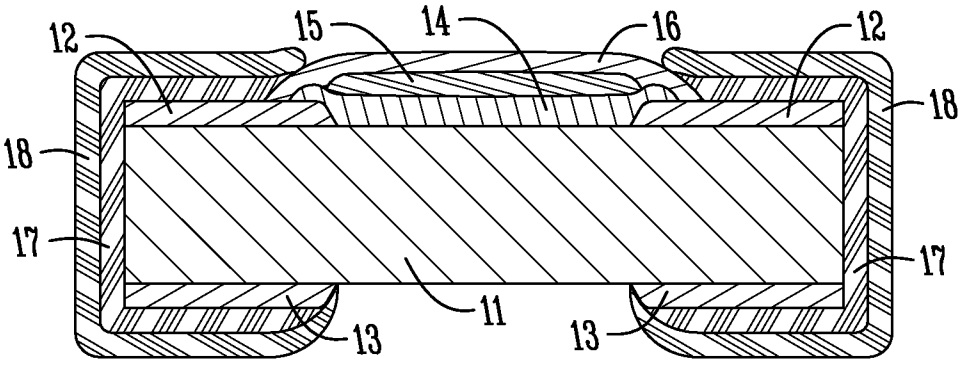

Fig. 1

(57) Abstract: A chip resistor includes an insulating substrate 11, top terminal electrodes 12 formed on top surface of the substrate using silver-based cermet, bottom electrodes 13, resistive element 14 that is situated between the top terminal electrodes 12 and overlaps them partially, an optional internal protective coating 15 that covers resistive element 14 completely or partially, an external protective coating 16 that covers completely the internal protection coating 15 and partially covers top terminal electrodes 12, a plated layer of nickel 17 that covers face sides of the substrate, top 12 and bottom 13 electrodes, and overlaps partially external protective coating 16, finishing plated layer 18 that covers nickel layer 17. The overlap of nickel layer 17 and external protective layer 16 possesses a sealing property because of metallization of the edges of external protective layer 16 prior to the nickel plating process.

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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

TITLE: SULFURATION RESISTANT CHIP RESISTOR AND METHOD FOR MAKING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U.S.C. § 119 to provisional application Serial No. 60/892,503 filed March 1, 2007, herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to chip resistors, and in particular, chip resistors which are sulfuration resistant.

Terminal electrodes in a majority of thick-film chip resistors and in some thin-film resistors are made of silver-based cermets. Metallic silver has several advantageous properties, including high electrical conductivity and excellent immunity to oxidizing when silver based cermets are fired in the air. Unfortunately metallic silver also has its shortcomings. Once such shortcoming is metallic silver's remarkable susceptibility to sulfur and sulfur compounds. At that, silver forms non-conductive silver sulfide resulting in open circuit in the silver-based resistor terminals. The described failure mechanism is called sulfuration phenomenon or sulfuration.

A prior art non sulfur proof thick-film chip resistor is presented in Figure 2. It consists of an isolative substrate **1**, upper silver-based terminal electrodes **2**, bottom silver-based electrodes **3**, a resistive element **4**, an optional protective layer **5**, an external protective layer **6**, plated nickel layer **7**, and a plated finishing layer (commonly tin) **8**. Each upper electrode **2** is covered by abutting layers: (a) external protective coating **6** (glass or polymer), and (b) plated nickel **7** and finishing **8** layers. The problem is that non-metal coating **6** from one side, and plated metal layers **6**, **7** from another side have a poor adhesion to each other. It promotes a small gap between them and results in ambient air penetration to the surface of silver electrodes **2**. If the ambient air includes sulfur compounds, the silver electrodes will be destructed after a time. That is why commodity chip resistors often fail in automotive and industrial applications.

Two known ways to prevent the sulfuration phenomenon are used. One method involves replacing or cladding of silver by another noble metal that is sulfur proof (gold, silver-palladium alloy, etc.). A second method is to prevent the silver-based terminals from contact with ambient air (sealing of the terminals).

The disadvantages of the first method include the expensiveness of sulfur proof noble metals, the lower electrical conductivity of sulfur proof noble metals relative to metallic silver, as well as the possible incompatibility of non-silver terminals with thick-film resistor inks that are designed for use with silver termination.

The second method according to prior art (see for example US Patent 7,098,768, herein incorporated by reference in its entirety) consists of adding of two layers: auxiliary upper electrodes **9** (Figure 3) and uppermost overcoat **6'**. Auxiliary upper electrodes **9** cover completely each of upper silver-based terminal electrodes **2** and overlap partially the external protective coating **6**. The uppermost overcoat **6'** covers the middle portion of the resistor and overlaps auxiliary upper electrodes **9**.

In such a configuration, the auxiliary upper electrodes should be both platable (conductive) and sulfur proof. Examples of such material include polymer-based thick-film inks with carbon filler or base metal filler and sintering-type thick-film inks with base metal filler. The disadvantages of using auxiliary upper electrodes include low electrical conductivity and poor platability of polymer-based materials with carbon or base metal filler, possible resistance shift when sintering type inks are used for auxiliary upper electrodes, problematic implementation in small size resistors (1 mm length and less) where it is difficult to keep positional relationship between multiple layers that overlap each other in the terminal, and increased resistor thickness.

What is needed is an improved chip resistor which is sulfuration resistant.

BRIEF SUMMARY OF THE INVENTION

It is therefore a principal object, feature, aspect, or advantage of the present invention to improve over the state of the art relative to addressing the sulfuration phenomenon with chip type of resistor.

Another object, feature, or advantage of the present invention is to provide for a chip resistor which is sulfuration resistant which does not require an additional protective layer which would increase thickness of the chip resistor beyond the thickness of a standard (non-sulfuration resistant) chip resistor.

Yet another object, feature, or advantage of the present invention is a configuration or design that is applicable to all sizes of chip resistors, including the smallest ones where, for example, introduction of an additional protective layer with secure overlaps with adjacent layers would be potentially problematic.

A still further object, feature, or advantage of the present invention is to provide a chip resistor which does not have the limitations associate with the additional protective layers found in the prior art, such as being (a) conductive, (b) non-silver, (c) suitable for deposition at low temperature. Materials that meet such requirements (for example polymer based carbon ink) have limited platability.

Thus, a still further object, feature, or advantage of the present invention is to provide a sulfuration resistant chip resistor with terminals having good platability.

Further objects, features, aspects, and advantages of the present invention will become more apparent with reference to the other parts of this application. One or more of these and/or other objects, features, aspects, or advantages of the present invention will become apparent from the specification and claims that follow.

According to one aspect of the present invention a chip resistor includes upper sulfuration-susceptible terminal electrodes on opposite sides of a resistive element mounted over an insulating substrate and an external non-conductive protective coating over the resistive element. There is at least one conducting metal plated layer covering opposite face sides of the insulating substrate and part of the top sulfuration-susceptible terminal electrodes, the metal plated layer being adhered to the sulfuration-susceptible terminal electrodes and adjacent edges of the external non-conductive protective coating by a pre-applied metal layer.

According to another aspect of the present invention, a method is provided for deterring sulfuration in a chip resistor having upper sulfuration-susceptible terminal electrodes on opposite sides of a resistive element mounted over an insulating substrate, an external non-conductive protective coating over the resistive element, and at least one conducting metal plated layer covering opposite face sides of the insulating substrate and part of the top sulfuration-susceptible terminal electrodes. The method provides for sealing the terminal electrodes from the external environment. The sealing may be performed by overlapping the metal plated layer over exposed top portions of the terminal electrodes and over adjacent edges of the external non-conductive protective coating or sealing the terminal electrodes comprises moralizing adjacent edges of the external non-conductive protective coating prior to application of the metal plated layer.

According to another aspect of the present invention, a chip resistor is formed by the process of forming top terminal electrodes and a resistive element on the top of an insulative substrate having face sides, forming a non-conducting external protective coating over the resistive element and adjacent portions of the top terminal electrodes, masking a middle portion of the external protective coating, metallizing edges of the external protective coating by sputtering, metallizing face sides of the substrate by sputtering or by conductive ink application, removing the mask, nickel plating the metallized edges of the external protective coating and face sides of the substrate, and placing a finishing layer over the nickel plating.

According to another aspect of the present invention, a chip resistor includes an insulating substrate having a top surface, an opposite bottom surface and opposing face surfaces, top terminal electrodes formed on the top surface of the substrate, bottom electrodes formed on the bottom surface of the substrate, a resistive element positioned between the top terminal electrodes and partially overlapping the top terminal electrodes, an external protective coating that partially covers the top terminal electrodes, wherein edges of the external protective coating being activated to facilitate coverage by plating, a plated layer of nickel covering the face surfaces of the substrate, the top and bottom electrodes, and overlapping the edges of the external protective coating thereby sealing the underlying top terminal electrodes from ambient atmosphere.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a substantially enlarged cross-sectional view of an apparatus according to one aspect of the present invention.

Figure 2 is a substantially enlarged cross-sectional view of a prior art (non sulfuration resistant) resistor.

Figure 3 is similar to Figure 2 but illustrates a prior art sulfuration resistant resistor.

Figure 4 is a cross-sectional diagram and illustration of a method of making the resistor of Figure 1 according to an aspect of the present invention.

Figure 5 is a cross-sectional diagram and illustration of a method of making a resistor using a metallization process using low intensity sputtering (without masking).

Figure 6 is a cross-sectional diagram and illustration of a method of making a resistor using very high intensity sputtering (with or without masking).

Figure 7 is a flow diagram illustrating one embodiment of a manufacturing process of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

For a better understanding of the invention, a specific apparatus and method of making same will now be described in detail. It is to be understood that this is but one form the invention can take. Variations obvious to those skilled in the art will be included within the invention.

The present invention relates to a chip resistor (Figure 1) that comprises an insulating substrate **11**, top terminal electrodes **12** formed on top surface of the substrate using silver-based cermet, bottom electrodes **13**, resistive element **14** that is situated between the top terminal electrodes **12** and overlaps them partially, optional internal protective coating **15** that covers resistive element **14** completely or partially, external protective coating **16** that covers completely the internal protection coating **15** and partially

covers top terminal electrodes **12**, plated layer of nickel **17** that covers face sides of the substrate, top **12** and bottom **13** electrodes, and overlaps partially external protective coating **16**, finishing plated layer **18** that covers nickel layer **17**.

The overlap of nickel layer **17** and external protective layer **16** possesses a sealing property because of making the edges of external protective layer **16** platable prior to nickel plating process. Thus, silver terminal electrodes are sealed without use of dedicated protective layers. The silver terminal electrodes are sealed by imparting a protective function to the nickel plating layer that is commonly used as diffusion and leaching barrier between the silver electrodes and the finishing metallization layer (commonly, the tin layer) in terminals of standard (non sulfur proof) chip resistors.

Possible ways to make dielectric material like protective layer **16** platable include, without limitation, activating it for example by application of conductive material (metal sputtering, chemical deposition of metal, etc.) or by changing its structure (carbonization of polymers by heating, etc.).

Figure 4 shows a process where metal sputtering is used for activation of the edges of the external protective coating **16**. An appropriate metal (for example nichrome alloy) is sputtered on external protective coating **16** making its edges not covered by mask **19** platable. During the following plating process the sputtered metallization layer promotes nickel to plate not only silver terminals **12**, **13**, and face surfaces **11'** of the substrate **11** but to extend to the edges of external protective coating **16** sealing the underlying silver electrodes **12**. A good adhesion between nickel layer and metallized edges of external protective coating **16** insures good sealing of silver electrodes **12**.

Figure 5 shows a second implementation of sputtering process. Sputtering is performed from the top side of chip resistor without masking of the external protective coating **16** but with extremely low intensity of sputtering. Resulting poor metallization facilitates plating of the external protective coating edge but very soon degrades in plating bath because of mechanical abrasion. Therefore, solid metallization of entire top surface does not form.

Figure 6 shows a third implementation of sputtering process. Sputtering is performed from face sides of stacked chips with or without masking of external protective coating **16** with very high intensity of sputtering sufficient to penetrate into the gap

between the adjacent stacked chips and insure metallization of extreme portions of top side of chip. The gap between stacked chips exists because the middle portion of chip covered by external protective coating **16** is thicker than terminal area.

In the prior art (Figure 2 and Figure 3) nickel layer **7** cannot act as a silver protection element because of the poor adhesion of plated nickel layer **7** to the edge of protective coatings **6** (Figure 2) and **6'** (Figure 3).

In order to protect the sulfuration-susceptible electrodes the present invention provides for imparting the function of protective layer to the plated nickel layer that is commonly used as diffusion and leaching barrier between silver electrodes and finishing metallization layer (tin layer) in terminals of standard (non sulfur proof chip resistor). For this purpose an appropriate metal (for example nichrome alloy) is deposed on the edges of external protective coating (that are adjacent to silver electrodes) making these edges platable. It promotes nickel to plate not only silver electrodes but to extend to the edges of external protective coating sealing the underlying silver electrodes.

Advantages of this approach include that no additional protective layer is needed. Therefore, thickness of chip resistor is the same as thickness of standard (non sulfur-proof) chip resistor. In addition, the configuration is applicable to all sizes of chips including the smallest ones as there need not be an additional protective layer. In addition, the terminals maintain good platability.

Manufacturing process

The present invention also relates to the method of making the chip resistor. Figure 7 illustrates one embodiment of a manufacturing process of the present invention. In step **20**, the top **12** and bottom **13** terminal electrodes formation is performed. Next, in step 21, resistive element **14** formation is performed. Next, in step **22**, an optional internal protective coating **15** formation may be performed. Of course, this step is optional and not required. Next, in step **23**, external protective coating **16** formation is performed. In step **24**, an optional masking of middle portion of external protective coating by mask **19** may be performed. In step **25**, activation of the edges of external protective coating **16** (for example by metal sputtering as shown in Figures 4-6) is performed. In step **26**, activation of face sides **11'** of the substrate **11** (for example by metal sputtering or by conductive ink

application) is performed. In step **27**, removal of the optional mask is performed where the optional mask was used. In step **28**, plating is performed (preferably using nickel or a nickel alloy). In step **29**, the layer plating is finished. Although presented in one order, the sequence of steps maybe altered as appropriate. For example, the sequence of top **12**, bottom **13** terminal electrodes, and resistor **14** formation may be altered if necessary.

Step **25** imparts the withstand ability of chip resistor to sulfur containing ambient environment by sealing the sulfuration susceptible terminals. Thus, a method and apparatus for a sulfuration resistant chip resistor has been disclosed. The present invention contemplates numerous variations, including variations in the type of materials, the sequence of steps, whether optional steps are performed or not, and other variations, alternatives, and options within the spirit and scope of the invention.

What is claimed is:

1. A chip resistor comprising:
upper sulfuration-susceptible terminal electrodes on opposite sides of a resistive element mounted over an insulating substrate;
an external non-conductive protective coating over the resistive element;
at least one conducting metal plated layer covering opposite face sides of the insulating substrate and part of the top sulfuration-susceptible terminal electrodes, the metal plated layer being adhered to the sulfuration-susceptible terminal electrodes and adjacent edges of the external non-conductive protective coating by a pre-applied metal layer.

2. The chip resistor of claim 1 wherein the pre-applied metallization layer is applied by metallization of face sides of the insulating substrate and edges of the external non-conductive protective coating.

3. The chip resistor of claim 2 wherein the metallization layer is accomplished by sputtering.

4. The chip resistor of claim 1 wherein the metal plated layer is applied by sputtering.

5. The chip resistor of claim 1 further comprising a second metal plated layer over the metal plated layer adhered to the terminal electrodes.

6. The chip resistor of claim 1 further comprising overlapping the metal plated layer over a portion of the adjacent edges of the external non-conductive protective coating.

7. The chip resistor of claim 6 wherein the metallization layer and overlapping effectively seals the terminal electrodes.

8. The chip resistor of claim 7 wherein the sealing resists sulfuration phenomenon relative the terminal electrodes.

9. The chip resistor of claim 1 wherein the chip resistor is a thick film chip resistor.

10. The chip resistor of claim 1 wherein the chip resistor is a thin film chip resistor.

11. The chip resistor of claim 1 wherein the terminal electrodes comprise silver.

12. A method of deterring sulfuration in a chip resistor having upper sulfuration-susceptible terminal electrodes on opposite sides of a resistive element mounted over an insulating substrate, an external non-conductive protective coating over the resistive element, and at least one conducting metal plated layer covering opposite face sides of the insulating substrate and part of the top sulfuration-susceptible terminal electrodes, the method comprising sealing the terminal electrodes from the external environment.

13. The method of claim 12 wherein the step of sealing the terminal electrodes comprises overlapping the metal plated layer over exposed top portions of the terminal electrodes and over adjacent edges of the external non-conductive protective coating.

14. The method of claim 12 wherein the step of sealing the terminal electrodes comprises metallizing adjacent edges of the external non-conductive protective coating prior to application of the metal plated layer.

15. A chip resistor made by the process of claim 14.

16. A chip resistor made by the process comprising:

forming top terminal electrodes and a resistive element on the top of an insulative substrate having face sides;

forming a non-conducting external protective coating over the resistive element and adjacent portions of the top terminal electrodes;

masking a middle portion of the external protective coating;

metallizing edges of the external protective coating by sputtering;

metallizing face sides of the substrate by sputtering or by conductive ink application;

removing the mask;

nickel plating the metallized edges of the external protective coating and face sides of the substrate; and

placing a finishing layer over the nickel plating.

17. A chip resistor, comprising:

an insulating substrate having a top surface, an opposite bottom surface and opposing face surfaces;

top terminal electrodes formed on the top surface of the substrate;

bottom electrodes formed on the bottom surface of the substrate;

a resistive element positioned between the top terminal electrodes and partially overlapping the top terminal electrodes;

an external protective coating that partially covers the top terminal electrodes;

wherein edges of the external protective coating being activated to facilitate coverage by plating;

a plated layer of nickel covering the face surfaces of the substrate, the top and bottom electrodes, and overlapping the edges of the external protective coating thereby sealing the underlying top terminal electrodes from ambient atmosphere.

18. The chip resistor of claim 17 further comprising an internal protective coating at least partially covering the resistive element and wherein the external protective coating entirely covers the internal protective coating.

19. The chip resistor of claim 17 wherein the top terminal electrodes and the bottom terminal electrodes are formed of a sulfuration susceptible material.

20. The chip resistor of claim 19 wherein the sulfuration susceptible material comprises silver.

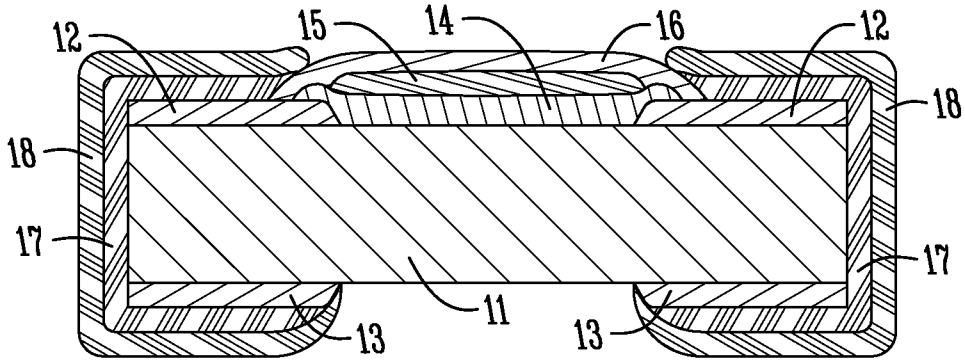


Fig. 1

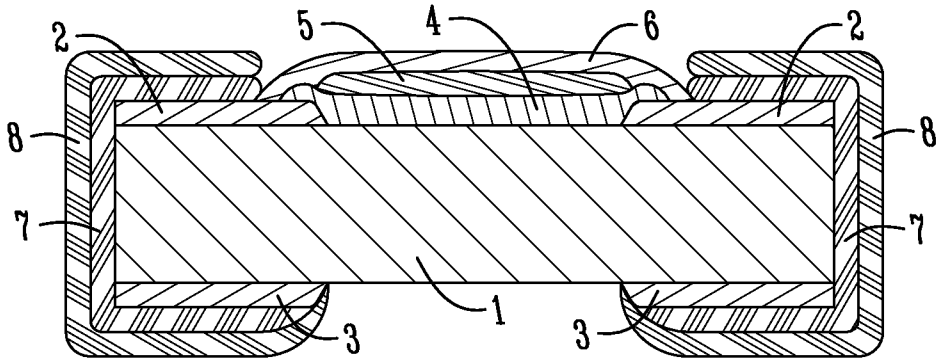


Fig.2 PRIOR ART)

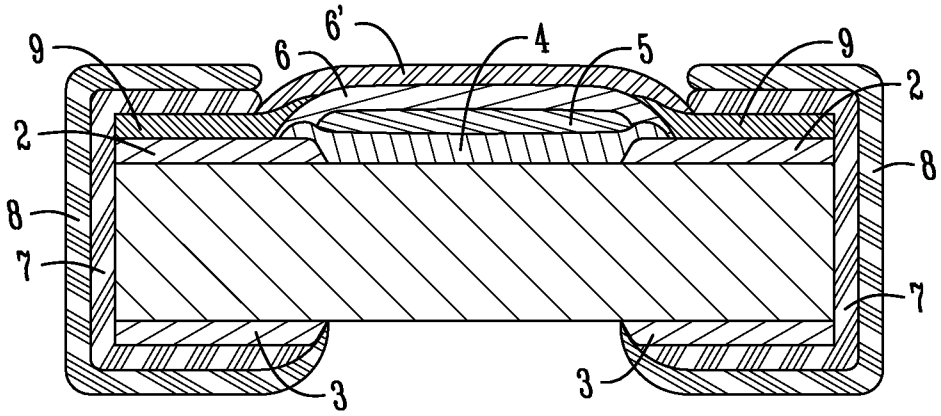


Fig.3 PRIOR ART)

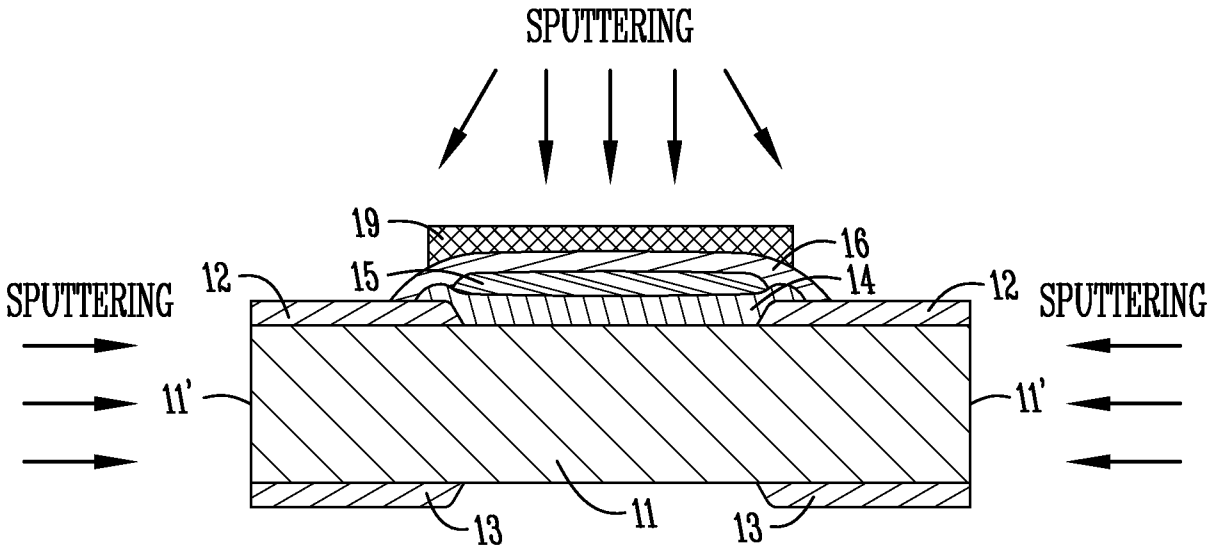
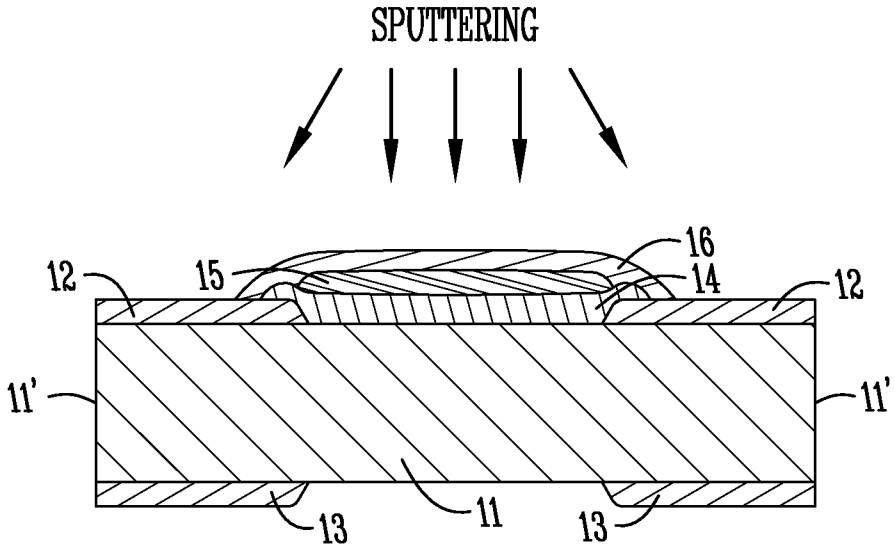


Fig.4


SPUTTERING
16
12
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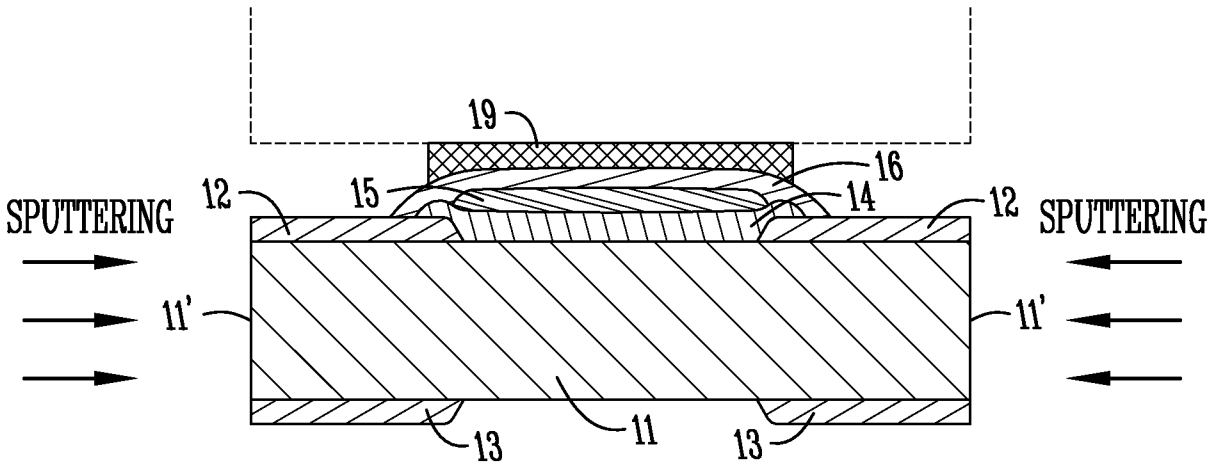
13
11
13

Fig. 5


19
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SPUTTERING
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14
12
SPUTTERING
11'
11'
13
11
13

Fig. 6

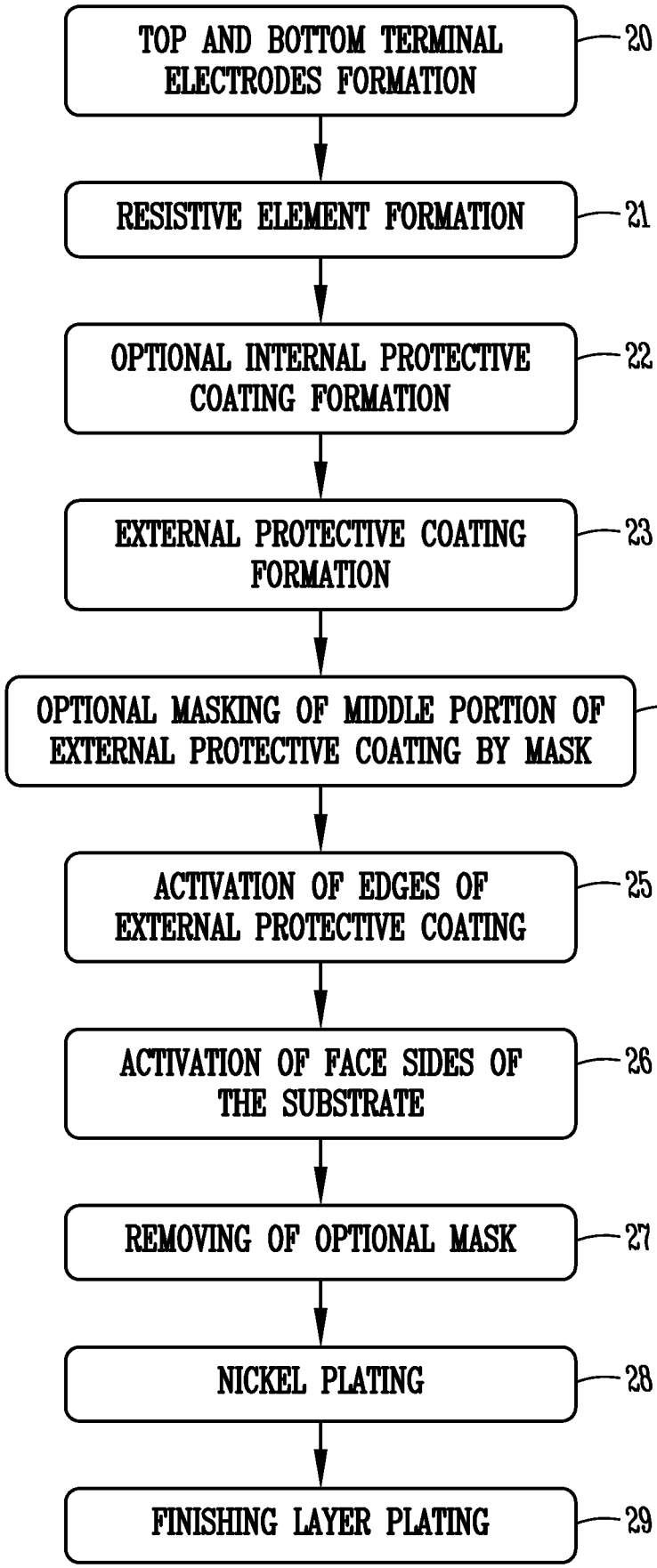
TOP AND BOTTOM TERMINAL ELECTRODES FORMATION
20
RESISTIVE ELEMENT FORMATION
21
OPTIONAL INTERNAL PROTECTIVE COATING FORMATION
22
EXTERNAL PROTECTIVE COATING FORMATION
23
OPTIONAL MASKING OF MIDDLE PORTION OF EXTERNAL PROTECTIVE COATING BY MASK
24
ACTIVATION OF EDGES OF EXTERNAL PROTECTIVE COATING
25
ACTIVATION OF FACE SIDES OF THE SUBSTRATE
26
REMOVING OF OPTIONAL MASK
27
NICKEL PLATING
28
FINISHING LAYER PLATING
29

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/054557

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01C17/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01C H05K B23P H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X X	US 2002/148106 A1 (TSUKADA TORAYUKI [JP] ET AL) 17 October 2002 (2002-10-17) paragraphs [0031], [0032], [0048], [0053]; figures 1,9,11	1 1-20
X	US 6 201 290 B1 (YAMADA HIROYUKI [JP] ET AL) 13 March 2001 (2001-03-13) column 4; claims 1,5; figures 1,2	1-20
Y	EP 1 271 566 A (ALPS ELECTRIC CO LTD [JP]) 2 January 2003 (2003-01-02) paragraph [0015]	1-20
Y	US 5 966 067 A (MURAKAMI MAMORU [US] ET AL) 12 October 1999 (1999-10-12) column 2, lines 6-60	1-20

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
3 July 2008	14/07/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Dessaux, Christophe

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/054557

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Information on patent family members

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