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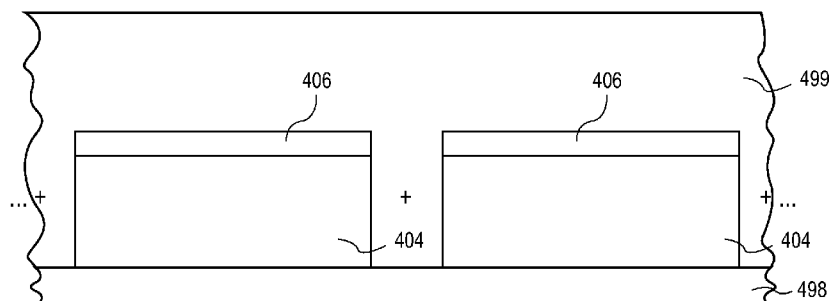


FIG. 4D

(57) Abstract: Methods of dicing semiconductor wafers, and transporting singulated die, are described. In an example, a method of dicing a wafer having a plurality of integrated circuits thereon involves dicing the wafer into a plurality of singulated dies disposed above a dicing tape. The method also involves forming a water soluble material layer over and between the plurality of singulated dies, above the dicing tape.

METHOD OF DICED WAFER TRANSPORTATION**CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] This application claims the benefit of U.S. Provisional Application No. 61/671,365, filed July 13, 2012, and U.S. Provisional Application No. 61/775,149, filed March 8, 2013, the entire contents of which are hereby incorporated by reference herein.

BACKGROUND**1) FIELD**

[0002] Embodiments of the present invention pertain to the field of semiconductor processing and, in particular, to methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

2) DESCRIPTION OF RELATED ART

[0003] In semiconductor wafer processing, integrated circuits are formed on a wafer (also referred to as a substrate) composed of silicon or other semiconductor material. In general, layers of various materials which are either semiconducting, conducting or insulating are utilized to form the integrated circuits. These materials are doped, deposited and etched using various well-known processes to form integrated circuits. Each wafer is processed to form a large number of individual regions containing integrated circuits known as dice.

[0004] Following the integrated circuit formation process, the wafer is "diced" to separate the individual die from one another for packaging or for use in an unpackaged form within larger circuits. The two main techniques that are used for wafer dicing are scribing and sawing. With scribing, a diamond tipped scribe is moved across the wafer surface along pre-formed scribe lines. These scribe lines extend along the spaces between the dice. These spaces are commonly referred to as "streets." The diamond scribe forms shallow scratches in the wafer surface along the streets. Upon the application of pressure, such as with a roller, the wafer separates along the scribe lines. The breaks in the wafer follow the crystal lattice structure of the wafer substrate. Scribing can be used for wafers that are about 10 mils (thousandths of an inch) or less in thickness. For thicker wafers, sawing is presently the preferred method for dicing.

[0005] With sawing, a diamond tipped saw rotating at high revolutions per minute contacts the wafer surface and saws the wafer along the streets. The wafer is mounted on a supporting member such as an adhesive film stretched across a film frame and the saw is repeatedly applied to both the vertical and horizontal streets. One problem with either scribing or sawing is that chips and gouges can form along the severed edges of the dice. In addition, cracks can form and propagate from the edges of the dice into the substrate and render the integrated circuit inoperative. Chipping and cracking are particularly a problem with scribing because only

one side of a square or rectangular die can be scribed in the <110>direction of the crystalline structure. Consequently, cleaving of the other side of the die results in a jagged separation line. Because of chipping and cracking, additional spacing is required between the dice on the wafer to prevent damage to the integrated circuits, e.g., the chips and cracks are maintained at a distance from the actual integrated circuits. As a result of the spacing requirements, not as many dice can be formed on a standard sized wafer and wafer real estate that could otherwise be used for circuitry is wasted. The use of a saw exacerbates the waste of real estate on a semiconductor wafer. The blade of the saw is approximate 15 microns thick. As such, to insure that cracking and other damage surrounding the cut made by the saw does not harm the integrated circuits, three to five hundred microns often must separate the circuitry of each of the dice. Furthermore, after cutting, each die requires substantial cleaning to remove particles and other contaminants that result from the sawing process.

[0006] Plasma dicing has also been used, but may have limitations as well. For example, one limitation hampering implementation of plasma dicing may be cost. A standard lithography operation for patterning resist may render implementation cost prohibitive. Another limitation possibly hampering implementation of plasma dicing is that plasma processing of commonly encountered metals (e.g., copper) in dicing along streets can create production issues or throughput limits.

SUMMARY

[0007] Embodiments of the present invention include methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

[0008] In an embodiment, a method of dicing a wafer having a plurality of integrated circuits thereon involves dicing the wafer into a plurality of singulated dies disposed above a dicing tape. The method also involves forming a water soluble material layer over and between the plurality of singulated dies, above the dicing tape.

[0009] In an embodiment, an apparatus includes a plurality of singulated dies disposed above a dicing tape. A water soluble material layer is disposed over and between the plurality of singulated die, above the dicing tape.

[0010] In an embodiment, a method of dicing a wafer having a plurality of integrated circuits thereon involves forming a water soluble mask layer above the wafer, the wafer disposed above a dicing tape. The method also involves scribing the water soluble mask layer with a laser scribing process to expose portions of the wafer. The method also involves etching the exposed portions of the wafer with a plasma process to dice the wafer into a plurality of singulated dies. The method also involves forming a water soluble protecting layer over and between the plurality of singulated dies, above the dicing tape.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 illustrates a top plan of a semiconductor wafer to be diced, in accordance with an embodiment of the present invention.

[0012] Figure 2 illustrates a top plan of a semiconductor wafer to be diced that has a dicing mask formed thereon, in accordance with an embodiment of the present invention.

[0013] Figure 3 is a Flowchart representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention.

[0014] Figure 4A-4E illustrate cross-sectional views of a semiconductor wafer including a plurality of integrated circuits during various operations in a method of dicing the semiconductor wafer, corresponding to the operations of the Flowchart of Figure 3, in accordance with an embodiment of the present invention.

[0015] Figure 5 illustrates the effects of using a laser pulse in the femtosecond range versus longer pulse times, in accordance with an embodiment of the present invention.

[0016] Figure 6 illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present invention.

[0017] Figure 7 includes a plot of absorption coefficient as a function of photon energy for crystalline silicon (c-Si), copper (Cu), crystalline silicon dioxide (c-SiO₂), and amorphous silicon dioxide (a-SiO₂), in accordance with an embodiment of the present invention.

[0018] Figure 8 is an equation showing the relationship of laser intensity for a given laser as a function of laser pulse energy, laser pulse width, and laser beam radius.

[0019] Figures 9A-9D illustrate cross-sectional views of various operations in a method of dicing a semiconductor wafer, in accordance with an embodiment of the present invention.

[0020] Figure 10 illustrates compaction on a semiconductor wafer achieved by using narrower streets versus conventional dicing which may be limited to a minimum width, in accordance with an embodiment of the present invention.

[0021] Figure 11 illustrates freeform integrated circuit arrangement allowing denser packing and, hence, more die per wafer versus grid alignment approaches, in accordance with an embodiment of the present invention.

[0022] Figure 12 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present invention.

[0023] Figure 13 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0024] Methods of dicing semiconductor wafers, and transporting singulated die, are described. In the following description, numerous specific details are set forth, such as femtosecond-based laser scribing and plasma etching conditions and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known aspects, such as integrated circuit fabrication, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0025] One or more embodiments are directed to transportation of singulated die during a die singulation process. For example, upon completely dicing a semiconductor wafer, the resulting singulated die may need to be transported as a plurality of die. In an embodiment, a wafer to be diced is mounted on a dicing tape on a frame ring prior to dicing. After dicing, dies are singulated relative to one another but stay on the dicing tape. Prior to die pick for subsequent packaging/assembly, transportation of the singulated dies as a group may need to be performed in order to relocate the dies to a remote place (e.g., another country or city) with all singulated dies staying on the framed dicing tape. Since, in an embodiment, the die-to-die spacing (the dicing kerf) is only several tens micrometers or less, during transportation, dies may shift from their original locations and physically contact or crash into their neighboring dies. The resultant mechanical stresses may cause die cracking/breakage, especially for 50um or thinner dies and dies with narrow dicing kerfs. Therefore, safe handling and transportation of singulated dies before die pickup must be resolved.

[0026] In a related aspect, a hybrid wafer or substrate dicing process involving an initial laser scribe and subsequent plasma etch may be implemented for die singulation. The laser scribe process may be used to cleanly remove a mask layer, organic and inorganic dielectric layers, and device layers. The laser etch process may then be terminated upon exposure of, or partial etch of, the wafer or substrate. The plasma etch portion of the dicing process may then be employed to etch through the bulk of the wafer or substrate, such as through bulk single crystalline silicon, to yield die or chip singulation or dicing.

[0027] Conventional wafer dicing approaches include diamond saw cutting based on a purely mechanical separation, initial laser scribing and subsequent diamond saw dicing, or nanosecond or picosecond laser dicing. For thin wafer or substrate singulation, such as 50 microns thick bulk silicon singulation, the conventional approaches have yielded only poor

process quality. Some of the challenges that may be faced when singulating die from thin wafers or substrates may include microcrack formation or delamination between different layers, chipping of inorganic dielectric layers, retention of strict kerf width control, or precise ablation depth control. Embodiments of the present invention include a hybrid laser scribing and plasma etching die singulation approach that may be useful for overcoming one or more of the above challenges.

[0028] In accordance with an embodiment of the present invention, a combination of laser scribing, e.g., femtosecond-based laser scribing, and plasma etching is used to dice a semiconductor wafer into individualized or singulated integrated circuits. In one embodiment, femtosecond-based laser scribing is used as an essentially, if not totally, non-thermal process. For example, the femtosecond-based laser scribing may be localized with no or negligible heat damage zone. In an embodiment, approaches herein are used to singulated integrated circuits having ultra-low k films. With convention dicing, saws may need to be slowed down to accommodate such low k films. Furthermore, semiconductor wafers are now often thinned prior to dicing. As such, in an embodiment, a combination of mask patterning and partial wafer scribing with a femtosecond-based laser, followed by a plasma etch process, is now practical. In one embodiment, direct writing with laser can eliminate need for a lithography patterning operation of a photo-resist layer and can be implemented with very little cost. In one embodiment, through-via type silicon etching is used to complete the dicing process in a plasma etching environment.

[0029] Thus, in an aspect of the present invention, a combination of femtosecond-based laser scribing and plasma etching may be used to dice a semiconductor wafer into singulated integrated circuits. Figure 1 illustrates a top plan of a semiconductor wafer to be diced, in accordance with an embodiment of the present invention. Figure 2 illustrates a top plan of a semiconductor wafer to be diced that has a dicing mask formed thereon, in accordance with an embodiment of the present invention.

[0030] Referring to Figure 1, a semiconductor wafer 100 has a plurality of regions 102 that include integrated circuits. The regions 102 are separated by vertical streets 104 and horizontal streets 106. The streets 104 and 106 are areas of semiconductor wafer that do not contain integrated circuits and are designed as locations along which the wafer will be diced. Some embodiments of the present invention involve the use of a combination femtosecond-based laser scribe and plasma etch technique to cut trenches through the semiconductor wafer along the streets such that the dice are separated into individual chips or die. Since both a laser scribe and a plasma etch process are crystal structure orientation independent, the crystal structure of the semiconductor wafer to be diced may be immaterial to achieving a vertical trench through the

wafer.

[0031] Referring to Figure 2, the semiconductor wafer 100 has a mask 200 deposited upon the semiconductor wafer 100. In one embodiment, the mask is deposited in a conventional manner to achieve an approximately 4-10 micron thick layer. The mask 200 and a portion of the semiconductor wafer 100 are patterned with a laser scribing process to define the locations (e.g., gaps 202 and 204) along the streets 104 and 106 where the semiconductor wafer 100 will be diced. The integrated circuit regions of the semiconductor wafer 100 are covered and protected by the mask 200. The regions 206 of the mask 200 are positioned such that during a subsequent etching process, the integrated circuits are not degraded by the etch process. Horizontal gaps 204 and vertical gaps 202 are formed between the regions 206 to define the areas that will be etched during the etching process to finally dice the semiconductor wafer 100.

[0032] Figure 3 is a Flowchart 300 representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention. Figures 4A-4E illustrate cross-sectional views of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operations of Flowchart 300, in accordance with an embodiment of the present invention.

[0033] Referring to operation 302 of Flowchart 300, and corresponding Figure 4A, a mask 402 is formed above a semiconductor wafer or substrate 404. The mask 402 is composed of a layer covering and protecting integrated circuits 406 formed on the surface of semiconductor wafer 404. The mask 402 also covers intervening streets 407 formed between each of the integrated circuits 406. The semiconductor wafer or substrate 404 is disposed on dicing tape 498. The dicing tape 498 as shown may be a portion of a framed dicing tape, e.g., framed by a metal or plastic, or other material, ring.

[0034] In accordance with an embodiment of the present invention, forming the mask 402 includes forming a layer such as, but not limited to, a photo-resist layer or an I-line patterning layer. For example, a polymer layer such as a photo-resist layer may be composed of a material otherwise suitable for use in a lithographic process. In one embodiment, the photo-resist layer is composed of a positive photo-resist material such as, but not limited to, a 248 nanometer (nm) resist, a 193 nm resist, a 157 nm resist, an extreme ultra-violet (EUV) resist, or a phenolic resin matrix with a diazonaphthoquinone sensitizer. In another embodiment, the photo-resist layer is composed of a negative photo-resist material such as, but not limited to, poly-cis-isoprene and poly-vinyl-cinnamate. However, in other embodiments, non-photo-sensitive and/or less costly materials are used as the mask 402. In an embodiment, the mask is formed by uniformly spinning on a mask above a semiconductor wafer, the mask comprising layer covering

and protecting bumps or pillars of the integrated circuits.

[0035] In an embodiment, semiconductor wafer or substrate 404 is composed of a material suitable to withstand a fabrication process and upon which semiconductor processing layers may suitably be disposed. For example, in one embodiment, semiconductor wafer or substrate 404 is composed of a group IV-based material such as, but not limited to, crystalline silicon, germanium or silicon/germanium. In a specific embodiment, providing semiconductor wafer 404 includes providing a monocrystalline silicon substrate. In a particular embodiment, the monocrystalline silicon substrate is doped with impurity atoms. In another embodiment, semiconductor wafer or substrate 404 is composed of a III-V material such as, e.g., a III-V material substrate used in the fabrication of light emitting diodes (LEDs).

[0036] In an embodiment, semiconductor wafer or substrate 404 has disposed thereon or therein, as a portion of the integrated circuits 406, an array of semiconductor devices. Examples of such semiconductor devices include, but are not limited to, memory devices or complimentary metal-oxide-semiconductor (CMOS) transistors fabricated in a silicon substrate and encased in a dielectric layer. A plurality of metal interconnects may be formed above the devices or transistors, and in surrounding dielectric layers, and may be used to electrically couple the devices or transistors to form the integrated circuits 406. Materials making up the streets 407 may be similar to or the same as those materials used to form the integrated circuits 406. For example, streets 407 may be composed of layers of dielectric materials, semiconductor materials, and metallization. In one embodiment, one or more of the streets 407 includes test devices similar to the actual devices of the integrated circuits 406.

[0037] Referring to operation 304 of Flowchart 300, and corresponding Figure 4B, the mask 402 is patterned with a laser scribing process to provide a patterned mask 408 with gaps 410, exposing regions of the semiconductor wafer or substrate 404 between the integrated circuits 406. As such, the laser scribing process is used to remove the material of the streets 407 originally formed between the integrated circuits 406. In accordance with an embodiment of the present invention, patterning the mask 402 with the laser scribing process includes forming trenches 412 partially into the regions of the semiconductor wafer 404 between the integrated circuits 406, as depicted in Figure 4B.

[0038] In an embodiment, patterning the mask 406 with the laser scribing process includes using a laser having a pulse width in the femtosecond range. Specifically, a laser with a wavelength in the visible spectrum plus the ultra-violet (UV) and infra-red (IR) ranges (totaling a broadband optical spectrum) may be used to provide a femtosecond-based laser, i.e., a laser with a pulse width on the order of the femtosecond (10^{-15} seconds). In one embodiment, ablation is not, or is essentially not, wavelength dependent and is thus suitable for complex films such as

films of the mask 402, the streets 407 and, possibly, a portion of the semiconductor wafer or substrate 404.

[0039] Figure 5 illustrates the effects of using a laser pulse in the femtosecond range versus longer frequencies, in accordance with an embodiment of the present invention. Referring to Figure 5, by using a laser with a pulse width in the femtosecond range heat damage issues are mitigated or eliminated (e.g., minimal to no damage 502C with femtosecond processing of a via 500C) versus longer pulse widths (e.g., damage 502B with picosecond processing of a via 500B and significant damage 502A with nanosecond processing of a via 500A). The elimination or mitigation of damage during formation of via 500C may be due to a lack of low energy recoupling (as is seen for picosecond-based laser ablation) or thermal equilibrium (as is seen for nanosecond-based laser ablation), as depicted in Figure 5.

[0040] Laser parameters selection, such as pulse width, may be critical to developing a successful laser scribing and dicing process that minimizes chipping, microcracks and delamination in order to achieve clean laser scribe cuts. The cleaner the laser scribe cut, the smoother an etch process that may be performed for ultimate die singulation. In semiconductor device wafers, many functional layers of different material types (e.g., conductors, insulators, semiconductors) and thicknesses are typically disposed thereon. Such materials may include, but are not limited to, organic materials such as polymers, metals, or inorganic dielectrics such as silicon dioxide and silicon nitride.

[0041] A street between individual integrated circuits disposed on a wafer or substrate may include the similar or same layers as the integrated circuits themselves. For example, Figure 6 illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present invention.

[0042] Referring to Figure 6, a street region 600 includes the top portion 602 of a silicon substrate, a first silicon dioxide layer 604, a first etch stop layer 606, a first low K dielectric layer 608 (e.g., having a dielectric constant of less than the dielectric constant of 4.0 for silicon dioxide), a second etch stop layer 610, a second low K dielectric layer 612, a third etch stop layer 614, an undoped silica glass (USG) layer 616, a second silicon dioxide layer 618, and a layer of photo-resist 620, with relative thicknesses depicted. Copper metallization 622 is disposed between the first and third etch stop layers 606 and 614 and through the second etch stop layer 610. In a specific embodiment, the first, second and third etch stop layers 606, 610 and 614 are composed of silicon nitride, while low K dielectric layers 608 and 612 are composed of a carbon-doped silicon oxide material.

[0043] Under conventional laser irradiation (such as nanosecond-based or picosecond-based laser irradiation), the materials of street 600 behave quite differently in terms of optical

absorption and ablation mechanisms. For example, dielectrics layers such as silicon dioxide, is essentially transparent to all commercially available laser wavelengths under normal conditions. By contrast, metals, organics (e.g., low K materials) and silicon can couple photons very easily, particularly in response to nanosecond-based or picosecond-based laser irradiation. For example, Figure 7 includes a plot 700 of absorption coefficient as a function of photon energy for crystalline silicon (c-Si, 702), copper (Cu, 704), crystalline silicon dioxide (c-SiO₂, 706), and amorphous silicon dioxide (a-SiO₂, 708), in accordance with an embodiment of the present invention. Figure 8 is an equation 800 showing the relationship of laser intensity for a given laser as a function of laser pulse energy, laser pulse width, and laser beam radius.

[0044] Using equation 800 and the plot 700 of absorption coefficients, in an embodiment, parameters for a femtosecond laser-based process may be selected to have an essentially common ablation effect on the inorganic and organic dielectrics, metals, and semiconductors even though the general energy absorption characteristics of such materials may differ widely under certain conditions. For example, the absorptivity of silicon dioxide is non-linear and may be brought more in-line with that of organic dielectrics, semiconductors and metals under the appropriate laser ablation parameters. In one such embodiment, a high intensity and short pulse width femtosecond-based laser process is used to ablate a stack of layers including a silicon dioxide layer and one or more of an organic dielectric, a semiconductor, or a metal. In a specific embodiment, pulses of approximately less than or equal to 400 femtoseconds are used in a femtosecond-based laser irradiation process to remove a mask, a street, and a portion of a silicon substrate.

[0045] By contrast, if non-optimal laser parameters are selected, in stacked structures that involve two or more of an inorganic dielectric, an organic dielectric, a semiconductor, or a metal, a laser ablation process may cause delamination issues. For example, a laser penetrate through high bandgap energy dielectrics (such as silicon dioxide with an approximately of 9eV bandgap) without measurable absorption. However, the laser energy may be absorbed in an underlying metal or silicon layer, causing significant vaporization of the metal or silicon layers. The vaporization may generate high pressures to lift-off the overlying silicon dioxide dielectric layer and potentially causing severe interlayer delamination and microcracking. In an embodiment, while picoseconds-based laser irradiation processes lead to microcracking and delaminating in complex stacks, femtosecond-based laser irradiation processes have been demonstrated to not lead to microcracking or delamination of the same material stacks.

[0046] In order to be able to directly ablate dielectric layers, ionization of the dielectric materials may need to occur such that they behave similar to a conductive material by strongly absorbing photons. The absorption may block a majority of the laser energy from penetrating

through to underlying silicon or metal layers before ultimate ablation of the dielectric layer. In an embodiment, ionization of inorganic dielectrics is feasible when the laser intensity is sufficiently high to initiate photon-ionization and impact ionization in the inorganic dielectric materials.

[0047] In accordance with an embodiment of the present invention, suitable femtosecond-based laser processes are characterized by a high peak intensity (irradiance) that usually leads to nonlinear interactions in various materials. In one such embodiment, the femtosecond laser sources have a pulse width approximately in the range of 10 femtoseconds to 500 femtoseconds, although preferably in the range of 100 femtoseconds to 400 femtoseconds. In one embodiment, the femtosecond laser sources have a wavelength approximately in the range of 1570 nanometers to 200 nanometers, although preferably in the range of 540 nanometers to 250 nanometers. In one embodiment, the laser and corresponding optical system provide a focal spot at the work surface approximately in the range of 3 microns to 15 microns, though preferably approximately in the range of 5 microns to 10 microns.

[0048] The spacial beam profile at the work surface may be a single mode (Gaussian) or have a shaped top-hat profile. In an embodiment, the laser source has a pulse repetition rate approximately in the range of 200 kHz to 10 MHz, although preferably approximately in the range of 500kHz to 5MHz. In an embodiment, the laser source delivers pulse energy at the work surface approximately in the range of 0.5 uJ to 100 uJ, although preferably approximately in the range of 1uJ to 5uJ. In an embodiment, the laser scribing process runs along a work piece surface at a speed approximately in the range of 500mm/sec to 5m/sec, although preferably approximately in the range of 600mm/sec to 2m/sec.

[0049] The scribing process may be run in single pass only, or in multiple passes, but, in an embodiment, preferably 1-2 passes. In one embodiment, the scribing depth in the work piece is approximately in the range of 5 microns to 50 microns deep, preferably approximately in the range of 10 microns to 20 microns deep. The laser may be applied either in a train of single pulses at a given pulse repetition rate or a train of pulse bursts. In an embodiment, the kerf width of the laser beam generated is approximately in the range of 2 microns to 15 microns, although in silicon wafer scribing/dicing preferably approximately in the range of 6 microns to 10 microns, measured at the device/silicon interface.

[0050] Laser parameters may be selected with benefits and advantages such as providing sufficiently high laser intensity to achieve ionization of inorganic dielectrics (e.g., silicon dioxide) and to minimize delamination and chipping caused by underlayer damage prior to direct ablation of inorganic dielectrics. Also, parameters may be selected to provide meaningful process throughput for industrial applications with precisely controlled ablation width (e.g., kerf

width) and depth. As described above, a femtosecond-based laser is far more suitable to providing such advantages, as compared with picosecond-based and nanosecond-based laser ablation processes. However, even in the spectrum of femtosecond-based laser ablation, certain wavelengths may provide better performance than others. For example, in one embodiment, a femtosecond-based laser process having a wavelength closer to or in the UV range provides a cleaner ablation process than a femtosecond-based laser process having a wavelength closer to or in the IR range. In a specific such embodiment, a femtosecond-based laser process suitable for semiconductor wafer or substrate scribing is based on a laser having a wavelength of approximately less than or equal to 540 nanometers. In a particular such embodiment, pulses of approximately less than or equal to 400 femtoseconds of the laser having the wavelength of approximately less than or equal to 540 nanometers are used. However, in an alternative embodiment, dual laser wavelengths (e.g., a combination of an IR laser and a UV laser) are used.

[0051] Referring to operation 306 of Flowchart 300, and corresponding Figure 4C, the semiconductor wafer 404 is etched through the gaps 410 in the patterned mask 408 to singulate the integrated circuits 406. In accordance with an embodiment of the present invention, etching the semiconductor wafer 404 includes etching the trenches 412 formed with the femtosecond-based laser scribing process to ultimately etch entirely through semiconductor wafer 404, as depicted in Figure 4C. In one such embodiment, the etching exposes portions of the dicing tape 498, as depicted in Figure 4C.

[0052] In an embodiment, etching the semiconductor wafer 404 includes using a plasma etching process. In one embodiment, a through-silicon via type etch process is used. For example, in a specific embodiment, the etch rate of the material of semiconductor wafer 404 is greater than 25 microns per minute. An ultra-high-density plasma source may be used for the plasma etching portion of the die singulation process. An example of a process chamber suitable to perform such a plasma etch process is the Applied Centura® Silvia™ Etch system available from Applied Materials of Sunnyvale, CA, USA. The Applied Centura® Silvia™ Etch system combines the capacitive and inductive RF coupling, which gives much more independent control of the ion density and ion energy than was possible with the capacitive coupling only, even with the improvements provided by magnetic enhancement. This combination enables effective decoupling of the ion density from ion energy, so as to achieve relatively high density plasmas without the high, potentially damaging, DC bias levels, even at very low pressures. This results in an exceptionally wide process window. However, any plasma etch chamber capable of etching silicon may be used. In an exemplary embodiment, a deep silicon etch is used to etch a single crystalline silicon substrate or wafer 404 at an etch rate greater than approximately 40% of conventional silicon etch rates while maintaining essentially precise profile control and virtually

scallop-free sidewalls. In a specific embodiment, a through-silicon via type etch process is used. The etch process is based on a plasma generated from a reactive gas, which generally a fluorine-based gas such as SF₆, C₄ F₈, CHF₃, XeF₂, or any other reactant gas capable of etching silicon at a relatively fast etch rate. In an embodiment, the mask layer 408 is removed after the singulation process, as depicted in Figure 4C. Furthermore, in an embodiment, the etching process and/or mask removal has little to no impact on the dicing tape 498, as depicted in Figure 4C.

[0053] Upon completely etching through semiconductor wafer 404, the singulated die may need to be transported as a plurality of die, e.g., as remaining on dicing tape 498. Referring to Figure 4D and corresponding operation 308 of Flowchart 300, after dicing, dies are singulated to each other but stay on the dicing tape. Since the die-to-die spacing (the dicing kerf) may be only several tens micrometers or less, during transportation, dies may shift from their original locations as to physically contact and/or crash into their neighboring dies. The resultant mechanical stresses may cause die cracking/breakage, especially for 50um or thinner dies and dies with narrow dicing kerfs. Thus, in an embodiment, as depicted in Figure 4D, a water soluble material layer 499 is formed over and between the singulated dies (shown as 406/404 pairings).

[0054] In one embodiment, the suitable water soluble material layer 499 is readily dissolvable in an aqueous media. For example, in one embodiment, the water-soluble material layer 499 is composed of a material that is soluble in one or more of an alkaline solution, an acidic solution, or in deionized water. In one embodiment, the water-soluble material layer 499 is composed of a material such as, but not limited to, polyvinyl alcohol, polyacrylic acid, dextran, polymethacrylic acid, polyethylene imine, or polyethylene oxide. In a specific embodiment, the water-soluble material layer 499 has an etch rate in an aqueous solution approximately in the range of 1 – 15 microns per minute and, more particularly, approximately 1.3 microns per minute. In another specific embodiment, the water-soluble material layer 499 is formed by a spin-on technique.

[0055] Referring to Figure 4E, upon delivery to a desired location, the water-soluble material layer 499 is removed. In one such embodiment, removal is achieved by dissolving the water-soluble material layer 499 in one or more of an alkaline solution, an acidic solution, or in deionized water. Furthermore, the singulated die (shown as 406/404 pairings) can be removed from the dicing tape 498. In another embodiment, the masking layer 406 is a water-soluble layer and is not removed from the singulated dies until the time of the water-soluble material layer 499 removal process.

[0056] Thus, in general, one or more embodiments of the present invention include a wafer handling process first involving, subsequent to wafer dicing, the singulated dies remain on

the dicing tape. A water soluble mask layer is formed on and over the singulated dies to ensure the water soluble material essentially fills into the die-to-die spacing area. In one embodiment, the water soluble layer is spin coated on, but can also be sprayed on. To ensure sufficient filling of mask into the gap between dies, a relatively low viscosity water soluble material may be used. The spin coating may be performed at relatively low speed to avoid die breakage. In one embodiment, after spin coating, the wafer is gently baked at low temperature (e.g., up to 50C) to solidify the mask material. The process next involves transporting the singulated dies transported to a different location. Once the singulated wafer is delivered to the destination, the water soluble mask is removed from the dies by an aqueous treatment subsequent drying treatment. The cleaned and dried singulated dies are ready to be picked for further assembly and/or testing. In an embodiment, an advantage includes filling water soluble material in the spacing between dies as cushion to ensure safe transportation of singulated wafers.

[0057] Accordingly, referring again to Flowchart 300 and Figures 4A-4E, wafer dicing may be performed by initial laser ablation through a mask layer, through wafer streets (including metallization), and partially into a silicon substrate. The laser pulse width may be selected in the femtosecond range. Die singulation may then be completed by subsequent through-silicon deep plasma etching. A water soluble material layer may then be disposed over the resulting singulated dies for safe handling and transportation of the singulated dies. A specific example of a materials stack for dicing is described below in association with Figures 9A-9D, in accordance with an embodiment of the present invention.

[0058] Referring to Figure 9A, a materials stack for hybrid laser ablation and plasma etch dicing includes a mask layer 902, a device layer 904, and a substrate 906. The mask layer, device layer, and substrate are disposed above a die attach film 908 which is affixed to an underlying dicing or backing tape 910. In an embodiment, the mask layer 902 is a photo-resist layer such as the photo-resist layers described above in association with mask 402. In another embodiment, the mask 402 is a water-soluble mask. The device layer 904 includes an inorganic dielectric layer (such as silicon dioxide) disposed above one or more metal layers (such as copper layers) and one or more low K dielectric layers (such as carbon-doped oxide layers). The device layer 904 also includes streets arranged between integrated circuits, the streets including the same or similar layers to the integrated circuits. The substrate 906 is a bulk single-crystalline silicon substrate.

[0059] In an embodiment, the bulk single-crystalline silicon substrate 906 is thinned from the backside prior to being affixed to the die attach film 908. The thinning may be performed by a backside grind process. In one embodiment, the bulk single-crystalline silicon substrate 906 is thinned to a thickness approximately in the range of 50 – 100 microns. It is important to note

that, in an embodiment, the thinning is performed prior to a laser ablation and plasma etch dicing process. In an embodiment, the photo-resist layer 902 has a thickness of approximately 5 microns and the device layer 904 has a thickness approximately in the range of 2 – 3 microns. In an embodiment, the die attach film 908 (or any suitable substitute capable of bonding a thinned or thin wafer or substrate to the backing tape 910) has a thickness of approximately 20 microns.

[0060] Referring to Figure 9B, the mask 902, the device layer 904 and a portion of the substrate 906 are patterned with a femtosecond-based laser scribing process 912 to form trenches 914 in the substrate 906. Referring to Figure 9C, a through-silicon deep plasma etch process 916 is used to extend the trench 914 down to the die attach film 908, exposing the top portion of the die attach film 908 and singulating the silicon substrate 906. The device layer 904 is protected by the photo-resist layer 902 during the through-silicon deep plasma etch process 916.

[0061] Referring to Figure 9D, the singulation process may further include patterning the die attach film 908, exposing the top portion of the backing tape 910 and singulating the die attach film 908. In an embodiment, the die attach film is singulated by a laser process or by an etch process. Whether or not the die attach film is patterned, in an embodiment, the singulated dies are covered with a water soluble material layer 999, as depicted in Figure 9D. The water soluble material layer 999 may be used to protect the dies during transportation. Further embodiments may include subsequently dissolving the water soluble material layer 999 in an aqueous medium and then removing the singulated portions of substrate 906 (e.g., as individual integrated circuits) from the backing tape 910. In one embodiment, a singulated die attach film 908 is retained on the back sides of the singulated portions of substrate 906. Other embodiments may include removing the masking layer 902 from the device layer 904. In an alternative embodiment, in the case that substrate 906 is thinner than approximately 50 microns, the laser ablation process 912 is used to completely singulate substrate 906 without the use of an additional plasma process.

[0062] Referring again to Figures 4A-4E, the plurality of integrated circuits 406 may be separated by streets 407 having a width of approximately 10 microns or smaller. The use of a femtosecond-based laser scribing approach, at least in part due to the tight profile control of the laser, may enable such compaction in a layout of integrated circuits. For example, Figure 10 illustrates compaction on a semiconductor wafer or substrate achieved by using narrower streets versus conventional dicing which may be limited to a minimum width, in accordance with an embodiment of the present invention.

[0063] Referring to Figure 10, compaction on a semiconductor wafer is achieved by using narrower streets (e.g., widths of approximately 10 microns or smaller in layout 1002) versus conventional dicing which may be limited to a minimum width (e.g., widths of

approximately 70 microns or larger in layout 1000). It is to be understood, however, that it may not always be desirable to reduce the street width to less than 10 microns even if otherwise enabled by a femtosecond-based laser scribing process. For example, some applications may require a street width of at least 40 microns in order to fabricate dummy or test devices in the streets separating the integrated circuits.

[0064] Referring again to Figures 4A-4E, the plurality of integrated circuits 406 may be arranged on semiconductor wafer or substrate 404 in a non-restricted layout. For example, Figure 11 illustrates freeform integrated circuit arrangement allowing denser packing. The denser packing may provide for more die per wafer versus grid alignment approaches, in accordance with an embodiment of the present invention. Referring to Figure 11, a freeform layout (e.g., a non-restricted layout on semiconductor wafer or substrate 1102) allows denser packing and hence more die per wafer versus grid alignment approaches (e.g., a restricted layout on semiconductor wafer or substrate 1100). In an embodiment, the speed of the laser ablation and plasma etch singulation process is independent of die size, layout or the number of streets.

[0065] A single process tool may be configured to perform many or all of the operations in a hybrid laser ablation and plasma etch singulation process. For example, Figure 12 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present invention.

[0066] Referring to Figure 12, a process tool 1200 includes a factory interface 1202 (FI) having a plurality of load locks 1204 coupled therewith. A cluster tool 1206 is coupled with the factory interface 1202. The cluster tool 1206 includes one or more plasma etch chambers, such as plasma etch chamber 1208. A laser scribe apparatus 1210 is also coupled to the factory interface 1202. The overall footprint of the process tool 1200 may be, in one embodiment, approximately 3500 millimeters (3.5 meters) by approximately 3800 millimeters (3.8 meters), as depicted in Figure 12.

[0067] In an embodiment, the laser scribe apparatus 1210 houses a femtosecond-based laser. The femtosecond-based laser is suitable for performing a laser ablation portion of a hybrid laser and etch singulation process, such as the laser ablation processes described above. In one embodiment, a moveable stage is also included in laser scribe apparatus 1200, the moveable stage configured for moving a wafer or substrate (or a carrier thereof) relative to the femtosecond-based laser. In a specific embodiment, the femtosecond-based laser is also moveable. The overall footprint of the laser scribe apparatus 1210 may be, in one embodiment, approximately 2240 millimeters by approximately 1270 millimeters, as depicted in Figure 12.

[0068] In an embodiment, the one or more plasma etch chambers 1208 is configured for etching a wafer or substrate through the gaps in a patterned mask to singulate a plurality of

integrated circuits. In one such embodiment, the one or more plasma etch chambers 1208 is configured to perform a deep silicon etch process. In a specific embodiment, the one or more plasma etch chambers 1208 is an Applied Centura® Silvia™ Etch system, available from Applied Materials of Sunnyvale, CA, USA. The etch chamber may be specifically designed for a deep silicon etch used to create singulate integrated circuits housed on or in single crystalline silicon substrates or wafers. In an embodiment, a high-density plasma source is included in the plasma etch chamber 1208 to facilitate high silicon etch rates. In an embodiment, more than one etch chamber is included in the cluster tool 1206 portion of process tool 1200 to enable high manufacturing throughput of the singulation or dicing process.

[0069] The factory interface 1202 may be a suitable atmospheric port to interface between an outside manufacturing facility with laser scribe apparatus 1210 and cluster tool 1206. The factory interface 1202 may include robots with arms or blades for transferring wafers (or carriers thereof) from storage units (such as front opening unified pods) into either cluster tool 1206 or laser scribe apparatus 1210, or both.

[0070] Cluster tool 1206 may include other chambers suitable for performing functions in a method of singulation. For example, in one embodiment, in place of an additional etch chamber, a deposition chamber 1212 is included. The deposition chamber 1212 may be configured for water soluble material deposition, e.g., by spin coating, on and in between each of a plurality of singulated dies subsequent to dicing. In another embodiment, in place of an additional etch chamber, a wet/dry station 1214 is included. The wet/dry station may be suitable for cleaning residues and fragments, or for removing a mask, subsequent to a laser scribe and plasma etch singulation process of a substrate or wafer. In an embodiment, a metrology station is also included as a component of process tool 1200.

[0071] Embodiments of the present invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present invention. In one embodiment, the computer system is coupled with process tool 1200 described in association with Figure 12. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory (“ROM”), random access memory (“RAM”), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

[0072] Figure 13 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 1300 within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein, may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term “machine” shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

[0073] The exemplary computer system 1300 includes a processor 1302, a main memory 1304 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 1306 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 1318 (e.g., a data storage device), which communicate with each other via a bus 1330.

[0074] Processor 1302 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 1302 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 1302 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 1302 is configured to execute the processing logic 1326 for performing the operations described herein.

[0075] The computer system 1300 may further include a network interface device 1308. The computer system 1300 also may include a video display unit 1310 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 1312 (e.g., a keyboard), a cursor control device 1314 (e.g., a mouse), and a signal generation device 1316 (e.g., a speaker).

[0076] The secondary memory 1318 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 1331 on which is stored one or more

sets of instructions (e.g., software 1322) embodying any one or more of the methodologies or functions described herein. The software 1322 may also reside, completely or at least partially, within the main memory 1304 and/or within the processor 1302 during execution thereof by the computer system 1300, the main memory 1304 and the processor 1302 also constituting machine-readable storage media. The software 1322 may further be transmitted or received over a network 1320 via the network interface device 1308.

[0077] While the machine-accessible storage medium 1331 is shown in an exemplary embodiment to be a single medium, the term “machine-readable storage medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term “machine-readable storage medium” shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term “machine-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

[0078] In accordance with an embodiment of the present invention, a machine-accessible storage medium has instructions stored thereon which cause a data processing system to perform a method of dicing a semiconductor wafer having a plurality of integrated circuits. The method involves dicing a wafer into a plurality of singulated dies disposed above a dicing tape. The method also involves forming a water soluble material layer over and between the plurality of singulated dies, above the dicing tape.

[0079] Thus, methods of dicing semiconductor wafers, and transporting singulated die, have been disclosed.

CLAIMS

What is claimed is:

1. A method of dicing a wafer having a plurality of integrated circuits thereon, the method comprising:
 - dicing the wafer into a plurality of singulated dies disposed above a dicing tape; and
 - forming a water soluble material layer over and between the plurality of singulated dies, above the dicing tape.
2. The method of claim 1, further comprising:
 - transporting the dicing tape, wherein the water soluble material layer protects the singulated dies from damage during the transporting.
3. The method of claim 2, further comprising:
 - subsequent to the transporting, removing the water soluble material layer with an aqueous medium.
4. The method of claim 2, further comprising:
 - baking the water soluble material layer prior to the transporting.
5. The method of claim 1, wherein forming the water soluble material layer comprises forming a material selected from the group consisting of polyvinyl alcohol, polyacrylic acid, dextran, polymethacrylic acid, polyethylene imine, and polyethylene oxide.
6. The method of claim 5, wherein the water soluble material layer has an etch rate in an aqueous solution approximately in the range of 1 – 15 microns per minute.
7. The method of claim 1, wherein the forming the water soluble material layer comprises spin-coating the water soluble material layer.
8. The method of claim 1, wherein dicing the wafer into the plurality of singulated dies comprises using a laser ablation process.
9. The method of claim 1, wherein dicing the wafer into the plurality of singulated dies comprises using a laser scribing plus plasma etching hybrid dicing process.

10. The method of claim 1, wherein a water soluble mask is disposed on the wafer during the dicing of the wafer into the plurality of singulated dies, and wherein the water soluble mask is removed during the removing of the water soluble material layer.
11. The method of claim 1, wherein the dicing tape is housed in a frame.
12. An apparatus, comprising:
 - a plurality of singulated dies disposed above a dicing tape;
 - a water soluble material layer disposed over and between the plurality of singulated die, above the dicing tape.
13. The apparatus of claim 12, wherein the water soluble material layer comprises forming a material selected from the group consisting of polyvinyl alcohol, polyacrylic acid, dextran, polymethacrylic acid, polyethylene imine, and polyethylene oxide.
14. The apparatus of claim 12, further comprising:
 - a water soluble mask disposed on each of the plurality of singulated dies, between each of the plurality of singulated dies and the water soluble material layer.
15. The apparatus of claim 12, wherein the dicing tape is housed in a frame.

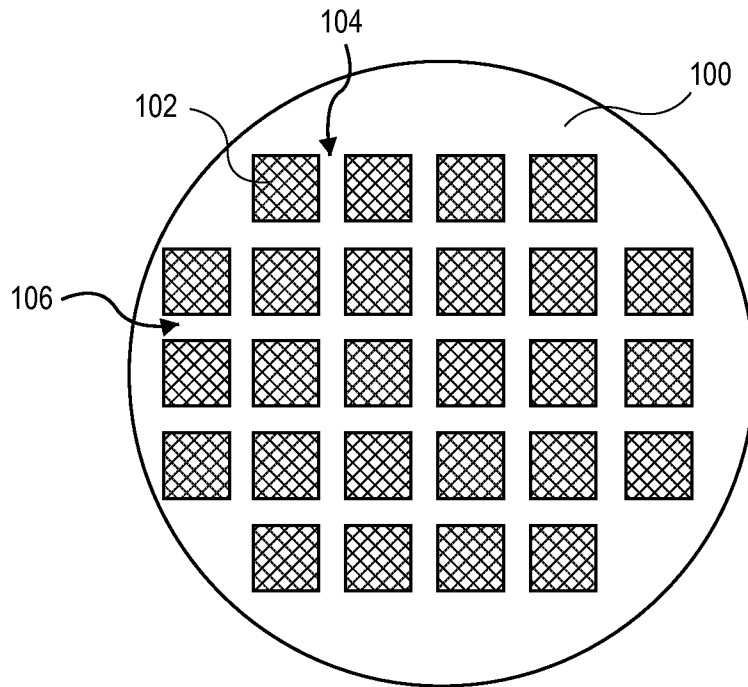


FIG. 1

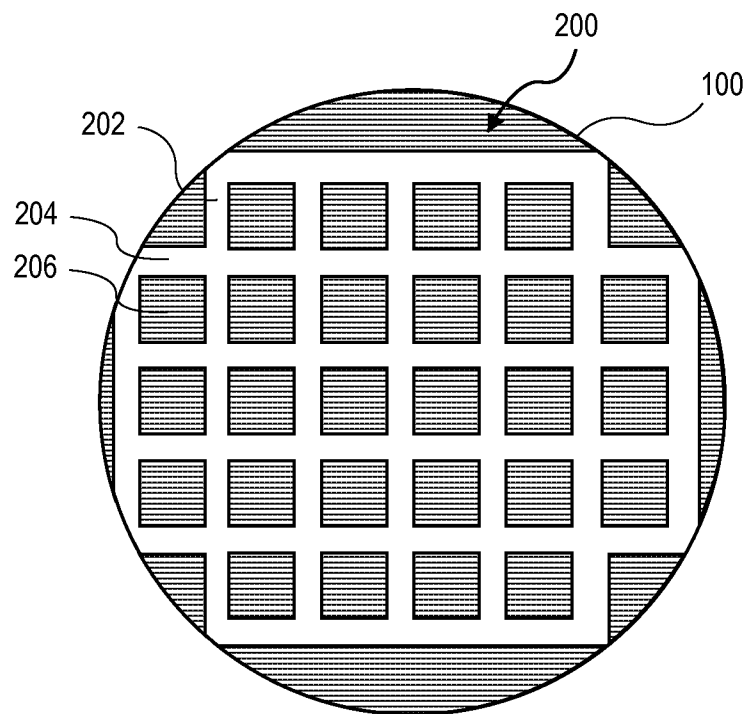
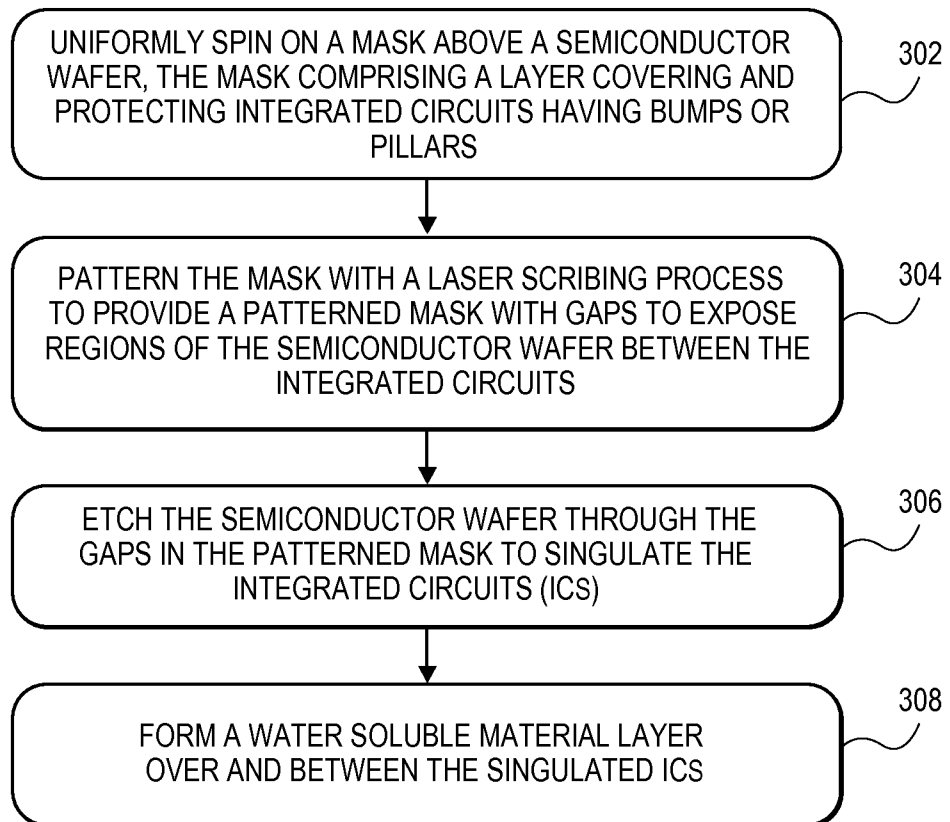


FIG. 2

FLOWCHART 300

**FIG. 3**

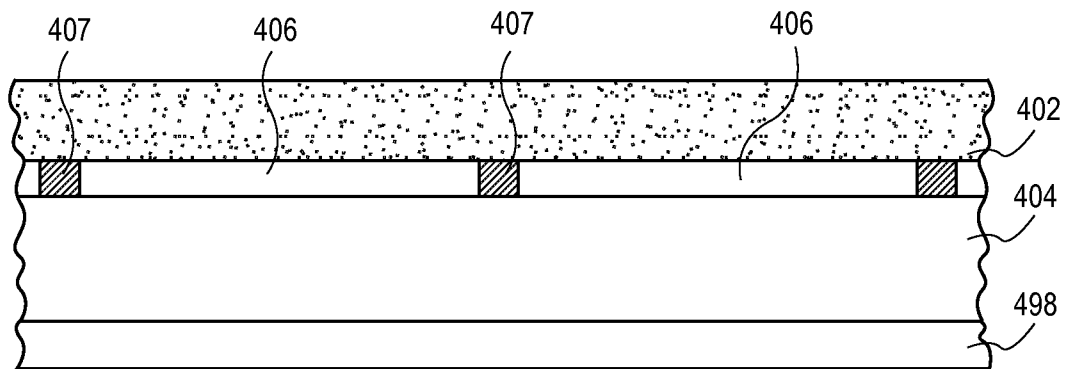


FIG. 4A

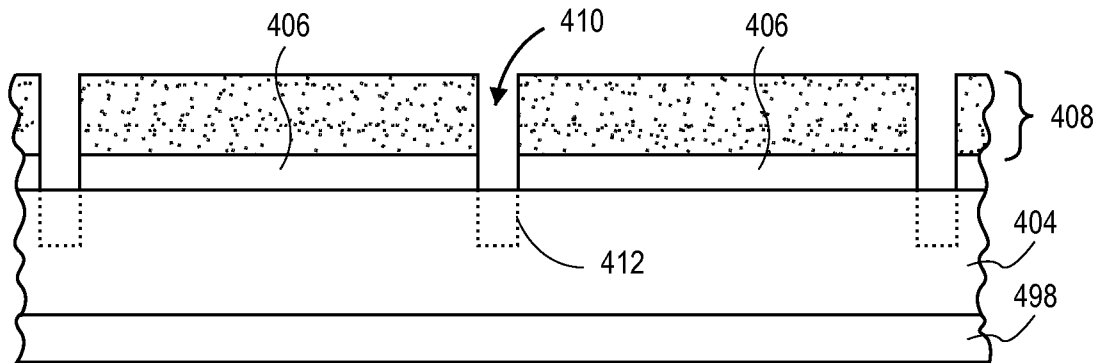


FIG. 4B

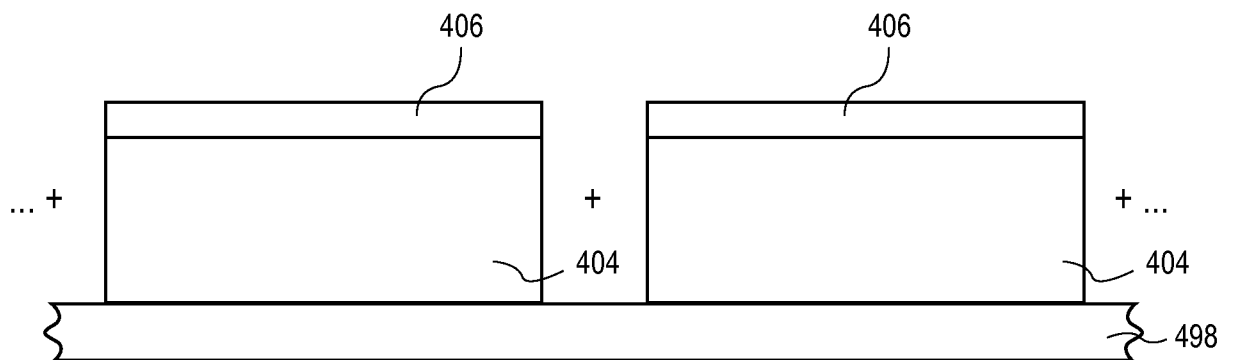


FIG. 4C

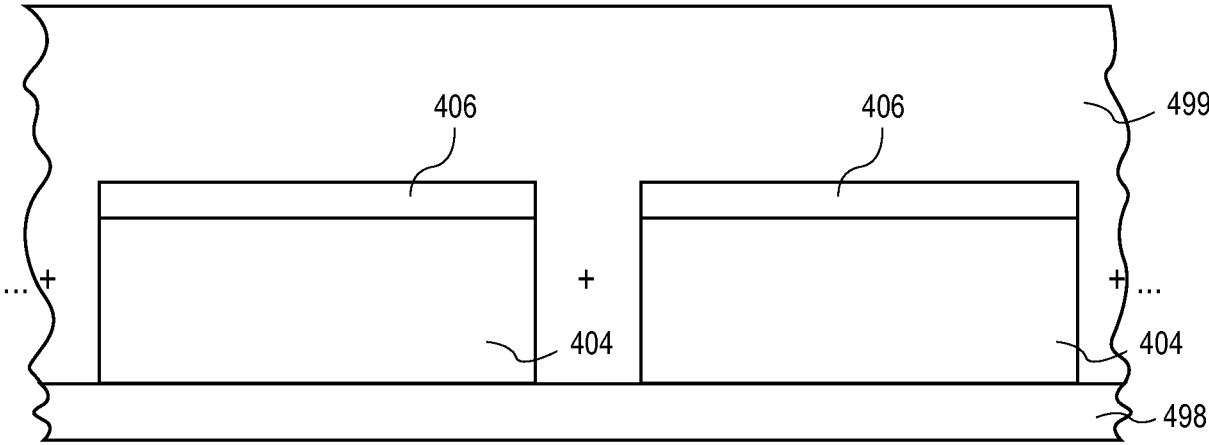


FIG. 4D

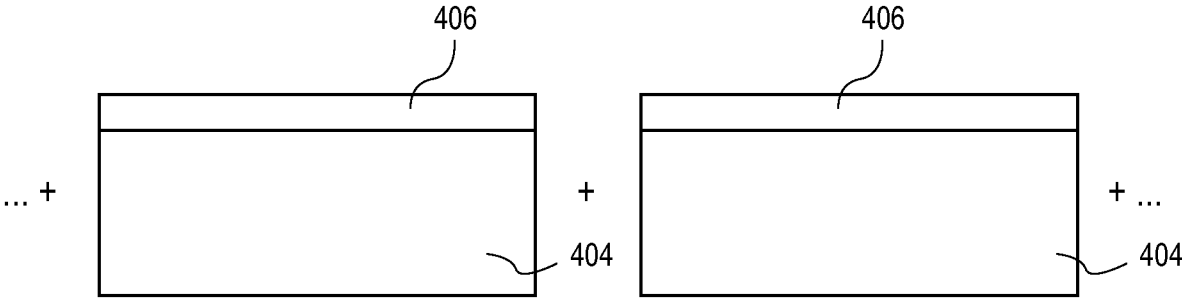


FIG. 4E

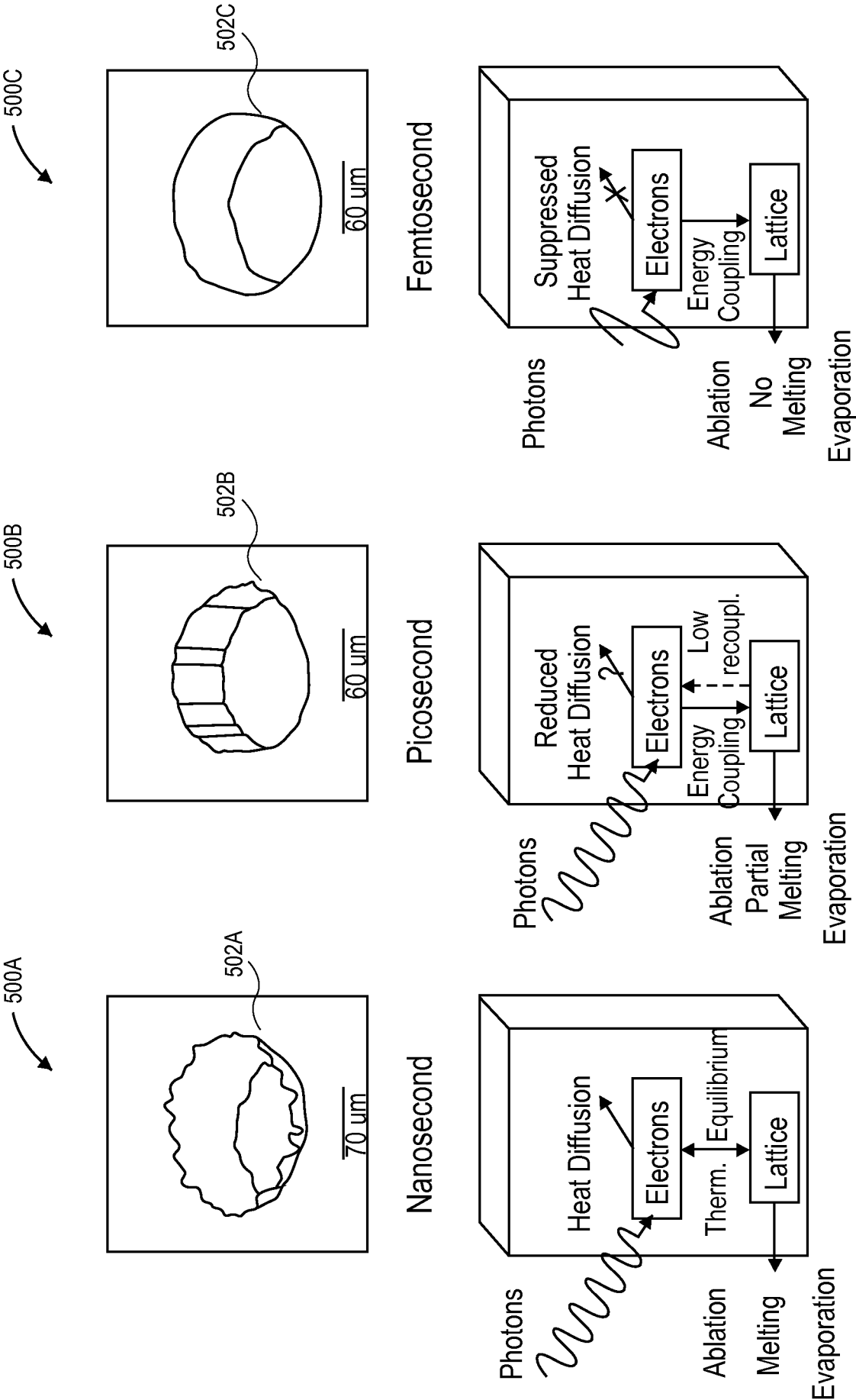


FIG. 5

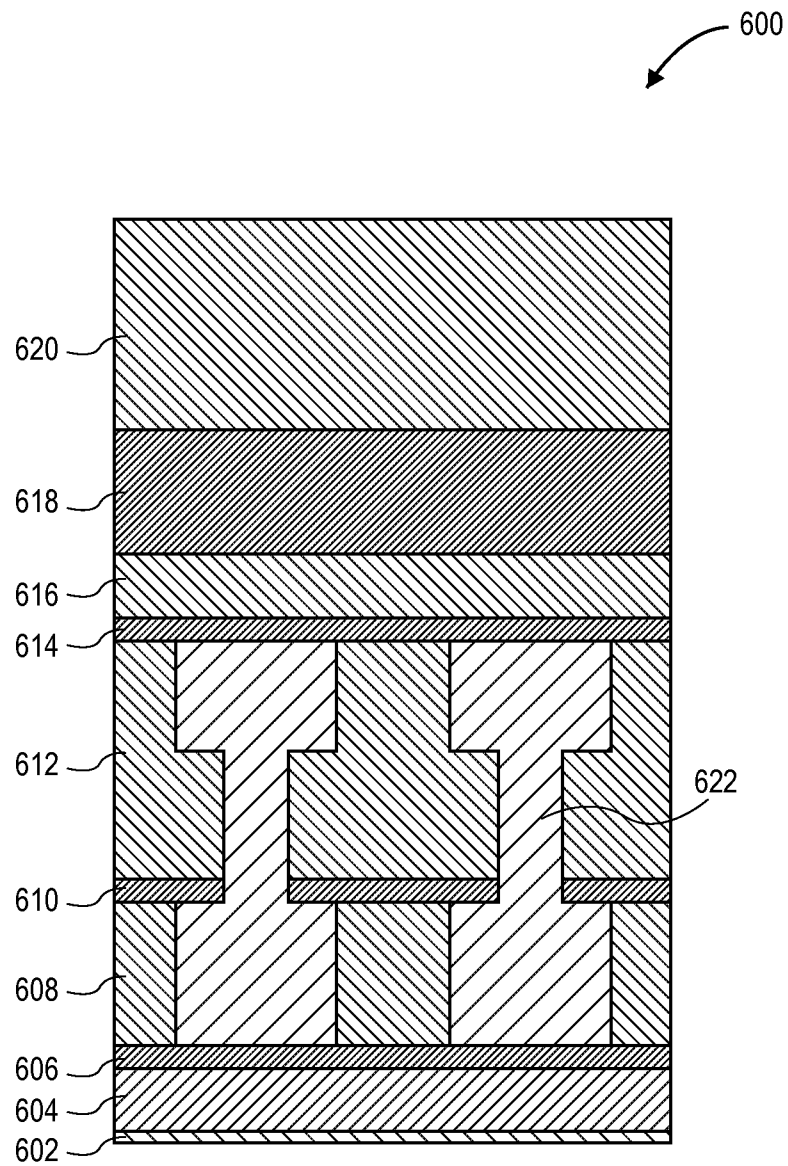
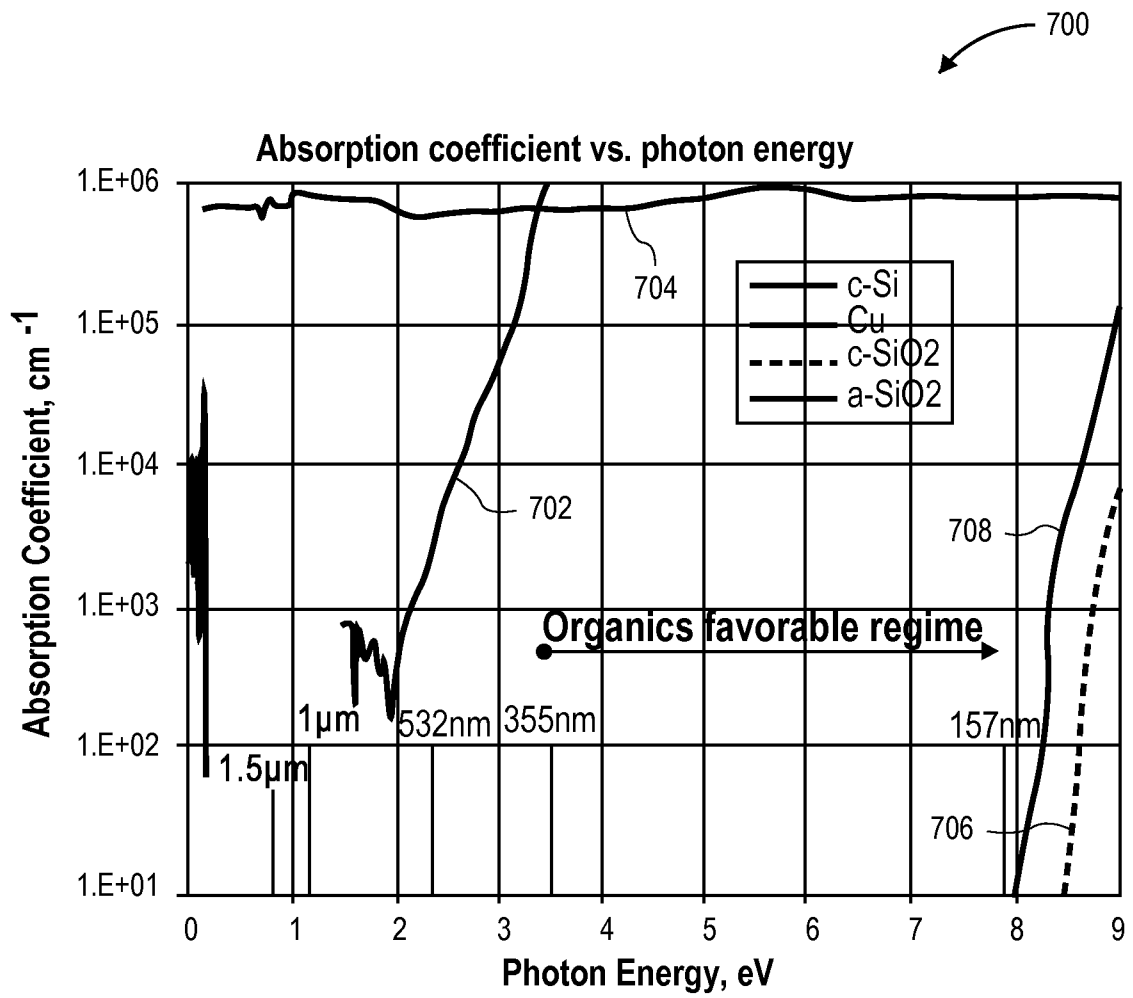


FIG. 6



$$I = \frac{\text{Pulse Energy } E_p}{\pi \cdot w_0^2 \cdot \tau}$$

Intensity

Beam Radius

Pulse Width

FIG. 8

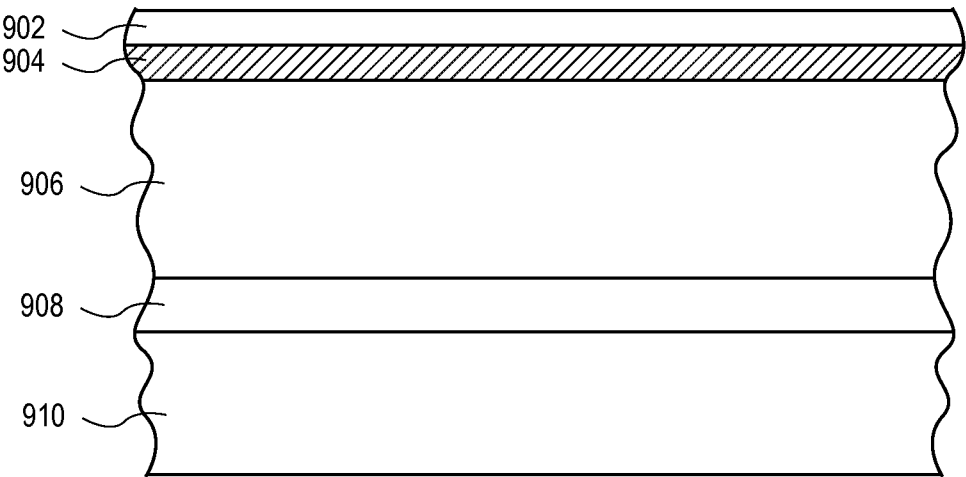


FIG. 9A

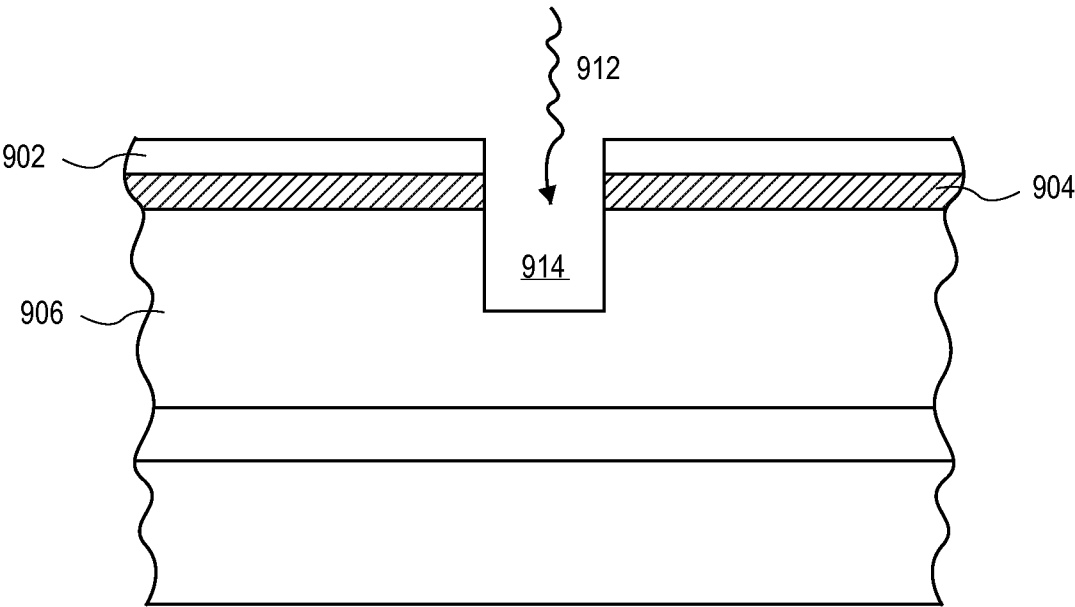


FIG. 9B

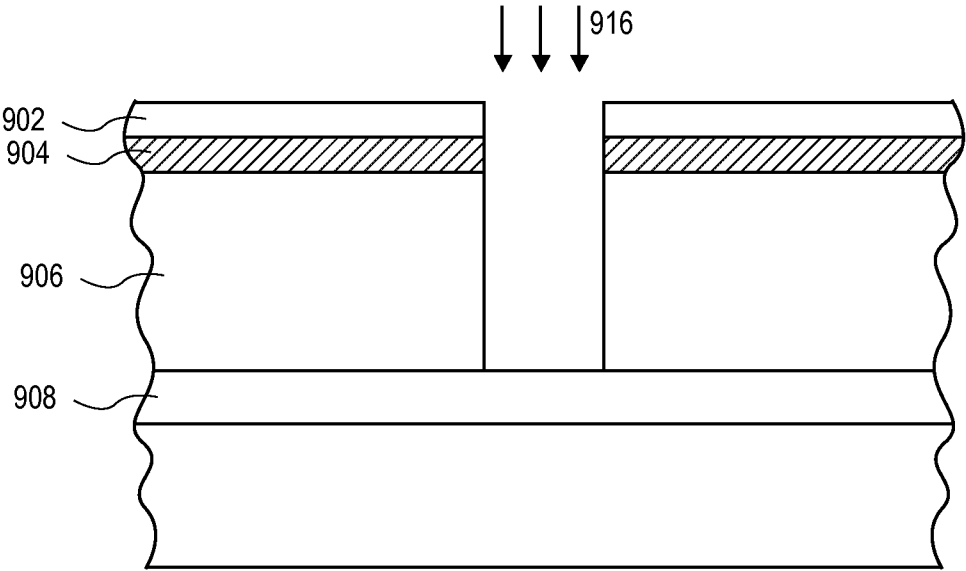


FIG. 9C

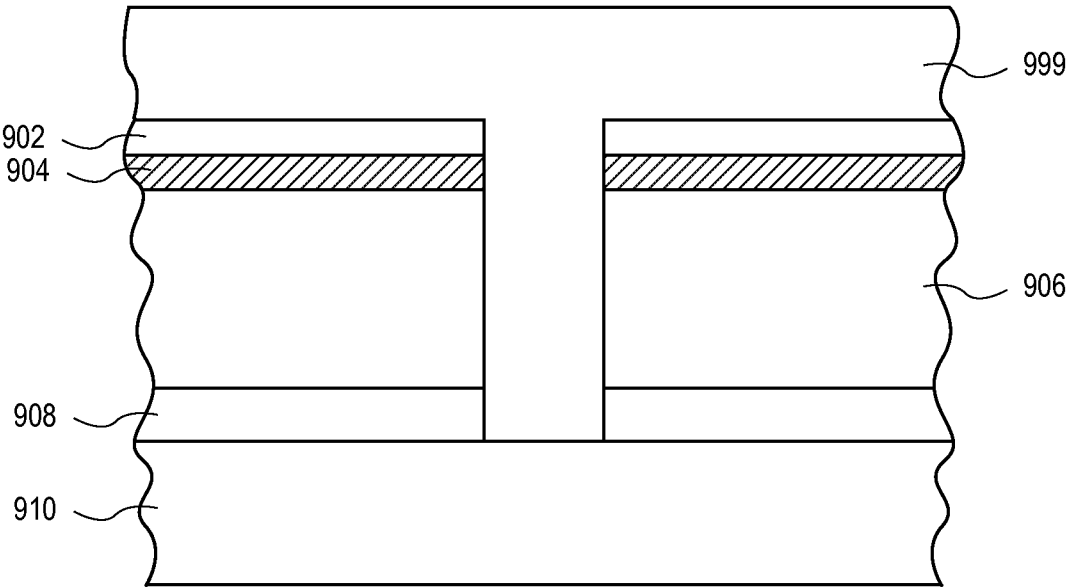


FIG. 9D

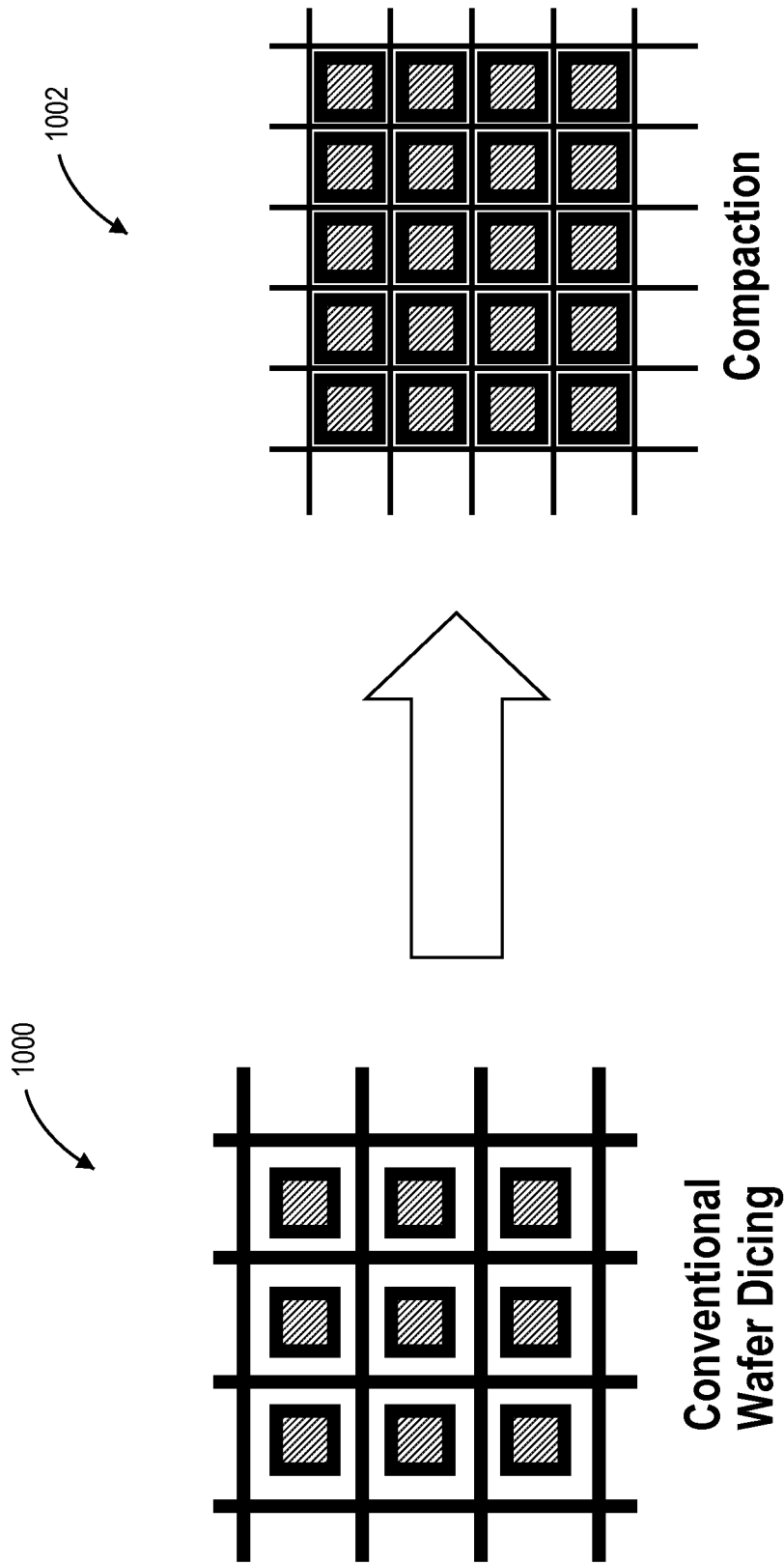


FIG. 10

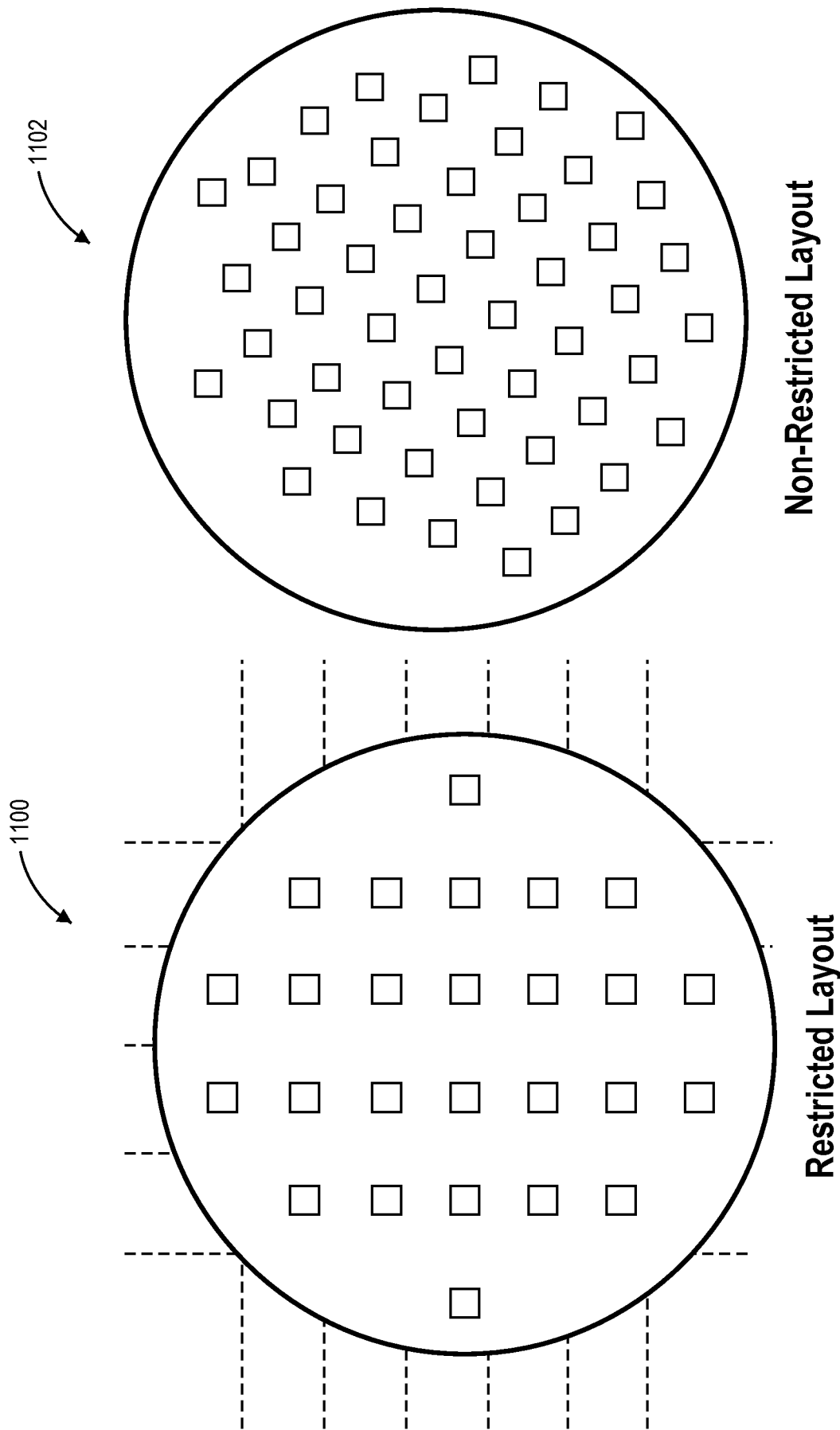


FIG. 11

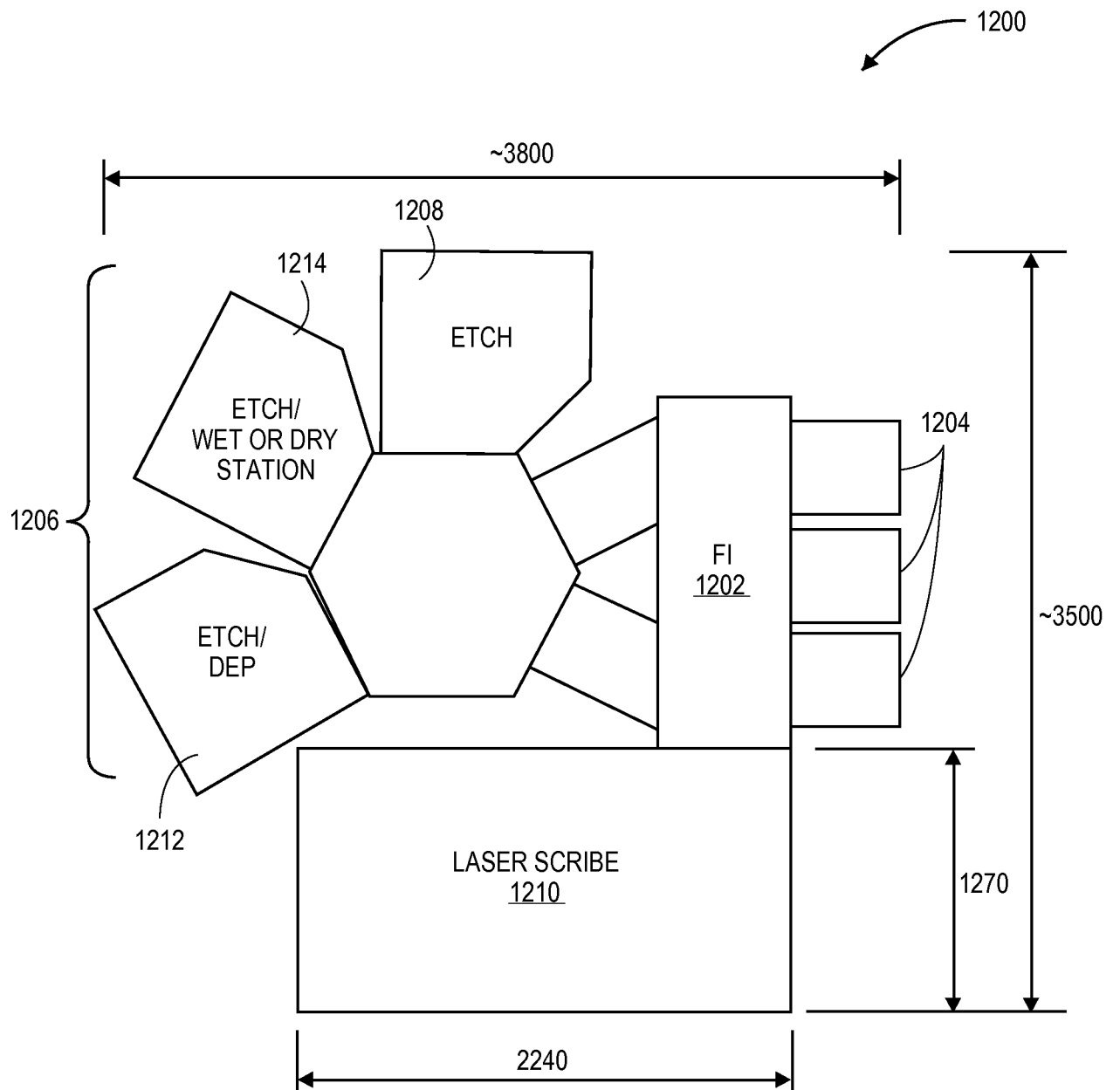
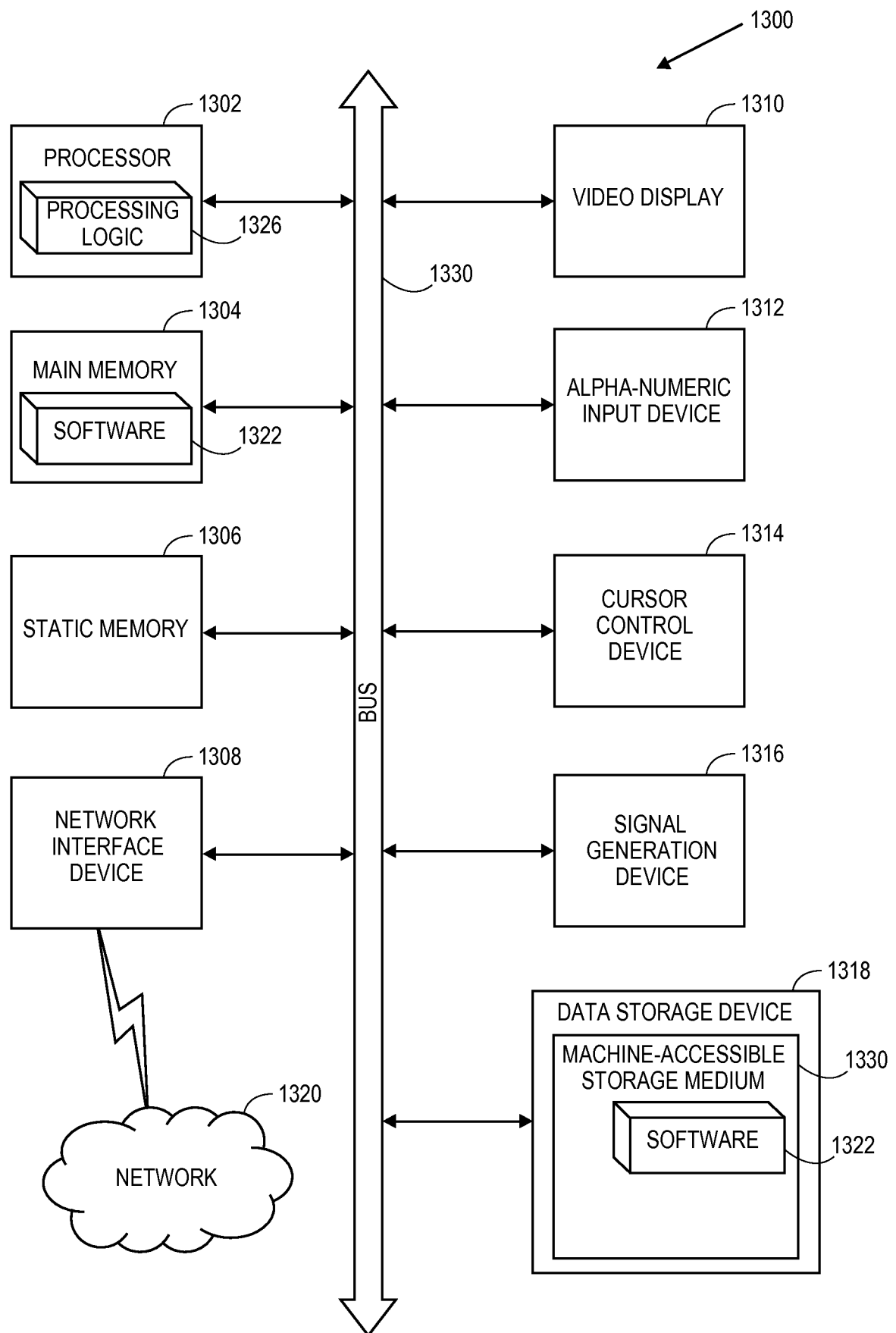


FIG. 12

**FIG. 13**

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/301(2006.01)i, H01L 21/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/301; H01L 21/027; H01L 21/304; G03F 7/40; H01L 21/78; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:dicing, water-soluble, laser scribing, etching, wafer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0040510 A1 (HOSEUNG YOO) 16 February 2012 See abstract, paragraphs [0009]-[0012] and claim 1.	1-15
A	KR 10-2010-0027120 A (AZ ELECTRONIC MATERIALS (JAPAN) KK) 10 March 2010 See abstract, paragraphs [0017]-[0018] and figure 1.	1-15
A	JP 2007-281526 A (MATSUSHITA ELECTRIC IND CO., LTD.) 25 October 2007 See abstract, paragraphs [0018]-[0031] and figures 1-2.	1-15
A	US 2004-0137700 A1 (KAZUMA SEKIYA) 15 July 2004 See abstract, paragraphs [0032]-[0051] and figures 1A-10.	1-15
A	US 2006-0205182 A1 (KOJI SOEJIMA) 14 September 2006 See paragraphs [0093]-[0109], claim 1 and figures 7A-11.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 August 2013 (27.08.2013)

Date of mailing of the international search report

28 August 2013 (28.08.2013)

Name and mailing address of the ISA/KR

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CHOI Sang Won

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/046898

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0040510 A1	16/02/2012	JP 2012-525010 A KR 10-2012-0007524 A TW 201104736 A WO 2010-124179 A2 WO 2010-124179 A3	18/10/2012 20/01/2012 01/02/2011 28/10/2010 20/01/2011
KR 10-2010-0027120 A	10/03/2010	CN 101675390 A CN 101675390 B EP 2146250 A1 EP 2146250 A8 JP 2008-275995 A JP 5069494 B2 TW 200916523 A US 2010-0119717 A1 WO 2008-136499 A1	17/03/2010 18/07/2012 20/01/2010 03/03/2010 13/11/2008 07/11/2012 16/04/2009 13/05/2010 13/11/2008
JP 2007-281526 A	25/10/2007	JP 4488037 B2	23/06/2010
US 2004-0137700 A1	15/07/2004	AU 2003-246348 A1 CN 1515025 A CN 1515025 C0 DE 10391811 B4 DE 10391811 T5 JP 2003-071591 A1 JP 4447325 B2 KR 10-2004-0086725 A TW 282118 A TW 282118 B TW I282118 B WO 03-071591 A1	09/09/2003 21/07/2004 21/07/2004 21/06/2012 14/04/2005 28/08/2003 07/04/2010 12/10/2004 01/06/2007 01/06/2007 01/06/2007 28/08/2003
US 2006-0205182 A1	14/09/2006	JP 2006-253402 A KR 10-0741864 B1	21/09/2006 24/07/2007