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(71) Applicant *(for all designated States except US)*: BOOKHAM TECHNOLOGY LIMITED [GB/GB]; 90 Milton Park, Abingdon, Oxfordshire OX14 4RY (GB).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: MAUND, Brigg [GB/GB]; Home Farm Cottage, 21a School Lane, Milton, Abingdon, Oxfordshire OX14 4EH (GB).

(74) Agents: PALMER, Roger et al.; Page White & Farrer, 54 Doughty Street, London WC1N 2LS (GB).

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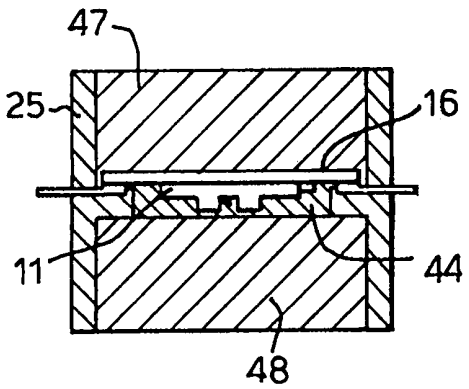
(54) Title: LEAD FRAME ATTACHMENT FOR OPTOELECTRONIC DEVICE

(57) Abstract

An optoelectronic device is mounted on a planar substrate in electrical connection with solder bumps adjacent an edge of the substrate and connection to a lead frame is made by loading the edge of the substrate on a lead frame support with lead frame conductors in engagement with the solder bumps and applying heat to melt the solder.



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# LEAD FRAME ATTACHMENT FOR OPTOELECTRONIC DEVICE

The invention relates to a method and apparatus for lead frame attachment to an optoelectronic device.

Optoelectronic devices are known, for example, integrated silicon waveguide devices, which are mounted on a rigid substrate prior to connecting to an electrical lead frame assembly and encapsulation to form a sealed product. In the case of integrated silicon waveguide devices having a connection to an optical fibre system, it is important to obtain an maintain correct position and orientation of the waveguide device with the optical fibre. It may also be necessary to form electrical connections to the device from a lead frame assembly and to package the assembly in a sealed manner so as to prevent degradation of operation of the optoelectronic device. For this reason integrated silicon waveguide devices may be mounted on a high mechanical modulus substrate such as a ceramic substrate. It has been known to locate such substrates within a premoulded encapsulating casing and to form electrical connections between conductors on the substrate and conductors of a lead frame assembly. Known techniques for interconnection of a ceramic substrate have involved wire bonding from the substrate to the lead frame. This may represent a second wire bonding operation in cases where the optoelectronic device has itself required a wire bonding operation to connect electrical devices to a conducting network on the substrate. In cases where the substrate is located within the walls of a package, restricted access can present problems in making wire bonded connections inside the walls of the package. Furthermore there may be reduced electrical performance due to the length of wire bonds necessary to connect the substrate to the lead frame.

It is an object of the present invention to provide improved method and apparatus for connecting a supporting substrate to a lead frame particularly when forming an enclosed package.

The invention provides a method of connecting an optoelectronic device to a lead frame assembly comprising mounting the optoelectronic device on a planar substrate having electrical connecting circuitry for connection to the optoelectronic device, connecting said device to said connecting circuitry, providing a plurality of solder bumps on a major face of the substrate adjacent an edge of the face, the solder bumps being in electrical connection with said connecting circuitry, mounting the substrate on a lead frame support which engages said major face adjacent its periphery, said lead frame support having lead frame conductors exposed on said support so as to contact said solder bumps, and applying heat to melt the solder and thereby form secure electrical connections between the lead frame conductors and the solder bumps.

Preferably said lead frame support forms part of a casing which is positioned around the substrate and which is sealed to enclose the optoelectronic device.

Preferably the lead frame support forms part of a mould which surrounds the substrate and the method includes moulding encapsulating material in the mould around the optoelectronic device and substrate to form a sealed product. Alternatively the lead frame is sealed using an adhesive lid.

Preferably the solder bumps are located on a peripheral region of the substrate between the optoelectronic device and said edge of the face so as to overlie the lead frame conductors when positioned on the lead frame support.

Preferably the solder bumps are provided on the same major face of the substrate as the optoelectronic device and said substrate is inverted to locate the solder bumps under the substrate when the substrate is mounted on the lead frame support.

Preferably pressure as well as heat is applied to urge the substrate into engagement with the lead frame support to cause

the solder bumps to form secure electrical connection with the lead frame conductors.

Preferably thermal access passages are provided through the thickness of said substrate adjacent said solder bumps and heat is transferred through said passages to melt the solder when connecting the substrate to the lead frame.

Thermal access passages may be provided through the lead frame support and heat is transferred through the passages in the lead frame support to melt the solder when connecting the substrate to the lead frame.

The substrate may comprise a rigid support providing a connection of fixed relationship of position and direction between an optical fibre and an integrated optical waveguide device which may include an optoelectrical light source or receiver and forming at least part of said optoelectronic device.

The optoelectronic device may comprise an integrated silicon chip providing an optical waveguide and may include an optoelectrical light source and/or receiver.

Preferably the substrate is a ceramic substrate.

The invention includes an optoelectronic assembly comprising a planar substrate having electrical connecting circuitry, and an optoelectronic device mounted on said planar substrate and having electrical connection to said electrical connecting circuitry, said substrate being provided with a plurality of solder bumps on a major face of the planar support adjacent an edge of the planar support, said solder bumps being in electrical connection with said electrical connecting circuitry, whereby said assembly may be located on a lead frame support with said solder bumps in engagement with lead frame conductors for securing thereto by application of heat.

The invention includes an optoelectronic assembly as aforesaid together with a lead frame assembly comprising a lead frame support with a plurality of lead frame conductors thereon, said support engaging the solder bumps of the planar substrate so that the lead frame conductors are secured to respective solder bumps by heat treatment of the solder bumps.

Some embodiments of the invention will now be described by way of example and with reference to the accompanying drawings in which:

Figure 1 is a top plan view of an optoelectronic device mounted on a substrate in accordance with the present invention,

Figure 2 is a section through the thickness of the assembly shown in Figure 1,

Figure 3 is an enlarged view of a peripheral region of the substrate used in Figures 1 and 2,

Figure 4 is a top plan view of a lead frame and mould assembly for use in accordance with the invention,

Figure 5 is an underplan view of the assembly of Figure 4,

Figure 6 is a top plan view of the assembly of Figure 4 when an optoelectronic device has been located in the mould,

Figure 7 is a section across the assembly of Figure 6,

Figure 8 is an underplan view of the assembly of Figure 6,

Figure 9 is a section across Figure 8,

Figure 10 shows an alternative structure of lead frame and mould used with an optoelectronic device of the type shown in Figure 1,

Figure 11 shows the assembly of Figure 10 when encapsulating material has been used and the mould sealed by lids,

Figure 12 shows a variation of Figure 11 in which different types of encapsulation have been used, and

Figure 13 shows a further variation of encapsulation without lids at the mould ends.

This example relates to the connection of an optoelectronic device to a lead frame in a sealed enclosure. The optoelectronic device may comprise an integrated silicon waveguide device of the type shown in our UK Patent 2307786. Such a device is shown in Figure 1 and marked 11. The device is formed as an integrated silicon chip having thereon one or more waveguides 12 interconnecting optoelectrical devices 13 such as laser diodes or photodiodes. The optical waveguides 12 are connected to an external optical fibre 14 which passes through a feeder channel 15 and is secured on an angled support pad 10 to give the required position and orientation for the connection between the fibre 14 and the waveguides 12 on the chip 11.

To maintain the correct positioning of the optical fibre 14 and silicon chip 11 they are both mounted on a planar substrate 16 which in this example is a high mechanical modulus material formed as a ceramic planar substrate. The substrate is provided with electrical connecting circuitry in the form of a plurality of leads 17 which extend across the substrate to provide an interconnection between the electrical devices on the chip 11 and external contact points 18 on the substrate. Firstly the chip 11 is fixed in known manner in a secure position on the substrate 16 and a first wire bonding operation interconnects the devices 13 by wires 19 to the array of leads 17 on the substrate. The substrate itself may have mounted thereon additional electronic devices such as that marked 20 and this is in turn connected to one of the external connections 18 on the substrate.

In this example the external electrical connections 18 are formed as solder bumps located on the upper major face of the substrate 16. The chip 11 is also secured on the same upper major face of the substrate 16 and is positioned away from the edges of the substrate so that the solder bumps 18 lie on the major face adjacent edges of the substrate and are located between the chip 11 and the edges of the substrate. This is shown more clearly in Figure 3 which shows an enlarged view of one solder bump 18 mounted on the substrate 16 and the electrical lead 17 forming a connection with the solder bump 18 is seen extending across the upper surface of the substrate 16. A thermal passage 22 is provided through the thickness of the substrate 16 adjacent each of the solder bumps 18 so that heat may be transferred through the thermal passage to the solder bump when attaching the assembly to the lead frame. The passageway 22 may be a hollow passage or contain a heat conductor of high thermal conductivity. To mount the device of Figures 1 and 2, a lead frame and mould assembly is provided as shown in Figures 4 and 5. Figure 4 shows a rectangular mould wall 25 having on its inner face a lead frame support in the form of a shelf 26. The shelf 26 surrounds a hollow space and provides a shoulder on which the substrate 16 of Figure 1 may be supported. An array of lead frame conducting wires 28 extend through the wall 25 on two opposite sides of the rectangular frame and have exposed conductors 30 on the upper surface of the shelf 26. At one end of the frame a projecting channel 31 is provided to hold the optical fibre 14 in position when the assembly of Figure 1 is located in the frame of Figure 4. The assembly of Figure 1 is inverted so that the chip 11 is on the underface of the substrate 16 and the assembly of Figure 1 then drops into position in the frame of Figure 4 so that the frame closely surrounds the substrate with the peripheral regions of the major face of the substrate resting on the shoulder 26. The solder bumps 18 are then resting in face to face engagement with respective wire ends 30 of the lead frame conductors. As shown in Figure 4 additional bonding strips 36 are provided on the shelf 26 and arranged to engage mating bonding strips 37 on the substrate 16 (shown in Figure 1). This assists in securing

the substrate 16 in the required position with the solder bumps 18 engaging respective lead frame wire ends 30.

As shown in Figure 5, the shelf 26 seen from the underside has a plurality of thermal passageways 38 provided through the thickness of the shelf 26 immediately below respective conductor ends 30. When the substrate 16 is located in position, heat and pressure is applied to urge the substrate 16 into contact with the shelf 26 and melt the solder bumps 18 so as to form a secure electrical connection between the solder bumps 18 and respective conductors of the lead frame assembly. When the heat and pressure is removed the solder will solidify leaving permanent electrical connections with the components maintained in their required relative positions.

This operation is illustrated in Figures 6 to 9. Figure 6 shows an assembly similar to that of Figure 1 when it has been inverted and dropped into position in the mould and lead frame assembly of the type shown in Figure 4. As the chip has been inverted Figure 6 shows the underface of the substrate 16 and in the particular arrangement shown in Figure 6 the substrate 16 has been modified to provide additional thermal passages 39 through the thickness of the substrate to assist in the passage of heat to melt the solder during the bonding operation. The thermal passages 39 provided in the substrate may be in addition to the thermal passages 38 provided through the shelf of the frame 25. Figure 7 shows the passages 38 through the shelf 26 lying below the substrate 16. As illustrated in Figure 7 the shelf 26 is positioned partway between the opposite ends of the frame so that when the substrate 16 is located in position with the chip 11 on its underface, the contents of the frame are spaced inwardly from the ends so that encapsulating material may be added on both sides of the substrate 16 to encapsulate the assembly and seal the optoelectronic device against the external environment. Figure 8 shows the underplan view of the assembly in Figure 6 and is similar to the view of Figure 5 with the substrate and chip in position. Figure 9 illustrates the same assembly as Figure

7 but turned back to the position in which the substrate 16 lies below the chip 11.

It will be appreciated that by using the solder bump array which overlies the ends of the lead frame conductors 28 in face to face engagement with them, there is no requirement for a second wire bonding operation which would extend the lateral extent of wires from the substrate 16. Furthermore there is no requirement for the insertion of any wire bonding tool between the edges of the substrate 16 and the surrounding frame 25. Consequently access is not a problem as the heat and pressure is applied through the top and bottom open ends of the frame 25 through which access is not restricted. It will be understood that the bonds with a plurality, and preferably with all, of the solder bumps 18 are formed simultaneously by a single operation.

Once the bonding has taken place, the package may be sealed in a variety of different ways. The atmosphere within the frame may be purged to provide an inert atmosphere. The starting point for this is illustrated in one example in Figure 10 when the assembly has been secured in position but no material has been added to either end of the frame 25 to seal the unit. The substrate and chip 11 may be surrounded with a silicone encapsulant material such as is illustrated by 40 and 41 on both sides of the substrate 16 in Figure 11. Such silicone material may totally encapsulate the substrate 16 and chip 11 although it need not necessarily fill the frame 25 to reach both ends of the frame. The package may be sealed by upper and lower lids 42 and 43 as illustrated in Figure 11. As an alternative epoxy resin may be used to fill or partially fill the cavity within the frame 25. In Figure 12 a silicone layer 44 has been used to cover the major face of the substrate on which the chip 11 is mounted. In that way the chip itself is secured within a silicone encapsulant. Epoxy resin is then used as indicated at 45 and 46 to partially fill opposite sides of the frame on both sides of the substrate 16. Lids 42 and 43 enclose the package as already described with reference to Figure 11 in the case of an alternative arrangement

shown in Figure 13 the face of the substrate 16 on which the chip 11 is mounted is encased in a silicone layer 44 similar to that shown in Figure 12. In this case the remainder of the cavity within the mould frame 25 is filled with epoxy material 47 and 48 on opposite sides of the substrate 16 so that the frame is completely filled with epoxy resin flush with opposite ends of the package. In such an arrangement no additional lids 42 and 43 are required.

The invention is not limited to the details of the foregoing examples.

CLAIMS:

1. A method of connecting an optoelectronic device to a lead frame assembly comprising mounting the optoelectronic device on a planar substrate having electrical connecting circuitry for connection to the optoelectronic device, connecting said device to said connecting circuitry, providing a plurality of solder bumps on a major face of the substrate adjacent an edge of the face, the solder bumps being in electrical connection with said connecting circuitry, mounting the substrate on a lead frame support which engages said major face adjacent its periphery, said lead frame support having lead frame conductors exposed on said support so as to contact said solder bumps, and applying heat to melt the solder and thereby form secure electrical connections between the lead frame conductors and the solder bumps.

2. A method according to claim 1 in which heat to melt the solder is applied to a plurality of solder bumps simultaneously to bond the bumps to respective lead frame conductors in a single operation.

3. A method according to claim 1 or claim 2 in which said lead frame support forms part of a casing which is positioned around the substrate and which is sealed to enclose the optoelectronic device.

4. A method according to any one of the preceding claims in which the lead frame support forms part of a mould which surrounds the substrate and the method includes moulding encapsulating material in the mould around the optoelectronic device and substrate to form a sealed product.

5. A method according to any one of the preceding claims in which the solder bumps are located on a peripheral region of the substrate between the optoelectronic device and said edge of the face so as to overlie the lead frame conductors when positioned

on the lead frame support.

6. A method according to any one of the preceding claims in which the solder bumps are provided on the same major face of the substrate as the optoelectronic device and said substrate is inverted to locate the solder bumps under the substrate when the substrate is mounted on the lead frame support.

7. A method according to any one of the preceding claims in which pressure as well as heat is applied to urge the substrate into engagement with the lead frame support to cause the solder bumps to form secure electrical connection with the lead frame conductors.

8. A method according to any one of the preceding claims in which thermal access passages are provided through the thickness of said substrate adjacent said solder bumps and heat is transferred through said passages to melt the solder when connecting the substrate to the lead frame.

9. A method according to any one of the preceding claims in which thermal access passages are provided through the lead frame support and heat is transferred through the passages in the lead frame support to melt the solder when connecting the substrate to the lead frame.

10. A method according to any one of the preceding claims in which the substrate comprises a rigid support providing a connection of fixed relationship of position and direction between an optical fibre and an integrated optical waveguide device including at least one optoelectrical light source or receiver and forming at least part of said optoelectronic device.

11. A method according to claim 10 in which the optoelectronic device comprises an integrated silicon chip providing an optical waveguide and including an optoelectrical light source and/or receiver.

12. A method according to any one of the preceding claims in which the substrate is a ceramic substrate.

13. A optoelectronic assembly comprising a planar substrate having electrical connecting circuitry, and an optoelectronic device mounted on said planar substrate and having electrical connection to said electrical connecting circuitry, said substrate being provided with a plurality of solder bumps on a major face of the planar support adjacent an edge of the planar support, said solder bumps being in electrical connection with said electrical connecting circuitry, whereby said assembly may be located on a lead frame support with said solder bumps in engagement with lead frame conductors for securing thereto by application of heat.

14. An optoelectronic assembly according to claim 13 in which said solder bumps are provided on a peripheral region of a major face of the substrate and located between the optoelectronic device and said edge of the support.

15. An assembly according to claim 13 or claim 14 in which thermal conducting passages are provided through the planar support adjacent said solder bumps.

16. An optoelectronic assembly according to any of claims 13 to 15 together with a lead frame assembly comprising a lead frame support with a plurality of lead frame conductors thereon, said support engaging the solder bumps of the planar substrate so that the lead frame conductors are secured to respective solder bumps by heat treatment of the solder bumps.

17. An assembly according to claim 16 in which securing means are located between edge regions of the substrate and the lead frame support to secure the substrate in position on the support.

18. An optoelectronic assembly according to claim 16 or claim

17 in which the lead frame support forms part of a casing which is positioned around the substrate and which is sealed to enclose the optoelectronic device.

19. An assembly according to claim 18 in which the lead frame support forms part of a mould surrounding the substrate, said mould containing encapsulating material around the optoelectronic device and substrate to form a sealed product.

20. An assembly according to any of claims 16 to 19 in which the solder bumps are located on the same face of the substrate as the optoelectronic device and said substrate is inverted to locate the solder bumps under the substrate in engagement with the lead frame conductors.

21. An assembly according to any one of claims 16 to 20 in which thermal access passages are provided through the lead frame support for the transfer of heat to the solder bumps during connection of the bumps to the lead frame conductors.

22. A method of connecting an optoelectronic device to a lead frame assembly substantially as hereinbefore described with reference to the accompanying drawings.

23. An optoelectronic assembly comprising a planar support with an optoelectronic device mounted thereon together with a lead frame assembly connected to the substrate substantially as hereinbefore described with reference to the accompanying drawings.

Fig.1.

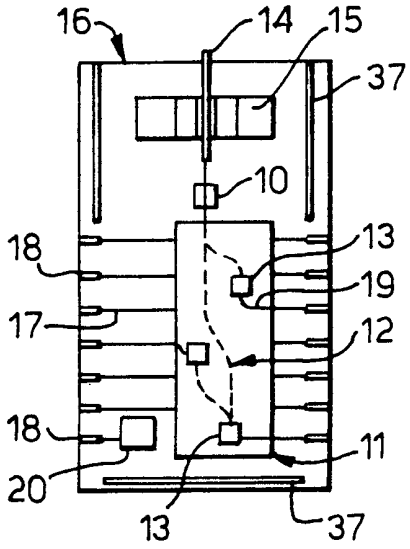



Fig.2.

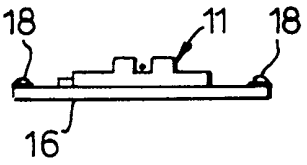



Fig.3.

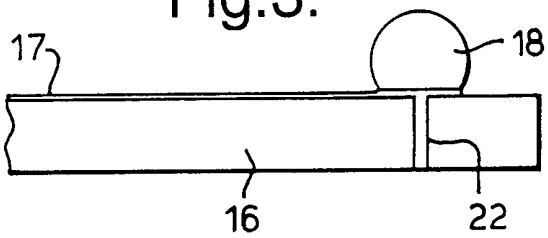



Fig.4.

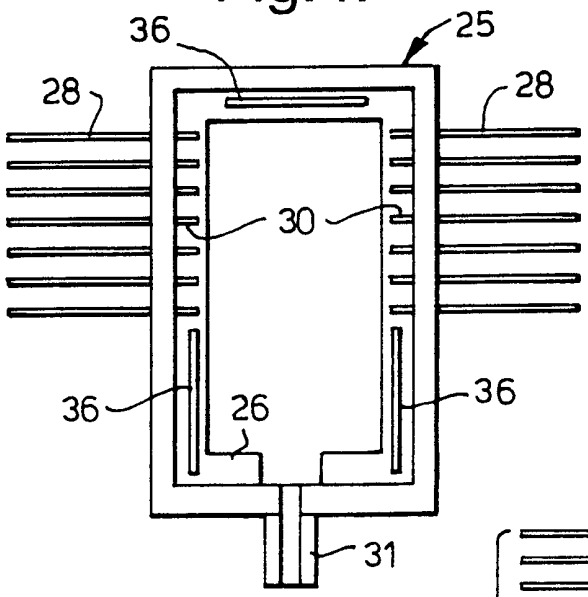



Fig.5.

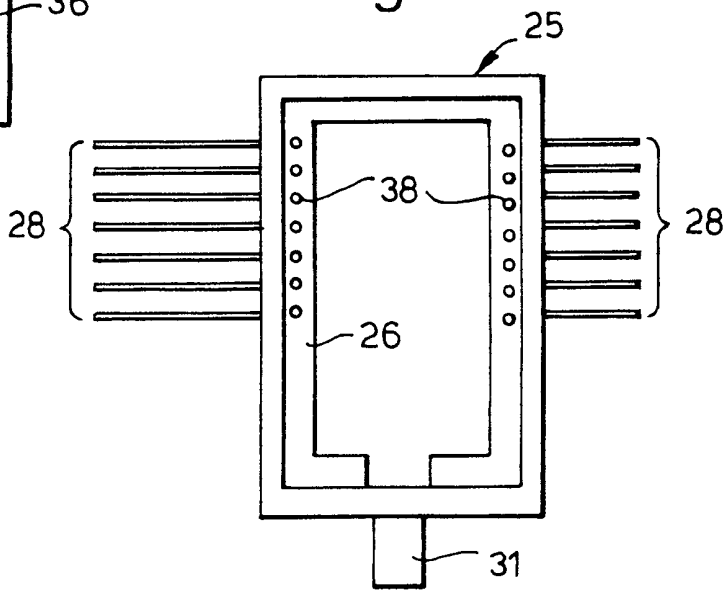


Fig.6.

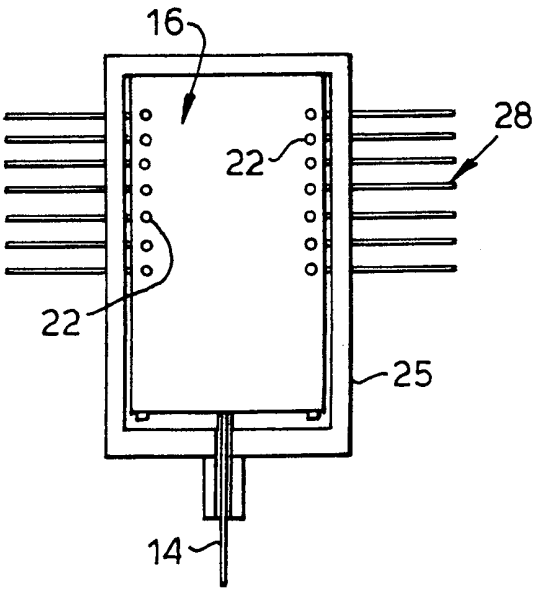



Fig.7.

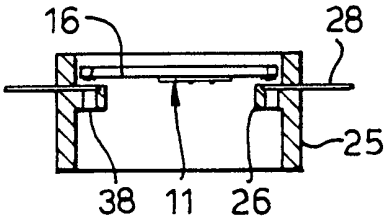



Fig.8.

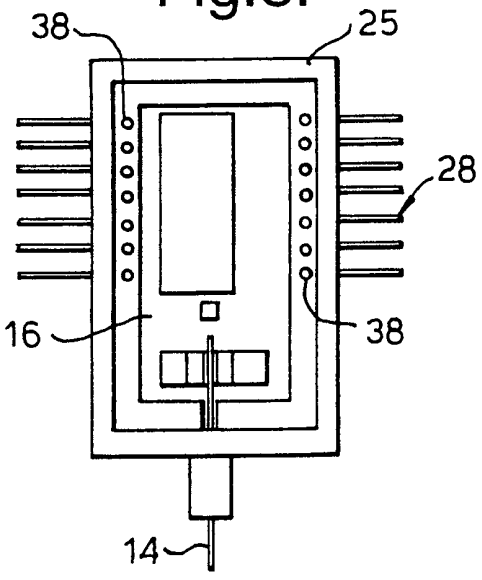



Fig.9.

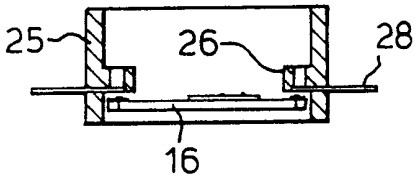


Fig.10.

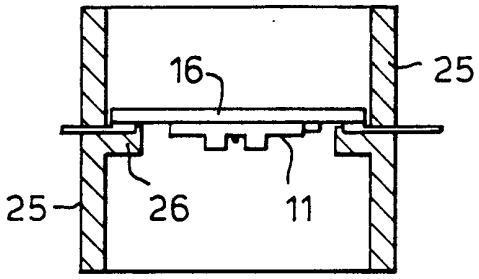



Fig.11.

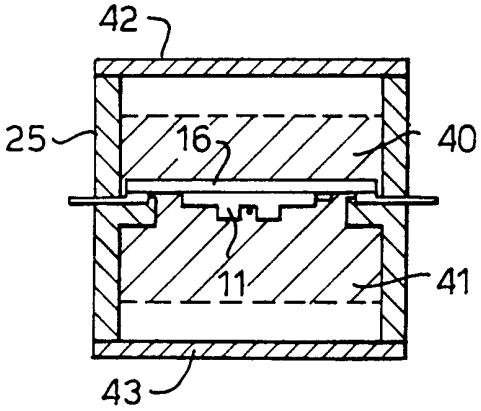



Fig.12.

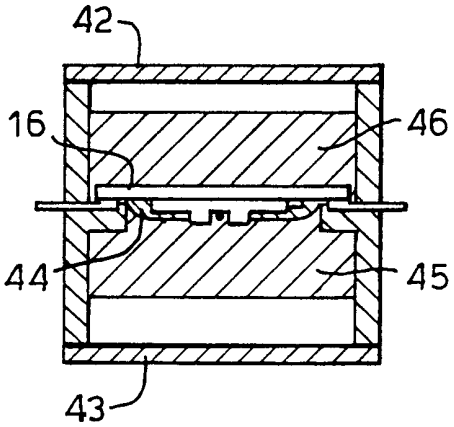
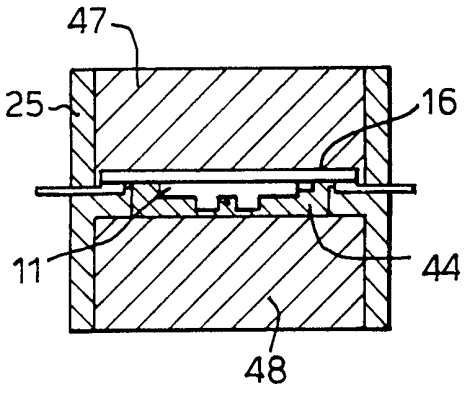



Fig.13.



# INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/01970

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L31/0203 H01L33/00 H01L21/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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| X | US 5 753 857 A (CHOI SIHN) 19 May 1998 (1998-05-19) the whole document | 1-7, 12-14, 16-20, 22,23 |
| Y | | 8,9,15, 21 |
| Y | US 5 640 048 A (SELNA ERICH) 17 June 1997 (1997-06-17) abstract; figure 2 | 8,9,15, 21 |
| X | EP 0 579 438 A (AMERICAN TELEPHONE & TELEGRAPH) 19 January 1994 (1994-01-19) the whole document | 1-7, 10-14, 16, 18-20, 22,23 |

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| 29 September 1999 | 06/10/1999 |

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| European Patent Office, P.B. 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel. (+31–70) 340–2040, Tx. 31 651 epo nl,<br>Fax: (+31–70) 340–3016 | Munnix, S |

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