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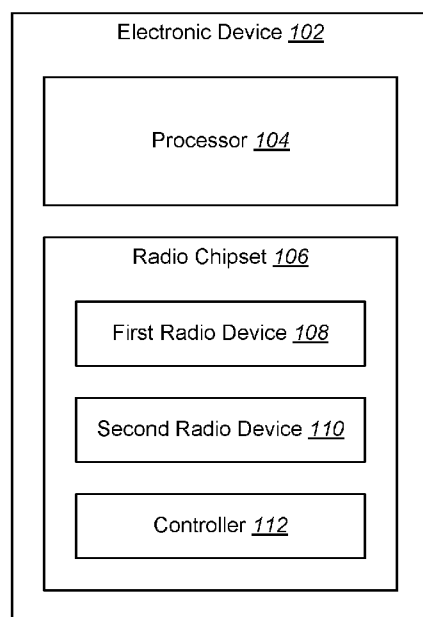


FIG. 1

(57) Abstract: Examples of electronic devices are described herein. In some examples, an electronic device includes a radio chipset that includes a controller, a first radio device, and a second radio device. In some examples, the electronic device includes a processor to detect a hang condition for the first radio device, and send a hang condition signal to the second radio device. In some examples, the controller is to reset the first radio device in response to receiving the hang condition signal from the second radio device.

RESET FOR RADIO CHIPSETS

BACKGROUND

[0001] Electronic technology has advanced to become virtually ubiquitous in society and has been used to improve many activities in society. For example, electronic devices are used to perform a variety of tasks, including work activities, communication, research, and entertainment. Different varieties of electronic circuits may be utilized to provide different varieties of electronic technology.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Various examples will be described below by referring to the following figures.

[0003] FIG. 1 is a block diagram illustrating an example of an electronic device that may be utilized to reset a radio chipset;

[0004] FIG. 2 is a block diagram illustrating another example of an electronic device that may be utilized to reset a radio chipset;

[0005] FIG. 3 is a block diagram illustrating an example of a computer-readable medium to reset a radio chipset; and

[0006] FIG. 4 is a flow diagram illustrating an example of a method for resetting a radio chipset.

[0007] Throughout the drawings, identical or similar reference numbers may designate similar, but not necessarily identical, elements. The figures are not necessarily to scale, and the size of some parts may be exaggerated to more clearly illustrate the example shown. Moreover, the drawings provide examples

in accordance with the description; however, the description is not limited to the examples provided in the drawings.

DETAILED DESCRIPTION

[0008] An electronic device may be a device that includes electronic circuitry. For instance, an electronic device may include integrated circuitry (e.g., transistors, digital logic, semiconductor technology, etc.). Examples of electronic devices include computing devices, laptop computers, desktop computers, smartphones, tablet devices, wireless communication devices, game consoles, smart appliances, printing devices, vehicles with electronic components, aircraft, drones, robots, smart appliances, etc.

[0009] The examples described herein provide a self-recovery approach for a radio chipset. In some examples, the radio chipset may include a first radio device and a second radio device. The radio chipset may also include a controller to control the first radio device and the second radio device. In some examples, the first radio device may communicate using a first radio technology (e.g., Bluetooth) and the second radio device may communicate using a second radio technology (e.g., IEEE 802.11 standards (also referred to as WiFi)). In some examples, the components of the radio chipset (e.g., the first radio device, the second radio device, and the controller) may be included on a single substrate (e.g., a semiconductor wafer).

[0010] In some examples, the radio chipset may be included in an electronic device. A processor of the electronic device may implement a first radio driver to communicate with the first radio device on the radio chipset. The processor may also implement a second radio driver to communicate with the second radio device.

[0011] The first radio driver (e.g., a Bluetooth driver) may monitor the first radio device (e.g., Bluetooth device) for a hang condition. In some examples, a hang condition may occur when the first radio device becomes unresponsive to the first radio driver. For example, the first radio device may stop functioning properly. In another example, a hang condition may occur when a

communication bus (referred to herein as a first bus) used by the first radio driver to communicate with the first radio device becomes unresponsive such that the first radio driver is unable to communicate with the first radio device. A hang condition may also be referred to as a crash or hang.

[0012] If the first radio driver detects a hang condition in the first radio device, the electronic device may use the second radio device to communicate the presence of the hang condition back to the radio chipset. For example, the second radio driver (e.g., WiFi driver) may send a hang condition signal to the second radio device (e.g., WiFi device). The second radio device may then inform the controller on the radio chipset about the hang condition of the first radio device. The controller may then reset the first radio device.

[0013] FIG. 1 is a block diagram illustrating an example of an electronic device 102 that may be utilized to reset a radio chipset 106. Examples of the electronic device 102 may include computing devices, laptop computers, desktop computers, tablet devices, cellular phones, smartphones, wireless communication devices, game consoles, smart appliances, printing devices, vehicles with electronic components, aircraft, drones, robots, smart appliances, etc.

[0014] In some examples, the electronic device 102 may include a processor 104 and/or a memory (not shown). The processor 104 may be any of a central processing unit (CPU), a semiconductor-based microprocessor, graphics processing unit (GPU), field-programmable gate array (FPGA), an application-specific integrated circuit (ASIC), and/or other hardware device suitable for retrieval and execution of instructions stored in the memory. The processor 104 may fetch, decode, and/or execute instructions stored in the memory. While a single processor 104 is shown in FIG. 1, in other examples, the processor 104 may include multiple processors (e.g., a CPU and a GPU).

[0015] The memory may be any electronic, magnetic, optical, and/or other physical storage device that contains or stores electronic information (e.g., instructions and/or data). The memory may be, for example, Random Access Memory (RAM), Electrically Erasable Programmable Read-Only Memory (EEPROM), Dynamic Random Access Memory (DRAM), Synchronous DRAM

(SDRAM), magnetoresistive random-access memory (MRAM), phase change RAM (PCRAM), non-volatile random-access memory (NVRAM), memristor, flash memory, a storage device, and/or an optical disc, etc. In some examples, the memory may be a non-transitory tangible computer-readable storage medium, where the term “non-transitory” does not encompass transitory propagating signals. The processor 104 may be in electronic communication with the memory. In some examples, a processor 104 and/or memory of the electronic device 102 may be combined with or separate from a processor (e.g., CPU) and/or memory of a host device.

[0016] In some examples, the electronic device 102 may include different sets of memory. For example, the electronic device 102 may store certain information (e.g., instructions executed by the processor 104) in a first memory. The electronic device 102 may store other information (e.g., instructions executed by a controller 112) in a second memory.

[0017] The electronic device 102 may include a radio chipset 106. In some examples, the radio chipset 106 may include a first radio device 108, a second radio device 110 and a controller 112. In some examples, the radio chipset 106 may be implemented as a system on chip (SoC) in which the components of the radio chipset (e.g., the first radio device 108, the second radio device 110, and the controller 112) are fabricated on a single substrate (e.g., a semiconductor wafer). Therefore, the radio chipset 106 may be a distinct module that is included in the electronic device 102.

[0018] In some examples, the first radio device 108 may communicate using a first radio technology (e.g., Bluetooth) and the second radio device 110 may communicate using a second radio technology (e.g., IEEE 802.11 standards (also referred to as WiFi)). In other examples, the first radio device 108 and/or the second radio device 110 may communicate using a wireless wide area network (WWAN) (e.g., cellular communication, 2G, 3G, 4G, LTE, 5G, etc.), Global Positioning System (GPS), inductive communication (e.g., NFC), Zigbee, or other radio communication technology.

[0019] In some examples, the controller 112 of the radio chipset 106 may include a semiconductor-based processor (e.g., microprocessor), field-

programmable gate array (FPGA), an application-specific integrated circuit (ASIC), and/or other hardware device suitable for retrieval and execution of instructions stored in memory. The processor of the controller 112 may fetch, decode, and/or execute instructions stored in memory.

[0020] In some examples, the electronic device 102 may provide power to the radio chipset 106 via a single power pin. In some examples, the electronic device 102 may include a single reset pin to reset the radio chipset 106. In some examples, the first radio device 108 may communicate with the processor 104 over a first bus. The second radio device 110 may communicate with the processor 104 over a second bus. As used herein, a bus is an interface between components of the electronic device 102. Some examples of the first bus and/or second bus include a universal serial bus (USB), peripheral component interconnect (PCI) bus, or peripheral component interconnect express (PCIe) bus.

[0021] In some cases, the first radio device 108 may experience a hang condition. As used herein, a hang condition may be a persistent unresponsive state of a component. For example, the first radio device 108 may crash or may experience anomalous behavior that restricts the ability for the processor 104 to communicate with the first radio device 108. In some examples, the hang condition may occur due to a programming logic issue. In other examples, a hang condition may occur if the first bus becomes unresponsive, thus restricting communication between the processor 104 and the first radio device 108.

[0022] In some examples, the processor 104 may not be able to reset the first radio device 108. For example, if the first radio device 108 becomes unresponsive, a reset command sent on the first bus may be ineffective. In another example, if the first bus is in a hang condition, then a reset signal sent by the processor 104 on the first bus may not be able to reach the first radio device 108.

[0023] In some examples, a global reset of the radio chipset 106 by the processor 104 may cause a disruptive reset of the entire radio chipset 106. For example, if the power pin and/or reset pin for the radio chipset 106 are shared by the first radio device 108 and the second radio device 110, then a reset by

the processor 104 via the power pin or reset pin will reset both the first radio device 108 and the second radio device 110. In an example, a user may listen to music using the first radio device 108 (e.g., a Bluetooth device) while simultaneously using the second radio device 110 (e.g., a WiFi device). In this example, if the first radio device 108 becomes unresponsive due to a hang condition, then a global reset of the radio chipset 106 would also reset the second radio device 110 (e.g., WiFi). This scenario may result in a poor user experience.

[0024] The examples described herein provide for a self-recovery of the first radio device 108 without performing a global reset of the radio chipset 106 by the processor 104. In these examples, the processor 104 may inform the radio chipset 106 of the hang condition of the first radio device 108 using the second radio device 110. The radio chipset 106 may then reset the first radio device 108 without resetting the second radio device 110.

[0025] The processor 104 may detect a hang condition for the first radio device 108. For example, the processor 104 may determine that the first radio device 108 or the first bus is unresponsive. The processor 104 may detect the hang condition for the first radio device 108 using the first bus. In some examples, the processor 104 may monitor the first bus for responses from the first radio device 108. In some examples, the processor 104 may send a command or other signal to elicit a response from the first radio device 108 on the first bus. If the first radio device 108 does not respond to the processor 104, then the processor 104 may determine that the first radio device 108 is in a hang condition.

[0026] The processor 104 may send a hang condition signal to the second radio device 110 in response to detecting the hang condition. For example, the processor 104 may send the hang condition signal to the second radio device 110 using the second bus. In some examples, the hang condition signal may indicate that a hang condition has been detected for the first radio device 108.

[0027] Upon receiving the hang condition signal from the processor 104, the second radio device 110 may send the hang condition signal to the controller 112. The controller 112 may reset the first radio device 108 in response to

receiving the hang condition signal from the second radio device 110. For example, the controller 112 may set a register (referred to herein as the first radio reset register) to reset the first radio device 108. In this example, setting the first radio reset register to reset the first radio device 108 may cause the first radio device 108 to perform a reset procedure. In this example, setting the first radio reset register may include setting a value (e.g., “1” or “0”) in the first radio reset register that causes the first radio device 108 to perform a reset procedure. In some examples, the reset procedure may clear memory inside the first radio device 108. The reset procedure may also reinitialize the first bus to establish communication between the first radio device 108 and the processor 104.

[0028] In another example, the controller 112 may actuate a reset pin (referred to as a first radio reset pin) for resetting the first radio device 108. For example, the first radio reset pin may be a pin that is internal to the radio chipset 106. The controller 112 may actuate the first radio reset pin by changing the state (e.g., the electrical state or logic state) of the first radio reset pin to reset the first radio device 108. For example, the controller 112 may pull the first radio reset pin high or low to reset the first radio device 108.

[0029] In yet another example, the controller 112 may reset the first radio device 108 by cycling power to the first radio device 108. For example, the controller 112 may switch power to the first radio device 108 off and then back on. This power cycling may cause the first radio device 108 to restart, thus resetting communication with the processor 104.

[0030] The second radio device 110 may remain active while the controller 112 resets the first radio device 108. For example, the radio chipset 106 may include separate mechanisms to reset the first radio device 108 and the second radio device 110. In some examples, the controller 112 may use the first radio reset register or first radio reset pin to reset the first radio device 108 independent of the second radio device 110. Therefore, the controller 112 may reset the first radio device 108 (e.g., via the first radio reset register or first radio reset pin) without resetting the second radio device 110.

[0031] FIG. 2 is a block diagram illustrating another example of an electronic device that may be utilized to reset a radio chipset 206. The electronic device 202 may be implemented in accordance with the electronic device 102 described in FIG. 1. For example, the electronic device 202 may include a processor 204 and a radio chipset 206 as described in FIG. 1.

[0032] In some examples, the processor 204 may implement a first radio driver 220 for communicating with the first radio device 208 of the radio chipset 206. The processor 204 may also implement a second radio driver 222 for communicating with the second radio device 210 of the radio chipset 206. As used herein, a driver is a program executed by the processor 204 that operates, controls and/or communicates with a device included in the electronic device 202. A driver may provide an interface for an operating system 214 and/or Basic Input/Output System (BIOS) 216 of the electronic device 202 to interact with hardware components.

[0033] As used herein, a basic input/output system (BIOS) 216 refers to hardware or hardware and instructions to initialize, control, or operate the electronic device 202 prior to execution of an operating system (OS) 214 of the electronic device 202. Instructions included within the BIOS 216 may be software, firmware, microcode, or other programming that defines or controls functionality or operation of the BIOS 216. In one example, the BIOS 216 may be implemented using instructions, such as platform firmware of the electronic device 202, executable by the processor 204. The BIOS 216 may operate or execute prior to the execution of the OS 214 of the electronic device 202. The BIOS 216 may initialize, control, or operate components such as hardware components of the electronic device 202 and may load or boot the OS 214 of the electronic device 202.

[0034] In some examples, the BIOS 216 may provide or may establish an interface between hardware devices or platform firmware of the electronic device 202 and the OS 214 of the electronic device 202, via which the OS 214 of the electronic device 202 may control or operate hardware devices or platform firmware of the electronic device 202. In some examples, the BIOS 216 may implement the Unified Extensible Firmware Interface (UEFI) specification or

another specification or standard for initializing, controlling, or operating the electronic device 202.

[0035] In some examples, the electronic device 202 may include a first bus 224 for communications between the first radio device 208 and the first radio driver 220. The electronic device 202 may also include second bus 226 for communications between the second radio device 210 and the second radio driver 222. The first bus 224 and/or the second bus 226 may be a USB, PCI bus, a PCIe bus, or a bus using another communication protocol.

[0036] The first radio driver 220 may monitor the first bus 224 for a hang condition by the first radio device 208. For example, the first radio driver 220 may send a command or other signal to the first radio device 208 on the first bus 224 to elicit a response from the first radio device 208. In some examples, the first radio driver 220 may periodically send the command or other signal to the first radio device 208. For example, the first radio driver 220 may send the command or other signal at a certain frequency.

[0037] The first radio driver 220 may detect the hang condition in response to a failure to receive a response to the command from the first radio device 208. For example, if the first radio device 208 fails to respond to the command after a certain number (e.g., 3) of attempts, then the first radio driver 220 may determine that a hang condition exists for the first radio device 208 and/or the first bus 224.

[0038] The first radio driver 220 may send a hang condition signal to a background process 218 in response to detecting the hang condition. In some examples, the first radio driver 220 and the second radio driver 222 may not be able to communicate directly with each other. For instance, the first radio driver 220 and the second radio driver 222 may be low layer programs that facilitate communication between the first radio device 208 and second radio device 210 and higher layer programs of the OS 214 and/or BIOS 216. The background process 218 (also referred to as a daemon or service) may run in the background without user intervention. The background process 218 may be a higher layer program that communicates with both the first radio driver 220 and the second radio driver 222.

[0039] Upon receiving the hang condition signal from the first radio driver 220, the background process 218 may send the hang condition signal to the second radio driver 222. The second radio driver 222 may then send the hang condition signal to the second radio device 210 on the second bus 226.

[0040] Upon receiving the hang condition signal from the second radio driver 222, the second radio device 210 may send the hang condition signal to the controller 212. The hang condition signal may cause the controller 212 to reset the first radio device 208. For example, the controller 212 may set a first radio reset register or actuate a first radio reset pin to reset the first radio device 208.

[0041] The second radio device 210 may remain active while the controller 212 resets the first radio device 208. This may minimize the impact on a user experience as the user may continue to use the second radio device 210 while the first radio device 208 resets.

[0042] FIG. 3 is a block diagram illustrating an example of a computer-readable medium 330 to reset a radio chipset. The computer-readable medium 330 may be a non-transitory, tangible computer-readable medium 330. The computer-readable medium 330 may be, for example, RAM, EEPROM, a storage device, an optical disc, and the like. In some examples, the computer-readable medium 330 may be volatile and/or non-volatile memory, such as DRAM, EEPROM, MRAM, PCRAM, memristor, flash memory, and the like. In some examples, the computer-readable medium 330 described in FIG. 3 may be an example of memory for an electronic device 102 described in FIG. 1 or memory for an electronic device 202 described in FIG. 2. In some examples, code (e.g., data and/or executable code or instructions) of the computer-readable medium 330 may be transferred and/or loaded to memory or memories of the electronic device 102 or electronic device 202.

[0043] The computer-readable medium 330 may include code (e.g., data and/or executable code or instructions). For example, the computer-readable medium 330 may include hang condition detection instructions 332, and/or hang condition signal instructions 334.

[0044] In some examples, the hang condition detection instructions 332 may be instructions that when executed cause a processor of the electronic device to

detect, by a first radio driver, a hang condition for a first radio device on a radio chipset that includes the first radio device, a second radio device and a controller. For example, the first radio driver may monitor a first bus for the hang condition by the first radio device. Monitoring by the first radio driver may include sending a command to the first radio device and detecting the hang condition in response to a failure to receive a response to the command from the first radio device. In some examples, this may be accomplished as described in FIGS. 1–2.

[0045] In some examples, the hang condition signal instructions 334 may be instructions that when executed cause the processor of the electronic device to send, by a second radio driver, a hang condition signal to the second radio device. The hang condition signal may cause the controller of the radio chipset to reset the first radio device. In some examples, the hang condition signal instructions 334 may further include instructions that when executed cause the processor of the electronic device to send, by the first radio driver, the hang condition signal to a background process. The background process may then send the hang condition signal to the second radio driver. In some examples, this may be accomplished as described in FIGS. 1–2.

[0046] FIG. 4 is a flow diagram illustrating an example of a method 400 for resetting a radio chipset. The method 400 and/or an element or elements of the method 400 may be performed by an electronic device. For example, an element or elements of the method 400 may be performed by the electronic device 102, the processor 104, the controller 112 described in FIG. 1, and/or the electronic device 202, the processor 204, or the controller 212 described in FIG. 2, any of which may be referred to generally as an “electronic device” in FIG. 4.

[0047] A first radio device of the electronic device may enter 402 a hang condition. For example, the first radio device of a radio chipset and/or a first bus may crash or may otherwise become unresponsive.

[0048] The first radio driver of the electronic device may detect 404 the hang condition. For example, the processor of the electronic device may execute the first radio driver to communicate with the first radio device. The first radio driver may monitor a first bus for the hang condition. In some examples, the first radio

driver may send a command to the first radio device. The first radio driver may detect the hang condition in response to a failure to receive a response to the command from the first radio device.

[0049] The first radio driver may send 406 a hang condition signal to a background process. For example, the processor of the electronic device may execute a background process to communicate with the first radio driver and a second radio driver. Upon receiving the hang condition signal, the background process may send 408 the hang condition signal to the second radio driver executed by the processor of the electronic device.

[0050] The second radio driver may send 410 the hang condition signal to the second radio device. For example, the second radio driver may send 410 the hang condition signal to the second radio device on a second bus.

[0051] Upon receiving the hang condition signal, the second radio device may send 412 the hang condition signal to the controller of the radio chipset. For example, the radio chipset may include a communication link (e.g., a bus) for communication between the second radio device and the controller. The second radio device may use the communication link to forward the hang condition signal to the controller.

[0052] The controller may reset 414 the first radio device in response to receiving the hang condition signal from the second radio device. For example, upon receiving the hang condition signal, the controller may set a first radio reset register to reset the first radio device. In another example, the controller may actuate a first radio reset pin to reset the first radio device.

[0053] As used herein, the term “and/or” may mean an item or items. For example, the phrase “A, B, and/or C” may mean any of: A (without B and C), B (without A and C), C (without A and B), A and B (but not C), B and C (but not A), A and C (but not B), or all of A, B, and C.

[0054] While various examples are described herein, the disclosure is not limited to the examples. Variations of the examples described herein may be within the scope of the disclosure. For example, operations, functions, aspects, or elements of the examples described herein may be omitted or combined.

CLAIMS

1. An electronic device, comprising:
a radio chipset comprising:
a controller;
a first radio device; and
a second radio device; and
a processor to:
detect a hang condition for the first radio device; and
send a hang condition signal to the second radio device,
wherein the controller is to reset the first radio device in response to
receiving the hang condition signal from the second radio device.
2. The electronic device of claim 1, wherein the processor to detect the hang condition for the first radio device comprises the processor to determine that the first radio device or a first bus is unresponsive.
3. The electronic device of claim 1, further comprising a first bus on which the processor is to detect the hang condition for the first radio device.
4. The electronic device of claim 1, further comprising a second bus to send the hang condition signal to the second radio device.
5. The electronic device of claim 1, wherein the second radio device is to remain active while the controller resets the first radio device.
6. An electronic device, the electronic device to:
receive a hang condition signal at a second radio device in response to a hang condition for a first radio device on a radio chipset comprising the first radio device, the second radio device and a controller;
send the hang condition signal to the controller; and

reset the first radio device in response to the controller receiving the hang condition signal from the second radio device.

7. The electronic device of claim 6, wherein the first radio device comprises a Bluetooth device and the second radio device comprises a WiFi device.

8. The electronic device of claim 6, wherein the electronic device to reset the first radio device comprises the controller to set a first radio reset register to reset the first radio device.

9. The electronic device of claim 6, wherein the electronic device to reset the first radio device comprises the controller to actuate a first radio reset pin for the first radio device.

10. The electronic device of claim 6, wherein the radio chipset comprises a system on a chip that includes the first radio device, the second radio device and the controller on a single substrate.

11. A non-transitory tangible computer-readable medium comprising instructions when executed cause a processor of an electronic device to:

- detect, by a first radio driver, a hang condition for a first radio device on a radio chipset comprising the first radio device, a second radio device and a controller;
- send, by a second radio driver, a hang condition signal to the second radio device, the hang condition signal to cause the controller to reset the first radio device.

12. The non-transitory tangible computer-readable medium of claim 11, further comprising instructions when executed cause the processor of the electronic device to:

- send, by the first radio driver, the hang condition signal to a background process; and

send, by the background process; the hang condition signal to the second radio driver.

13. The non-transitory tangible computer-readable medium of claim 11, wherein the first radio driver is to:

send a command to the first radio device; and
detect the hang condition in response to a failure to receive a response to the command from the first radio device.

14. The non-transitory tangible computer-readable medium of claim 11, wherein the first radio driver monitors a first bus for the hang condition by the first radio device.

15. The non-transitory tangible computer-readable medium of claim 11, wherein the second radio driver sends the hang condition signal to the second radio device on a second bus.

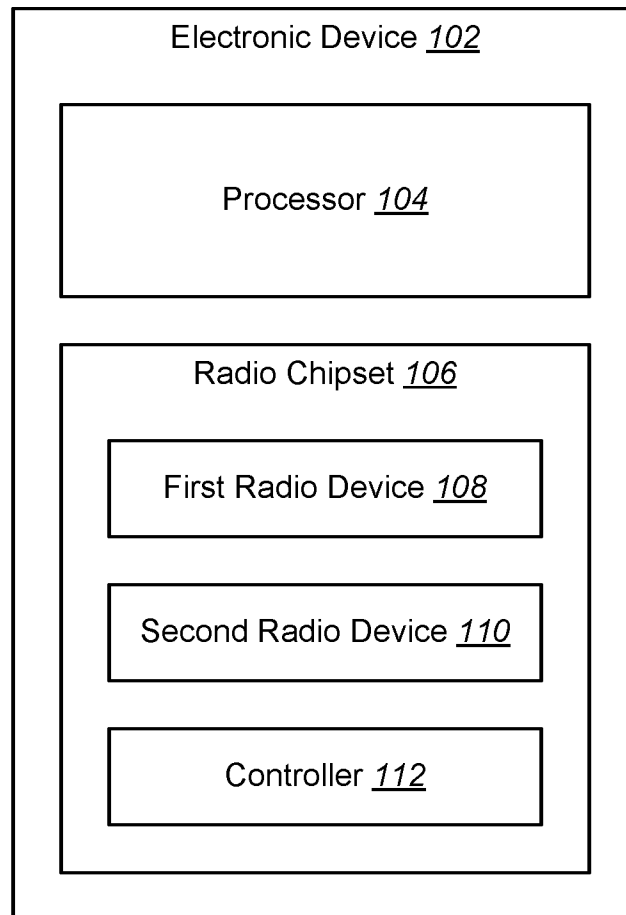
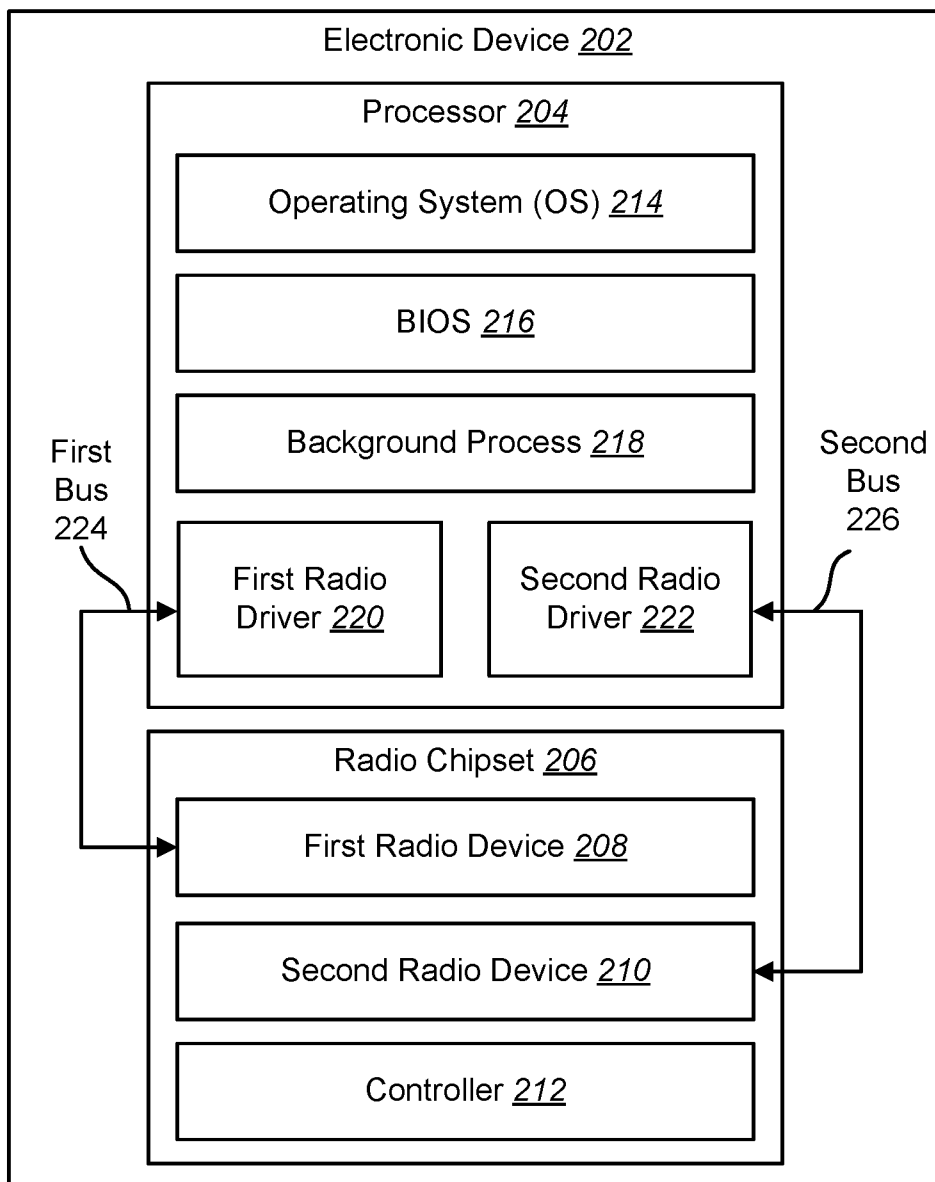


FIG. 1

**FIG. 2**

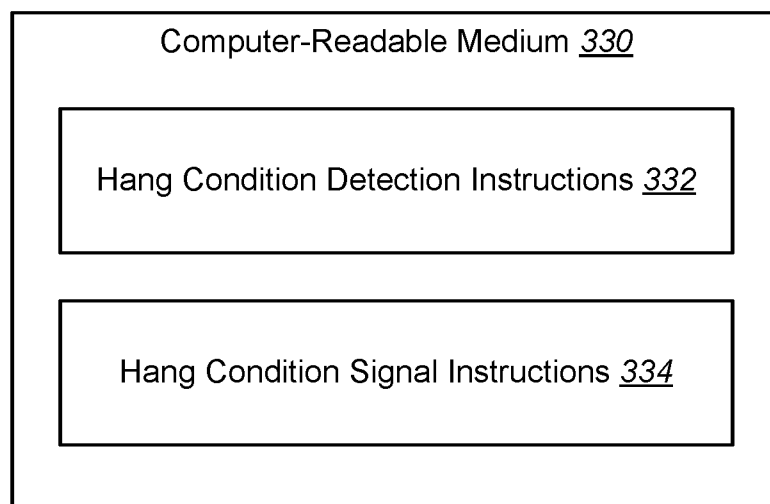


FIG. 3

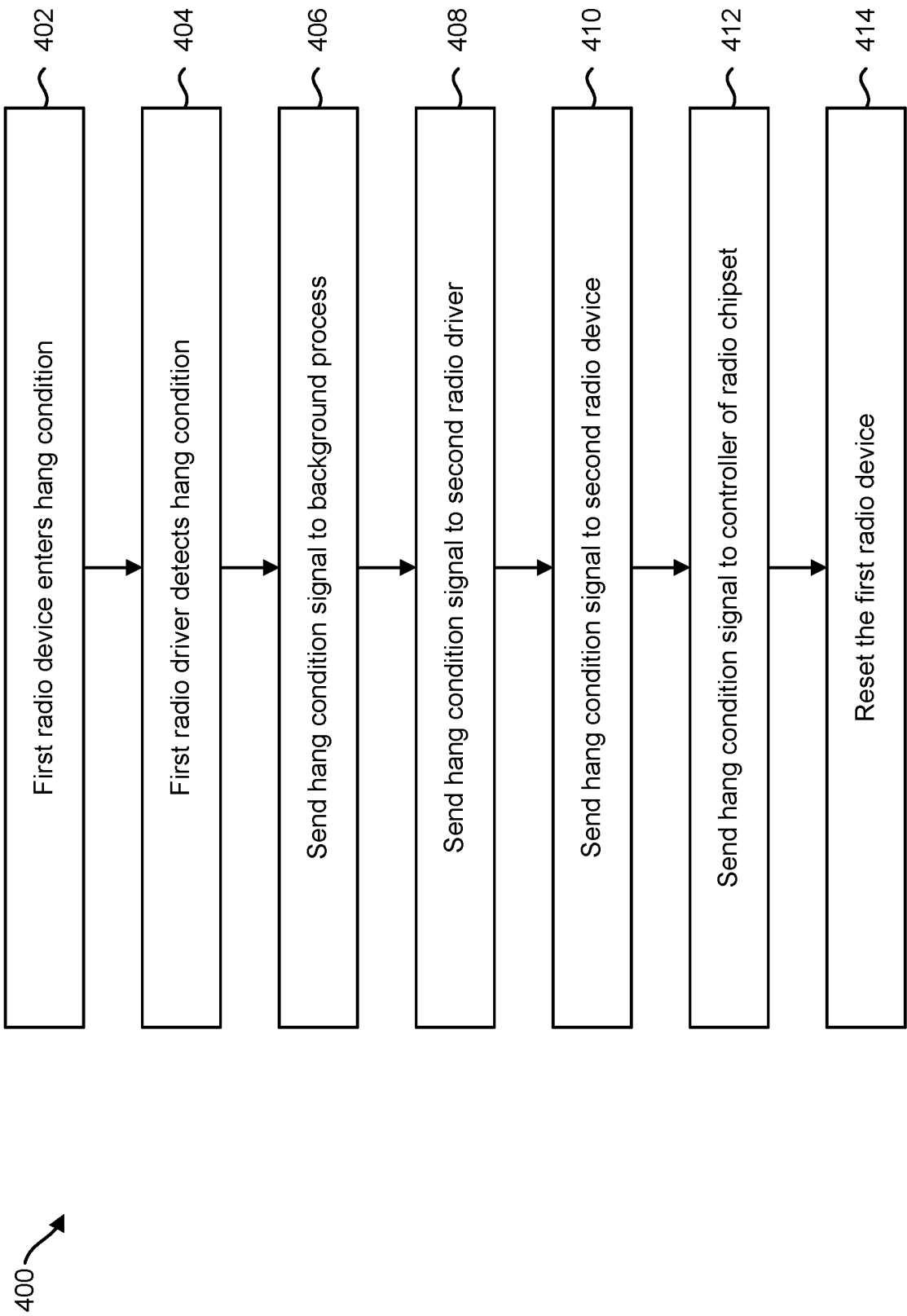


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2020/048514

A. CLASSIFICATION OF SUBJECT MATTER <i>H04B 17/10 (2015.01)</i> <i>G06F 11/00 (2006.01)</i> According to International Patent Classification (IPC) or to both national classification and IPC																
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H04B 17/00-17/10, 1/00-1/44, G06F 11/00, 13/00 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) PatSearch (RUPTO Internal), USPTO, PAJ, Espacenet, Information Retrieval System of FIPS																
C. DOCUMENTS CONSIDERED TO BE RELEVANT																
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.														
Y	US 2007/0238483 A1 (PALM, INC) 11.10.2007, abstract, figures 2-3,10-12, table 5, paragraphs [0018], [0028], [0030], [0035], [0036], [0038], [0041], [0043], [0057], [0081]-[0086], [0099]	1-15														
Y	US 6496890 B1 (MICHAEL JOSEPH AZEVEDO et al.) 17.12.2002, abstract, figure 1, column 7, line 21 - column 8, line 50	1-15														
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