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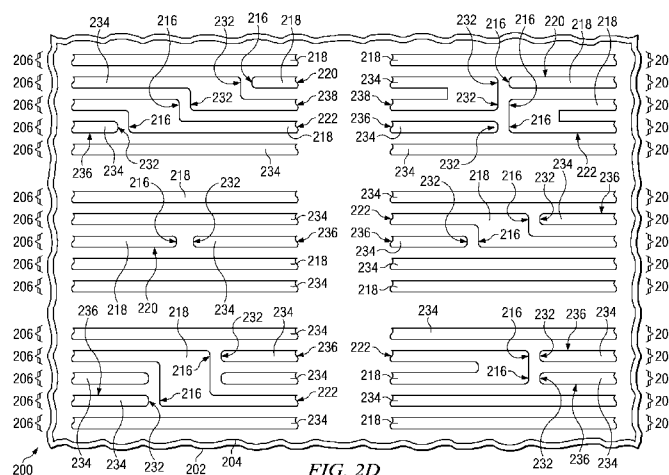
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Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

[Continued on next page]

(54) Title: **PATTERN-SPLIT DECOMPOSITION STRATEGY FOR DOUBLE-PATTERNED LITHOGRAPHY PROCESS**

(57) Abstract: An integrated circuit may be formed by a process of forming a first interconnect pattern (208) in a plurality of parallel route tracks (206), and forming a second interconnect pattern (224) in the plurality of parallel route tracks. The first interconnect pattern (208) includes a first lead pattern which extends to a first point (216) in an instance of the first plurality of parallel route tracks, and the second interconnect pattern (224) includes a second lead pattern which extends to a second point (232) in the same instance of the plurality of parallel route tracks, such that the second point (232) is laterally separated from the first point (216) by a distance one to one and one-half times a space between adjacent parallel lead patterns in the plurality of parallel route tracks. A metal interconnect formation process is performed which forms metal interconnect lines in an interconnect level defined by the first interconnect pattern and the second interconnect pattern.



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PATTERN-SPLIT DECOMPOSITION STRATEGY
FOR DOUBLE-PATTERNED LITHOGRAPHY PROCESS

[0001] This relates to the field of integrated circuits and, more particularly, to photolithography processes for forming integrated circuits.

BACKGROUND

[0002] Integrated circuits may be formed using photolithography processes with illuminations sources having wavelengths more than twice a desired pitch distance of metal interconnect lines in the integrated circuits. Attaining desired tradeoffs between fabrication costs and fabrication yield may be difficult. For example, technology nodes at and beyond the 28 nanometer node using 193 nanometer illumination sources may require more than one pattern step to obtain desired first metal interconnect layouts. Forming crossovers between adjacent parallel route tracks, U-turns and separated lines in the first metal level with desired lateral dimensions may be problematic.

SUMMARY

[0003] An integrated circuit may be formed by a process of forming a first interconnect pattern in a plurality of parallel route tracks, and forming a second interconnect pattern in the plurality of parallel route tracks. The first interconnect pattern includes a first lead pattern which extends to a first point in an instance of the first plurality of parallel route tracks, and the second interconnect pattern includes a second lead pattern which extends to a second point in the same instance of the plurality of parallel route tracks, such that the second point is laterally separated from the first point by a distance of one to one and one-half times a space between adjacent parallel lead patterns in the plurality of parallel route tracks. A metal interconnect formation process is performed which forms metal interconnect lines in an interconnect level defined by the first interconnect pattern and the second interconnect pattern. A first lead and a second lead are formed by the metal interconnect formation process in an area defined by the first lead pattern and an area defined by the second lead pattern, respectively. The first lead and the second lead are laterally separated at the first point and second point by a distance of one to one and one-half of a space between adjacent parallel metal interconnect lines in the plurality of parallel route tracks. The first lead and/or the second

lead may extend out of the route track at the first point and/or the second point, respectively, for example to form a crossover to another route track.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIGS. 1A - 1C depict example illumination sources for photolithographic processes which may be used to form integrated circuits according to embodiments described herein.

[0005] FIGS. 2A - 2E are top views of an integrated circuit formed according a first embodiment using a damascene metal process and an illumination source with a dipole component, depicted in successive stages of fabrication.

[0006] FIGS. 3A - 3D are top views of an integrated circuit formed according a first embodiment using an etched metal process and an illumination source with a dipole component, depicted in successive stages of fabrication.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0007] An integrated circuit may be formed by a process of forming a first interconnect pattern in a plurality of parallel route tracks, and forming a second interconnect pattern in the plurality of parallel route tracks. The first interconnect pattern includes a first lead pattern which extends to a first point in an instance of the first plurality of parallel route tracks, and the second interconnect pattern includes a second lead pattern which extends to a second point in the same instance of the plurality of parallel route tracks, such that the second point is laterally separated from the first point by a distance of one to one and one-half times a space between adjacent parallel lead patterns in the plurality of parallel route tracks. A metal interconnect formation process is performed which forms metal interconnect lines in an interconnect level defined by the first interconnect pattern and the second interconnect pattern. A first lead and a second lead are formed by the metal interconnect formation process in an area defined by the first lead pattern and an area defined by the second lead pattern, respectively. The first lead and the second lead are laterally separated at the first point and second point by a distance of one to one and one-half of a space between adjacent parallel metal interconnect lines in the plurality of parallel route tracks. The first lead and/or the second lead may extend out of the route track at the first point and/or the second point, respectively, for example to form a crossover to another route track.

[0008] FIGS. 1A - 1C depict example illumination sources for photolithographic processes which may be used to form integrated circuits according to embodiments described herein. FIG. 1A depicts an off-axis illumination source with a moderate dipole component; the emitting area is configured in two large dipole regions 100 along the vertical direction and smaller source regions 102 along the horizontal and diagonal directions. FIG. 1B depicts an off-axis illumination source with a strong dipole component; the emitting area is configured in two large dipole regions 104 along the vertical direction and smaller, weaker source regions 106 along the horizontal and diagonal directions. FIG. 1C depicts an off-axis illumination source with a dipole component; the emitting area is configured in two dipole regions 108 along the vertical direction and a distributed annular region 110.

[0009] FIGS. 2A - 2E are top views of an integrated circuit formed according a first embodiment using a damascene metal process and an illumination source with a dipole component, depicted in successive stages of fabrication. The instant embodiment uses an illumination source with a dipole component, for example any of the illuminations sources described in reference to FIGS. 1A - 1C. In FIG. 2A, the integrated circuit 200 is formed in and on a semiconductor substrate 202, which may be, for example, a single crystal silicon wafer, a silicon wafer with silicon-germanium regions, a silicon-on-insulator (SOI) wafer, a hybrid orientation technology (HOT) wafer with regions of different crystal orientations, or other material appropriate for fabrication of the integrated circuit 200.

[0010] A dielectric layer 204 is formed over the substrate 202. The dielectric layer 204 may be a stack of dielectric sub-layers, and may include, for example a pre-metal dielectric (PMD) layer and an inter-level dielectric (ILD) layer. The PMD layer may include a PMD liner, a PMD main layer, and an optional PMD cap layer, not shown. The PMD liner may include silicon nitride or silicon dioxide, 10 to 100 nanometers thick, deposited by plasma enhanced chemical vapor deposition (PECVD) on an existing top surface of the integrated circuit 200. The PMD main layer may be a layer of silicon dioxide formed by a high aspect ration process (HARP) followed by a layer of silicon dioxide, phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG), commonly 100 to 1000 nanometers thick, deposited by a PECVD process on a top surface of the

PMD liner, and sometimes leveled by a chemical-mechanical polish (CMP) process. The optional PMD cap layer is commonly 10 to 100 nanometers of a hard material such as silicon nitride, silicon carbide nitride or silicon carbide, formed on a top surface of the PMD main layer.

[0011] The ILD layer may include, for example, an etch stop layer of 5 to 25 nanometers of silicon nitride, silicon carbide, or silicon carbide nitride, a main layer of 100 to 200 nanometers of low-k dielectric material such as organosilicate glass (OSG), carbon-doped silicon oxides (SiCO or CDO) or dielectric material formed from methylsilsequioxane (MSQ), or possibly ultra low-k dielectric material such as porous OSG (p-OSG), and a cap layer of 10 to 40 nanometers of silicon nitride, silicon carbide nitride or silicon carbide.

[0012] Areas for a plurality of parallel route tracks 206 are defined over the integrated circuit 200. A first interconnect pattern 208, depicted in FIG. 2A with a stipple pattern, is formed of photoresist over the dielectric layer 204 which creates a first plurality of exposed areas 210. The first interconnect pattern 208 is formed using an illumination source with a dipole component oriented perpendicular to the parallel route tracks 206. The first plurality of exposed areas 210 includes a first plurality of terminating lead patterns 212 which extend to, and terminate at, instances of a first point 216 in instances of the route tracks 206 and a first plurality of branching lead patterns 214 which extend to, and branch at, instances of the first point 216 in instances of the route tracks 206. In the instant embodiment, due to the dipole component of the illumination sources used in the photolithography process to produce the first interconnect pattern 208, a resolvable pitch distance of the first interconnect pattern 208 in a direction parallel to the parallel route tracks 206 is at least two times a pitch distance of the parallel route tracks 206. A first instance of the first plurality of exposed areas 210 in a first instance of the plurality of parallel route tracks 206 may be disposed immediately adjacent to a second instance of the first plurality of exposed areas 210 in a second instance of the plurality of parallel route tracks 206 immediately adjacent to the first instance of the plurality of parallel route tracks 206 as depicted in FIG. 2A. In one version of the instant embodiment, the illumination source may provide 193 nanometer radiation, and the pitch distance of the parallel route tracks 206 may be 75 to 81 nanometers. In one version of

the instant embodiment, the first interconnect pattern 208 may be formed of novolak resin based photoresist and developed using a positive tone develop process such as exposure to an alkaline aqueous developing solution. In another version, the first interconnect pattern 208 may be formed of photoresist and developed using a negative tone develop process.

[0013] Referring to FIG. 2B, a first interconnect trench etch process is performed which removes dielectric material from the dielectric layer 204 in the first plurality of exposed areas 210 to form a first plurality of interconnect trenches 218, including a first plurality of terminating lead trenches 220 which extend to, and terminate at, instances of the first point 216 in instances of the parallel route tracks 206 and a first plurality of branching lead trenches 222 which extend to, and branch at, instances of the first point 216 in instances of the route tracks 206. The first interconnect pattern 208 is removed after the first interconnect trench etch process is completed, for example by exposing the integrated circuit 200 to an oxygen containing plasma, followed by a wet cleanup to remove any organic residue from the top surface of the dielectric layer 204.

[0014] Referring to FIG. 2C, a second interconnect pattern 224, depicted in FIG. 2C with a stipple pattern, is formed of photoresist over the dielectric layer 204 which creates a second plurality of exposed areas 226. The second interconnect pattern 224 is formed with an illumination source having a substantially equal dipole component as the illumination source used to form the first interconnect pattern 208, and the dipole component is oriented perpendicular to the parallel route tracks 206. An instance of the second plurality of exposed areas 226 may be disposed immediately adjacent to an instance of the first plurality of interconnect trenches 218 as depicted in FIG. 2C. The second plurality of exposed areas 226 includes a second plurality of terminating lead patterns 228 which extend to, and terminate at, instances of a second point 232 proximate to corresponding instances of the first point 216 in instances of the route tracks 206 and a second plurality of branching lead patterns 230 which extend to, and branch at, instances of the second point 232 proximate to corresponding instances of the first point 216 in instances of the route tracks 206. Each instance of the second point 232 may be laterally separated from the corresponding instance of the first point 216 by a lateral distance of one to one and one-half times a space between adjacent parallel instances of the first

plurality of exposed areas 210 and the second plurality of exposed areas 226 in the parallel route tracks 206.

[0015] Referring to FIG. 2D, a second interconnect trench etch process is performed which removes dielectric material from the dielectric layer 204 in the second plurality of exposed areas 226 to form a second plurality of interconnect trenches 234, including a second plurality of terminating trenches 236 which extend to, and terminate at, instances of the second point 232 proximate to corresponding instances of the first point 216 in instances of the route tracks 206 and a second plurality of branching trenches 238 which extend to, and branch at, instances of the second point 232 proximate to corresponding instances of the first point 216 in instances of the route tracks 206. The second interconnect pattern 224 is removed after the second interconnect trench etch process is completed, for example as described in reference to FIG. 2B.

[0016] Referring to FIG. 2E, a damascene metal interconnect formation process is performed which forms metal interconnect lines 240 in the first plurality of interconnect trenches 218 and the second plurality of interconnect trenches 234. The metal interconnect lines 240 are depicted in FIG. 2E with a star hatch pattern. The damascene metal interconnect formation process may include, for example, forming a tantalum nitride liner 1 to 5 nanometers thick in the first plurality of interconnect trenches 218 and the second plurality of interconnect trenches 234 by an atomic layer deposition (ALD) process, forming a copper seed layer 5 to 80 nanometers thick on the liner by sputtering, electroplating copper on the seed layer so as to fill the first plurality of interconnect trenches 218 and the second plurality of interconnect trenches 234, and subsequently removing copper and liner metal from a top surface of the dielectric layer 204 by a copper CMP process.

[0017] The metal interconnect lines 240 include a first plurality of terminating lines 242, formed in the first plurality of terminating lead trenches 220, which extend to, and terminate at, instances of the first point 216 in instances of the route tracks 206, and a first plurality of branching lines 244, formed in the first plurality of branching lead trenches 222, which extend to, and branch at, instances of the first point 216 in instances of the route tracks 206. The metal interconnect lines 240 further include a second plurality of terminating lines 246, formed in the second plurality of terminating trenches

236, which extend to, and terminate at, instances of the second point 232 proximate to corresponding instances of the first point 216 in instances of the route tracks 206, and a second plurality of branching lines 248, formed in the second plurality of branching trenches 238, which extend to, and branch at, instances of the second point 232 proximate to corresponding instances of the first point 216 in instances of the route tracks 206. Instances of the second plurality of terminating lines 246 may be laterally separated at corresponding instances of the second point 232 from laterally adjacent instances of the first plurality of terminating lines 242 at corresponding instances of the first point 216 by a lateral distance of one to one and one-half times a space between adjacent parallel instances of the metal interconnect lines 240 in the parallel route tracks 206.

[0018] FIGS. 3A - 3D are top views of an integrated circuit formed according a first embodiment using an etched metal process and an illumination source with a dipole component, depicted in successive stages of fabrication. The instant embodiment uses an illumination source with a dipole component, for example any of the illuminations sources described in reference to FIGS. 1A - 1C. In FIG. 3A, the integrated circuit 300 is formed in and on a semiconductor substrate 302 as described in reference to FIG. 2A. A dielectric layer 304 is formed over the substrate 302, as described in reference to FIG. 2A. Areas for a plurality of parallel route tracks 306 are defined over the integrated circuit 300. An interconnect metal layer 308 is formed over the dielectric layer 304. The interconnect metal layer 308 may include, for example, an adhesion layer of titanium tungsten or titanium nitride 3 to 15 nanometers thick formed by a metal organic chemical vapor deposition (MOCVD) process, a sputtered aluminum layer with 0.5 to 2 percent copper, silicon and/or titanium 100 to 200 nanometers thick, and a titanium nitride cap layer 5 to 20 nanometers thick formed by an MOCVD process.

[0019] A first interconnect pattern 310, depicted in FIG. 3A with a stipple pattern, is formed of photoresist over the interconnect metal layer 308 which creates a first plurality of masked areas 312. The first interconnect pattern 310 is formed using an illumination source with a dipole component oriented perpendicular to the parallel route tracks 306. The first plurality of masked areas 312 includes a first plurality of terminating lead patterns 314 which extend to, and terminate at, instances of a first point 318 in instances of the route tracks 306 and a first plurality of branching lead patterns 316

which extend to, and branch at, instances of the first point 318 in instances of the route tracks 306. In the instant embodiment, due to the dipole component of the illumination sources used in the photolithography process to produce the first interconnect pattern 310, a resolvable pitch distance of the first interconnect pattern 310 in a direction parallel to the parallel route tracks 306 is at least two times a pitch distance of the parallel route tracks 306. A first instance of the first plurality of masked areas 312 in a first instance of the plurality of parallel route tracks 306 may be disposed immediately adjacent to a second instance of the first plurality of masked areas 312 in a second instance of the plurality of parallel route tracks 306 immediately adjacent to the first instance of the plurality of parallel route tracks 306 as depicted in FIG. 3A. In one version of the instant embodiment, the illumination source may provide 193 nanometer radiation, and the pitch distance of the parallel route tracks 306 may be 75 to 81 nanometers. The first interconnect pattern 310 may be formed using a positive tone develop process or a negative tone develop process, as described in reference to FIG. 2A.

[0020] Referring to FIG. 3B, a resist freeze process is performed which hardens the first interconnect pattern 310 so as to allow a second photoresist pattern to be formed on the integrated circuit 300. The first interconnect pattern 310 after completion of the resist freeze process is depicted in FIG. 3B with a coarse stipple pattern. The litho freeze process may include, for example, an ultraviolet (UV) cure step, a thermal cure step and/or a chemical cure step.

[0021] Referring to FIG. 3C, a second interconnect pattern 320, depicted in FIG. 3C with a stipple pattern, is formed of photoresist over the interconnect metal layer 308 which creates a second plurality of masked areas 322. The second interconnect pattern 320 is formed with an illumination source having a substantially equal dipole component as the illumination source used to form the first interconnect pattern 310, and the dipole component is oriented perpendicular to the parallel route tracks 306. A first instance of the second plurality of masked areas 322 in a first instance of the plurality of parallel route tracks 306 may be disposed immediately adjacent to a second instance of the second plurality of masked areas 322 in a second instance of the plurality of parallel route tracks 306 immediately adjacent to the first instance of the plurality of parallel route tracks 306 as depicted in FIG. 3C. The second plurality of masked areas 322 includes a

second plurality of terminating lead patterns 324 which extend to, and terminate at, instances of a second point 328 proximate to corresponding instances of the first point 318 in instances of the route tracks 306 and a second plurality of branching lead patterns 326 which extend to, and branch at, instances of the second point 328 proximate to corresponding instances of the first point 318 in instances of the route tracks 306. Each instance of the second point 328 is laterally separated from the corresponding instance of the first point 318 by a lateral distance of one to one and one-half times a space between adjacent parallel instances of the first plurality of masked areas 312 and the second plurality of masked areas 322 in the parallel route tracks 306.

[0022] Referring to FIG. 3D, a metal etch process is performed which removes metal from the interconnect metal layer 308 outside of the first interconnect pattern 310 and the second interconnect pattern 320 so as to form metal interconnect lines 330, depicted in FIG. 3D with a star hatch pattern. The metal etch process may include, for example an RIE step with a chlorine-containing plasma to etch the aluminum. The metal interconnect lines 330 are disposed in an interconnect level of the integrated circuit 300 defined by the first interconnect pattern 310 and the second interconnect pattern 320.

[0023] The metal interconnect lines 330 include a first plurality of terminating lines 332, formed in areas defined by the first plurality of terminating lead patterns 314, which extend to, and terminate at, instances of the first point 318 in instances of the route tracks 306, and a first plurality of branching lines 334, formed in the first plurality of branching lead patterns 316, which extend to, and branch at, instances of the first point 318 in instances of the route tracks 306. The metal interconnect lines 330 further include a second plurality of terminating lines 336, formed in areas defined by the second plurality of terminating lead patterns 324, which extend to, and terminate at, instances of the second point 328 proximate to corresponding instances of the first point 318 in instances of the route tracks 306, and a second plurality of branching lines 338, formed in areas defined by the second plurality of branching lead patterns 326, which extend to, and branch at, instances of the second point 328 proximate to corresponding instances of the first point 318 in instances of the route tracks 306. Instances of the second plurality of terminating lines 336 may be laterally separated at corresponding instances of the second point 328 from laterally adjacent instances of the first plurality of terminating lines 332 at

corresponding instances of the first point 318 by a lateral distance of one to one and one-half times a space between adjacent parallel instances of the metal interconnect lines 330 in the parallel route tracks 306.

[0024] Those skilled in the art will appreciate that modifications may be made to the described example embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. A process of forming an integrated circuit, comprising the steps of:
forming a dielectric layer over a substrate;
defining areas for a plurality of parallel route tracks on a top surface of said dielectric layer, said plurality of parallel route tracks having a pitch distance;
forming a first interconnect pattern creating a plurality of first exposed areas including a first lead pattern, wherein said first lead pattern is located in an instance of said plurality of parallel route tracks;
performing a first trench etch process to form a plurality of first interconnect trenches in said plurality of first exposed areas;
forming a second interconnect pattern creating a plurality of second exposed areas including a second lead pattern, wherein said second lead pattern is located in said instance of said plurality of parallel route tracks, wherein said second lead pattern is separated from said first lead pattern by a distance of one to one and one-half times a space between said first lead pattern and an adjacent lead pattern located in an adjacent instance of said plurality of parallel route tracks;
wherein said first interconnect pattern and said second interconnect pattern are formed using two distinct photolithography processes having a dipole illumination source;
performing a second trench etch process to form a plurality of second interconnect trenches in said plurality of second exposed areas; and
forming metal interconnect lines in said first interconnect trenches and said second interconnect trenches.
2. The process of claim 1, in which said first lead pattern terminates adjacent to said second lead pattern.
3. The process of claim 1, in which said first lead pattern branches adjacent to said second lead pattern.

4. The process of claim 1, in which said dipole illumination source provides 193 nanometer radiation; and said pitch distance of said plurality of parallel route tracks is 75 to 81 nanometers.

5. A process of forming an integrated circuit, comprising the steps of:
forming a dielectric layer over a substrate;
defining a plurality of parallel route tracks on a top surface of said dielectric layer, said plurality of parallel route tracks having a pitch distance;
forming a first interconnect pattern in said plurality of parallel route tracks including a first lead pattern located in a route track of said plurality of parallel route tracks;
forming a second interconnect pattern in said plurality of parallel route tracks including a second lead pattern located in said route track, wherein said second lead pattern is separated from said first lead pattern in said route track by a distance of one to one and one-half times a space between interconnect patterns in adjacent instances of said plurality of parallel route tracks;
wherein said first interconnect pattern and said second interconnect pattern are formed using two distinct photolithography processes which have dipole illumination sources capable of resolving said interconnect patterns in adjacent instances of said plurality of parallel route tracks; and
forming metal interconnect lines in said dielectric layer as defined by said first interconnect pattern and said second interconnect pattern.

6. The process of claim 5, in which said dipole illumination source provides 193 nanometer radiation; and said pitch distance of said parallel route tracks is 75 to 81 nanometers.

7. A process of forming an integrated circuit, comprising the steps of:
- forming a dielectric layer over a substrate;
 - defining areas for a plurality of parallel route tracks on a top surface of said dielectric layer, said plurality of parallel route tracks having a pitch distance;
 - forming a first interconnect pattern over said dielectric layer, said first interconnect pattern creating a first plurality of lead patterns which extend to instances of a first point in instances of said parallel route tracks;
 - performing a first trench etch process to form a first plurality of interconnect trenches using said first interconnect pattern;
 - forming a second interconnect pattern over said dielectric layer, said second interconnect pattern creating a second plurality of lead patterns which extend to instances of a second point in said instances of said parallel route tracks, in which each instance of said second point is laterally separated from a corresponding instance of said first point by a distance of one to one and on-half times a space between adjacent parallel instances of said first plurality of exposed areas and the second plurality of exposed areas in said parallel route tracks;
 - wherein said first interconnect pattern and said second interconnect pattern are formed using two distinct photolithography processes having a dipole illumination source;
 - performing a second trench etch process to form a second plurality of interconnect trenches using said second interconnect pattern; and
 - forming metal interconnect lines in said first plurality of interconnect trenches and said second plurality of interconnect trenches, said metal interconnect lines including:
 - a first plurality of lines, which extend to instances of said first point in instances of said parallel route tracks; and
 - a second plurality of lines, which extend to instances of said second point proximate to corresponding instances of said first point in instances of said route tracks.

8. The process of claim 1, in which a subset of said first plurality of lines terminate at said instances of said first point.

9. The process of claim 1, in which a subset of said first plurality of lines branch at said instances of said first point.

10. The process of claim 1, in which said dipole illumination source provides 193 nanometer radiation; and said pitch distance of plurality of said parallel route tracks is 75 to 81 nanometers.

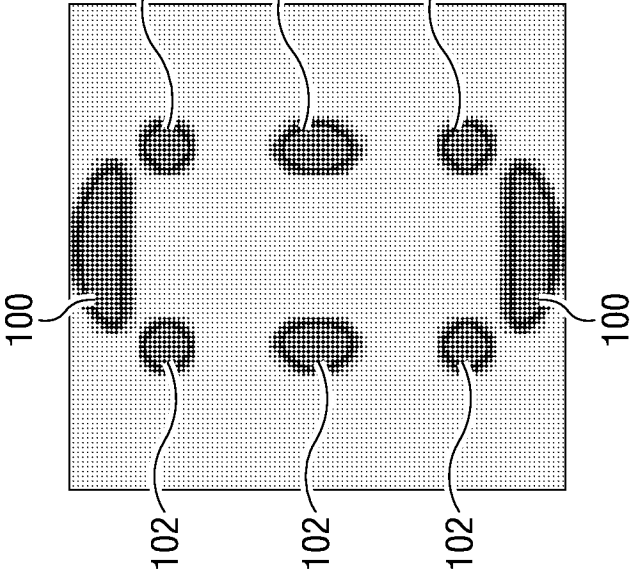


FIG. 1A

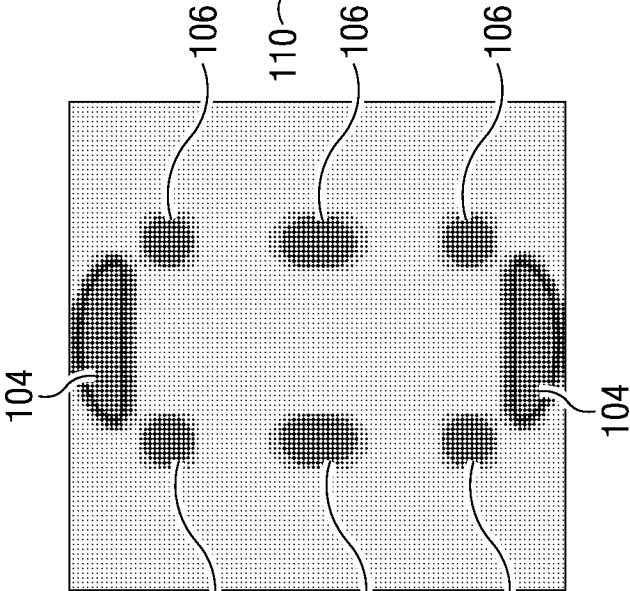


FIG. 1B

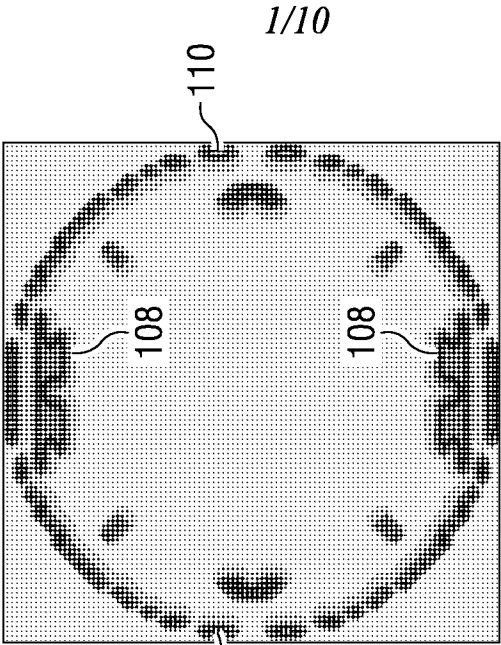
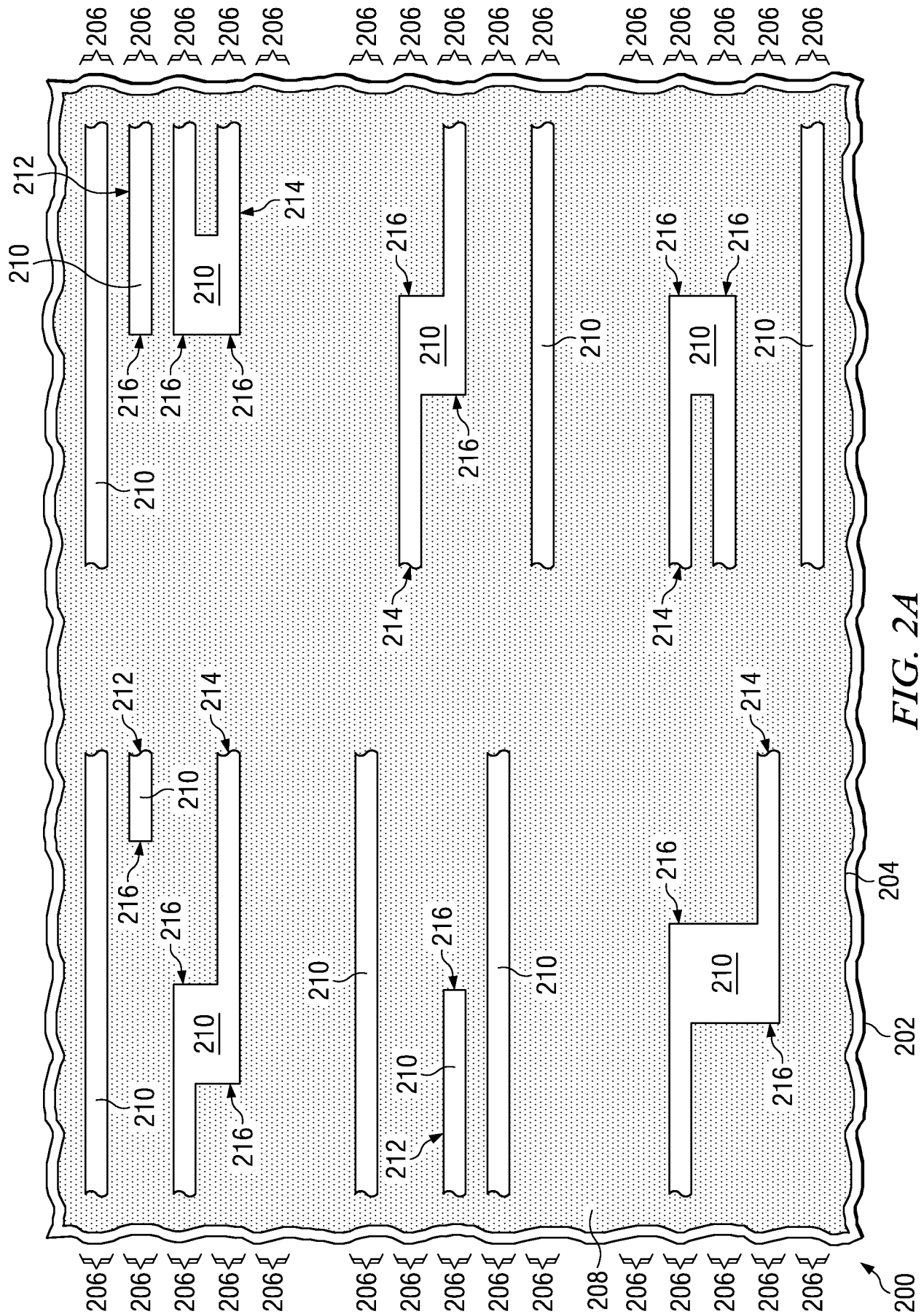


FIG. 1C



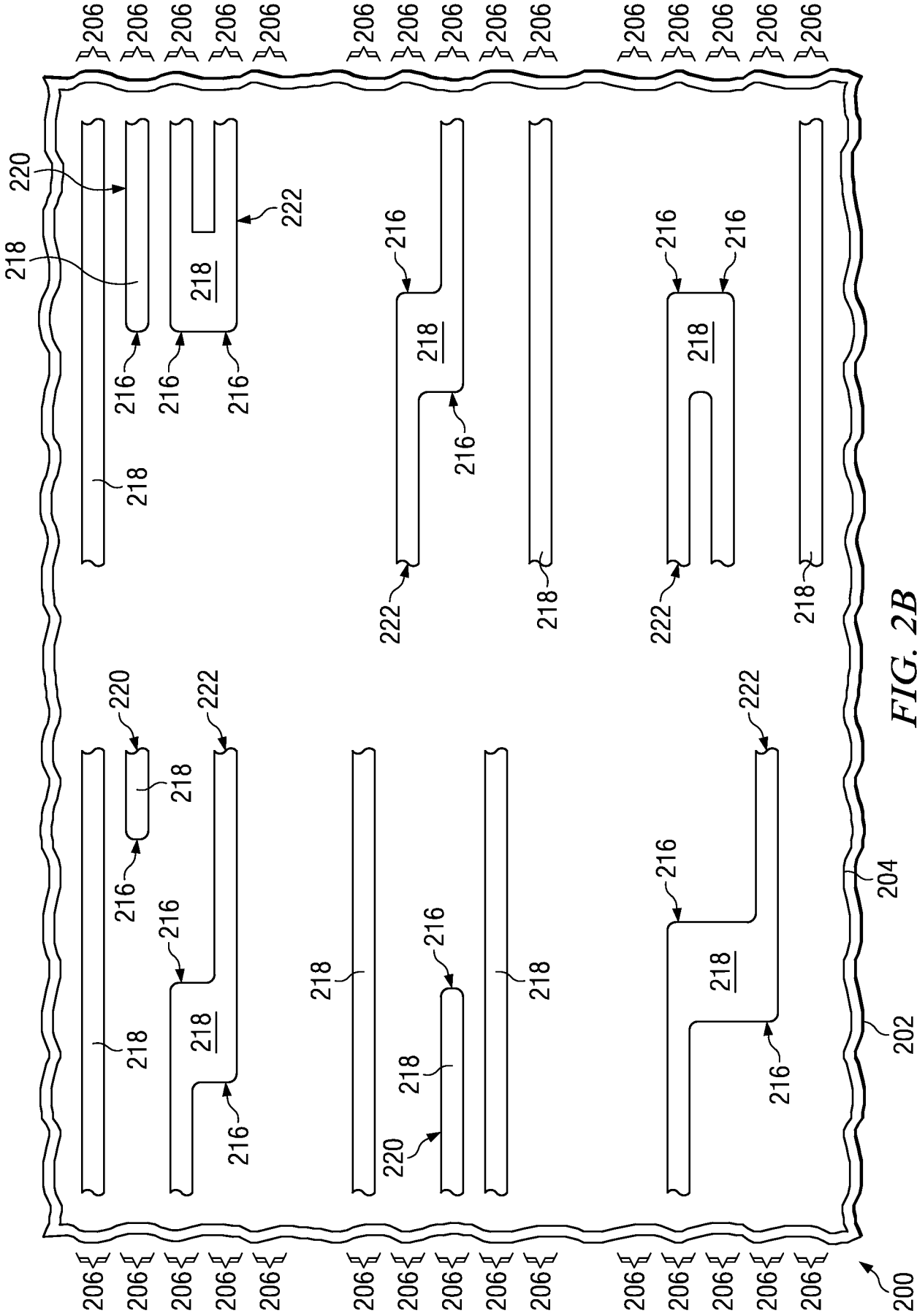


FIG. 2B

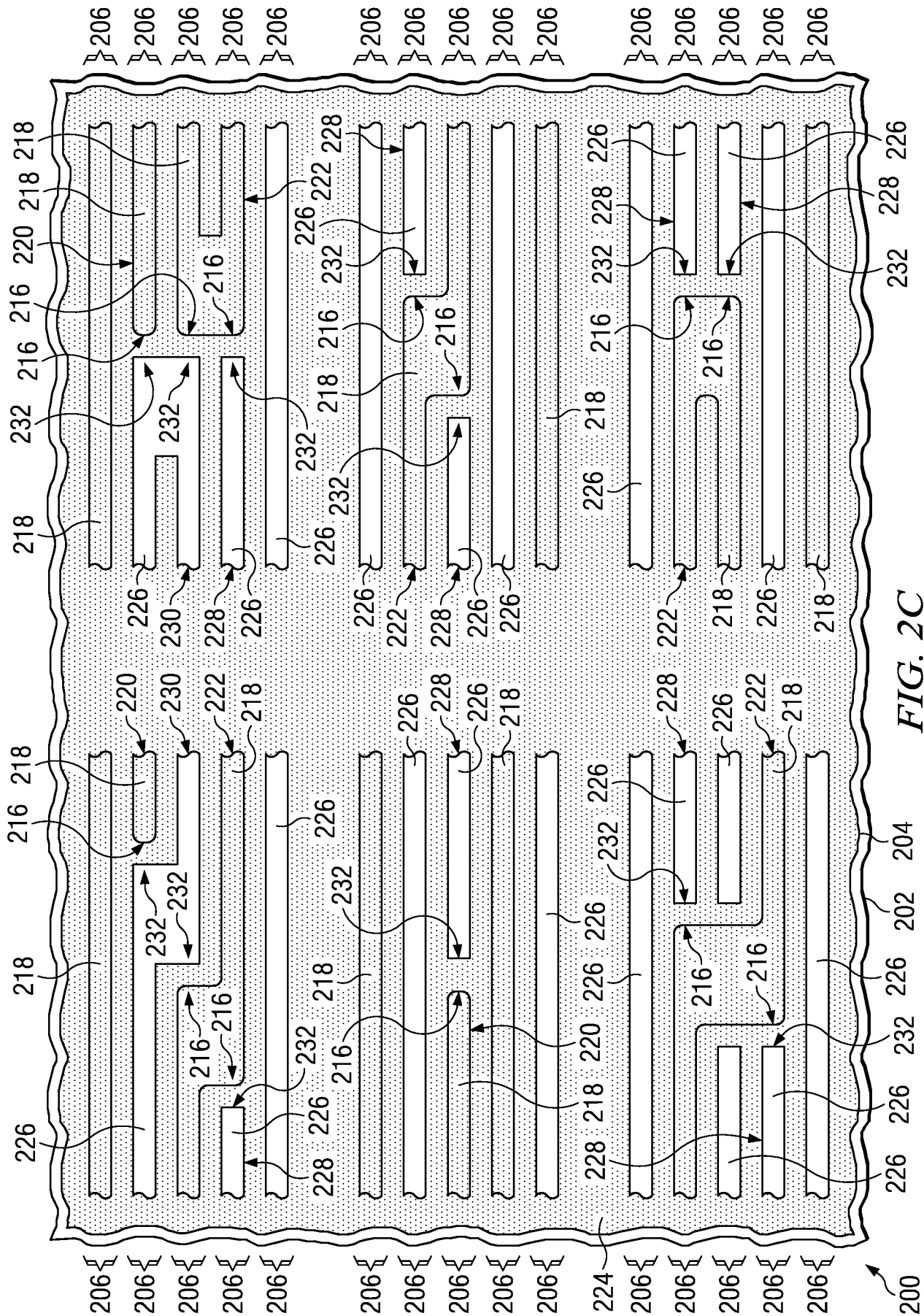
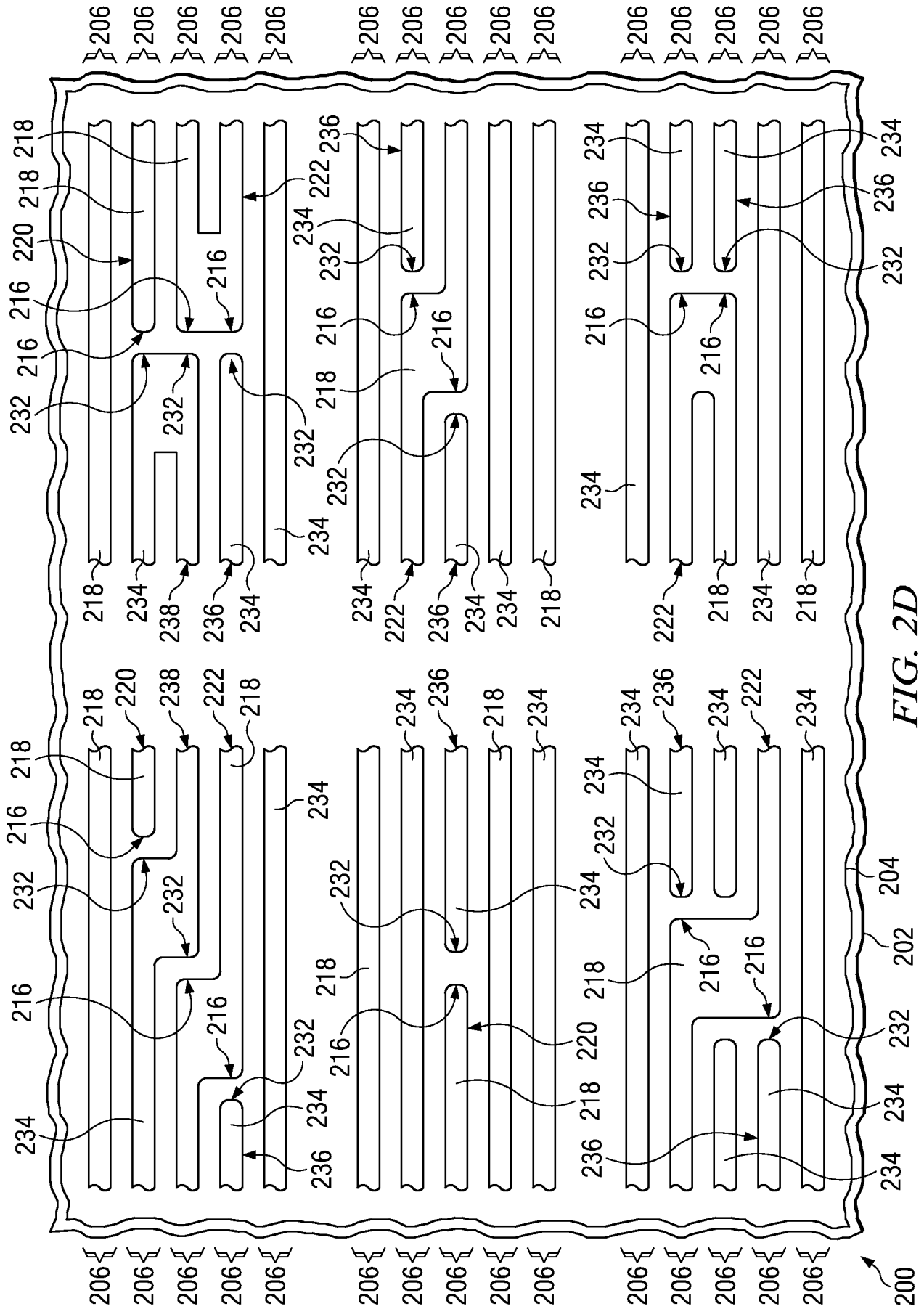


FIG. 2C



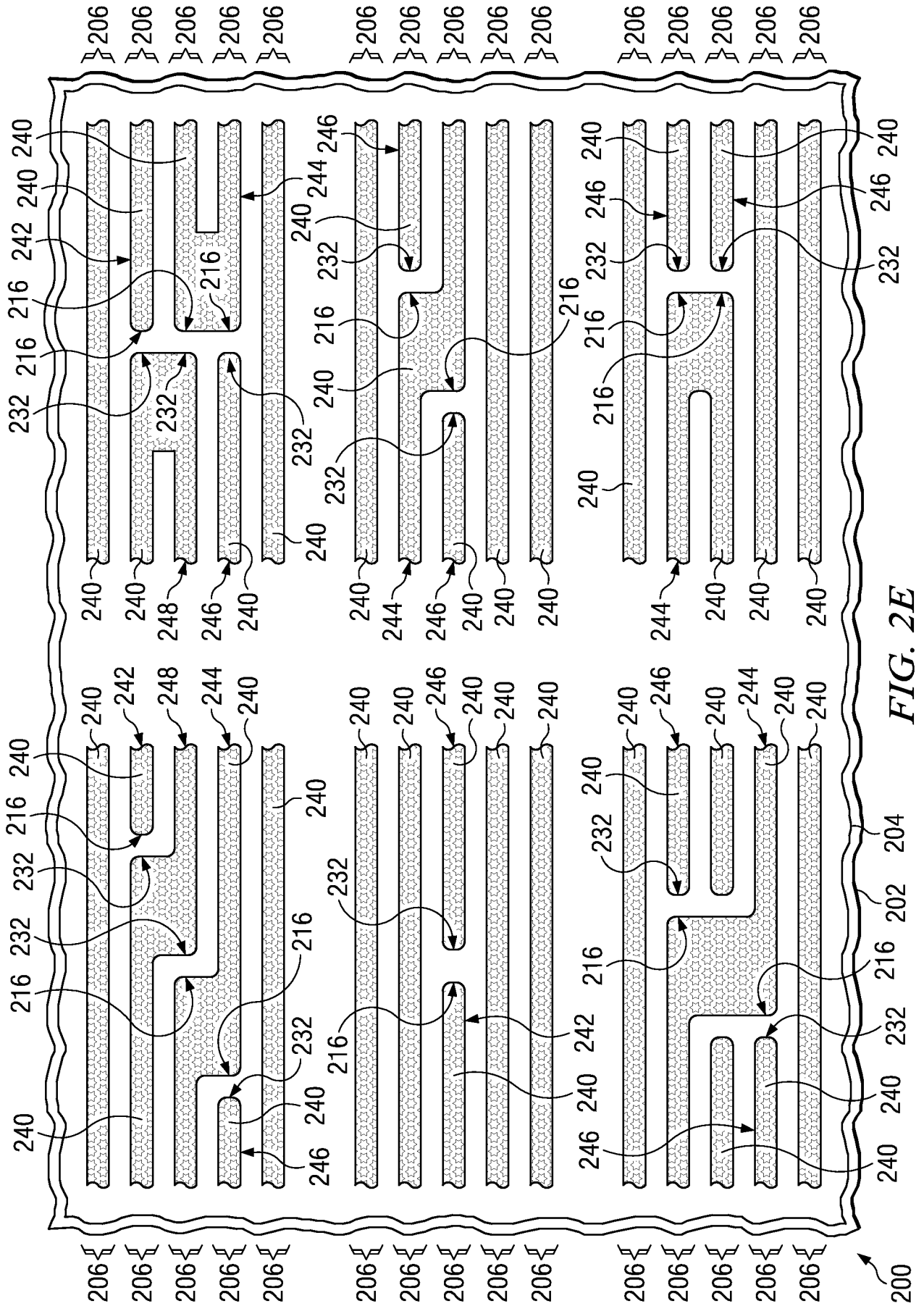


FIG. 2E

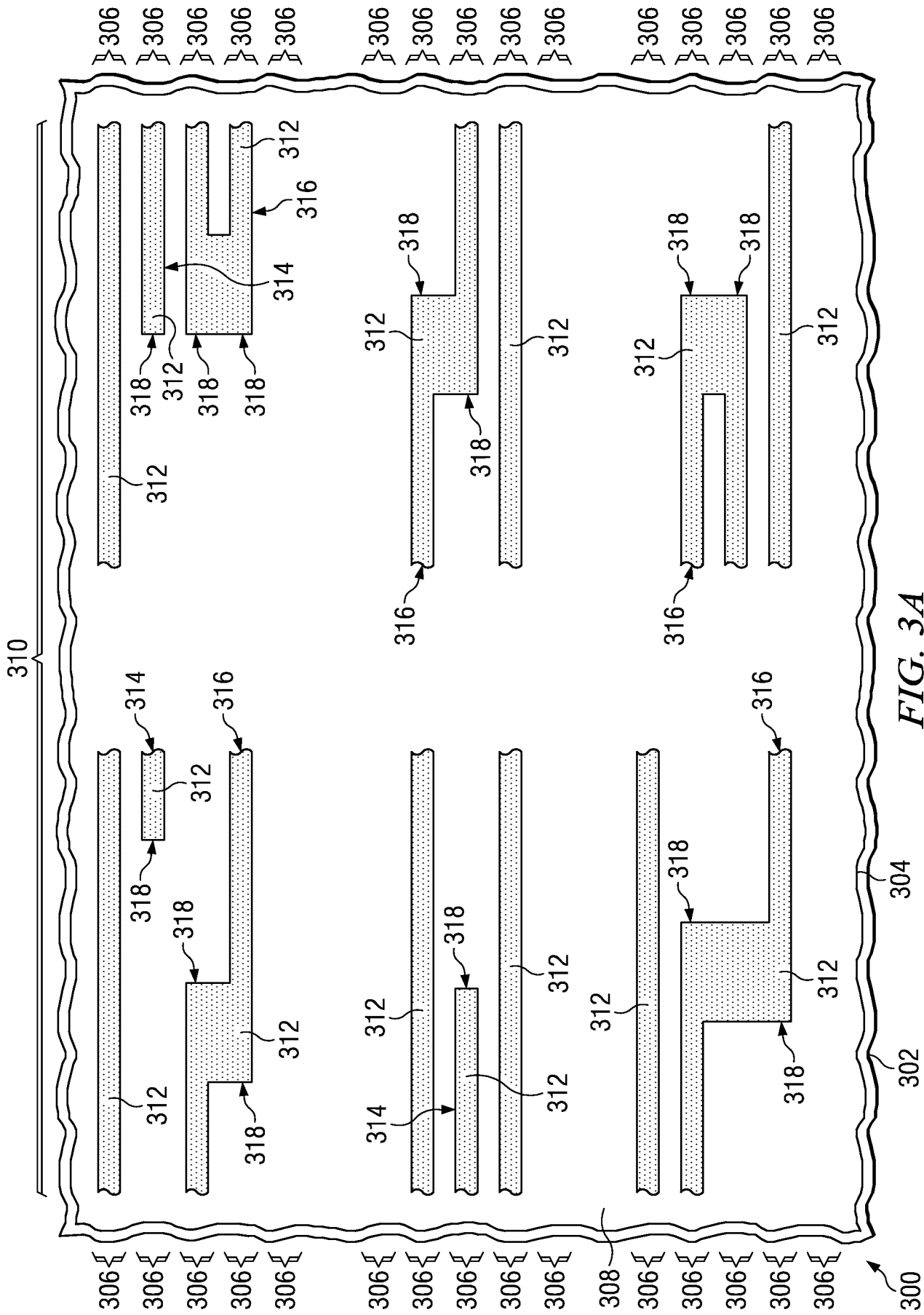
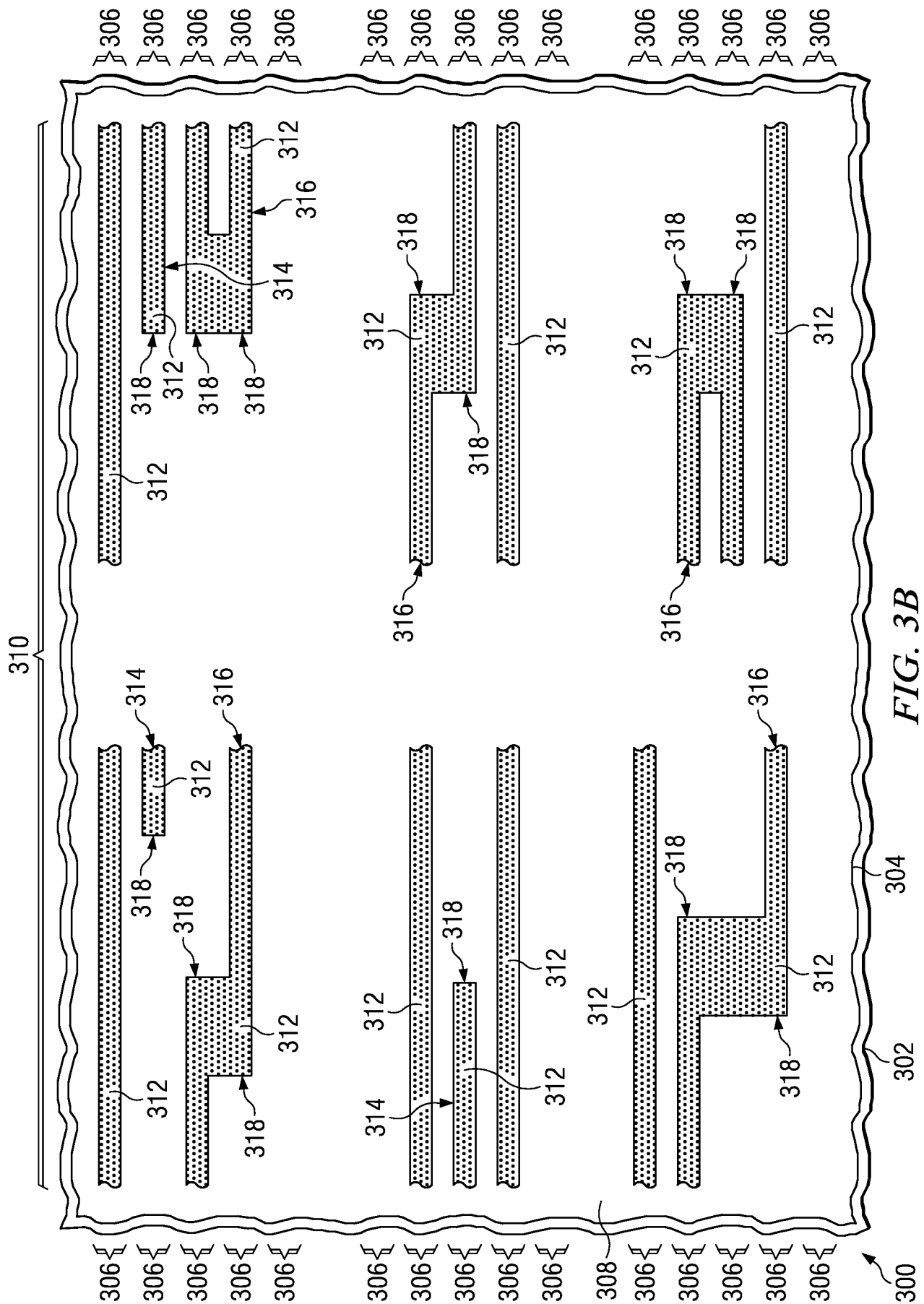


FIG. 3A



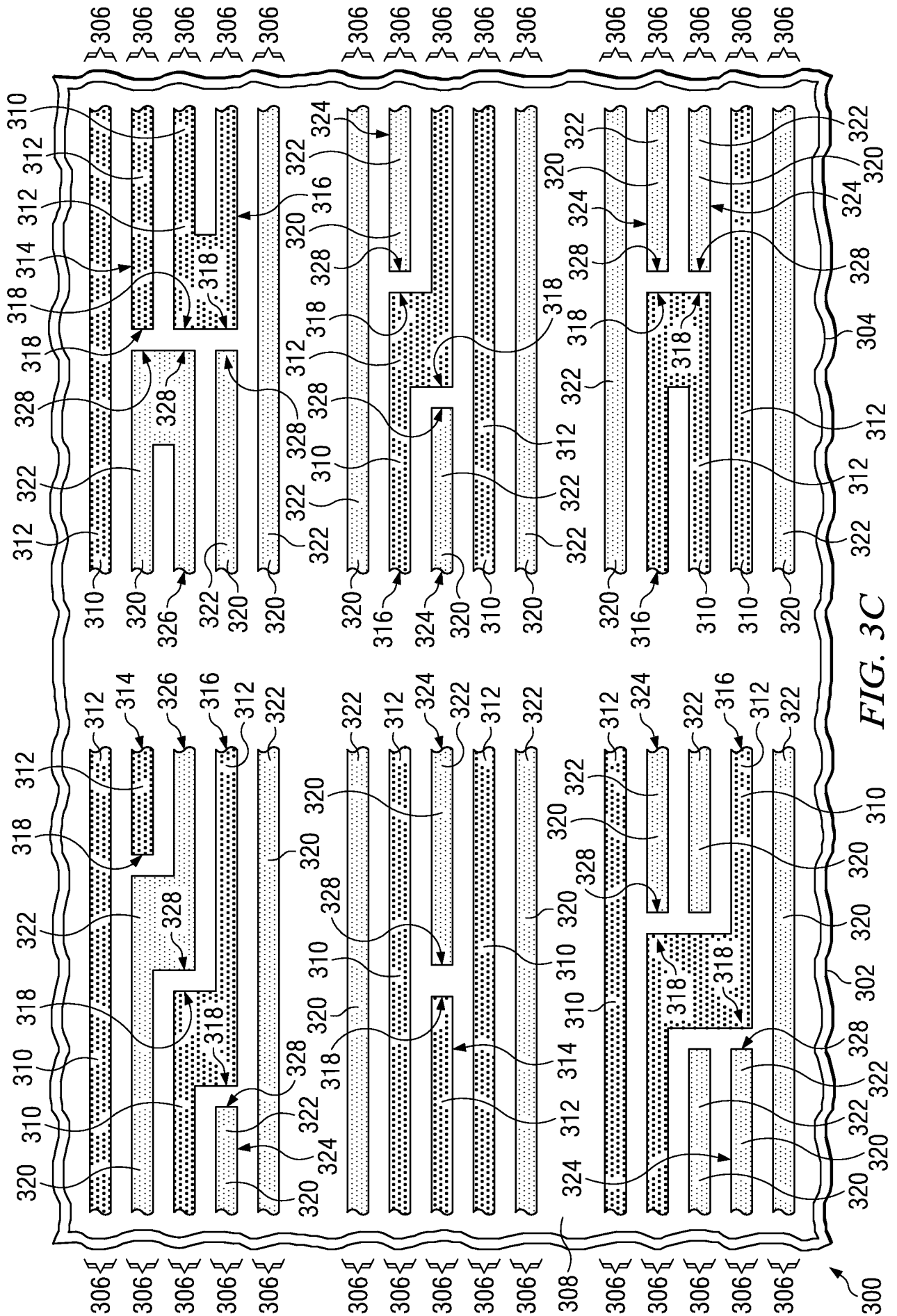


FIG. 3C

