(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 January 2004 (22.01.2004)

PCT

(10) International Publication Number
WO 2004/008633 A2

(51) International Patent Classification[7]: H03G

(21) International Application Number:
PCT/IB2003/003047

(22) International Filing Date: 1 July 2003 (01.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02015376.3 10 July 2002 (10.07.2002) EP

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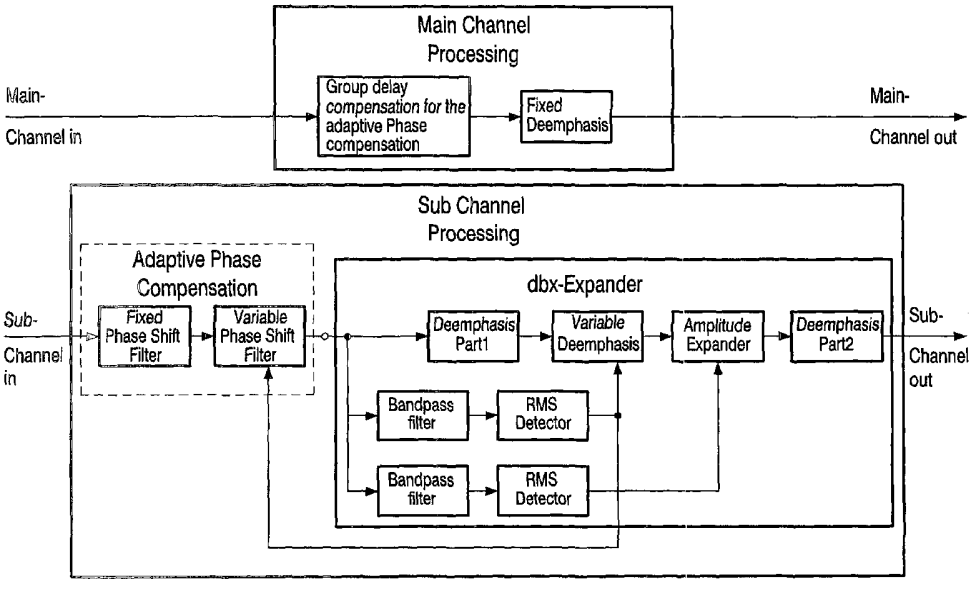
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

[Continued on next page]

(54) **Title:** A STEREO SIGNAL PROCESSING APPARATUS



(57) **Abstract:** Disclosed is a stereo signal processing apparatus, in particular for a digital BTSC television decoder, comprising a sub-channel signal processing section which comprises an input for inputting an input sub-channel signal, a DBX expanding means and an output for outputting an output sub-channel signal. The particularity of the present invention is that said sub-channel signal processing section further comprises a phase error compensating means for correcting a phase error of said DBX expanding means so that at said output of said sub-channel signal processing section the phase of the output sub-channel signal is essentially constant or zero over a predetermined frequency range.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A stereo signal processing apparatus

The present invention relates to a stereo signal processing apparatus, in particular for a digital BTSC television decoder, comprising a sub-channel signal processing section which comprises an input for inputting an input sub-channel signal, a DBX expanding means and an output for outputting an output sub-channel signal.

Such an apparatus provides a channel separation during stereo transmission of audio signals so as to reconstruct the original L (left) and R (right) audio signals wherein the sub-channel signal is the stereo audio difference signal (L-R) which is processed in addition to a main channel signal which is the sum stereo audio signal (L+R).

Such a stereo signal processing apparatus is particularly used in BTSC decoders for television, video tape recorders and other multimedia devices operating under the BTSC television standard. The DBX expanding means is provided for decoding the sub-channel signal which is encoded in accordance with the BTSC multichannel sound system standard including DBX companding.

US 5,373,562 A discloses a signal processor for stereo signals wherein an expander circuit is provided for decoding audio signals which were encoded in accordance with the BTSC multichannel sound system standard including DBX companding. A wideband expander circuit is utilized and a DBX expander can be accommodated. The wideband expander circuit is provided with a signal path having an input low pass filter, a stereo difference signal (L-R) demodulator, a second low pass filter, and a voltage controlled amplifier, the gain of which is controlled by a control signal derived from the demodulated difference signal which has been operated on by a bandpass filter and an integrating peak detector. The output of the voltage controlled amplifier is provided to a de-emphasis network before being fed to a decoder matrix for combining with the sum stereo signal (L+R) for reconstructing the original L and R signals. When a DBX expander is connected, the DBX expander is substituted in place of the de-emphasis network, the voltage controlled amplifier control signal, which

provides the wideband expansion, is overridden by a predetermined voltage, the bandpass filtering characterristic of the bandpass filter is disabled, and the input is switched to bypass the input low pass filter. The disablement of the bandpass filter filtering characteristics actuates the switching of the input to bypass the input low pass filter.

Similar circuits are described in EP 0 584 718 A2 and EP 1 083 656 A2.

However, it has been observed that in the conventional stereo signal processing apparatus the channel separation becomes poor for higher audio frequencies.

It is an object of the present invention to avoid the above mentioned drawback of the prior art and to provide a stereo signal processing apparatus with an improved construction so that the channel separation is satisfying not only for lower frequencies, but also for higher frequencies.

In order to achieve this and further objects, according to the present invention, there is provided a stereo signal processing apparatus, in particular for a digital BTSC television decoder, comprising a sub-channel signal processing section which comprises an input for inputting an input sub-channel signal, a DBX expanding means and an output for outputting an output sub-channel signal, characterized in that said sub-channel signal processing section further comprises a phase error compensating means for correcting a phase error of said DBX expanding means so that at said output of said sub-channel signal processing section the phase of the output sub-channel signal is essentially constant or zero over a predetermined frequency range.

Namely, it has been found that the poor channel separation in particular at higher audio frequencies results from a phase error which occurs in the DBX expanding means and increases up to about half of the scanning frequency (0.5 x Fs). In order to reduce or eliminate such phase error, according to the present invention, the sub-channel signal processing section is provided with a phase error compensating means which results in that the phase is corrected so as to be essentially constant or zero over the interesting frequency range which usually is the audio frequency range. Consequently, by the invention the channel separation during stereo transmission, and, thus, the sound quality can be improved not only for lower, but also for higher audio frequencies.

In particular, the present invention is very useful for a digital implementation of the stereo signal processing apparatus and in particular of the sub-channel signal processing section in BTSC decoder.

Further advantageous embodiments of the invention are defined in the dependent claims.

Preferably, said phase error compensating means is coupled between said input of said sub-channel signal processing section and said DBX expanding means.

In particular, it has been found that the DBX expanding means exhibits a phase deviation which is essentially linear over the frequency range and is depending on the amplitude of the input signal. So, to overcome this, said phase error compensating means comprises a linear level depending phase error correction means. To implement the level dependency, said linear level depending phase error correction means should be controlled in accordance with the amplitude of the sub-channel signal. This results in a very good phase error compensation. In case said DBX expanding means comprises a spectral expander having a control signal output for outputting a control signal, in particular a root main square (RMS) control signal, said linear level depending phase error correction means should be controlled by said control signal.

In a still further preferred embodiment, said linear level depending phase error correction means comprises a variable phase delay (VPD) filter, preferably with an extended mixer functionality. Namely, it has been found that such a filter has a phase response which can be essentially linear up to 0.5 x Fs. Preferably, the control input of such VPD filter is connected to the control signal output of the DBX expanding means.

As mentioned above, the provision of a VPD filter results in a very good phase error compensation, but therefore a VPD filter with a very high order is needed. However, with an economic VPD filter it is possible to compensate the phase error up to about FS/4, wherein afterwards the phase response of such a VPD filter is losing linearity and turns smoothly to zero. If the provision of such an economic VPD filter is wanted without increasing the filter order, it is suggested to additionally provide a fixed phase shift filter for formatting the phase error in a way that it fits mostly to the phase response of such a VPD filter. Such an additional fixed phase shift filter can be an all-pass filter and coupled between said input of said sub-channel signal processing section and said VPD filter.

Finally, in a still further preferred embodiment of the present invention, the main channel signal processing section comprises a delay means for delaying the main channel signal by a delay time which essentially corresponds to the processing time of said phase error compensating means so as to render both the main channel and sub-channel signals time-parallel to each other.

In the following, the present invention will be described in greater detail based on a preferred embodiment with reference to the accompanying drawings in which

Fig. 1 shows a block diagram of a preferred embodiment of a stereo signal processing system;

Fig. 2 a graph showing the phase deviation of the DBX expander for different input levels and the phase response of the fixed phase shift filter; and

Fig. 3 a graph showing the overlay of the phase deviation of the DBX expander and the fixed phase shift filter response in solid lines and the phase response of the VPD filter in dotted lines.

An implementation of the stereo signal processing system is shown as block diagram in Figure 1. The System includes a main channel processing section and a sub-channel processing section. The sub-channel processing section includes a DBX expander with fixed de-emphasis, amplitude and spectral expander. Such DBX expander is a conventional DBX expander known from the prior art. The system shown in Figure 1 is mainly used for a digital BTSC television decoder.

As further shown in Figure 1, the sub-channel processing section additionally comprises an adaptive phase compensation circuit which is coupled between the sub-channel input and the DBX expander.

Namely, a problem of a digital DBX implementation is the linear level depending phase error of the variable de-emphasis filter. To overcome this, a linear level depending phase error correction is needed. For this issue a VPD (variable phase

delay) filter is provided in the adaptive phase compensation circuit since such a VPD filter has a theoretical linear phase response up to half of the scanning frequency (Fs/2). To implement the level dependency the control input of the VPD filter is connected to a route main square (RMS) control output of the spectral expander. This results in very good phase error compensation, but therefore a VPD filter with a very high order is needed.

With an economic VPD filter it is possible to compensate the phase error up to FS/4. Afterwards the phase response of the VPD filter is loosing linearity and turns smoothly to zero. To overcome this without increasing the filter order of the VPD filter, a second fixed phase shift filter is provided in the adaptive phase compensation circuit and coupled between the sub-channel input and the VPD filter to format the phase error in a way that it fits mostly to the phase response of the used VPD filter. Figure 2 shows the linear phase error of the DBX expander and the phase response of the fixed phase shift filter.

In Figure 3, it is shown the overlay of the phase deviation of the DBX expander and the fixed phase shift filter response (solid line) together with the phase response of the VDP filter (dotted line) by instance of three input levels. It can be seen that the sum of the phase response of the DBX expander plus the phase response of the fixed phase shift filter almost fits to the phase response of the VDP filter up to Fs/2. Therefore it is possible to compensate the DBX expander phase error with an economic VPD filter by creating a difference between the sum of the phase response of the DBX expander plus the phase response of the fixed phase shift filter and the phase response of the VPD filter so as to obtain a phase error of about zero up to almost Fs/2.

As further shown in Figure 1, the main channel processing section includes in addition to a fixed de-emphasis circuit a delay circuit for group delay compensation. This additional group delay compensation circuit which is coupled between the main channel input and the fixed de-emphasis circuit is used to compensate the additional group delay caused by the above described phase compensation in the sub-channel processing section.

Although the invention is described above with reference to an example shown in the attached drawings, it is apparent that the invention is not restricted to it, but can vary in many ways within the scope disclosed in the attached claims.

CLAIMS:

1. A stereo signal processing apparatus, in particular for a digital BTSC television decoder, comprising a sub-channel signal processing section which comprises an input for inputting an input sub-channel signal, a DBX expanding means and an output for outputting an output sub-channel signal,
characterized in that said sub-channel signal processing section further comprises a phase error compensating means for correcting a phase error of said DBX expanding means so that at said output of said sub-channel signal processing section the phase of the output sub-channel signal is essentially constant or zero over a predetermined frequency range.

2. The apparatus according to claim 1,
characterized in that said phase error compensating means is coupled between said input of said sub-channel signal processing section and said DBX expanding means.

3. The apparatus according to claim 1 or 2,
characterized in that said phase error compensating means comprises a linear level depending phase error correction means.

4. The apparatus according to claim 3,
characterized in that said linear level depending phase error correction means is controlled in accordance with the amplitude of the sub-channel signal.

5. The apparatus according to claim 3 or 4, wherein said DBX expanding means comprises a spectral expander having a control signal output for outputting a control signal, in particular a route main square (RMS) control signal,

characterized in that said linear level depending phase error correction means is controlled by said control signal.

6. The apparatus according to at least any one of the claims 3 to 5, characterized in that said linear level depending phase error correction means comprises a variable phase delay filter, preferably with an extended mixer functionality.

7. The apparatus according to the claims 5 and 6, characterized in that said variable phase delay filter comprises a control input which is connected to said control signal output.

8. The apparatus according to claim 6 or 7, characterized in that said phase error compensating means further comprises a fixed phase shift filter.

9. The apparatus according to claim 8, characterized in that said fixed phase shift filter is coupled between said input of said sub-channel signal processing section and said variable phase delay filter.

10. The apparatus according to at least any one of the preceding claims, further comprising a main channel signal processing section, characterized in that said main channel signal processing section comprises a delay means for delaying the main channel signal by a delay time which essentially corresponds to the processing time of said phase error compensating means.

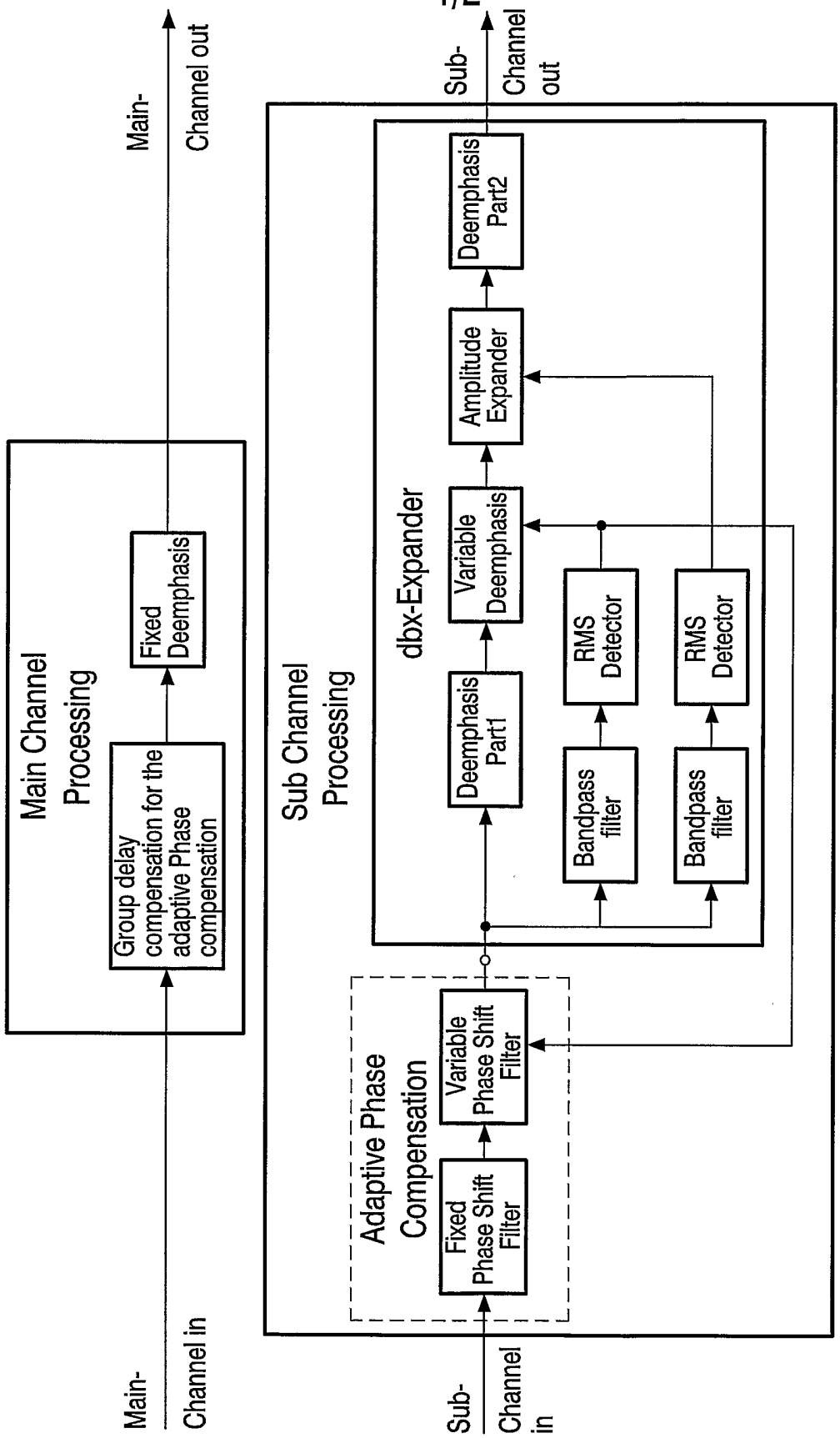
Main-
Channel in
Sub-
Channel in
Main Channel
Processing
Group delay
compensation for the
adaptive Phase
compensation
Fixed
Deemphasis
Main-
Channel out
Sub Channel
Processing
Adaptive Phase
Compensation
Fixed
Phase Shift
Filter
Variable
Phase Shift
Filter
dbx-Expander
Deemphasis
Part1
Variable
Deemphasis
Amplitude
Expander
Deemphasis
Part2
Bandpass
filter
Bandpass
filter
RMS
Detector
RMS
Detector
Sub-
Channel
out

FIG.1

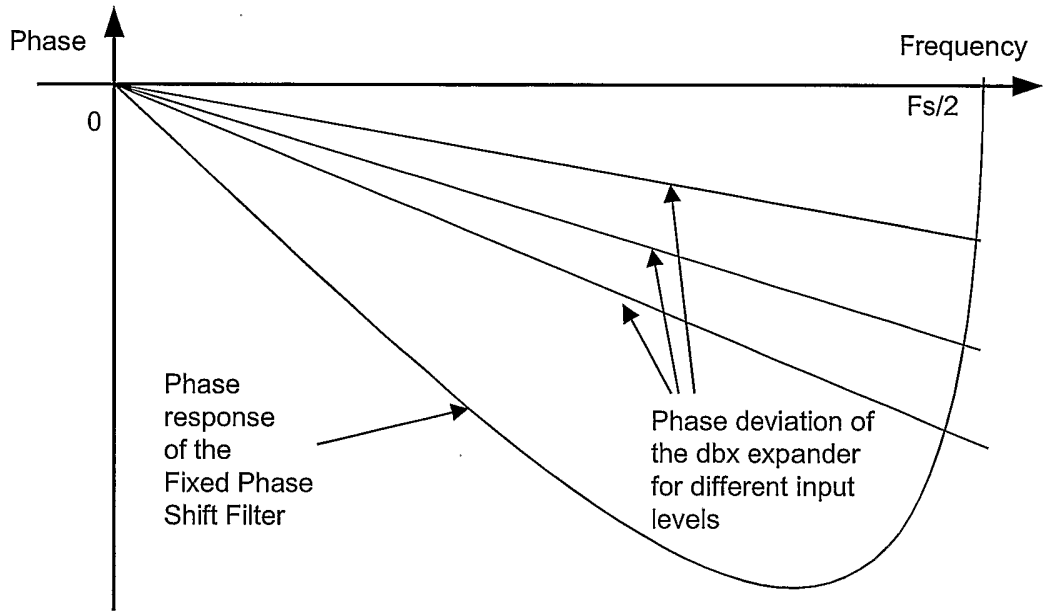
Phase
Frequency
0
Fs/2
Phase response of the Fixed Phase Shift Filter
Phase deviation of the dbx expander for different input levels

FIG.2

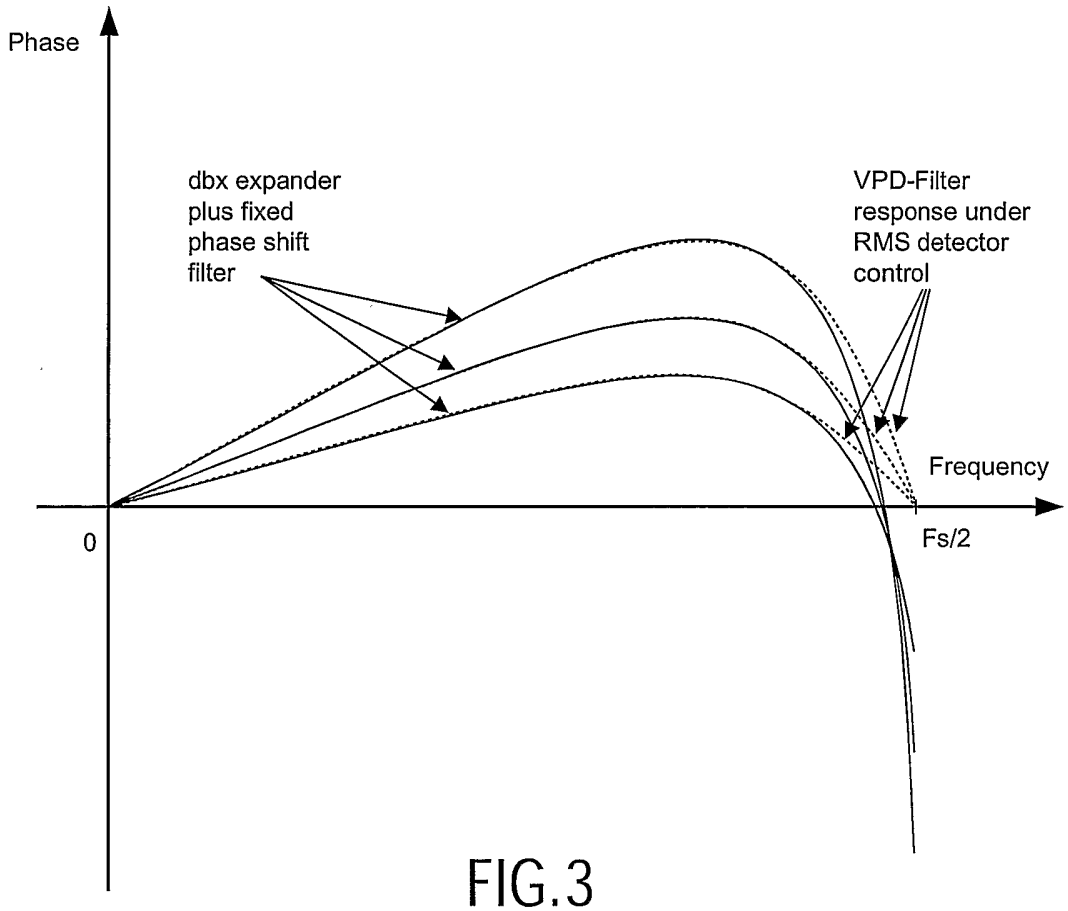
Phase
dbx expander plus fixed phase shift filter
VPD-Filter response under RMS detector control
Frequency
0
Fs/2

FIG.3