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(54) Title: AN ENCODER, A DECODER AND CORRESPONDING METHODS OF FLEXIBLE PROFILE CONFIGURATION

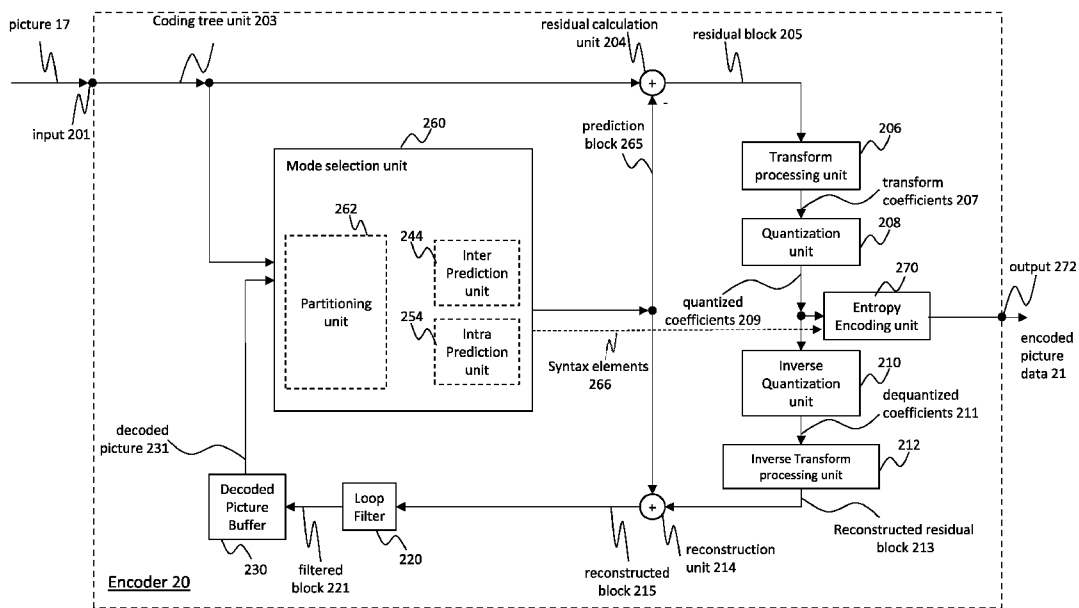


FIG. 2

(57) Abstract: A method for decoding of a video bitstream implemented by a decoding device, wherein the video bitstream includes data representing one or more sequence parameter set, SPS, flags, the method comprising: for an SPS flag of the one or more SPS flags, obtaining two variables of the SPS flag, respectively, by parsing the video bitstream, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag; obtaining the SPS flag, by parsing the video bitstream; evaluating whether the value of the SPS flag is valid based on the values of the two variables; and in case that the value of the SPS flag is valid, decoding the video bitstream according to the value of the SPS flag.



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AN ENCODER, A DECODER AND CORRESPONDING METHODS OF FLEXIBLE PROFILE CONFIGURATION

CROSS-REFERENCE TO RELATED APPLICATIONS

- 5 This patent application claims priority of international patent application PCT/EP2020/050077 filed on January 3, 2020. The disclosure of the aforementioned patent application is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

- 10 Embodiments of the present application (disclosure) generally relate to the field of picture processing and more particularly to high-level syntax and bitstream conformance.

BACKGROUND

- 15 Video coding (video encoding and decoding) is used in a wide range of digital video applications, for example broadcast digital TV, video transmission over internet and mobile networks, real-time conversational applications such as video chat, video conferencing, DVD and Blu-ray discs, video content acquisition and editing systems, and camcorders of security applications.
- 20 The amount of video data needed to depict even a relatively short video can be substantial, which may result in difficulties when the data is to be streamed or otherwise communicated across a communications network with limited bandwidth capacity. Thus, video data is generally compressed before being communicated across modern day telecommunications networks. The size of a video could also be an issue when the video is stored on a storage
- 25 device because memory resources may be limited. Video compression devices often use software and/or hardware at the source to code the video data prior to transmission or storage, thereby decreasing the quantity of data needed to represent digital video images. The compressed data is then received at the destination by a video decompression device that decodes the video data. With limited network resources and ever-increasing demands of
- 30 higher video quality, improved compression and decompression techniques that improve compression ratio with little to no sacrifice in picture quality are desirable.

SUMMARY

Embodiments of the present application provide apparatuses and methods for encoding and decoding according to the independent claims.

5 The foregoing and other objects are achieved by the subject matter of the independent claims. Further implementation forms are apparent from the dependent claims, the description and the figures.

Particular embodiments are outlined in the attached independent claims, with other embodiments in the dependent claims.

10 The present disclosure provides a method for decoding of a video bitstream implemented by a decoding device, wherein the video bitstream includes data representing one or more sequence parameter set, SPS, flags, the method comprising: for an SPS flag of the one or more SPS flags, obtaining two variables of the SPS flag, respectively, by parsing the video bitstream, wherein the value of one variable of the two variables is the minimum allowed
15 value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag; obtaining a value of the SPS flag, by parsing the video bitstream; evaluating whether the value of the SPS flag is valid based on the values of the two variables; and in case that the value of the SPS flag is valid, decoding the video bitstream according to the value of the SPS flag.

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In the following, the terms sps and SPS, sps flag and SPS flag, sps flags and SPS flags, sps flag value and SPS flag value, should be understood to have the same meaning, respectively.

Thus, the present disclosure introduces one additional syntax element to SPS, which is
25 intended to restrict SPS flags from the lower boundary, i.e., the minimum allowed value of the SPS flag.

The method as described above may further comprise: in case the value of the value of the SPS flag is not valid, stop decoding the video bitstream.

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In the method as described above, the two variables of the SPS flag may be Boolean variables, wherein the two variables may be respectively packed in two syntax elements(e.g. toolset_idc_H and toolset_idc_L), wherein the two variables may correspond to a specific bit inside the two syntax elements, respectively.

In the method as described above, the values of the two variables may be from a set $\{0,1\}$.

5 In the method as described above, the value of the SPS flag may be equal to one of the values of the variables.

In the method as described above, the values of the two variables may be from the set $\{0,1\}$, may be denoted l_i and h_i , and may be signalled in the bitstream before the SPS flag and wherein $l_i \leq sps_i \leq h_i$, where sps_i is the value of the SPS flag.

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In the method as described above, for all SPS flags of the one or more SPS flags, the two variables from the set $\{0,1\}$ may be signalled by two vectors with elements from the set $\{0,1\}$: $toolset_idc_l = l_0 l_1, \dots, l_i, \dots, l_{n-1}$ and $toolset_idc_h = h_0 h_1, \dots, h_i, \dots, h_{n-1}$, where n is a number of the one or more SPS flags, and i is an integer.

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It should be noted that in the prior art a mechanism such as `toolset_idc` mechanism only allows restricting an SPS flag value to 0, there is no method to restrict the SPS flag to 1.

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In view of this, the present disclosure overcomes this problem by extending the `toolset_idc` mechanism so as to support the functionality from both low and high boundary. In other words, the solution according to the present disclosure can be used to force both 0 and 1 SPS flag value.

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The present disclosure further provides a method for encoding of a video bitstream implemented by an encoding device, wherein the video bitstream includes data representing one or more sequence parameter set, SPS, flags, the method comprising:

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for an SPS flag of the one or more SPS flags, setting two variables of the SPS flag, respectively, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag; determining the value of the SPS flag according to the two variables of the SPS flag; and encoding the value of the SPS flag and the two variables of the SPS flag into the video bitstream.

Setting two variables of the SPS flag is based on the required coding capability.

The method as described above may further comprise: in case the value of the one variable being the minimum allowed value of the SPS flag is equal to 1, determining the value of the SPS flag to be 1.

- 5 The method as described above may further comprise: in case the value of the one variable being the maximum allowed value of the SPS flag is equal to 0, determining the value of the SPS flag to be 0.

10 The method as described above may further comprise: in case the values of both of the two variables of the SPS flag is equal to 1, determining the value of the SPS flag to be 1, respectively.

15 The method as described above may further comprise: in case the value of both of the two variables of the SPS flag is equal to 0, determining the value of the SPS flag to be 0, respectively.

20 In the method as described above, the two variables of the SPS flag may be Boolean variables, wherein the two variables may be respectively packed in two syntax elements, wherein the two variables may correspond to a specific bit inside the two syntax elements, respectively.

In the method as described above, the values of the two variables may be from a set $\{0,1\}$.

25 In the method as described above, the value of the SPS flag may be equal to one of the values of the variables.

30 In the method as described above, the values of the two variables may be from a set $\{0,1\}$, may be denoted l_i and h_i , and may be signalled in the bitstream before the SPS flag and wherein $l_i \leq sps_i \leq h_i$, where sps_i is the value of the SPS flag.

In the method as described above, for all SPS flags of the one or more SPS flags, the two variables from the set $\{0,1\}$ may be signalled by two vectors with elements from the set

$\{0,1\}$: $toolset_idc_l = l_0l_1, \dots, l_i, \dots, l_{n-1}$ and $toolset_idc_h = h_0h_1, \dots, h_i, \dots, h_{n-1}$,
where n is a number of the one or more SPS flags, and i is an integer.

5 The present disclosure further discloses an encoder comprising processing circuitry for carrying out the method as described above.

The present disclosure further discloses a decoder comprising processing circuitry for carrying out the method as described above.

10 The present disclosure further discloses a computer program product comprising program code for performing the method as described above when executed on a computer or a processor.

15 The present disclosure further discloses a decoder, comprising: one or more processors; and a non-transitory computer-readable storage medium coupled to the processors and storing programming for execution by the processors, wherein the programming, when executed by the processors, configures the decoder to carry out the method as described above.

20 The present disclosure further discloses an encoder, comprising: one or more processors; and a non-transitory computer-readable storage medium coupled to the processors and storing programming for execution by the processors, wherein the programming, when executed by the processors, configures the encoder to carry out the method as described above.

25 The present disclosure further discloses a non-transitory computer-readable medium carrying a program code which, when executed by a computer device, causes the computer device to perform the method as described above.

30 The present disclosure further discloses a non-transitory storage medium which includes an encoded bitstream decoded by an image decoding device, the bitstream being generated by dividing a frame of a video signal or an image signal into a plurality blocks, and including a plurality of SPS flags, wherein the bitstream further comprises two variables of an SPS flag, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag.

The present disclosure further discloses a decoder for decoding of a video bitstream, wherein the video bitstream includes data representing one or more sequence parameter set, SPS, flags, the decoder comprising: a first obtaining unit configured to obtain two variables for an SPS flag of the one or more SPS flags, respectively, by parsing the video bitstream, wherein
5 the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag; a second obtaining unit configured to obtain a value of the SPS flag, by parsing the video bitstream; an evaluating unit configured to evaluate whether the value of
10 the SPS flag is valid based on the values of the two variables; and a decoding unit configured to decode the video bitstream according to the value of the SPS flag in case that the value of the SPS flag is valid.

The present disclosure further discloses an encoder for encoding of a video bitstream,
15 wherein the video bitstream includes data representing one or more sequence parameter set, SPS, flags, the encoder comprising:
an indicating unit configured to set two variables for an SPS flag of the one or more SPS flags, respectively, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two
20 variables is the maximum allowed value of the SPS flag, and
a determining unit configured to determine the value of the SPS flag according to the two variables of the SPS flag; and
an encoding unit configured to encode the value of the SPS flag and the two variables of the SPS flag into the video bitstream.

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Details of one or more embodiments are set forth in the accompanying drawings and the description below. Other features, objects, and advantages will be apparent from the description, drawings, and claims.

30 BRIEF DESCRIPTION OF THE DRAWINGS

In the following embodiments of the invention are described in more detail with reference to the attached figures and drawings, in which:

FIG. 1A is a block diagram showing an example of a video coding system configured to implement embodiments of the invention;

- FIG. 1B is a block diagram showing another example of a video coding system configured to implement embodiments of the invention;
- FIG. 2 is a block diagram showing an example of a video encoder configured to implement embodiments of the invention;
- 5 FIG. 3 is a block diagram showing an example structure of a video decoder configured to implement embodiments of the invention;
- FIG. 4 is a block diagram illustrating an example of an encoding apparatus or a decoding apparatus;
- FIG. 5 is a block diagram illustrating another example of an encoding apparatus or a
10 decoding apparatus;
- FIG. 6 is a block diagram showing an example structure of a content supply system 3100, which realizes a content delivery service;
- FIG. 7 is a block diagram showing a structure of an example of a terminal device;
- FIG. 8 illustrates a flowchart of a method for decoding of a video bitstream according to
15 an embodiment of the present disclosure;
- FIG. 9 illustrates a decoder for decoding of a video bitstream according to an embodiment of the present disclosure;
- FIG. 10 illustrates a flowchart of a method for encoding of a video bitstream according to an embodiment of the present disclosure; and
- 20 FIG. 11 illustrates an encoder for encoding of a video bitstream according to an embodiment of the present disclosure.

In the following identical reference signs refer to identical or at least functionally equivalent features if not explicitly specified otherwise.

25 DETAILED DESCRIPTION OF THE EMBODIMENTS

In the following description, reference is made to the accompanying figures, which form part of the disclosure, and which show, by way of illustration, specific aspects of embodiments of the invention or specific aspects in which embodiments of the present invention may be used. It is understood that embodiments of the invention may be used in other aspects and comprise
30 structural or logical changes not depicted in the figures. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

For instance, it is understood that a disclosure in connection with a described method may also hold true for a corresponding device or system configured to perform the method and vice versa. For example, if one or a plurality of specific method steps are described, a corresponding device may include one or a plurality of units, e.g., functional units, to perform the described one or plurality of method steps (e.g., one unit performing the one or plurality of steps, or a plurality of units each performing one or more of the plurality of steps), even if such one or more units are not explicitly described or illustrated in the figures. On the other hand, for example, if a specific apparatus is described based on one or a plurality of units, e.g. functional units, a corresponding method may include one step to perform the functionality of the one or plurality of units (e.g. one step performing the functionality of the one or plurality of units, or a plurality of steps each performing the functionality of one or more of the plurality of units), even if such one or plurality of steps are not explicitly described or illustrated in the figures. Further, it is understood that the features of the various exemplary embodiments and/or aspects described herein may be combined with each other, unless specifically noted otherwise.

Video coding typically refers to the processing of a sequence of pictures, which form the video or video sequence. Instead of the term “picture”, the term “frame” or “image” may be used as synonyms in the field of video coding. Video coding (or coding in general) comprises two parts video encoding and video decoding. Video encoding is performed at the source side, typically comprising processing (e.g., by compression) the original video pictures to reduce the amount of data required for representing the video pictures (for more efficient storage and/or transmission). Video decoding is performed at the destination side and typically comprises the inverse processing compared to the encoder to reconstruct the video pictures. Embodiments referring to “coding” of video pictures (or pictures in general) shall be understood to relate to “encoding” or “decoding” of video pictures or respective video sequences. The combination of the encoding part and the decoding part is also referred to as CODEC (Coding and Decoding).

In case of lossless video coding, the original video pictures can be reconstructed, i.e., the reconstructed video pictures have the same quality as the original video pictures (assuming no transmission loss or other data loss during storage or transmission). In case of lossy video coding, further compression, e.g., by quantization, is performed, to reduce the amount of data representing the video pictures, which cannot be completely reconstructed at the decoder, i.e.,

the quality of the reconstructed video pictures is lower or worse compared to the quality of the original video pictures.

Several video coding standards belong to the group of “lossy hybrid video codecs” (i.e.,
5 combine spatial and temporal prediction in the sample domain and 2D transform coding for applying quantization in the transform domain). Each picture of a video sequence is typically partitioned into a set of non-overlapping blocks and the coding is typically performed on a block level. In other words, at the encoder the video is typically processed, i.e. encoded, on a block (video block) level, e.g. by using spatial (intra picture) prediction and/or temporal (inter
10 picture) prediction to generate a prediction block, subtracting the prediction block from the current block (block currently processed/to be processed) to obtain a residual block, transforming the residual block and quantizing the residual block in the transform domain to reduce the amount of data to be transmitted (compression), whereas at the decoder the inverse processing compared to the encoder is applied to the encoded or compressed block to
15 reconstruct the current block for representation. Furthermore, the encoder duplicates the decoder processing loop such that both will generate identical predictions (e.g., intra- and inter predictions) and/or re-constructions for processing, i.e., coding, the subsequent blocks.

In the following embodiments of a video coding system 10, a video encoder 20 and a video
20 decoder 30 are described based on FIGs. 1 to 3.

FIG. 1A is a schematic block diagram illustrating an example coding system 10, e.g., a video coding system 10 (or short coding system 10) that may utilize techniques of this present application. Video encoder 20 (or short encoder 20) and video decoder 30 (or short decoder
25 30) of video coding system 10 represent examples of devices that may be configured to perform techniques in accordance with various examples described in the present application.

As shown in FIG. 1A, the coding system 10 comprises a source device 12 configured to provide encoded picture data 21 e.g., to a destination device 14 for decoding the encoded
30 picture data 13.

The source device 12 comprises an encoder 20, and may additionally, i.e., optionally, comprise a picture source 16, a pre-processor (or pre-processing unit) 18, e.g., a picture pre-processor 18, and a communication interface or communication unit 22.

The picture source 16 may comprise or be any kind of picture capturing device, for example a camera for capturing a real-world picture, and/or any kind of a picture generating device, for example a computer-graphics processor for generating a computer animated picture, or any kind of other device for obtaining and/or providing a real-world picture, a computer generated picture (e.g. a screen content, a virtual reality (VR) picture) and/or any combination thereof (e.g. an augmented reality (AR) picture). The picture source may be any kind of memory or storage storing any of the aforementioned pictures.

In distinction to the pre-processor 18 and the processing performed by the pre-processing unit 18, the picture or picture data 17 may also be referred to as raw picture or raw picture data 17.

Pre-processor 18 is configured to receive the (raw) picture data 17 and to perform pre-processing on the picture data 17 to obtain a pre-processed picture 19 or pre-processed picture data 19. Pre-processing performed by the pre-processor 18 may, e.g., comprise trimming, color format conversion (e.g., from RGB to YCbCr), color correction, or denoising. It can be understood that the pre-processing unit 18 may be optional component.

The video encoder 20 is configured to receive the pre-processed picture data 19 and provide encoded picture data 21 (further details will be described below, e.g., based on FIG. 2).

Communication interface 22 of the source device 12 may be configured to receive the encoded picture data 21 and to transmit the encoded picture data 21 (or any further processed version thereof) over communication channel 13 to another device, e.g., the destination device 14 or any other device, for storage or direct reconstruction.

The destination device 14 comprises a decoder 30 (e.g., a video decoder 30), and may additionally, i.e., optionally, comprise a communication interface or communication unit 28, a post-processor 32 (or post-processing unit 32) and a display device 34.

The communication interface 28 of the destination device 14 is configured receive the encoded picture data 21 (or any further processed version thereof), e.g., directly from the

source device 12 or from any other source, e.g., a storage device, e.g., an encoded picture data storage device, and provide the encoded picture data 21 to the decoder 30.

5 The communication interface 22 and the communication interface 28 may be configured to transmit or receive the encoded picture data 21 or encoded data 13 via a direct communication link between the source device 12 and the destination device 14, e.g., a direct wired or wireless connection, or via any kind of network, e.g., a wired or wireless network or any combination thereof, or any kind of private and public network, or any kind of combination thereof.

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The communication interface 22 may be, e.g., configured to package the encoded picture data 21 into an appropriate format, e.g., packets, and/or process the encoded picture data using any kind of transmission encoding or processing for transmission over a communication link or communication network.

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The communication interface 28, forming the counterpart of the communication interface 22, may be, e.g., configured to receive the transmitted data and process the transmission data using any kind of corresponding transmission decoding or processing and/or de-packaging to obtain the encoded picture data 21.

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Both, communication interface 22 and communication interface 28 may be configured as unidirectional communication interfaces as indicated by the arrow for the communication channel 13 in FIG. 1A pointing from the source device 12 to the destination device 14, or bi-directional communication interfaces, and may be configured, e.g. to send and receive messages, e.g. to set up a connection, to acknowledge and exchange any other information related to the communication link and/or data transmission, e.g. encoded picture data transmission.

30 The decoder 30 is configured to receive the encoded picture data 21 and provide decoded picture data 31 or a decoded picture 31 (further details will be described below, e.g., based on FIG. 3 or FIG. 5).

The post-processor 32 of destination device 14 is configured to post-process the decoded picture data 31 (also called reconstructed picture data), e.g., the decoded picture 31, to obtain

post-processed picture data 33, e.g., a post-processed picture 33. The post-processing performed by the post-processing unit 32 may comprise, e.g., color format conversion (e.g., from YCbCr to RGB), color correction, trimming, or re-sampling, or any other processing, e.g., for preparing the decoded picture data 31 for display, e.g., by display device 34.

5

The display device 34 of the destination device 14 is configured to receive the post-processed picture data 33 for displaying the picture, e.g., to a user or viewer. The display device 34 may be or comprise any kind of display for representing the reconstructed picture, e.g., an integrated or external display or monitor. The displays may, e.g., comprise liquid crystal displays (LCD), organic light emitting diodes (OLED) displays, plasma displays, projectors, micro LED displays, liquid crystal on silicon (LCoS), digital light processor (DLP) or any kind of other display.

10

Although FIG. 1A depicts the source device 12 and the destination device 14 as separate devices, embodiments of devices may also comprise both or both functionalities, the source device 12 or corresponding functionality and the destination device 14 or corresponding functionality. In such embodiments the source device 12 or corresponding functionality and the destination device 14 or corresponding functionality may be implemented using the same hardware and/or software or by separate hardware and/or software or any combination thereof.

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As will be apparent for the skilled person based on the description, the existence and (exact) split of functionalities of the different units or functionalities within the source device 12 and/or destination device 14 as shown in FIG. 1A may vary depending on the actual device and application.

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The encoder 20 (e.g., a video encoder 20) or the decoder 30 (e.g., a video decoder 30) or both encoder 20 and decoder 30 may be implemented via processing circuitry as shown in FIG. 1B, such as one or more microprocessors, digital signal processors (DSPs), application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), discrete logic, hardware, video coding dedicated or any combinations thereof. The encoder 20 may be implemented via processing circuitry 46 to embody the various modules as discussed with respect to encoder 20 of FIG. 2 and/or any other encoder system or subsystem described herein. The decoder 30 may be implemented via processing circuitry 46 to embody the

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various modules as discussed with respect to decoder 30 of FIG. 3 and/or any other decoder system or subsystem described herein. The processing circuitry may be configured to perform the various operations as discussed later. As shown in fig. 5, if the techniques are implemented partially in software, a device may store instructions for the software in a suitable, non-transitory computer-readable storage medium and may execute the instructions in hardware using one or more processors to perform the techniques of this disclosure. Either of video encoder 20 and video decoder 30 may be integrated as part of a combined encoder/decoder (CODEC) in a single device, for example, as shown in FIG. 1B.

10 Source device 12 and destination device 14 may comprise any of a wide range of devices, including any kind of handheld or stationary devices, e.g. notebook or laptop computers, mobile phones, smart phones, tablets or tablet computers, cameras, desktop computers, set-top boxes, televisions, display devices, digital media players, video gaming consoles, video streaming devices (such as content services servers or content delivery servers), broadcast receiver device, broadcast transmitter device, or the like and may use no or any kind of operating system. In some cases, the source device 12 and the destination device 14 may be equipped for wireless communication. Thus, the source device 12 and the destination device 14 may be wireless communication devices.

20 In some cases, video coding system 10 illustrated in FIG. 1A is merely an example and the techniques of the present application may apply to video coding settings (e.g., video encoding or video decoding) that do not necessarily include any data communication between the encoding and decoding devices. In other examples, data is retrieved from a local memory, streamed over a network, or the like. A video encoding device may encode and store data to memory, and/or a video decoding device may retrieve and decode data from memory. In some examples, the encoding and decoding is performed by devices that do not communicate with one another, but simply encode data to memory and/or retrieve and decode data from memory.

30 For convenience of description, embodiments of the invention are described herein, for example, by reference to High-Efficiency Video Coding (HEVC) or to the reference software of Versatile Video coding (VVC), the next generation video coding standard developed by the Joint Collaboration Team on Video Coding (JCT-VC) of ITU-T Video Coding Experts

Group (VCEG) and ISO/IEC Motion Picture Experts Group (MPEG). One of ordinary skill in the art will understand that embodiments of the invention are not limited to HEVC or VVC.

Encoder and Encoding Method

5 FIG. 2 shows a schematic block diagram of an example video encoder 20 that is configured to implement the techniques of the present application. In the example of FIG. 2, the video encoder 20 comprises an input 201 (or input interface 201), a residual calculation unit 204, a transform processing unit 206, a quantization unit 208, an inverse quantization unit 210, and inverse transform processing unit 212, a reconstruction unit 214, a loop filter unit 220, a
10 decoded picture buffer (DPB) 230, a mode selection unit 260, an entropy encoding unit 270 and an output 272 (or output interface 272). The mode selection unit 260 may include an inter prediction unit 244, an intra prediction unit 254 and a partitioning unit 262. Inter prediction unit 244 may include a motion estimation unit and a motion compensation unit (not shown). A video encoder 20 as shown in FIG. 2 may also be referred to as hybrid video
15 encoder or a video encoder according to a hybrid video codec.

The residual calculation unit 204, the transform processing unit 206, the quantization unit 208, the mode selection unit 260 may be referred to as forming a forward signal path of the encoder 20, whereas the inverse quantization unit 210, the inverse transform processing unit
20 212, the reconstruction unit 214, the buffer 216, the loop filter 220, the decoded picture buffer (DPB) 230, the inter prediction unit 244 and the intra-prediction unit 254 may be referred to as forming a backward signal path of the video encoder 20, wherein the backward signal path of the video encoder 20 corresponds to the signal path of the decoder (see video decoder 30 in FIG. 3). The inverse quantization unit 210, the inverse transform processing
25 unit 212, the reconstruction unit 214, the loop filter 220, the decoded picture buffer (DPB) 230, the inter prediction unit 244 and the intra-prediction unit 254 are also referred to forming the “built-in decoder” of video encoder 20.

Pictures & Picture Partitioning (Pictures & Blocks)

30 The encoder 20 may be configured to receive, e.g., via input 201, a picture 17 (or picture data 17), e.g., picture of a sequence of pictures forming a video or video sequence. The received picture or picture data may also be a pre-processed picture 19 (or pre-processed picture data 19). For sake of simplicity, the following description refers to the picture 17. The picture 17 may also be referred to as current picture or picture to be coded (in particular in video coding

to distinguish the current picture from other pictures, e.g., previously encoded and/or decoded pictures of the same video sequence, i.e., the video sequence which also comprises the current picture).

5 A (digital) picture is or can be regarded as a two-dimensional array or matrix of samples with intensity values. A sample in the array may also be referred to as pixel (short form of picture element) or a pel. The number of samples in horizontal and vertical direction (or axis) of the array or picture define the size and/or resolution of the picture. For representation of color, typically three color components are employed, i.e., the picture may be represented or include
10 three sample arrays. In RGB format or color space a picture comprises a corresponding red, green and blue sample array. However, in video coding each pixel is typically represented in a luminance and chrominance format or color space, e.g., YCbCr, which comprises a luminance component indicated by Y (sometimes also L is used instead) and two chrominance components indicated by Cb and Cr. The luminance (or short luma) component
15 Y represents the brightness or grey level intensity (e.g., like in a grey-scale picture), while the two chrominance (or short chroma) components Cb and Cr represent the chromaticity or color information components. Accordingly, a picture in YCbCr format comprises a luminance sample array of luminance sample values (Y), and two chrominance sample arrays of chrominance values (Cb and Cr). Pictures in RGB format may be converted or transformed
20 into YCbCr format and vice versa, the process is also known as color transformation or conversion. If a picture is monochrome, the picture may comprise only a luminance sample array. Accordingly, a picture may be, for example, an array of luma samples in monochrome format or an array of luma samples and two corresponding arrays of chroma samples in 4:2:0, 4:2:2, and 4:4:4 colour format.

25 Embodiments of the video encoder 20 may comprise a picture partitioning unit (not depicted in FIG. 2) configured to partition the picture 17 into a plurality of (typically non-overlapping) picture blocks 203. These blocks may also be referred to as root blocks, macro blocks (H.264/AVC) or coding tree blocks (CTB) or coding tree units (CTU) (H.265/HEVC and
30 VVC). The picture-partitioning unit may be configured to use the same block size for all pictures of a video sequence and the corresponding grid defining the block size, or to change the block size between pictures or subsets or groups of pictures, and partition each picture into the corresponding blocks.

In further embodiments, the video encoder may be configured to receive directly a block 203 of the picture 17, e.g., one, several or all blocks forming the picture 17. The picture block 203 may also be referred to as current picture block or picture block to be coded.

- 5 Like the picture 17, the picture block 203 again is or can be regarded as a two-dimensional array or matrix of samples with intensity values (sample values), although of smaller dimension than the picture 17. In other words, the block 203 may comprise, e.g., one sample array (e.g., a luma array in case of a monochrome picture 17, or a luma or chroma array in case of a color picture) or three sample arrays (e.g., a luma and two chroma arrays in case of
- 10 a color picture 17) or any other number and/or kind of arrays depending on the color format applied. The number of samples in horizontal and vertical direction (or axis) of the block 203 define the size of block 203. Accordingly, a block may, for example, an $M \times N$ (M -column by N -row) array of samples, or an $M \times N$ array of transform coefficients.
- 15 Embodiments of the video encoder 20 as shown in FIG. 2 may be configured to encode the picture 17 block by block, e.g., the encoding and prediction is performed per block 203.

Embodiments of the video encoder 20 as shown in FIG. 2 may be further configured to partition and/or encode the picture by using slices (also referred to as video slices), wherein a

20 picture may be partitioned into or encoded using one or more slices (typically non-overlapping), and each slice may comprise one or more blocks (e.g., CTUs) or one or more groups of blocks (e.g., tiles (H.265/HEVC and VVC) or bricks (VVC)).

Embodiments of the video encoder 20 as shown in FIG. 2 may be further configured to

25 partition and/or encode the picture by using slices/tile groups (also referred to as video tile groups) and/or tiles (also referred to as video tiles), wherein a picture may be partitioned into or encoded using one or more slices/tile groups (typically non-overlapping), and each slice/tile group may comprise, e.g. one or more blocks (e.g. CTUs) or one or more tiles, wherein each tile, e.g. may be of rectangular shape and may comprise one or more blocks

30 (e.g. CTUs), e.g. complete or fractional blocks.

Residual Calculation

The residual calculation unit 204 may be configured to calculate a residual block 205 (also referred to as residual 205) based on the picture block 203 and a prediction block 265 (further

details about the prediction block 265 are provided later), e.g., by subtracting sample values of the prediction block 265 from sample values of the picture block 203, sample by sample (pixel by pixel) to obtain the residual block 205 in the sample domain.

5 Transform

The transform processing unit 206 may be configured to apply a transform, e.g., a discrete cosine transform (DCT) or discrete sine transform (DST), on the sample values of the residual block 205 to obtain transform coefficients 207 in a transform domain. The transform coefficients 207 may also be referred to as transform residual coefficients and represent the residual block 205 in the transform domain.

The transform processing unit 206 may be configured to apply integer approximations of DCT/DST, such as the transforms specified for H.265/HEVC. Compared to an orthogonal DCT transform, such integer approximations are typically scaled by a certain factor. In order to preserve the norm of the residual block which is processed by forward and inverse transforms, additional scaling factors are applied as part of the transform process. The scaling factors are typically chosen based on certain constraints like scaling factors being a power of two for shift operations, bit depth of the transform coefficients, tradeoff between accuracy and implementation costs, etc. Specific scaling factors are, for example, specified for the inverse transform, e.g., by inverse transform processing unit 212 (and the corresponding inverse transform, e.g., by inverse transform processing unit 312 at video decoder 30) and corresponding scaling factors for the forward transform, e.g., by transform processing unit 206, at an encoder 20 may be specified accordingly.

Embodiments of the video encoder 20 (respectively transform processing unit 206) may be configured to output transform parameters, e.g., a type of transform or transforms, e.g., directly or encoded or compressed via the entropy encoding unit 270, so that, e.g., the video decoder 30 may receive and use the transform parameters for decoding.

30 Quantization

The quantization unit 208 may be configured to quantize the transform coefficients 207 to obtain quantized coefficients 209, e.g., by applying scalar quantization or vector quantization. The quantized coefficients 209 may also be referred to as quantized transform coefficients 209 or quantized residual coefficients 209.

The quantization process may reduce the bit depth associated with some or all of the transform coefficients 207. For example, an n-bit transform coefficient may be rounded down to an m-bit Transform coefficient during quantization, where n is greater than m. The degree of quantization may be modified by adjusting a quantization parameter (QP). For example, 5 for scalar quantization, different scaling may be applied to achieve finer or coarser quantization. Smaller quantization step sizes correspond to finer quantization, whereas larger quantization step sizes correspond to coarser quantization. The applicable quantization step size may be indicated by a quantization parameter (QP). The quantization parameter may for 10 example be an index to a predefined set of applicable quantization step sizes. For example, small quantization parameters may correspond to fine quantization (small quantization step sizes) and large quantization parameters may correspond to coarse quantization (large quantization step sizes) or vice versa. The quantization may include division by a quantization step size and a corresponding and/or the inverse dequantization, e.g., by inverse 15 quantization unit 210, may include multiplication by the quantization step size. Embodiments according to some standards, e.g., HEVC, may be configured to use a quantization parameter to determine the quantization step size. Generally, the quantization step size may be calculated based on a quantization parameter using a fixed-point approximation of an equation including division. Additional scaling factors may be introduced for quantization 20 and dequantization to restore the norm of the residual block, which might be modified because of the scaling used in the fixed-point approximation of the equation for quantization step size and quantization parameter. In one example implementation, the scaling of the inverse transform and dequantization might be combined. Alternatively, customized quantization tables may be used and signaled from an encoder to a decoder, e.g., in a 25 bitstream. The quantization is a lossy operation, wherein the loss increases with increasing quantization step sizes.

Embodiments of the video encoder 20 (respectively quantization unit 208) may be configured to output quantization parameters (QP), e.g., directly or encoded via the entropy encoding 30 unit 270, so that, e.g., the video decoder 30 may receive and apply the quantization parameters for decoding.

Inverse Quantization

The inverse quantization unit 210 is configured to apply the inverse quantization of the quantization unit 208 on the quantized coefficients to obtain dequantized coefficients 211, e.g., by applying the inverse of the quantization scheme applied by the quantization unit 208 based on or using the same quantization step size as the quantization unit 208. The dequantized coefficients 211 may also be referred to as dequantized residual coefficients 211 and correspond - although typically not identical to the transform coefficients due to the loss by quantization - to the transform coefficients 207.

10 Inverse Transform

The inverse transform processing unit 212 is configured to apply the inverse transform of the transform applied by the transform processing unit 206, e.g., an inverse discrete cosine transform (DCT) or inverse discrete sine transform (DST) or other inverse transforms, to obtain a reconstructed residual block 213 (or corresponding dequantized coefficients 213) in the sample domain. The reconstructed residual block 213 may also be referred to as transform block 213.

Reconstruction

The reconstruction unit 214 (e.g., adder or summer 214) is configured to add the transform block 213 (i.e., reconstructed residual block 213) to the prediction block 265 to obtain a reconstructed block 215 in the sample domain, e.g., by adding – sample by sample - the sample values of the reconstructed residual block 213 and the sample values of the prediction block 265.

25 Filtering

The loop filter unit 220 (or short “loop filter” 220), is configured to filter the reconstructed block 215 to obtain a filtered block 221, or in general, to filter reconstructed samples to obtain filtered sample values. The loop filter unit is, e.g., configured to smooth pixel transitions, or otherwise improve the video quality. The loop filter unit 220 may comprise one or more loop filters such as a de-blocking filter, a sample-adaptive offset (SAO) filter or one or more other filters, e.g., an adaptive loop filter (ALF), a noise suppression filter (NSF), or any combination thereof. In an example, the loop filter unit 220 may comprise a de-blocking filter, a SAO filter and an ALF filter. The order of the filtering process may be the deblocking filter, SAO and ALF. In another example, a process called the luma mapping with chroma

scaling (LMCS) (namely, the adaptive in-loop reshaper) is added. This process is performed before deblocking. In another example, the deblocking filter process may be also applied to internal sub-block edges, e.g., affine sub-blocks edges, ATMVP sub-blocks edges, sub-block transform (SBT) edges and intra sub-partition (ISP) edges. Although the loop filter unit 220 is shown in FIG. 2 as being an in loop filter, in other configurations, the loop filter unit 220 may be implemented as a post loop filter. The filtered block 221 may also be referred to as filtered reconstructed block 221.

Embodiments of the video encoder 20 (respectively loop filter unit 220) may be configured to output loop filter parameters (such as SAO filter parameters or ALF filter parameters or LMCS parameters), e.g., directly or encoded via the entropy encoding unit 270, so that, e.g., a decoder 30 may receive and apply the same loop filter parameters or respective loop filters for decoding.

15 Decoded Picture Buffer

The decoded picture buffer (DPB) 230 may be a memory that stores reference pictures, or in general reference picture data, for encoding video data by video encoder 20. The DPB 230 may be formed by any of a variety of memory devices, such as dynamic random access memory (DRAM), including synchronous DRAM (SDRAM), magnetoresistive RAM (MRAM), resistive RAM (RRAM), or other types of memory devices. The decoded picture buffer (DPB) 230 may be configured to store one or more filtered blocks 221. The decoded picture buffer 230 may be further configured to store other previously filtered blocks, e.g. previously reconstructed and filtered blocks 221, of the same current picture or of different pictures, e.g. previously reconstructed pictures, and may provide complete previously reconstructed, i.e. decoded, pictures (and corresponding reference blocks and samples) and/or a partially reconstructed current picture (and corresponding reference blocks and samples), for example for inter prediction. The decoded picture buffer (DPB) 230 may be also configured to store one or more unfiltered reconstructed blocks 215, or in general unfiltered reconstructed samples, e.g., if the reconstructed block 215 is not filtered by loop filter unit 220, or any other further processed version of the reconstructed blocks or samples.

Mode Selection (Partitioning & Prediction)

The mode selection unit 260 comprises partitioning unit 262, inter-prediction unit 244 and intra-prediction unit 254, and is configured to receive or obtain original picture data, e.g. an

original block 203 (current block 203 of the current picture 17), and reconstructed picture data, e.g. filtered and/or unfiltered reconstructed samples or blocks of the same (current) picture and/or from one or a plurality of previously decoded pictures, e.g. from decoded picture buffer 230 or other buffers (e.g. line buffer, not shown).. The reconstructed picture data is used as reference picture data for prediction, e.g., inter-prediction or intra-prediction, to obtain a prediction block 265 or predictor 265.

Mode selection unit 260 may be configured to determine or select a partitioning for a current block prediction mode (including no partitioning) and a prediction mode (e.g., an intra or inter prediction mode) and generate a corresponding prediction block 265, which is used for the calculation of the residual block 205 and for the reconstruction of the reconstructed block 215.

Embodiments of the mode selection unit 260 may be configured to select the partitioning and the prediction mode (e.g., from those supported by or available for mode selection unit 260), which provide the best match or in other words the minimum residual (minimum residual means better compression for transmission or storage), or a minimum signaling overhead (minimum signaling overhead means better compression for transmission or storage), or which considers or balances both. The mode selection unit 260 may be configured to determine the partitioning and prediction mode based on rate distortion optimization (RDO), i.e., select the prediction mode, which provides a minimum rate distortion. Terms like “best”, “minimum”, “optimum” etc. in this context do not necessarily refer to an overall “best”, “minimum”, “optimum”, etc. but may also refer to the fulfillment of a termination or selection criterion like a value exceeding or falling below a threshold or other constraints leading potentially to a “sub-optimum selection” but reducing complexity and processing time.

In other words, the partitioning unit 262 may be configured to partition a picture from a video sequence into a sequence of coding tree units (CTUs), and the CTU 203 may be further partitioned into smaller block partitions or sub-blocks (which form again blocks), e.g. iteratively using quad-tree-partitioning (QT), binary partitioning (BT) or triple-tree-partitioning (TT) or any combination thereof, and to perform, e.g., the prediction for each of the block partitions or sub-blocks, wherein the mode selection comprises the selection of the

tree-structure of the partitioned block 203 and the prediction modes are applied to each of the block partitions or sub-blocks.

5 In the following the partitioning (e.g., by partitioning unit 260) and prediction processing (by inter-prediction unit 244 and intra-prediction unit 254) performed by an example video encoder 20 will be explained in more detail.

Partitioning

10 The partitioning unit 262 may be configured to partition a picture from a video sequence into a sequence of coding tree units (CTUs), and the partitioning unit 262 may partition (or split) a coding tree unit (CTU) 203 into smaller partitions, e.g., smaller blocks of square or rectangular size. For a picture that has three sample arrays, a CTU consists of an $N \times N$ block of luma samples together with two corresponding blocks of chroma samples. The maximum allowed size of the luma block in a CTU is specified to be 128×128 in the developing
15 versatile video coding (VVC), but it can be specified to be value rather than 128×128 in the future, for example, 256×256 . The CTUs of a picture may be clustered/grouped as slices/tile groups, tiles or bricks. A tile covers a rectangular region of a picture, and a tile can be divided into one or more bricks. A brick consists of a number of CTU rows within a tile. A tile that is not partitioned into multiple bricks can be referred to as a brick. However, a brick is a true
20 subset of a tile and is not referred to as a tile. There are two modes of tile groups are supported in VVC, namely the raster-scan slice/tile group mode and the rectangular slice mode. In the raster-scan tile group mode, a slice/tile group contains a sequence of tiles in tile raster scan of a picture. In the rectangular slice mode, a slice contains a number of bricks of a picture that collectively form a rectangular region of the picture. The bricks within a
25 rectangular slice are in the order of brick raster scan of the slice. These smaller blocks (which may also be referred to as sub-blocks) may be further partitioned into even smaller partitions. This is also referred to tree-partitioning or hierarchical tree-partitioning, wherein a root block, e.g. at root tree-level 0 (hierarchy-level 0, depth 0), may be recursively partitioned, e.g. partitioned into two or more blocks of a next lower tree-level, e.g. nodes at tree-level 1
30 (hierarchy-level 1, depth 1), wherein these blocks may be again partitioned into two or more blocks of a next lower level, e.g. tree-level 2 (hierarchy-level 2, depth 2), etc. until the partitioning is terminated, e.g. because a termination criterion is fulfilled, e.g. a maximum tree depth or minimum block size is reached. Blocks, which are not further partitioned, are also referred to as leaf-blocks or leaf nodes of the tree. A tree using partitioning into two

partitions is referred to as binary-tree (BT), a tree using partitioning into three partitions is referred to as ternary-tree (TT), and a tree using partitioning into four partitions is referred to as quad-tree (QT).

5 For example, a coding tree unit (CTU) may be or comprise a CTB of luma samples, two corresponding CTBs of chroma samples of a picture that has three sample arrays, or a CTB of samples of a monochrome picture or a picture that is coded using three separate colour planes and syntax structures used to code the samples. Correspondingly, a coding tree block (CTB) may be an $N \times N$ block of samples for some value of N such that the division of a component
10 into CTBs is a partitioning. A coding unit (CU) may be or comprise a coding block of luma samples, two corresponding coding blocks of chroma samples of a picture that has three sample arrays, or a coding block of samples of a monochrome picture or a picture that is coded using three separate colour planes and syntax structures used to code the samples. Correspondingly, a coding block (CB) may be an $M \times N$ block of samples for some values of
15 M and N such that the division of a CTB into coding blocks is a partitioning.

In embodiments, e.g., according to HEVC, a coding tree unit (CTU) may be split into CUs by using a quad-tree structure denoted as coding tree. The decision whether to code a picture area using inter-picture (temporal) or intra-picture (spatial) prediction is made at the leaf CU
20 level. Each leaf CU can be further split into one, two or four PUs according to the PU splitting type. Inside one PU, the same prediction process is applied and the relevant information is transmitted to the decoder on a PU basis. After obtaining the residual block by applying the prediction process based on the PU splitting type, a leaf CU can be partitioned into transform units (TUs) according to another quadtree structure similar to the coding tree
25 for the CU.

In embodiments, e.g., according to the latest video coding standard currently in development, which is referred to as Versatile Video Coding (VVC), a combined Quad-tree nested multi-type tree using binary and ternary splits segmentation structure for example used to partition
30 a coding tree unit. In the coding tree structure within a coding tree unit, a CU can have either a square or a rectangular shape. For example, the coding tree unit (CTU) is first partitioned by a quaternary tree. Then the quaternary tree leaf nodes can be further partitioned by a multi-type tree structure. There are four splitting types in multi-type tree structure, vertical binary splitting (SPLIT_BT_VER), horizontal binary splitting (SPLIT_BT_HOR), vertical ternary

splitting (SPLIT_TT_VER), and horizontal ternary splitting (SPLIT_TT_HOR). The multi-type tree leaf nodes are called coding units (CUs), and unless the CU is too large for the maximum transform length, this segmentation is used for prediction and transform processing without any further partitioning. This means that, in most cases, the CU, PU and TU have the same block size in the quadtree with nested multi-type tree coding block structure. The exception occurs when maximum supported transform length is smaller than the width or height of the colour component of the CU. VVC develops a unique signaling mechanism of the partition splitting information in quadtree with nested multi-type tree coding tree structure. In the signalling mechanism, a coding tree unit (CTU) is treated as the root of a quaternary tree and is first partitioned by a quaternary tree structure. Each quaternary tree leaf node (when sufficiently large to allow it) is then further partitioned by a multi-type tree structure. In the multi-type tree structure, a first flag (`mtt_split_cu_flag`) is signalled to indicate whether the node is further partitioned; when a node is further partitioned, a second flag (`mtt_split_cu_vertical_flag`) is signalled to indicate the splitting direction, and then a third flag (`mtt_split_cu_binary_flag`) is signalled to indicate whether the split is a binary split or a ternary split. Based on the values of `mtt_split_cu_vertical_flag` and `mtt_split_cu_binary_flag`, the multi-type tree splitting mode (`MttSplitMode`) of a CU can be derived by a decoder based on a predefined rule or a table. It should be noted, for a certain design, for example, 64×64 Luma block and 32×32 Chroma pipelining design in VVC hardware decoders, TT split is forbidden when either width or height of a luma coding block is larger than 64, as shown in Figure 6. TT split is also forbidden when either width or height of a chroma coding block is larger than 32. The pipelining design will divide a picture into Virtual pipeline data units (VPDUs) which are defined as non-overlapping units in a picture. In hardware decoders, successive VPDUs are processed by multiple pipeline stages simultaneously. The VPDU size is roughly proportional to the buffer size in most pipeline stages, so it is important to keep the VPDU size small. In most hardware decoders, the VPDU size can be set to maximum transform block (TB) size. However, in VVC, ternary tree (TT) and binary tree (BT) partition may lead to the increasing of VPDUs sizes. In addition, it should be noted that, when a portion of a tree node block exceeds the bottom or right picture boundary, the tree node block is forced to be split until the all samples of every coded CU are located inside the picture boundaries.

As an example, the Intra Sub-Partitions (ISP) tool may divide luma intra-predicted blocks vertically or horizontally into 2 or 4 sub-partitions depending on the block size.

In one example, the mode selection unit 260 of video encoder 20 may be configured to perform any combination of the partitioning techniques described herein.

5 As described above, the video encoder 20 is configured to determine or select the best or an optimum prediction mode from a set of (e.g., pre-determined) prediction modes. The set of prediction modes may comprise, e.g., intra-prediction modes and/or inter-prediction modes.

Intra-Prediction

10 The set of intra-prediction modes may comprise 35 different intra-prediction modes, e.g., non-directional modes like DC (or mean) mode and planar mode, or directional modes, e.g., as defined in HEVC, or may comprise 67 different intra-prediction modes, e.g., non-directional modes like DC (or mean) mode and planar mode, or directional modes, e.g., as defined for VVC. As an example, several conventional angular intra prediction modes are adaptively replaced with wide-angle intra prediction modes for the non-square blocks, e.g., as
15 defined in VVC. As another example, to avoid division operations for DC prediction, only the longer side is used to compute the average for non-square blocks. In addition, the results of intra prediction of planar mode may be further modified by a position dependent intra prediction combination (PDPC) method.

20 The intra-prediction unit 254 is configured to use reconstructed samples of neighboring blocks of the same current picture to generate an intra-prediction block 265 according to an intra-prediction mode of the set of intra-prediction modes.

25 The intra prediction unit 254 (or in general the mode selection unit 260) is further configured to output intra-prediction parameters (or in general information indicative of the selected intra prediction mode for the block) to the entropy encoding unit 270 in form of syntax elements 266 for inclusion into the encoded picture data 21, so that, e.g., the video decoder 30 may receive and use the prediction parameters for decoding.

30 Inter-Prediction

The set of (or possible) inter-prediction modes depends on the available reference pictures (i.e. previous at least partially decoded pictures, e.g. stored in DBP 230) and other inter-prediction parameters, e.g. whether the whole reference picture or only a part, e.g. a search window area around the area of the current block, of the reference picture is used for

searching for a best matching reference block, and/or e.g. whether pixel interpolation is applied, e.g. half/semi-pel, quarter-pel and/or 1/16 pel interpolation, or not.

5 Additional to the above prediction modes, skip mode, direct mode and/or other inter prediction mode may be applied.

For example, Extended merge prediction, the merge candidate list of such mode is constructed by including the following five types of candidates in order: Spatial MVP from spatial neighbor CUs, Temporal MVP from collocated CUs, History-based MVP from an
10 FIFO table, Pairwise average MVP and Zero MVs. In addition, a bilateral-matching based decoder side motion vector refinement (DMVR) may be applied to increase the accuracy of the MVs of the merge mode. Merge mode with MVD (MMVD), which comes from merge mode with motion vector differences. A MMVD flag is signaled right after sending a skip flag and merge flag to specify whether MMVD mode is used for a CU. In addition, a CU-
15 level adaptive motion vector resolution (AMVR) scheme may be applied. AMVR allows MVD of the CU to be coded in different precision. Dependent on the prediction mode for the current CU, the MVDs of the current CU can be adaptively selected. When a CU is coded in merge mode, the combined inter/intra prediction (CIIP) mode may be applied to the current CU. Weighted averaging of the inter and intra prediction signals is performed to obtain the
20 CIIP prediction. Affine motion compensated prediction, the affine motion field of the block is described by motion information of two control point (4-parameter) or three control point motion vectors (6-parameter). Subblock-based temporal motion vector prediction (SbTMVP), which is similar to the temporal motion vector prediction (TMVP) in HEVC, but predicts the motion vectors of the sub-CUs within the current CU. Bi-directional optical flow (BDOF),
25 previously referred to as BIO, is a simpler version that requires much less computation, especially in terms of number of multiplications and the size of the multiplier. Triangle partition mode, in such a mode, a CU is split evenly into two triangle-shaped partitions, using either the diagonal split or the anti-diagonal split. Besides, the bi-prediction mode is extended beyond simple averaging to allow weighted averaging of the two prediction signals.

30

The inter prediction unit 244 may include a motion estimation (ME) unit and a motion compensation (MC) unit (both not shown in FIG.2). The motion estimation unit may be configured to receive or obtain the picture block 203 (current picture block 203 of the current picture 17) and a decoded picture 231, or at least one or a plurality of previously

reconstructed blocks, e.g., reconstructed blocks of one or a plurality of other/different previously decoded pictures 231, for motion estimation. E.g., a video sequence may comprise the current picture and the previously decoded pictures 231, or in other words, the current picture and the previously decoded pictures 231 may be part of or form a sequence of pictures forming a video sequence.

The encoder 20 may, e.g., be configured to select a reference block from a plurality of reference blocks of the same or different pictures of the plurality of other pictures and provide a reference picture (or reference picture index) and/or an offset (spatial offset) between the position (x, y coordinates) of the reference block and the position of the current block as inter prediction parameters to the motion estimation unit. This offset is also called motion vector (MV).

The motion compensation unit is configured to obtain, e.g., receive, an inter prediction parameter and to perform inter prediction based on or using the inter prediction parameter to obtain an inter prediction block 265. Motion compensation, performed by the motion compensation unit, may involve fetching or generating the prediction block based on the motion/block vector determined by motion estimation, possibly performing interpolations to sub-pixel precision. Interpolation filtering may generate additional pixel samples from known pixel samples, thus potentially increasing the number of candidate prediction blocks that may be used to code a picture block. Upon receiving the motion vector for the PU of the current picture block, the motion compensation unit may locate the prediction block to which the motion vector points in one of the reference picture lists.

The motion compensation unit may also generate syntax elements associated with the blocks and video slices for use by video decoder 30 in decoding the picture blocks of the video slice. In addition, or as an alternative to slices and respective syntax elements, tile groups and/or tiles and respective syntax elements may be generated or used.

Entropy Coding

The entropy encoding unit 270 is configured to apply, for example, an entropy encoding algorithm or scheme (e.g. a variable length coding (VLC) scheme, an context adaptive VLC scheme (CAVLC), an arithmetic coding scheme, a binarization, a context adaptive binary arithmetic coding (CABAC), syntax-based context-adaptive binary arithmetic coding

(SBAC), probability interval partitioning entropy (PIPE) coding or another entropy encoding methodology or technique) or bypass (no compression) on the quantized coefficients 209, inter prediction parameters, intra prediction parameters, loop filter parameters and/or other syntax elements to obtain encoded picture data 21 which can be output via the output 272, e.g. in the form of an encoded bitstream 21, so that, e.g., the video decoder 30 may receive and use the parameters for decoding, . The encoded bitstream 21 may be transmitted to video decoder 30, or stored in a memory for later transmission or retrieval by video decoder 30.

Other structural variations of the video encoder 20 can be used to encode the video stream. For example, a non-transform based encoder 20 can quantize the residual signal directly without the transform processing unit 206 for certain blocks or frames. In another implementation, an encoder 20 can have the quantization unit 208 and the inverse quantization unit 210 combined into a single unit.

15 Decoder and Decoding Method

FIG. 3 shows an example of a video decoder 30 that is configured to implement the techniques of this present application. The video decoder 30 is configured to receive encoded picture data 21 (e.g., encoded bitstream 21), e.g., encoded by encoder 20, to obtain a decoded picture 331. The encoded picture data or bitstream comprises information for decoding the encoded picture data, e.g., data that represents picture blocks of an encoded video slice (and/or tile groups or tiles) and associated syntax elements.

In the example of FIG. 3, the decoder 30 comprises an entropy decoding unit 304, an inverse quantization unit 310, an inverse transform processing unit 312, a reconstruction unit 314 (e.g., a summer 314), a loop filter 320, a decoded picture buffer (DPB) 330, a mode application unit 360, an inter prediction unit 344 and an intra prediction unit 354. Inter prediction unit 344 may be or include a motion compensation unit. Video decoder 30 may, in some examples, perform a decoding pass generally reciprocal to the encoding pass described with respect to video encoder 100 from FIG. 2.

As explained with regard to the encoder 20, the inverse quantization unit 210, the inverse transform processing unit 212, the reconstruction unit 214, the loop filter 220, the decoded picture buffer (DPB) 230, the inter prediction unit 344 and the intra prediction unit 354 are also referred to as forming the “built-in decoder” of video encoder 20. Accordingly, the

inverse quantization unit 310 may be identical in function to the inverse quantization unit 110, the inverse transform processing unit 312 may be identical in function to the inverse transform processing unit 212, the reconstruction unit 314 may be identical in function to reconstruction unit 214, the loop filter 320 may be identical in function to the loop filter 220, and the decoded picture buffer 330 may be identical in function to the decoded picture buffer 230. Therefore, the explanations provided for the respective units and functions of the video 20 encoder apply correspondingly to the respective units and functions of the video decoder 30.

10 Entropy Decoding

The entropy decoding unit 304 is configured to parse the bitstream 21 (or in general encoded picture data 21) and perform, for example, entropy decoding to the encoded picture data 21 to obtain, e.g., quantized coefficients 309 and/or decoded coding parameters (not shown in FIG. 3), e.g. any or all of inter prediction parameters (e.g. reference picture index and motion vector), intra prediction parameter (e.g. intra prediction mode or index), transform parameters, quantization parameters, loop filter parameters, and/or other syntax elements. Entropy decoding unit 304 may be configured to apply the decoding algorithms or schemes corresponding to the encoding schemes as described with regard to the entropy-encoding unit 270 of the encoder 20. Entropy decoding unit 304 may be further configured to provide inter prediction parameters, intra prediction parameter and/or other syntax elements to the mode application unit 360 and other parameters to other units of the decoder 30. Video decoder 30 may receive the syntax elements at the video slice level and/or the video block level. In addition, or as an alternative to slices and respective syntax elements, tile groups and/or tiles and respective syntax elements may be received and/or used.

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Inverse Quantization

The inverse quantization unit 310 may be configured to receive quantization parameters (QP) (or in general information related to the inverse quantization) and quantized coefficients from the encoded picture data 21 (e.g. by parsing and/or decoding, e.g. by entropy decoding unit 304) and to apply based on the quantization parameters an inverse quantization on the decoded quantized coefficients 309 to obtain dequantized coefficients 311, which may also be referred to as transform coefficients 311. The inverse quantization process may include use of a quantization parameter determined by video encoder 20 for each video block in the

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video slice (or tile or tile group) to determine a degree of quantization and, likewise, a degree of inverse quantization that should be applied.

Inverse Transform

5 Inverse transform processing unit 312 may be configured to receive dequantized coefficients 311, also referred to as transform coefficients 311, and to apply a transform to the dequantized coefficients 311 in order to obtain reconstructed residual blocks 213 in the sample domain. The reconstructed residual blocks 213 may also be referred to as transform blocks 313. The transform may be an inverse transform, e.g., an inverse DCT, an inverse
10 DST, an inverse integer transform, or a conceptually similar inverse transform process. The inverse transform processing unit 312 may be further configured to receive transform parameters or corresponding information from the encoded picture data 21 (e.g., by parsing and/or decoding, e.g., by entropy decoding unit 304) to determine the transform to be applied to the dequantized coefficients 311.

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Reconstruction

The reconstruction unit 314 (e.g., adder or summer 314) may be configured to add the reconstructed residual block 313, to the prediction block 365 to obtain a reconstructed block 315 in the sample domain, e.g., by adding the sample values of the reconstructed residual
20 block 313 and the sample values of the prediction block 365.

Filtering

The loop filter unit 320 (either in the coding loop or after the coding loop) is configured to filter the reconstructed block 315 to obtain a filtered block 321, e.g., to smooth pixel
25 transitions, or otherwise improve the video quality. The loop filter unit 320 may comprise one or more loop filters such as a de-blocking filter, a sample-adaptive offset (SAO) filter or one or more other filters, e.g., an adaptive loop filter (ALF), a noise suppression filter (NSF), or any combination thereof. In an example, the loop filter unit 220 may comprise a de-blocking filter, a SAO filter and an ALF filter. The order of the filtering process may be the deblocking
30 filter, SAO and ALF. In another example, a process called the luma mapping with chroma scaling (LMCS) (namely, the adaptive in-loop resaper) is added. This process is performed before deblocking. In another example, the deblocking filter process may be also applied to internal sub-block edges, e.g., affine sub-blocks edges, ATMVP sub-blocks edges, sub-block transform (SBT) edges and intra sub-partition (ISP) edges. Although the loop filter unit 320

is shown in FIG. 3 as being an in loop filter, in other configurations, the loop filter unit 320 may be implemented as a post loop filter.

Decoded Picture Buffer

5 The decoded video blocks 321 of a picture are then stored in decoded picture buffer 330, which stores the decoded pictures 331 as reference pictures for subsequent motion compensation for other pictures and/or for output respectively display.

10 The decoder 30 is configured to output the decoded picture 311, e.g., via output 312, for presentation or viewing to a user.

Prediction

The inter prediction unit 344 may be identical to the inter prediction unit 244 (in particular to the motion compensation unit) and the intra prediction unit 354 may be identical to the inter prediction unit 254 in function, and performs split or partitioning decisions and prediction based on the partitioning and/or prediction parameters or respective information received from the encoded picture data 21 (e.g., by parsing and/or decoding, e.g., by entropy decoding unit 304). Mode application unit 360 may be configured to perform the prediction (intra or inter prediction) per block based on reconstructed pictures, blocks or respective samples (filtered or unfiltered) to obtain the prediction block 365.

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When the video slice is coded as an intra coded (I) slice, intra prediction unit 354 of mode application unit 360 is configured to generate prediction block 365 for a picture block of the current video slice based on a signaled intra prediction mode and data from previously decoded blocks of the current picture. When the video picture is coded as an inter coded (i.e., B, or P) slice, inter prediction unit 344 (e.g., motion compensation unit) of mode application unit 360 is configured to produce prediction blocks 365 for a video block of the current video slice based on the motion vectors and other syntax elements received from entropy decoding unit 304. For inter prediction, the prediction blocks may be produced from one of the reference pictures within one of the reference picture lists. Video decoder 30 may construct the reference frame lists, List 0 and List 1, using default construction techniques based on reference pictures stored in DPB 330. The same or similar may be applied for or by embodiments using tile groups (e.g., video tile groups) and/or tiles (e.g., video tiles) in

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addition or alternatively to slices (e.g., video slices), e.g., a video may be coded using I, P or B tile groups and /or tiles.

Mode application unit 360 is configured to determine the prediction information for a video
5 block of the current video slice by parsing the motion vectors or related information and other
syntax elements, and uses the prediction information to produce the prediction blocks for the
current video block being decoded. For example, the mode application unit 360 uses some of
the received syntax elements to determine a prediction mode (e.g., intra or inter prediction)
used to code the video blocks of the video slice, an inter prediction slice type (e.g., B slice, P
10 slice, or GPB slice), construction information for one or more of the reference picture lists for
the slice, motion vectors for each inter encoded video block of the slice, inter prediction
status for each inter coded video block of the slice, and other information to decode the video
blocks in the current video slice. The same or similar may be applied for or by embodiments
using tile groups (e.g., video tile groups) and/or tiles (e.g., video tiles) in addition or
15 alternatively to slices (e.g., video slices), e.g., a video may be coded using I, P or B tile
groups and/or tiles.

Embodiments of the video decoder 30 as shown in FIG. 3 may be configured to partition
and/or decode the picture by using slices (also referred to as video slices), wherein a picture
20 may be partitioned into or decoded using one or more slices (typically non-overlapping), and
each slice may comprise one or more blocks (e.g., CTUs) or one or more groups of blocks
(e.g., tiles (H.265/HEVC and VVC) or bricks (VVC)).

Embodiments of the video decoder 30 as shown in FIG. 3 may be configured to partition
25 and/or decode the picture by using slices/tile groups (also referred to as video tile groups)
and/or tiles (also referred to as video tiles), wherein a picture may be partitioned into or
decoded using one or more slices/tile groups (typically non-overlapping), and each slice/tile
group may comprise, e.g. one or more blocks (e.g. CTUs) or one or more tiles, wherein each
tile, e.g. may be of rectangular shape and may comprise one or more blocks (e.g. CTUs), e.g.
30 complete or fractional blocks.

Other variations of the video decoder 30 can be used to decode the encoded picture data 21.
For example, the decoder 30 can produce the output video stream without the loop-filtering
unit 320. For example, a non-transform based decoder 30 can inverse-quantize the residual

signal directly without the inverse-transform processing unit 312 for certain blocks or frames. In another implementation, the video decoder 30 can have the inverse-quantization unit 310 and the inverse-transform processing unit 312 combined into a single unit.

5 It should be understood that, in the encoder 20 and the decoder 30, a processing result of a current step might be further processed and then output to the next step. For example, after interpolation filtering, motion vector derivation or loop filtering, a further operation, such as Clip or shift, may be performed on the processing result of the interpolation filtering, motion vector derivation or loop filtering.

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It should be noted that further operations might be applied to the derived motion vectors of current block (including but not limit to control point motion vectors of affine mode, sub-block motion vectors in affine, planar, ATMVP modes, temporal motion vectors, and so on). For example, the value of motion vector is constrained to a predefined range according to its
15 representing bit. If the representing bit of motion vector is bitDepth, then the range is $-2^{(\text{bitDepth}-1)} \sim 2^{(\text{bitDepth}-1)}-1$, where “^” means exponentiation. For example, if bitDepth is set equal to 16, the range is $-32768 \sim 32767$; if bitDepth is set equal to 18, the range is $-131072 \sim 131071$. For example, the value of the derived motion vector (e.g., the MVs of four 4x4 sub-blocks within one 8x8 block) is constrained such that the max difference between
20 integer parts of the four 4x4 sub-block MVs is no more than N pixels, such as no more than 1 pixel. Here provides two methods for constraining the motion vector according to the bitDepth.

FIG. 4 is a schematic diagram of a video coding device 400 according to an embodiment of the disclosure. The video coding device 400 is suitable for implementing the disclosed
25 embodiments as described herein. In an embodiment, the video coding device 400 may be a decoder such as video decoder 30 of FIG. 1A or an encoder such as video encoder 20 of FIG. 1A.

The video coding device 400 comprises ingress ports 410 (or input ports 410) and receiver
30 units (Rx) 420 for receiving data; a processor, logic unit, or central processing unit (CPU) 430 to process the data; transmitter units (Tx) 440 and egress ports 450 (or output ports 450) for transmitting the data; and a memory 460 for storing the data. The video coding device 400 may also comprise optical-to-electrical (OE) components and electrical-to-optical (EO)

components coupled to the ingress ports 410, the receiver units 420, the transmitter units 440, and the egress ports 450 for egress or ingress of optical or electrical signals.

The processor 430 is implemented by hardware and software. The processor 430 may be implemented as one or more CPU chips, cores (e.g., as a multi-core processor), FPGAs, ASICs, and DSPs. The processor 430 is in communication with the ingress ports 410, receiver units 420, transmitter units 440, egress ports 450, and memory 460. The processor 430 comprises a coding module 470. The coding module 470 implements the disclosed embodiments described above. For instance, the coding module 470 implements, processes, prepares, or provides the various coding operations. The inclusion of the coding module 470 therefore provides a substantial improvement to the functionality of the video coding device 400 and effects a transformation of the video coding device 400 to a different state. Alternatively, the coding module 470 is implemented as instructions stored in the memory 460 and executed by the processor 430.

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The memory 460 may comprise one or more disks, tape drives, and solid-state drives and may be used as an over-flow data storage device, to store programs when such programs are selected for execution, and to store instructions and data that are read during program execution. The memory 460 may be, for example, volatile and/or non-volatile and may be a read-only memory (ROM), random access memory (RAM), ternary content-addressable memory (TCAM), and/or static random-access memory (SRAM).

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FIG. 5 is a simplified block diagram of an apparatus **500** that may be used as either or both of the source device 12 and the destination device 14 from FIG. 1 according to an exemplary embodiment.

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A processor 502 in the apparatus 500 can be a central processing unit. Alternatively, the processor 502 can be any other type of device, or multiple devices, capable of manipulating or processing information now existing or hereafter developed. Although the disclosed implementations can be practiced with a single processor as shown, e.g., the processor 502, advantages in speed and efficiency can be achieved using more than one processor.

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A memory 504 in the apparatus 500 can be a read only memory (ROM) device or a random access memory (RAM) device in an implementation. Any other suitable type of storage device can be used as the memory 504. The memory 504 can include code and data 506 that is accessed by the processor 502 using a bus 512. The memory 504 can further include an operating system 508 and application programs 510, the application programs 510 including at least one program that permits the processor 502 to perform the methods described here. For example, the application programs 510 can include applications 1 through N, which further include a video coding application that performs the methods described here. The apparatus 500 can also include one or more output devices, such as a display 518. The display 518 may be, in one example, a touch sensitive display that combines a display with a touch sensitive element that is operable to sense touch inputs. The display 518 can be coupled to the processor 502 via the bus 512.

Although depicted here as a single bus, the bus 512 of the apparatus 500 can be composed of multiple buses. Further, the secondary storage 514 can be directly coupled to the other components of the apparatus 500 or can be accessed via a network and can comprise a single integrated unit such as a memory card or multiple units such as multiple memory cards. The apparatus 500 can thus be implemented in a wide variety of configurations.

The usage of sequence parameters set (SPS) flags is well-known technique (e.g., from AVC, HEVC, VVC) to control the coding algorithms used for reconstructing a picture from its coded representation in the bitstream. For instance, if `sps_sao_enabled` flag is 1 then SAO algorithm is used to obtain the reconstructed picture, otherwise if `sps_sao_enabled` flag is 0 then SAO is not used and similar to any of existing SPS control flag.

25 Profiling mechanism.

An important task in video codecs are is profiles definition, which is used to guarantee that video decoder is compatible with a bitstream it receives. For this purpose, a video coding standard normally defines several sets of capabilities, which are referred to as profiles, targeting specific classes of applications. These are declared using a profile code (`profile_idc`) and sometimes a set of additional constraints applied in the encoder. The profile code and indicated constraints allow a decoder to recognize the requirements for decoding that specific bitstream. (And in many system environments, only one or two profiles are allowed to be used, so decoders in those environments do not need to be concerned with recognizing the less commonly used profiles). In MPEG-5/EVC besides `profile_idc` mechanism there is an

extension of coding tools restriction called toolset_idc method. It assumes signalling of an additional array of {0,1} elements, where each bit corresponds to one specific codec feature, e.g., coding algorithm influences decoded picture, controlled by SPS control flag and put additional limitation on the usage of this tool in a following way: if a specific bit in the toolset_idc equals to 1, then the corresponding SPS flag can be either 1 or 0. Otherwise, the corresponding SPS flag shall be equal to 0. More general, any certain SPS flag shall be less or equal than correspondent bit in toolse_idc array.

The following syntax table provides the method of EVC toolset_idc signalling.

10

seq_parameter_set_rbsp() {	Descriptor
profile_idc	u(8)
level_idc	u(8)
toolset_idc	u(32)

The following table provides the SPS flags restrictions based on toolset_idc values in EVC.

tools_idc binIdx	SPS tool flag	Conformance requirement
0	sps_btt_flag	sps_btt_flag <= toolset_idc & 0x1
1	sps_suco_flag	sps_suco_flag <= toolset_idc & 0x2
2	sps_amvr_flag	sps_amvr_flag <= toolset_idc & 0x4
3	sps_mmvd_flag	sps_mmvd_flag <= toolset_idc & 0x8
4	sps_affine_flag	sps_affine_flag <= toolset_idc & 0x10
5	sps_dmvr_flag	sps_dmvr_flag <= toolset_idc & 0x20
6	sps_alf_flag	sps_alf_flag <= toolset_idc & 0x40
7	sps_admvp_flag	sps_admvp_flag <= toolset_idc & 0x80
8	sps_eipd_flag	sps_eipd_flag <= toolset_idc & 0x100
9	sps_adcc_flag	sps_adcc_flag <= toolset_idc & 0x200
10	sps_amis_flag	sps_amis_flag <= toolset_idc & 0x400
11	sps_ibc_flag	sps_ibc_flag <= toolset_idc & 0x800
12	sps_iqt_flag	sps_iqt_flag <= toolset_idc & 0x1000
13	sps_htdf_flag	sps_htdf_flag <= toolset_idc & 0x2000
14	sps_addb_flag	sps_addb_flag <= toolset_idc & 0x4000
15	sps_cm_init_flag	sps_cm_init_flag <= toolset_idc & 0x8000
16	sps_ats_flag	sps_ats_flag <= toolset_idc & 0x10000
17	sps_rpl_flag	sps_rpl_flag <= toolset_idc & 0x20000
18	sps_pocs_flag	sps_pocs_flag <= toolset_idc & 0x40000
19	sps_dquant_flag	sps_dquant_flag <= toolset_idc & 0x80000
20..31	Reserved for future use by ISO/IEC.	Reserved for future use by ISO/IEC.

It should be noted that in the prior art toolset_idc mechanism only allows to restrict an SPS flag value to 0, there is no method to restrict the SPS flag to 1.

5 In view of this, the present disclosure overcomes this problem by extending the toolset_idc mechanism so as to support the functionality from both low and high boundary. In other words, the solution according to the present disclosure can be used to force both 0 and 1 SPS flag value.

10 In order to achieve this solution, the present disclosure introduces one additional syntax element to sps, called tools_idc_L, which is intended to restrict SPS flags from the lower boundary, i.e. the minimum allowed value of the respective SPS flag.

15 It should be noted that the additional syntax element may also be denoted as tools_idc_l, see below, intending the same purpose, namely restricting SPS flags from the lower boundary, i.e., the minimum allowed value of the respective SPS flag.

20 In a first embodiment of the current invention in addition to tools_idc (tools_idc_H) SPS flag one more SPS flag tools_idc_L is introduced. The following table provides an example of SPS signalling according to the embodiment.

seq_parameter_set_rbsp() {	Descriptor
profile_idc	u(8)
level_idc	u(8)
toolset_idc_H	u(32)
toolset_idc_L	u(32)

The usage of toolset_idc_H and toolset_idc_L syntax elements is given below.

tools_idc binidx	SPS tool flag	Conformance requirement
0	sps_btt_flag	sps_btt_flag <= tools_idc_H & 0x1 && sps_btt_flag >= tools_idc_L & 0x1
1	sps_suco_flag	sps_suco_flag <= toolset_idc_H & 0x2 && sps_suco_flag >= tools_idc_L & 0x2
2	sps_amvr_flag	sps_amvr_flag <= toolset_idc_H & 0x4 && sps_amvr_flag >= tools_idc_L & 0x4
3	sps_mmvd_flag	sps_mmvd_flag <= tools_idc_H & 0x8 && sps_mmvd_flag >= tools_idc_L & 0x8
4	sps_affine_flag	sps_affine_flag <= tools_idc_H & 0x10 && sps_affine_flag >= tools_idc_L & 0x10
5	sps_dmvr_flag	sps_dmvr_flag <= tools_idc_H & 0x20 && sps_dmvr_flag >= tools_idc_L & 0x20
6	sps_alf_flag	sps_alf_flag <= tools_idc_H & 0x40 && sps_alf_flag >= tools_idc_L & 0x40
7	sps_admvp_flag	sps_admvp_flag <= tools_idc_H & 0x80 && sps_admvp_flag >= tools_idc_L & 0x80
8	sps_eipd_flag	sps_eipd_flag <= tools_idc_H & 0x100 && sps_eipd_flag >= tools_idc_L & 0x100
9	sps_adcc_flag	sps_adcc_flag <= tools_idc_H & 0x200 && sps_adcc_flag >= tools_idc_L & 0x200
10	sps_amis_flag	sps_amis_flag <= tools_idc_H & 0x400 && sps_amis_flag >= tools_idc_L & 0x400
11	sps_ibc_flag	sps_ibc_flag <= tools_idc_H & 0x800 && sps_ibc_flag >= tools_idc_L & 0x800
12	sps_iqt_flag	sps_iqt_flag <= tools_idc_H & 0x1000 && sps_iqt_flag >= tools_idc_L & 0x1000
13	sps_htdf_flag	sps_htdf_flag <= tools_idc_H & 0x2000 && sps_htdf_flag >= tools_idc_L & 0x2000
14	sps_addb_flag	sps_addb_flag <= tools_idc_H & 0x4000 && sps_addb_flag >= tools_idc_L & 0x4000
15	sps_cm_init_flag	sps_cm_init_flag <= tools_idc_H & 0x8000 && sps_cm_init_flag >= tools_idc_L & 0x8000
16	sps_ats_flag	sps_ats_flag <= tools_idc_H & 0x10000 && sps_ats_flag >= tools_idc_L & 0x10000
17	sps_rpl_flag	sps_rpl_flag <= tools_idc_H & 0x20000 && sps_rpl_flag >= tools_idc_L & 0x20000
18	sps_pocs_flag	sps_pocs_flag <= tools_idc_H & 0x40000 && sps_pocs_flag >= tools_idc_L & 0x40000
19	sps_dquant_flag	sps_dquant_flag <= tools_idc_H & 0x80000 && sps_dquant_flag >= tools_idc_L & 0x80000
20	sps_addb_flag	sps_addb_flag <= tools_idc_H & 0x100000 && sps_addb_flag >= tools_idc_L & 0x100000
21..31	Reserved for future use by ISO/IEC.	Reserved for future use by ISO/IEC.

- sps_btt_flag equal to 1 specifies that the binary and ternary splits are used. sps_btt_flag equal to 0 specifies that the binary and ternary splits are not used and the quad split is only used.
- sps_suco_flag equal to 1 specifies that the split unit coding ordering is used. sps_suco_flag equal to 0 specifies that the split unit coding ordering is not used.
- 5 sps_affine_flag equal to 1 specifies that the affine model based motion compensation can be used for inter prediction. sps_affine_flag equal to 0 specifies that the syntax shall be constrained such that no affine model based motion compensation is used in the CVS, and affine_flag, affine_merge_idx and affine_mode_flag are not present in the coding unit syntax of the CVS. When sps_affine_flag is not present, it is inferred to be equal to 0.
- 10 sps_amvr_flag equal to 1 specifies that the adaptive motion vector resolution is used. sps_amvr_flag equal to 0 specifies that the adaptive motion vector resolution is not used. When sps_amvr_flag is not present, it is inferred to be equal to 0.
- sps_dmvr_flag equal to 1 specifies that decoder-side motion vector refinement can be used. sps_dmvr_flag equal to 0 specifies that decoder-side motion vector refinement is not used.
- 15 When sps_dmvr_flag is not presented, it is inferred to be equal to 0.
- sps_mmvd_flag equal to 1 specifies that MMVD can be used. sps_mmvd_flag equal to 0 specifies that MMVD is not used. When sps_mmvd_flag is not present, it is inferred to be equal to 0.
- sps_alf_flag equal to 1 specifies that the adaptive loop filter can be applied. sps_alf_flag equal to 0 specifies that the adaptive loop filter is not applied.
- 20 sps_admvp_flag equal to 1 specifies that the advanced motion vector prediction, signalling and interpolation are used. sps_admvp_flag equal to 0 specifies that the advanced motion vector prediction, signalling and interpolation are not used.
- sps_eipd_flag equal to 1 specifies that the extended intra prediction modes are used.
- 25 sps_eipd_flag equal to 0 specifies that the extended intra prediction modes are not used.
- sps_ibc_flag equal to 1 specifies that the intra block copy can be used. sps_ibc_flag equal to 0 specifies that the intra block copy is not used. When sps_ibc_flag is not present, it is inferred to be equal to 0.
- sps_cm_init_flag equal to 1 specifies that the context modeling and initialization processes are used. sps_cm_init_flag equal to 0 specifies that the context modeling and initialization processes are not used.
- 30 sps_adcc_flag equal to 1 specifies that the advanced residual coding is used. sps_adcc_flag equal to 0 specifies that the run-length residual coding is used. When sps_adcc_flag is not presented, it is inferred to be equal to 0.

- sps_iqt_flag equal to 1 specifies that the improved quantization and transform are used.
sps_iqt_flag equal to 0 specifies that the improved quantization and transform are not used.
sps_ats_flag equal to 1 specifies that ats_cu_intra_flag and ats_cu_inter_flag may be present in the residual coding syntax of the CVS. sps_ats_flag equal to 0 specifies that
- 5 ats_cu_intra_flag and ats_cu_inter_flag are not present in the residual coding syntax of the CVS. When not present, the value of sps_ats_flag is inferred to be equal to 0.
sps_addb_flag equal to 1 specifies that the advanced deblocking filter can be applied.
sps_addb_flag equal to 0 specifies that the deblocking filter can be applied.
sps_alf_flag equal to 1 specifies that the adaptive loop filter can be applied. sps_alf_flag
- 10 equal to 0 specifies that the adaptive loop filter is not applied.
sps_htdf_flag equal to 1 specifies that the hadamard transform domain filter can be applied.
sps_htdf_flag equal to 0 specifies that the hadamard transform domain filter is not applied.
sps_rpl_flag equal to 1 specifies that syntax related to reference picture lists is present.
sps_rpl_flag equal to 0 specifies that syntax related to reference picture lists is not present.
- 15 sps_pocs_flag equal to 1 specifies that syntax related to picture order count is present.
sps_pocs_flag equal to 0 specifies that syntax related to picture order count is not present.
sps_dquant_flag equal to 1 specifies that the improved delta qp signalling processes is used.
sps_dquant_flag equal to 0 specifies that the improved delta qp signalling process is not used.
sps_dquant_flag shall be equal to 0 when both sps_btt_flag and sps_admvp_flag are equal to
- 20 0.
sps_cm_init_flag equal to 1 specifies that the context modeling and initialization processes are used. sps_cm_init_flag equal to 0 specifies that the context modeling and initialization processes are not used.
sps_addb_flag equal to 1 specifies that the advanced deblocking filter can be applied.
- 25 sps_addb_flag equal to 0 specifies that the deblocking filter can be applied.
In other words, all specific SPS flags shall be in range, which is defined by toolset_idc_H and toolset_idc_L syntax elements.

It should be noted that tables above provide just examples of usage the technology and it be

30 simply applied for other set of SPS flags and/or other mapping between SPS flags and arrays of {0,1} elements.

In a modification of the first embodiment of the current invention in addition to tools_idc (tools_idc_h) SPS flag one more SPS flag tools_idc_h is introduced. The following table provides an example of SPS signalling according to this modified embodiment.

seq_parameter_set_rbsp() {	Descriptor
profile_idc	u(8)
level_idc	u(8)
toolset_idc_h	u(32)
toolset_idc_l	u(32)

5

The usage of toolset_idc_h and toolset_idc_l syntax elements is given below.

toolset_idc_h indicates set of constraints to which the CVS conforms as specified in the following table.

10 If a particular bit in syntax element toolset_idc_h is equal to 0, the corresponding, as per the following table, SPS flag shall be equal to 0.

Otherwise, when the bit value in syntax element toolset_idc_h is equal to 1, the corresponding, as per the following table, SPS flag value is not constrained.

toolset_idc_l indicates set of constraints to which the CVS conforms as specified in the following table.

15 If a particular bit in syntax element toolset_idc_l is equal to 1, the corresponding, as per the following table, SPS flag shall be equal to 1.

Otherwise, when the bit value in syntax element toolset_idc_l is equal to 0, the corresponding, as per the following table, SPS flag value is not constrained.

The value of toolset_idc_l shall satisfy the following constraint:

20 — The value of (toolset_idc_l | toolset_idc_h) shall be equal to toolset_idc_h.

tools_idc binidx	SPS tool flag(or SPS flag)	Conformance requirement
0	sps_btt_flag	sps_btt_flag <= toolset_idc_h & 0x1 && sps_btt_flag >= toolset_idc_l & 0x1
1	sps_suco_flag	sps_suco_flag <= (toolset_idc_h & 0x2) >> 1 && sps_suco_flag >= (toolset_idc_l & 0x2) >> 1
2	sps_amvr_flag	sps_amvr_flag <= (toolset_idc_h & 0x4) >> 2 && sps_amvr_flag >= (toolset_idc_l & 0x4) >> 2
3	sps_mmvd_flag	sps_mmvd_flag <= (toolset_idc_h & 0x8) >> 3 && sps_mmvd_flag >= (toolset_idc_l & 0x8) >> 3
4	sps_affine_flag	sps_affine_flag <= (toolset_idc_h & 0x10) >> 4 && sps_affine_flag >= (toolset_idc_l & 0x10) >> 4
5	sps_dmvr_flag	sps_dmvr_flag <= (toolset_idc_h & 0x20) >> 5 && sps_dmvr_flag >= (toolset_idc_l & 0x20) >> 5
6	sps_alf_flag	sps_alf_flag <= (toolset_idc_h & 0x40) >> 6 && sps_alf_flag >= (toolset_idc_l & 0x40) >> 6
7	sps_admvp_flag	sps_admvp_flag <= (toolset_idc_h & 0x80) >> 7 && sps_admvp_flag >= (toolset_idc_l & 0x80) >> 7
8	sps_eipd_flag	sps_eipd_flag <= (toolset_idc_h & 0x100) >> 8 && sps_eipd_flag >= (toolset_idc_l & 0x100) >> 8
9	sps_adcc_flag	sps_adcc_flag <= (toolset_idc_h & 0x200) >> 9 && sps_adcc_flag >= (toolset_idc_l & 0x200) >> 9
10	sps_ibc_flag	sps_ibc_flag <= (toolset_idc_h & 0x400) >> 10 && sps_ibc_flag >= (toolset_idc_l & 0x400) >> 10
11	sps_iqt_flag	sps_iqt_flag <= (toolset_idc_h & 0x800) >> 11 && sps_iqt_flag >= (toolset_idc_l & 0x800) >> 11
12	sps_htdf_flag	sps_htdf_flag <= (toolset_idc_h & 0x1000) >> 12 && sps_htdf_flag >= (toolset_idc_l & 0x1000) >> 12
13	sps_addb_flag	sps_addb_flag <= (toolset_idc_h & 0x2000) >>13 && sps_addb_flag >= (toolset_idc_l & 0x2000) >>13
14	sps_cm_init_flag	sps_cm_init_flag <= (toolset_idc_h & 0x4000) >>14 && sps_cm_init_flag >= (toolset_idc_l & 0x4000) >>14
15	sps_ats_flag	sps_ats_flag <= (toolset_idc_h & 0x8000) >> 15 && sps_ats_flag >= (toolset_idc_l & 0x8000) >> 15
16	sps_rpl_flag	sps_rpl_flag <= (toolset_idc_h & 0x10000) >> 16 && sps_rpl_flag >= (toolset_idc_l & 0x10000) >> 16
17	sps_pocs_flag	sps_pocs_flag <= (toolset_idc_h & 0x20000) >> 17 && sps_pocs_flag >= (toolset_idc_l & 0x20000) >> 17
18	sps_dquant_flag	sps_dquant_flag <= (toolset_idc_h & 0x40000) >> 18 && sps_dquant_flag >= (toolset_idc_l & 0x40000) >> 18
19	sps_dra_flag	sps_dra_flag <= (toolset_idc_h & 0x80000) >> 19 && sps_dra_flag >= (toolset_idc_l & 0x80000) >> 19
20	sps_hmvp_flag	sps_hmvp_flag <= (toolset_idc_h & 0x100000) >> 20 && sps_hmvp_flag >= (toolset_idc_l & 0x100000) >> 20
21..31	Reserved for future use by ISO/IEC.	Reserved for future use by ISO/IEC.

In other words, all specific sps flags shall be in range, which is defined by toolset_idc_h and toolset_idc_l syntax elements.

It should be noted that also the tables of the modified first embodiment shown above provide just examples of usage the technology and it be simply applied for other set of SPS flags and/or other mapping between SPS flags and arrays of {0,1} elements.

5 FIG. 8 illustrates a flowchart of a method for decoding of a video bitstream according to an embodiment of the present disclosure. The method illustrated in FIG. 8 is a method for decoding of a video bitstream implemented by a decoding device, wherein the video bitstream includes data representing one or more sequence parameter set, SPS, flags, the method comprising: for an SPS flag of the one or more SPS flags, (1601) obtaining two
10 variables of the SPS flag, respectively, by parsing the video bitstream, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag; (1603) obtaining a value of the SPS flag, by parsing the video bitstream; (1605) evaluating whether the value of the SPS flag is valid based on the values of the two variables;
15 and in case that the value of the SPS flag is valid, (1607) decoding the video bitstream according to the value of the SPS flag.

FIG. 9 illustrates a decoder 30, may be corresponding the method of FIG. 8, for decoding of a video bitstream according to an embodiment of the present disclosure. The decoder 30
20 illustrated in FIG. 9 is a decoder 30 for decoding of a video bitstream, wherein the video bitstream includes data representing one or more sequence parameter set (SPS) flags, the decoder comprising: a first obtaining unit 3001 configured to obtain two variables for an SPS flag of the one or more SPS flags, respectively, by parsing the video bitstream, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and
25 wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag; a second obtaining unit 3003 configured to obtain a value of the SPS flag, by parsing the video bitstream; an evaluating unit 3005 configured to evaluate whether the value of the SPS flag is valid based on the values of the two variables; and a decoding unit 3007 configured to decode the video bitstream according to the value of the SPS flag in case that
30 the value of the SPS flag is valid.

Wherein the unit may be a software module for execution by the processors, or processing circuitry.

Wherein both of the first obtaining unit 3001 and the second obtaining unit 3003 may be entropy decoding unit 304. Both of the evaluating unit 3005 and the decoding unit 3007 may be a unit related to the SPS flag in fig. 3. The decoder 30 may be the destination device 14,
5 the apparatus 500, the video decoder 3206 or the terminal device 3106.

FIG. 10 illustrates a flowchart of a method for encoding of a video bitstream according to an embodiment of the present disclosure. The method illustrated in FIG. 10 is a method for
10 encoding of a video bitstream implemented by an encoding device, wherein the video bitstream includes data representing one or more sequence parameter set (SPS) flags, the method comprising: for an SPS flag of the one or more SPS flags, (1701) setting two variables of the SPS flag, respectively, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of
15 the two variables is the maximum allowed value of the SPS flag; (1703) determining the value of the SPS flag according to the two variables of the SPS flag; and (1705) encoding the value of the SPS flag and the two variables of the SPS flag into the video bitstream.

FIG. 11 illustrates an encoder 20, may be corresponding the method of FIG. 10, for encoding
20 of a video bitstream according to an embodiment of the present disclosure. The encoder illustrated in FIG. 11 is an encoder 20 for encoding of a video bitstream, wherein the video bitstream includes data representing one or more sequence parameter set, SPS, flags, the encoder comprising: an setting unit 2001 configured to set two variables for an SPS flag of the one or more SPS flags, respectively, wherein the value of one variable of the two
25 variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag; a determining unit 2003 configured to determine the value of the SPS flag according to the two variables of the SPS flag; and an encoding unit 2005 configured to encode the value of the SPS flag and the two variables of the SPS flag into the video bitstream.

30

Wherein the unit may be a software module for execution by the processors, or processing circuitry.

Wherein the encoding unit 2005 may be Entropy encoding unit 270. Both of the setting unit 2001 and the determining unit 2003 may be may be a unit related to the SPS flag in fig. 2. The encoder 20 may be the source device 12, or the apparatus 500.

5

The following provides an explanation of the applications of the encoding method as well as the decoding method as shown in the above-mentioned embodiments, and a system using them. FIG. 6 is a block diagram showing a content supply system 3100 for realizing content distribution service. This content supply system 3100 includes capture device 3102, terminal device 3106, and optionally includes display 3126. The capture device 3102 communicates with the terminal device 3106 over communication link 3104. The communication link may include the communication channel 13 described above. The communication link 3104 includes but not limited to WIFI, Ethernet, Cable, wireless (3G/4G/5G), USB, or any kind of combination thereof, or the like.

10

The capture device 3102 generates data, and may encode the data by the encoding method as shown in the above embodiments. Alternatively, the capture device 3102 may distribute the data to a streaming server (not shown in the Figures), and the server encodes the data and transmits the encoded data to the terminal device 3106. The capture device 3102 includes but not limited to camera, smart phone or Pad, computer or laptop, video conference system, PDA, vehicle mounted device, or a combination of any of them, or the like. For example, the capture device 3102 may include the source device 12 as described above. When the data includes video, the video encoder 20 included in the capture device 3102 may actually perform video encoding processing. When the data includes audio (i.e., voice), an audio encoder included in the capture device 3102 may actually perform audio encoding processing. For some practical scenarios, the capture device 3102 distributes the encoded video and audio data by multiplexing them together. For other practical scenarios, for example in the video conference system, the encoded audio data and the encoded video data are not multiplexed. Capture device 3102 distributes the encoded audio data and the encoded video data to the terminal device 3106 separately.

20

25

In the content supply system 3100, the terminal device 310 receives and reproduces the encoded data. The terminal device 3106 could be a device with data receiving and recovering capability, such as smart phone or Pad 3108, computer or laptop 3110, network video recorder (NVR)/ digital video recorder (DVR) 3112, TV 3114, set top box (STB) 3116, video conference system 3118, video surveillance system 3120, personal digital assistant (PDA) 3122,

30

vehicle mounted device 3124, or a combination of any of them, or the like capable of decoding the above-mentioned encoded data. For example, the terminal device 3106 may include the destination device 14 as described above. When the encoded data includes video, the video decoder 30 included in the terminal device is prioritized to perform video decoding. When the encoded data includes audio, an audio decoder included in the terminal device is prioritized to perform audio decoding processing.

For a terminal device with its display, for example, smart phone or Pad 3108, computer or laptop 3110, network video recorder (NVR)/ digital video recorder (DVR) 3112, TV 3114, personal digital assistant (PDA) 3122, or vehicle mounted device 3124, the terminal device can feed the decoded data to its display. For a terminal device equipped with no display, for example, STB 3116, video conference system 3118, or video surveillance system 3120, an external display 3126 is contacted therein to receive and show the decoded data.

When each device in this system performs encoding or decoding, the picture-encoding device or the picture-decoding device, as shown in the above-mentioned embodiments, can be used.

FIG. 7 is a diagram showing a structure of an example of the terminal device 3106. After the terminal device 3106 receives stream from the capture device 3102, the protocol proceeding unit 3202 analyzes the transmission protocol of the stream. The protocol includes but not limited to Real Time Streaming Protocol (RTSP), Hyper Text Transfer Protocol (HTTP), HTTP Live streaming protocol (HLS), MPEG-DASH, Real-time Transport protocol (RTP), Real Time Messaging Protocol (RTMP), or any kind of combination thereof, or the like.

After the protocol proceeding unit 3202 processes the stream, stream file is generated. The file is outputted to a demultiplexing unit 3204. The demultiplexing unit 3204 can separate the multiplexed data into the encoded audio data and the encoded video data. As described above, for some practical scenarios, for example in the video conference system, the encoded audio data and the encoded video data are not multiplexed. In this situation, the encoded data is transmitted to video decoder 3206 and audio decoder 3208 without through the demultiplexing unit 3204.

Via the demultiplexing processing, video elementary stream (ES), audio ES, and optionally subtitle are generated. The video decoder 3206, which includes the video decoder 30 as explained in the above-mentioned embodiments, decodes the video ES by the decoding method as shown in the above-mentioned embodiments to generate video frame, and feeds this data to the synchronous unit 3212. The audio decoder 3208, decodes the audio ES to generate audio frame, and feeds this data to the synchronous unit 3212. Alternatively, the video frame may store in a buffer (not shown in FIG. 7) before feeding it to the synchronous unit 3212. Similarly,

the audio frame may store in a buffer (not shown in FIG. 7) before feeding it to the synchronous unit 3212.

The synchronous unit 3212 synchronizes the video frame and the audio frame, and supplies the video/audio to a video/audio display 3214. For example, the synchronous unit 3212
5 synchronizes the presentation of the video and audio information. Information may code in the syntax using time stamps concerning the presentation of coded audio and visual data and time stamps concerning the delivery of the data stream itself.

If subtitle is included in the stream, the subtitle decoder 3210 decodes the subtitle, synchronizes it with the video frame and the audio frame, and supplies the video/audio/subtitle to a
10 video/audio/subtitle display 3216.

The present invention is not limited to the above-mentioned system, and either the picture-encoding device or the picture-decoding device in the above-mentioned embodiments can be incorporated into other system, for example, a car system.

15 Mathematical Operators

The mathematical operators used in this application are similar to those used in the C programming language. However, the results of integer division and arithmetic shift operations are defined more precisely, and additional operations are defined, such as
20 exponentiation and real-valued division. Numbering and counting conventions generally begin from 0, e.g., "the first" is equivalent to the 0-th, "the second" is equivalent to the 1-th, etc.

Arithmetic operators

25 The following arithmetic operators are defined as follows:

+	Addition
-	Subtraction (as a two-argument operator) or negation (as a unary prefix operator)
*	Multiplication, including matrix multiplication
x^y	Exponentiation. Specifies x to the power of y. In other contexts, such notation is used for superscripting not intended for interpretation as exponentiation.
/	Integer division with truncation of the result toward zero. For example, $7 / 4$ and $-7 / -4$ are truncated to 1 and $-7 / 4$ and $7 / -4$ are truncated to -1.
÷	Used to denote division in mathematical equations where no truncation or rounding is intended.
$\frac{x}{y}$	Used to denote division in mathematical equations where no truncation or rounding is intended.

$\sum_{i=x}^y f(i)$ The summation of $f(i)$ with i taking all integer values from x up to and including y .

$x \% y$ Modulus. Remainder of x divided by y , defined only for integers x and y with $x \geq 0$ and $y > 0$.

Logical operators

The following logical operators are defined as follows:

$x \&\& y$ Boolean logical "and" of x and y

$x \|\| y$ Boolean logical "or" of x and y

5 $!$ Boolean logical "not"

$x ? y : z$ If x is TRUE or not equal to 0, evaluates to the value of y ; otherwise, evaluates to the value of z .

Relational operators

10 The following relational operators are defined as follows:

$>$ Greater than

$>=$ Greater than or equal to

$<$ Less than

$<=$ Less than or equal to

15 $==$ Equal to

$!=$ Not equal to

20 When a relational operator is applied to a syntax element or variable that has been assigned the value "na" (not applicable), the value "na" is treated as a distinct value for the syntax element or variable. The value "na" is considered not to be equal to any other value.

Bit-wise operators

The following bit-wise operators are defined as follows:

25 $\&$ Bit-wise "and". When operating on integer arguments, operates on a two's complement representation of the integer value. When operating on a binary argument that contains fewer bits than another argument, the shorter argument is extended by adding more significant bits equal to 0.

30 $|$ Bit-wise "or". When operating on integer arguments, operates on a two's complement representation of the integer value. When operating on a binary argument that contains fewer bits than another argument, the shorter argument is extended by adding more significant bits equal to 0.

35 \wedge Bit-wise "exclusive or". When operating on integer arguments, operates on a two's complement representation of the integer value. When operating on a binary argument that contains fewer bits than another argument, the shorter argument is extended by adding more significant bits equal to 0.

$x \gg y$ Arithmetic right shift of a two's complement integer representation of x by y binary digits. This function is defined only for non-negative integer values of y . Bits shifted into the most significant bits (MSBs) as a result of the right shift have a value equal to the MSB of x prior to the shift operation.

$x \ll y$ Arithmetic left shift of a two's complement integer representation of x by y binary digits. This function is defined only for non-negative integer values of y . Bits shifted into the least significant bits (LSBs) as a result of the left shift have a value equal to 0.

5

Assignment operators

The following arithmetic operators are defined as follows:

- = Assignment operator
- ++ Increment, i.e., $x++$ is equivalent to $x = x + 1$; when used in an array index, evaluates to the value of the variable prior to the increment operation.
- Decrement, i.e., $x--$ is equivalent to $x = x - 1$; when used in an array index, evaluates to the value of the variable prior to the decrement operation.
- += Increment by amount specified, i.e., $x += 3$ is equivalent to $x = x + 3$, and $x += (-3)$ is equivalent to $x = x + (-3)$.
- = Decrement by amount specified, i.e., $x -= 3$ is equivalent to $x = x - 3$, and $x -= (-3)$ is equivalent to $x = x - (-3)$.

10

15

Range notation

The following notation is used to specify a range of values:

- $x = y..z$ x takes on integer values starting from y to z , inclusive, with x , y , and z being integer numbers and z being greater than y .

20

Mathematical functions

The following mathematical functions are defined:

25
$$\text{Abs}(x) = \begin{cases} x & ; \quad x \geq 0 \\ -x & ; \quad x < 0 \end{cases}$$

$\text{Asin}(x)$ the trigonometric inverse sine function, operating on an argument x that is in the range of -1.0 to 1.0 , inclusive, with an output value in the range of $-\pi/2$ to $\pi/2$, inclusive, in units of radians

30 $\text{Atan}(x)$ the trigonometric inverse tangent function, operating on an argument x , with an output value in the range of $-\pi/2$ to $\pi/2$, inclusive, in units of radians

$$\text{Atan2}(y, x) = \begin{cases} \text{Atan}\left(\frac{y}{x}\right) & ; \quad x > 0 \\ \text{Atan}\left(\frac{y}{x}\right) + \pi & ; \quad x < 0 \ \&\& \ y \geq 0 \\ \text{Atan}\left(\frac{y}{x}\right) - \pi & ; \quad x < 0 \ \&\& \ y < 0 \\ +\frac{\pi}{2} & ; \quad x = 0 \ \&\& \ y \geq 0 \\ -\frac{\pi}{2} & ; \quad \text{otherwise} \end{cases}$$

$\text{Ceil}(x)$ the smallest integer greater than or equal to x .

$\text{Clip1}_y(x) = \text{Clip3}(0, (1 \ll \text{BitDepth}_y) - 1, x)$

$\text{Clip1}_c(x) = \text{Clip3}(0, (1 \ll \text{BitDepth}_c) - 1, x)$

$$\text{Clip3}(x, y, z) = \begin{cases} x & ; \quad z < x \\ y & ; \quad z > y \\ z & ; \quad \text{otherwise} \end{cases}$$

$\text{Cos}(x)$ the trigonometric cosine function operating on an argument x in units of radians.

$\text{Floor}(x)$ the largest integer less than or equal to x .

$$\text{GetCurrMsb}(a, b, c, d) = \begin{cases} c + d & ; \quad b - a \geq d / 2 \\ c - d & ; \quad a - b > d / 2 \\ c & ; \quad \text{otherwise} \end{cases}$$

5 $\text{Ln}(x)$ the natural logarithm of x (the base- e logarithm, where e is the natural logarithm base constant 2.718 281 828...).

$\text{Log2}(x)$ the base-2 logarithm of x .

$\text{Log10}(x)$ the base-10 logarithm of x .

$$\text{Min}(x, y) = \begin{cases} x & ; \quad x \leq y \\ y & ; \quad x > y \end{cases}$$

10 $\text{Max}(x, y) = \begin{cases} x & ; \quad x \geq y \\ y & ; \quad x < y \end{cases}$

$\text{Round}(x) = \text{Sign}(x) * \text{Floor}(\text{Abs}(x) + 0.5)$

$$\text{Sign}(x) = \begin{cases} 1 & ; \quad x > 0 \\ 0 & ; \quad x == 0 \\ -1 & ; \quad x < 0 \end{cases}$$

$\text{Sin}(x)$ the trigonometric sine function operating on an argument x in units of radians

$\text{Sqrt}(x) = \sqrt{x}$

15 $\text{Swap}(x, y) = (y, x)$

$\text{Tan}(x)$ the trigonometric tangent function operating on an argument x in units of radians

Order of operation precedence

20 When an order of precedence in an expression is not indicated explicitly by use of parentheses, the following rules apply:

- Operations of a higher precedence are evaluated before any operation of a lower precedence.
- Operations of the same precedence are evaluated sequentially from left to right.

25 The table below specifies the precedence of operations from highest to lowest; a higher position in the table indicates a higher precedence.

For those operators that are also used in the C programming language, the order of precedence used in this Specification is the same as used in the C programming language.

30

Table: Operation precedence from highest (at top of table) to lowest (at bottom of table)

operations (with operands x, y, and z)
"x+", "x- -"
"!x", "-x" (as a unary prefix operator)
x^y
"x * y", "x / y", "x ÷ y", " $\frac{x}{y}$ ", "x % y"
"x + y", "x - y" (as a two-argument operator), " $\sum_{i=x}^y f(i)$ "
"x << y", "x >> y"
"x < y", "x <= y", "x > y", "x >= y"
"x == y", "x != y"
"x & y"
"x y"
"x && y"
"x y"
"x ? y : z"
"x.y"
"x = y", "x += y", "x -= y"

Text description of logical operations

5 In the text, a statement of logical operations as would be described mathematically in the following form:

```

    if( condition 0 )
        statement 0
    else if( condition 1 )
        statement 1
10    ...
        else /* informative remark on remaining condition */
            statement n
    
```

may be described in the following manner:

- 15 ... as follows / ... the following applies:
- If condition 0, statement 0
 - Otherwise, if condition 1, statement 1
 - ...
 - Otherwise (informative remark on remaining condition), statement n

20 Each "If ... Otherwise, if ... Otherwise, ..." statement in the text is introduced with "... as follows" or "... the following applies" immediately followed by "If ... ". The last condition of the "If ... Otherwise, if ... Otherwise, ..." is always an "Otherwise, ...". Interleaved "If ...

Otherwise, if ... Otherwise, ..." statements can be identified by matching "... as follows" or "... the following applies" with the ending "Otherwise, ...".

5 In the text, a statement of logical operations as would be described mathematically in the following form:

```

    if( condition 0a  &&  condition 0b )
      statement 0
    else if( condition 1a  ||  condition 1b )
      statement 1
10  ...
    else
      statement n

```

may be described in the following manner:

... as follows / ... the following applies:

- 15
- If all of the following conditions are true, statement 0:
 - condition 0a
 - condition 0b
 - Otherwise, if one or more of the following conditions are true, statement 1:
 - condition 1a
20 - condition 1b
 - ...
 - Otherwise, statement n

In the text, a statement of logical operations as would be described mathematically in the following form:

```

25  if( condition 0 )
      statement 0
    if( condition 1 )
      statement 1

```

may be described in the following manner:

- 30
- When condition 0, statement 0
 - When condition 1, statement 1

Although embodiments of the invention have been primarily described based on video coding, it should be noted that embodiments of the coding system 10, encoder 20 and decoder 30 (and correspondingly the system 10) and the other embodiments described herein may also be configured for still picture processing or coding, i.e. the processing or coding of an individual picture independent of any preceding or consecutive picture as in video coding. In general only inter-prediction units 244 (encoder) and 344 (decoder) may not be available in case the picture processing coding is limited to a single picture 17. All other functionalities (also referred to as tools or technologies) of the video encoder 20 and video decoder 30 may equally be used for still picture processing, e.g. residual calculation 204/304, transform 206, quantization 208, inverse quantization 210/310, (inverse) transform 212/312, partitioning 262/362, intra-prediction 254/354, and/or loop filtering 220, 320, and entropy coding 270 and entropy decoding 304.

Embodiments, e.g. of the encoder 20 and the decoder 30, and functions described herein, e.g. with reference to the encoder 20 and the decoder 30, may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on a computer-readable medium or transmitted over communication media as one or more instructions or code and executed by a hardware-based processing unit.

Computer-readable media may include computer-readable storage media, which corresponds to a tangible medium such as data storage media, or communication media including any medium that facilitates transfer of a computer program from one place to another, e.g., according to a communication protocol. In this manner, computer-readable media generally may correspond to (1) tangible computer-readable storage media, which is non-transitory, or (2) a communication medium such as a signal or carrier wave. Data storage media may be any available media that can be accessed by one or more computers or one or more processors to retrieve instructions, code and/or data structures for implementation of the techniques described in this disclosure. A computer program product may include a computer-readable medium.

By way of example, and not limiting, such computer-readable storage media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage, or other magnetic storage devices, flash memory, or any other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer. In addition, any connection is properly termed a computer-readable medium.

For example, if instructions are transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. It should be understood, however, that computer-readable storage media and data storage media do not include connections, carrier waves, signals, or other transitory media, but are instead directed to non-transitory, tangible storage media. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc, where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

Instructions may be executed by one or more processors, such as one or more digital signal processors (DSPs), general purpose microprocessors, application specific integrated circuits (ASICs), field programmable logic arrays (FPGAs), or other equivalent integrated or discrete logic circuitry. Accordingly, the term “processor,” as used herein may refer to any of the foregoing structure or any other structure suitable for implementation of the techniques described herein. In addition, in some aspects, the functionality described herein may be provided within dedicated hardware and/or software modules configured for encoding and decoding, or incorporated in a combined codec. In addition, the techniques could be fully implemented in one or more circuits or logic elements.

The techniques of this disclosure may be implemented in a wide variety of devices or apparatuses, including a wireless handset, an integrated circuit (IC) or a set of ICs (e.g., a chip set). Various components, modules, or units are described in this disclosure to emphasize functional aspects of devices configured to perform the disclosed techniques, but do not necessarily require realization by different hardware units. Rather, as described above, various units may be combined in a codec hardware unit or provided by a collection of interoperative hardware units, including one or more processors as described above, in conjunction with suitable software and/or firmware.

The present disclosure discloses the following twelve further aspects:

1. An aspect of a method of processing an image or video data, the method comprising: determining, based on a signaled property of a bitstream that comprises an encoded representation of the data, whether a decoder is able to decode the bitstream,
 - 5 wherein the bitstream conforms to a coding specification and comprises a plurality of sequence level (SPS) control flags; and
 - wherein for each element of a non-empty subset of the SPS control flags, two variables from $\{0,1\}$ set are signalled; and
 - wherein each element of the non-empty subset of the SPS control flags is equal to one
 - 10 of the signalled variables.
2. An aspect of a method of aspect 1, wherein the two variables from $\{0,1\}$ set L_i and H_i are signalled in the bitstream before the i -th SPS flag from the non-empty subset of the SPS control flags and wherein $L_i \leq sps_i \leq H_i$, where sps_i is the i -th SPS flag.
3. An aspect of a method of aspect 2, wherein the two variables from $\{0,1\}$ set corresponding
 - 15 to all SPS flags from the non-empty subset of the SPS control flags are signalled as two vectors with elements from $\{0,1\}$ set: $toolset_idc_L = L_0L_1, \dots, L_i, \dots, L_{n-1}$ and $toolset_idc_H = H_0H_1, \dots, H_i, \dots, H_{n-1}$, where n is a number of elements inside the subset of the SPS control flags.
4. An aspect of a method for decoding of a video bitstream implemented by a decoding device,
 - 20 wherein the video bitstream includes data representing a plurality of sequence level (SPS) control flags, the decoding method comprising: obtaining two variables for an SPS control flag of the SPS control flags, by parsing the video bitstream, wherein the value of one variable of the two variables is the lower bound of the value of the SPS control flag, and the value of another variable of the two variables is the maximum allowed value of the value of the SPS
 - 25 control flag;
 - Decoding an encoder picture referring to the SPS, according to the two variables.
5. An aspect of the method of aspect 4, the method further comprises: when both of the two variables are equal to 1, determining the value of the SPS control flag is 1 without parsing the video bitstream.
6. An aspect of the method of aspect 4, the method further comprises: when both of the two
 - 30 variables are equal to 0, determining the value of the SPS control flag is 0 without parsing the video bitstream.

7. An aspect of an encoder (20) comprising processing circuitry for carrying out the method according to any one of aspects 1 to 6.
8. An aspect of a decoder (30) comprising processing circuitry for carrying out the method according to any one of aspects 1 to 6.
- 5 9. An aspect of a computer program product comprising program code for performing the method according to any one of the preceding claims when executed on a computer or a processor.
- 10 10. An aspect of a decoder, comprising: one or more processors; and a non-transitory computer-readable storage medium coupled to the processors and storing programming for execution by the processors, wherein the programming, when executed by the processors, configures the decoder to carry out the method according to any one of the preceding aspects.
- 15 11. An aspect of an encoder, comprising: one or more processors; and a non-transitory computer-readable storage medium coupled to the processors and storing programming for execution by the processors, wherein the programming, when executed by the processors, configures the encoder to carry out the method according to any one of the preceding aspects.
12. An aspect of a non-transitory computer-readable medium carrying a program code which, when executed by a computer device, causes the computer device to perform the method of any one of the preceding aspects.

CLAIMS

1. A method for decoding of a video bitstream implemented by a decoding device, wherein the video bitstream includes data representing one or more sequence parameter set (SPS) flags, the method comprising:
- 5 for an SPS flag of the one or more SPS flags, obtaining two variables of the SPS flag, respectively, by parsing the video bitstream, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag;
- 10 obtaining a value of the SPS flag, by parsing the video bitstream;
- evaluating whether the value of the SPS flag is valid based on the values of the two variables; and
- in case that the value of the SPS flag is valid, decoding the video bitstream according to the value of the SPS flag.
- 15
2. The method of claim 1, wherein the method further comprises: in case the value of the value of the SPS flag is not valid, stop decoding the video bitstream.
3. The method of any one of claims 1 or 2, wherein the two variables of the SPS flag are
- 20 Boolean variables, wherein the two variables are respectively packed in two syntax elements, wherein the two variables correspond to a specific bit inside the two syntax elements, respectively.
4. The method of any one of claims 1 to 3, wherein the values of the two variables are from
- 25 a set $\{0,1\}$.
5. The method of any one of claims 1 to 4, wherein the value of the SPS flag is equal to one of the values of the variables.
- 30 6. The method of claim 5, wherein the values of the two variables are from the set $\{0,1\}$, are denoted l_i and h_i , and are signalled in the bitstream before the SPS flag and wherein $l_i \leq sps_i \leq h_i$, where sps_i is the value of the SPS flag.

7. The method of claim 6, wherein for all SPS flags of the one or more SPS flags, the two variables from the set $\{0,1\}$ are signalled by two vectors with elements from the set $\{0,1\}$: $toolset_idc_l = l_0 l_1, \dots, l_i, \dots, l_{n-1}$ and $toolset_idc_h = h_0 h_1, \dots, h_i, \dots, h_{n-1}$, where n is a number of the one or more SPS flags, and i is an integer.

5

8. A method for encoding of a video bitstream implemented by an encoding device, wherein the video bitstream includes data representing one or more sequence parameter set (SPS) flags, the method comprising:

for an SPS flag of the one or more SPS flags, setting two variables of the SPS flag,

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respectively, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag;

determining the value of the SPS flag according to the two variables of the SPS flag; and

encoding the value of the SPS flag and the two variables of the SPS flag into the video

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bitstream.

9. The method of claim 8, wherein in case the value of the one variable being the minimum allowed value of the SPS flag is equal to 1, determining the value of the SPS flag to be 1.

20

10. The method of claim 8, wherein in case the value of the one variable being the maximum allowed value of the SPS flag is equal to 0, determining the value of the SPS flag to be 0.

11. The method of claim 8, the method further comprising:

in case the values of both of the two variables of the SPS flag is equal to 1, determining the

25

value of the SPS flag to be 1, respectively.

12. The method of claim 8, the method further comprising:

in case the values of both of the two variables of the SPS flag is equal to 0, determining the value of the SPS flag to be 0, respectively.

30

13. The method of any one of claims 8 to 12, wherein the two variables of the SPS flag are Boolean variables, wherein the two variables are respectively packed in two syntax elements, wherein the two variables correspond to a specific bit inside the two syntax elements, respectively.

14. The method of any one of claims 8 to 13, wherein the values of the two variables are from a set $\{0,1\}$.
- 5 15. The method of any one of claims 8 to 14, wherein the value of the SPS flag is equal to one of the values of the variables.
16. The method of claim 15, wherein the values of the two variables are from a set $\{0,1\}$, are denoted l_i and h_i , and are signalled in the bitstream before the SPS flag and wherein $l_i \leq$
 10 $sps_i \leq h_i$, where sps_i is the value of the SPS flag.
17. The method of claim 16, wherein for all SPS flags of the one or more SPS flags, the two variables from the set $\{0,1\}$ are signalled by two vectors with elements from the set $\{0,1\}$:
 $toolset_idc_l = l_0 l_1, \dots, l_i, \dots, l_{n-1}$ and $toolset_idc_h = h_0 h_1, \dots, h_i, \dots, h_{n-1}$, where n is a
 15 number of the one or more SPS flags, and i is an integer.
18. An encoder (20) comprising processing circuitry for carrying out the method according to any one of claims 8 to 17.
- 20 19. A decoder (30) comprising processing circuitry for carrying out the method according to any one of claims 1 to 7.
20. A computer program product comprising program code for performing the method according to any one of the claims 1 to 17 when executed on a computer or a processor.
 25
21. A decoder, comprising:
 one or more processors; and
 a non-transitory computer-readable storage medium coupled to the processors and storing programming for execution by the processors, wherein the programming, when
 30 executed by the processors, configures the decoder to carry out the method according to any one of claims 1 to 7.

22. An encoder, comprising:
one or more processors; and
a non-transitory computer-readable storage medium coupled to the processors and
storing programming for execution by the processors, wherein the programming, when
5 executed by the processors, configures the encoder to carry out the method according to any
one of claims 8 to 17.
23. A non-transitory computer-readable medium carrying a program code which, when
executed by a computer device, causes the computer device to perform the method of any one
10 of claims 1 to 17.
24. A non-transitory storage medium which includes an encoded bitstream decoded by an
image decoding device, the bitstream being generated by dividing a frame of a video signal or
an image signal into a plurality blocks, and including a plurality of SPS flags, wherein the
15 bitstream further comprises two variables of an SPS flag, wherein the value of one variable of
the two variables is the value of the minimum allowed value of the SPS flag, and wherein the
value of the other variable of the two variables is the value of the maximum allowed value of
the SPS flag.
- 20 25. A decoder (30) for decoding of a video bitstream, wherein the video bitstream includes
data representing one or more sequence parameter set, SPS, flags, the decoder comprising:
a first obtaining unit configured to obtain two variables for an SPS flag of the one or more
SPS flags, respectively, by parsing the video bitstream, wherein the value of one variable of
the two variables is the minimum allowed value of the SPS flag, and wherein the value of the
25 other variable of the two variables is the maximum allowed value of the SPS flag;
a second obtaining unit configured to obtain a value of the SPS flag, by parsing the video
bitstream;
an evaluating unit configured to evaluate whether the value of the SPS flag is valid based
on the values of the two variables; and
30 a decoding unit configured to decode the video bitstream according to the value of the
SPS flag in case that the value of the SPS flag is valid.

26. An encoder (20) for encoding of a video bitstream, wherein the video bitstream includes data representing one or more sequence parameter set, SPS, flags, the encoder comprising:
- an indicating unit configured to set two variables for an SPS flag of the one or more SPS flags, respectively, wherein the value of one variable of the two variables is the minimum allowed value of the SPS flag, and wherein the value of the other variable of the two variables is the maximum allowed value of the SPS flag, and
 - a determining unit configured to determine the value of the SPS flag according to the two variables of the SPS flag; and
 - an encoding unit configured to encode the value of the SPS flag and the two variables of the SPS flag into the video bitstream.

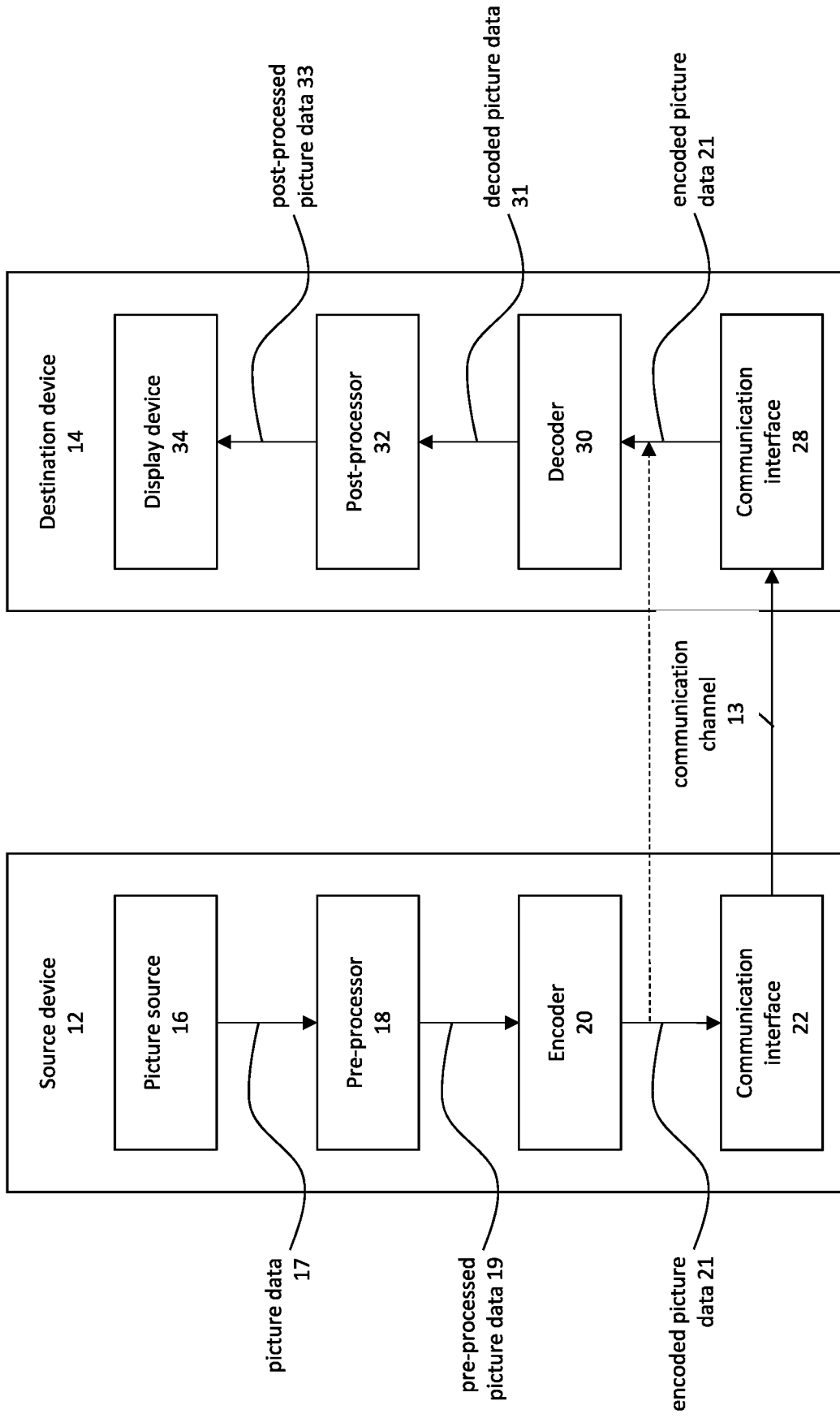


FIG. 1A

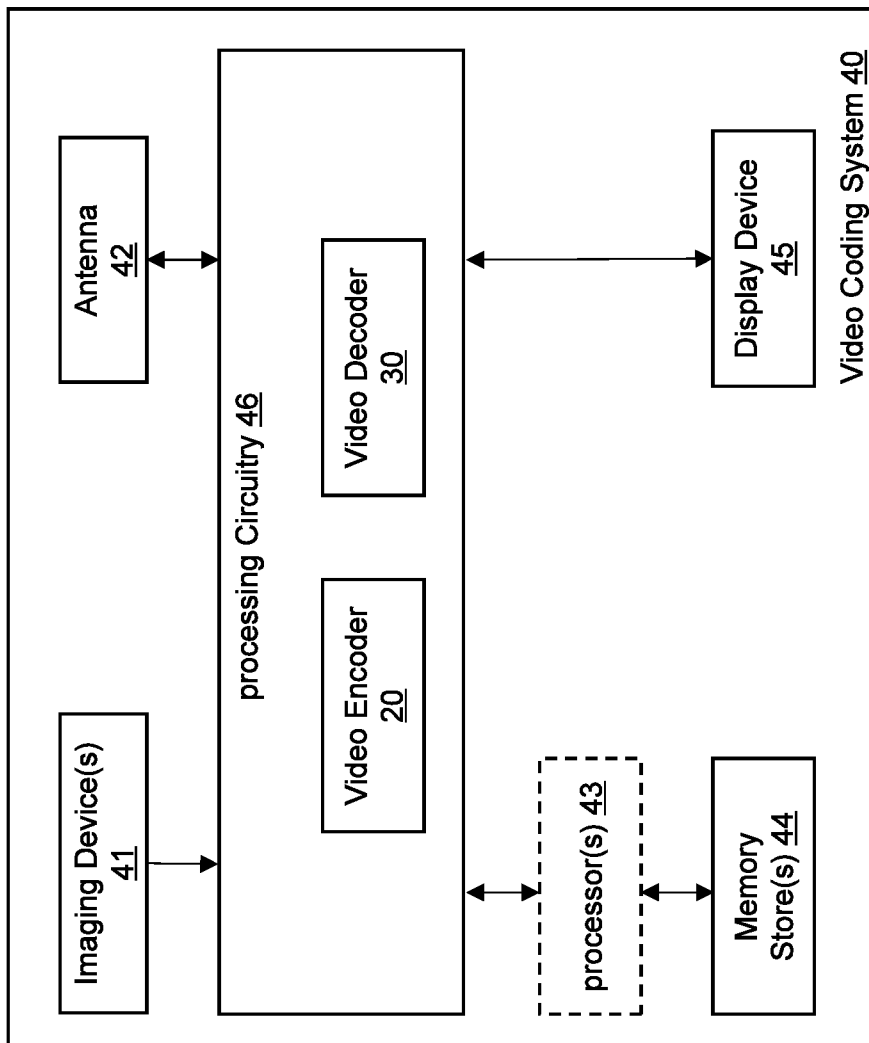


FIG. 1B

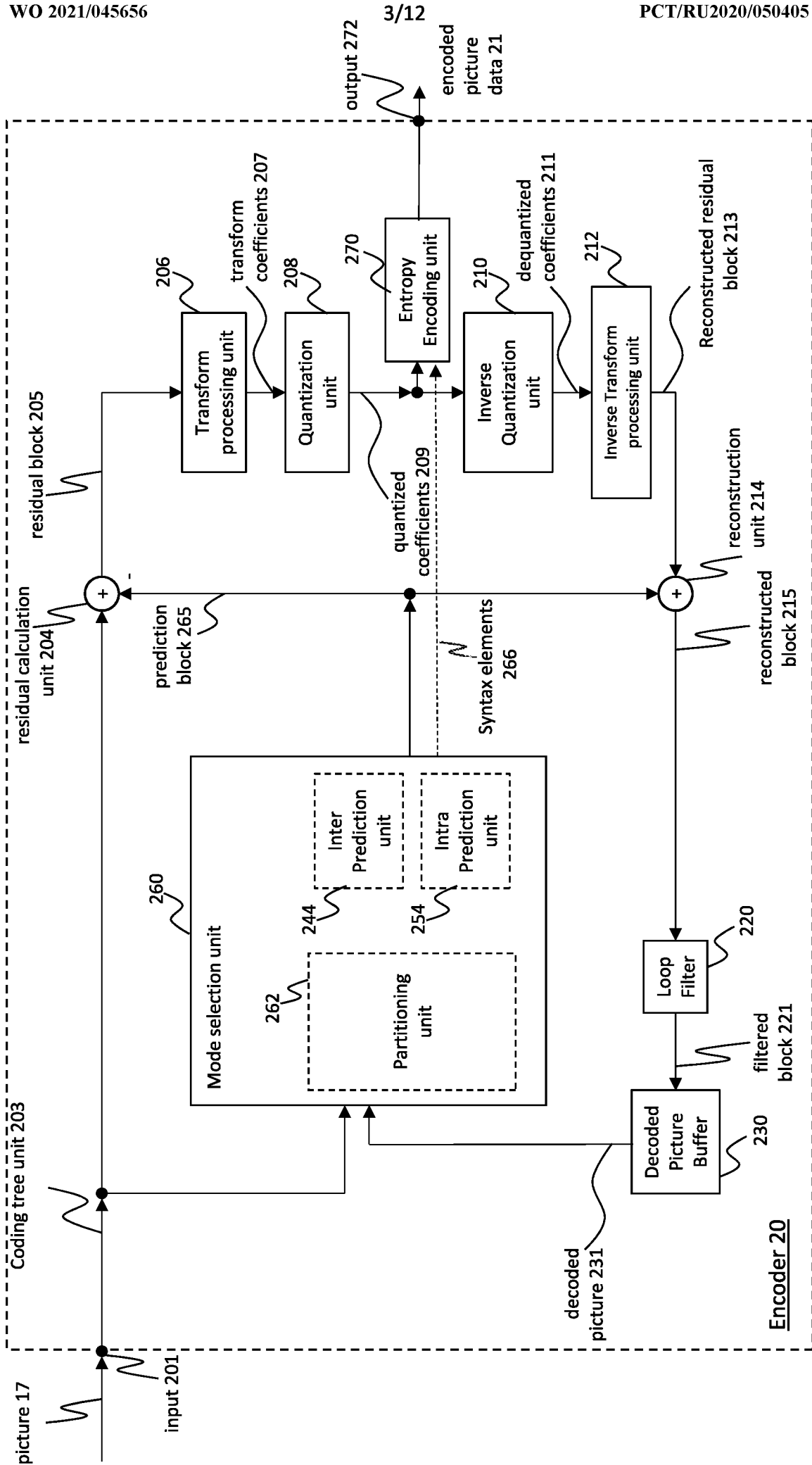


FIG. 2

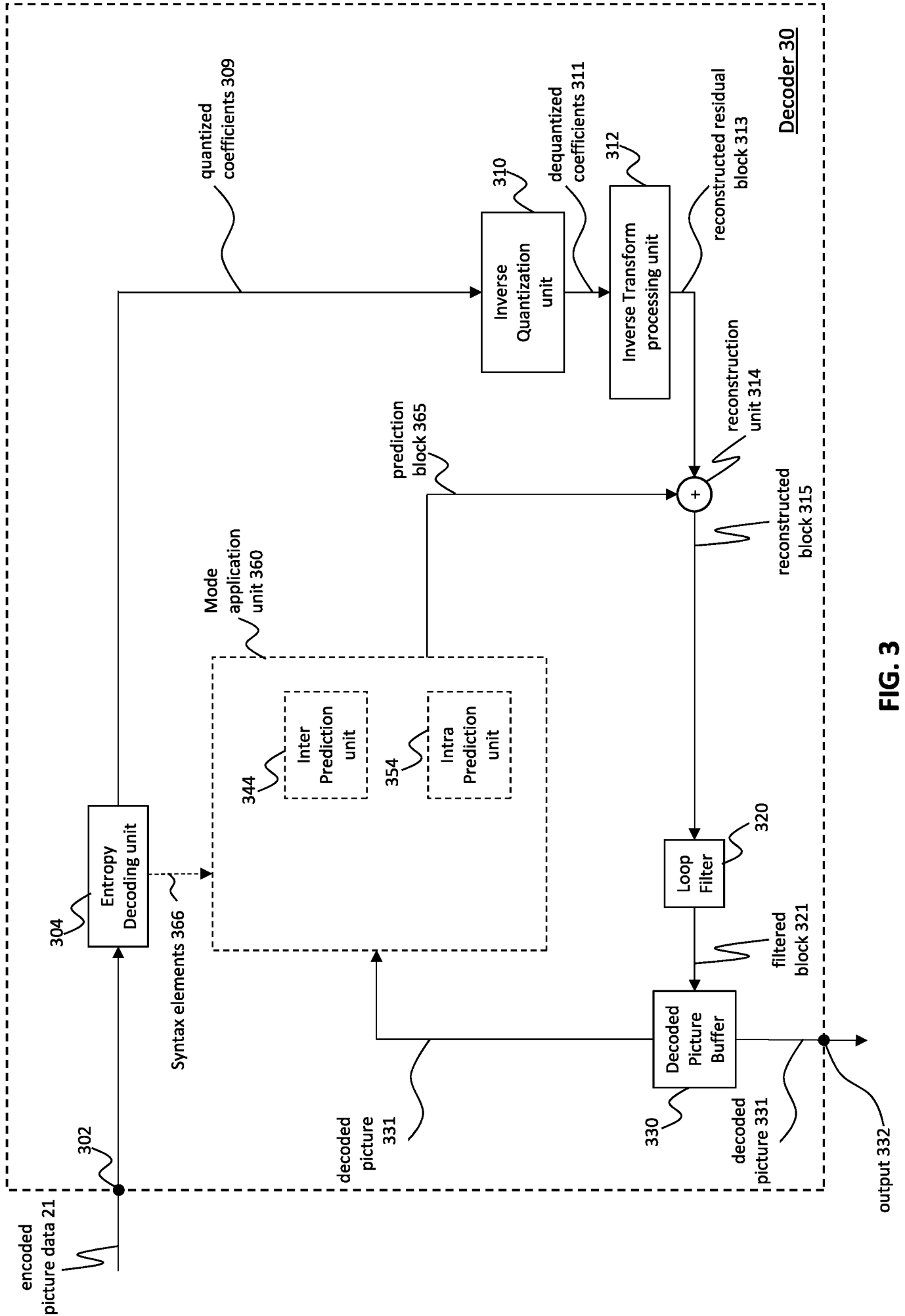


FIG. 3

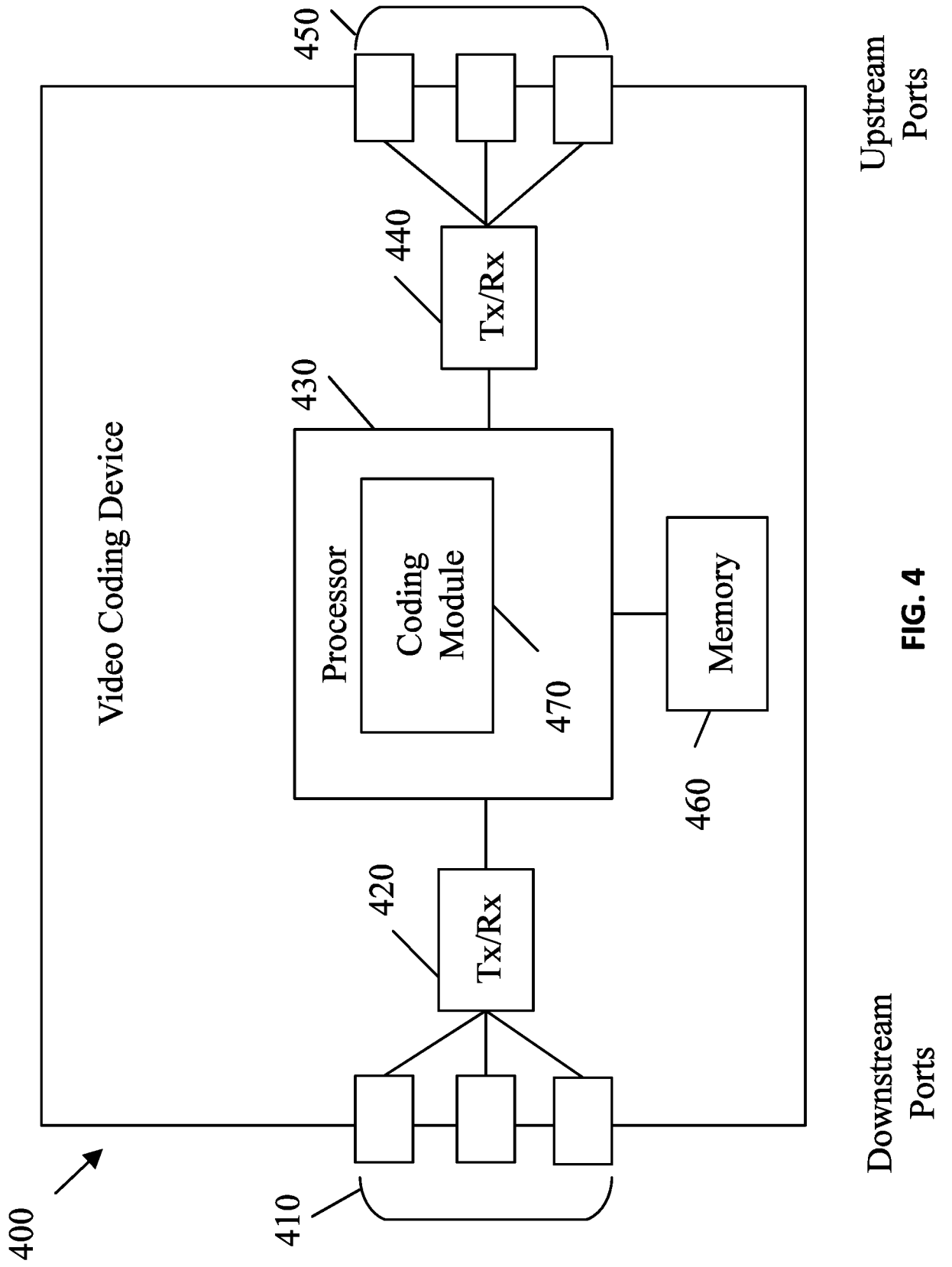


FIG. 4

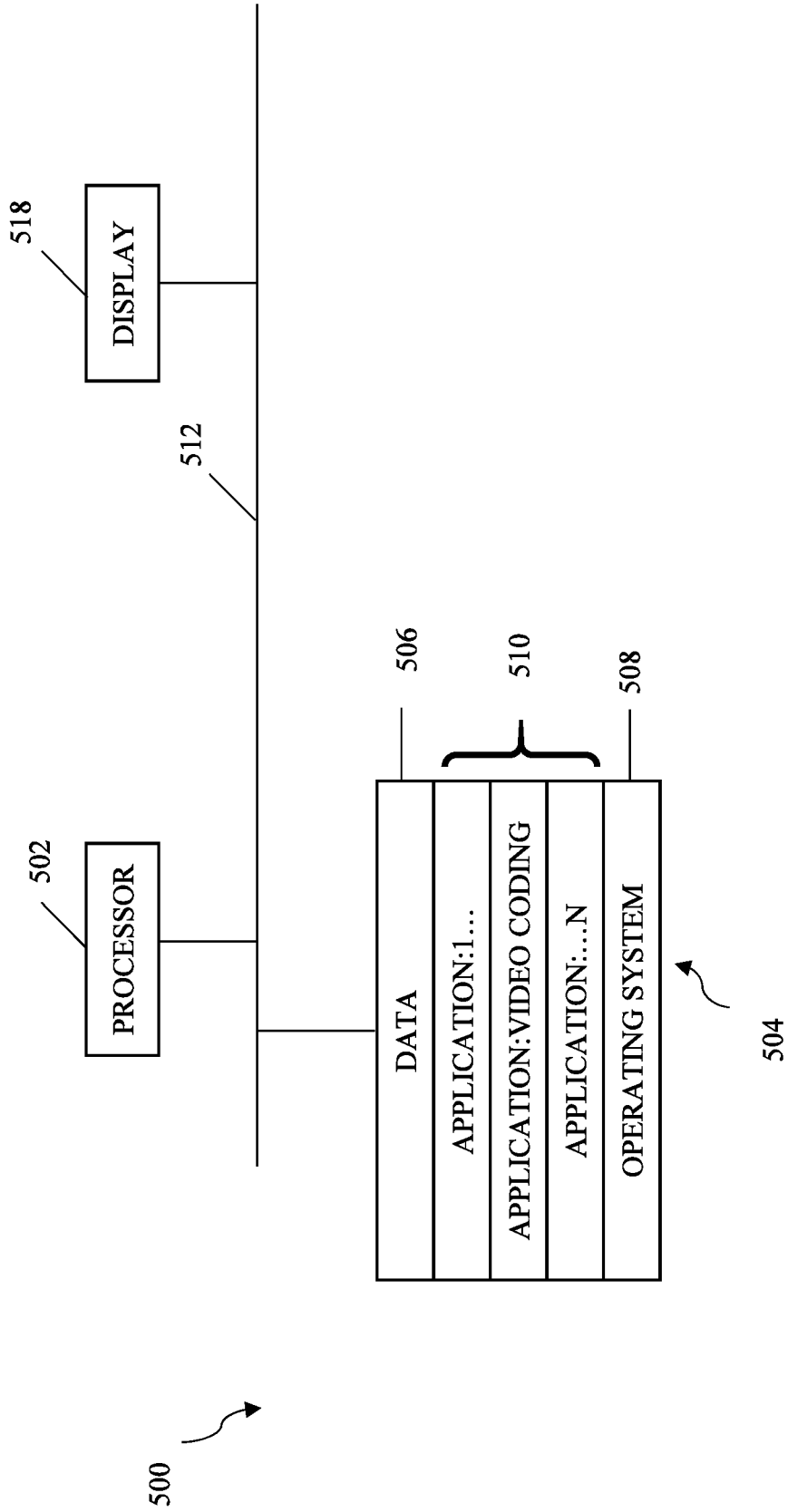


FIG. 5

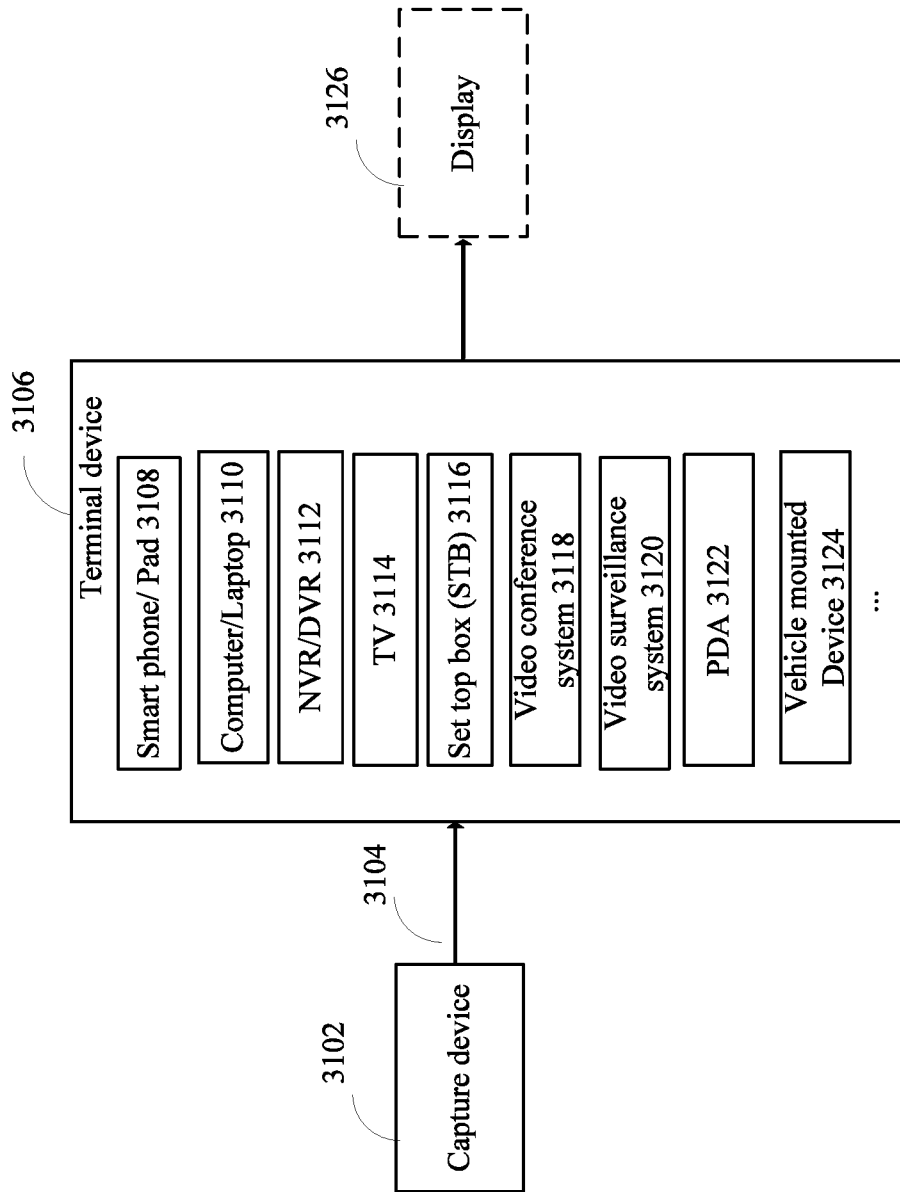


FIG. 6

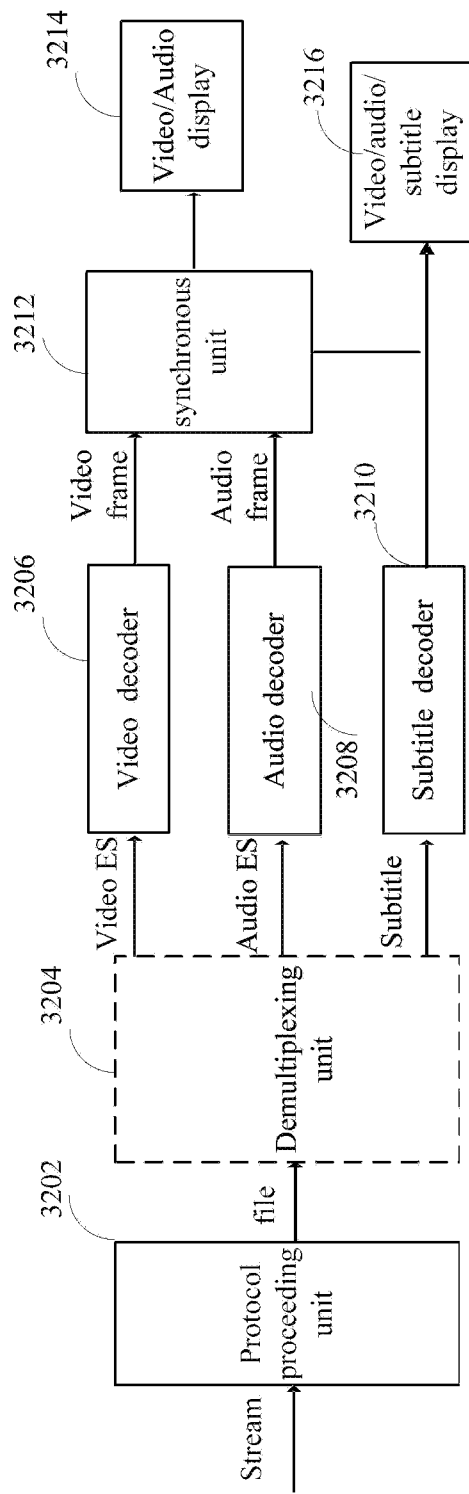


FIG. 7

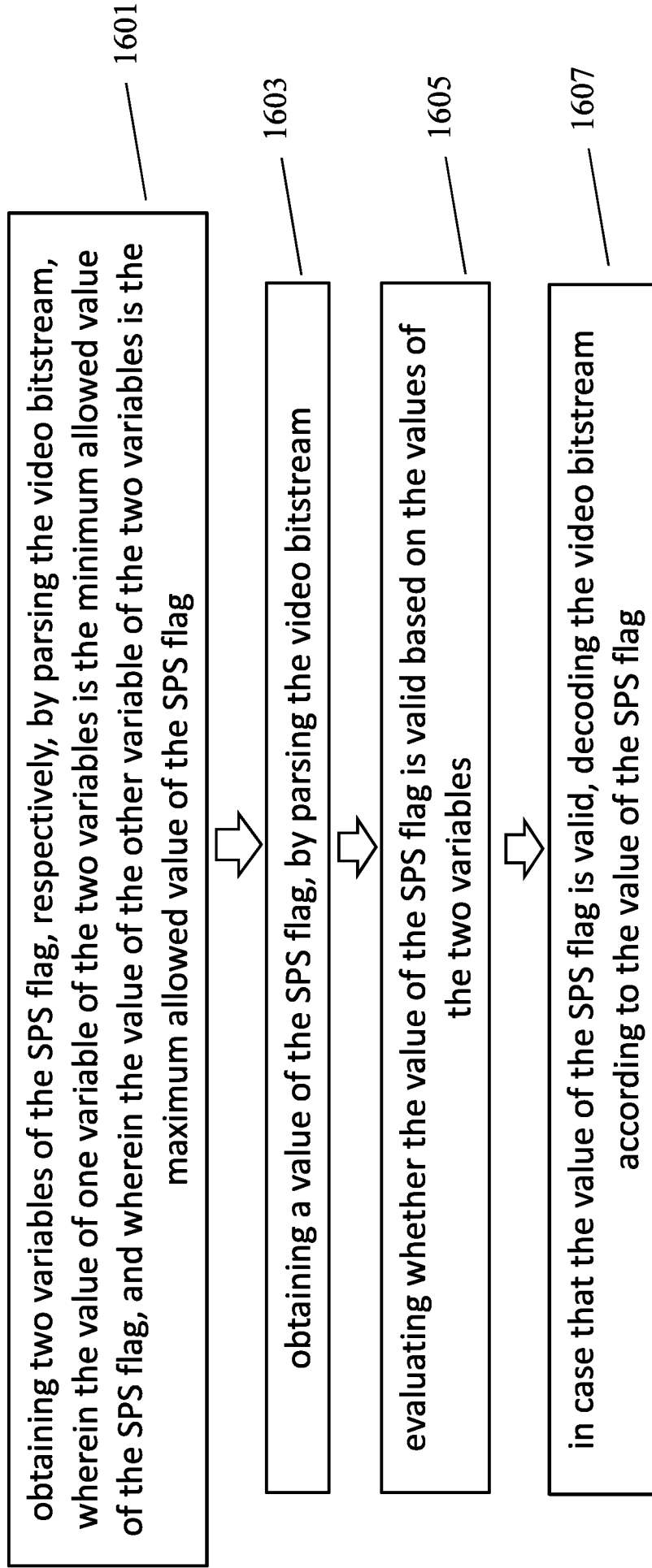


FIG. 8

30

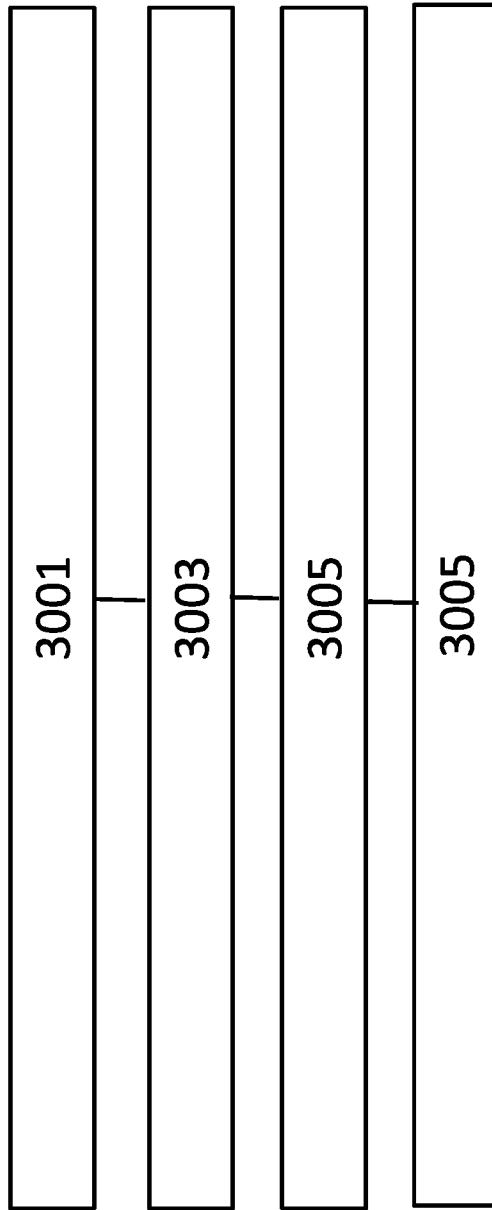


FIG. 9

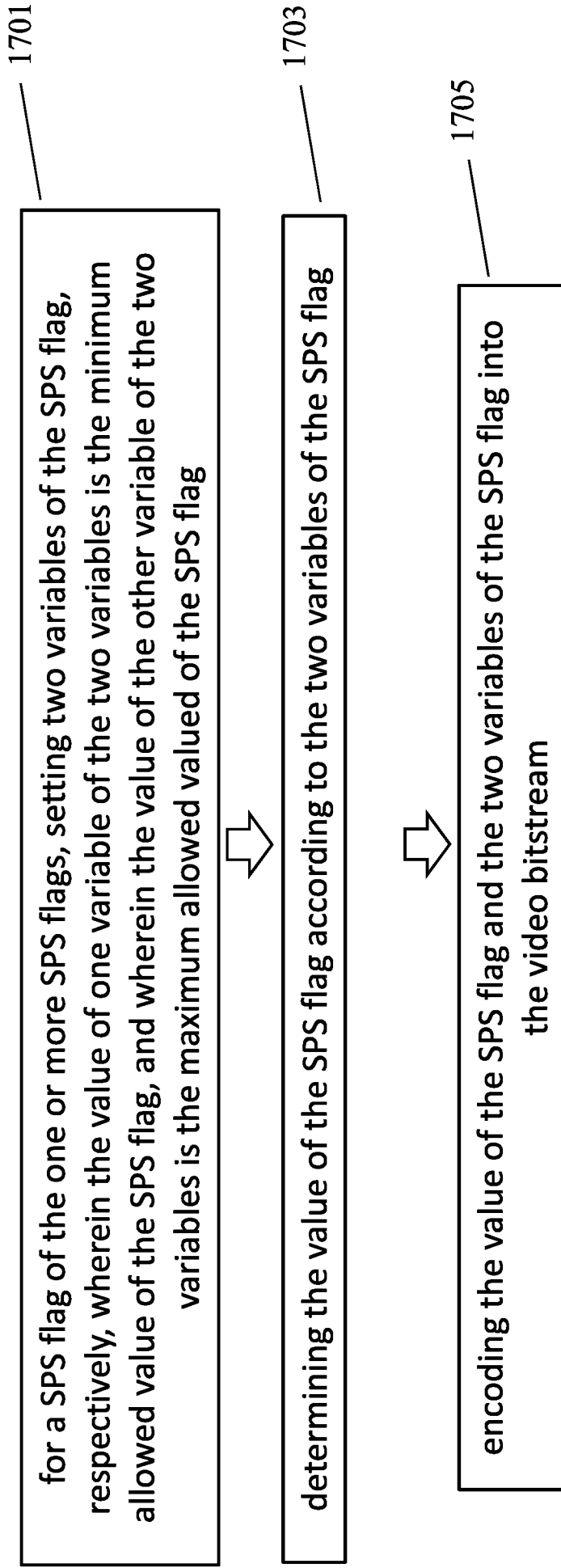


FIG. 10

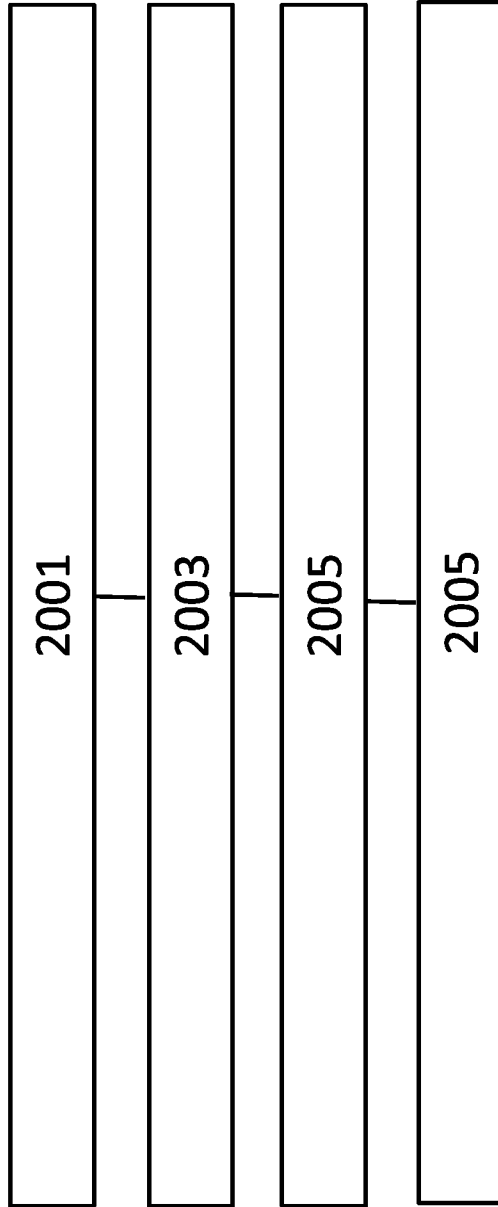


FIG. 11