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(54) Title: SPLIT T-CHAIN MEMORY COMMAND AND ADDRESS BUS TOPOLOGY

(57) Abstract: Embodiments of the invention provide a memory command and address (CA) bus architecture that can accommodate higher CA data output frequencies with reduced signal degradation. For one embodiment of the invention the CA is divided on the motherboard and a CA signal component routed to each of two dual in-line memory modules (DIMMs) of a two-DIMM/channel memory bus design. The CA signal component on each DIMM is then routed sequentially through each dynamic random access memory (DRAM) chip on the respective DIMM. In one embodiment, after routing through each DRAM, the CA signal is terminated on the DIMM. In an alternative embodiment, the CA signal is terminated on the die at the last DRAM of each respective DIMM.

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SPLIT T-CHAIN MEMORY COMMAND AND ADDRESS BUS TOPOLOGY

FIELD

[0001] Embodiments of the invention relate generally to the field of digital processing system memory architecture and more particularly to memory command and address bus topology.

BACKGROUND

[0002] Typical memory architectures have several drawbacks that limit their performance. This is due to the increasing data output frequencies for dynamic random access memory (DRAM). Synchronous DRAM (SDRAM) delivers data at high speed by using, among other things, an interface synchronized to the processor's internal clock. Therefore SDRAM has an output data frequency equal to the clock frequency. Double data rate (DDR) SDRAM provides data even faster by outputting data on the rising and falling edge of the clock, thus having an output data frequency of twice the clock frequency. For both SDRAM and DDR, the clock frequency is synchronous with the core frequency. For DDR II, the I/O buffers are clocked at twice the core frequency thereby providing an even greater output data frequency.

[0003] As the output data frequency increases, the signal integrity decreases. Figure 1 illustrates a typical memory architecture in accordance with the prior art. Memory architecture 100, shown in Figure 1, includes chipset 105. The chipset (core logic) 105 includes a memory controller 106 that controls the data flow between the system processor (not shown) and the system memory. The system memory may be contained on one or more dual in-line memory modules (DIMMs) 110. In such architecture, the command and address (CA) signals are propagated from the memory controller 106 along CA bus 108 to each DIMM 110. CA bus 108 may have, for example, eight parallel lines to propagate CA

signals to the DRAM. On the board the CA signal is divided and routed to each DIMM. On each DIMM, the CA signals are successively divided to route to each DRAM over traces 109 as shown in Figure 1. This successive division results in proportionately reduced CA signal components reaching each DRAM. Because the lengths of traces 109 are basically matched, the electrical delay to any DRAM is approximately the same. Therefore each reduced CA signal component hits the load of the respective DRAM at the same time substantially degrading each CA signal component. Additionally, the electrical reflection resulting from the trace pattern may result in interference. The extent of this interference depending upon the signal strength, and the ratio between the actual signal and the reflection.

[0004] The prior art architecture illustrated in Figure 1 is acceptable at lower frequencies (e.g., 200 Mhz). However, as frequencies increase and the signal length becomes proportional to the physical length of the traces, the signal degradation becomes unacceptable.

[0005] The signal degradation described above has been addressed in several ways including changing the circuitry (e.g., additional resistors, duplicated lines (extra pins), etc.) and buffering the DIMM (adding extra logic chips to reduce the loading on the CA busses). These methods are costly as they amount to significant departures to industry standards for particular designs.

[0006] Another prior art memory architecture, direct Rambus™ DRAM (DRDRAM), increases data output frequency through use of a 16-bit bus (rather than the DRAM's 8-bit bus), and data pipelining. DRDRAM addresses the lumped load problem through a sequential routing scheme, but because the signal is routed through 32 DRAM chips, the signal strength eventually degrades. Additionally, the direct DRDRAM routing is across one DIMM to a connector on the motherboard and across the next DIMM, finally

terminating on the motherboard, which requires additional pins at the connector. Moreover, routing through additional connectors causes signal degradation due to electrical reflection from the connectors as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The invention may be best understood by referring to the following description and accompanying drawings that are used to illustrate embodiments of the invention. In the drawings:

[0008] Figure 1 illustrates a typical memory architecture in accordance with the prior art;

[0009] Figure 2 illustrates a memory CA bus architecture in accordance with one embodiment of the present invention; and

[0010] Figure 3 illustrates a process in which CA signals are propagated from the memory controller to the system memory in accordance with one embodiment of the invention.

DETAILED DESCRIPTION

[0011] Embodiments of the invention provide a memory CA bus architecture that can accommodate higher CA data output frequencies with reduced signal degradation. For one embodiment of the invention the CA is divided on the motherboard and a CA signal component routed to each of two DIMMs of a two-DIMM/channel memory bus design. The CA signal component on each DIMM is then routed sequentially through each DRAM on the respective DIMM. In one embodiment, after routing through each DRAM, the CA signal is terminated at a termination point on the DIMM. In an alternative embodiment,

the CA signal is terminated at a termination point on the die at the last DRAM of each respective DIMM.

[0012] In the following description, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the understanding of this description.

[0013] Reference throughout the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearance of the phrases "in one embodiment" or "in an embodiment" in various places throughout the specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0014] Moreover, inventive aspects lie in less than all features of a single disclosed embodiment. Thus, the claims following the Detailed Description are hereby expressly incorporated into this Detailed Description, with each claim standing on its own as a separate embodiment of this invention.

[0015] Figure 2 illustrates a memory CA bus architecture in accordance with one embodiment of the present invention. Memory architecture 200, shown in Figure 2, includes a chipset 205 coupled to DIMM 210a and DIMM 210b by a CA bus 208. The chipset 205 includes memory controller 206. During operation, the CA signal is routed to one side of DIMM 210a. Figure 2 illustrates routing to the right side, however routing may be to the left side in alternative embodiments. On the motherboard, the CA signal is propagated from driver pin 207 on chipset 205 to connector pin 211a on DIMM 210a. At this point the CA signal is divided into two components. The first CA signal component is

propagated through DRAMs 1a – 16a on DIMM 210a starting with DRAM 1a. The first CA signal component is not further divided on DIMM 210a, but is propagated through each of DRAMs 1a –16a, one DRAM at a time. Therefore the load through which the signal propagates is a distributed load rather than a "lumped" load, as in prior art schemes. Upon propagation through each of the DRAMs on DIMM 210a, the signal terminates at termination point 212a on DIMM 210a. In alternative embodiments the termination point may be on the die of the last DRAM (e.g., DRAM 16a).

[0016] The second CA signal component is propagated to a connector pin 211b on DIMM 210b where it is similarly propagated through each DRAM, DRAMS 1b –16b, serially. Upon propagation through each of the DRAMs on DIMM 210b, the signal terminates at termination point 212b on DIMM 210b. Again, as noted, the termination point may be on the die of the last DRAM through which the signal has propagated. (e.g., DRAM 16b).

[0017] The load distribution through serial propagation of the CA signal components may require added logic. For example, added logic may be required to track the clock domain crossing due to the delay (time difference) between propagation of the signal through the first DRAM and propagation of the signal through the last DRAM (on each DIMM). For one embodiment, such added logic may be implemented on the chipset. In alternative embodiments the added logic may be implemented on the DRAM itself, or on both the chipset and the DRAM.

IMPEDANCE

[0018] As discussed above, mismatched impedance along the CA bus may result in reflections that degrade the CA signal. The CA bus topology in accordance with one embodiment of the invention, simplifies the routing of the CA signal across the DIMM as well as across the motherboard resulting in reduced signal reflection. Additionally, the

CA bus topology in accordance with one embodiment of the invention provides greater flexibility for matching impedances. For one embodiment, the DRAM impedance and Bloch mode impedance for a given bandwidth is matched to the on-DIMM impedance which is greater than or equal to the mother board impedance. The chipset driver impedance is matched to the motherboard impedance and the DIMM termination point impedance is matched to the on-DIMM impedance.

[0019] The most significant parasitics are the interconnect resistance and interconnect (ground and coupling) capacitance, as well as substrate cross-talk. Interconnect parasitics are becoming the more significant concern, especially with multiple metal interconnect layers.

[0020] The CA bus architecture in accordance with one embodiment of the invention takes advantage of the small DRAM capacitive silicon loading and package to adjust the PCB routing to match a Bloch mode impedance across a given bandwidth as described above.

[0021] An estimate of DDRIII scaled parasitics would hit an on-DIMM impedance of approximately 50-60 Ohms and a motherboard impedance of approximately 25-50 Ohms. A data rate bandwidth in excess of 800MT/s can be achieved with substantially the specifications of DDRII. Eye diagrams at 800 MT/s are included as Appendix A. Diagrams A1 and A2 illustrate the eye diagram for DRAMs 1 and 16, respectively, without crosstalk. Diagrams A3 and A4 illustrate the eye diagram for DRAMs 1 and 16, respectively, with crosstalk.

[0022] Figure 3 illustrates a process in which CA signals are propagated from the memory controller to the system memory in accordance with one embodiment of the invention. Process 300, shown in Figure 3, begins at operation 305 in which a CA signal is propagated from the memory controller to the first of two or more DIMMs.

[0023] At operation 310 the CA signal is divided into two or more components depending upon the number of DIMMs in the memory system (e.g., two), and each component is propagated to a respective DIMM.

[0024] At operation 315 the CA signal components at each DIMM are concurrently propagated to each DRAM of the respective DIMM. Each CA signal component is propagated serially starting with a DRAM on a specified side of the DIMM.

[0025] At operation 320 each CA signal component is terminated upon the DIMM. In an alternative embodiment of the invention, the CA signal component may be terminated on the die of the last DRAM to which the CA signal component was propagated.

GENERAL MATTERS

[0026] Embodiments of the invention provide a CA bus architecture suited for a two DIMM/channel memory bus design common in Desktop and Mobile platforms. In alternative embodiments, the CA bus architecture may be applied to other memory bus designs. The CA bus architecture in accordance with one embodiment, increases CA bandwidth without a significant departure from existing industry standards. For one embodiment, the pin count is minimized and with only a slight increase in logic complexity.

[0027] For one embodiment, the channel design is optimized to take advantage of the unidirectional bus CA DRAM parasitics to improve the channel bandwidth by a factor of eight over prior art CA topology schemes.

For one embodiment of the invention the on-Dimm routing and motherboard routing is simplified providing the flexibility to adjust the impedances to provide optimized voltage swing and minimal reflections, and thus higher performance.

In reference to Figure 2, the order of propagation of the CA signal is described as initially proceeding through all of the DRAMs on the front side of DIMM 210a (i.e.,

DRAMs 1a – 8a) and then continuing through all of the DRAMs on the back side of DIMM 210a (i.e., DRAMs 9a – 16a). In alternative embodiments, the propagation of the CA signal may instead alternate from a front-side DRAM to a back-side DRAM or vice versa. For example, the propagation of the CA signal start at DRAM 1a, proceed to DRAM 16a, and alternate from front-side DRAMs to back-side DRAMs, finally terminating on or near DRAM 9a.

While the invention has been described in terms of several embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.

CLAIMS

What is claimed is:

1. A memory system architecture comprising:

a memory controller;

a plurality of memory modules, each memory module containing a plurality of memory chips;

a command and address bus coupling the memory controller to each of the plurality of memory modules such that a command and address signal propagated from the memory controller to one of the memory chips is propagated to a first memory module, divided into components, each component corresponding to one of the plurality of memory modules, each component propagated serially to each of the plurality of memory chips of the corresponding memory module.

2. The memory system architecture of claim 1 wherein each memory module is a dual in-line memory module and each memory chip is a dynamic random access memory chip.

3. The memory system architecture of claim 2 wherein the command and address bus is a unidirectional address bus.

4. The memory system architecture of claim 1 wherein the plurality of memory modules comprises two memory modules and the plurality of memory chips comprises sixteen memory chips.

5. The memory system architecture of claim 3 wherein the command and address signal is propagated from a pin on a chipset containing the memory controller to a pin on the first memory module.

6. The memory system architecture of claim 5 wherein each component is terminated at a signal termination point on the corresponding memory module after propagating serially through each of the plurality of memory chips.

7. The memory system architecture of claim 1 wherein each component is terminated at a signal termination point on a die of a last memory chip after propagating serially through each of the plurality of memory chips of the corresponding memory module.

8. The memory system architecture of claim 6 wherein a first impedance between the connector on the chipset and the connector on the first memory module is less than a second impedance through a memory module.

9. The memory system architecture of claim 8 wherein the second impedance is the same, within a specified tolerance, as a third impedance through the plurality of memory chips plus a Bloch mode impedance corresponding to a specified data output frequency.

10. The memory system architecture of claim 9 wherein a chipset driver impedance is the same, within a specified tolerance, as the first impedance and an impedance of the signal termination point is the same, within a specified tolerance, as the second impedance.

11. A method comprising:

propagating a command and address signal over a command and address bus to one of a plurality of memory modules, each memory module containing a plurality of memory devices;

dividing the command and address signal into a plurality of components, each component corresponding to one of the plurality of memory modules; and

propagating each component, serially to each of the plurality of memory devices of the corresponding memory module.

12. The method of claim 11 wherein each memory module is a dual in-line memory module and each memory device is a dynamic random access memory device.

13. The method of claim 12 wherein the command and address bus is a unidirectional address bus.

14. The method of claim 11 wherein the plurality of memory modules comprises two memory modules and the plurality of memory devices comprises sixteen memory devices.

15. The method of claim 13 wherein the command and address signal is propagated from a pin on a chipset containing the memory controller to a pin on the first memory module.

16. The method of claim 11 further comprising:

terminating each component at a signal termination point on the corresponding memory module.

17. The method of claim 11 further comprising:

terminating each component at a signal termination point on a die of a last memory device.

18. The method of claim 16 wherein a first impedance between the connector on the chipset and the connector on the first memory module is less than a second impedance through a memory module.

19. The method of claim 18 wherein the second impedance is the same, within a specified tolerance, as a third impedance through the plurality of memory chips plus a Bloch mode impedance corresponding to a specified data output frequency.

20. The method of claim 19 wherein a chipset driver impedance is the same, within a specified tolerance, as the first impedance and an impedance of the signal termination point is the same, within a specified tolerance, as the second impedance.

21. A system comprising:

a processor;

a memory controller coupled to the processor;

a command and address bus coupled to the memory controller, the command and address bus configured to propagate a command and address signal to one of a plurality of memory modules, divide the command and address signal into a plurality of components,

each component corresponding to a memory module, and propagate each component, serially through each of a plurality of memory devices contained within the corresponding memory module.

22. The system of claim 21 wherein each memory module is a dual in-line memory module and each memory device is a dynamic random access memory device.

23. The system of claim 22 wherein the command and address bus is a unidirectional address bus.

24. The system of claim 21 wherein the plurality of memory modules comprises two memory modules and the plurality of memory devices comprises sixteen memory devices.

25. The system of claim 23 wherein the command and address signal is propagated from a pin on a chipset containing the memory controller to a pin on the first memory module.

26. The system of claim 21 further comprising:

terminating each component at a signal termination point on the corresponding memory module.

27. The system of claim 21 further comprising:

terminating each component at a signal termination point on a die of a last memory device.

28. The system of claim 26 wherein a first impedance between the connector on the chipset and the connector on the first memory module is less than a second impedance through a memory module.

29. The system of claim 28 wherein the second impedance is the same, within a specified tolerance, as a third impedance through the plurality of memory chips plus a Bloch mode impedance corresponding to a specified data output frequency.

30. The system of claim 29 wherein a chipset driver impedance is the same, within a specified tolerance, as the first impedance and an impedance of the signal termination point is the same, within a specified tolerance, as the second impedance.

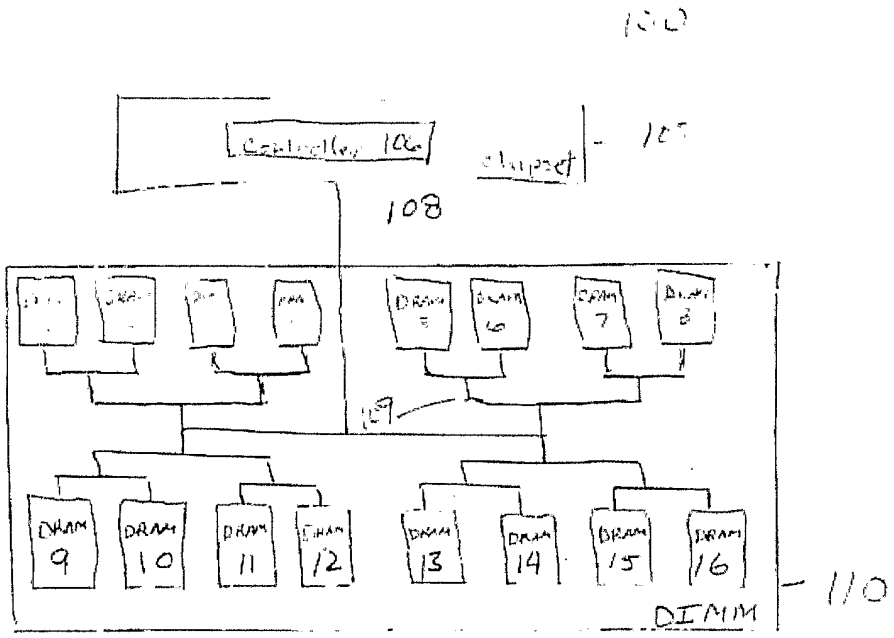


Fig. 1
(Prior Art)

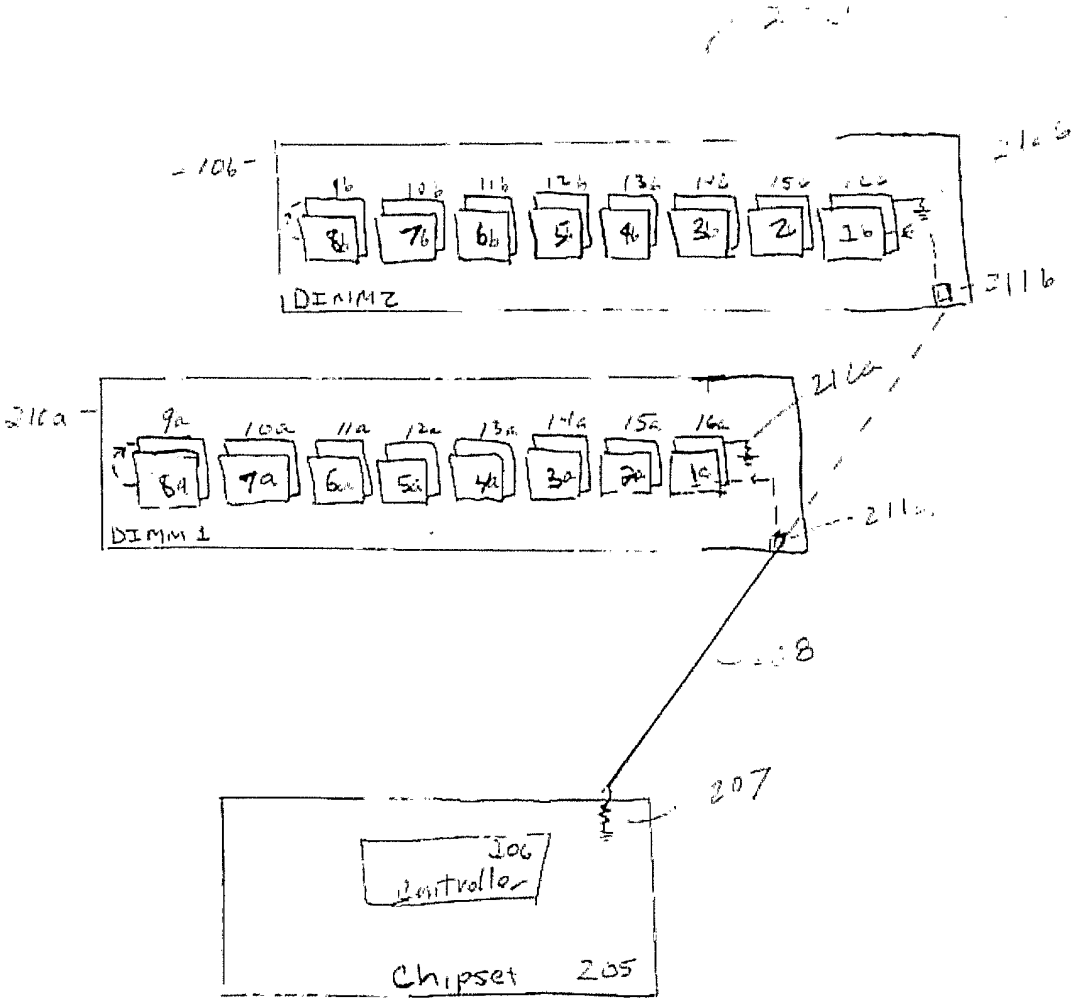


Fig. 2

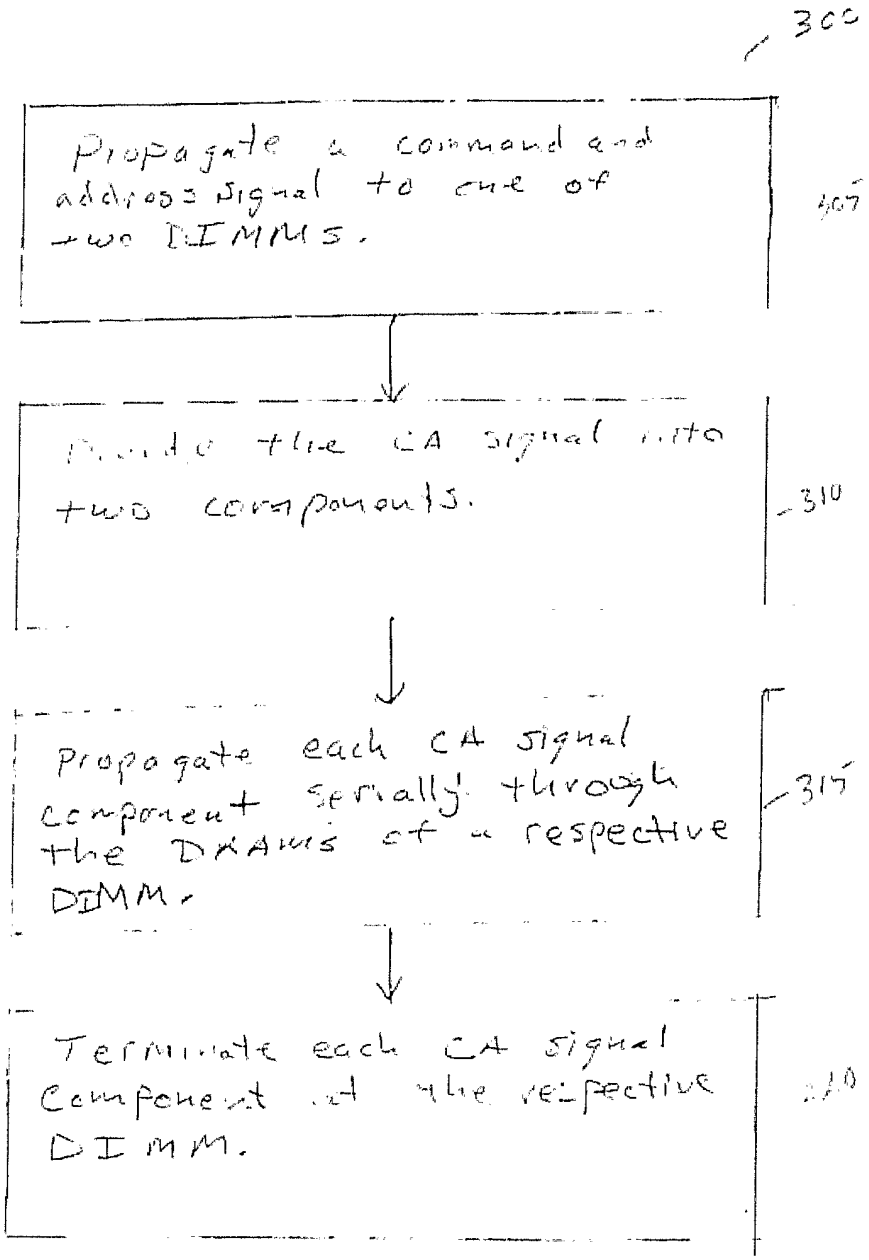
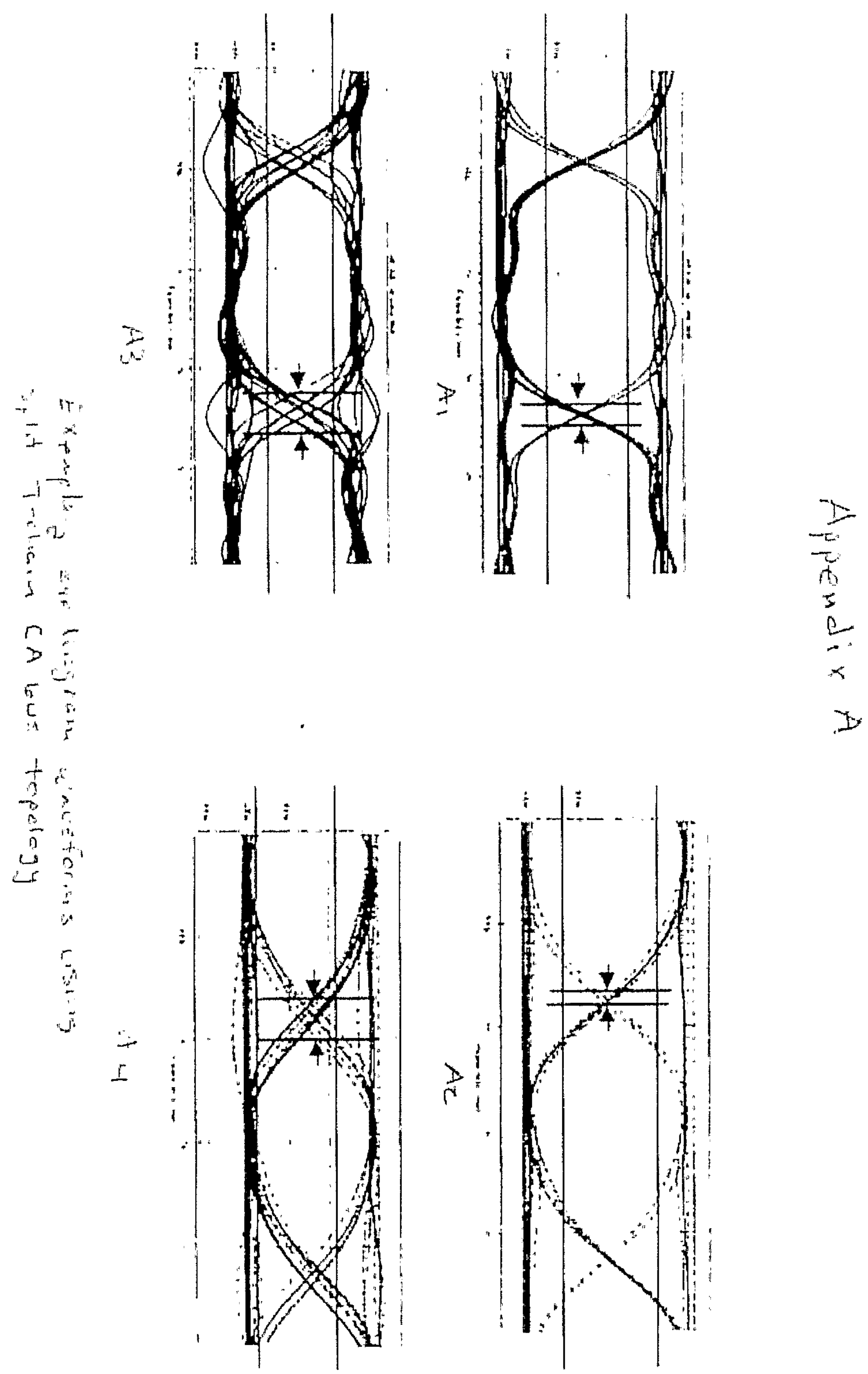

300
Propagate a command and address signal to one of two DIMMS.
305
Divide the CA signal into two components.
310
Propagate each CA signal component serially through the DRAMs of a respective DIMM.
315
Terminate each CA signal component at the respective DIMM.

Fig 3


Appendix A
A3
A1