US 20050104027A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2005/0104027 A1

Lazarev (43) Pub. Date: May 19, 2005

(54) THREE-DIMENSIONAL INTEGRATED CIRCUIT WITH INTEGRATED HEAT SINKS

(76) Inventor: **Pavel I. Lazarev**, Belmont, CA (US)

Correspondence Address:
Aldo J. Test
DORSEY & WHITNEY LLP
Suite 3400
4 Embarcadero Center
San Francisco, CA 94111 (US)

(21) Appl. No.: **10/965,065**

(22) Filed: **Oct. 13, 2004**

Related U.S. Application Data

(60) Provisional application No. 60/512,256, filed on Oct. 17, 2003.

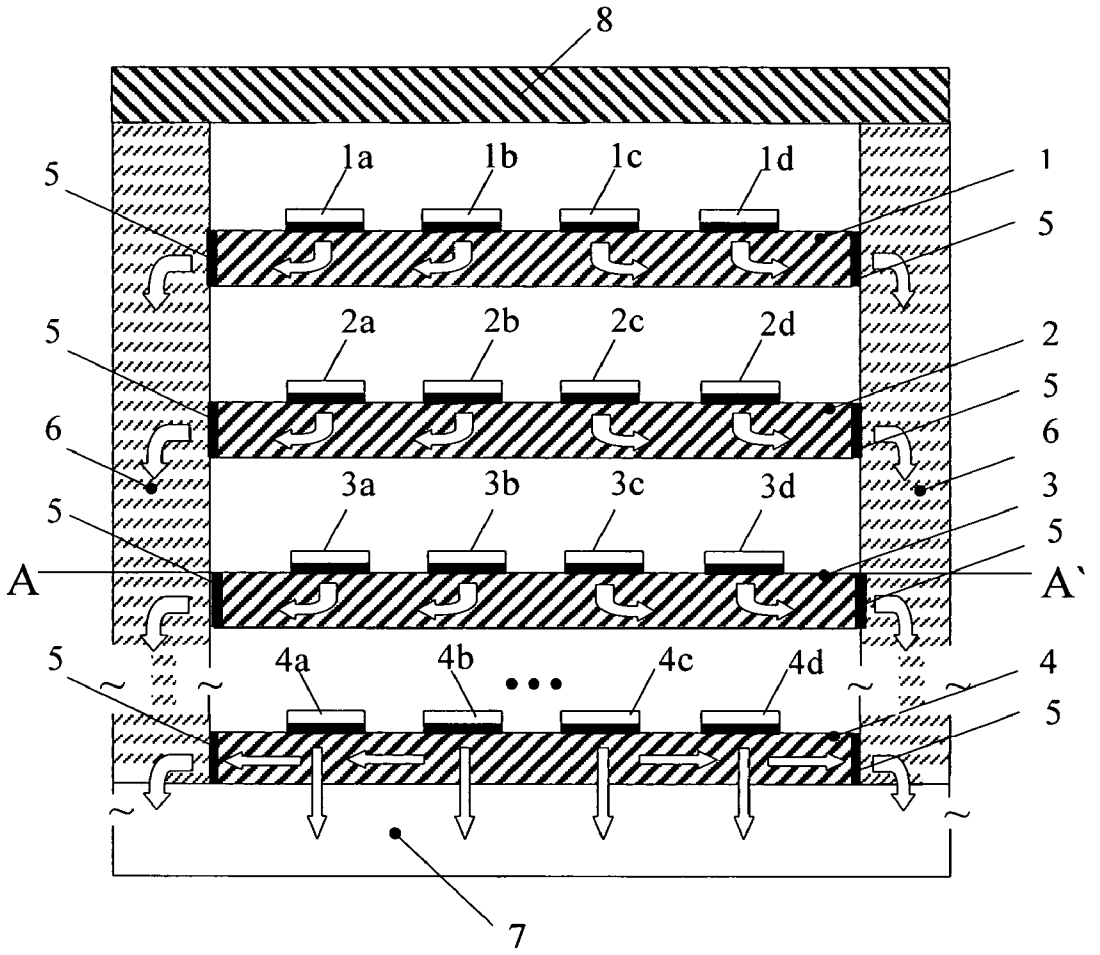
Publication Classification

(51) **Int. Cl.**[7] **E04B 1/74**

(52) **U.S. Cl.** **252/62**

(57) **ABSTRACT**

The present invention is directed to a three-dimensional semiconducting integrated circuit incorporating an integrated heat-sink dissipating heat produced by the semiconductor device mounted thereon.



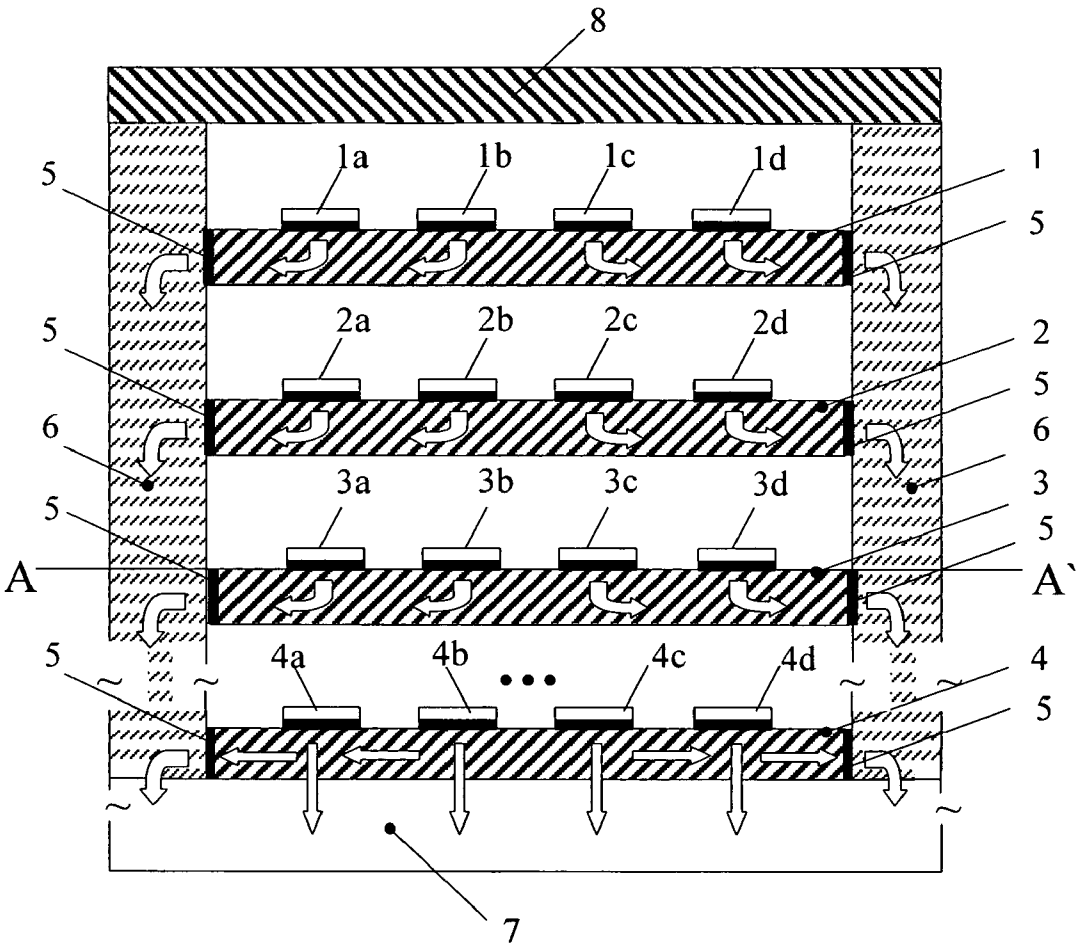


Fig. 1a

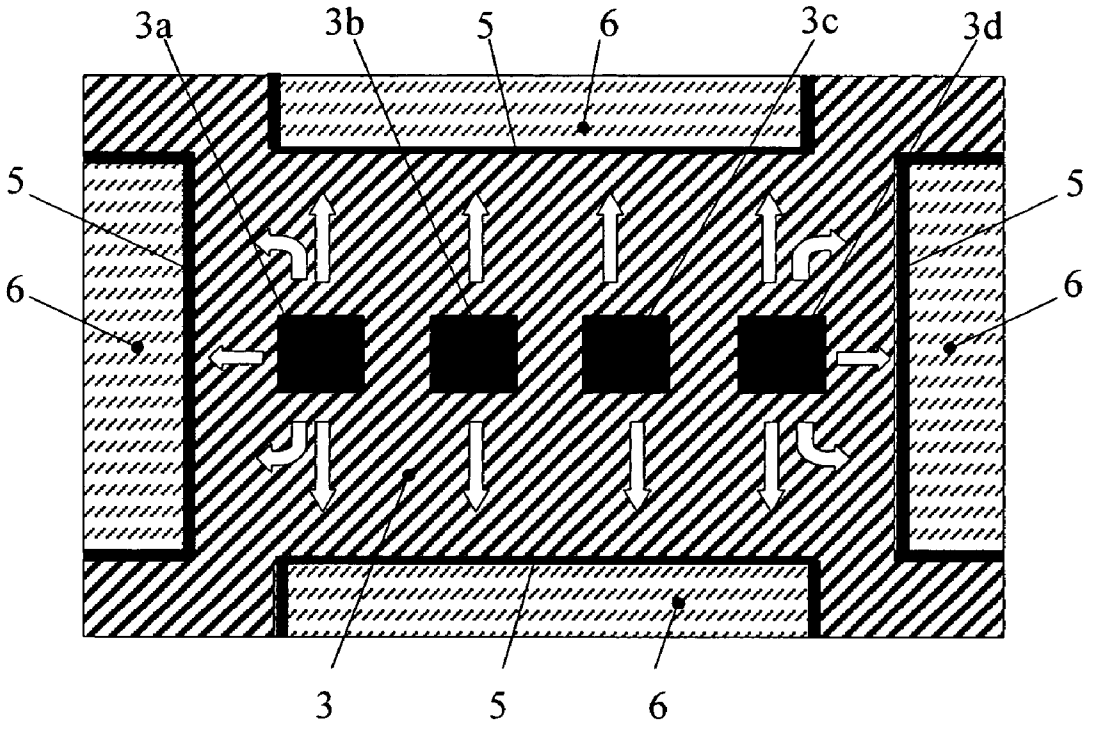


Fig. 1b

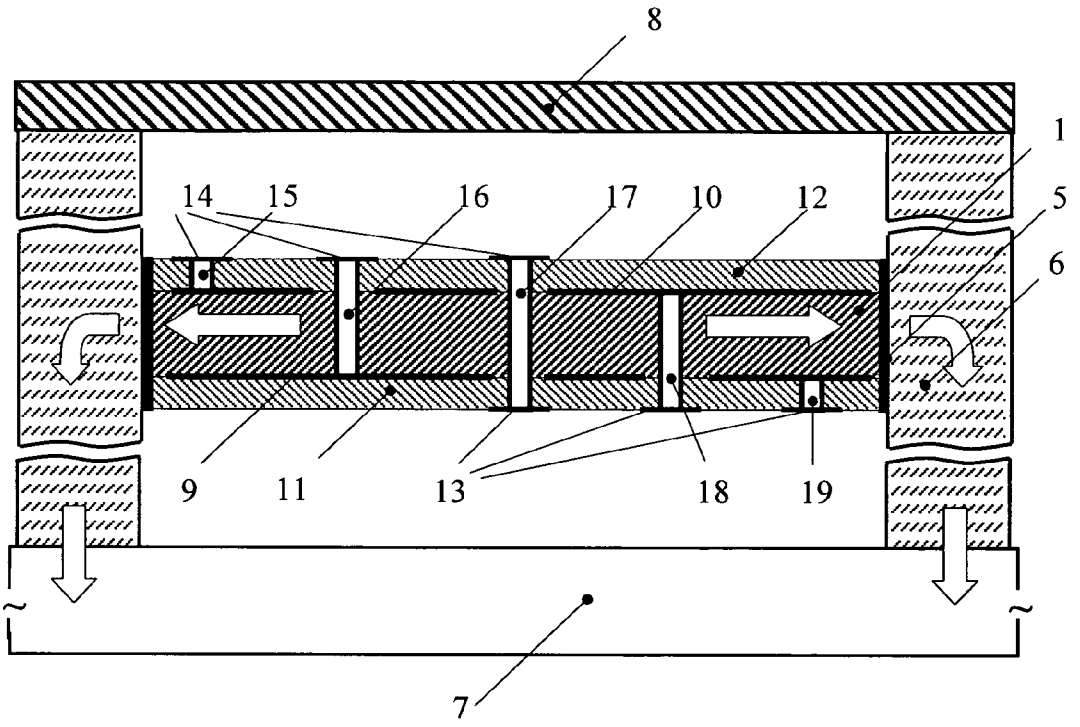


Fig. 2

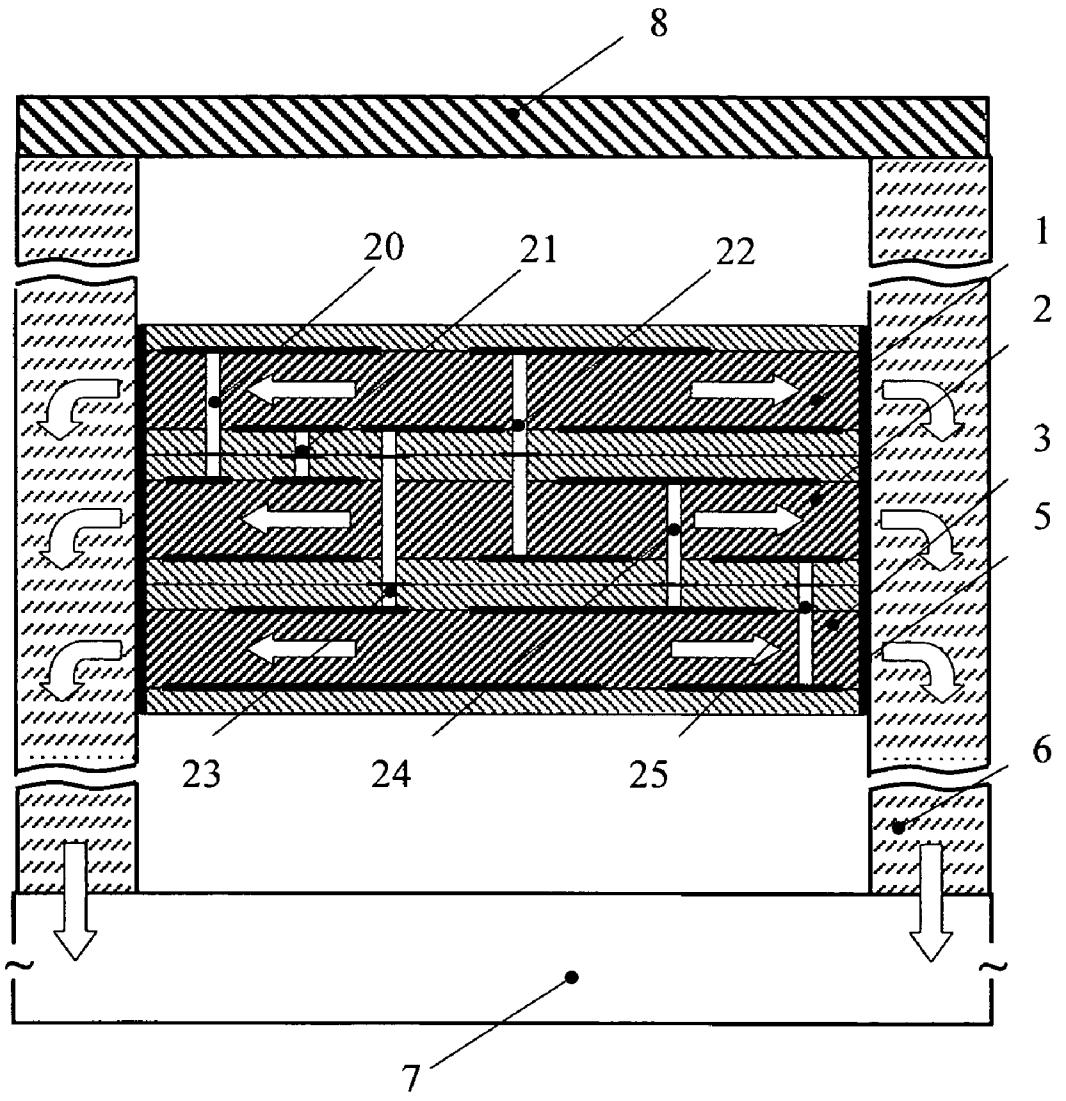


Fig. 3

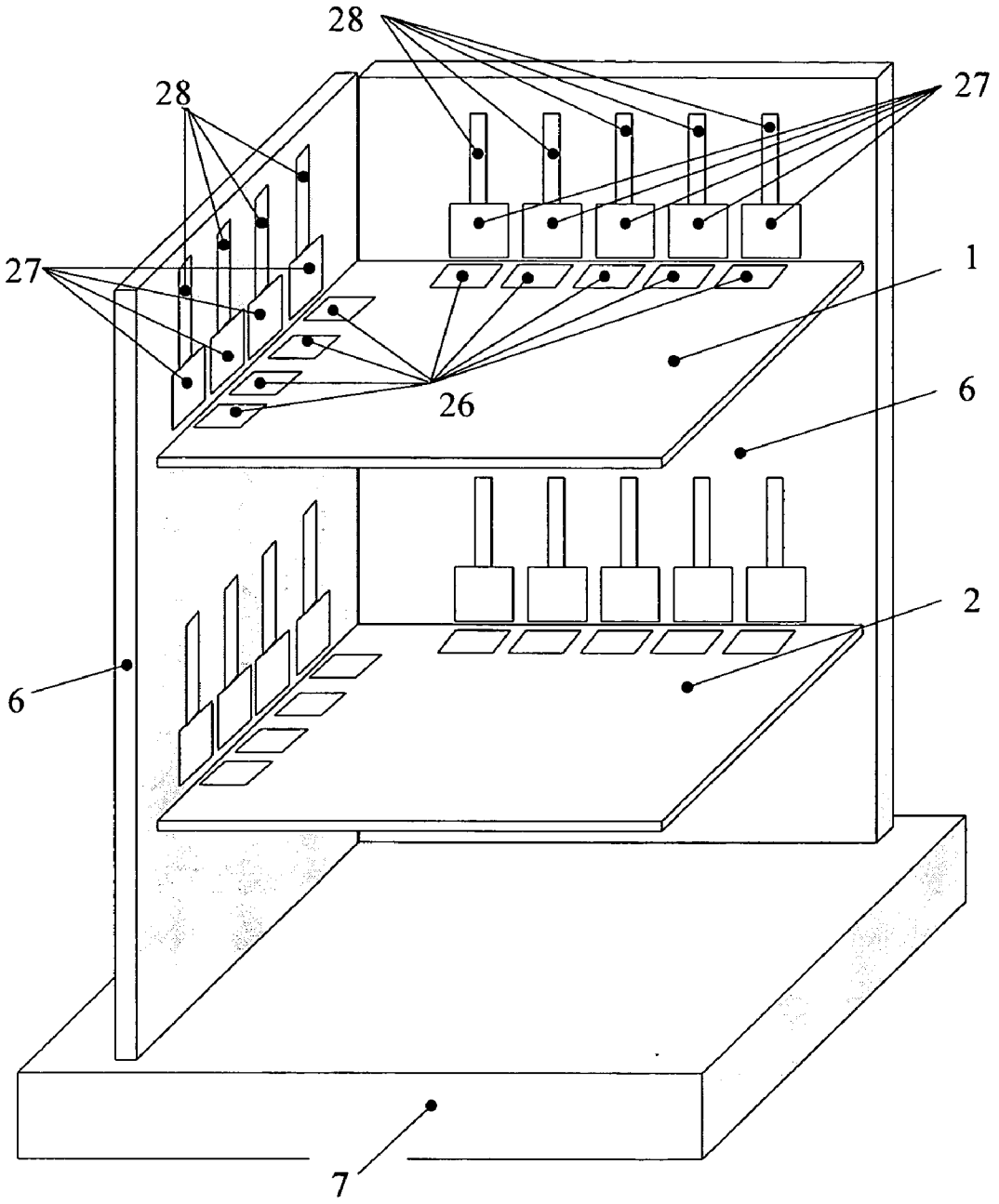


Fig. 4

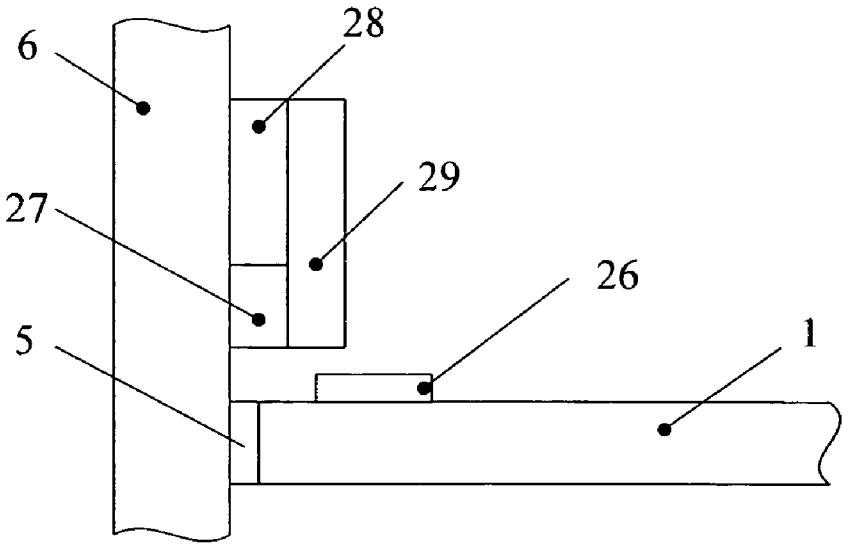


Fig. 5a

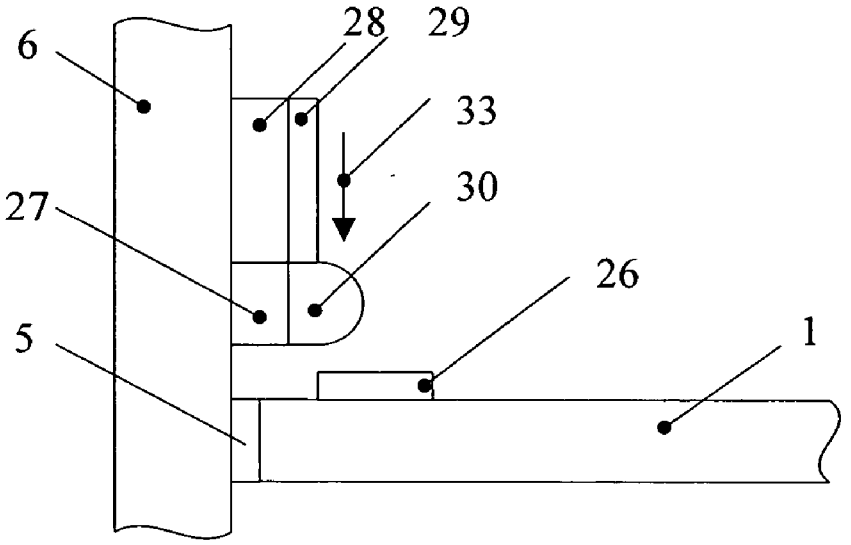


Fig. 5b

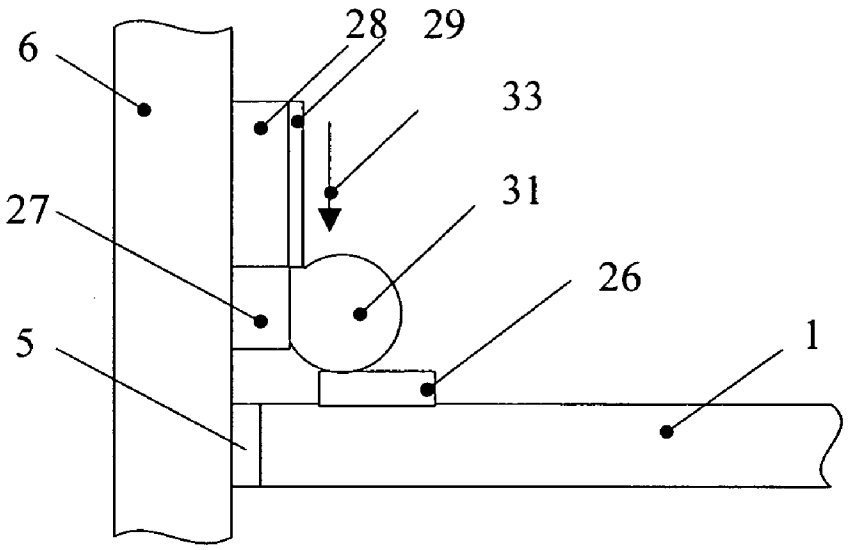


Fig. 5c

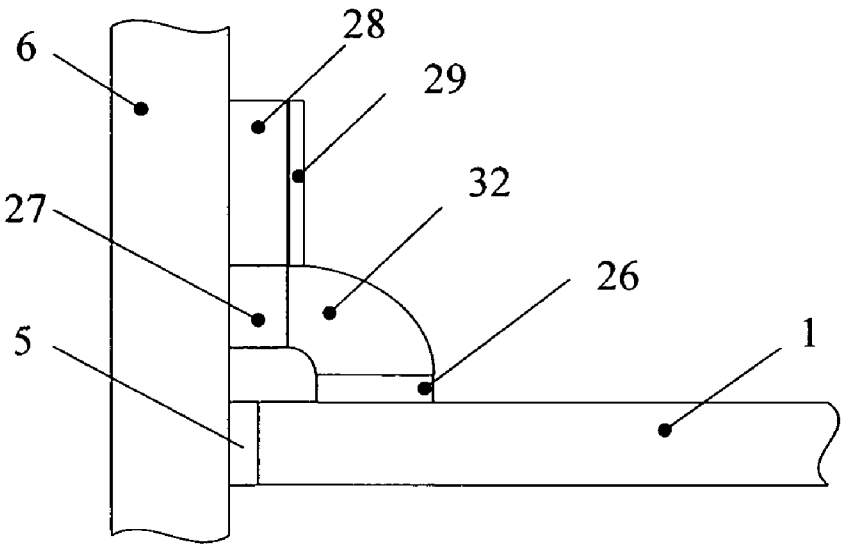


Fig. 5d

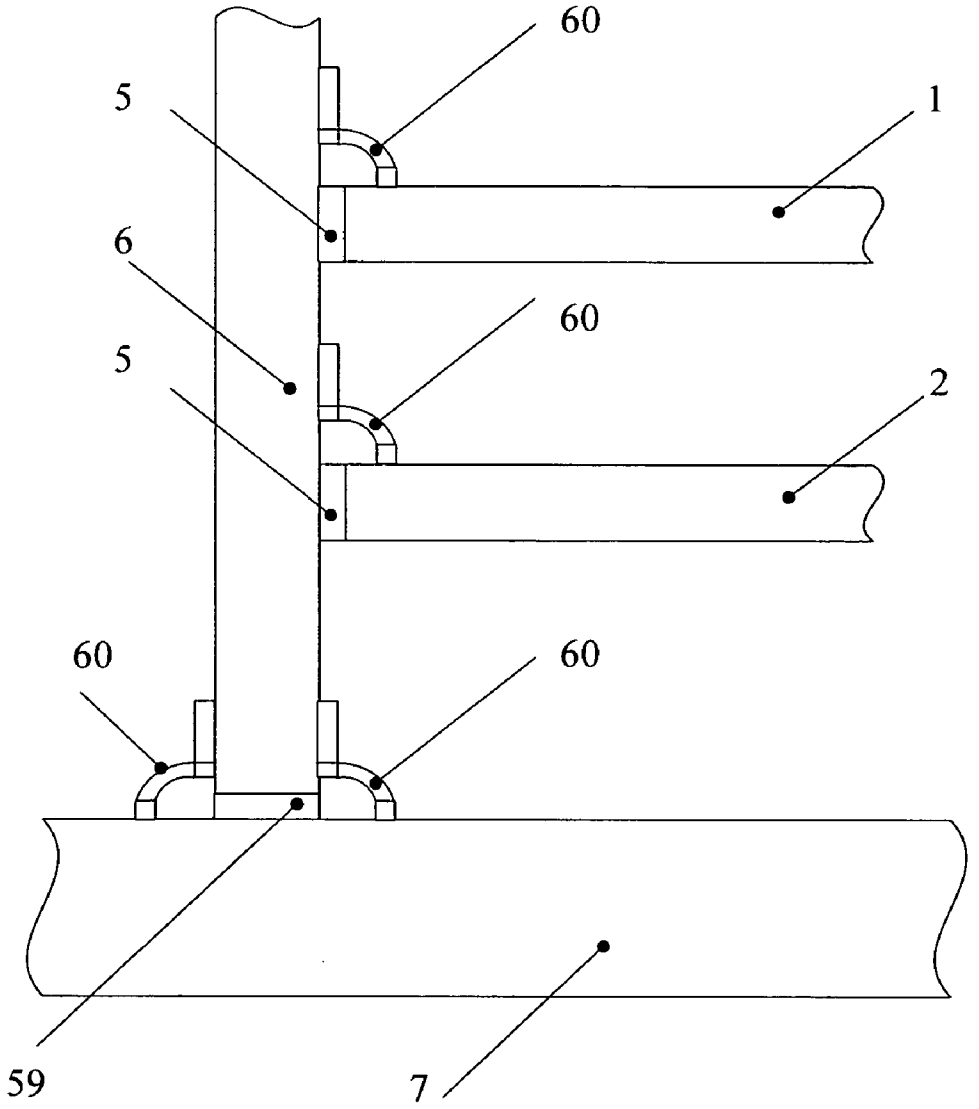


Fig. 6

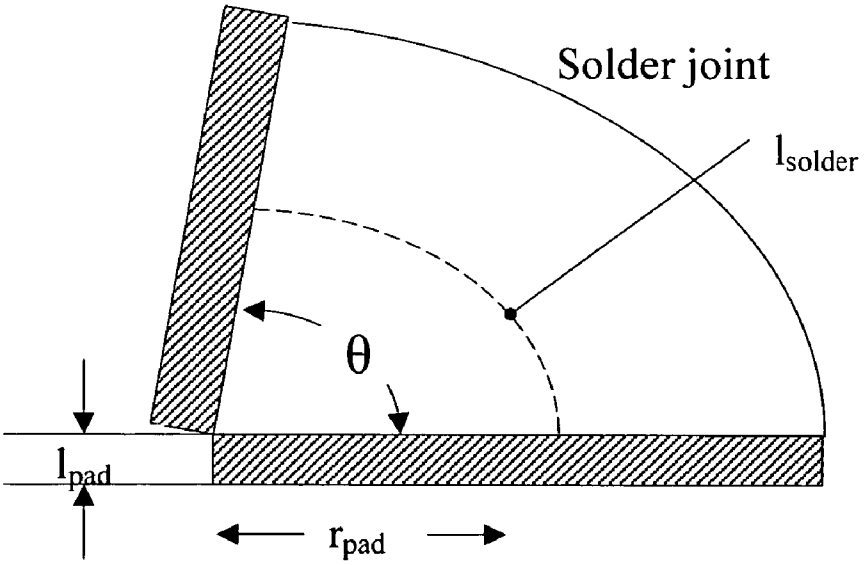

Solder joint
l_{solder}
θ
l_{pad}
r_{pad}

Fig. 7a

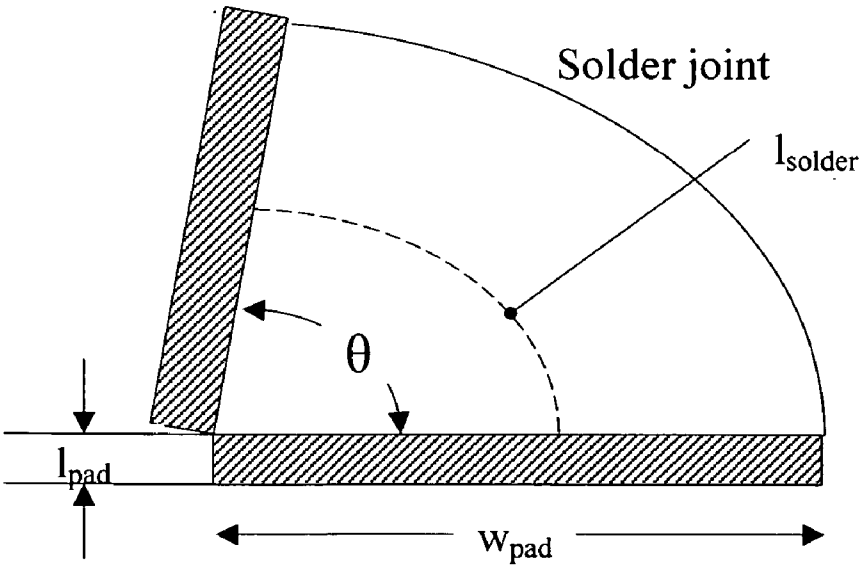

Solder joint
l_{solder}
θ
l_{pad}
w_{pad}

Fig. 7b

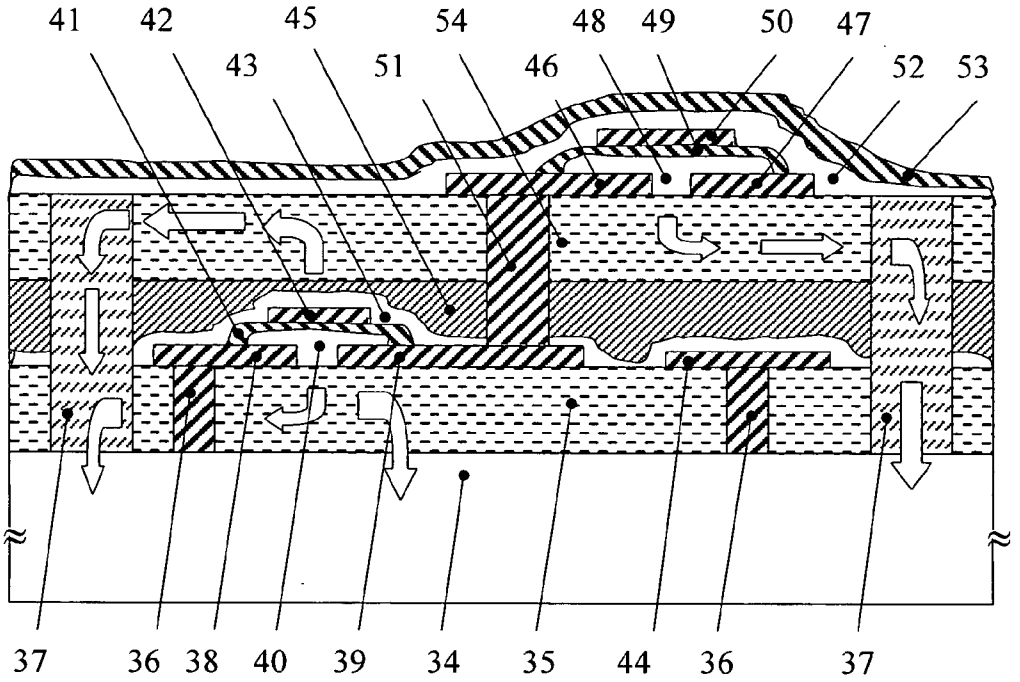


Fig. 8

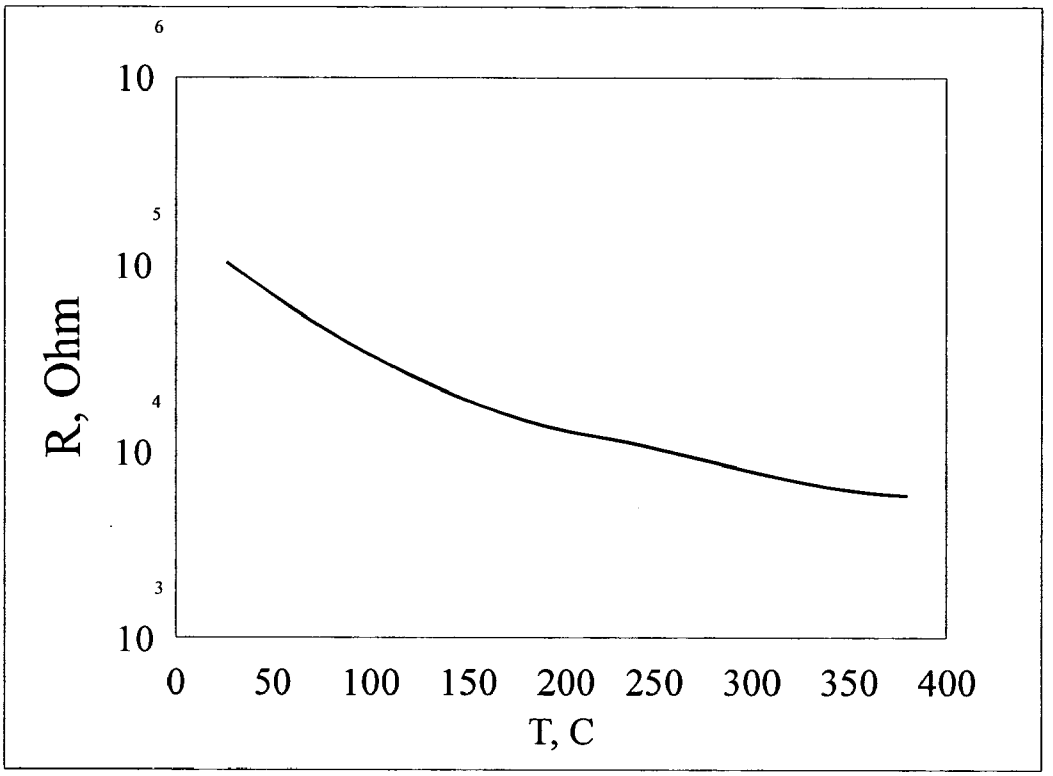


Fig. 9

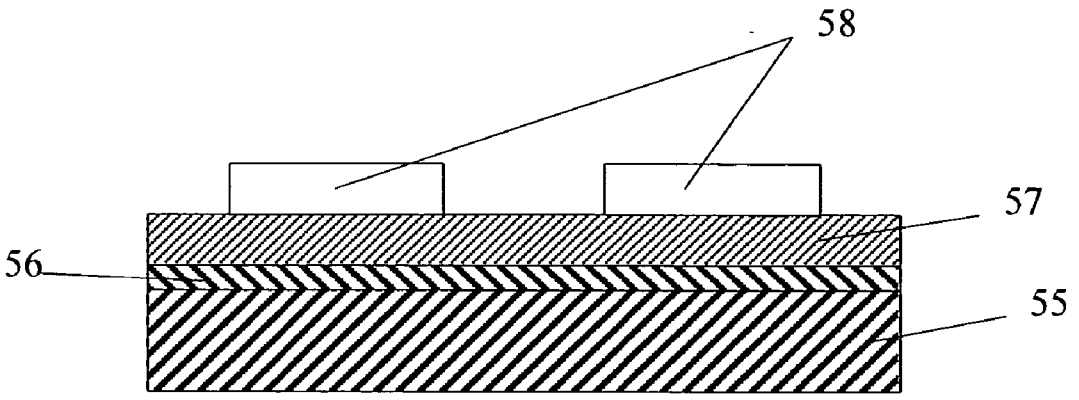


Fig. 10

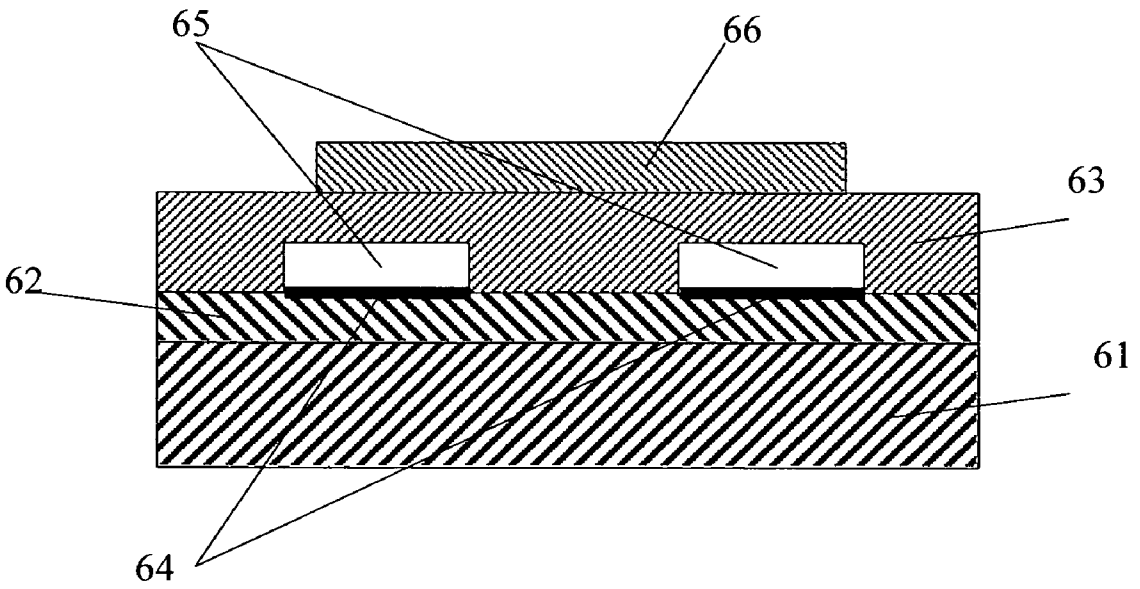


Fig. 11

THREE-DIMENSIONAL INTEGRATED CIRCUIT WITH INTEGRATED HEAT SINKS

RELATED APPLICATION

[0001] This application claims the benefit of, and priority to, of U.S. provisional patent application Ser. No. 60/152,256 filed on Oct. 17, 2003, entitled "Three-Dimensional Integrated Circuit with Integrated Heat Sinks", the entire disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to a three-dimensional integrated circuit incorporating an integrated heat sink for dissipating heat produced by the integrated semiconductor devices mounted thereon.

BACKGROUND OF THE INVENTION

[0003] Conventional ICs are formed on the surface of a silicon substrate. A high integration is achieved through enlarging the chip area and employing a discrete approach, which implies making each individual element small and each wiring fine. The discrete approach has limitations in wafer process technology. Accordingly, three-dimensional ICs have been proposed.

[0004] However, the dissipation of heat generated by the integrated components becomes a problem in three-dimensional integrated circuits. To function appropriately, each component should be kept at or below a preset tolerable operating temperature In particular, memory devices running at a high transfer rate produce heat during operation and the integrated circuit rapidly heats up. Without proper heat dissipation, the IC may overheat and malfunction.

[0005] In the general case, a heat sink is used for dissipating heat produced by components in an integrated circuit. IC. The heat sink has to be in good thermal contact with each component and exposed to the surrounds to maximize heat dissipation. In a three-dimensional circuit it is difficult to provide sufficient exposure of the heat sink to the surrounds.

SUMMARY OF THE INVENTION

[0006] It is an object of the present invention to provide a three-dimensional integrated circuit with improved heat dissipation.

[0007] The disclosed invention represents a three-dimensional integrated circuit comprising a heat sink and a set of discrete integrated circuits arranged one above another and system of integrated heat sinks for conducting heat from the integrated circuits to the heat sink. Each of said discrete integrated circuits has a heat-conducting substrate and functional elements formed on front and/or rear substrate surface, wherein at least one of the functional elements is a heat-generating element. The integrated heat sinks are in thermal contact both with at least one of said substrates and with the heat sink. In said three-dimensional integrated circuit the widths, lengths, thicknesses and thermal conductivities of the substrates of discrete integrated circuits, as well as the number, cross sectional areas, lengths, and thermal conductivities of said integrated heat sinks, are selected so as to ensure that the temperature in any region of the three-dimensional integrated circuit does not exceed a preset tolerable operation temperature determined for previously established intensities of said functional heat-generating elements and their known positions in the three-dimensional integrated circuit.

[0008] Another aspect of the present invention is a monolithic three-dimensional integrated circuit comprising a heat sink and a monolithic multilayer structure representing a system of unit integrated circuits stacked one above another. This monolithic multilayer structure is mounted on said heat sink. Each of said unit integrated circuits comprises a heat-conducting substrate having front surface and rear surface facing the heat sink. Each of these unit integrated circuits comprises a conducting wiring pattern formed on the front substrate surface, and functional elements mounted on front substrate surface and connected to the wiring pattern. One or more of these elements is a heat-generating element. Each unit integrated circuit is provided with a protective insulating layer, formed above said wiring pattern and said functional elements, and a planarization layer possessing a flat surface. This flat surface of the planarization layer, which is most distant from the front surface of the substrate, serves a base for the subsequent unit integrated circuit of said stacked system. Said three-dimensional monolithic integrated circuit also contains a system of integrated heat sinks. Each integrated heat sink is in thermal contact with said heat sink and penetrates into the monolithic multilayer structure, thus providing thermal contact with at least one substrate of said unit integrated circuits. In this monolithic three-dimensional integrated circuit, the substrate thicknesses and thermal conductivities, as well as the number, cross sectional areas, lengths, arrangement, and thermal conductivities of said integrated heat sinks, are selected so as to ensure that the temperature in any region of the three-dimensional monolithic integrated circuit would not exceed a preset tolerable operation temperature determined for preliminarily established intensities of the said functional heat-generating elements and their known positions in the three-dimensional monolithic integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Other objects and advantages of the present invention will become apparent upon reading the detailed description of the invention, and upon reference to the drawings, in which:

[0010] **FIG. 1***a* is a schematic diagram of a three-dimensional integrated circuit representing a system of several discrete integrated circuits.

[0011] **FIG. 1***b* is a sectional view of the integrated circuit of **FIG. 1***a* taken along the line A-A.

[0012] **FIG. 2** shows the main types of electrically conducting elements for connecting to neighboring discrete integrated circuits in a three-dimensional integrated circuit.

[0013] **FIG. 3** shows an example of electrical connections between discrete integrated circuits in a three-dimensional integrated circuit via electrically conducting elements of various types.

[0014] **FIG. 4** shows an axonometric image of a system of substrates, integrated heat sinks, and a heat sink according to the present invention.

[0015] **FIGS. 5***a*-**5***d* are cross-sections of arched solder joint with pads according to the present invention, during intermediate fabrication steps.

[0016] **FIG. 6** is a schematic diagram of a three-dimensional integrated circuit with integrated heat sinks according to the present invention, in which thermal contacts are obtained with the use of arched solder joints.

[0017] **FIGS. 7***a* **-7***b* show schematic diagrams of the arched solder joints with dimensions according to the present invention.

[0018] **FIG. 8** is a schematic diagram of a three-dimensional monolithic integrated circuit according to the present invention.

[0019] **FIG. 9** shows the typical temperature dependence of resistance of an semiconductor thin crystal film sample.

[0020] **FIG. 10** shows a thin-film transistor structure with top source and drain contacts.

[0021] **FIG. 11** shows a thin-film transistor structure with bottom source and drain contacts.

DETAILED DESCRIPTION OF THE INVENTION

[0022] The present invention now will be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may be, however, embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout.

[0023] One preferred embodiment of the disclosed invention is a three-dimensional integrated circuit (IC) comprising a heat sink, a set of discrete ICs arranged one above another, and system of integrated heat sinks for conducting heat from the integrated circuits to the heat sink. This set of discrete ICs is mounted on said heat sink. Each of said discrete ICs has a heat-conducting substrate, and functional elements formed on front and/or rear substrate surface, wherein at least one of the functional elements is a heat-generating element. The three-dimensional IC also comprises a system of integrated heat sinks in thermal contact with at least one of said substrates and with the heat sink. In this three-dimensional IC, the widths, lengths, thicknesses and thermal conductivities of the substrates of discrete integrated circuits, as well as the number, cross sectional areas, lengths, and thermal conductivities of said integrated heat sinks, are selected so as to ensure that the temperature in any region of the said three-dimensional IC will not exceed a preset tolerable operation temperature determined for preliminarily established intensities of the said heat-generating elements and their known positions in the three-dimensional IC. In disclosed invention the thermal fluxes from heat sources first spread over heat-conducting substrates, then enter into integrated heat sinks, and are eventually dissipated in the heat sink.

[0024] The functional elements of discrete IC are thin-film passive elements (capacitors, resistors, and inductive coils) and active semiconductor devices (transistors and diodes).

[0025] In one embodiment of the disclosed three-dimensional IC, at least one substrate is made of Al_2O_3 based ceramics. In another variant of the disclosed three-dimensional IC, the substrate of the bottom discrete integrated circuit is in direct thermal contact with the heat sink.

[0026] In another preferred embodiment, the present invention provides a three-dimensional IC in which at least one said functional element is made using a semiconductor thin crystal film (SCTCF) formed by rodlike supramolecules composed of at least one organic compound with conjugated π-system, wherein a crystal structure of the film has an intermolecular spacing of 3.4±0.3 Å in the direction of at least one crystal axis. This SCTCF is based on an aromatic polycyclic compound and has the electron-hole type of conductivity. A necessary condition is the presence of a developed system of conjugated π-electronic bonds between conjugated aromatic rings of the molecules and the presence of groups (such as amine, phenol, ketone, etc.) lying in the plane of the molecule and involved into the aromatic system of bonds. The molecules and/or their molecular fragments possess a planar structure and are capable of forming supramolecules in solutions. Another necessary condition is the maximum overlap of π-orbitals in the stacks of supramolecules.

[0027] **FIGS. 1***a* and **1***b* illustrate one possible embodiment of a three-dimensional (3D) integrated circuit according to the disclosed invention. The three-dimensional IC comprises a set of discrete integrated circuits, each formed on a separate substrate (**1-4**) made of heat-conducting material. Al_2O_3 based ceramics offers an example of such a material. In the description to follow, these discrete integrated circuits are referred to as elementary ICs. Three-dimensional integrated circuits are not restricted to four discrete integrated circuits as depicted in **FIG. 1***a*. Each discrete substrate accommodates an IC topology which includes heat-generating elements (**1***a*-**1***d* on substrate **1**, **2***a*-**2***d* on substrate **2**, etc.). The discrete integrated circuits can be electrically connected to each other (neither wiring topologies not interconnections are depicted in **FIG. 1**). The substrates are fastened with heat-conducting glue or solder layers **5** to integrated heat sinks **6** which in turn are connected to a common heat sink **7** so as to form a 3D structure. Coating **8** protects the three-dimensional IC structure. Active elements in such ICs can be discrete diodes and transistors, as well as microassemblies (each including several diodes and/or transistors) made of inorganic or organic materials.

[0028] In **FIG. 1***a*, the functional heat-generating elements of ICs are depicted schematically, with black areas representing regions containing heat sources. In a thin-film transistor, the main heat source is the region of a conducting channel between source and drain. In this region, the heat is generated as a result of current passage in the course of transistor operation. Another heat source in a TFT is related to the gate circuit. Heat generated in the functional heat-generating elements is initially dissipated in the corresponding substrates. Arrows in **FIGS. 1***a* and **1***b* indicate the directions of thermal fluxes in the 3D structure under consideration. Heat liberated in the bottom discrete IC is transferred directly to the heat sink, while heat generated in the other discrete ICs (**1**, **2**, **3** and other analogous discrete discrete circuits) is first transferred to integrated sinks **6** and then to the common heat sink **7**.

[0029] **FIG. 1***b* shows a cross section of the 3D integrated circuit of **FIG. 1***a* taken along the line AA'. The integrated

heat sinks integrated into the three-dimensional integrated IC have a rectangular cross section. According to the disclosed invention, the cross section of these integrated heat sinks can be of arbitrary shape selected from circle, ellipse, square, rectangle, or polygon. The geometry of elements of a 3D integrated circuit according to this invention can vary. Variable parameters include the thicknesses of the regions of functional heat-generating elements representing heat sources, the thicknesses of the substrates under discrete ICs, and the dimensions (height, width, thickness) of the integrated heat sinks. By appropriately selecting these parameters, it is possible to provide for the optimum thermal regime of operation of the disclosed 3D integrated circuit, to assure that the working temperature of any active element in the 3D scheme will not exceed a preset maximum tolerable operation temperature.

[0030] **FIG. 2** shows the main types of electrically conducting elements that can be used for connecting neighboring discrete integrated circuits so as to provide for 3D integration. For the sake of simplicity, **FIG. 2** shows a single discrete IC comprising a substrate **1** with topological wiring patterns formed on the rear and front surfaces. Metallization layers **9** and **10** represent these patterns. In addition, both rear and front substrate surfaces bear protective dielectric layers **11** and **12** respectively. The rear protective layer **11** also includes contact pads **13**, and the frontal protective layer **12** includes analogous contact pads **14**. These contact pads are used to provide for the electric connections between neighboring discrete integrated circuits. To this end, metallized (metal-filled) window **15** provides for the connection between topological wiring pattern of the front surface and one of the contact pads **14**. By the same token, metallized window **16** connects topological wiring pattern of the rear surface to one of the front contact pads **14**, metallized window **17** connects one of the frontal contact pads **14** to one of the rear pads **13**, metallized window **18** connects topological wiring pattern of the front surface to one of the rear contact pads **13**, and metallized window **19** connects topological wiring pattern of the rear surface to one of the rear contact pads **13**. Said discrete IC is fastened to integrated heat sinks **6** with a layer of heat-conducting glue or solder **5**, which provides for a good thermal contact with low thermal resistance. In turn, the integrated heat sinks **6** are in good thermal contact with the heat sink **7**. Arrows in **FIG. 2** indicate the paths of thermal fluxes in the given 3D integrated circuit.

[0031] **FIG. 3** shows how various types of electrically conducting elements via metallized windows can be used for connecting several discrete integrated circuits in a 3D structure. For the sake of simplicity, **FIG. 3** shows the electrically conducting elements between three discrete ICs (**1**-**3**). In order to link any two discrete integrated circuits, for example **1** and **2**, it is necessary to connect contact pads on the front and/or rear surface of the first IC to contact pads on the front and/or rear surface of the second IC. In other words, the wiring patterns of the discrete ICs should contain connection points that have to be linked during assembly of the 3D integrated circuit. Similarly, to link discrete ICs **2** and **3**, it is necessary to connect contact pads on the front and/or rear surface of the second IC to contact pads on the front and/or rear surface of the third IC. In **FIG. 3**, a system of metallized windows and contact pads **20** connects a topological pattern of the front surface of IC **1** to that of the front surface of IC **2**, while the system of metallized windows and contact pads type **21** connects a topological pattern of the rear surface of IC **1** to that of the front surface of IC **2**, and the system **22** connects a topological pattern of the front surface of IC **1** to that of the rear surface of IC **2**. By the same token, system **23** connects a topological pattern of the rear surface of IC **1** to that of the front surface of IC **3**, system **24** connects the front surface of IC **2** to front surface of IC **3**, and system **25** connects the rear surface of IC **2** to the rear surface of IC **3**.

[0032] **FIG. 4** shows a 3D integrated circuit according to the present invention, comprising first **1** and second **2** substrates, integrated heat sinks **6**, and a heat sink **7**. Substrates **1** and **2** contain rows of pads **26** and integrated heat sinks **6** contain rows of pads **27** connected to elongated pad extensions **28**. The pads may differ in the number, dimensions, and arrangement on substrates **1** and **2**. Although square pads are depicted in **FIG. 4**, they can be of any shape. The rows of pads can be also be present on the rear surfaces of substrates **1** and **2**, as well as on their edges (this variant is not shown). Said pairs of pads can be used for making thermal contacts of different substrates with integrated heat sinks. Both substrate **1** and substrate **2** may represent integrated circuit chips, printed circuit boards, multi-layer ceramic substrates, or any other substrates used in microelectronics. Methods for the formation of pads on such substrates are well known and need not be described further herein.

[0033] The spacing of pads **27** in the rows on integrated heat sinks **6** preferably corresponds to the spacing of the corresponding row of pads **26** in substrates **1** or **2**. It should be noted that the pad pitches need not be identical, since one substrate can be mounted on heat sink at an angle, so that one pad pitch may be less than the other pitch.

[0034] As will be described below, substrates **1** and **2** are mounted on integrated heat sinks **6** by means of soldering, whereby arched solder joints are formed between pads on the substrates and those on the heat sinks. In order to form the solder joints in a preferred embodiment of the invention, pads in at least one of the first and second rows are provided with elongated pad extensions, which are narrower than the pads. Thus, as shown in **FIG. 4**, the row of pads **27** has such a system of elongated pad extensions **28**, which are narrower than the pads. Each elongated pad extensions **28** is connected to the corresponding pad **27** in the row. The pad extensions, as well as the pads, are preferably covered with a layer of solder.

[0035] **FIGS. 5*a*-5*d*** show the cross sections of arched solder joint with pads according to the present invention, involving substrate **1** and integrated heat sink **6**, during intermediate fabrication steps. As shown in **FIG. 5*a***, substrate **1** is nonparallel to integrated heat sink **6** and the edge of this substrate is close to integrated heat sink **6**. The substrate contains a row of pads **26**, and integrated heat sink **6** contains a row of pads **27** adjacent to and arranged along the edge of substrate **1**. It will also be understood that two, three, or more substrates containing the appropriate rows of pads can be mutually oriented for assembly.

[0036] As is also depicted in **FIG. 5*a***, pads in one of the rows (in this case, pads **27**) have elongated extensions **28**. Such pad extensions can be formed on substrate **1** and/or integrated heat sink **6** or both, depending on the particular geometry of the pads, the volumes of solder bumps that have

to be formed, and other arched solder joint parameters. As is shown in **FIG. 5***a*, pads **27** and the associated elongated pad extensions **28** are coated with a layer of solder **29**.

[**0037**] **FIG. 5***a* depicts integrated heat sink **6** oriented perpendicularly to substrate **1**. However, the integrated heat sink and substrate can be oriented at an angle relative to one another. **FIG. 5***a* shows a bonding layer **5**, which can be used to attach the integrated heat sink and substrate to one another prior to soldering. The bonding layer may be glue or flux or any other common adhesive used in the microelectronic industry. The material of bonding layer **5** can possess high thermal conductivity, thus favoring the formation of a thermal contact with lower thermal resistance between the substrate and the integrated heat sink. Alternatively, a clamp or other fixture can be used to hold the substrate and heat sink together in the absence of a bonding layer, or the force of gravity may hold them in contact.

[**0038**] The solder layer **29** on pads **27** and pad extensions **28** can be formed by various methods. Techniques for forming a solder layer on pads and extended regions could be found for example in WO 9,631,905 "A Solder Bump Structure for Microelectronic Substrate" and U.S. Pat. No. 6,389,691 "Methods for Forming Integrated Redistribution Routing Conductors and Solder Bumps".

[**0039**] **FIGS. 5***b*, **5***c* and **5***d* illustrate the reflow soldering process. Initially, as shown in **FIG. 5***b*, a solder bump **30** forms on pad **27** as solder **29** flows from over elongated pad extension **28** to pad **27** in the direction shown by arrow **33**. Solder flows from the elongated pad extension onto the pad due to the surface tension within the solder, which causes the flowing solder to flow from a relatively thin extension to the relatively wide pad, as described in WO 9,631,905 and U.S. Pat. No. 6,389,691. As the reflow continues (**FIG. 5***c*), a solder bump **31** of increasing volume forms since more solder is supplied from elongated pad extension **28** to pad **27**. As also shown in **FIG. 5***c*, reflow causes the solder bump **31** to expand laterally beyond the edge of substrate **1** and thereby contact pad **26** on substrate **1**. Finally, once the increasing solder bump contacts pad **26**, the surface tension of the solder will create an arched solder joint **32** (**FIG. 5***d*) that extends from pad **27** on heat sink **6** to pad **26** on substrate **1**. The arched solder joint **32** may be considered as a part of a ring (here, a quarter-ring arc). As is depicted in **FIG. 5***d*, the arched solder joint preferably possesses a uniform transverse cross section, which represent an excellent conductor for thermal flux. In other configurations, the cross-section need not be uniform. For example, both pads may be rectangles rotated 90° relative to one another, so that the arched solder joint is also rotated by 90°. The arched solder joints can be used for mechanical connections in the microelectronic packages.

[**0040**] Let us consider the solder packaging method in more detail. According to **FIGS. 5***a*-**5***d*, solder layer **29** is formed using a patterned plating template that defines regions of differing internal pressures in the molten solder. During reflow, the molten solder flows preferentially to the low-pressure regions, thereby forming a large bump that extends beyond the edge of the substrate. The bump can wet the solder pad and form an arched solder joint that provides thermal connection and/or mechanically supports the package. The method illustrated in **FIGS. 5***a*-**5***d* begins with the formation of a solder bump on integrated heat sink **6**. It is clear that a solder bump can be as well formed on substrate **1** and then expanded to contact a pad on integrated heat sink **6**. In another alternative, solder bumps may be formed on both integrated heat sink and substrate, and then expand to contact one another and thereby form the arched solder joint **32**. Arched solder joints **32** offer several thermal and mechanical advantages. The arched solder joint may also provide structural support, while allowing some compliance for improved reliability, in contrast to the conventional fillet type joints.

[**0041**] The disclosed package may provide many new system assembly options with low weight, compactness, and good thermal management, together with low cost and potentially enhanced performance. One application of the technology is a compact, low cost multi-chip module assembly where there may be significant reduction in the area devoted to the second level package. A typical application may be for large-scale memories. Another application may be in mixed signal assembly integration. Thus, for example, an assembly may be provided with mixed analog/digital/microwave systems in a compact package, as illustrated below.

[**0042**] **FIG. 6** is a schematic diagram illustrating a preferred embodiment of the three-dimensional IC with integrated heat sinks according to the present invention, in which thermal contacts are obtained with the use of a solder material. Here, the thermal contacts of substrates **1** and **2** with integrated heat sink **6** and the thermal contact of this integrated heat sink **6** and the heat sink **7** are provided by arched solder joints **60**. The bonding layer **59** between the edge of the integrated heat sink **6** and the heat sink **7** provides for an additional thermal contact. To this end, the adhesive material of layer **59** must possess high thermal conductivity. For the sake of simplicity, other elements of the 3D integration in **FIG. 6** are not depicted.

[**0043**] Since the main heat removal path is via conduction through a single row of solder bumps, thermal flux management is important for this technology. Each of these solder joints can be modeled by a series of thermal resistances involving the solder joint and the pad resistance on each end. A thermal model for this 3D technology with round pads is shown in **FIG. 7***a*. This model assumes the contact pads to be round, of radius r_{pad} and thickness l_{pad}, and possess a thermal conductivity of k_{pad}, while the solder material possesses a thermal conductivity of k_{solder}. According to this model, the thermal path length L_{solder} is related to the cross section area of the path. The thermal path length is

$$l_{solder}=\theta(\text{rad})\cdot r_{pad}$$

[**0044**] and the cross sectional area is

$$A_{solder}=\pi\cdot r^2_{pad}.$$

[**0045**] Therefore, the solder thermal resistance is

$$R_{solder}=\theta/(\pi\cdot k_{solder}\cdot r_{pad}).$$

[**0046**] However, the thermal resistance of the pad is

$$R_{pad}=l_{pad}/(\pi\cdot k_{pad}\cdot r^2_{pad}).$$

[**0047**] This makes the total thermal resistance

$$R_{total}=(2R_{pad}+R_{solder})/n,$$

[**0048**] where n is the number of solder bumps connecting the substrate to the heat sink. Since the bumps form parallel

heat conduction paths to the heat sink, the total thermal resistance is inversely proportional to n. This number is

$$n=L/(2\cdot r_{pad}),$$

[0049] where L is the length of row of pads. Therefore, total thermal resistance is

$$R_{total}=4\cdot l_{pad}/(\pi\cdot L\cdot k_{pad}\cdot r_{pad})+2\cdot\theta/(\pi\cdot L\cdot k_{solder}).$$

[0050] In this expression, the first term represents the thermal resistance of two contact pads and the second, that of the solder. An analysis of this relation shows that the thermal resistance of the solder is independent of the cross section radius (r_{pad}). At the same time, the thermal resistance of the contact pads increases with decreasing radius r_{pad}. Therefore, it is possible that, for sufficiently small r_{pad}, the thermal resistance of the contact pads will exceed that of the solder bumps. In order to avoid this, r_{pad} has to be limited by the condition that the thermal resistance of the contact pads must not exceed that of the solder bumps.

[0051] Thus, according to the above expression, that the following condition should be fulfilled:

$$r_{pad}\geqq(2\cdot l_{pad}/\theta)\cdot(k_{solder}/k_{pad}).$$

[0052] **FIG. 7***b* illustrates a thermal model for the 3D package with square pads is shown in **FIG. 7***b*. This model assumes the contact pads to be squares with a side length of w_{pad}, a thickness of l_{pad}, and a thermal conductivity of k_{pad}, while the solder material possesses a thermal conductivity of k_{solder}. According to this model, the thermal path length is

$$l_{solder}=\theta(\text{rad})\cdot w_{pad}/2$$

[0053] and the cross sectional area is

$$A_{solder}=w^2_{pad}.$$

[0054] Therefore, the solder thermal resistance is

$$R_{solder}=\theta/(2\cdot k_{solder}\cdot w_{pad}).$$

[0055] However, the thermal resistance of the pad is

$$R_{pad}=l_{pad}/(k_{pad}\cdot w^2_{pad}).$$

[0056] This gives for the total thermal resistance

$$R_{total}=(2R_{pad}+R_{solder})/n,$$

[0057] where n is the number of solder bumps connecting the substrates to the heat sink. Since the bumps form parallel heat conduction paths to the heat sink, the total thermal resistance is inversely proportional to n. This number is

$$n=L/(2\cdot w_{pad}),$$

[0058] where L is the length of row of pads. Therefore, the total thermal resistance is

$$R_{total}=2\cdot l_{pad}/(L\cdot k_{pad}\cdot w_{pad})+\theta/(2\cdot L\cdot k_{solder}).$$

[0059] In this expression, the first term represents the thermal resistance of two contact pads and the second, that of the solder. An analysis of this relation shows that the thermal resistance of the solder is independent of the cross section radius, i.e. of the square side length (w_{pad}). At the same time, the thermal resistance of the contact pads increases with decreasing w_{pad}. Therefore, it is possible that, for sufficiently small w_{pad}, the thermal resistance of the contact pads will exceed that of the solder bumps. In order to avoid this, w_{pad} has to be limited by the condition that the thermal resistance of the contact pads must not exceed that of the solder bumps.

[0060] Thus, according to the above expression, that the following condition should be fulfilled:

$$w_{pad}\geqq(4\cdot l_{pad}/\theta)\cdot(k_{solder}/k_{pad}).$$

[0061] **FIG. 8** presents a schematic diagram of another possible embodiment of the 3D integrated circuit according to the present invention. Each layer in this structure is formed immediately on the preceding layer, so that the 3D structure is monolithic. This monolithic 3D integrated circuit is carried on plate **34** representing a heat sink. The heat sink should be made of a material possessing high thermal conductivity, such as copper, which can simultaneously serve as the electric "ground" of the IC. The base carries a layer of dielectric **35**, which also possesses high thermal conductivity (a candidate material is Al_2O_3 ceramics). The dielectric layer contains windows (holes), which can be either metallized (to provide for electrical ground **36**) or made of a material which possesses high thermal conductivity (acting as integrated heat sinks **37**). Integrated heat sinks can be made either of Al_2O_3 based ceramics or of any other good heat conductor. Although not shown, the heat sink may be cooled by circulating a fluid therethrough.

[0062] A 3D monolithic structure of the type under consideration may contain several dielectric layers. The IC depicted in **FIG. 8** contains two such layers (**35** and **54**) bearing all the active (diodes, transistors) and passive (capacitors, inductances, and resistors) elements of the 3D circuit. **FIG. 8** shows an IC including a thin-film transistor and a contact area **44** formed on the dielectric layer **35** and grounded via metallized window **36**. The transistor contains source **38** and drain **39** electrodes formed immediately on the dielectric layer **35** (the source is grounded via metallized window **36**). The transistor may contain a layer of inorganic or organic semiconductor **40**, insulating layer **41**, gate electrode **42**, and a protective layer **43**. During operation of the transistor, the heat is liberated in a current-conducting channel formed between source and drain in the semiconductor layer on boundary with an insulating layer and in the gate circuit of the transistor (during switching between open and closed states). Arrows in **FIG. 8** indicate the directions of heat transfer from the transistor channel and the gate circuit.

[0063] The 3D monolithic integrated circuit of **FIG. 8** contains a planarization layer **45** carrying the second dielectric layer **54**. This layer bears the second thin-film transistor with source **46** and drain **47** electrodes, a layer of organic semiconductor **48**, an insulating layer **49**, and gate electrode **50**. The drain of the first thin-film transistor is connected to the source of the second transistor via metallized window **51** formed in the protective layer **43**, planarization layer **45**, and dielectric layer **54**. In addition, the IC contains protective layers for the transistor **52** and the whole structure **53**. The dimensions of all elements of the monolithic 3D integrated-circuit can be considered as variable parameters. These include the thicknesses of current-conducting channels **35** and dielectric layers **54** and the dimensions (height, width, thickness) of the integrated heat sinks **37**. By varying these parameters, it is possible to provide for the optimum IC operation thermal regime in which the working temperature of the 3D structure will not exceed a preset maximum tolerable IC temperature.

[0064] The 3D integrated circuits depicted in **FIGS. 1 and 8** are not the only possible embodiments of the disclosed

invention. In particular, active thin-film elements based on inorganic semiconductors can be incorporated into the integrated circuit together with organic thin-film transistors and diodes. In this case, the 3D structure will contain additional layers of inorganic semiconductors (e.g., silicon). The number of integrated heat sinks is not limited by four as in **FIG. 1***b* or two as in **FIG. 8**. The arrangement and number of such integrated heat sinks is selected so as to provide for the normal thermal regime of operation for all elements of the integrated circuit.

[**0065**] In one variant of the disclosed three-dimensional IC, at least one functional heat-generating element is a semiconductor transistor.

[**0066**] In another variant of the disclosed three-dimensional IC, at least one functional heat-generating element is a semiconductor diode comprising a semiconductor layer and electrode (cathode and anode) layers. These layers can also be made of both organic and inorganic materials. Therefore, there are three possible variants, whereby (i) all layers in the transistor structure are made of organic materials, (ii) all layers are made of inorganic materials, or (iii) some layers are organic and the others are inorganic.

[**0067**] In still another variant of the disclosed three-dimensional IC, at least one functional heat-generating element is a thin film resistor.

[**0068**] In one possible variant of the disclosed three-dimensional IC, at least one integrated heat sink is made of an Al_2O_3 based ceramic material.

[**0069**] In another embodiment of the disclosed three-dimensional IC, at least one integrated heat sink has a front surface facing said discrete integrated circuits and an edge face facing the heat sink. Said integrated heat sink has the shape of the cross section parallel to rear surface of said substrates, which shape is selected from the list comprising circle, ellipse, square, rectangle, polygon, or any combination thereof.

[**0070**] In order to provide for the effective heat removal from a three-dimensional IC, it is necessary that thermal contacts between heat-conducting substrates and integrated heat sinks, as well as the thermal contacts between these integrated heat sinks and the heat sink, possess low thermal resistances. In a possible embodiment of present invention, the disclosed three-dimensional IC further comprises at least one bonding layer made of a heat-conducting adhesive material. This layer is located between the front surface at least of one of said integrated heat sinks and the edge face at least of one of said substrates. Said substrate is oriented relative to integrated heat sink so that the edge face of this substrate is adjacent said integrated heat sink.

[**0071**] In one embodiment of the disclosed invention the three-dimensional integrated circuit further comprises at least one bonding layer made of a heat-conducting adhesive material. Said bonding layer is located between said heat sink and the edge face at least of one of said integrated heat sinks. The integrated heat sink is oriented so that its edge face is adjacent to said heat sink.

[**0072**] In one possible variant of the invention, the three-dimensional integrated circuit further comprises at least one set of arched solder joints forming thermal contacts between the front surface of at least one of said integrated heat sinks and at least one surface of at least one of said substrates. In another variant of the three-dimensional integrated circuit, said arched solder joints have nonuniform cross sections along their lengths. In still another variant, the three-dimensional integrated circuit further comprises at least two rows of pads, wherein the first row of pads is positioned on said integrated heat sink and the second row of pads on said substrate adjacent to the first row of pads and arranged along the edge face of said substrate, said pads in at least one of these rows having elongated pad extensions which are narrower than the pads and said set of arched solder joints connects said pads of first row with pads of second row. In yet another variant of the invention, the three-dimensional integrated circuit further comprises at least one bonding layer made of a heat-conducting adhesive material and located between said heat sink and the edge face at least of one of said integrated heat sinks.

[**0073**] The disclosed invention makes use of several main types of conducting elements between discrete ICs, which allow these ICs to be electrically connected into a three-dimensional IC. Some possible variants are considered below.

[**0074**] In a possible variant of the disclosed three-dimensional integrated circuit, at least one discrete integrated circuit comprises the conducting wiring pattern and the functional elements formed on the front and rear substrate surfaces. Said discrete integrated circuit further comprises a front protective dielectric layer covering the wiring pattern and the functional elements situated on the front surface of the substrate, and a rear protective dielectric layer covering the wiring pattern and the functional elements situated on the rear surface of the substrate. In one variant of the disclosed three-dimensional IC, at least one discrete IC comprises at least one frontal contact pad situated on said front protective dielectric layer. This discrete IC also contains at least one electrically conducting element penetrating through said front protective dielectric layer and the substrate so as to connect the wiring pattern (topology) of the rear surface of said substrate to said front contact pad.

[**0075**] In another variant of the disclosed three-dimensional IC, at least one discrete IC contains at least one rear contact pad, situated on said rear protective dielectric layer, and at least one electrically conducting element penetrating through said rear protective dielectric layer and through the substrate of this IC. This conductor connects the wiring pattern of the front surface of said substrate to said rear contact pad.

[**0076**] In still another variant of the disclosed three-dimensional IC, at least one discrete IC further comprises at least one front contact pad situated on said front protective dielectric layer at least one rear contact pad situated on said rear protective dielectric layer. This discrete IC also contains at least one electrically conducting element penetrating through the front protective dielectric layer, the substrate, and the rear protective dielectric layer so as to connect said frontal contact pad to said rear contact pad.

[**0077**] In a possible variant of the disclosed three-dimensional IC, at least one discrete IC further comprises at least one frontal contact pad, situated on said frontal protective dielectric layer, and at least one rear contact pad situated on said rear protective dielectric layer. This discrete IC also contains at least one electrically conducting element pen-

etrating through the frontal protective dielectric layer, the substrate, and the rear protective dielectric layer of this IC. This conductor connects said frontal contact pad to at said rear contact pad.

[0078] In yet another variant of the disclosed three-dimensional IC, at least one discrete IC comprises the conducting wiring pattern and the functional elements formed at least on the front substrate surface. Said discrete IC further comprises a front protective dielectric layer covering said wiring pattern and functional elements connected to the said wiring pattern, and at least one front contact pad, situated on said front protective dielectric layer. This discrete IC also contains at least one electrically conducting element penetrating through said front protective dielectric layer, which connects the wiring pattern to said front contact pad.

[0079] In still another possible variant of the disclosed three-dimensional IC, at least one discrete integrated circuit comprises the conducting wiring pattern formed at least on the rear substrate surface. This discrete integrated circuit further comprises a rear protective dielectric layer covering said wiring pattern and functional elements connected to the said wiring pattern, and at least one rear contact pad, situated on said rear protective dielectric layer. Said discrete IC also contains at least one electrically conducting element penetrating through said rear protective dielectric layer, which connects the wiring pattern to said rear contact pad.

[0080] In one variant of the disclosed three-dimensional integrated circuit, at least two of the adjacent discrete integrated circuits are formed so that first of them comprises the conducting wiring pattern and functional elements at least on the front substrate surface, and the second discrete integrated circuit positioned above the first circuit comprises the conducting wiring pattern and functional elements at least on the rear substrate surface. In another variant of the disclosed invention, the three-dimensional integrated circuit further comprises a first protective dielectric layer covering the conducting wiring pattern and functional elements of the first discrete integrated circuit. Furthermore, said three-dimensional integrated circuit further comprises at least one front contact pad, situated on said first protective dielectric layer. Then, said three-dimensional integrated circuit further comprises a second protective dielectric layer covering the conducting wiring pattern and functional elements of the second discrete integrated circuit. Finally, the three-dimensional integrated circuit further comprises at least one rear contact pad, situated on said second protective dielectric layer, and at least one electrically conducting element, which connects said rear contact pad with said front contact pad.

[0081] Another preferred embodiment of the present invention is a monolithic three-dimensional integrated circuit comprising a heat sink and a monolithic multilayer structure representing a system of unit ICs stacked one above another. This monolithic multilayer structure is mounted on a heat sink. Each of said unit ICs has a heat-conducting substrate having rear surface facing the heat sink and the front surface. Each of these unit ICs has a conducting wiring pattern (topology), formed on front substrate surface, and functional elements mounted on front substrate surface and connected to the wiring pattern, at least one of these elements being a functional heat-generating element representing a heat source. In addition, each unit IC is provided with a protective insulating layer formed above said wiring pattern and said functional elements, and a planarization layer formed above the protective layer. The flat surface of the planarization layer serves a base for the subsequent unit IC of said stacked system. Said three-dimensional monolithic IC also comprises a system of integrated heat sinks, wherein each integrated heat sink is in thermal contact with said heat sink and penetrate into the monolithic multilayer structure, thus providing thermal contact with at least one substrates of said unit ICs. In this monolithic three-dimensional IC, the substrate thicknesses and thermal conductivities, as well as the number, cross sectional areas, lengths, arrangement, and thermal conductivities of said integrated heat sinks, are selected so as to ensure that the temperature in any region of the three-dimensional monolithic IC would not exceed a preset tolerable operation temperature determined for preliminarily established intensities of the said heat-generating elements and their known positions in the three-dimensional monolithic IC. Thus, in this preferred embodiment of the disclosed invention, thermal fluxes from the heat sources first spread over heat-conducting substrates, then enter into integrated heat sinks, and are eventually dissipated in the heat sink. The arrangement of integrated heat sinks in the monolithic structure should provide heat removal from functional heat-generating elements. The arrangement of integrated heat sinks depends on a position and thermal power of functional heat-generating elements in the three-dimensional monolithic IC. Said arrangement is characterized by number of integrated heat sinks, which environ each of said functional heat-generating elements, and by average distance between said integrated heat sinks and said functional heat-generating element. For this purpose the integrated heat sinks are positioned adjacent to the functional heat-generating elements. The more thermal power of functional heat-generating element, the more said number and less said distance. Thus, said number of integrated heat sinks, located around of everyone functional heat-generating element, and average distance between said integrated heat sinks and said functional heat-generating element are selected so as to ensure that the temperature in any region of the three-dimensional monolithic integrated circuit would not exceed a preset tolerable operation temperature.

[0082] In order to provide for the effective heat removal from said monolithic three-dimensional IC the thermal contacts of heat-conducting substrates with integrated heat sinks, as well as the thermal contacts of these integrated heat sinks with the heat sink, possess low thermal resistances. This is achieved through the formation of integrated heat sinks by the known technological means immediately on the heat sink, which provides for a low thermal resistance of the thermal contacts between the integrated heat sinks and the heat sink. The integrated heat sinks are created stage by stage in the course of formation of adjacent IC units of said multilayer structure. According to this, known technological methods are used to open windows after the formation of a sequential layer and to fill these windows with a selected heat-conducting material which forms a part of the integrated heat sink. Then, the next layer of said multilayer structure is formed and the windows, matched to those in the preceding layer, are opened and filled with the heat-conducting material to obtain the corresponding part of the integrated heat sink. This cycle is repeated in each stage of assembly of the multilayer structure. As a result, a system of integrated heat sinks penetrating into the said monolithic

three-dimensional IC structure is formed. The disclosed method of forming integrated heat sinks allows thermal contacts with low thermal resistances to be obtained.

[0083] In one variant of the disclosed monolithic three-dimensional IC, at least one functional heat-generating element represents a semiconductor thin-film transistor. Said transistor includes a semiconductor layer, an insulating layer, and electrode layers (source, drain, and gate). These layers can be made of both organic and inorganic materials. In another variant of the disclosed monolithic three-dimensional IC, at least one functional heat-generating element represents a semiconductor diode comprising a semiconductor layer and electrode (cathode and anode) layers. In still another variant of the disclosed monolithic three-dimensional IC, at least one functional heat-generating element represents a thin-film resistor.

[0084] In a possible variant of the disclosed monolithic three-dimensional IC, at least one integrated heat sink is made of Al_2O_3 based ceramics.

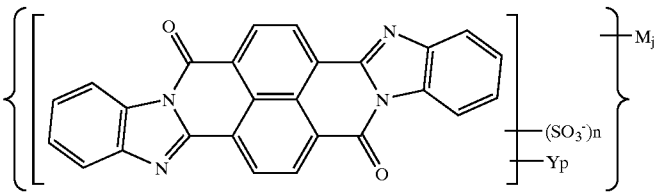
[0085] In one embodiment of the disclosed monolithic three-dimensional IC, at least one integrated heat sink has the shape of the cross section parallel to the front surface of said substrate selected from the list comprising circle, ellipse, square, rectangle, polygon, or any combination thereof. In another possible embodiment, at least one substrate of at least one unit integrated circuit further comprises at least one conducting element. Said conducting element is formed penetrating said substrate and contacting with wiring pattern (topology) arranged on the front surface of said substrate. In still another possible variant, the disclosed monolithic three-dimensional IC contains at least one electrically conducting element situated between two adjacent substrates. This element connects the wiring pattern of a discrete IC arranged on the front surface of one substrate to the wiring pattern of a discrete IC arranged on the front surface of another substrate. In a possible variant of the monolithic three-dimensional IC, at least one planarization layer is made of a thermoelastic material. Such materials are capable of passing to a liquid (flowable) state in a certain temperature interval. In this state, the surface of said thermoelastic material becomes flat.

[0086] In another embodiment, the present invention provides the three-dimensional integrated circuit having the discrete integrated circuits or the monolithic three-dimensional IC, which contain at least one functional element such as TFT made using a semiconductor thin crystal film (SCTCF). The SCTCFs are formed by rodlike supramolecules composed of at least one organic compound with conjugated π-system, wherein a crystal structure of the film has an intermolecular spacing of 3.4±0.3 Å in the direction of at least one crystal axis. This semiconductor thin crystal film (SCTCF) is based on an aromatic polycyclic compound and has the electron-hole type of conductivity. A condition is the presence of a developed system of π-conjugated bonds between conjugated aromatic rings of the molecules and the presence of groups (such as amine, phenol, ketone, etc.) lying in the plane of the molecule and involved into the aromatic system of bonds. The molecules and/or their molecular fragments possess a planar structure and are capable of forming supramolecules in solutions. Another condition is the maximum overlap of π-orbitals in the stacks of supramolecules.

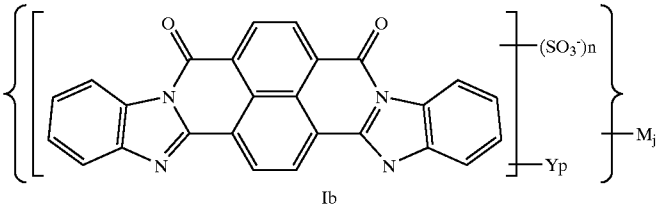
[0087] Aromatic compounds suitable for the obtaining of SCTCFs are characterized by the general formula $\{R\}\{F\}_n$, where R is a polycyclic core featuring a π-electron system, F is a modifying functional group ensuring solubility of a given compound in nonpolar or polar solvents (including aqueous media), and n is the number of functional groups.

[0088] In particular, these organic compounds include the following:

[0089] sulfoderivatives of perynone dyes with the general structural formula from the group consisting of structures I-XVII:

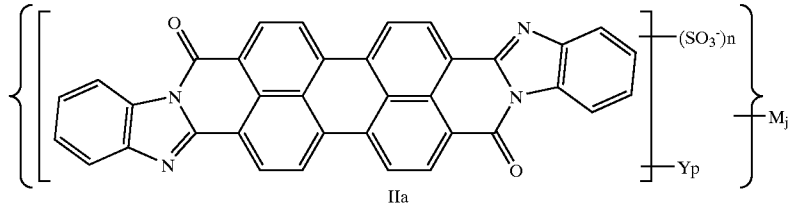


Ia

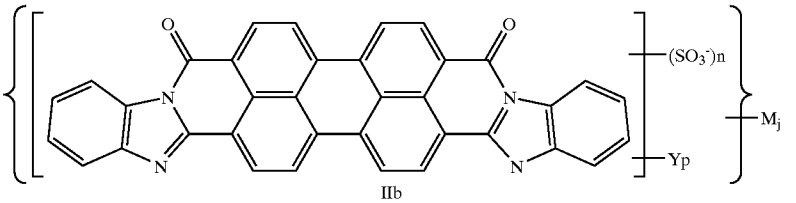


Ib

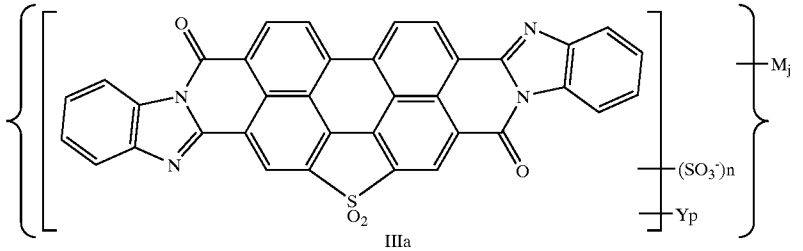
-continued



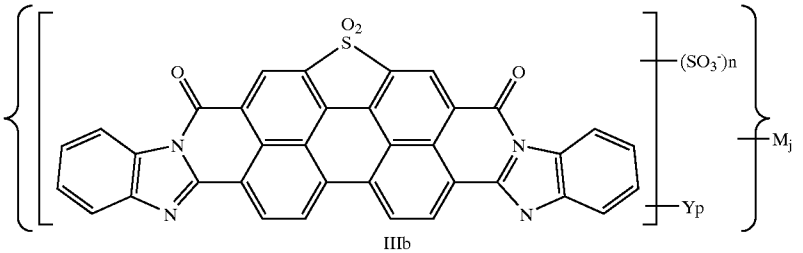
IIa



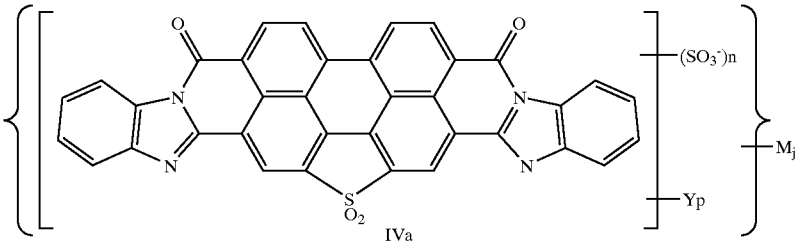
IIb



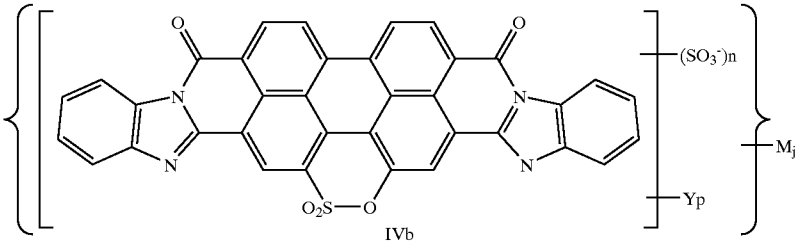
IIIa



IIIb

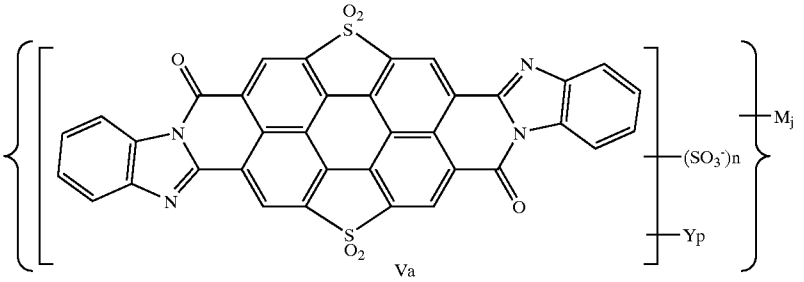


IVa

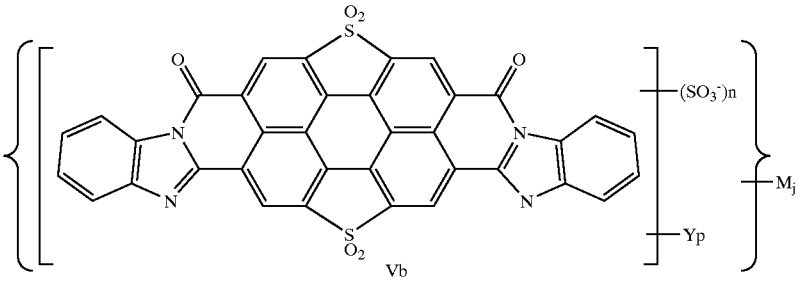


IVb

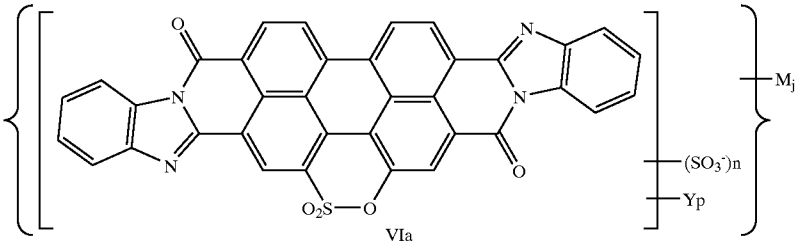
-continued



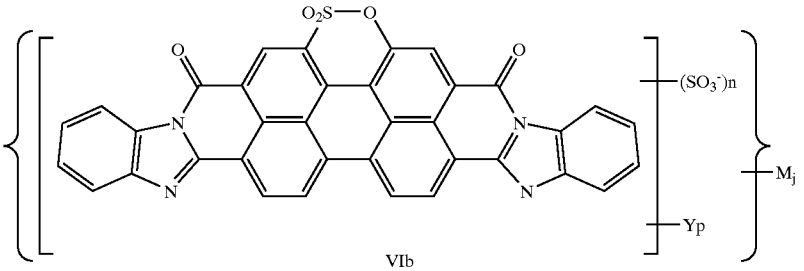
Va



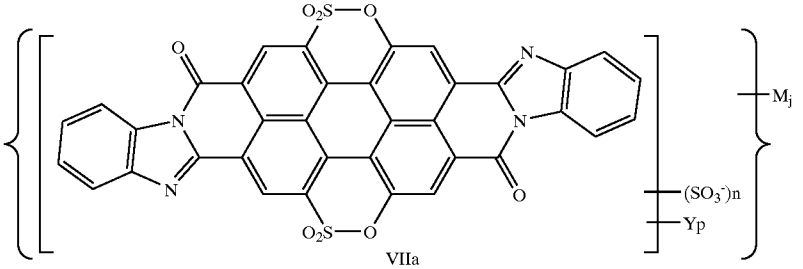
Vb



VIa

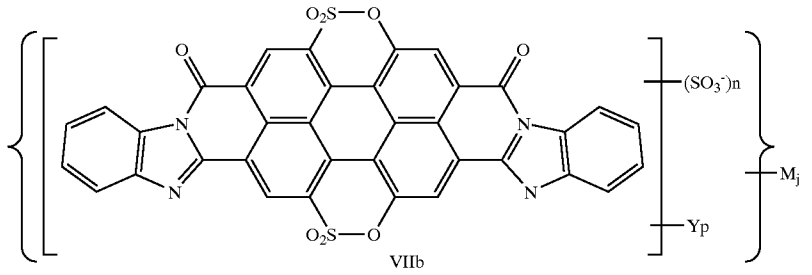


VIb

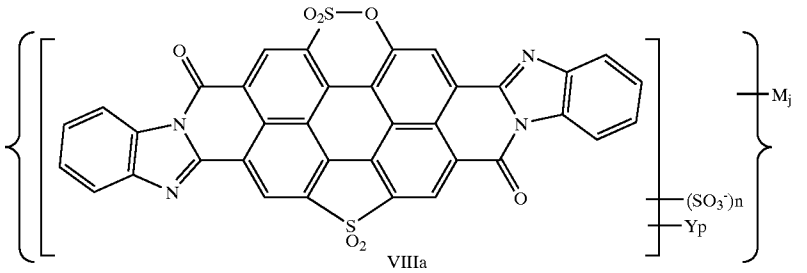


VIIa

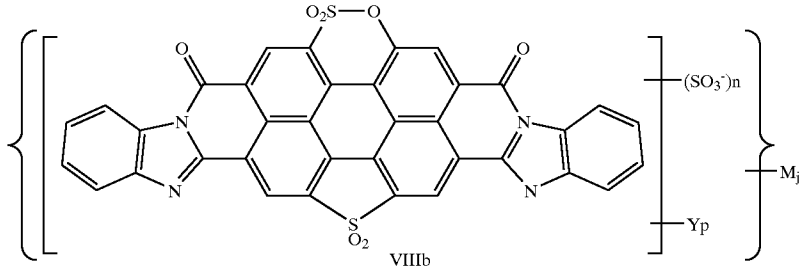
-continued



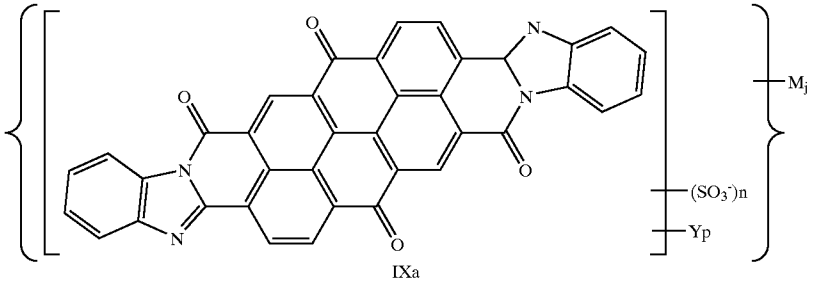
VIIb



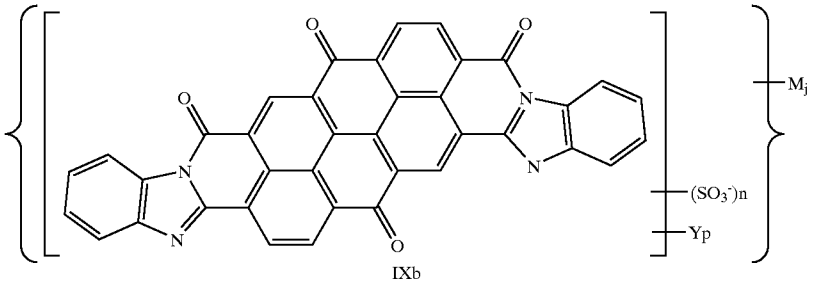
VIIIa



VIIIb

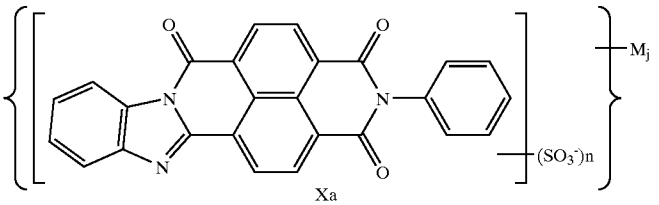


IXa

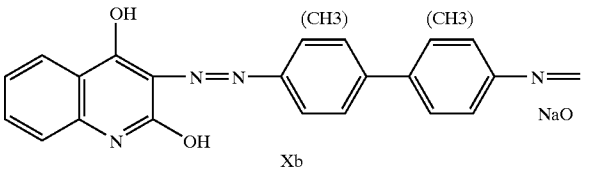


IXb

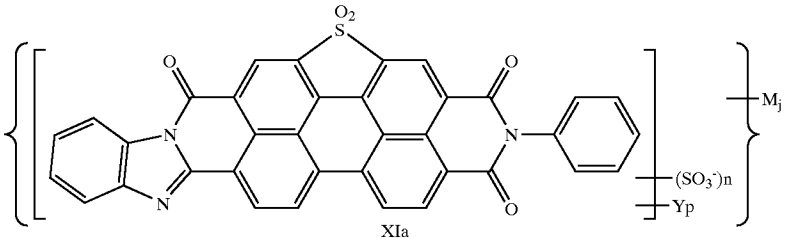
-continued



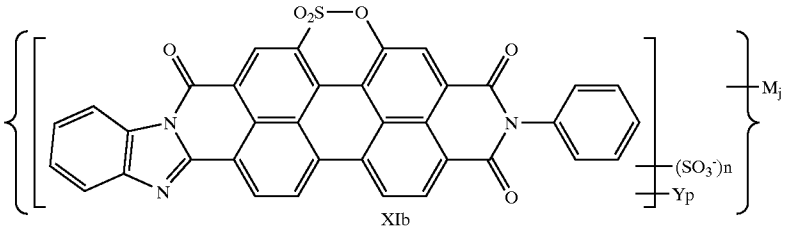
Xa



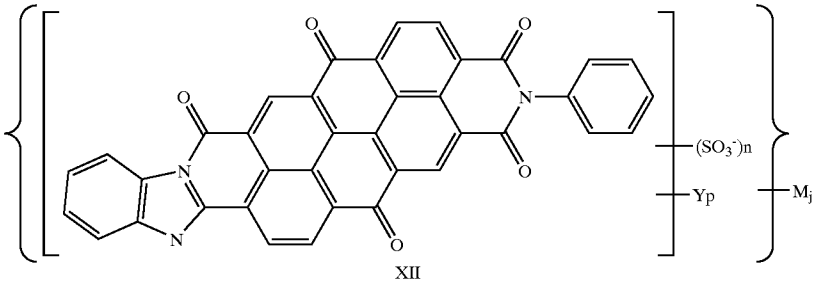
Xb



XIa

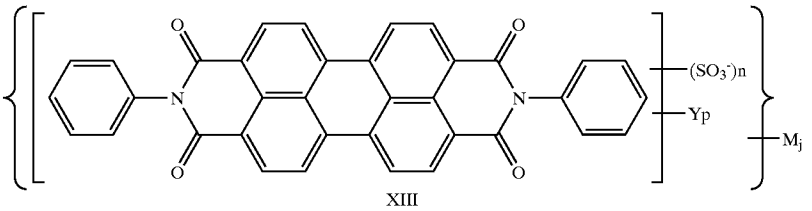


XIb

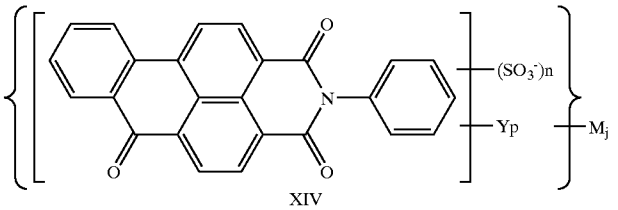


XII

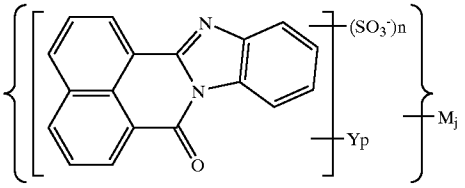
-continued



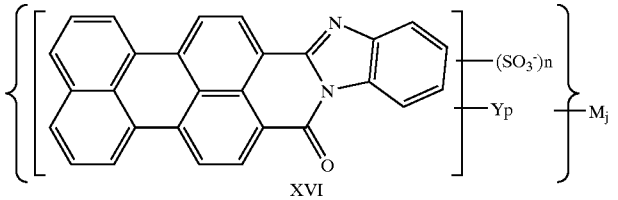
XIII



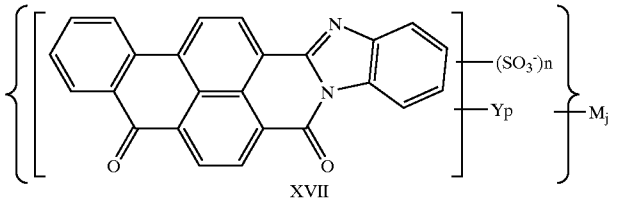
XIV



XV



XVI

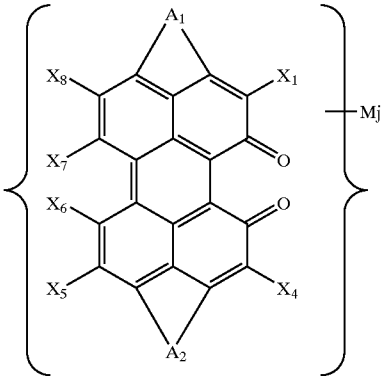


XVII

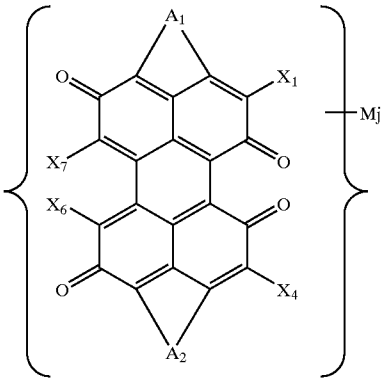
[0090] where n is an integer in the range of 1 to 4 and p is an integer in the range of 0 to 6; Y is individually selected from the group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2 and NH_2; M is a counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved;

[0091] sulfoderivatives of heteroaromatic polycycloquinones with the general structural formulas XVIIIa-XVIIId:

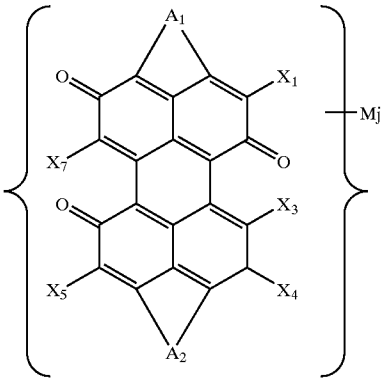
XVIIIa



XVIIIb

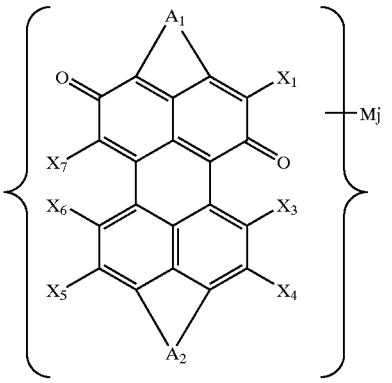


XVIIIc

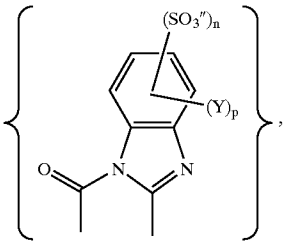


-continued

XVIIId



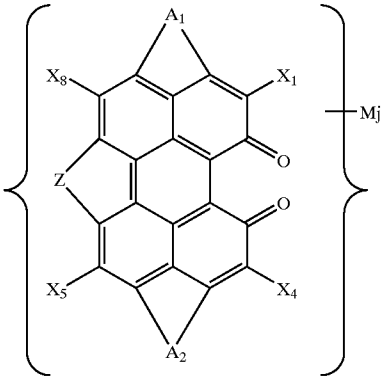
[0092] where A_1 и A_2 are fragments of the general structural formula



[0093] $X_1, X_3, X_4, X_5, X_6, X_7, X_8$ are substituents from the group including H, OH, SO_3H, such that at least one of these substituents is different from H; Y is a substituent from the series H, Cl, F, Br, Alk, OH, OAlk, NO_2, NH_2 and p is an integer in the range of 0, 1, 2, 3 and 4; n is one of the group including 0, 1, 2, such that at least one of fragments A_1or A_2 comprises at least one sulfogroup; M is counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved;

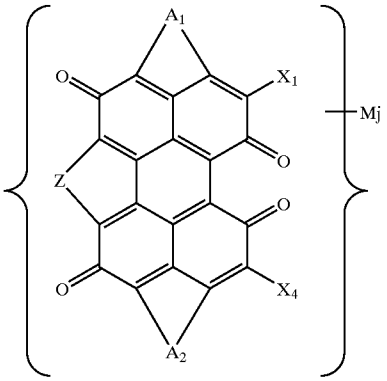
[0094] sulfoderivatives of heteroaromatic polycycloquinones with the general structural formulas from the group XIXa-XIXc:

XIXa

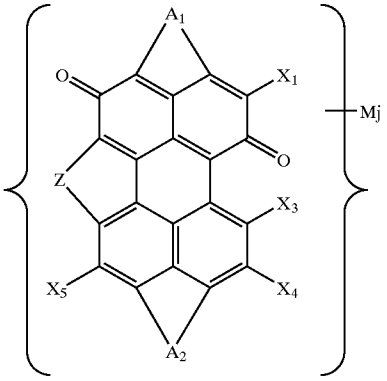


-continued

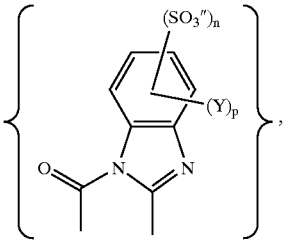
XIXb



XIXc



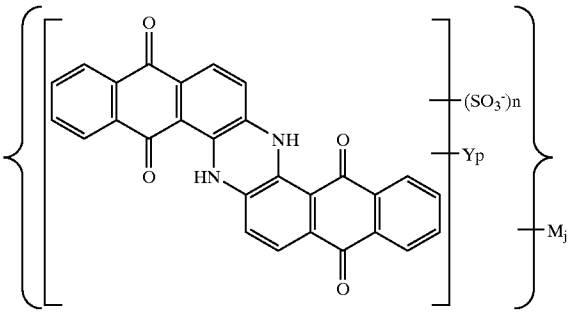
[0095] where A_1 и A_2 are fragments of general structural formula



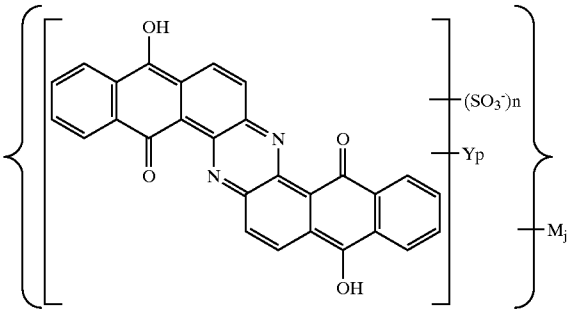
[0096] X_1, X_3, X_4, X_5, X_6, X_7, X_8 are substituents from the group including H, OH, SO_3H; Z is a bridge closing new heterocyclic systems chosen from the series —O—, —SO_2—, —SO_2—O—; Y is a substituent from the series H, Cl, F, Br, Alk, OH, OAlk, NO_2, NH_2 and p is an integer in the range of 0, 1, 2, 3 and 4; n is one of the group including 0, 1, 2, such that at least one of fragments A_1 or A_2 comprises at least one sulfogroup; M is counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved;

[0097] sulfoderivatives of dyes with anthraquinone fragment with the general structural formulas from the group XX-XXIV:

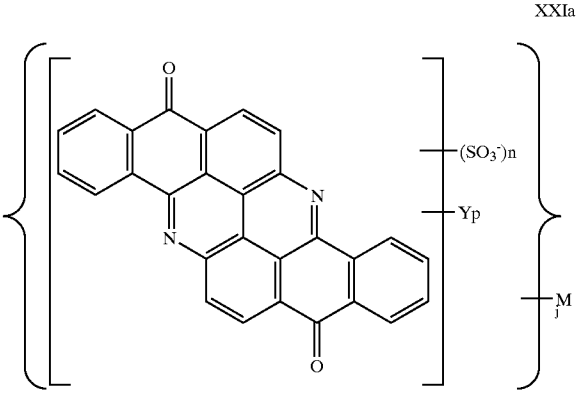
XXA



XXb

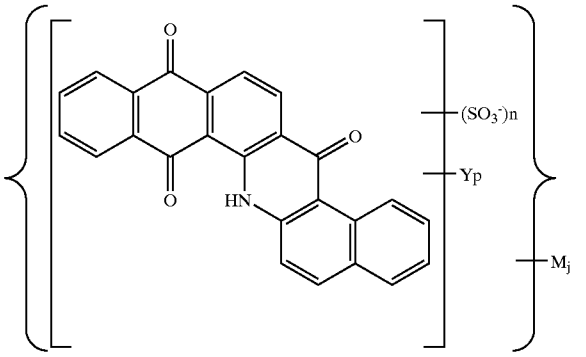


XXIa

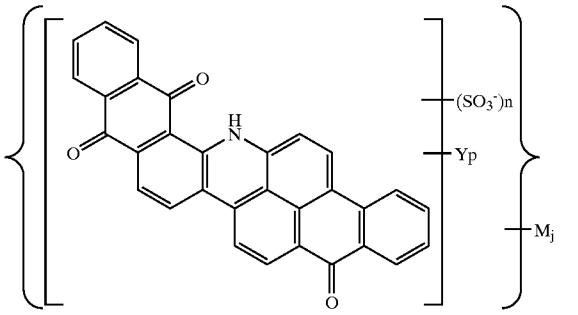


-continued

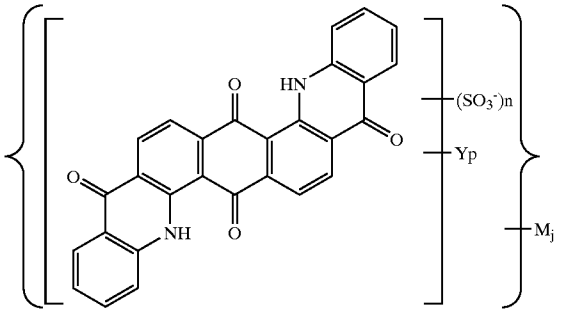
XXIb



XXIIa

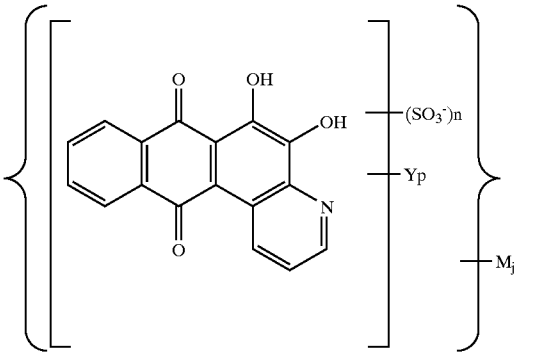


XXIIb

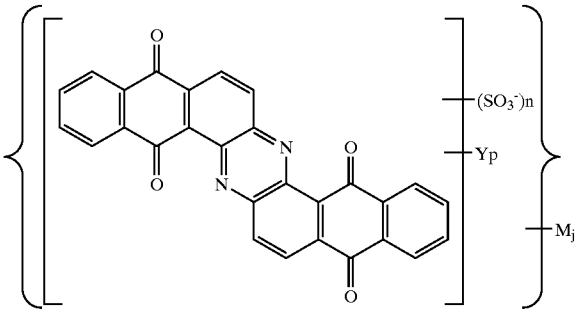


-continued

XXIII

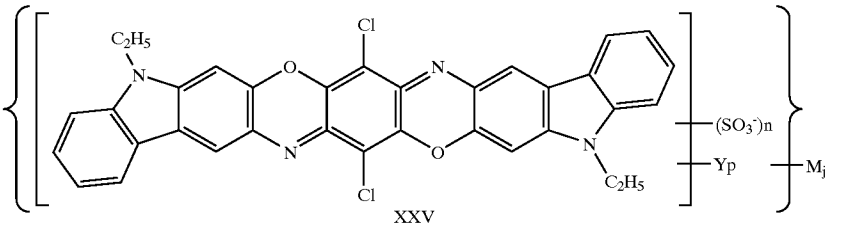


XXIV



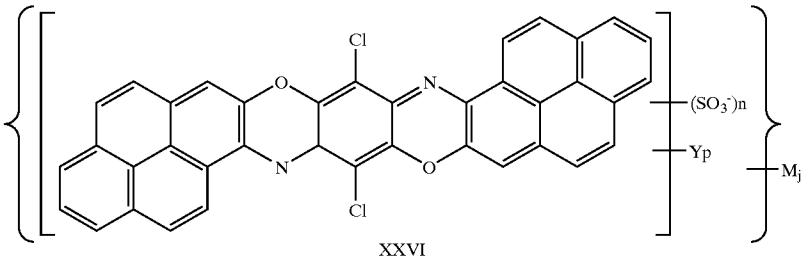
[0098] where n is an integer in the range of 1 to 4 and p is an integer in the range of 0 to 8; Y is individually selected from the group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2 and NH_2; M is a counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved;

[0099] sulfoderivatives of fused polycyclic heteroaromatic compounds comprising five or six members with N or O or both (pyrrole, pyridine, oxazole, furan, oxazine, azine, chromone, pyridopyrimidine) with the structural formulas XXV-XXVIII:

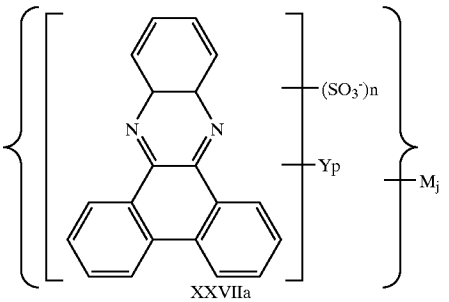


XXV

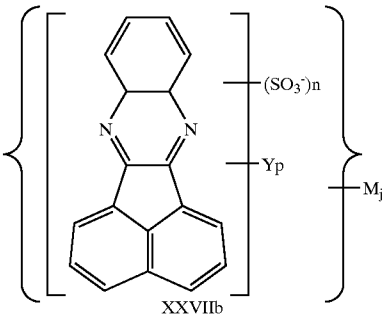
-continued



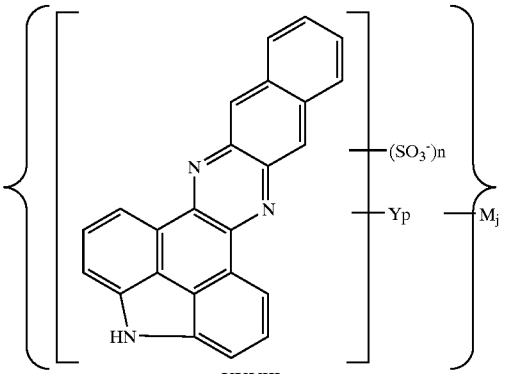
XXVI



XXVIIa



XXVIIb



XXVIII

[0100] where n is an integer in the range of 1 to 4 and p is an integer in the range of 0 to 8; Y is individually selected from the group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2 and NH_2; M is a counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved.

[0101] A low sensitivity of the disclosed monolithic three-dimensional IC with respect to temperature variations is achieved, in particular, due to the fact that said SCTCFs possess higher temperature stability as compared to the conventional materials. Indeed, SCTCFs can be treated at temperatures of up to 700° C. without any significant change in the electrical properties. The ability of the disclosed three-dimensional ICs to retain their working properties at high ambient temperatures allow these ICs to be used in electronic devices intended for steel making industry (melt level sensors), in aerospace technologies (electronic transducers for engine nozzles), and in many other high-temperature applications.

[0102] Another advantage of SCTCFs implemented in the disclosed monolithic three-dimensional ICs consists in the possibility of using printing technology for the creation of functional semiconductor elements of the discrete ICs.

[0103] Said SCTCFs can be obtained by a method, called Cascade Crystallization Process developed by Optiva Technology. The process is further described in detail in P. Lazarev and M. Paukshto, *Proceedings of the* 7th *International Workshop "Displays, Materials and Components"* (Kobe, Japan, Nov. 29-Dec. 1, 2000), pp. 1159-1160. According to this method such an organic compound dissolved in an appropriate solvent forms a colloidal system which is lyotropic liquid crystal solution, in which molecules are aggregated into supramolecules constituting kinetic units of the system. This liquid crystal phase is essentially a precursor of the ordered state of the system, from which a solid anisotropic crystal film is formed in the course of subsequent alignment of the supramolecules and removal of the solvent. The film is also named thin crystal film or TCF.

[0104] A method stipulated for the synthesis of anisotropic semiconducting thin crystal films from a colloidal system with supramolecules includes the following stages:

[0105] (i) application of the aforementioned colloidal system onto a substrate (or onto a device or a layer in a multilayer structure); the colloidal system must possess thixotropic properties, which are provided by maintaining a preset temperature and a certain concentration of the dispersed phase;

[0106] (ii) conversion of the applied colloidal system into a high flow (reduced viscosity) state by any external action (heating, shear straining, etc.) decreasing viscosity of the solution; this action can be either applied during the whole subsequent alignment stage or last for a minimum necessary time, so that the system would not relax into a state with increased viscosity during the alignment stage;

[0107] (iii) external alignment action upon the system, which can be produced using mechanical factors or by any other means; the degree of the external action must be sufficient for the kinetic units of the colloidal system to acquire the necessary orientation and form a structure that would serve as a base of the crystal lattice of the anisotropic thin crystal film;

[0108] (iv) conversion of the aligned region of the layer from the state of reduced viscosity, achieved due to the external action, into the state of the initial or higher viscosity; this transition is performed so as not to cause disorientation of the anisotropic thin crystal film structure and not to produce surface defects;

[0109] (v) final stage of solvent removal (drying), in the course of which the final anisotropic thin crystal film structure is formed; this stage can also include an additional thermal treatment (annealing) characterized by the duration, character, and temperature, which are selected so as to ensure full or at least partial removal of water molecules from said crystal hydrate structure, while retaining the structure of supramolecules and crystalline structure of conjugated aromatic crystalline layer intact.

[0110] In the resulting anisotropic SCTCF, the molecular planes are parallel to each other and the molecules form a three-dimensional crystal structure, at least in a part of the layer. Optimization of the production technology may allow the formation of a single-crystal film.

[0111] The SCTCF thickness usually does not exceed 1 μm. The film thickness can be controlled by changing the content of a solid substance in the applied solution and by varying the applied layer thickness. In order to obtain the films possessing desired optical characteristics, it is possible to use mixed colloidal systems (such mixtures can form joint supramolecules).

[0112] The mixing of said organic compounds in solutions results in the formation of mixed aggregates of variable composition. The analysis of X-ray diffraction patterns for the mixtures allow us to judge about the molecular packing in supramolecules by the presence of a characteristic diffraction peak corresponding to intermolecular spacing in the range from 3.1 to 3.7 Å. In general, this value is common for aromatic compounds in the form of crystals and aggregates. The peak intensity and sharpness increase in the course of drying, however, no changes in the peak position are observed. This diffraction peak corresponds to the intermolecular spacing within aggregates (stacks) and has been observed in the X-ray diffraction patterns of various materials. The mixing is favored by the planar structure of molecules or their fragments and by the coincidence of one molecular dimension in the organic compounds under consideration. In the applied aqueous layer, the organic molecules possess a long-range order in one direction, which is related to the alignment of supramolecules on the substrate surface. As the solvent is evaporated, it is energetically favorable for the molecules to form a three-dimensional crystal structure.

[0113] Thin crystal films obtained by the method described above exhibit electric conductivity of two types: electron, related to the system of π-conjugated bonds in supramolecules, and ionic, related to the ion component of the crystalline film and the presence of free water (solvent). As the water content in the film decreases in the course of drying, the ion component drops; using additional annealing step, this component can be completely eliminated. The electron conductivity component of SCTCFs depends primarily on the length of supramolecules that can be controlled in the course of manufacture. In the presence of an electric field, the free electrons can drift along supramolecules (stacks), while the transitions between stacks are

determined by tunneling effects. Thus, SCTCFs possess a pronounced anisotropy of the electrical properties.

[0114] SCTCFs possess a high degree of optical anisotropy as well. Such films exhibit the properties of E-type polarizers, which are related to peculiarities of the optical absorption of supramolecular complexes, and behave as retarders (al known as phase-shifting films) in the spectral ranges where the absorption is insignificant. The retarding properties of these anisotropic films are related to their birefringence (also known as double refraction) that is, to a difference in refractive indices measured in the direction of application of the LLC solution onto a substrate and in the perpendicular direction. Films formed from the LLC systems based on light-fast organic molecules are characterized by high thermal stability and light resistance.

[0115] **FIG. 9** shows the temperature dependence of a SCTCF sample obtained as described above and measured in the direction perpendicular to the direction of application. As can be seen, the resistance decreases with increasing temperature, which is characteristic of semiconductors. The decrease in the resistance reflects an increase in the density of free charge carriers: the higher the sample temperature, the greater the number of mobile free electrons in the conduction band (for a n-type semiconductor) or mobile holes in the valence band (for a p-type semiconductor).

Experimental Results

EXAMPLE 1

[0116] The method illustrated in **FIGS. 5***a* **-5***d* has been demonstrated using a one centimeter square integrated circuit chip with 41-125 μm solder bumps on 250 μm centers along one edge. This chip was mounted perpendicular to a heat sink. Prior to assembly, the first chip was coated with a bonding layer in the form of a rosin-based flux to provide enough tack to hold the chip in position during the reflow process. The assembly was then reflowed in a nitrogen-filled infrared belt furnace.

EXAMPLE 2

[0117] A thin-film transistor structure with top source and drain contacts was obtained using a silicon wafer with an insulating SiO_2 layer. The wafer was coated with SCTCF, above which the electric contacts were deposited by conventional methods. **FIG. 10** shows a schematic diagram of such an organic TFT structure with top source and drain contacts, comprising a Si wafer **55** that serves as a gate contact, a SiO_2 insulating layer **56**, an SCTCF **57**, and gold source and drain contacts **58**. The procedure of depositing contacts consisted of the following steps: (i) cutting a Si/SiO_2 wafer covered with SCTCF to the required size; (ii) placing a mask (a mechanical mask was glued to the sample surface using Aquaricum silicone gel); (iii) covering the sample surface with gold. The last stage was performed using an NRC/Varian Model 3117 Thermal Evaporator equipped with a TM-350 thickness monitor (MAXTEC Inc.). The device was operated at a working pressure inside the evaporator of 10^{-6}-10^{-7} Torr and an evaporator current of 150 A. The typical contact layer thickness was ~50 nm. All processing steps were visually controlled using a NIKON Eclipse L200 microscope.

[0118] The bottom contacts were made using a photolithographic method. The contact pattern was obtained in a Karl Suss MJB 3 setup. The contacts were deposited in a Temescal VES-2550 electron beam evaporator with an INFICTION IC/5 deposition controller. Covering with Sio_2 layer was performed using an Airco Temescal CV-8 electron beam evaporator with an INFICTION XTC/2 deposition controller. **FIG. 11** shows a schematic diagram of the TFT structure with bottom source and drain contacts comprising a 500 μm thick Si wafer **61** which also served as the gate contact, a 200 nm thick insulating Sio_2 layer **62**, an SCTCF **63**, a 2.5 nm thick titanium layer **64** for better adhesion of gold, 50 nm thick gold source and drain contacts **65**, and a 800 nm thick protecting SiO_2 layer **66**. The contacts were deposited perpendicular and parallel to the film coating direction. The samples with different channel lengths and channel widths are available.

[0119] The above drawings, examples and specification have illustrated typical preferred embodiments of the disclosed invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

What is claimed is:

1. A three-dimensional integrated circuit comprising

(i) a heat sink,

(ii) a set of discrete integrated circuits arranged one above another and mounted on said heat sink, each of said discrete integrated circuits comprising

a heat-conducting substrate, and

functional elements formed on front and/or rear surface of said substrate,

wherein at least one of the functional elements is a heat-generating element, and

(iii) a system of integrated heat sinks being in thermal contact with at least one of said substrates and with the heat sink.

2. The three-dimensional integrated circuit according to claim 1, wherein width, length, thickness and thermal conductivity of the substrate of said discrete integrated circuit, as well as the number, cross sectional area, length, and thermal conductivity of said integrated heat sinks, are selected so as to ensure that temperature in any region of the three-dimensional integrated circuit does not exceed a preset tolerable operation temperature determined for previously established intensities of said functional heat-generating elements and their known positions in the three-dimensional integrated circuit.

3. The three-dimensional integrated circuit as in claim 1 in which the substrate of a bottom discrete integrated circuit is in direct thermal contact with the heat sink.

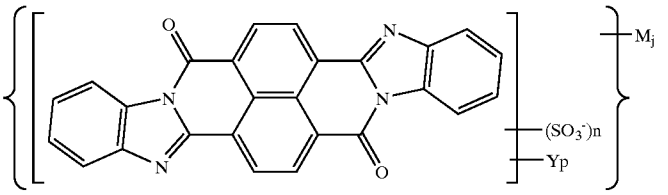
4. The three-dimensional integrated circuit as in claims **1**, wherein at least one said substrate is an Al_2O_3 based ceramic material.

5. The three-dimensional integrated circuit as in claim 1, wherein at least one functional element is comprises a semiconductor thin crystal film formed by rodlike supramolecules composed of at least one organic compound with conjugated π-system, wherein a crystal structure of the film

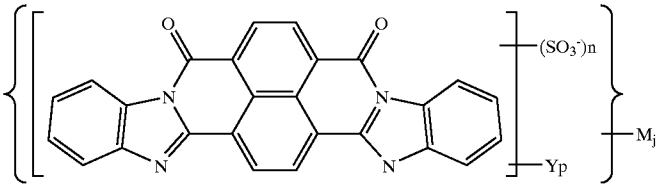
has an intermolecular spacing of 3.4±0.3 Å in the direction of at least one crystal axis.

6. The three-dimensional integrated circuit according to claim 5, wherein said organic compound is a polycyclic organic compound comprising at least one component of the general structural formula $\{R\}\{F\}_n$, where R is a polycyclic core with conjugated π-system, F are modifying functional groups, and n is the number of functional groups.

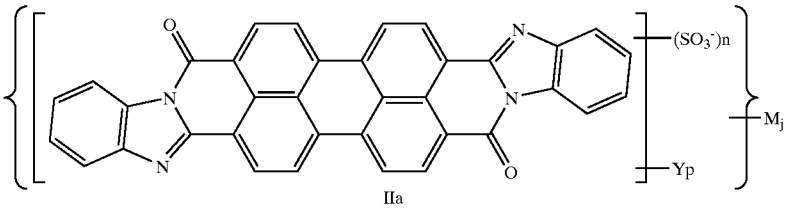
7. The three-dimensional integrated circuit according to claim 6, wherein said polycyclic organic compound is a sulfoderivative of a perynone dye of the general structural formula from the group consisting of structures I-XVII:



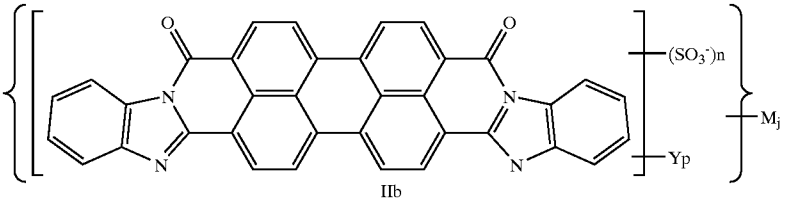
Ia



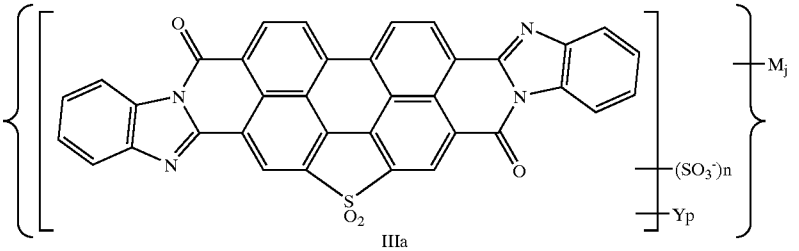
Ib



IIa

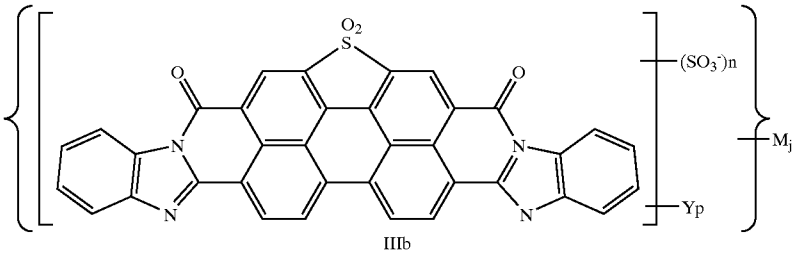


IIb

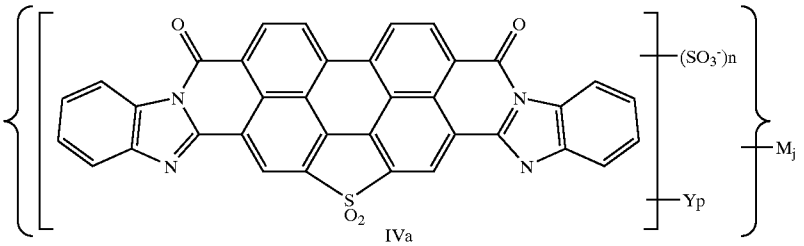


IIIa

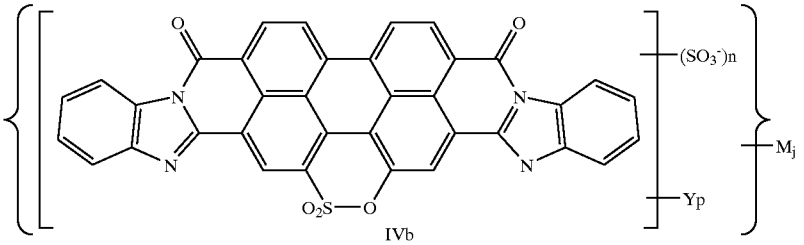
-continued



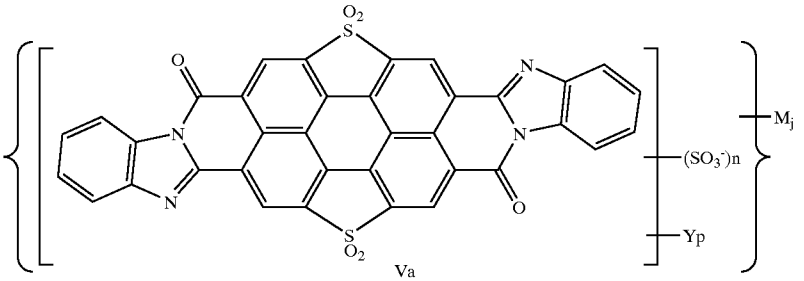
IIIb



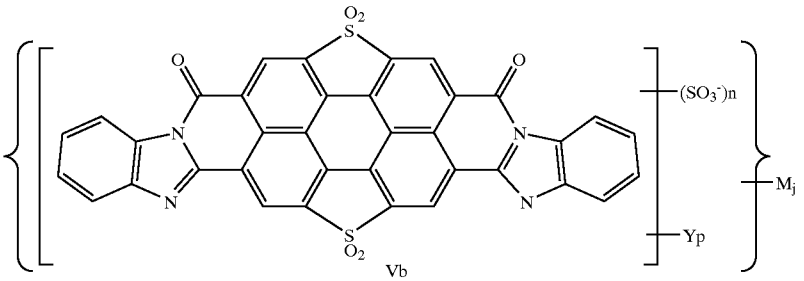
IVa



IVb

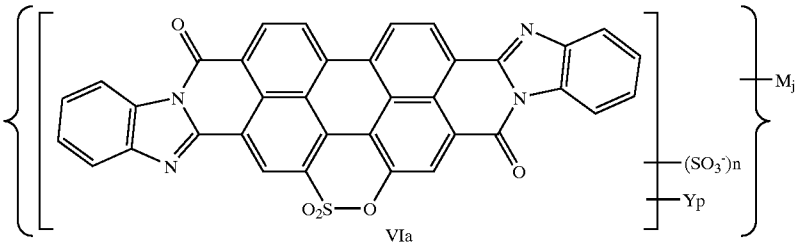


Va

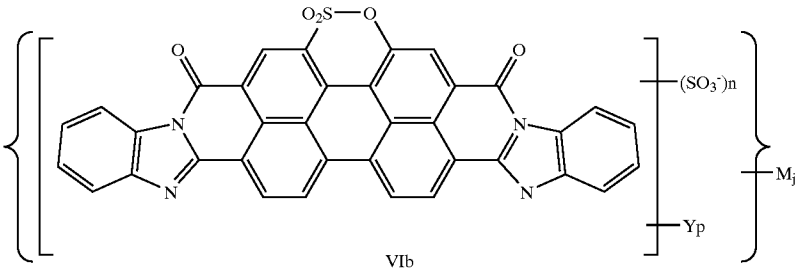


Vb

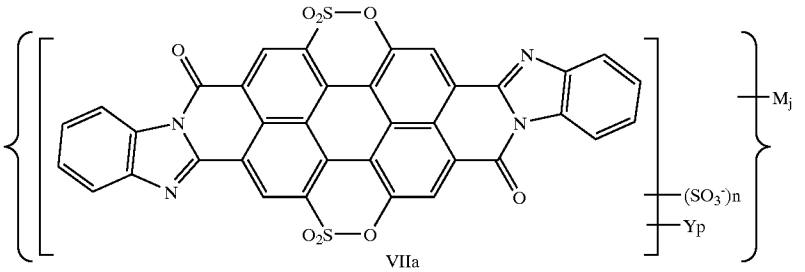
-continued



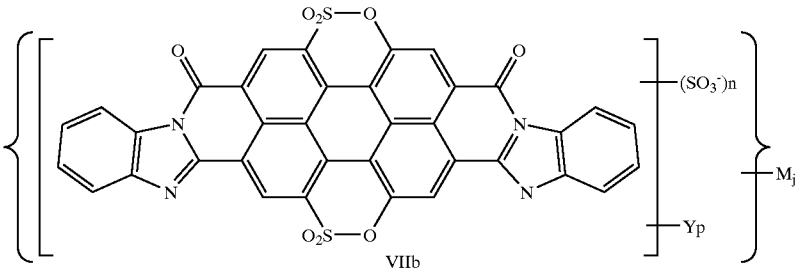
VIa



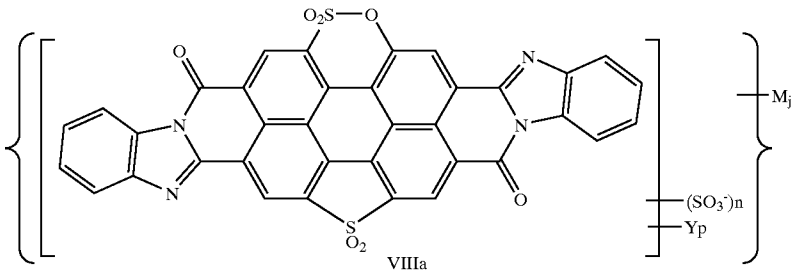
VIb



VIIa

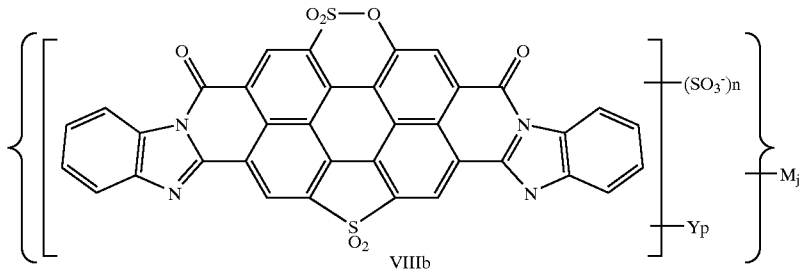


VIIb

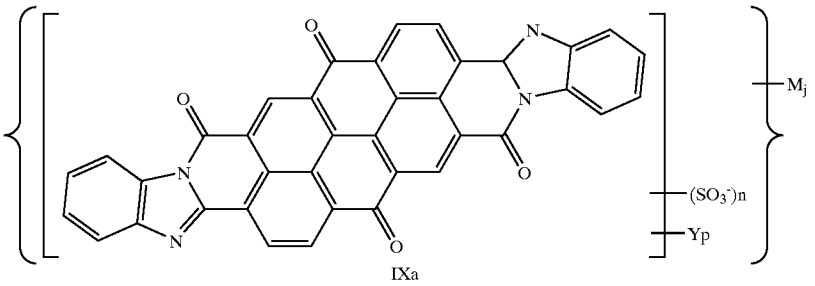


VIIIa

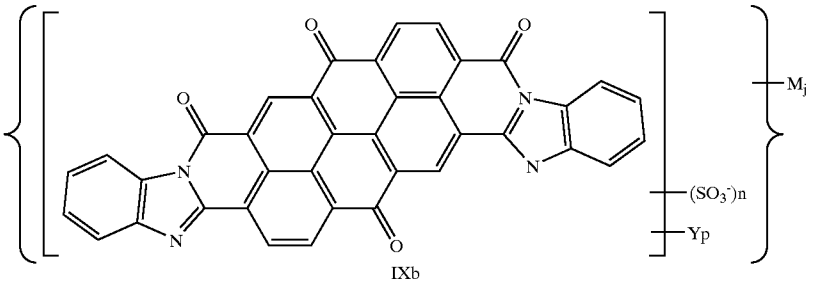
-continued



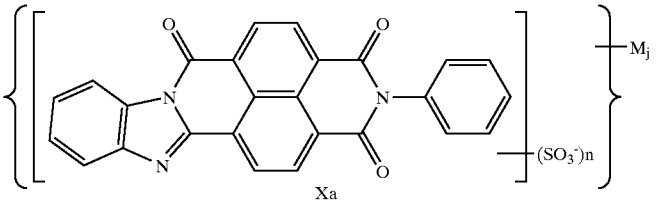
VIIIb



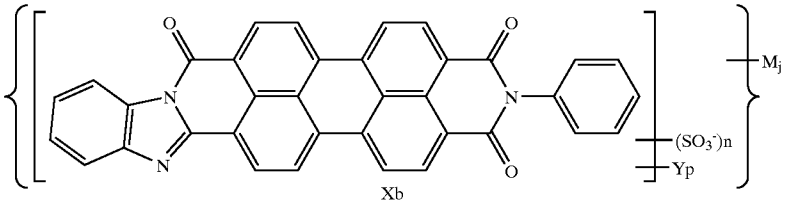
IXa



IXb

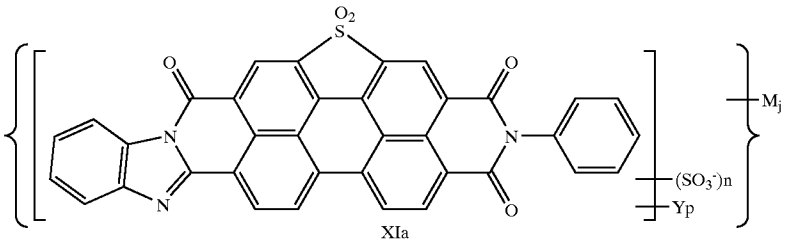


Xa

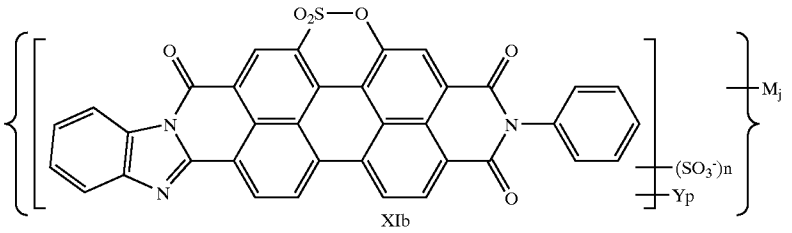


Xb

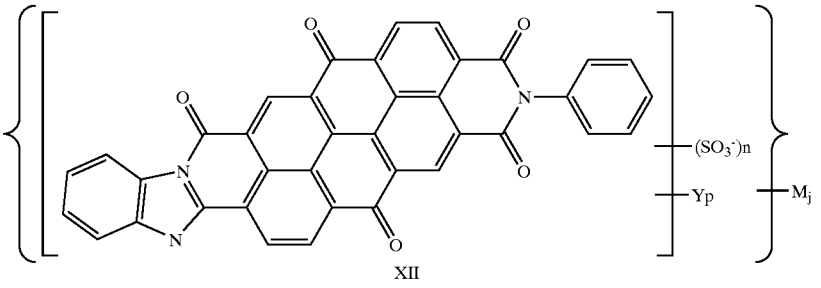
-continued



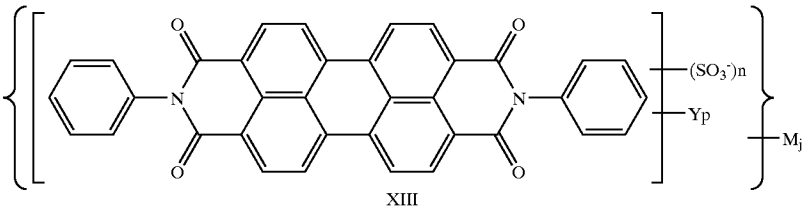
XIa



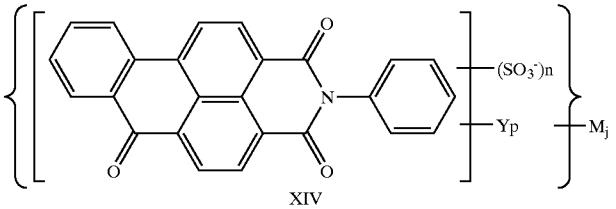
XIb



XII

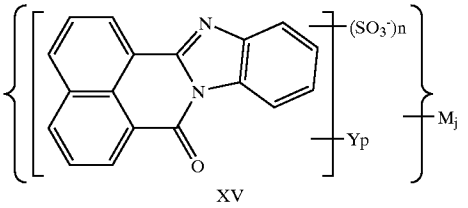


XIII

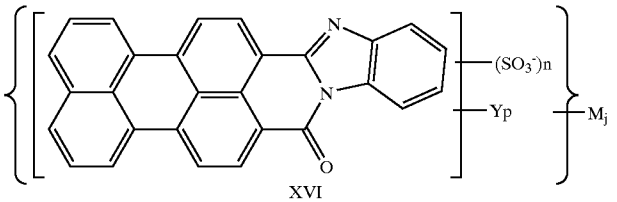


XIV

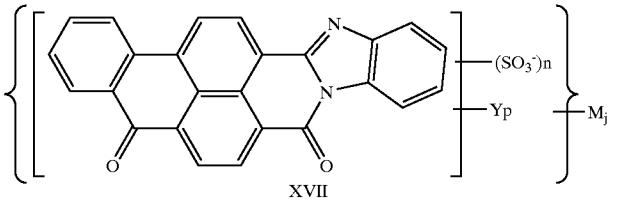
-continued



XV



XVI

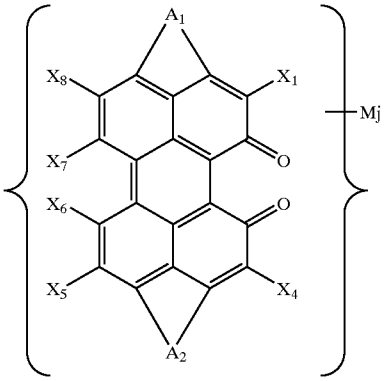


XVII

where n is an integer in the range of 1 to 4, p is an integer in the range of 0 to 6; Y is individually selected from the group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2 and NH_2; M is a counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved.

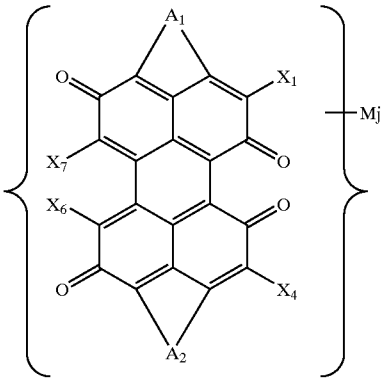
8. The three-dimensional integrated circuit according to claim 6, wherein said polycyclic organic compound is a sulfoderivative of a heteroaromatic polycycloquinone of the general structural formula from the group XVIIIa-XVIIId:

XVIIIa

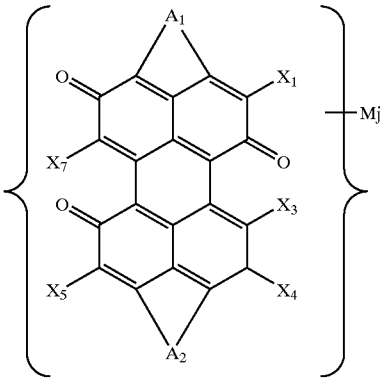


-continued

XVIIIb

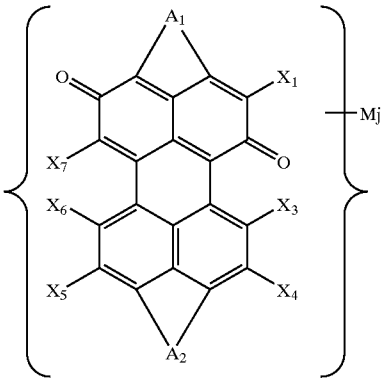


XVIIIc

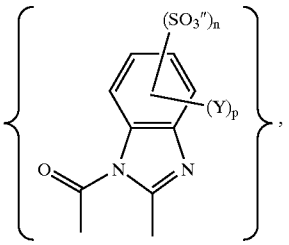


-continued

XVIIId



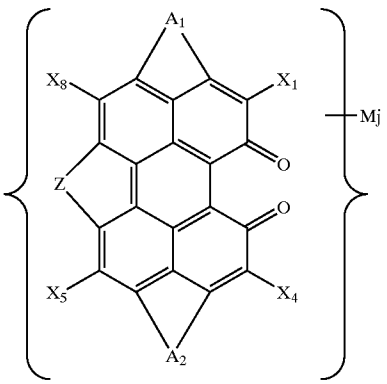
where A_1 и A_2 are fragments of the general structural formula



X_1, X_3, X_4, X_5, X_6, X_7, X_8 are substituents from the group consisting of H, OH, SO_3H, such that at least one of these substituents is different from H; Y is a substituent from the group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2, NH_2; p is an integer in the range of 0, 1, 2, 3 and 4; n is an integer of the group including 0, 1, 2, such that at least one of fragments A_1 or A_2 comprises at least one sulfogroup; M is counterion; and j is the number of counterions in the molecule, which can be fractional if the counterion belongs to several molecules; for n>1, different counterions M can be involved.

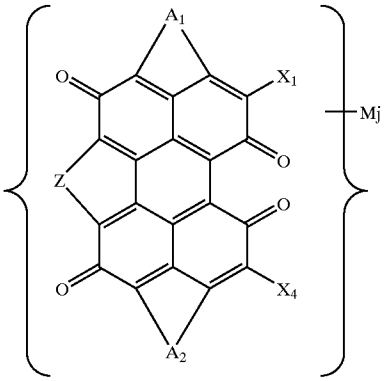
9. A three-dimensional integrated circuit according to claim 6, wherein the polycyclic organic compound is a sulfoderivative of a heteroaromatic polycycloquinone of the general structural formula from the group XIXa-XIXc:

XIXa

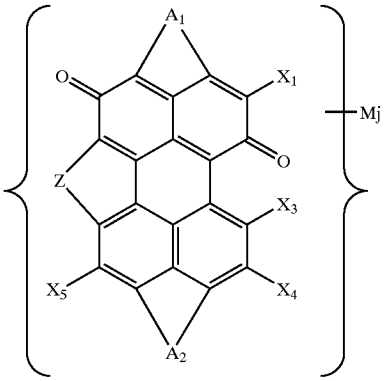


-continued

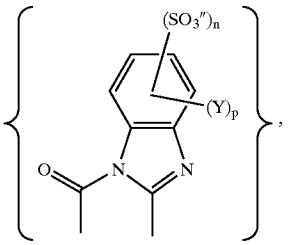
XIXb



XIXc



where A_1 и A_2 are fragments of the general structural formula

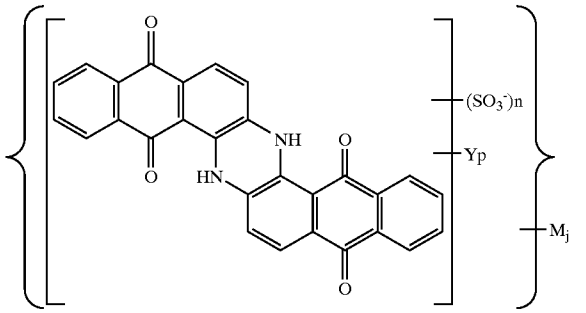


X_1, X_3, X_4, X_5, X_6, X_7, X_8 are substituents from the group consisting of H, OH, SO_3H, and Z is bridge forming new heterocyclic systems, said bridge is chosen from the series —O—, —SO_2—, —SO_2—O—; Y is a substituent from the series H, Cl, F, Br, Alk, OH, OAlk, NO2, NH2; p is an integer in the range of 0, 1, 2, 3 and 4; n is one of the group including 0, 1, 2, such that at least one of fragments A_1 or A_2 comprises at least one sulfogroup; M is counterion; and j is the number of counterions in the molecule, which can be fractional if the counterion belongs to several molecules; for n>1, different counterions M can be involved.

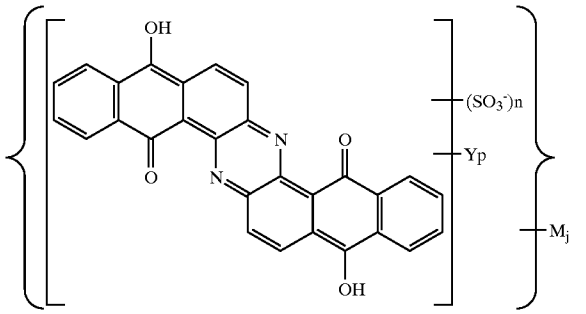
10. A three-dimensional integrated circuit according to claim 6, wherein said polycyclic organic compound is a sulfoderivative of dyes comprising anthraquinone fragment of the general structural formula from the group XX-XXIV:

-continued

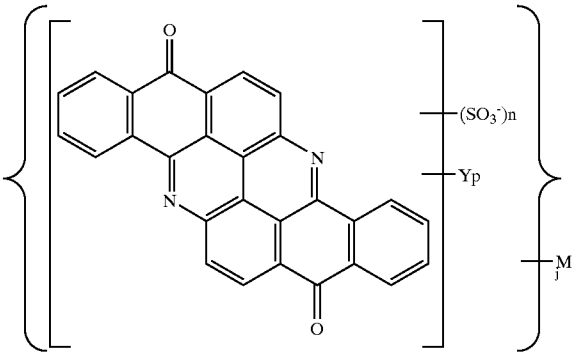
XXA



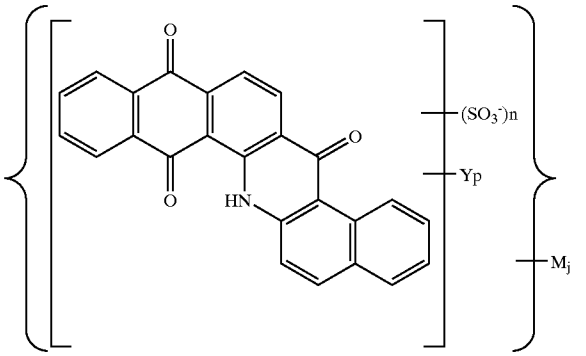
XXb



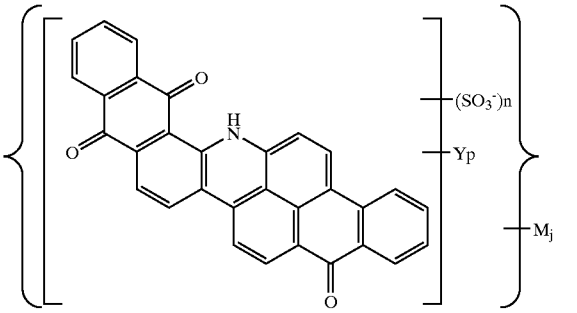
XXIa



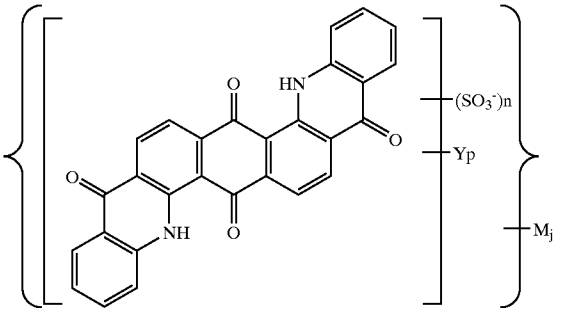
XXIb



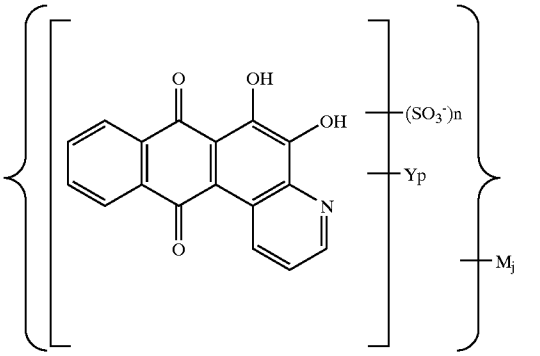
XXIIa



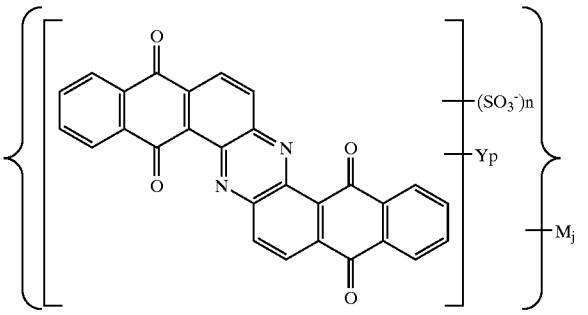
XXIIb



XXIII



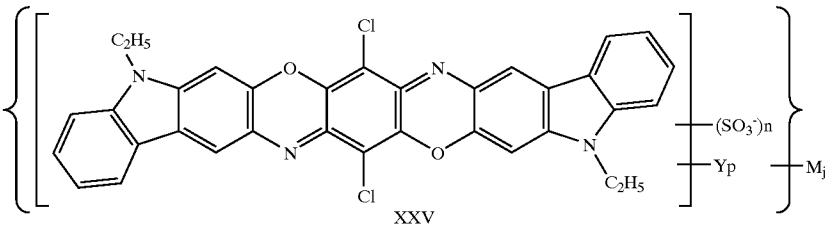
XXIV



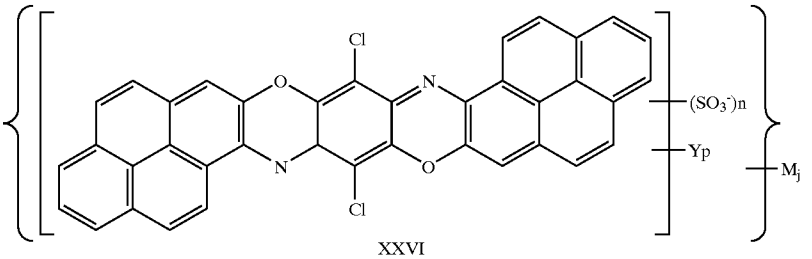
where n is an integer in the range of 1 to 4, p is an integer in the range of 0 to 8; Y is individually selected from the

group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2 and NH_2; M is a counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved.

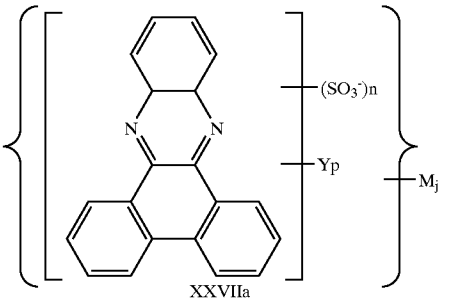
11. A The three-dimensional integrated circuit according to claim 6, wherein said organic compound is a sulfoderivative of fused polycyclic heteroaromatic compound comprising 5 or 6-membered rings with N or O or both: pyrrole, pyridine, oxazole, furan, oxazine, azine, chromone, pyridopyrimidine of the general structural formula from the group XXV-XXVIII:



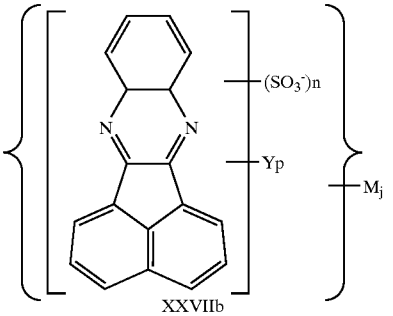
XXV



XXVI

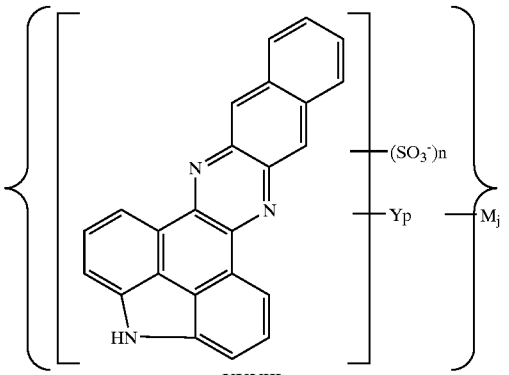


XXVIIa



XXVIIb

-continued



XXVIII

where n is an integer in the range of 1 to 4, p is an integer in the range of 0 to 8; Y is individually selected from the group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2 and NH_2; M is a counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved.

12. A three-dimensional integrated circuit according to claim 1, wherein at least one said functional heat-generating element is a semiconductor thin film transistor.

13. A three-dimensional integrated circuit according to claim 1, wherein at least one said functional heat-generating element is a semiconductor diode.

14. A three-dimensional integrated circuit according to claim 1, wherein at least one said functional heat-generating element is a thin film resistor.

15. A three-dimensional integrated circuit according to claim 1, wherein at least one said integrated heat sink is made of an Al_2O_3 based ceramic material.

16. A three-dimensional integrated circuit according to claim 1, wherein said integrated heat sink has a front surface facing said discrete integrated circuits and an edge face facing the heat sink, said integrated heat sink having a cross-sectional shape selected from the group consisting of circle, ellipse, square, rectangle, or polygon, or any combination thereof.

17. A three-dimensional integrated circuit according to claim 16, further comprising at least one bonding layer made of a heat-conducting adhesive material and located between the front surface at least of one of said integrated heat sinks and the edge face at least of one of said substrates.

18. A three-dimensional integrated circuit according to claim 16, further comprising at least one set of arched solder joints forming thermal contacts between the front surface of at least one of said integrated heat sinks and at least one surface of at least one of said substrates.

19. A three-dimensional integrated circuit according to claim 18, wherein said arched solder joints have nonuniform cross sections along their lengths.

20. A three-dimensional integrated circuit according to claims **18**, further comprising at least two rows of pads, wherein first row of pads is positioned on said integrated heat sink and second row of pads on said substrate adjacent to the first row of pads and arranged along the edge face of said substrate, said pads in at least one of the rows having elongated pad extensions which are narrower than the pads, and said set of arched solder joints connects said pads of the first row with the pads of the second row.

21. A three-dimensional integrated circuit according to claim 16, further comprising at least one bonding layer made of a heat-conducting adhesive material and located between said heat sink and the edge face at least of one of said integrated heat sinks.

22. A three-dimensional integrated circuit according to claims **1**, wherein at least one said discrete integrated circuit further comprising a conducting wiring pattern formed on the front and the rear substrate surfaces, a front protective dielectric layer covering the wiring pattern and the functional elements situated on the front surface of the substrate, and a rear protective dielectric layer covering the wiring pattern and the functional elements situated on the rear surface of the substrate.

23. A three-dimensional integrated circuit according to claim 22, wherein the discrete integrated circuit further comprises at least one front contact pad, situated on said front protective dielectric layer, and at least one electrically conducting element penetrating through said front protective dielectric layer and through the substrate so as to connect the wiring pattern of the rear surface of said substrate to said front contact pad.

24. A three-dimensional integrated circuit according to claim 22, wherein the discrete integrated circuit further comprises at least one rear contact pad, situated on said rear protective dielectric layer, and at least one electrically con-

ducting element penetrating through said rear protective dielectric layer and through the substrate so as to connect the wiring pattern of the front surface of said substrate to said rear contact pads.

25. A three-dimensional integrated circuit according to claim 22, wherein the discrete integrated circuit further comprises at least one front contact pad situated on said front protective dielectric layer, at least one rear contact pad situated on said rear protective dielectric layer, and at least one electrically conducting element penetrating through the front protective dielectric layer, the substrate, and the rear protective dielectric layer so as to connect said front contact pad to said rear contact pad.

26. A three-dimensional integrated circuit according to claims **1**, wherein at least one said discrete integrated circuit further comprising a conducting wiring pattern and the functional elements formed at least on the front substrate surface, a front protective dielectric layer covering said wiring pattern and the functional elements connected to the said wiring pattern, at least one front contact pad situated on said front protective dielectric layer, and at least one electrically conducting element penetrating through said front protective dielectric layer and which connects the wiring pattern to said front contact pad.

27. A three-dimensional integrated circuit according to claims **1**, wherein at least one said discrete integrated circuit further comprising a conducting wiring pattern formed at least on the rear substrate surface, a rear protective dielectric layer covering said wiring pattern and the functional elements connected to said wiring pattern, at least one rear contact pad, situated on said rear protective dielectric layer, and at least one electrically conducting element penetrating through said rear protective dielectric layer, which connects the wiring pattern to said rear contact pad.

28. A three-dimensional integrated circuit according to claim 1, comprising at least two discrete integrated circuits, wherein at least said two discrete integrated circuits adjacent to each other are formed so that a first said discrete integrated circuit further comprises a conducting wiring pattern at least on the front substrate surface, and adjacent to the first one a second discrete integrated circuit positioned above the first circuit further comprises a conducting wiring pattern at least on the rear substrate surface.

29. A three-dimensional integrated circuit according to claim 28, further comprising a first protective dielectric layer covering the conducting wiring pattern on the first discrete integrated circuit and the functional elements of the first discrete integrated circuit, at least one front contact pad situated on said first protective dielectric layer, a second protective dielectric layer covering the conducting wiring pattern on the first discrete integrated circuit and the functional elements of the second discrete integrated circuit, at least one rear contact pad situated on said second protective dielectric layer, and at least one electrically conducting element which connects said rear contact pad with said front contact pad.

30. A monolithic three-dimensional integrated circuit comprising:

(i) a heat sink, and

(ii) a monolithic multilayer structure comprising

stacked unit integrated circuits, wherein each of said unit integrated circuits comprises a heat-conducting substrate having a front surface and a rear surface facing the heat sink,

a conducting wiring pattern formed on the front substrate surface,

functional elements mounted on the front substrate surface and connected to the wiring pattern,

wherein at least one of the functional elements is a heat-generating element,

a protective dielectric layer formed above said wiring pattern and said functional elements, and

a planarization layer formed above the protective layer,

wherein the monolithic multilayer structure is mounted on said heat sink, and

(iii) a system of integrated heat sinks,

wherein each integrated heat sink is in thermal contact with said heat sink and penetrate into the monolithic multilayer structure providing thermal contact with at least one said substrate of the stacked unit integrated circuits.

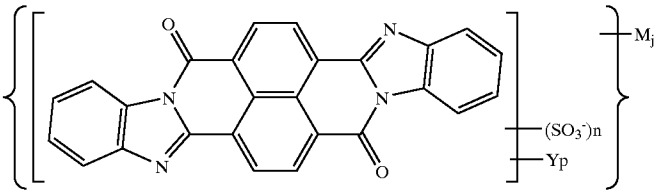
31. A monolithic three-dimensional integrated circuit according to claim 30, wherein thickness and thermal conductivity of said substrate, and number, cross sectional area, length, arrangement, and thermal conductivity of said integrated heat sinks, are selected so as to ensure that temperature in any region of the three-dimensional monolithic integrated circuit will not exceed a preset tolerable operation temperature determined for preliminarily established intensities of said functional heat-generating elements and their known positions in the three-dimensional monolithic integrated circuit.

32. A monolithic three-dimensional integrated circuit according to claims **30** or **31**, wherein at least one said substrate is made of an Al_2O_3 based ceramic material.

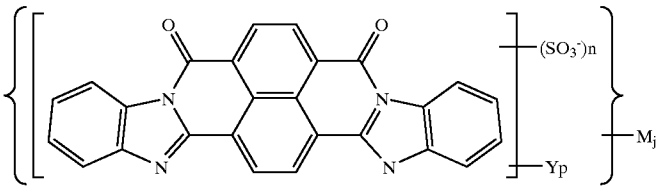
33. A monolithic three-dimensional integrated circuit according to claims **30** or **31**, wherein at least one functional element is made of a semiconducting thin crystal film formed by rodlike supramolecules composed of at least one organic compound with conjugated π-system, wherein a crystal structure of the film has an intermolecular spacing of 3.4±0.3 Å in the direction of at least one crystal axis.

34. A monolithic three-dimensional integrated circuit according to claim 33, wherein said organic compound is a polycyclic organic compound comprising at least one component of the general structural formula $\{R\}\{F\}_n$, where R is a polycyclic core with conjugated π-system, F are modifying functional groups, and n is the number of functional groups.

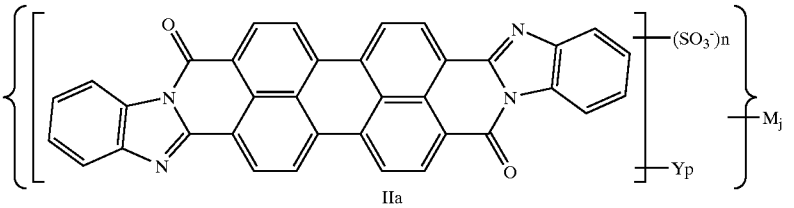
35. A monolithic three-dimensional integrated circuit according to claim 34, wherein said polycyclic organic compound is a sulfoderivative of a perynone dye with the general structural formula from the group I-XVII:



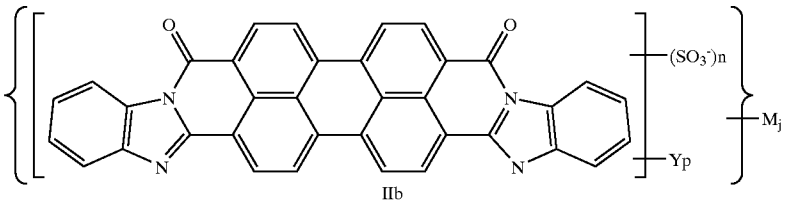
Ia



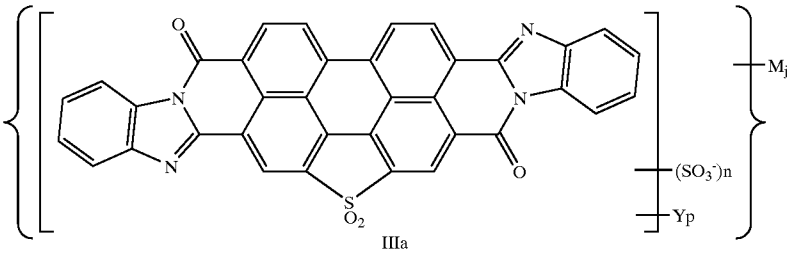
Ib



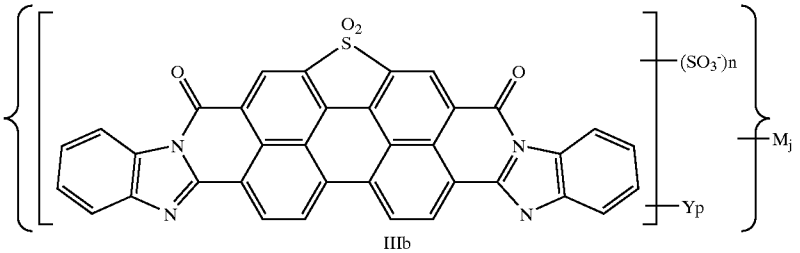
IIa



IIb

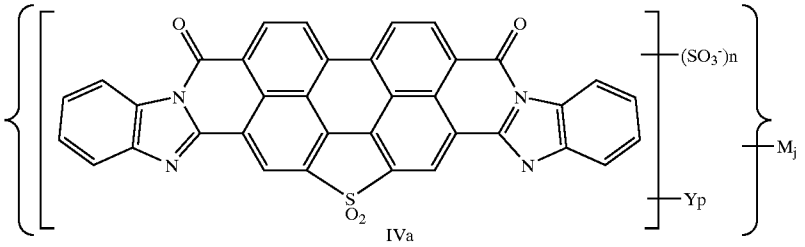


IIIa

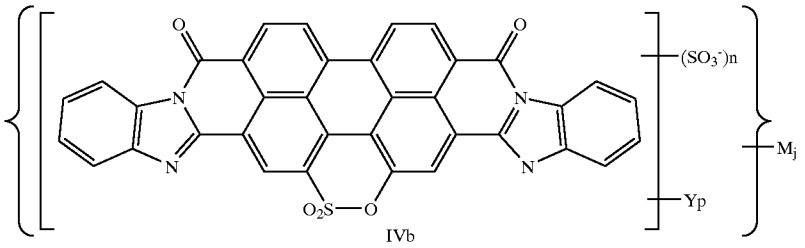


IIIb

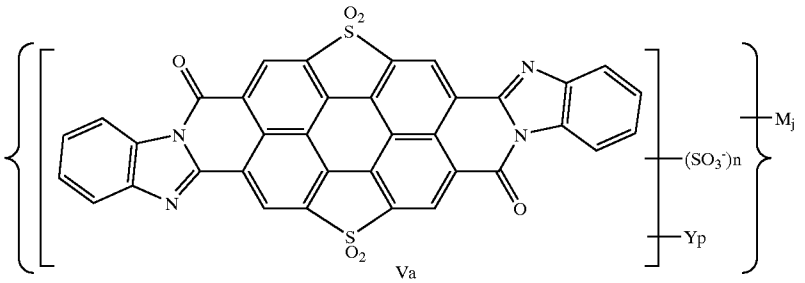
-continued



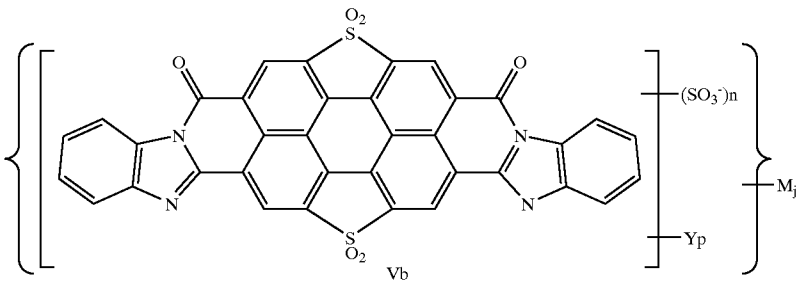
IVa



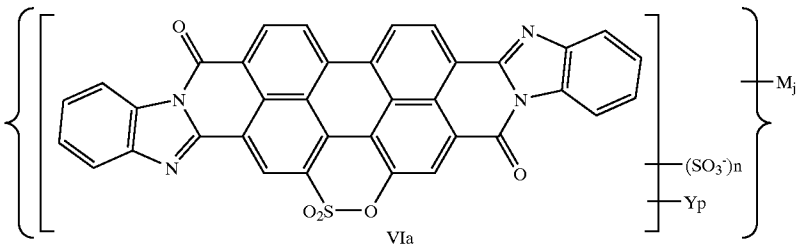
IVb



Va

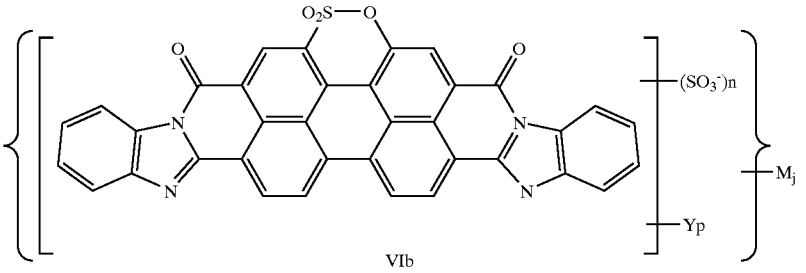


Vb

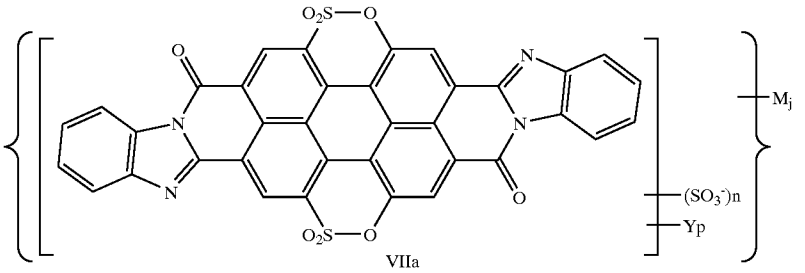


VIa

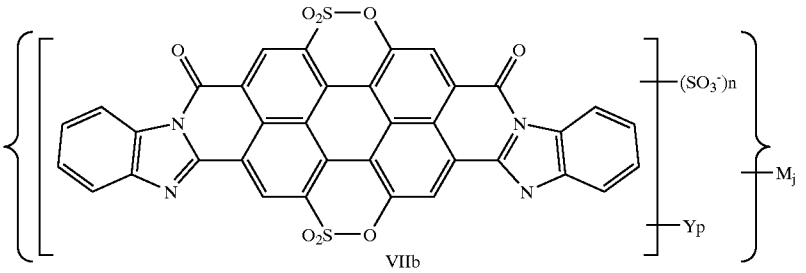
-continued



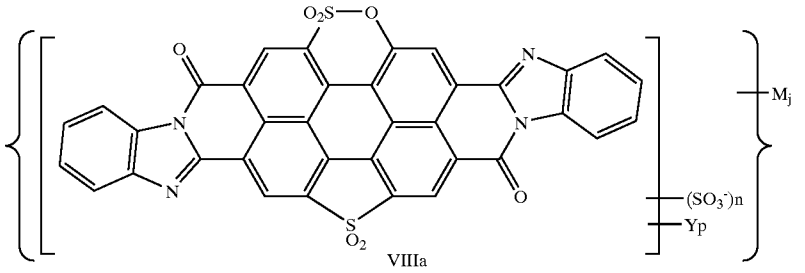
VIb



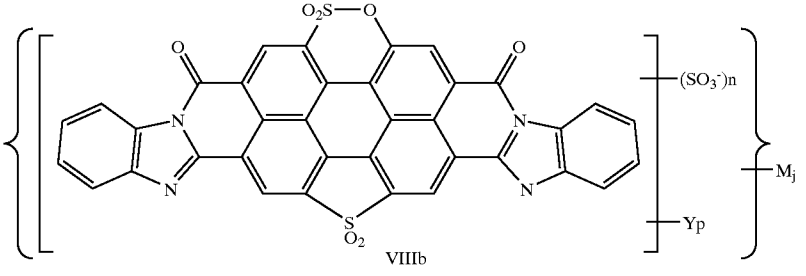
VIIa



VIIb

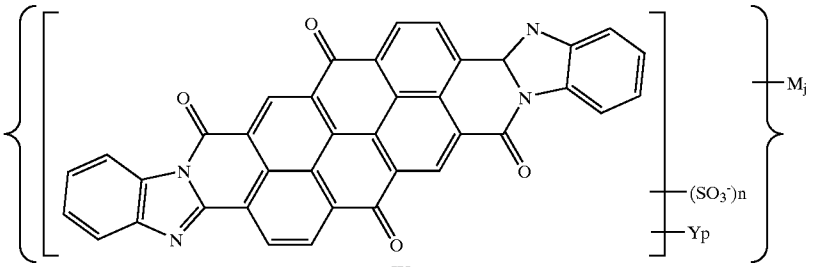


VIIIa

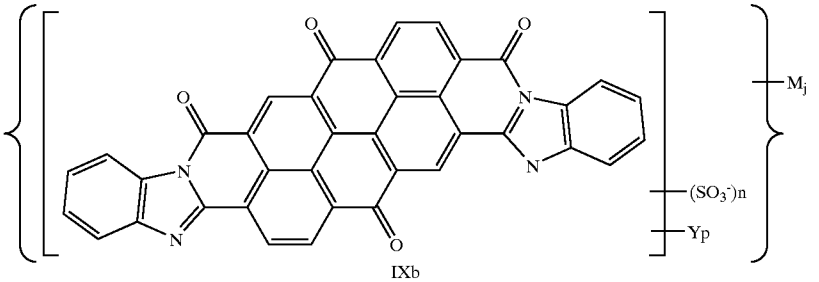


VIIIb

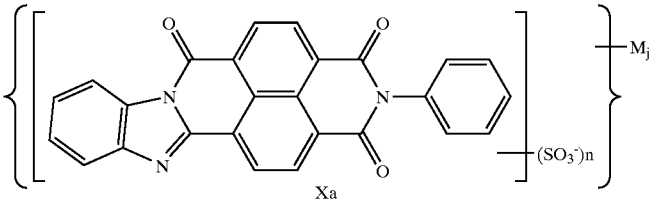
-continued



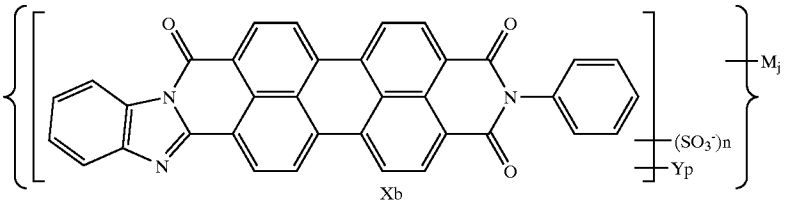
IXa



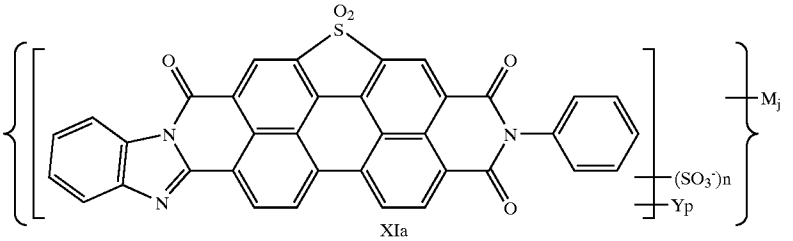
IXb



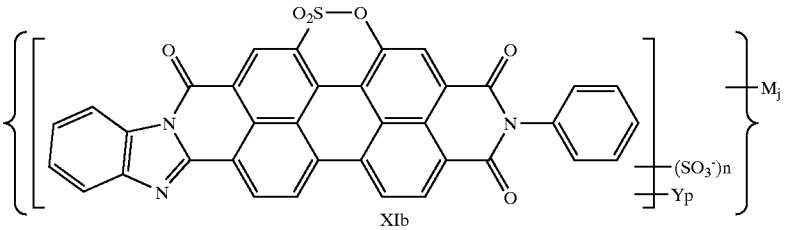
Xa



Xb

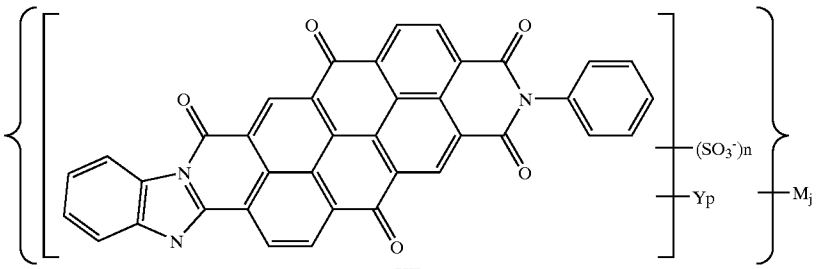


XIa

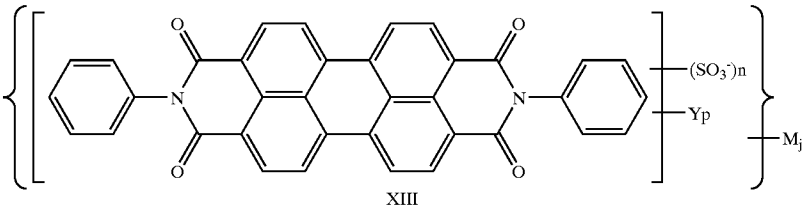


XIb

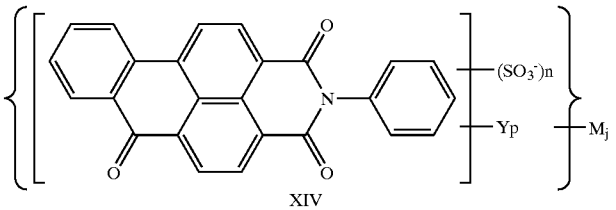
-continued



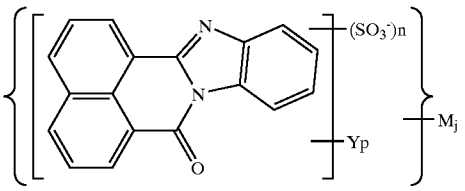
XII



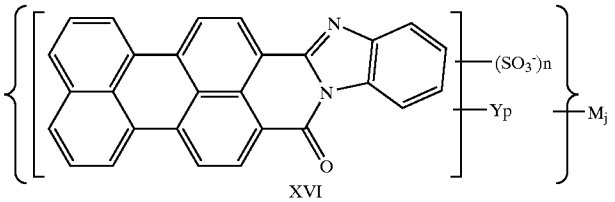
XIII



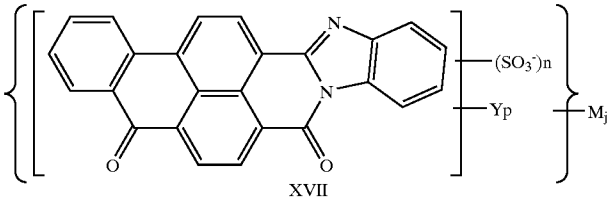
XIV



XV



XVI

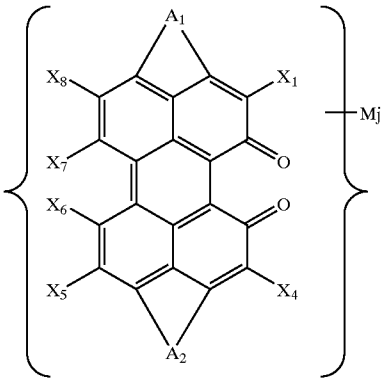


XVII

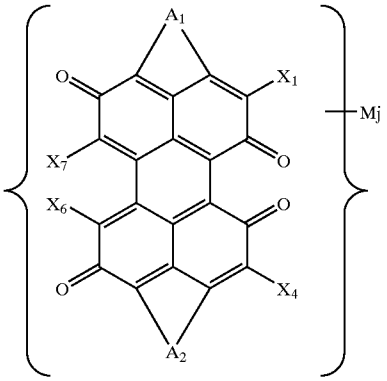
where n is an integer in the range of 1 to 4 and p is an integer in the range of 0 to 6; Y is individually selected from the group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2 and NH_2; M is a counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved.

36. A monolithic three-dimensional integrated circuit according to claim 34, wherein the polycyclic organic compound is a sulfoderivative of a heteroaromatic polycycloquinone with the general structural formula from the group XVIIIa-XVIIId:

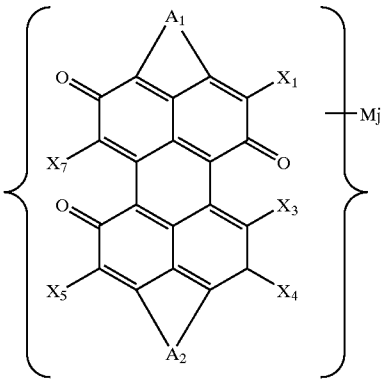
XVIIIa



XVIIIb

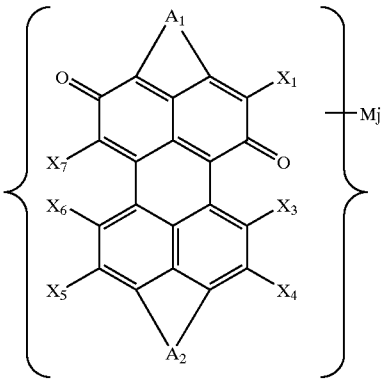


XVIIIc

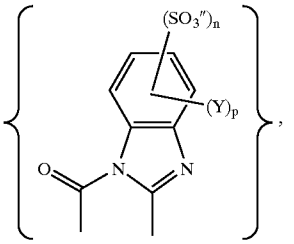


-continued

XVIIId



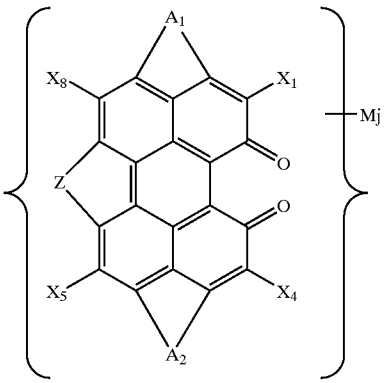
where A_1 и A_2 are fragments of the general structural formula,



X_1, X_3, X_4, X_5, X_6, X_7, X_8 are substituents from the group including H, OH, SO_3H, such that at least one of these substituents is different from H; Y is a substituent from the series H, Cl, F, Br, Alk, OH, OAlk, NO2, NH2 and p is an integer in the range of 0, 1, 2, 3 and 4; n is one of the group including 0, 1, 2, such that at least one of fragments A_1 or A_2 comprises at least one sulfogroup; M is counterion; and j is the number of counterions in the molecule, which can be fractional if the counterion belongs to several molecules; for n>1, different counterions M can be involved.

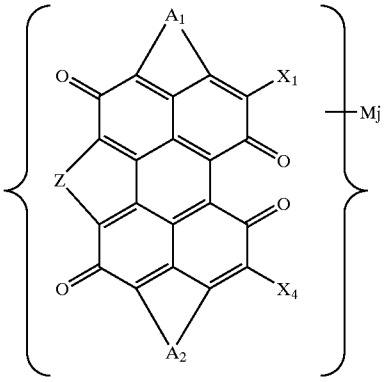
37. A monolithic three-dimensional integrated circuit according to claim 34 wherein the polycyclic organic compound is a sulfoderivative of a heteroaromatic polycycloquinone of the general structural formula from the group XIXa-XIXc:

XIXa

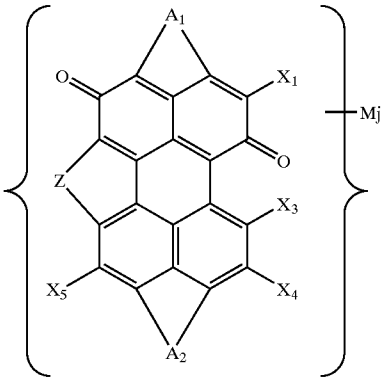


-continued

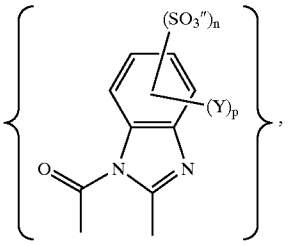
XIXb



XIXc



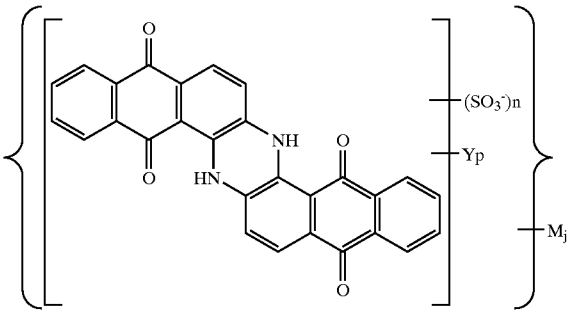
where A_1 и A_2 are fragments of the general structural formula



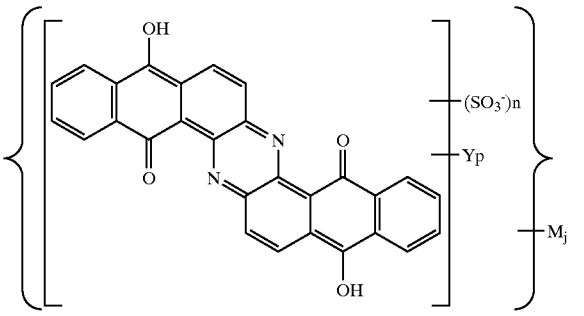
X_1, X_3, X_4, X_5, X_6, X_7, X_8 are substituents from the group including H, OH, SO_3H, and Z is bridge closing new heterocyclic systems chosen from the series —O—, —SO_2—, —SO_2—O—; Y is a substituent from the series H, Cl, F, Br, Alk, OH, OAlk, NO2, NH2 and p is an integer in the range of 0, 1, 2, 3 and 4; n is one of the group including 0, 1, 2, such that at least one of fragments A_1 or A_2 comprises at least one sulfogroup; M is counterion; and j is the number of counterions in the molecule, which can be fractional if the counterion belongs to several molecules; for n>1, different counterions M can be involved.

38. A monolithic three-dimensional integrated circuit according to claim 34, wherein the polycyclic organic compound is a sulfoderivative of dyes containing anthraquinone fragment of the general structural formula from the group XX-XXIV:

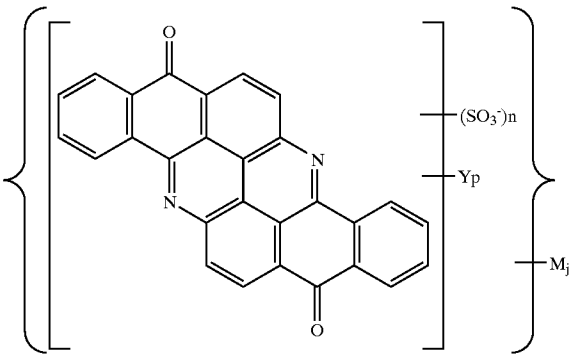
XXa



XXb

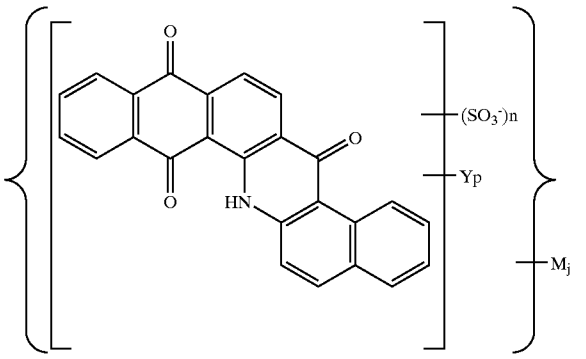


XXIa

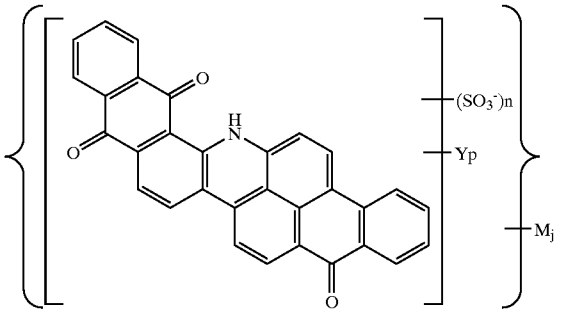


-continued

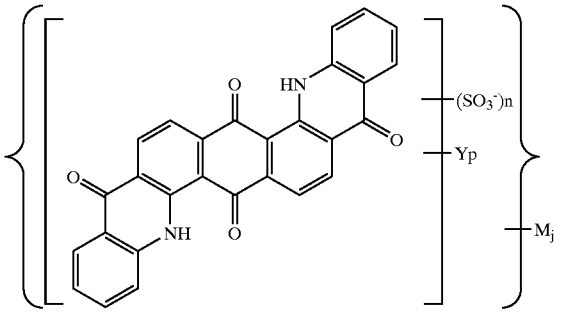
XXIb



XXIIa

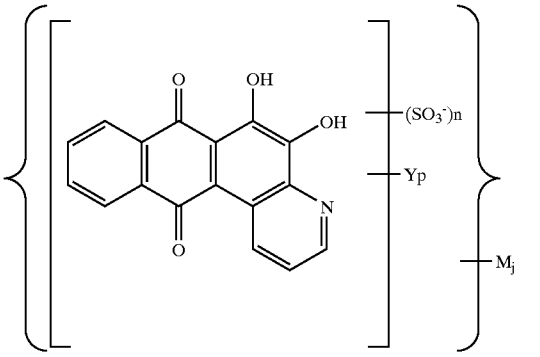


XXIIb

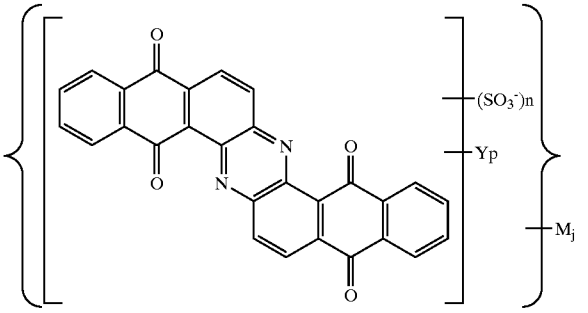


-continued

XXIII

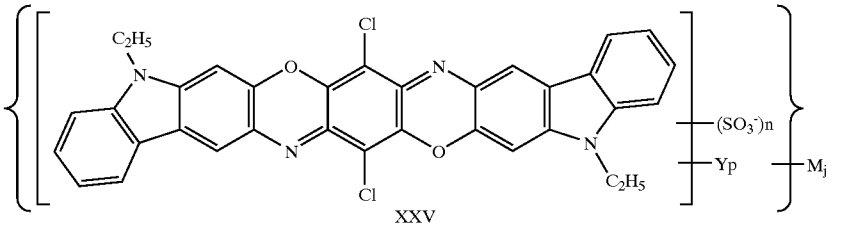


XXIV



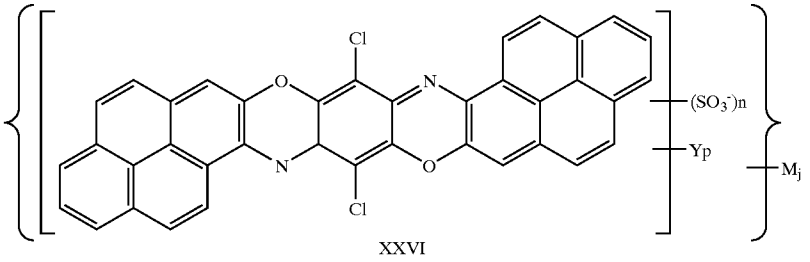
where n is an integer in the range of 1 to 4 and p is an integer in the range of 0 to 8; Y is individually selected from the group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2 and NH_2; M is a counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved.

39. A monolithic three-dimensional integrated circuit according to claim 34, wherein the polycyclic organic compound is sulfoderivative of fused polycyclic heteroaromatic compound comprising 5 or 6-membered rings with N or O or both: pyrrole, pyridine, oxazole, furan, oxazine, azine, chromone, pyridopyrimidine of the general structural formula from the group XXV-XXVIII:

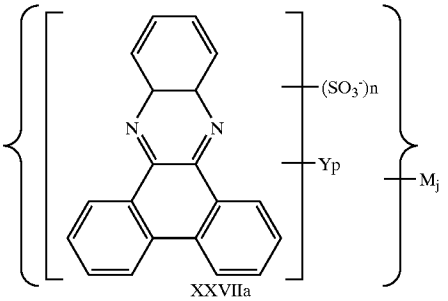


XXV

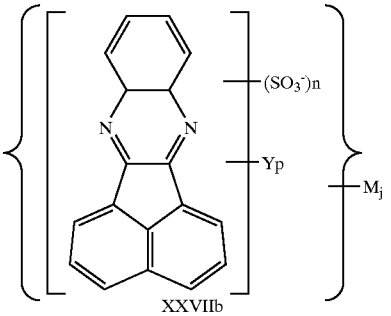
-continued



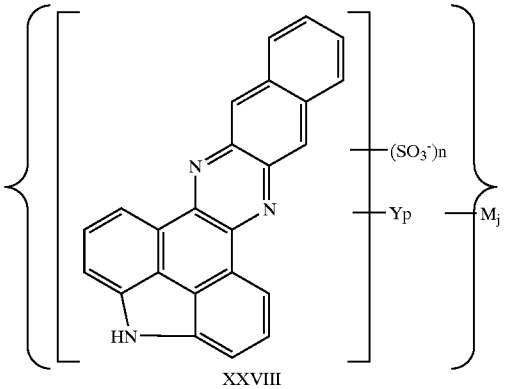
XXVI



XXVIIa



XXVIIb



XXVIII

where n is an integer in the range of 1 to 4 and p is an integer in the range of 0 to 8; Y is individually selected from the group consisting of H, Cl, F, Br, Alk, OH, OAlk, NO_2 and NH_2; M is a counterion; and j is the number of counterions in the molecule; for n>1, different counterions M can be involved.

40. The monolithic three-dimensional integrated circuit according to claims **30** or **31**, wherein at least one said functional heat-generating element is a semiconductor thin film transistor.

41. A monolithic three-dimensional integrated circuit according to claim 30, wherein at least one said functional heat-generating element is a semiconductor diode.

42. A monolithic three-dimensional integrated circuit according to claim 30, wherein at least one said functional heat-generating element is a thin-film resistor.

43. A monolithic three-dimensional integrated circuit according to claim 30, wherein at least one the integrated heat sink is made of an Al_2O_3 based ceramic material.

44. A monolithic three-dimensional integrated circuit according to claim 30, wherein at least one integrated heat sink has the shape of the cross section parallel to the front surface of said substrate selected from the list comprising circle, ellipse, square, rectangle, polygon, or any combination thereof.

45. A monolithic three-dimensional integrated circuit according to claim 30, wherein at least one unit integrated circuit further comprises at least one conducting element penetrating said substrate from rear surface to front surface and contacting with wiring pattern arranged on the front surface of said substrate.

46. A monolithic three-dimensional integrated circuit according to claim 30, further comprising at least one electrically conducting element, which is situated between two adjacent substrates and connects the wiring pattern arranged on the front surface of one substrate to the wiring pattern arranged on the front surface of another substrate.

47. A monolithic three-dimensional integrated circuit according to claim 30, wherein the planarization layer of at least one unit integrated circuit is made of a thermosetting material.

* * * * *