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(71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 South Federal Way, Boise, ID 83706–9632 (US).

(72) Inventor: BASCERI, Cem; 3236 Gekeler Lane, Apartment B–204, Boise, ID 83706 (US).

(74) Agent: D'AMICO, Thomas, J.; Dickstein Shapiro Morin & Oshinsky LLP, 2101 L Street, N.W., Washington, DC 20037–1526 (US).

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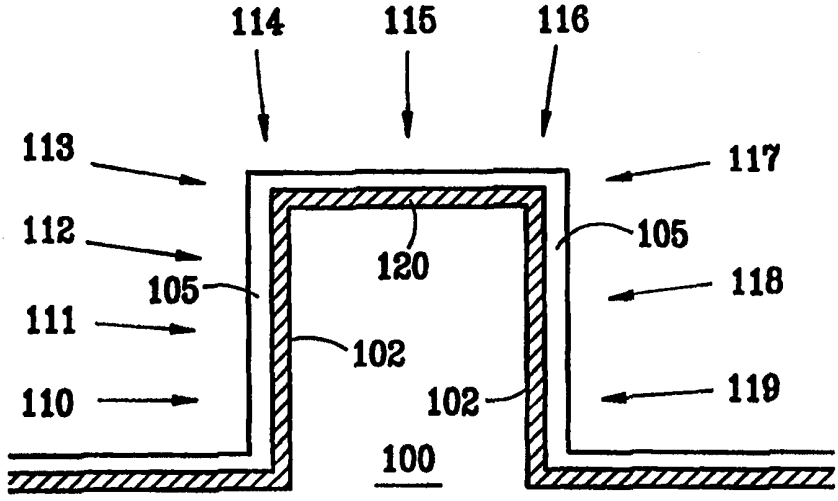
(54) Title: METHOD FOR IMPROVING THE SIDEWALL STOICHIOMETRY OF THIN FILM CAPACITORS

(57) Abstract

A method for ion implantation of high dielectric constant materials with dopants to improve sidewall stoichiometry is disclosed. Particularly, the invention relates to ion implantation of $(Ba,Sr)TiO_3$ (BST) with Ti dopants. The invention also relates to varying the ion implantation angle of the dopant to uniformly dope the high dielectric constant materials when they have been fabricated over a stepped structure. Additionally, the invention relates to forming a capping layer over a horizontal portion of the BST film to reduce excess dopant from being implanted into the horizontal section of the BST film. The invention also relates to integrated circuits having a thin film high dielectric material with improved sidewall stoichiometry used as an insulating layer in a capacitor structure.



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METHOD FOR IMPROVING THE SIDEWALL STOICHIOMETRY OF THIN FILM CAPACITORS

Field of the Invention

The invention relates generally to ion implantation of high dielectric constant materials with dopants to improve the sidewall stoichiometry of high dielectric thin films deposited over 3-D formations. Particularly, the invention relates to ion implantation of Ti into a $(Ba,Sr)TiO_3$ (BST) film by varying the implantation angle of the dopant to improve the sidewall stoichiometry the BST film. The invention also relates to integrated circuits having a doped thin film high dielectric material, used, for example, as an insulating layer in a capacitor.

Background of the Invention

High dielectric constant (HDC) materials have many microelectronic applications, such as DRAMs, embedded DRAMs, SRAMs, FeRAMS, on-chip capacitors and high frequency capacitors. Typically, these applications employ HDC materials in a capacitive structure, although the present invention may be used to make an HDC thin film with improved properties which is not part of a capacitor.

To facilitate construction of larger DRAMs with correspondingly smaller memory cells, capacitor structures and materials which can store the necessary charge in smaller spaces are needed. One of the most promising

avenues of research to achieve this goal is the area of HDC materials. HDC materials have dielectric constants of greater than about 50. Examples of particular HDC materials are metal oxide materials such as, lead zirconate titanate (PZT), barium titanate ($BaTiO_3$), strontium titanate ($SrTiO_3$), and barium strontium titanate (BST). It is desirable that such a material, if used for DRAMs and other microelectronics applications, be formable over an electrode and underlying structure (without significant harm to either), have low leakage current characteristics and long lifetime, and, for most applications, possess a high dielectric constant. The present invention relates to a method of forming a HDC film, for example, a BST dielectric film, with improved sidewall stoichiometry.

While BST materials have been manufactured in bulk form previously, the physical and electrical properties of the material is not well understood when BST is formed as a thin film (generally less than 5 um) on a semiconducting device. Methods to form the (Ba,Sr) TiO_3 material include deposition by a metal organic chemical vapor deposition (MOCVD) process using appropriate precursors. Typical MOCVD deposition of BST utilizes the precursors of Ba(bis(2,2,2,6-tetramethyl-3,5-heptanedionate))$_2$-tetraethylene glycol dimethyl ether; Sr(bis(2,2,2,6-tetramethyl-3,5-heptanedionate))$_2$-tetraethylene glycol dimethyl ether and Ti(bis(isopropoxy))$_2$bis(2,2,2,6-tetramethyl-3,5-heptanedionate)$_2$. A liquid delivery system mixed, metered and transported the precursors at room temperature and high pressure to a heated zone, where the precursors were

then flash vaporized and mixed with a carrier gas, typically argon, to produce a controlled temperature, low pressure vapor stream. The gas stream was then flowed into a reactor mixing manifold where the gas stream mixed with oxidizer gases. Typically the oxidizer gases were O_2 and N_2O. The mixture of the gas stream and the oxidizer gases then passed through a shower head injector into a deposition chamber. In the MOCVD deposition, both the ratio of the concentrations of the metalorganic compounds in the vaporized liquid and the deposition conditions determine the final film stoichiometry. However, the MOCVD BST deposition process suffers from the inhomogeneity in stoichiometry (A:B site ratio) on 3-D structures.

In addition, in submicron microcircuits such as DRAM capacitors, particular constraints are placed on BST thin film. First, the annealing temperature for BST thin films must generally be kept far below the temperatures commonly used for sintering bulk BST ceramics (generally less than 700°C vs. typically greater than 1100°C for bulk BST) to avoid damage to the underlying device structure. Thus, the grain nucleation and growth kinetics of the BST crystal lattice is inhibited resulting in smaller grain sizes. Second, the desired film thickness in microelectronic applications may be much less than 5 um (preferably between about 0.05 um and about 0.1 um). It has been found that median grains sizes generally less than half the BST film thickness are required to control dielectric uniformity and avoid shorted capacitors. Finally, when a BST film is formed in a microelectronic application such as a container or a stud, the sidewall components of the film

generally contains less titanium than is present in the horizontal components of the container or stud formation. The percentage of titanium in the film is critical to the physical end electrical functionality of the film. It has been shown that the titanium must be between about 50% to about 53.5% of the BST film in order for the film to have beneficial physical and electrical properties Thus, a method for producing a HDC material such as BST in a thin film structure having good dielectric properties and uniform titanium content is needed.

Summary of the Invention

The present invention overcomes the drawbacks of the conventional methods and provides an ion implanted high dielectric constant material having improved sidewall stochiometry. Particularly, the present invention overcomes the observed Ti-stoichiometry variation on the sidewalls of 3-D structures for MOCVD (BST) thin film capacitors. The inventor has observed that MOCVD BST thin films exhibit a deviation in A:B site ratio on the sidewalls of the trench or stud type structures. Typically, at these regions, at %Ti in the thin film is less than the desired value. The present invention overcomes these problems by implanting Ti ions by ion implantation after MOCVD process of BST. With this technique, it is possible to tailor the Ti composition in BST films, preferably on the sidewalls, by appropriate ion implantation angles.

The present invention also provides a method for tailoring the sidewall stoichiometry by providing a capping layer over the 3-D structure before Ti ion implantation thereby adjusting the sidewall stoichiometry of the BST film with ion implantation by varying the implantation angles.

The above and other advantages and features of the invention will be more clearly understood from the following detailed description which is provided in connection with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 is a schematic view of one embodiment of an apparatus used in the present invention.

FIG. 2 is a cross-sectional view of a container capacitor formed according to the present invention.

FIG. 3 is a cross-sectional view of an ion implantation of the sidewalls of a semiconductor device having a stud formation.

FIG. 4 is a cross-sectional view of an ion implantation of the sidewalls of a semiconductor device having a stud formation according to a second embodiment of the present invention.

FIG. 5 is a cross-sectional view of an ion implantation step of a portion of a semiconductor device having a stud formation at a processing step subsequent to that shown in FIG. 4.

FIG. 6 is a cross-sectional view of an ion implantation step of a portion of a semiconductor device having a stud formation at a processing step subsequent to that shown in FIG. 5.

Detailed Description of the Preferred Embodiments

The terms wafer or substrate used in the description include any semiconductor-based structure having an exposed silicon surface in which to form the contact electrode structure of this invention. Wafer and substrate are to be understood as including silicon-on insulator (SOI) technology, silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure or foundation. It should also be understood that the term wafer or substrate may relate to a base semiconductor structure having undergone processing steps to arrive at a semiconductor platform which may undergo further processing.

The term "metal oxide" or "high dielectric constant material (HDC)" used herein means a material of the general form ABO_3 where A and B are cations. The term is intended to include materials were A and B represent multiple elements; for example, it includes materials of the form $A'A''BO_3$, $AB'B''O_3$, and $A'A''B'B''O_3$, where A', A'', B' and B'' are different metal elements. Preferably, A, A'', A'', are metals selected from the group of metals consisting of Ba, Bi, Sr, Pb, Ca, and La, and B, B', and B'' are metals selected from the group consisting of Ti, Zr, Ta, Mo, W, and Nb. Preferably the metal oxide is a perovskite. Many of these metal oxides are ferroelectrics; however the present invention is not so limited.

As will be understood by those skilled in the art, most crystalline materials having an ABO_3 formula are perovskite crystalline compounds. These structures ideally have a unit cell forming a simple cubic structure including A-type cations at the corners of a cube, a B-type cation at the centroid of the cube, and oxygen atoms entered at each facial plane of the cube; however, this idealized structure may vary considerably with temperature. Other forms of perovskite-type compounds can be classified, for example, as orthombic, pseudocubic, pseudotetragonal, rombohedral, and tetragonal.

Some materials falling within the class of ABO_3, such as barium strontium titanate (BST) exhibit electrical properties that are often very different when measured from bulk ceramics, as compared to the thin film

materials (i.e., those less than about ten microns thick) that are used in integrated circuits. Bulk ceramics are typically sintered at temperatures reaching from 1400°C to 1500°C, and this high temperature tends to produce a correspondingly high degree of defect-free crystallization. On the other hand, thin films are generally not sintered above about 900°C to 1100°C due to the potential for breakdown of integrated circuit wiring, layer interdiffusion, and cracking. Thin films are most often deposited by conventional sputtering techniques, e.g., radio frequency or DC magnetron sputtering. On a microscopic level, these techniques can provide clumped areas of massed materials having nonuniform thicknesses, stratified layers that are improperly mixed to non-homogeneic proportions that are incapable of forming proper average crystals according to the mixture of ingredients. Accordingly, those attempting to replicate bulk ceramic behavior in thin film electronic components have often been unable to duplicate these parameters, even if the electron transfer mechanism remains the same between the two thicknesses of materials.

The Ba/Sr ratio of BST should be about 70/30 allowing the material to operate in the paraelectric region for DRAM applications since this will reduce the complexity of understanding the material's response. Therefore, the importance of Ba/Sr ratio in the BST material is controlling the curie temperature (Tc) to be nearly room temperature, thus giving the material the advantage of having a high dielectric constant since the dielectric constant exhibits a peak near Tc while allowing the material to be in the

paraelectric region for the operating temperature of the DRAM cell. By maintaining a Ba/Sr ratio of about 70/30, the danger of shifting to ferroelectric state by a possible shift in temperature (less than room temperature) is eliminated. This is because the material exhibits a curie-point at room temperature for Ba/Sr: 70/30, but does not go to the ferroelectric phase until temperatures of about 190°K.

Additionally, it is important that the percentage of Ti in the BST thin film is between about 50% and about 53.5%. When the percentage of Ti in the BST thin film is outside this range, the BST thin film will exhibit poor physical and electrical properties. For example, when the percentage of Ti in the BST thin film is outside the prescribed range, the BST thin film will exhibit a poor dielectric constant and also will exhibit increased current leakage.

Since the stoichiometry of BST formed on the sidewalls of trenches can deviate from the target values, it is necessary to maintain the stoichiometry at the sidewalls. This becomes a serious issue for deep trenches (e.g., 10:1 aspect ratios) since properties such as dielectric constant, leakage, relaxation and resistance degradation will deviate at the sidewalls from other locations on a semiconductor. With the present invention sidewalls can be doped to achieve the desired stoichiometries by using appropriate implant angles. Thus, with appropriate doping levels, sidewall stoichiometries can be tailored to achieve desired physical properties.

The metal oxides or high dielectric constant materials according to the present invention are doped by ion implantation of dopants into the host lattice of the metal oxide or HDC material. Ion implantation is a well known process for the implantation of dopant elements into a material. The dopants are selected from Ba, Bi, Sr, Pb, Ca, and La for the A site and Ti, Zr, Ta, Mo, W, and Nb for the B-site based on the particular HDC material. For example, in a BST metal oxide, the A-site can be doped with additional Ba or Sr while the B-site can be doped with additional Ti to tailor the particular stoichiometry of the thin film.

Capacitor size requirements presently constitute a limiting factor in further reductions of DRAM cell size. A reduction in DRAM cell size is essential to further significant increases in DRAM cell densities for use in an integrated circuit, but this size reduction advantage will require a further reduction in the size of the cell capacitor. Reduction of the capacitor size can be achieved by increasing the dielectric constant of the material used in the dielectric layer of the capacitor, in order to permit the use of a smaller surface area in a capacitor having the desired dielectric properties. Prior methods for increasing the dielectric constant of materials have met with failure because these methods also increased the leakage current and the corresponding conductive current density of the dielectric material at fixed bias voltages. Excessive leakage current or conductive current density renders the material unfit for capacitors in integrated circuits and, in particular, unfit for capacitors in DRAM cells. It remains a problem in the field to increase the dielectric

constant of materials, even for high dielectric constant material, such as BST, without significantly increasing the leakage current.

By doping the HDC material with A or B ions it is possible to maintain the dielectric constant of the material as well as prevent current leakage from the material. An exemplary apparatus used in the process for ion implantation according to one embodiment of the present invention is described below. It is to be understood, however, that this apparatus is only one example of many possible different arrangements that may be used to implant dopants according to the invention. The invention is not intended to be limited by the particular apparatus described below.

Referring now to FIG. 1, a closed ion implant system 10 for ion implanting semiconductor wafers in accordance with the method of the invention is shown. The ion implant system 10 includes an ion implanter 16. The construction for the ion implanter 16 shown in FIG. 1 is merely illustrative as other types of ion implanter constructions would also be suitable. In the illustrative embodiment, the ion implanter 16 includes a wafer holder 40 for receiving a wafer 18 from the transport channel 26 and for holding the wafer for implantation. The wafer 18 has a HDC thin film layer formed thereon as discussed above. The ion implanter 16 includes an ion source 42, an analyzing magnet 44, an acceleration tube 46, a focus structure 48, and a gate plate 50. The ion implanter 16 is in flow communication with a suitable vacuum source (not shown) such as a turbo

molecular pump. This generates a vacuum within the process chamber of the ion implanter 16. With this arrangement an ion implant beam 52 is focused on the high dielectric constant thin film on the surface of the wafer 18 for implanting a desired dopant (such as, for example, Ba, Bi, Sr, Pb, Ca, and La for the A site and Ti, Zr, Ta, Mo, W, and Nb for the B-site based on the particular HDC material) into the crystal lattice structure of the high dielectric constant thin film. After ion implantation the wafer 18 is transferred from the wafer holder 40 to another transport channel 28. At the transport channel 28, the wafer 18 is discharged from the system 10.

At this point, the wafer 18 has a conductive layer 60 formed of a suitable conductive material with a doped dielectric film layer 65 formed over the conductive layer 60. A second conductive layer 68 is then formed over doped dielectric film layer 65 to form the container capacitor structure as shown in FIG. 2. The conductive layers 60, 68 may be formed of any conductive material such as metals, i.e., Pt, Ru, Ir, Pd, Au or conductive oxides such as a ruthenium oxide (RuO_x) or an iridium oxide (IrO_x). The doped dielectric film layer 65 is formed by doping a HDC material as described above.

Reference is now made to FIG. 3. This figure shows a representative view of a stud capacitor formation according to the present invention. Dopant levels of the HDC film, such as BST, formed on the sidewalls 102 of a stud 100 can deviate from the target values. This becomes

a serious issue for deep trenches (e.g., 10:1 aspect ratios) or studs as shown in FIG. 3 since properties such as dielectric constant and leakage will deviate at the sidewalls from the values for these properties in the horizontal portions of the device. According to the present invention the HDC, e.g. BST, dielectric layer 105 formed over a conductive layer 120 on the sidewalls 102 can be doped to achieve the desired stoichiometries by appropriate implant angles 110-119 by appropriate movement of wafer holder 40. A second electrode (not shown) may then be formed over the HDC, e.g. BST, layer 105 to arrive a capacitor structure. Thus, with appropriate doping levels, the HDC layer 105 overlying the conductive layer 120 on sidewalls 102 can be tailored to achieve desired physical properties.

Reference is now made to FIG. 4. This figure shows a representative view of a second embodiment of the present invention. Dopant levels of BST formed on the sidewalls 202 of a stud 200 can deviate from the target values. This becomes a serious issue for deep trenches (e.g., 10:1 aspect ratios) or studs as shown in FIGS. 4-6 since properties such as dielectric constant and leakage will deviate at the sidewalls from the values for these properties in the horizontal portions of the device. A passivation layer 250 is deposited over the horizontal sections of the stud 200 as shown in FIG. 4. The passivation layer 250 may be formed of any material such that the BST dielectric layer 205 formed under the passivation layer 250 is significantly shielded form ion implantation.

Reference is now made to FIG. 5. According to the second embodiment of the present invention the BST dielectric layer 205 formed over a conductive layer 220 on the sidewalls 202 can be doped to achieve the desired stoichiometries by appropriate implant angles 210-219. The appropriate movement of wafer holder 40, as shown in representative apparatus in FIG. 1, is used to effectuate the appropriate implant angels 210-219. The passivation layer 250 prevents dopant from being implanted into the BST film that overlies the horizontal regions of the stud 200.

The passivation layer 250 is then removed from the horizontal surfaces of the stud 200 as shown in FIG. 6. A second electrode (not shown) may then be formed over BST layer 205 to arrive at a capacitor structure. Thus, with appropriate doping levels, the BST layer 205 overlying the conductive layer 220 on sidewalls 202 can be tailored to achieve desired physical properties.

The present invention provides a method for ion implantation of HDC materials with dopants to reduce film leakage and improve resistance degradation. The invention also provides a method for varying the ion implantation angle of the dopant to uniformly dope the high dielectric constant materials when they have been fabricated over a stepped structure.

It should again be noted that although the invention has been described with specific reference to DRAM memory circuits and container capacitors, the invention has broader applicability and may be used in any

integrated circuit, such as, for example in a capacitor. Similarly, the process described above is but one method of many that could be used. Furthermore, although the invention has been described with reference to BST as a preferred HDC material which can be used in the invention, the invention has more widespread applicability to any HDC material. Accordingly, the above description and accompanying drawings are only illustrative of preferred embodiments which can achieve the features and advantages of the present invention. It is not intended that the invention be limited to the embodiments shown and described in detail herein. The invention is only limited by the spirit and scope of the following claims.

1. A method for maintaining the stoichiometry of a high dielectric constant thin film material formed on a three dimensional substrate, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a high dielectric constant thin film material on said substrate; and

doping said high dielectric thin film material with a dopant by ion implantation, wherein said high dielectric thin film material is doped to maintain the stoichiometry of said high dielectric thin film material.

2. The method according to claim 1, wherein said high dielectric thin film material is doped by varying the implant angle of the dopant.

3. The method according to claim 2, wherein said high dielectric constant thin film material is selected from the group consisting of BST, SBT, $SrTiO_3$ and PZT.

4. The method according to claim 3, wherein said high dielectric constant thin film material is BST.

5. The method according to claim 4, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

6. The method according to claim 2, wherein said high dielectric constant thin film material is a pervoskite of the formula ABO_3 where A represents metals selected from Ba, Bi, Sr, Pb, Ca, and La, and B represents metals selected from Ti, Zr, Ta, Mo, W, and Nb.

7. The method according to claim 6, wherein said doping step includes doping the A-site of said high dielectric constant thin film material with a dopant selected from the group consisting of Ba, Bi, Sr, Pb, Ca, and La.

8. The method according to claim 6, wherein said doping step includes doping the B-site of said high dielectric constant thin film material with a dopant selected from the group consisting of Ti, Zr, Ta, Mo, W, and Nb.

9. The method according to claim 6, wherein said pervoskite is barium strontium titanite and said doping step includes doping the A-site with a dopant selected from the group consisting of Ba, and Sr.

10. The method according to claim 6, wherein said pervoskite is barium strontium titanite and said doping step includes doping the B-site with Ti.

11. The method according to claim 10, wherein said barium strontium titanite is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% in said barium strontium titanite film.

12. The method according to claim 11, wherein the ratio of Ba to Sr is about 70:30.

13. A method for maintaining the stoichiometry of a high dielectric constant thin film material formed on a three dimensional substrate, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a high dielectric constant thin film material on said substrate;

forming a capping layer over said first level and said second level of said substrate; and

doping said high dielectric thin film material formed on said sidewalls with a dopant by ion implantation, wherein said high dielectric thin film material is doped to maintain the stoichiometry of said high dielectric thin film material.

14. The method according to claim 13, wherein said high dielectric thin film material is doped by varying the implant angle of the dopant.

15. The method according to claim 14, wherein said high dielectric constant thin film material is selected from the group consisting of BST, SBT, $SrTiO_3$ and PZT.

16. The method according to claim 15, wherein said high dielectric constant thin film material is BST.

17. The method according to claim 16, wherein said dopants are selected from the group consisting of barium, strontium and titanium..

18. The method according to claim 14, wherein said high dielectric constant thin film material is a pervoskite of the formula ABO_3 where A represents metals selected from Ba, Bi, Sr, Pb, Ca, and La, and B represents metals selected from Ti, Zr, Ta, Mo, W, and Nb.

19. The method according to claim 18, wherein said doping step includes doping the A-site of said high dielectric constant thin film material with a dopant selected from the group consisting of Ba, Bi, Sr, Pb, Ca, and La.

20. The method according to claim 18, wherein said doping step includes doping the B-site of said high dielectric constant thin film material with a dopant selected from the group consisting of Ti, Zr, Ta, Mo, W, and Nb.

21. The method according to claim 18, wherein said pervoskite is barium strontium titanite and said doping step includes doping the A-site with a dopant selected from the group consisting of Ba and Sr.

22. The method according to claim 18, wherein said pervoskite is barium strontium titanite and said doping step includes doping the B-site with Ti.

23. The method according to claim 22, wherein said barium strontium titanite is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% in said barium strontium titanite film.

24. The method according to claim 23, wherein the ratio of Ba to Sr is about 70:30.

25. A method for maintaining the stoichiometry of a BST high dielectric constant thin film material formed on a three dimensional substrate, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a BST high dielectric constant thin film material on said substrate; and

doping said BST high dielectric thin film material with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said BST high dielectric thin film material.

26. The method according to claim 25, wherein BST high dielectric thin film material is doped by varying the implant angle of the dopant.

27. The method according to claim 26, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

28. The method according to claim 27, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

29. The method according to claim 27, wherein said BST high dielectric thin film material is doped with Ti.

30. The method according to claim 29, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

31. The method according to claim 30, wherein the ratio of Ba to Sr is about 70:30.

32. A method for maintaining the stoichiometry of a BST high dielectric constant thin film material formed on a three dimensional substrate, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a BST high dielectric constant thin film material on said substrate;

forming a capping layer over said first and second levels of said substrate; and

doping said BST high dielectric thin film material formed on said sidewalls of said substrate with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said high dielectric thin film material.

33. The method according to claim 32, wherein BST high dielectric thin film material is doped by varying the implant angle of the dopant.

34. The method according to claim 33, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

35. The method according to claim 34, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

36. The method according to claim 34, wherein said BST high dielectric thin film material is doped with Ti.

37. The method according to claim 36, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

38. The method according to claim 37, wherein the ratio of Ba to Sr is about 70:30.

39. A BST high dielectric constant thin film material having improved sidewall stoichiometry formed by the steps of:

providing a substrate having at least one horizontal component and at least one vertical component;

forming a BST high dielectric constant thin film material on said substrate; and

doping said BST high dielectric thin film material with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said BST high dielectric thin film material.

40. The BST high dielectric constant thin film material according to claim 39, wherein BST high dielectric thin film material is doped by varying the implant angle of the dopant.

41. The BST high dielectric constant thin film material according to claim 40, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

42. The BST high dielectric constant thin film material according to claim 40, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

43. The BST high dielectric constant thin film material according to claim 40, wherein said BST high dielectric thin film material is doped with Ti.

44. The BST high dielectric constant thin film material according to claim 43, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

45. The BST high dielectric constant thin film material according to claim 44, wherein the ratio of Ba to Sr is about 70:30.

46. The BST high dielectric constant thin film material according to claim 40, wherein said BST high dielectric thin film material is included in a DRAM cell.

47. The BST high dielectric constant thin film material according to claim 40, wherein said BST high dielectric thin film material is formed in a capacitor.

48. A BST high dielectric constant thin film material having improved sidewall stoichiometry formed by the steps of:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a BST high dielectric constant thin film material on said substrate;

forming a capping layer over said first and second levels of said substrate; and

doping said BST high dielectric thin film material formed on said sidewalls of said substrate with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said high dielectric thin film material.

49. The BST high dielectric constant thin film material according to claim 48, wherein BST high dielectric thin film material is doped by varying the implant angle of the dopant.

50. The BST high dielectric constant thin film material according to claim 49, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

51. The BST high dielectric constant thin film material according to claim 49, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

52. The BST high dielectric constant thin film material according to claim 49, wherein said BST high dielectric thin film material is doped with Ti.

53. The BST high dielectric constant thin film material according to claim 52, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

54. The BST high dielectric constant thin film material according to claim 53, wherein the ratio of Ba to Sr is about 70:30.

55. The BST high dielectric constant thin film material according to claim 49, wherein said BST high dielectric thin film material is included in a DRAM cell.

56. The BST high dielectric constant thin film material according to claim 49, wherein said BST high dielectric thin film material is formed in a capacitor.

57. A method for fabricating a high capacitance thin film integrated circuit capacitor device, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a first electrode on said substrate;

forming a BST high dielectric constant thin film material on said first electrode;

doping said BST high dielectric thin film material with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped to maintain the stoichiometry of said BST high dielectric thin film material; and

forming a second electrode on said BST high capacitance thin film layer to complete said integrated circuit capacitor.

58. The method according to claim 57, wherein said B BST high dielectric thin film material is doped by varying the implant angle of the dopant.

59. The method according to claim 58, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

60. The method according to claim 59, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

61. The method according to claim 59, wherein said BST high dielectric thin film material is doped with Ti.

62. The method according to claim 61, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

63. The method according to claim 62, wherein the ratio of Ba to Sr is about 70:30.

64. The method according to claim 58, wherein said first and second electrodes are selected from the group consisting of Pt, Ru, Ir, Pd, Au ruthenium oxides, and iridium oxides.

65. The method according to claim 58, wherein said integrated circuit capacitor is fabricated in a DRAM cell.

66. A method for fabricating a high capacitance thin film integrated circuit capacitor device, said method comprising:

providing a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

forming a first electrode on said substrate;

forming a BST high dielectric constant thin film material on said first electrode;

forming a capping layer over said first and second levels of said BST high dielectric constant thin film material;

doping said BST high dielectric thin film material formed on said sidewalls with a dopant by ion implantation, wherein said BST high dielectric thin film material is doped by varying the ion implantation implant angle to maintain the stoichiometry of said BST high dielectric thin film material; and

removing said capping layer and forming a second electrode on said BST high capacitance thin film layer to complete said integrated circuit capacitor.

67. The method according to claim 66, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

68. The method according to claim 67, wherein said BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

69. The method according to claim 67, wherein said BST high dielectric thin film material is doped with Ti.

70. The method according to claim 69, wherein said BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

71. The method according to claim 70, wherein the ratio of Ba to Sr is about 70:30.

72. The method according to claim 66, wherein said first and second electrodes are selected from the group consisting of Pt, Ru, Ir, Pd, Au ruthenium oxides, and iridium oxides.

73. The method according to claim 66, wherein said integrated circuit capacitor is fabricated in a DRAM cell.

74. An integrated circuit capacitor device comprising:

a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

a first electrode provided on said substrate;

a doped BST high dielectric constant thin film material provided on said first electrode, said doped BST high dielectric thin film material being doped to maintain the stoichiometry of said BST high dielectric thin film material; and

a second electrode provided on said BST high capacitance thin film layer to complete said integrated circuit capacitor.

75. The integrated circuit capacitor device according to claim 74, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

76. The integrated circuit capacitor device according to claim 75, wherein said doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

77. The integrated circuit capacitor device according to claim 75, wherein said doped BST high dielectric thin film material is doped with Ti.

78. The integrated circuit capacitor device according to claim 76, wherein said doped BST high dielectric thin film material is doped with Ti to

maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

79. The integrated circuit capacitor device according to claim 78, wherein the ratio of Ba to Sr is about 70:30

80. The integrated circuit capacitor device according to claim 74, wherein said first and second electrodes are selected from the group consisting of Pt, Ru, Ir, Pd, Au ruthenium oxides, and iridium oxides.

81. The integrated circuit capacitor device according to claim 74, wherein said integrated circuit capacitor is a container capacitor.

82. The integrated circuit capacitor according to claim 74, wherein said integrated circuit capacitor is formed over a stud.

83. The integrated circuit capacitor according to claim 74, wherein said integrated circuit capacitor is fabricated in a DRAM cell.

84. An integrated circuit comprising:

a substrate having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

a first electrode provided on said substrate;

a doped BST high dielectric constant thin film material provided on said first electrode, said doped BST high dielectric thin film material being doped by angled ion implantation; and

a second electrode provided on said BST high capacitance thin film layer to complete said integrated circuit capacitor.

85. The integrated circuit capacitor device according to claim 84, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

86. The integrated circuit capacitor device according to claim 85, wherein said doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

87. The integrated circuit capacitor device according to claim 85, wherein said doped BST high dielectric thin film material is doped with Ti.

88. The integrated circuit capacitor device according to claim 86, wherein said doped BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

89. The integrated circuit capacitor device according to claim 88, wherein the ratio of Ba to Sr is about 70:30

90. The integrated circuit capacitor device according to claim 84, wherein said first and second electrodes are selected from the group consisting of Pt, Ru, Ir, Pd, Au ruthenium oxides, and iridium oxides.

91. The integrated circuit capacitor device according to claim 84, wherein said integrated circuit capacitor is a container capacitor.

92. The integrated circuit capacitor according to claim 84, wherein said integrated circuit capacitor is formed over a stud.

93. The integrated circuit capacitor according to claim 84, wherein said integrated circuit capacitor is fabricated in a DRAM cell.

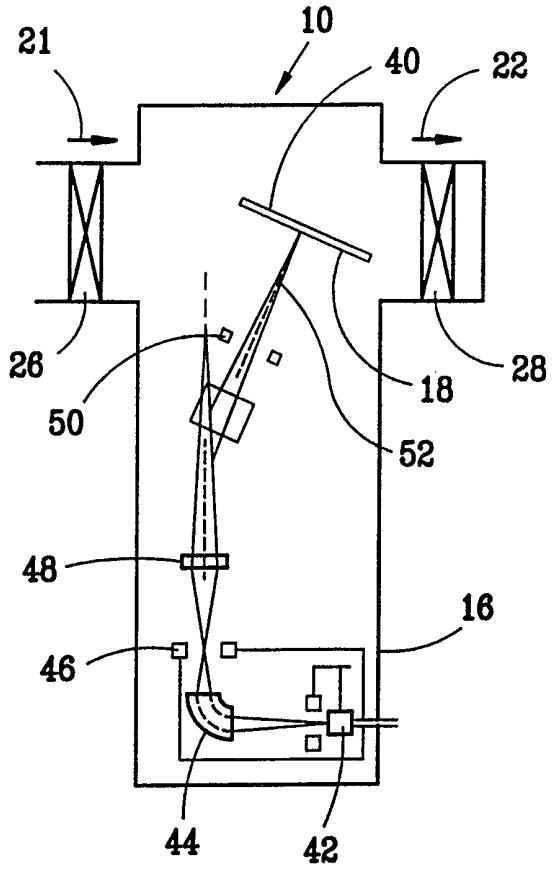

FIG. 1

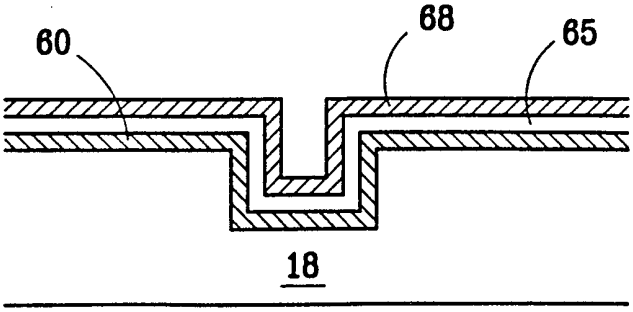

FIG. 2

FIG. 3

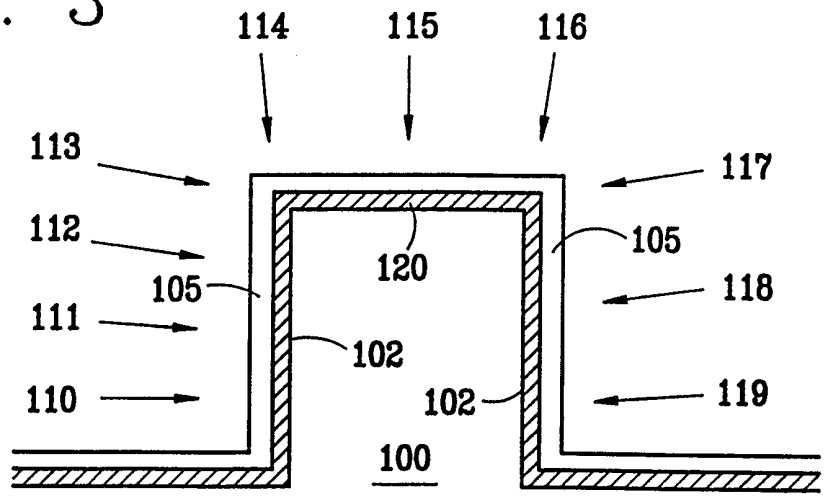
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FIG. 4

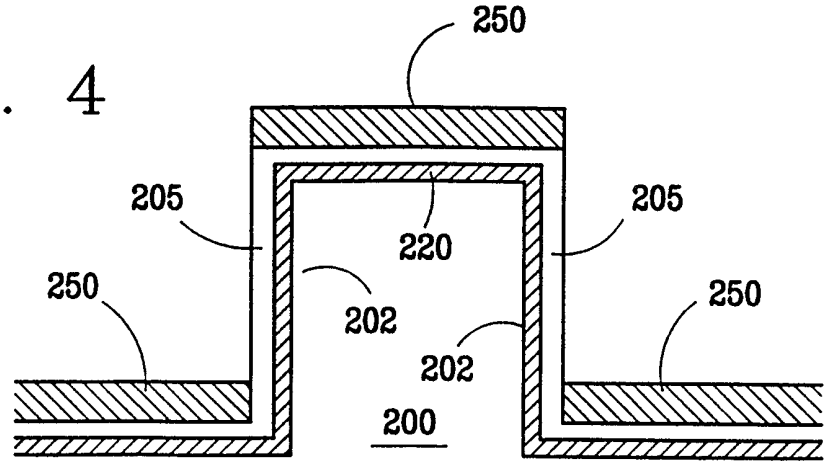
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FIG. 5

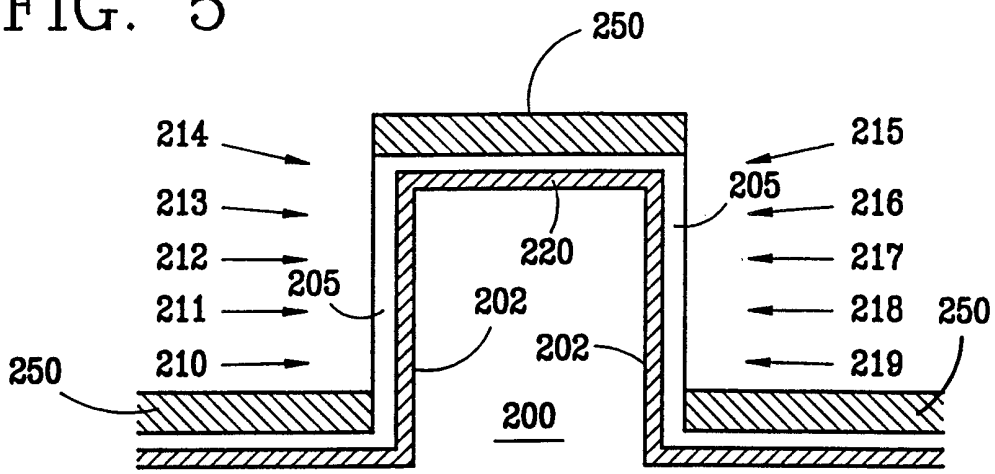
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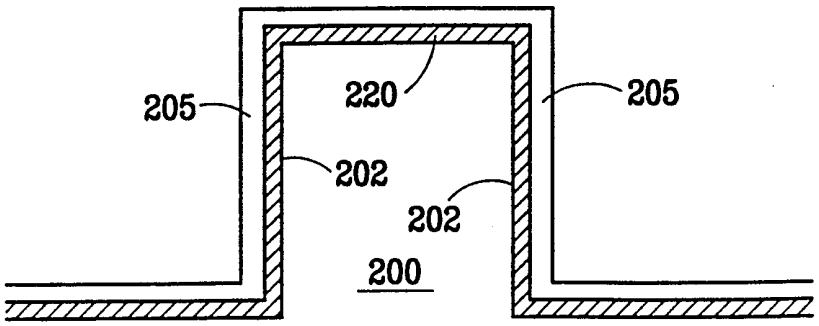
FIG. 6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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/00242

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/316

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	EP 0 380 326 A (SEIKO EPSON CORP) 1 August 1990 (1990-08-01) abstract; figure 1 column 3	1-38, 57-73
A	US 5 618 761 A (EGUCHI KAZUHIRO ET AL) 8 April 1997 (1997-04-08) figures 13-14,16B; example 2	39-56, 74-93

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
22 May 2000	02/06/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Szarowski, A

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INTERNATIONAL SEARCH REPORT

	national Application No
	PCT/US 00/00242

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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