



(51) International Patent Classification:

G01V 3/10 (2006.01) G01R 33/12 (2006.01)
G01N 27/72 (2006.01)

(21) International Application Number:

PCT/US2018/038766

(22) International Filing Date:

21 June 2018 (21.06.2018)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/524,234 23 June 2017 (23.06.2017) US

(71) Applicant: FIRST TEXAS PRODUCTS, LLC [US/US];
1120 Alza Dr., El Paso, Texas 79907 (US).

(72) Inventor: MORELAND, Carl W.; 93026 Applegate Trail,
Junction City, Oregon 97448 (US).

(74) Agent: MEYERS, William S.; FAEGRE BAKER
DANIELS LLP, 300 N. MERIDIAN ST., STE. 2700, Indi-
anapolis, Indiana 46204 (US).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,

KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a
patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the
earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

(54) Title: MULTI-FREQUENCY METAL DETECTOR

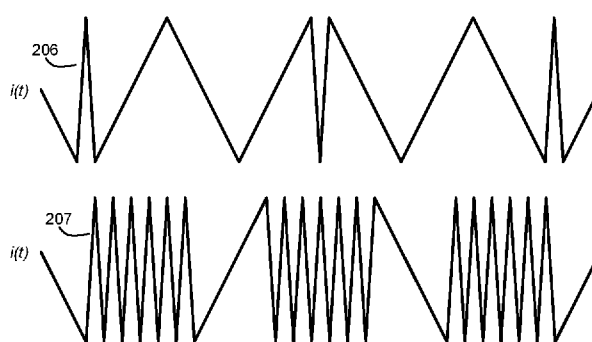


Fig. 7

(57) Abstract: A method of transmitting a magnetic field in a metal detector is provided. The method comprising receiving, by a plurality of switching elements connecting a supply voltage across one or more transmit inductance coils, one or more transmit clock signals; and in response to receiving the one or more transmit clock signals, driving current to the one or more transmit inductance coils by enabling the one or more of the plurality of switching elements to provide the supply voltage across the one or more transmit inductance coils causing a plurality of repeating sequences of currents to be applied through the one or more transmit inductance coils. Each of the repeating sequences of currents is associated with a frequency and provides half-slopes of current to the one or more transmit inductance coils. The half-slopes of current comprise a substantially linear positive-sloped half-slope of current and a substantially equal and linear negative-sloped half-slope of current.



MULTI-FREQUENCY METAL DETECTOR

Related Application

[0001] This application claims the benefit of US Provisional Application No. 62/524,234, filed June 23, 2017, titled MULTI-FREQUENCY METAL DETECTOR, docket FTH-0006-01-US, the entire disclosure of which is expressly incorporated by reference herein.

Field

[0002] The present disclosure relates to a metal detector capable of generating a variety of periodic transmit signals, including frequency selection and frequency weighting.

Background and Summary

[0003] Induction metal detectors are generally classified as either continuous-time (CT) (or so-called frequency-domain - FD) types or discrete-time (DT) (or time-domain - TD) types. CT types have traditionally utilized a continuous wave (CW) transmitter and CT demodulation. In most cases a single frequency metal detector transmits a sinusoidal current and utilizes continuous-time synchronous demodulation. The demodulation is typically performed using an in-phase and a quadrature-phase channel, which results in the ability to determine the amplitude and phase of the received signal. Because all of the received signal waveform is demodulated all the time, strong signal responses due to ground minerals cannot be eliminated at the demodulators, and must be dealt with in post-demodulator signal processing.

[0004] In time-domain detectors, particularly pulse induction (PI) types, demodulation is typically performed only on a portion of the received signal using DT methods. The PI detector also uses a DT transmit waveform, whereby the transmitter produces a short pulse of current followed by a longer period of zero current. Ferrite ground minerals decay much faster than typical target eddy current responses, so by slightly delaying the demodulation sampling beyond the turn-off point of the transmitter the response due to ferrite minerals can be substantially eliminated at the demodulator.

[0005] Multiple frequency metal detectors have utilized a combination of these approaches. In most cases, however, the transmit signal is based on a simple digitally switched

voltage applied to a coil. When a switched voltage is applied to an ideal coil the resulting current through the coil is described by

$$i(t) = \frac{1}{L} \int v(t) dt$$

[0006] For a constant voltage, the current is a linear ramp. If the voltage is switched between two DC levels then the coil current becomes a triangular waveform. An example of this approach is found in the “CZ”-series metal detectors produced by Fisher Research Labs. In the CZ, a 5 kHz square-wave voltage drive is applied to a transmit coil to produce a triangle wave current. A triangle wave is rich in odd-order harmonics; that is, it consists of a fundamental, a third harmonic, a fifth harmonic, etc. The resulting received signal is band pass-filtered at both the 5 kHz fundamental and the 15 kHz third harmonic; each frequency is then demodulated using CT quadrature demodulators. Because the coil current is a triangle wave, the fundamental signal strength at 5 kHz is nine times greater than the harmonic signal strength at 15 kHz.

[0007] A similar approach is found in the “DFX” metal detector produced by White’s Electronics. Instead of a simple square wave drive, a multi-period voltage drive creates a complex multi-ramp waveform, the intent of which is to more evenly balance the signal strengths produced at the low frequency (3 kHz) and the high frequency (15 kHz). The receiver still uses FD processing, whereby each frequency is band-pass filtered and demodulated using CT quadrature demodulators.

[0008] With both the CZ and the DFX both frequencies are transmitted concurrently and the receiver continuously demodulates both frequencies concurrently. These will be referred to as concurrent multi-frequency (CMF) designs. In both cases the transmit current waveform is a series of ramps, whereby the “frequencies” referred to in a “multi-frequency” metal detector consist of fundamental and harmonic energies of the signal. That is, the transmit signal “frequencies” are not pure sinusoidal frequencies, but pure sinusoidal frequencies can be extracted from the signal through the use of band pass filtering. Once a substantially sinusoidal frequency has been extracted, it can be demodulated and processed in essentially the same way as a single-frequency sinusoidal metal detector would do.

[0009] An alternative approach is found in the patents US5537041 and US5576624 which have been realized in multiple products (e.g. “Sovereign”) produced by Minelab Electronics. This method utilizes two distinct temporally-separated square wave frequencies to produce a single-cycle triangle wave current at 3.125 kHz, followed by 8 cycles of triangle wave current at 25 kHz. The received signal is temporally demodulated by separate low-frequency and high-frequency demodulators, but are done with DT quadrature demodulators. Because the low and high frequencies are sequentially transmitted and sequentially processed in the receiver, this method will be referred to as sequential multi-frequency (SMF). Another example is provided in US8063777.

[0010] Again, the transmit current waveform is a series of triangle waves, not sinusoids. Each triangle wave “frequency” consists of a fundamental frequency and its odd harmonics. Because SMF doesn’t easily lend itself to CT filtering and demodulation, it is normally processed using DT methods. As such, the demodulators of a given frequency channel are operated at the overall frequency of a particular triangle wave portion, which happens to also be its fundamental frequency.

[0011] Although SMF is most easily realized with a simple digital voltage driver that produces ramps or triangle waveforms, it can also be realized by use of sinusoidal currents. US5642050 and US5654638 describe a multi-frequency approach in which the transmit coil is resonated at multiple frequencies by switching in multiple resonant capacitors. Each frequency is then demodulated using a CT demodulator. The transition between frequencies is difficult and limits the practicality of this approach.

[0012] There are particular advantages of SMF over CMF. In CMF the frequencies must be odd-order harmonically related; that is, a fundamental and its odd-order harmonics. In SMF, there is no harmonic requirement. In CMF, the received signal must be band-pass filtered before demodulation to ensure each channel is processing only the desired channel frequency. In SMF, frequencies are separated temporally so that channel filtering is not required. Frequency selection with SMF is easier, since each frequency is produced with a simple square wave voltage, alternating between two or more frequencies. With CMF, timing must be carefully calculated to produce the desired frequencies, which is made more difficult if particular relative signal

strengths are desired. With SMF, it is a simple matter to produce 1, 2, 3, or even more frequencies, with each frequency being arbitrary. With CMF, selecting among 2 or more frequency sets requires predetermined transmit and demodulator waveforms that have little flexibility in terms of the desired frequencies.

[0013] SMF, as proposed in US5537041 and US5576624 and realized in Minelab products, has a significant shortcoming in that the transmitter switches between two fixed power supply voltages to produce both square wave drive frequencies. The result of this is that both frequencies have the same coil current slew rate, such that the high frequency peak current is one-eighth that of the low frequency. Minelab attempts to make up for the weaker high-frequency signal by repeating it eight times over, which theoretically equalizes the signal strengths. However, the practical result is that the high frequency transmit signal is still weaker, and products based on the technique are widely known to have weaker responses to low-conductive targets.

[0014] In an exemplary embodiment of the present disclosure, a method of transmitting a magnetic field in a metal detector is provided. The method comprising receiving, by a plurality of switching elements connecting a supply voltage across one or more transmit inductance coils, one or more transmit clock signals; and in response to receiving the one or more transmit clock signals, driving current to the one or more transmit inductance coils by enabling the one or more of the plurality of switching elements to provide the supply voltage across the one or more transmit inductance coils causing a plurality of repeating sequences of currents to be applied through the one or more transmit inductance coils. Each of the repeating sequences of currents is associated with a frequency and provides half-slopes of current to the one or more transmit inductance coils. The half-slopes of current comprise a substantially linear positive-sloped half-slope of current and a substantially equal and linear negative-sloped half-slope of current.

[0015] In an example thereof, the method further comprising dispersing a frequency associated with a first repeating sequence of current of the plurality of repeating sequences of current among other frequencies associated with other repeating sequences of currents of the plurality of repeating sequences of current.

[0016] In another example thereof, the plurality of half-slopes of current of a repeating sequence of current associated with a given frequency are sequential.

[0017] In yet another example thereof, the method further comprising selecting the number of plurality of repeating sequences of currents by a user.

[0018] In still another example thereof, the method further comprising selecting the frequency associated with each of the repeating sequences of currents by a user.

[0019] In a further example thereof, the method further comprising automatically selecting the frequencies in response to a preferred operating mode.

[0020] In yet a further example thereof, the method further comprising automatically selecting the frequencies in response to detecting operating conditions.

[0021] In still a further example, the method further comprising shifting all frequencies associated with the plurality of repeating sequences of current by a proportional amount, the proportional amount being less than 1%, to minimize interferers. In a variation thereof, the method further comprising selecting a frequency shift by a user. In another variation thereof, the method further comprising selecting a frequency shift by a detector in response to interference levels determined by a receiver circuit.

[0022] In yet sill a further example, the method further comprising independently shifting each frequency of the plurality of repeating sequences of current by an amount, the amount being less than 1%, to minimize interferers. In a variation thereof, the method further comprising selecting a frequency shift by a user. In another variation thereof, the method further comprising selecting a frequency shift by a detector in response to interference levels determined by a receiver circuit.

[0023] In another example thereof, the method further comprising balancing signal strengths of the plurality of frequencies associated with the plurality of repeating sequences of current such that their signal strengths as measured in a spectral measurement are approximately equal.

[0024] In a further example of thereof, the method further comprising intentionally unbalancing strengths of the plurality of frequencies associated with the plurality of repeating sequences of current to provide more signal strength to a more desired frequency than another.

In a variation thereof, the method further comprising selecting relative signal strengths of the plurality of frequencies by the user. In another variation thereof, the method further comprising automatically controlling relative signal strengths of the plurality of frequencies by the metal detector. In still another variation thereof, the method further comprising determining the relative signal strengths of the plurality of frequencies based on ground conditions.

[0025] In another yet example thereof, the supply voltage is a bipolar supply voltage.

[0026] In still another example thereof, the supply voltage is a unipolar supply voltage.

[0027] In yet another example thereof, the supply voltage includes an appropriate capacitor for power recycling.

[0028] In still yet another example thereof, residual non-linearities of the half-slopes of current of a given frequency associated with a first repeating sequence of current of the plurality of repeating sequences of current are compensated by variations in the corresponding power supply.

[0029] In a further yet example thereof, the method further comprising measuring peak current levels of driven current to the one or more transmit inductance coils, in which a measured peak current level is used to adjust a corresponding power supply voltage. In a variation thereof, the method further comprising adjusting the corresponding power supply voltage to compensate for coil manufacturing variations. In another variation thereof, the method further comprising adjusting the corresponding power supply voltage to compensate for ground mineralization. In a further example thereof, the plurality of switching elements include one or more high-side switching elements and one or more low-side switching elements. In a variation thereof, the low-side switching elements include NMOS devices. In another variation thereof, the low-side switching elements are driven by logic gates whose inputs are high-side clock signals of the one or more transmit clock signals. In still another variation thereof, the high-side switching elements include PMOS devices. In yet another variation thereof, the high-side switching elements include high-voltage reverse-conduction blocking elements. In a further variation thereof, a high-side switching element of the high-side switching elements is comprised of back-to-back PMOS devices. In a yet further variation, the one or more high-side switching elements is comprised of back-to-back NMOS devices.

[0030] In still another example thereof, the method further comprising a receiver circuit connected to one or more receive inductance coils, in which the one or more receive inductance coils produces one or more voltages in response to a received magnetic field signal, wherein the receiver circuit receives a receive demodulator clock signal to synchronously demodulate the one or more voltages to produce one or more demodulated outputs. In a variation thereof, a randomized timing jitter is applied to a transmit clock signal, and a coherent jitter is applied to the appropriate receiver demodulator clock signal. In another variation thereof, a frequency offset is applied to a transmit clock signal, and a coherent frequency offset is applied to the appropriate receiver demodulator clock signal. In a further variation thereof, the jitter or offset is applied to all frequencies. In still another variation thereof, the jitter or offset is applied to select frequencies.

[0031] In another exemplary embodiment of the present disclosure, a method of transmitting a plurality of frequencies with differing slew rates is provided. The method comprising in response to receiving a first clock, enabling a first switch and a second switch to provide a first positive voltage across a coil; in response to receiving a second clock, enabling a third switch and a fourth switch to provide a first negative voltage across the coil; in response to receiving a third clock, enabling a fifth switch and the second switch to provide a second positive voltage across the coil; and in response to receiving a fourth clock, enabling a sixth switch and the fourth switch to provide a second negative voltage across the coil.

[0032] In an example thereof, the second positive voltage is greater than the first positive voltage.

[0033] In yet another exemplary embodiment of the present disclosure, a method of transmitting a plurality of frequencies with differing slew rates is provided. The method comprising in response to receiving a first clock, enabling a first switch and a second switch to provide a first voltage across a coil in a first direction; in response to receiving a second clock, enabling a third switch and a fourth switch to provide the first voltage across the coil in a second direction; in response to receiving a third clock, enabling a fifth switch and the second switch to provide a second voltage across the coil in the first direction; and in response to receiving a

fourth clock, enabling a sixth switch and the fourth switch to provide the second voltage across the coil in the second direction.

[0034] In still another exemplary embodiment of the present disclosure, a method of transmitting a plurality of frequencies with differing slew rates is provided. The method comprising in response to receiving a first clock, enabling a first switch and a second switch to provide a positive low voltage across a coil; in response to receiving a second clock, enabling a third switch and a fourth switch to provide a negative low voltage across the coil; in response to receiving a third clock, enabling a fifth switch and a sixth switch to provide a positive high voltage across the coil; and in response to receiving a fourth clock, enabling a seventh switch and an eighth switch to provide a negative high voltage across the coil.

[0035] In still yet another exemplary embodiment of the present disclosure, a transmit circuit for transmitting at least a low frequency and a high frequency is provided. The transmit circuit comprising a coil with a first connection point and a second connection point, a low frequency switch circuit, and a high frequency switch circuit. The low frequency switch circuit comprising a first low frequency switch comprising a first low frequency input connection, a first low frequency output connection, and a first low frequency enable connection. The first low frequency input connection is electrically connected to a first low frequency voltage source. The first low frequency output connection is electrically connected to the first connection point of the coil. The first low frequency enable connection is electrically connected to a first low frequency clock source. The low frequency switch circuit further comprising a second low frequency switch comprising a second low frequency input connection, a second low frequency output connection, and a second low frequency enable connection. The second low frequency input connection is electrically connected to the first low frequency voltage source. The second low frequency output connection is electrically connected to the second connection point of the coil. The second low frequency enable connection is electrically connected to a second low frequency clock source. The low frequency switch circuit further comprising a third low frequency switch comprising a third low frequency input connection, a third low frequency output connection, and a third low frequency enable connection. The third low frequency input connection is electrically connected to a second low frequency voltage source. The third low frequency output

connection is electrically connected to the first connection point of the coil. The third low frequency enable connection is electrically connected to the second low frequency clock source. The low frequency switch circuit further comprising a fourth low frequency switch comprising a fourth low frequency input connection, a fourth low frequency output connection, and a fourth low frequency enable connection. The fourth low frequency input connection is electrically connected to the second low frequency voltage source. The fourth low frequency output connection is electrically connected to the second connection point of the coil. The fourth low frequency enable connection is electrically connected to the first low frequency clock source. The high frequency switch circuit comprising a first high frequency switch comprising a first high frequency input connection, a first high frequency output connection, and a first high frequency enable connection. The first high frequency input connection is electrically connected to a first high frequency voltage source. The first high frequency output connection is electrically connected to the first connection point of the coil. The first high frequency enable connection is electrically connected to a first high frequency clock source. The high frequency switch circuit further comprising a second high frequency switch comprising a second high frequency input connection, a second high frequency output connection, and a second high frequency enable connection. The second high frequency input connection is electrically connected to the first high frequency voltage source. The second high frequency output connection is electrically connected to the second connection point of the coil. The second high frequency enable connection is electrically connected to a second high frequency clock source. The high frequency switch circuit further comprising a third high frequency switch comprising a third high frequency input connection, a third high frequency output connection, and a third high frequency enable connection. The third high frequency input connection is electrically connected to a second high frequency voltage source. The third high frequency output connection is electrically connected to the first connection point of the coil. The third high frequency enable connection is electrically connected to the second high frequency clock source. The high frequency switch circuit further comprising a fourth high frequency switch comprising a fourth high frequency input connection, a fourth high frequency output connection, and a fourth high frequency enable connection. The fourth high frequency input connection is electrically connected to the second high frequency voltage source. The fourth high frequency

output connection is electrically connected to the second connection point of the coil. The fourth high frequency enable connection is electrically connected to the first high frequency clock source.

[0036] In a further exemplary embodiment of the present disclosure, a transmit circuit for transmitting at least a low frequency and a high frequency is provided. The transmit circuit comprising a coil with a first connection point and a second connection point; a low frequency switch circuit, a high frequency switching circuit, and a common switch circuit. The low frequency switch circuit comprising a first low frequency switch comprising a first low frequency input connection, a first low frequency output connection, and a first low frequency enable connection. The first low frequency input connection is electrically connected to a first low frequency voltage source. The first low frequency output connection is electrically connected to the first connection point of the coil. The first low frequency enable connection is electrically connected to a first low frequency clock source. The low frequency switch circuit further comprising a second low frequency switch comprising a second low frequency input connection, a second low frequency output connection, and a second low frequency enable connection. The second low frequency input connection is electrically connected to the first low frequency voltage source. The second low frequency output connection is electrically connected to the second connection point of the coil. The second low frequency enable connection is electrically connected to a second low frequency clock source. The high frequency switch circuit comprising a first high frequency switch comprising a first high frequency input connection, a first high frequency output connection, and a first high frequency enable connection. The first high frequency input connection is electrically connected to a first high frequency voltage source. The first high frequency output connection is electrically connected to the first connection point of the coil. The first high frequency enable connection is electrically connected to a first high frequency clock source. The high frequency switch circuit further comprising a second high frequency switch comprising a second high frequency input connection, a second high frequency output connection, and a second high frequency enable connection. The second high frequency input connection is electrically connected to the first high frequency voltage source. The second high frequency output connection is electrically connected to the second connection point of the coil. The second high frequency enable

connection is electrically connected to a second high frequency clock source. The common switch circuit comprising a first common switch comprising a first common input connection, a first common output connection, and a first common enable connection. The first common input connection is electrically connected to a first common voltage source. The first common output connection is electrically connected to the first connection point of the coil. The first common enable connection is electrically connected to the second low frequency clock source and the second high frequency clock source. The common switch circuit further comprising a second common switch comprising a second common input connection, a second common output connection, and a second common enable connection. The second common input connection is electrically connected to the first common voltage source. The second common output connection is electrically connected to the second connection point of the coil. The second common enable connection is electrically connected to the first low frequency clock source and the first high frequency clock source.

[0037] In an example thereof, the first common voltage source provides an electrical connection to ground.

[0038] Additional features of the present disclosure will become apparent to those skilled in the art upon consideration of the following detailed description of illustrative embodiments exemplifying the best mode of carrying out the invention as presently perceived.

Brief Description of the Drawings

[0039] The foregoing aspects and additional features of the present system and method will become more readily appreciated and become better understood by reference to the following detailed description when taken in conjunction with the accompanying drawings.

[0040] FIG. 1 illustrates a conventional H-bridge transmitter;

[0041] FIG. 2 illustrates a conventional single-period transmit waveform;

[0042] FIG. 3 illustrates a conventional two-period transmit waveform;

[0043] FIG. 4 illustrates a two-period scaled transmit waveform;

[0044] FIG. 5 illustrates an improved two-period scaled transmit waveform;

- [0045] FIG. 6 illustrates a dispersed two-period scaled transmit waveform;
- [0046] FIG. 7 illustrates weighted two-period scaled transmit waveforms;
- [0047] FIG. 8 illustrates a three-period scaled transmit waveform ;
- [0048] FIG. 9 illustrates a two-level H-bridge transmitter;
- [0049] FIG. 10 illustrates an improved two-level H-bridge transmitter;
- [0050] FIG. 11 illustrates coil current and clocking waveforms for an improved two-level H-bridge transmitter;
- [0051] FIG. 12 illustrates an example of a two-level H-bridge transmitter;
- [0052] FIG. 13 illustrates a two-level H-bridge transmitter with derived low-side clocks and coil current measurement;
- [0053] FIG. 14 illustrates a block diagram of a metal detector system utilizing described invention;
- [0054] Corresponding reference characters indicate corresponding parts throughout the several views. Although the drawings represent embodiments of various features and components according to the present disclosure, the drawings are not necessarily to scale and certain features may be exaggerated in order to better illustrate and explain the present disclosure.

Detailed Description of the Drawings

[0055] For the purposes of promoting an understanding of the principles of the present disclosure, reference will now be made to the embodiments illustrated in the drawings, which are described below. The embodiments disclosed below are not intended to be exhaustive or limit the invention to the precise form disclosed in the following detailed description. Rather, the embodiments are chosen and described so that others skilled in the art may utilize their teachings. It is understood that no limitation of the scope of the invention is thereby intended. The invention includes any alterations and further modifications in the illustrated devices and described methods and further applications of the principles of the invention which would normally occur to one skilled in the art to which the invention relates.

[0056] Fig. 1 shows a basic H-bridge driver 100 using MOSFETs 101, 102, 103, and 104 to drive current $i(t)$ through search coil inductor 105. With appropriate clock signals 106 and 107 applied it is possible to generate a continuous coil current waveform 108 as shown in Fig. 2. This represents a typical way in which to produce a multi-frequency transmit waveform. Although a full H-bridge is shown, and although MOSFET switches are shown, the driver could be implemented in a half-bridge circuit, and could utilize a variety of switching devices. The transmit current waveform 108 is indicative of that used in the Fisher CZ-series metal detectors.

[0057] It is possible to vary the clock rate to produce different “frequencies.” Fig. 3 shows a current waveform 109 consisting of a low frequency cycle followed by several high frequency cycles. The transmit drive voltages required to produce this signal are CLK1 (110) and CLK2 (111). This is the same as shown in US5537041 and utilized by Minelab in their multifrequency metal detectors such as the Sovereign and CTX3030. Although each “frequency” portion is a triangle wave rich in harmonic frequency content, the received signal is discrete-time demodulated and processed at the fundamental frequency of the corresponding triangle wave. Therefore, this would be regarded as a 2-frequency metal detector.

[0058] With only a single supply voltage the higher frequency triangle wave has the same slew rate as the lower frequency wave and so it has a proportionally lower peak current, requiring proportionally more timing cycles to produce a sufficiently strong (integrated) target response. Even so, the transmitted magnetic field, the target eddy currents, and the received signal strength from the target all scale with the peak coil current, and repetition only partially compensates for the weaker signal.

[0059] Furthermore, because the high-frequency component has the same slew rate as the low-frequency component, the target responses will essentially be identical, albeit truncated. That is, target eddy response is dependent on dB/dt , and for both low and high frequencies dB/dt is the same. The primary difference is in the duration of the current slopes, whereby the longer duration of the low frequency slope allows more time for high-conductor targets to fully respond.

[0060] The shortcomings can be solved by boosting the amplitude of the high frequency signal and achieving both a higher slew rate and a higher peak current. The waveform 201 in FIG. 4 is similar to the waveform 109 in FIG. 3 but with the peak currents equalized. It should be

noted that complete equalization of frequency peak currents is not necessary but for the purposes of discussion it will be assumed.

[0061] The waveform 201 in FIG. 4 is not preferable because the frequency change occurs in the middle of a current slope. It is preferable to change the slope at the peaks of the current slopes, where a slope polarity change is already occurring. FIG. 5 shows a 2-frequency example waveform 202 where the slope changes occur at the peaks.

[0062] In some situations it is furthermore advantageous to present the transmit waveform as an odd-symmetric waveform, as in waveform 203 in FIG. 6. Previously, a “frequency” was considered to be the fundamental frequency of a given triangle wave portion of the transmit waveform. Waveform 203 shows that “frequencies” can be dispersed as individual slopes. In this case, a “frequency” would correspond to twice the period of an individual slope. That is, if negative half-slope 204 has a duration of 100 microseconds (us), then when combined with a corresponding positive half-slope 205 with the same duration of 100us it would effect a complete cycle of a triangle wave with a period of 200us, which corresponds to a frequency of 5kHz.

[0063] If the high-frequency current peaks are now substantially equal to the low-frequency current peaks per waveform 203, there is more flexibility in choosing the relative number of repetitions. This could be done to balance the transmit signal strengths at the two frequencies as measured, for example, in a frequency spectral plot of the transmit signal. But it may be advantageous to boost one frequency signal strength over the other for a particular application or environmental conditions. FIG. 7 shows two such examples; waveform 206 shows a relatively higher contribution of the low frequency signal, and waveform 207 shows a relatively higher contribution of the high frequency signal. Selecting the contribution level might be controlled by the user, or it might be automatically controlled in response to e.g. ground conditions.

[0064] The technique discussed extends to any number of frequencies, typically 1 to 4 in a hand-held metal detector and possibly more in a geophysics application. Waveform 208 in FIG. 8 shows an example 3-frequency waveform.

[0065] The transmit driver 100 in FIG. 1 is sufficient to produce a transmit waveform with a single slew rate, such as waveforms 108 and 109. Multiple slew rates require multiple voltage drives, making the transmit circuitry more complex. FIG. 9 shows an exemplary transmit circuit 300 for transmitting two frequencies at two slew rates. For a low slew rate signal (low frequency), low voltages +VL and -VL are applied to coil 301 with switches 306 and 309 (controlled by clock CLKL1) for a rising (positive) current polarity, and with switches 307 and 308 (controlled by clock CLKL2) for a falling (negative) current polarity. For a high slew rate signal (high frequency), high voltages +VH and -VH are applied to coil 301 with switches 302 and 305 (controlled by clock CLKH1) for a rising (positive) current polarity, and with switches 303 and 304 (controlled by clock CLKH2) for a falling (negative) current polarity.

[0066] The switches 302-309 may be implemented in a variety of ways, including discrete devices like bipolar transistors or MOSFETs, integrated switching devices, or any combinations thereof. Power supply voltages may also be implemented in a variety of ways, but ideally should be substantially constant in value. Supply voltage values would be optimally selected to produce consistent peak coil currents for each frequency slew rate. That is, if the high frequency slew rate is four times the slew rate of the low frequency, the high voltages (+VH, -VH) would be four times higher than the low voltages (+VL, -VL). This is not an absolute requirement, and in reality the voltages could be set to other non-optimal values.

[0067] It is not necessary to employ bipolar supply voltages. FIG. 10 shows a simplified circuit 400 in which the -VL and -VH supplies are simply grounded. Circuit 400 performs the same operational function as circuit 300 but with fewer switches.

[0068] Furthermore, in circuit 300, low-side switches 304, 308 and 305, 309 are combined into low-side switches 404 and 405, respectively, in circuit 400. This slightly simplifies the circuit at the expense of slightly more complex timing, although the timing signals for the low-side switches 404 and 405 can be derived by logically combining the clocks for the high-side switches. FIG. 11 shows an example coil current waveform 410 and the clocking signals required to achieve it. Although the implementation discussed so far is described in terms of two frequencies, it can be expanded to more frequencies with additional high-side switches and power supply voltages. A particular example would be the use of 5V, 20V, and 80V to

achieve 4.5kHz, 18kHz, and 72kHz respectively. While additional frequencies require more high-side switches and power supply voltages, they do not require additional low-side switches; devices 404 and 405 will suffice for any number of frequencies.

[0069] In the aforementioned example, the selection of a 1mH transmit coil inductance would result in a peak-to-peak current of about 556mA. Regardless of the use of bipolar or unipolar supply voltages, it is not necessary for each power supply to have a current capacity equal to the peak dynamic current. Because the polarity of the coil current changes direction at each transition point (whether or not that transition point also produces a frequency change), coil current can be efficiently recycled by connecting an appropriate tank capacitor across each of the power supply voltages. At the instance beyond the transition point, the collapsing magnetic field provides a charging current into the capacitor, up to the point where the coil current falls to zero. Beyond that point, the same capacitor then provides current back to the coil for the remainder of the current slope, from zero current to the peak current at the next transition point. Ohmic losses in the coil, switches, and capacitor prevent complete power recycling, but this method provides for a highly efficient means for a large number of frequencies over a very wide range of frequencies. It is important to select a capacitor value that minimizes ramp non-linearities.

[0070] Although there are many ways to implement the switches in circuit 400, a preferred way is with MOSFET devices. FIG. 12 shows an example circuit 500 using NMOS transistors for the low-side switches 504, 505 and PMOS transistors for the high-side switches 502, 503, 506, 507. Those skilled in the arts will recognize that such an arrangement has a flaw in that the intrinsic body diodes of PMOS devices 506, 507 will get turned on by the application of +VH when PMOS devices 502, 503 are switched on, respectively. There are again many ways in which to mitigate this problem, including the use of high-voltage selectable blocking devices like inverted NMOS transistors, or by using high-side switches implemented with back-to-back PMOS or NMOS devices. There are many solutions to this issue, and these solutions are anticipated and within the scope of the present disclosure.

[0071] The required signals for CLKN1 and CLKN2 can be derived using logic gates applied to the high-side clock signals. FIG. 13 shows NAND gates 601, 602 creating the required low-side clocks. This simplifies clocking requirements to just the high-side switches. It is

possible to invert the entire circuitry so that the multiple voltages and multiple switches are on the low side, and the common switches are on the high side.

[0072] Circuit 600 in FIG. 13 also includes current measurement element 603 which may be used to monitor the peak current amplitudes of the various frequencies and make adjustments to the power supply voltages. This can be useful in compensating for slight manufacturing variations in the inductance of the transmit coil, or to compensate for variable ground conditions.

[0073] Metal detectors which employ an inductive coil for receiving target responses are also prone to receiving EMI, particularly EMI from a 50Hz or 60Hz electrical mains. A common way of minimizing the effect of mains interference is to carefully select a transmit frequency which is an exact multiple of the mains frequency, such that the signal from the mains EMI demodulates to a DC offset in the receiver demodulators. This offset is then filtered out. Because of the difficulty of exactly hitting a multiple of the mains frequency, many detectors instead choose a multiple-and-a-half of the mains frequency. This places the demodulated EMI signal at an offset of half the mains frequency (i.e., 30Hz for a 60Hz mains) away from the target's synchronously demodulated response, and is filtered out using low-pass filters.

[0074] A shortcoming of this method is that, while the mains frequency is very accurate over a long period of time, it can vary a fraction of a percent over a matter of hours. This can be enough to place its harmonic-and-a-half multiple inside the bandwidth of the aforementioned low-pass filter and cause interference. Indeed, it is not uncommon for a metal detectorist to have little interference one day and significant interference the next, all at the same location.

[0075] Many metal detectors offer a "frequency offset" control whereby, either manually or automatically, the transmit frequency is very slightly shifted, often by fractions of a percent, to move a demodulated interferer out-of-band. The amount of frequency shift is not sufficient to cause a meaningful difference in target responses. This technique can be effective in minimizing a particular interferer, but may be completely ineffective when multiple interferers are present. In previous multi-frequency metal detectors, including CMF and SMF, the frequency offset was applied proportionally to all frequencies. That is, a 3kHz + 15kHz detector might be shifted by +1% to produce 3.03kHz + 15.15kHz. Maintaining proportional frequency offsets is required in CMF, but not necessarily in SMF.

[0076] A preferred solution is to apply a random timing jitter to the transmit waveform, and to apply the same (coherent) jitter to the receiver demodulators. This approach does not work when using CT demodulators as either the in-phase or quadrature-phase demodulator signal (or both) will be corrupted. However, the method presented here, with the use of DT receiver demodulators, allows the use of intentional coherent jitter to randomize and reduce EMI effects. It should be noted that while the application of jitter slightly alters the transmitted frequencies in a strict sense, in a practical sense it is not enough to alter the target responses in a meaningful way, and so the transmitted “frequencies” are considered to be effectively unaltered.

[0077] Because the frequencies in SMF are independent of each other, the frequency offset — whether a fixed offset or a random jitter — applied to each frequency may also be independent. It is only important that the receiver demodulators which correspond to the shifted frequency also be shifted by an appropriate amount.

[0078] FIG. 14 shows an application of the invention to a metal detection system 700, in this example using three frequencies. Transmit circuit 704 creates a three frequency transmit waveform current applied to transmit coil 701, in response to the clock signals generated by timing block 705. Receive coil 702 receives target responses as magnetic anomalies and converts the magnetic responses to either a voltage or a current signal; amplifier 706 amplifies the received signal and applies it to demodulators 707, 708, and 709.

[0079] Each demodulator corresponds to one of the three frequencies and receives timing signals from timing block 705 that correspond to the proper frequency of concern. While a given demodulator block is labeled as an “I/Q demod” it may, in fact, consist of 1, 2, or more individual demodulators. It is also possible to create mixed-frequency demodulators where, for example, the reactive components from 2 or more frequencies are demodulated together to create a composite reactive signal.

[0080] The various demodulator signals may or may not be further processed in the analog domain, then digitized by ADC 710 and processed with digital signal processing block 711 to create audible and visual responses for the operator. DSP block 711 can also modify operating parameters of timing block 705 in response to the analysis of the demodulated signals for e.g. ground conditions.

[0081] User interface 712 may be incorporated to allow the user to manually control various aspects of the system as described, such as the selection of the operating frequencies or the relative weightings thereof. The user interface may be implemented using a traditional method such as an integrated keypad and LCD, or via a linked computer, or via a remote unit such as a wired or wireless device, including a cell phone app.

[0082] In one example, a method of transmitting a magnetic field in a metal detector, comprises: receiving, by a plurality of switching elements connecting a supply voltage across one or more transmit inductance coils, one or more transmit clock signals; in response to receiving the one or more transmit clock signals, driving current to the one or more transmit inductance coils by enabling the one or more of the plurality of switching elements to provide the supply voltage across the one or more transmit inductance coils causing a plurality of repeating sequences of currents to be applied through the one or more transmit inductance coils, wherein each of the repeating sequences of currents is associated with a frequency and provides half-slopes of current to the one or more transmit inductance coils, wherein the half-slopes of current comprise a substantially linear positive-sloped half-slope of current and a substantially equal and linear negative-sloped half-slope of current.

[0083] In one example, the method comprises dispersing a frequency associated with a first repeating sequence of current of the plurality of repeating sequences of current among other frequencies associated with other repeating sequences of currents of the plurality of repeating sequences of current. In another example, the plurality of half-slopes of current of a repeating sequence of current associated with a given frequency are sequential.

[0084] In one example the method includes selecting the number of plurality of repeating sequences of currents by a user. In another example the method includes selecting the frequency associated with each of the repeating sequences of currents by a user. In yet another example the method includes automatically selecting the frequencies in response to a preferred operating mode. In one example the method includes automatically selecting the frequencies in response to detecting operating conditions.

[0085] In one example, the method includes shifting all frequencies associated with the plurality of repeating sequences of current by a proportional amount, the proportional amount

being less than 1%, to minimize interferers. In one example, the method includes independently shifting each frequency of the plurality of repeating sequences of current by an amount, the amount being less than 1%, to minimize interferers. In one example, the method includes selecting a frequency shift by a user. In one example, the method includes selecting a frequency shift by a detector in response to interference levels determined by a receiver circuit.

[0086] In one example the method includes balancing signal strengths of the plurality of frequencies associated with the plurality of repeating sequences of current such that their signal strengths as measured in a spectral measurement are approximately equal.

[0087] In one example the method includes intentionally unbalancing strengths of the plurality of frequencies associated with the plurality of repeating sequences of current to provide more signal strength to a more desired frequency than another. For example, the method can include selecting relative signal strengths of the plurality of frequencies by the user.

[0088] In another example, the method can include automatically controlling relative signal strengths of the plurality of frequencies by the metal detector. In yet another example, the method includes determining the relative signal strengths of the plurality of frequencies based on ground conditions.

[0089] In one example, the supply voltage is a bipolar supply voltage. In another example, the supply voltage is a unipolar supply voltage. In yet another example, the supply voltage includes an appropriate capacitor for power recycling.

[0090] In one example, residual non-linearities of the half-slopes of current of a given frequency associated with a first repeating sequence of current of the plurality of repeating sequences of current are compensated by variations in the corresponding power supply.

[0091] One example includes measuring peak current levels of driven current to the one or more transmit inductance coils, in which a measured peak current level is used to adjust a corresponding power supply voltage. One example includes adjusting the corresponding power supply voltage to compensate for coil manufacturing variations. One example includes adjusting the corresponding power supply voltage to compensate for ground mineralization.

[0092] In one example, the plurality of switching elements include one or more high-side switching elements and one or more low-side switching elements. In one example, the low-side switching elements include NMOS devices. In one example, the low-side switching elements are driven by logic gates whose inputs are high-side clock signals of the one or more transmit clock signals. In one example, the high-side switching elements include PMOS devices. In one example, the high-side switching elements include high-voltage reverse-conduction blocking elements. In one example, a high-side switching element of the high-side switching elements is comprised of back-to-back PMOS devices. In one example, the one or more high-side switching elements is comprised of back-to-back NMOS devices.

[0093] In one example, a receiver circuit is connected to one or more receive inductance coils, wherein the one or more receive inductance coils produces one or more voltages in response to a received magnetic field signal, wherein the receiver circuit receives a receive demodulator clock signal to synchronously demodulate the one or more voltages to produce one or more demodulated outputs.

[0094] In one example, a randomized timing jitter is applied to a transmit clock signal, and a coherent jitter is applied to the appropriate receiver demodulator clock signal. In one example, a frequency offset is applied to a transmit clock signal, and a coherent frequency offset is applied to the appropriate receiver demodulator clock signal. In one example, the jitter or offset is applied to all frequencies. In another example, the jitter or offset is applied to select frequencies.

[0095] In one example, a method of transmitting a plurality of frequencies with differing slew rates comprises: in response to receiving a first clock, enabling a first switch and a second switch to provide a first positive voltage across a coil; in response to receiving a second clock, enabling a third switch and a fourth switch to provide a first negative voltage across the coil; in response to receiving a third clock, enabling a fifth switch and the second switch to provide a second positive voltage across the coil; and in response to receiving a fourth clock, enabling a sixth switch and the fourth switch to provide a second negative voltage across the coil. In one example, the second positive voltage is greater than the first positive voltage. In one example, the absolute value of the second negative voltage is greater than the absolute value of the first

negative voltage. In one example, the first positive voltage and the first negative voltage can be provided by a first voltage source, and the second positive voltage and the second negative voltage can be provided by a second voltage source.

[0096] In another example method of transmitting a plurality of frequencies with differing slew rates, the method comprises: in response to receiving a first clock, enabling a first switch and a second switch to provide a first voltage across a coil in a first direction; in response to receiving a second clock, enabling a third switch and a fourth switch to provide the first voltage across the coil in a second direction; in response to receiving a third clock, enabling a fifth switch and the second switch to provide a second voltage across the coil in the first direction; and response to receiving a fourth clock, enabling a sixth switch and the fourth switch to provide the second voltage across the coil in the second direction.

[0097] In yet another example method of transmitting a plurality of frequencies with differing slew rates, the method comprises: in response to receiving a first clock, enabling a first switch and a second switch to provide a positive low voltage across a coil; in response to receiving a second clock, enabling a third switch and a fourth switch to provide a negative low voltage across the coil; in response to receiving a third clock, enabling a fifth switch and a sixth switch to provide a positive high voltage across the coil; and in response to receiving a fourth clock, enabling a seventh switch and an eighth switch to provide a negative high voltage across the coil.

[0098] In one example transmit circuit for transmitting at least a low frequency and a high frequency, the transmit circuit comprises: a coil with a first connection point and a second connection point, and a low frequency switch circuit comprising a first low frequency switch comprising a first low frequency input connection, a first low frequency output connection, and a first low frequency enable connection wherein: the first low frequency input connection is electrically connected to a first low frequency voltage source; the first low frequency output connection is electrically connected to the first connection point of the coil; and the first low frequency enable connection is electrically connected to a first low frequency clock source.

[0099] The a low frequency switch circuit further includes a second low frequency switch comprising a second low frequency input connection, a second low frequency output

connection, and a second low frequency enable connection wherein: the second low frequency input connection is electrically connected to the first low frequency voltage source; the second low frequency output connection is electrically connected to the second connection point of the coil; and the second low frequency enable connection is electrically connected to a second low frequency clock source.

[00100] The a low frequency switch circuit also includes a third low frequency switch comprising a third low frequency input connection, a third low frequency output connection, and a third low frequency enable connection, wherein: the third low frequency input connection is electrically connected to a second low frequency voltage source; the third low frequency output connection is electrically connected to the first connection point of the coil; and the third low frequency enable connection is electrically connected to the second low frequency clock source.

[00101] The low frequency switch circuit further includes a fourth low frequency switch comprising a fourth low frequency input connection, a fourth low frequency output connection, and a fourth low frequency enable connection, wherein: the fourth low frequency input connection is electrically connected to the second low frequency voltage source; the fourth low frequency output connection is electrically connected to the second connection point of the coil; and the fourth low frequency enable connection is electrically connected to the first low frequency clock source.

[00102] The example transmit circuit also includes a high frequency switch circuit comprising a first high frequency switch comprising a first high frequency input connection, a first high frequency output connection, and a first high frequency enable connection wherein: the first high frequency input connection is electrically connected to a first high frequency voltage source; the first high frequency output connection is electrically connected to the first connection point of the coil; and the first high frequency enable connection is electrically connected to a first high frequency clock source.

[00103] The high frequency switch circuit also includes a second high frequency switch comprising a second high frequency input connection, a second high frequency output connection, and a second high frequency enable connection wherein: the second high frequency input connection is electrically connected to the first high frequency voltage source; the second

high frequency output connection is electrically connected to the second connection point of the coil; and the second high frequency enable connection is electrically connected to a second high frequency clock source.

[00104] The high frequency switch circuit further includes a third high frequency switch comprising a third high frequency input connection, a third high frequency output connection, and a third high frequency enable connection, wherein: the third high frequency input connection is electrically connected to a second high frequency voltage source; the third high frequency output connection is electrically connected to the first connection point of the coil; and the third high frequency enable connection is electrically connected to the second high frequency clock source.

[00105] The high frequency switch circuit also includes a fourth high frequency switch comprising a fourth high frequency input connection, a fourth high frequency output connection, and a fourth high frequency enable connection, wherein: the fourth high frequency input connection is electrically connected to the second high frequency voltage source; the fourth high frequency output connection is electrically connected to the second connection point of the coil; and the fourth high frequency enable connection is electrically connected to the first high frequency clock source.

[00106] In another example transmit circuit for transmitting at least a low frequency and a high frequency, the transmit circuit comprises a coil with a first connection point and a second connection point, and a low frequency switch circuit comprising a first low frequency switch comprising a first low frequency input connection, a first low frequency output connection, and a first low frequency enable connection wherein: the first low frequency input connection is electrically connected to a first low frequency voltage source; the first low frequency output connection is electrically connected to the first connection point of the coil; and the first low frequency enable connection is electrically connected to a first low frequency clock source.

[00107] The low frequency switch circuit also includes a second low frequency switch comprising a second low frequency input connection, a second low frequency output connection, and a second low frequency enable connection wherein: the second low frequency input connection is electrically connected to the first low frequency voltage source; the second low

frequency output connection is electrically connected to the second connection point of the coil; and the second low frequency enable connection is electrically connected to a second low frequency clock source.

[00108] The transmit circuit further comprises a high frequency switch circuit comprising a first high frequency switch comprising a first high frequency input connection, a first high frequency output connection, and a first high frequency enable connection wherein: the first high frequency input connection is electrically connected to a first high frequency voltage source; the first high frequency output connection is electrically connected to the first connection point of the coil; and the first high frequency enable connection is electrically connected to a first high frequency clock source.

[00109] The high frequency switch circuit also comprises a second high frequency switch comprising a second high frequency input connection, a second high frequency output connection, and a second high frequency enable connection wherein: the second high frequency input connection is electrically connected to the first high frequency voltage source; the second high frequency output connection is electrically connected to the second connection point of the coil; and the second high frequency enable connection is electrically connected to a second high frequency clock source.

[00110] The transmit circuit also comprises a common switch circuit comprising a first common switch comprising a first common input connection, a first common output connection, and a first common enable connection wherein: the first common input connection is electrically connected to a first common voltage source; the first common output connection is electrically connected to the first connection point of the coil; and the first common enable connection is electrically connected to the second low frequency clock source and the second high frequency clock source. In one example, the first common voltage source provides an electrical connection to ground.

[00111] The transmit circuit also comprises a second common switch comprising a second common input connection, a second common output connection, and a second common enable connection wherein: the second common input connection is electrically connected to the first common voltage source; the second common output connection is electrically connected to the

second connection point of the coil; and the second common enable connection is electrically connected to the first low frequency clock source and the first high frequency clock source.

[00112] While embodiments of the present disclosure have been described as having exemplary designs, the present invention may be further modified within the spirit and scope of this disclosure. This application is therefore intended to cover any variations, uses, or adaptations of the disclosure using its general principles. Further, this application is intended to cover such departures from the present disclosure as come within known or customary practice in the art to which this invention pertains.

CLAIMS:

1. A method of transmitting a magnetic field in a metal detector, comprising:
receiving, by a plurality of switching elements connecting a supply voltage across one or more transmit inductance coils, one or more transmit clock signals; and
in response to receiving the one or more transmit clock signals, driving current to the one or more transmit inductance coils by enabling the one or more of the plurality of switching elements to provide the supply voltage across the one or more transmit inductance coils causing a plurality of repeating sequences of currents to be applied through the one or more transmit inductance coils wherein each of the repeating sequences of currents is associated with a frequency and provides half-slopes of current to the one or more transmit inductance coils , wherein the half-slopes of current comprise a substantially linear positive-sloped half-slope of current and a substantially equal and linear negative-sloped half-slope of current.
2. The method in Claim 1 comprising dispersing a frequency associated with a first repeating sequence of current of the plurality of repeating sequences of current among other frequencies associated with other repeating sequences of currents of the plurality of repeating sequences of current.
3. The method in Claim 1, in which the plurality of half-slopes of current of a repeating sequence of current associated with a given frequency are sequential.
4. The method in Claim 1 comprising selecting the number of plurality of repeating sequences of currents by a user.
5. The method in Claim 1 comprising selecting the frequency associated with each of the repeating sequences of currents by a user.
6. The method in Claim 1 comprising automatically selecting the frequencies in response to a preferred operating mode.

7. The method in Claim 1 comprising automatically selecting the frequencies in response to detecting operating conditions.
8. The method in Claim 1 comprising shifting all frequencies associated with the plurality of repeating sequences of current by a proportional amount, the proportional amount being less than 1%, to minimize interferers.
9. The method in Claim 1, comprising independently shifting each frequency of the plurality of repeating sequences of current by an amount, the amount being less than 1%, to minimize interferers.
10. The method in Claim 8 or Claim 9, comprising selecting a frequency shift by a user.
11. The method in Claim 8 or Claim 9, comprising selecting a frequency shift by a detector in response to interference levels determined by a receiver circuit.
12. The method in Claim 1, comprising balancing signal strengths of the plurality of frequencies associated with the plurality of repeating sequences of current such that their signal strengths as measured in a spectral measurement are approximately equal.
13. The method in Claim 1, comprising intentionally unbalancing strengths of the plurality of frequencies associated with the plurality of repeating sequences of current to provide more signal strength to a more desired frequency than another.
14. The method in Claim 13, comprising selecting relative signal strengths of the plurality of frequencies by the user.
15. The method in Claim 13, comprising automatically controlling relative signal strengths of the plurality of frequencies by the metal detector.

16. The method in Claim 15, comprising determining the relative signal strengths of the plurality of frequencies based on ground conditions.
17. The method in Claim 1, in which the supply voltage is a bipolar supply voltage.
18. The method in Claim 1, in which the supply voltage is a unipolar supply voltage.
19. The method in Claim 1, in which the supply voltage includes an appropriate capacitor for power recycling.
20. The method in Claim 1, in which residual non-linearities of the half-slopes of current of a given frequency associated with a first repeating sequence of current of the plurality of repeating sequences of current are compensated by variations in the corresponding power supply.
21. The method in Claim 1, comprising measuring peak current levels of driven current to the one or more transmit inductance coils, in which a measured peak current level is used to adjust a corresponding power supply voltage.
22. The method of Claim 21, comprising adjusting the corresponding power supply voltage to compensate for coil manufacturing variations.
23. The method of Claim 21, comprising adjusting the corresponding power supply voltage to compensate for ground mineralization.
24. The method in Claim 1, in which the plurality of switching elements include one or more high-side switching elements and one or more low-side switching elements.
25. The method in Claim 24, in which the low-side switching elements include NMOS devices.

26. The method in Claim 25, in which the low-side switching elements are driven by logic gates whose inputs are high-side clock signals of the one or more transmit clock signals.
27. The method in Claim 24, in which the high-side switching elements include PMOS devices.
28. The method in Claim 27, in which the high-side switching elements include high-voltage reverse-conduction blocking elements.
29. The method in Claim 27, in which a high-side switching element of the high-side switching elements is comprised of back-to-back PMOS devices.
30. The method in Claim 24, in which the one or more high-side switching elements is comprised of back-to-back NMOS devices.
31. The method in Claim 1, comprising a receiver circuit connected to one or more receive inductance coils, in which the one or more receive inductance coils produces one or more voltages in response to a received magnetic field signal, wherein the receiver circuit receives a receive demodulator clock signal to synchronously demodulate the one or more voltages to produce one or more demodulated outputs.
32. The method in Claim 31, whereby a randomized timing jitter is applied to a transmit clock signal, and a coherent jitter is applied to the appropriate receiver demodulator clock signal.
33. The method in Claim 31, whereby a frequency offset is applied to a transmit clock signal, and a coherent frequency offset is applied to the appropriate receiver demodulator clock signal.
34. The method in Claim 32 or Claim 30, whereby the jitter or offset is applied to all frequencies.

35. The method in Claim 32 or Claim 30, whereby the jitter or offset is applied to select frequencies.
36. A method of transmitting a plurality of frequencies with differing slew rates comprising:
in response to receiving a first clock, enabling a first switch and a second switch to provide a first positive voltage across a coil;
in response to receiving a second clock, enabling a third switch and a fourth switch to provide a first negative voltage across the coil;
in response to receiving a third clock, enabling a fifth switch and the second switch to provide a second positive voltage across the coil; and
in response to receiving a fourth clock, enabling a sixth switch and the fourth switch to provide a second negative voltage across the coil.
37. The method of claim 36 wherein the second positive voltage is greater than the first positive voltage.
38. A method of transmitting a plurality of frequencies with differing slew rates comprising:
in response to receiving a first clock, enabling a first switch and a second switch to provide a first voltage across a coil in a first direction;
in response to receiving a second clock, enabling a third switch and a fourth switch to provide the first voltage across the coil in a second direction;
in response to receiving a third clock, enabling a fifth switch and the second switch to provide a second voltage across the coil in the first direction; and
in response to receiving a fourth clock, enabling a sixth switch and the fourth switch to provide the second voltage across the coil in the second direction.
39. A method of transmitting a plurality of frequencies with differing slew rates comprising:
in response to receiving a first clock, enabling a first switch and a second switch to provide a positive low voltage across a coil;

in response to receiving a second clock, enabling a third switch and a fourth switch to provide a negative low voltage across the coil;

in response to receiving a third clock, enabling a fifth switch and a sixth switch to provide a positive high voltage across the coil; and

in response to receiving a fourth clock, enabling a seventh switch and an eighth switch to provide a negative high voltage across the coil.

40. A transmit circuit for transmitting at least a low frequency and a high frequency comprising:

a coil with a first connection point and a second connection point;

a low frequency switch circuit comprising:

a first low frequency switch comprising a first low frequency input connection, a first low frequency output connection, and a first low frequency enable connection wherein:

the first low frequency input connection is electrically connected to a first low frequency voltage source;

the first low frequency output connection is electrically connected to the first connection point of the coil; and

the first low frequency enable connection is electrically connected to a first low frequency clock source;

a second low frequency switch comprising a second low frequency input connection, a second low frequency output connection, and a second low frequency enable connection wherein:

the second low frequency input connection is electrically connected to the first low frequency voltage source;

the second low frequency output connection is electrically connected to the second connection point of the coil; and

the second low frequency enable connection is electrically connected to a second low frequency clock source;

a third low frequency switch comprising a third low frequency input connection, a third low frequency output connection, and a third low frequency enable connection, wherein:

the third low frequency input connection is electrically connected to a second low frequency voltage source;

the third low frequency output connection is electrically connected to the first connection point of the coil; and

the third low frequency enable connection is electrically connected to the second low frequency clock source;

a fourth low frequency switch comprising a fourth low frequency input connection, a fourth low frequency output connection, and a fourth low frequency enable connection, wherein:

the fourth low frequency input connection is electrically connected to the second low frequency voltage source;

the fourth low frequency output connection is electrically connected to the second connection point of the coil; and

the fourth low frequency enable connection is electrically connected to the first low frequency clock source; and

a high frequency switch circuit comprising:

a first high frequency switch comprising a first high frequency input connection, a first high frequency output connection, and a first high frequency enable connection wherein:

the first high frequency input connection is electrically connected to a first high frequency voltage source;

the first high frequency output connection is electrically connected to the first connection point of the coil; and

the first high frequency enable connection is electrically connected to a first high frequency clock source;

a second high frequency switch comprising a second high frequency input connection, a second high frequency output connection, and a second high frequency enable connection wherein:

the second high frequency input connection is electrically connected to the first high frequency voltage source;

the second high frequency output connection is electrically connected to the second connection point of the coil; and

the second high frequency enable connection is electrically connected to a second high frequency clock source;

a third high frequency switch comprising a third high frequency input connection, a third high frequency output connection, and a third high frequency enable connection, wherein:

the third high frequency input connection is electrically connected to a second high frequency voltage source;

the third high frequency output connection is electrically connected to the first connection point of the coil; and

the third high frequency enable connection is electrically connected to the second high frequency clock source;

a fourth high frequency switch comprising a fourth high frequency input connection, a fourth high frequency output connection, and a fourth high frequency enable connection, wherein:

the fourth high frequency input connection is electrically connected to the second high frequency voltage source;

the fourth high frequency output connection is electrically connected to the second connection point of the coil; and

the fourth high frequency enable connection is electrically connected to the first high frequency clock source.

41. A transmit circuit for transmitting at least a low frequency and a high frequency comprising:
a coil with a first connection point and a second connection point;

a low frequency switch circuit comprising:

a first low frequency switch comprising a first low frequency input connection, a first low frequency output connection, and a first low frequency enable connection wherein:

the first low frequency input connection is electrically connected to a first low frequency voltage source;

the first low frequency output connection is electrically connected to the first connection point of the coil; and

the first low frequency enable connection is electrically connected to a first low frequency clock source; and

a second low frequency switch comprising a second low frequency input connection, a second low frequency output connection, and a second low frequency enable connection wherein:

the second low frequency input connection is electrically connected to the first low frequency voltage source;

the second low frequency output connection is electrically connected to the second connection point of the coil; and

the second low frequency enable connection is electrically connected to a second low frequency clock source;

a high frequency switch circuit comprising:

a first high frequency switch comprising a first high frequency input connection, a first high frequency output connection, and a first high frequency enable connection wherein:

the first high frequency input connection is electrically connected to a first high frequency voltage source;

the first high frequency output connection is electrically connected to the first connection point of the coil; and

the first high frequency enable connection is electrically connected to a first high frequency clock source;

a second high frequency switch comprising a second high frequency input connection, a second high frequency output connection, and a second high frequency enable connection wherein:

the second high frequency input connection is electrically connected to the first high frequency voltage source;

the second high frequency output connection is electrically connected to the second connection point of the coil; and

the second high frequency enable connection is electrically connected to a second high frequency clock source; and

a common switch circuit comprising:

a first common switch comprising a first common input connection, a first common output connection, and a first common enable connection wherein:

the first common input connection is electrically connected to a first common voltage source;

the first common output connection is electrically connected to the first connection point of the coil; and

the first common enable connection is electrically connected to the second low frequency clock source and the second high frequency clock source; and

a second common switch comprising a second common input connection, a second common output connection, and a second common enable connection wherein:

the second common input connection is electrically connected to the first common voltage source;

the second common output connection is electrically connected to the second connection point of the coil; and

the second common enable connection is electrically connected to the first low frequency clock source and the first high frequency clock source.

42. The transmit circuit of claim 41, wherein the first common voltage source provides an electrical connection to ground.

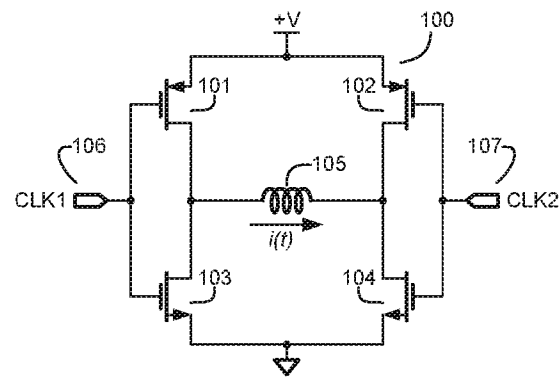


Fig. 1 (Prior art)

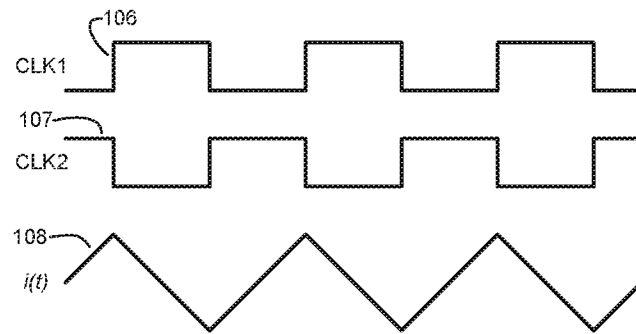


Fig. 2 (Prior art)

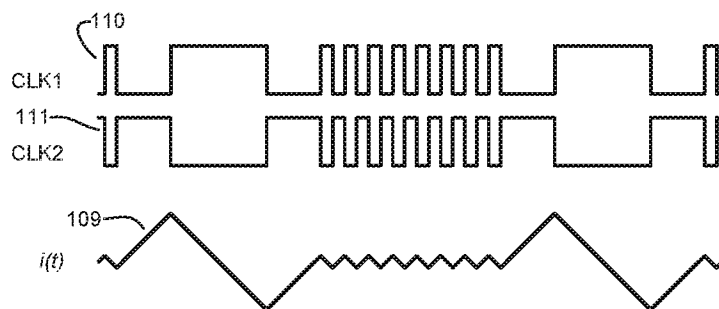


Fig. 3 (Prior art)

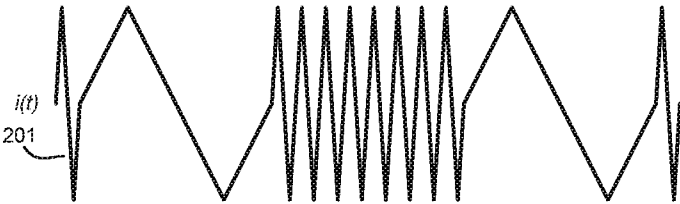


Fig. 4

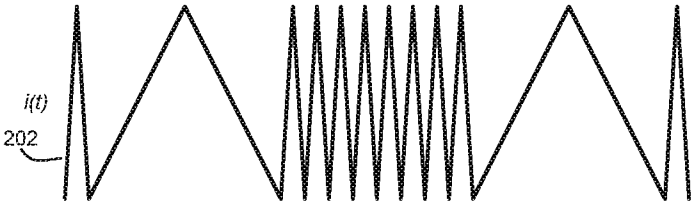


Fig. 5

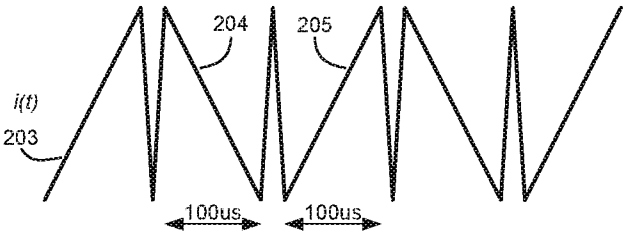


Fig. 6

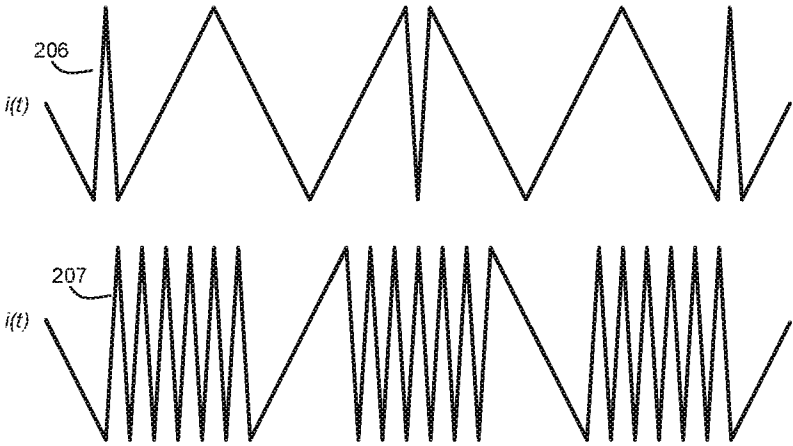


Fig. 7



Fig. 8

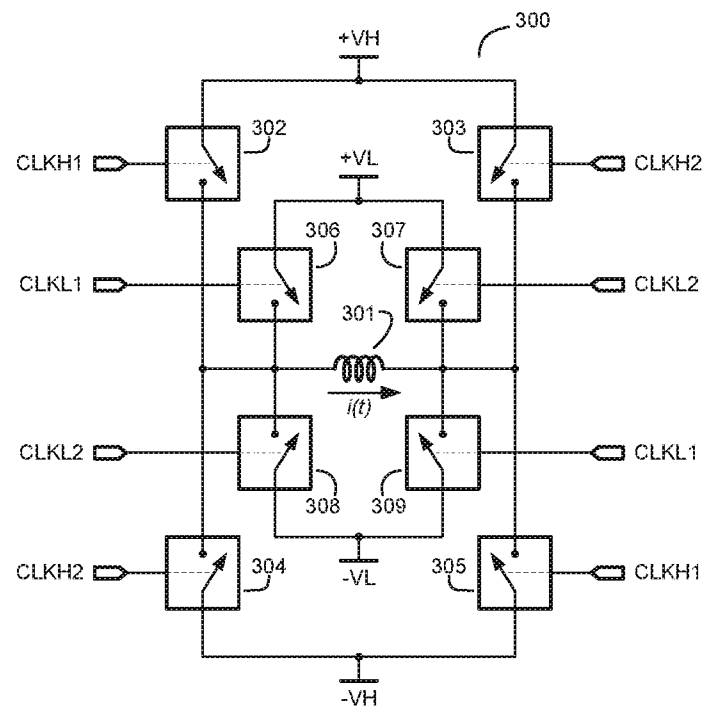


Fig. 9

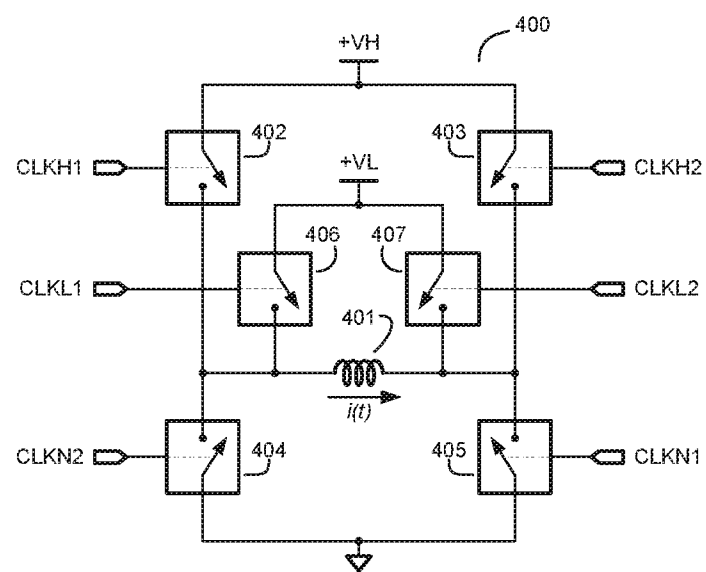


Fig. 10

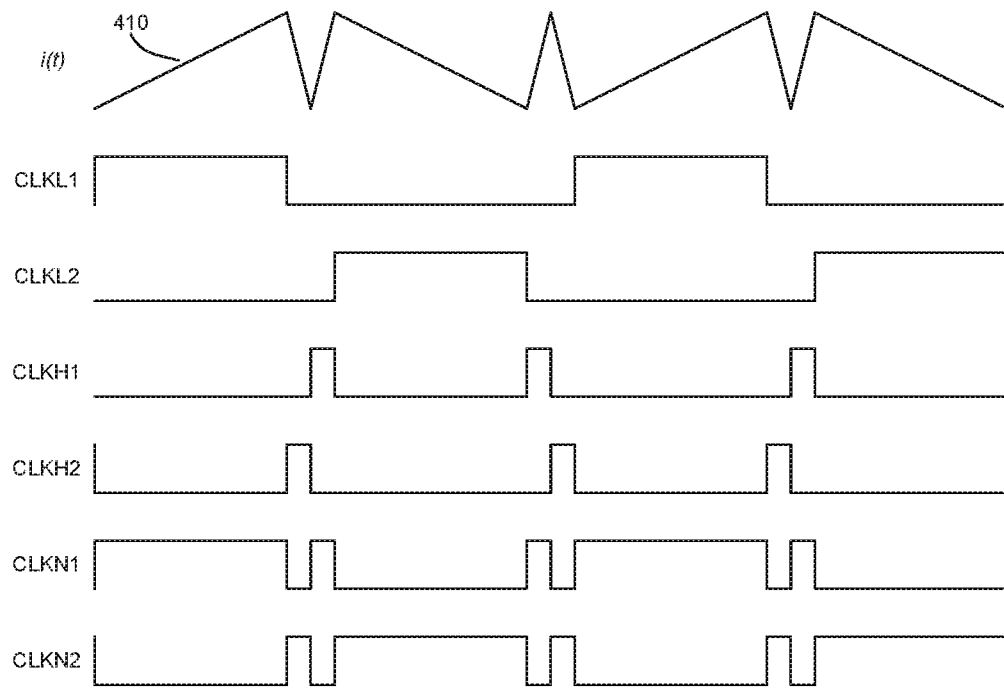


Fig. 11

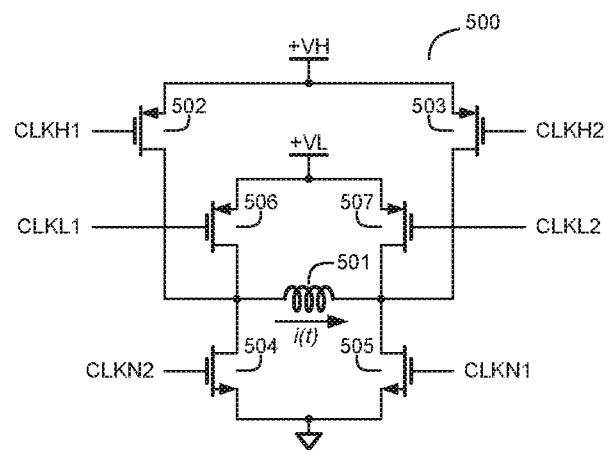


Fig. 12

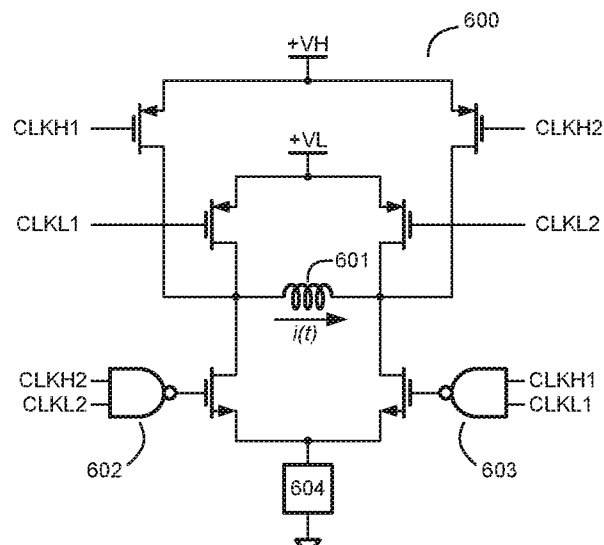


Fig. 13

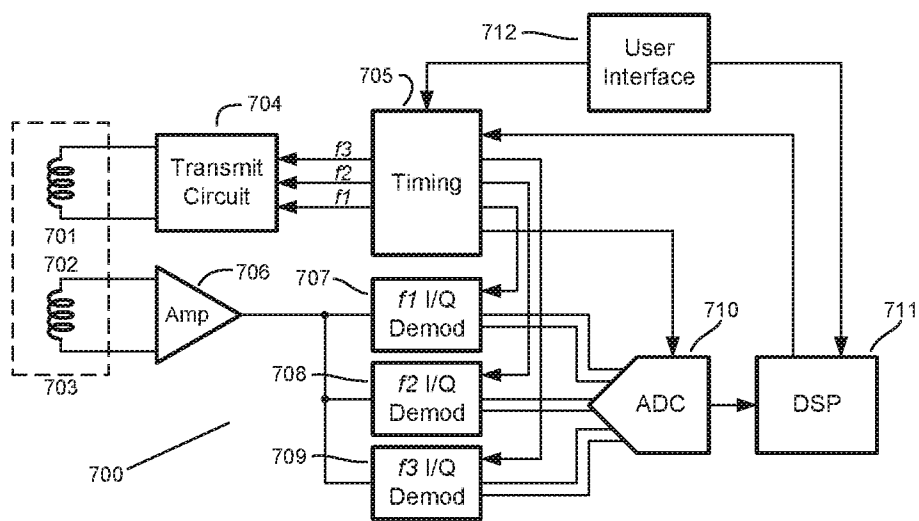


Fig. 14

INTERNATIONAL SEARCH REPORT

 International application No.
PCT/US2018/038766

A. CLASSIFICATION OF SUBJECT MATTER

G01V 3/10 (2006.01) G01N 27/72 (2006.01) G01R 33/12 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PATENW, Google and Google Scholar:

IPC/CPC: G01V3/10/LOW/IC/C/CNO; G01N27/72/LOW/IC/C/CNO; G01R33/12/LOW/IC/C/CNO

Keywords: metal detector, inductance, inductor, coil, triangle wave, current, mirror frequency, slope, gradient, positive, negative, half-slope, peak, repeat sequence, pulse, signal, current, transistor, NMOS, PMOS, clock generator, signal and similar terms

PATENW, Internal databases provided by IP Australia, Google and Google Scholar: Applicant/Inventor name search

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 14 September 2018	Date of mailing of the international search report 14 September 2018
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaustalia.gov.au	Authorised officer Boris Cetinich AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. +61399359619

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
the subject matter listed in Rule 39 on which, under Article 17(2)(a)(i), an international search is not required to be carried out, including
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See Supplemental Box for Details

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-35

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		PCT/US2018/038766
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013/0154649 A1 (MINELAB ELECTRONICS PTY LTD) 20 June 2013 whole document	1-35
A	WO 2005/047932 A1 (BHC CONSULTING PTY LTD) 26 May 2005 whole document	1-35
A	US 9,285,496 B1 (WHITE'S ELECTRONICS INC) 15 March 2016 whole document	1-35
A	US 8,629,677 B2 (WHITE'S ELECTRONICS INC) 14 January 2014 whole document	1-35
A	US 6,724,191 B1 (LARSEN) 20 April 2004 whole document	1-35

Form PCT/ISA/210 (fifth sheet) (January 2015)

Supplemental Box**Continuation of: Box III**

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

This Authority has found that there are different inventions based on the following features that separate the claims into distinct groups:

- Claims 1-35 are directed towards a method of transmitting a magnetic field in a metal detector. The feature of providing "half-slopes of current to the one or more transmit inductance coils, wherein the half-slopes of current comprise a substantially linear positive-sloped half-slope of current and a substantially equal and linear negative-sloped half-slope of current" comprises the first distinguishing feature.
- Claims 36-39 are directed a method of transmitting a plurality of frequencies with differing slew rates. The feature of "in response to receiving a fourth clock, enabling a sixth switch and the fourth switch to provide a second negative voltage across the coil" comprises the second distinguishing feature.
- Claims 40-42 are directed towards a transmit circuit for transmitting at least a low frequency and a high frequency. The feature of the "the second common enable connection is electrically connected to the first low frequency clock source and the first high frequency clock source" comprises the third distinguishing feature.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

When there is no special technical feature common to all the claimed inventions there is no unity of invention.

In the above groups of claims, the identified features may have the potential to make a contribution over the prior art but are not common to all the claimed inventions and therefore cannot provide the required technical relationship. The only feature common to all of the claimed inventions and which provides a technical relationship among them is "switching elements".

However this feature does not make a contribution over the prior art because it is disclosed in:

D1: US 2013/0154649 A1 (MINELAB ELECTRONICS PTY LTD) 20 June 2013 [abstract, paragraphs 47-49 and figure 3]

Therefore in the light of this document this common feature cannot be a special technical feature. Therefore there is no special technical feature common to all the claimed inventions and the requirements for unity of invention are consequently not satisfied *a posteriori*.

INTERNATIONAL SEARCH REPORT		International application No.	
Information on patent family members		PCT/US2018/038766	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
US 2013/0154649 A1	20 June 2013	US 2013154649 A1	20 Jun 2013
		US 9250348 B2	02 Feb 2016
WO 2005/047932 A1	26 May 2005	WO 2005047932 A1	26 May 2005
		AU 2004290091 A1	26 May 2005
		AU 2004290091 B2	18 Feb 2010
		US 2008074114 A1	27 Mar 2008
		US 7652477 B2	26 Jan 2010
US 9,285,496 B1	15 March 2016	US 9285496 B1	15 Mar 2016
US 8,629,677 B2	14 January 2014	US 2011316541 A1	29 Dec 2011
		US 8629677 B2	14 Jan 2014
		AU 2011203055 A1	19 Jan 2012
		AU 2011203055 B2	05 Feb 2015
US 6,724,191 B1	20 April 2004	US 6724191 B1	20 Apr 2004
		US 2004196045 A1	07 Oct 2004
		US 7123016 B2	17 Oct 2006
		US 2006238199 A1	26 Oct 2006
		US 7355409 B2	08 Apr 2008
		US 2008309344 A1	18 Dec 2008
		US 7705598 B2	27 Apr 2010
End of Annex			
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.			
Form PCT/ISA/210 (Family Annex)(January 2015)			