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YAMAZAKI et al.

(54) SEMICONDUCTOR DEVICE

(71) Applicant: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.**, Atsugi-shi (JP)

(72) Inventors: **Shunpei YAMAZAKI**, Setagaya (JP); **Daisuke MATSUBAYASHI**, Atsugi (JP); **Yutaka OKAZAKI**, Isehara (JP)

(73) Assignee: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.**, Atsugi-shi (JP)

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H01L 29/786 (2006.01)

(52) **U.S. Cl.**
CPC *H01L 29/78696* (2013.01)
USPC **257/43**

(57) **ABSTRACT**

A transistor in which a short-channel effect is not substantially caused and which has switching characteristics even in the case where the channel length is short is provided. Further, a highly integrated semiconductor device including the transistor is provided. A short-channel effect which is caused in a transistor including silicon is not substantially caused in the transistor including an oxide semiconductor film. The channel length of the transistor including the oxide semiconductor film is greater than or equal to 5 nm and less than 60 nm, and the channel width thereof is greater than or equal to 5 nm and less than 200 nm. At this time, the channel width is made 0.5 to 10 times as large as the channel length.

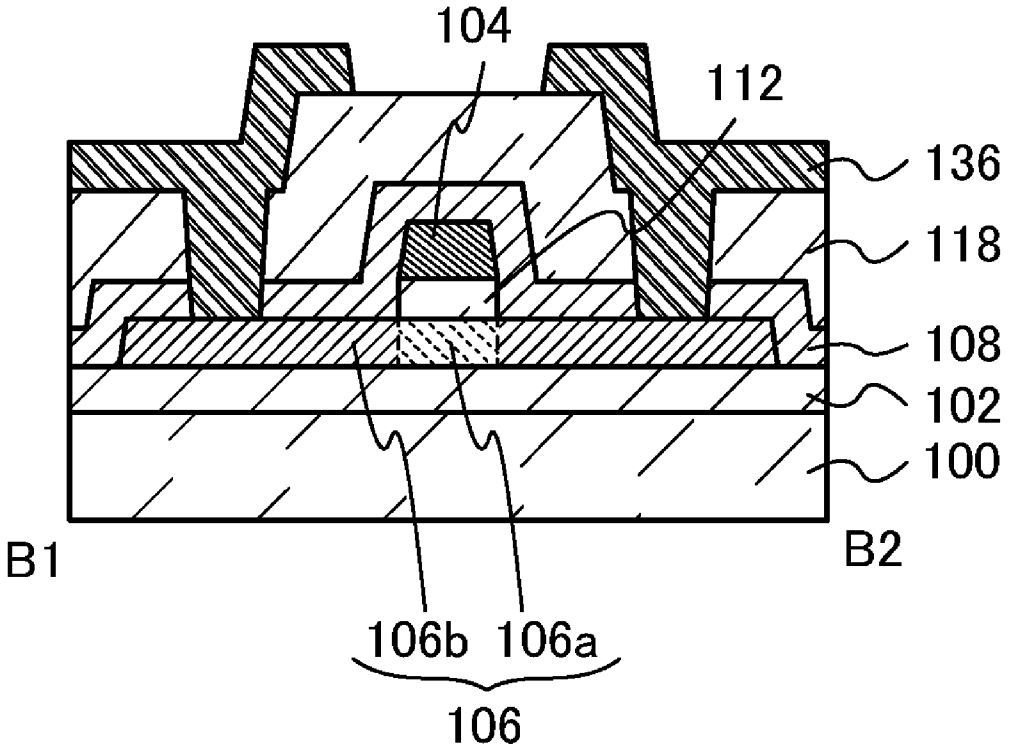


FIG. 1A

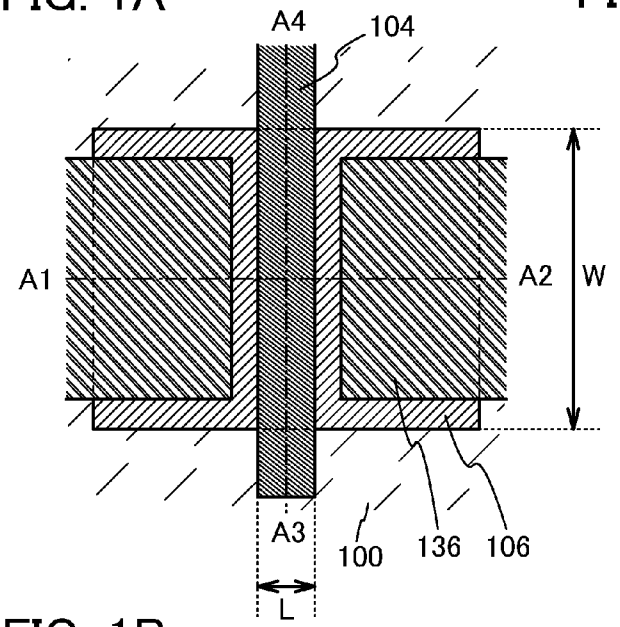


FIG. 1C

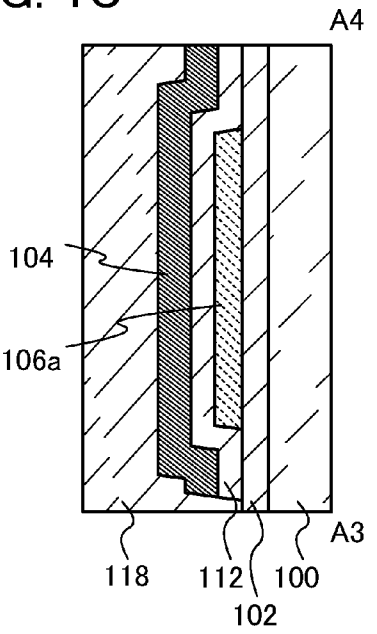


FIG. 1B

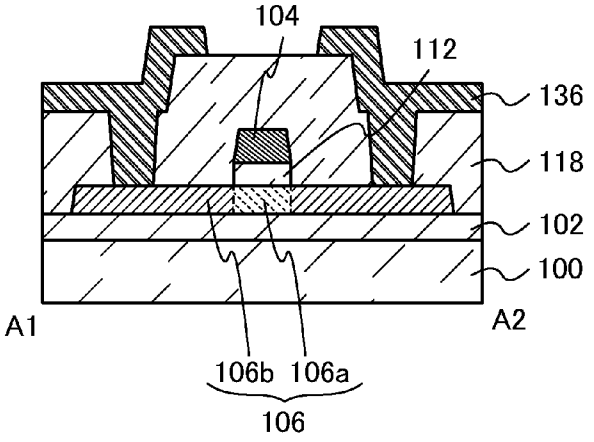


FIG. 2A

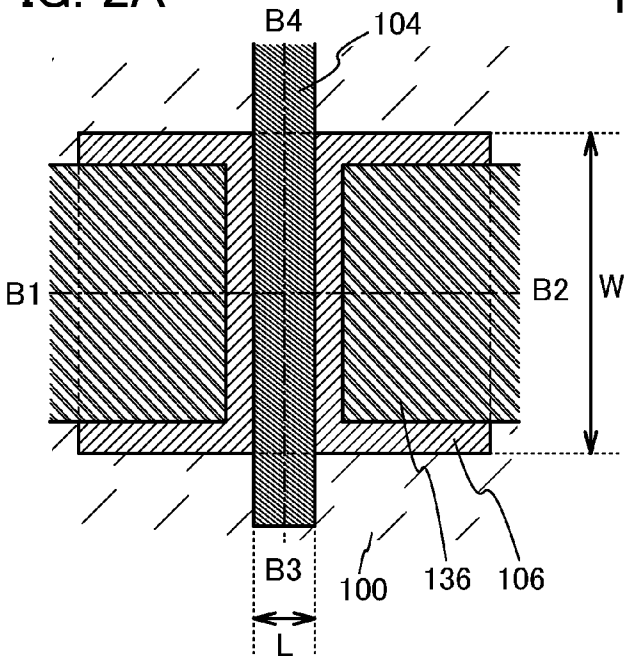


FIG. 2C

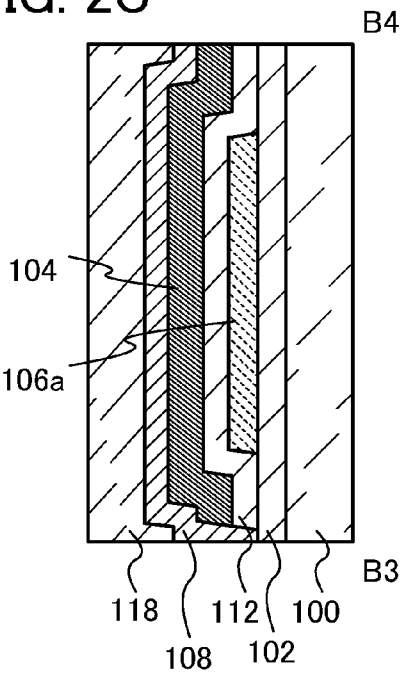


FIG. 2B

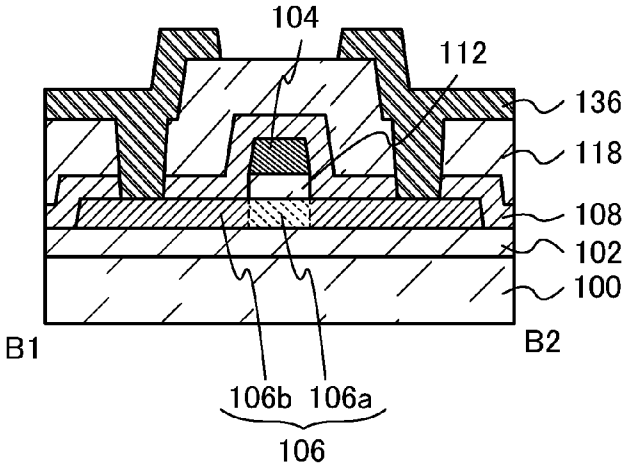


FIG. 3A

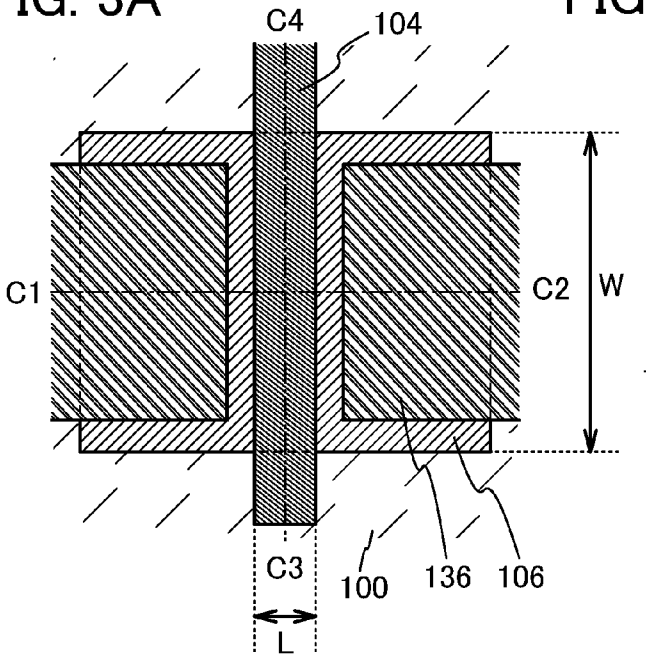


FIG. 3C

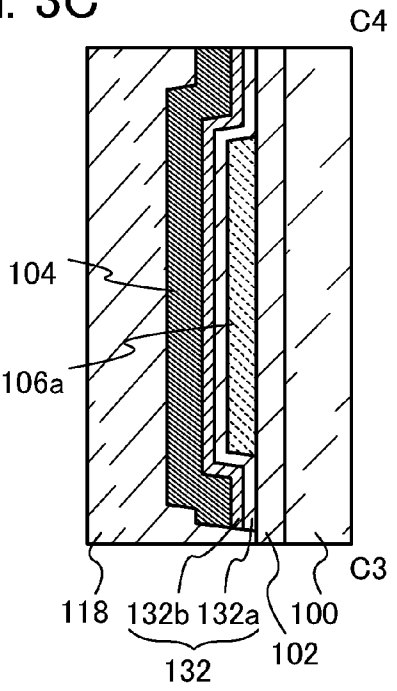


FIG. 3B

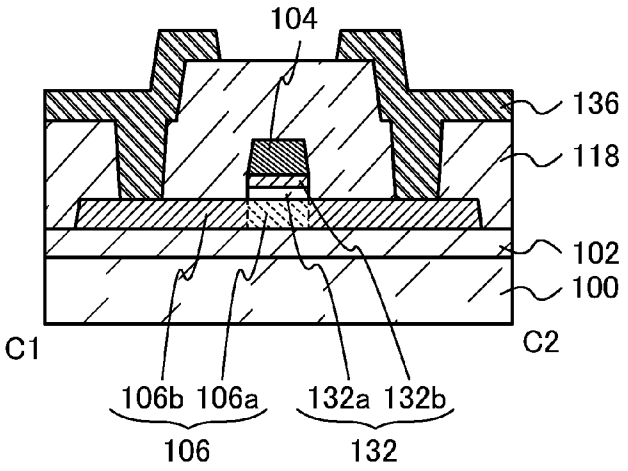


FIG. 4A

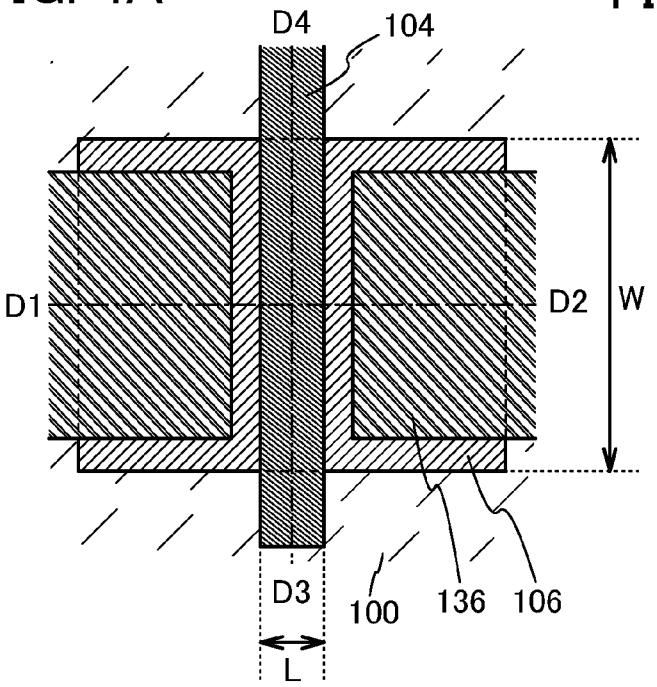


FIG. 4C

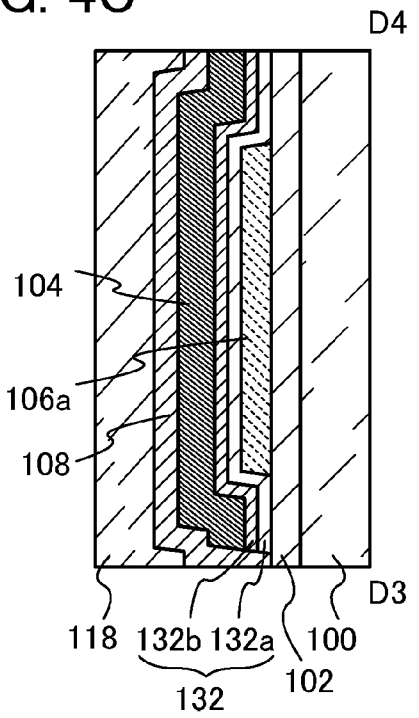


FIG. 4B

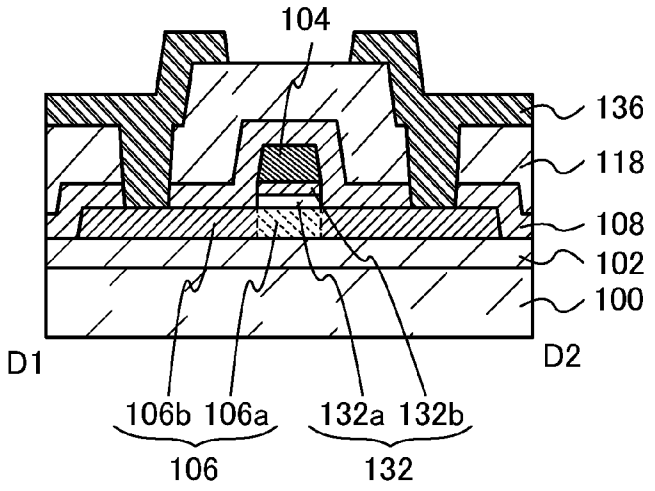


FIG. 5A

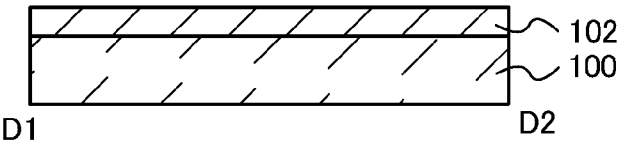


FIG. 5B

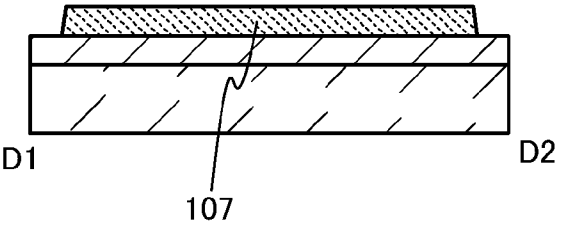


FIG. 5C

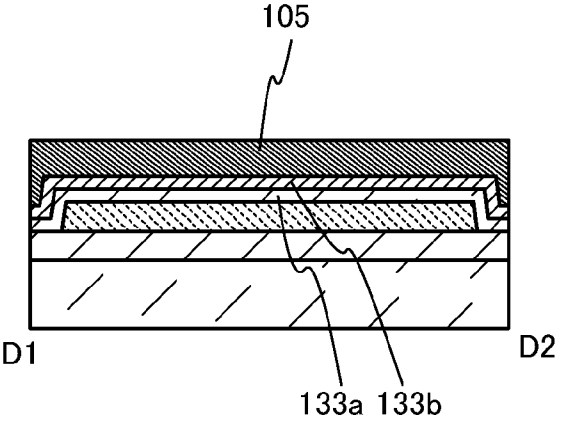


FIG. 6A

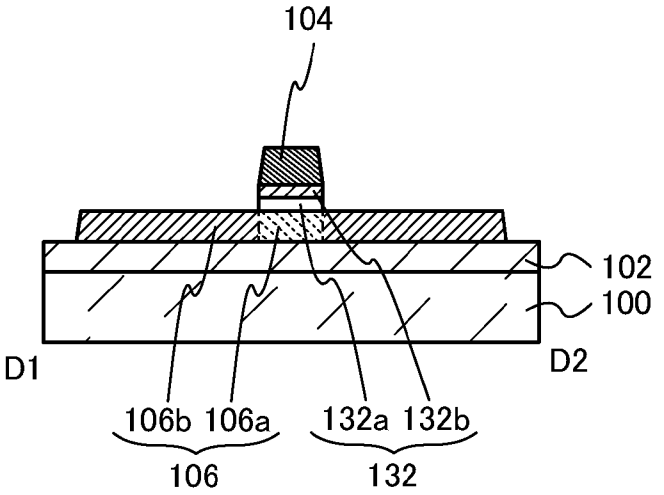


FIG. 6B

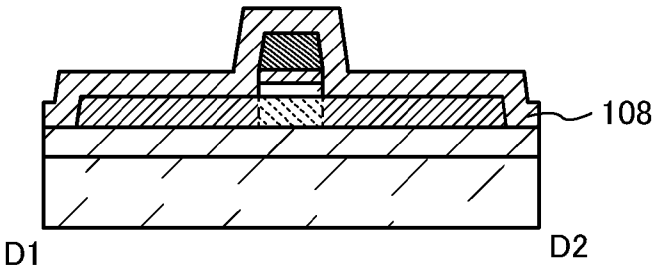


FIG. 6C

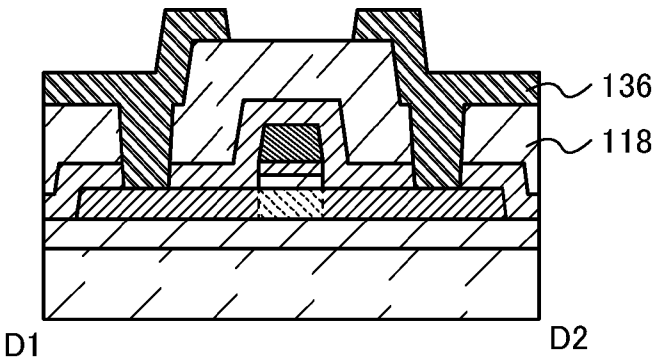


FIG. 7A

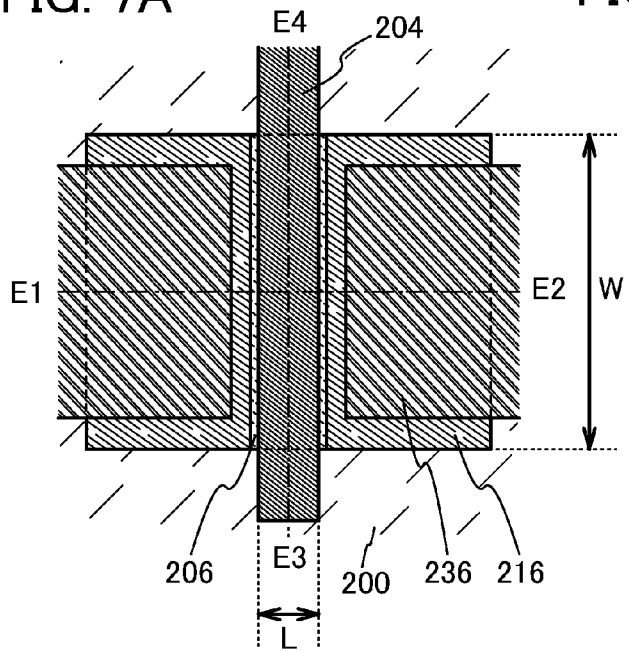


FIG. 7C

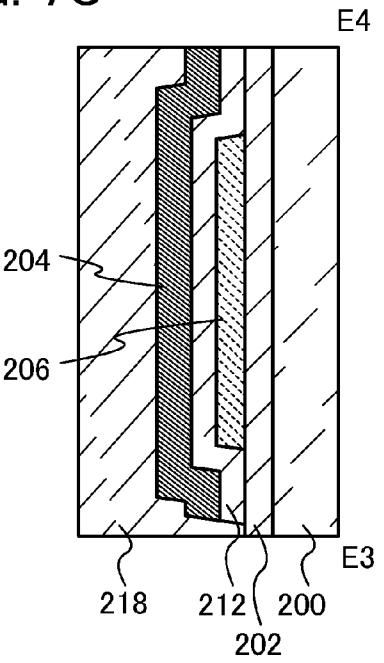


FIG. 7B

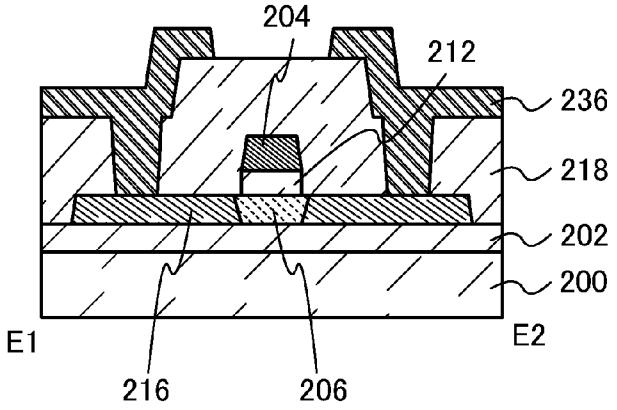


FIG. 8A

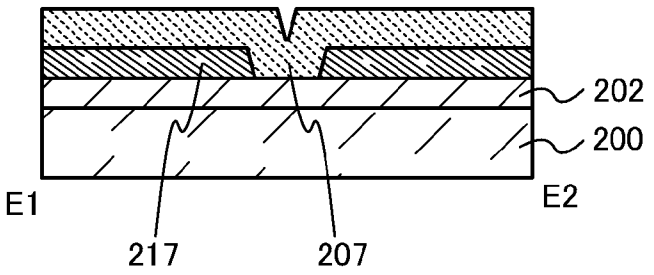
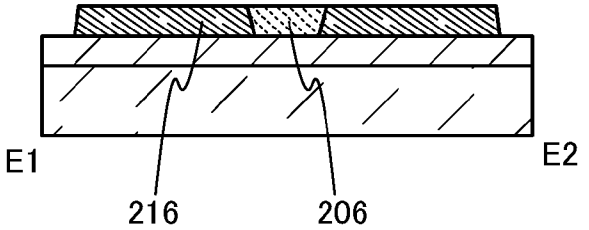


FIG. 8B



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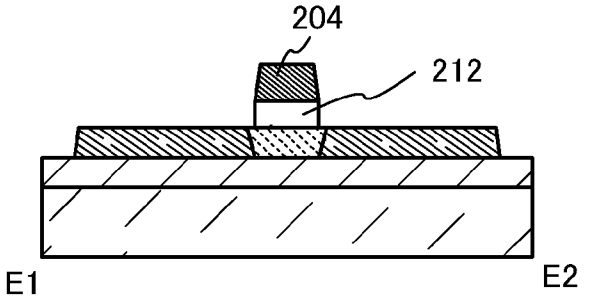


FIG. 8D

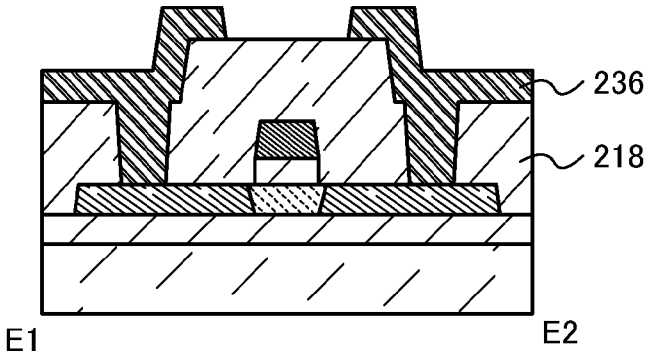


FIG. 9A

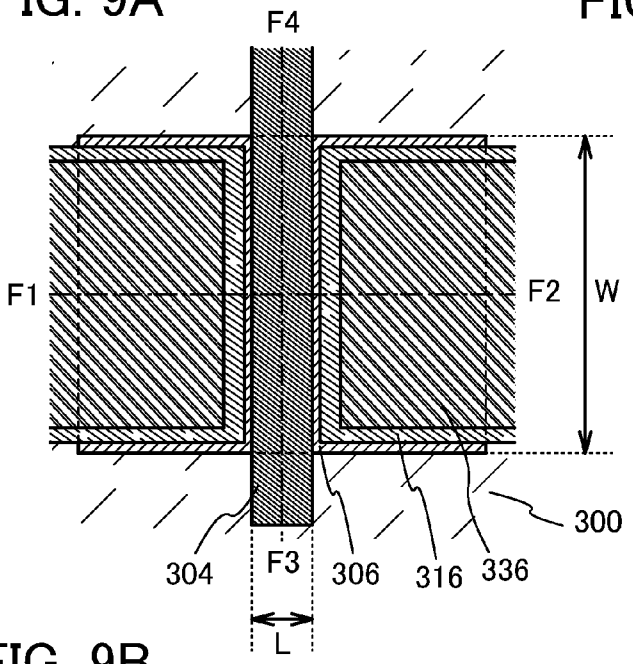


FIG. 9C

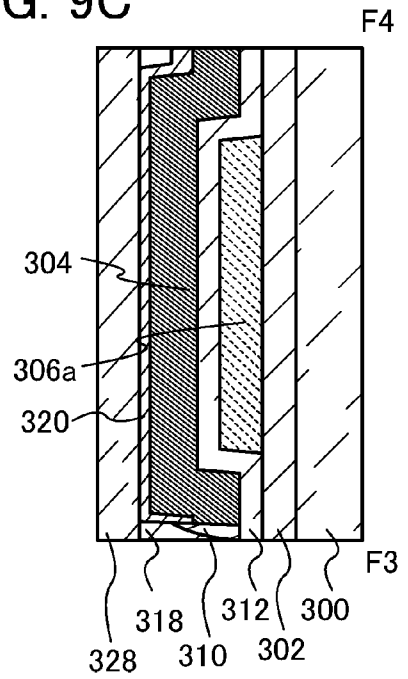


FIG. 9B

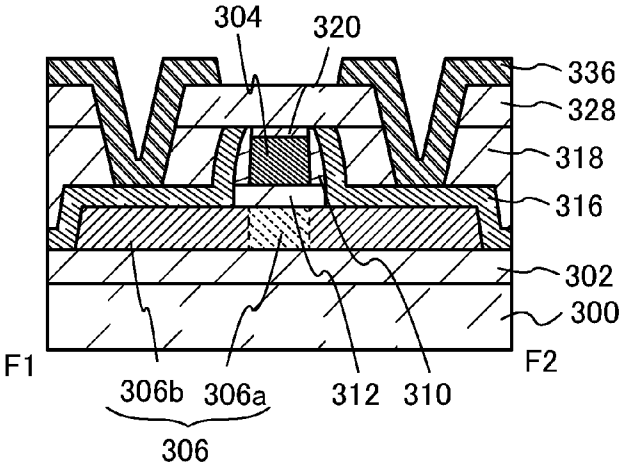


FIG. 10A

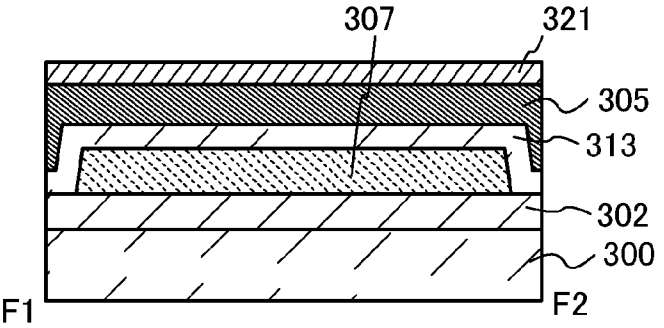


FIG. 10B

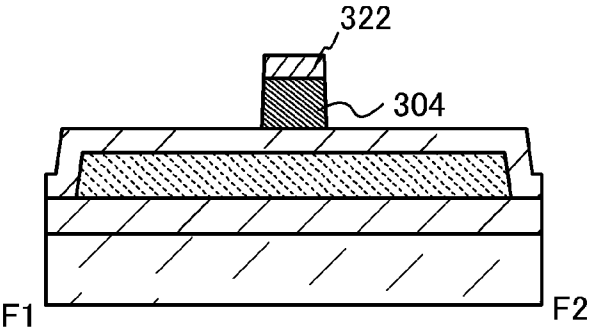


FIG. 10C

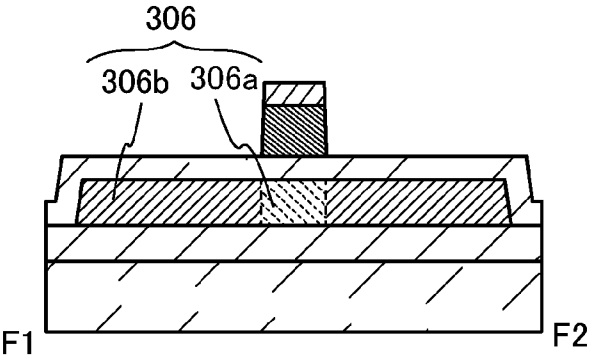


FIG. 11A

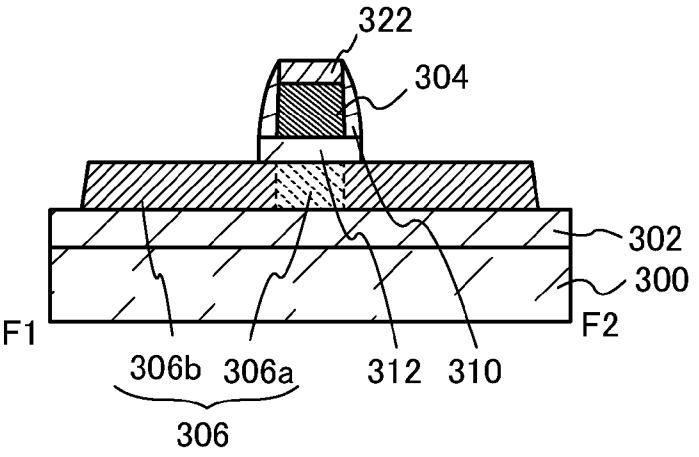


FIG. 11B

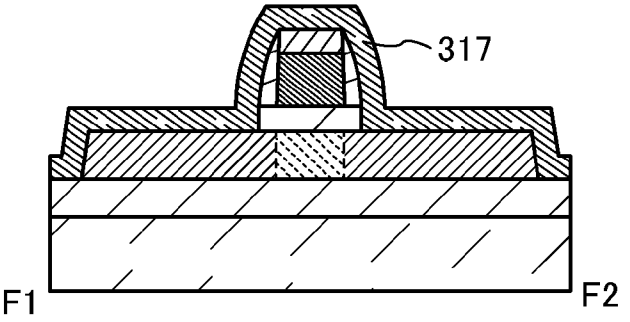


FIG. 11C

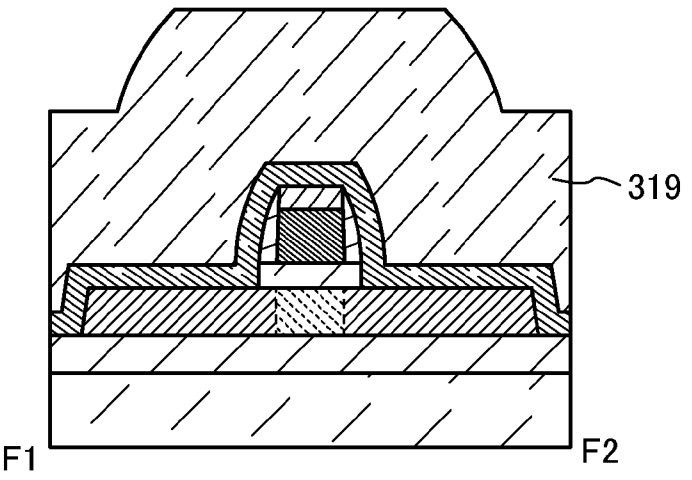


FIG. 12A

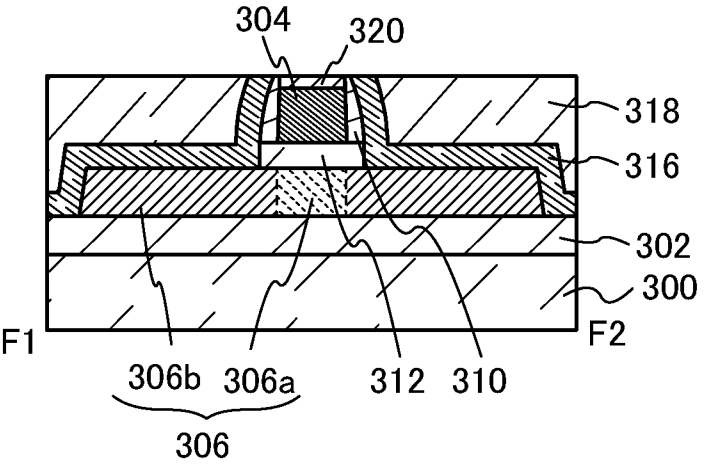


FIG. 12B

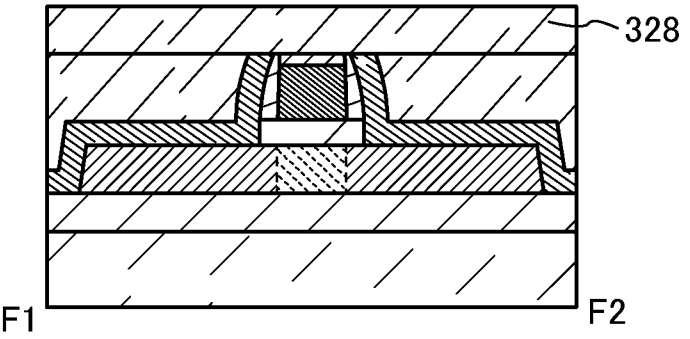


FIG. 12C

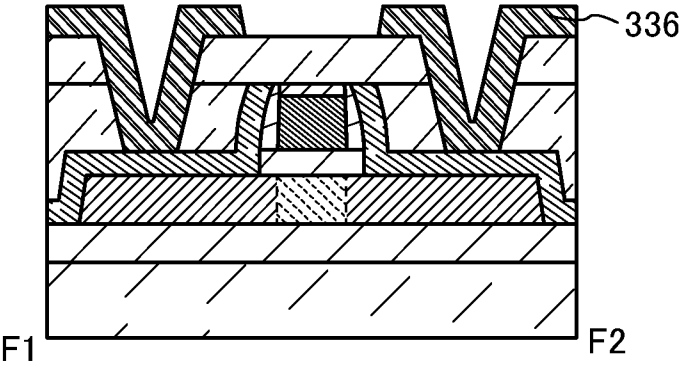


FIG. 13A

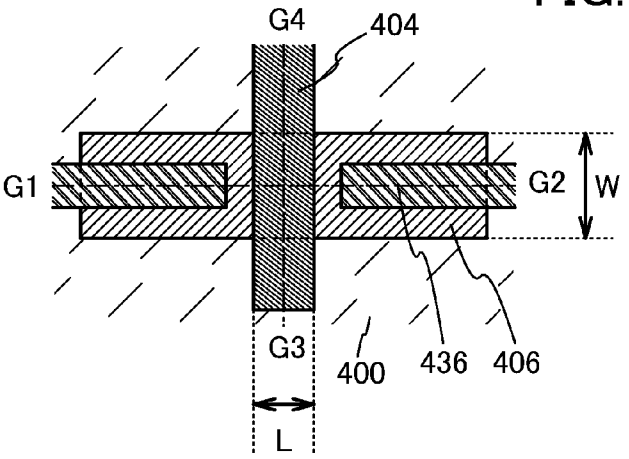


FIG. 13C

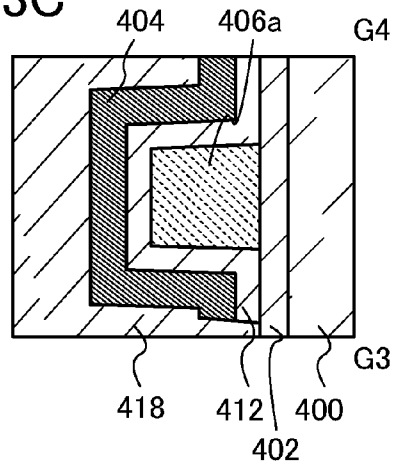


FIG. 13B

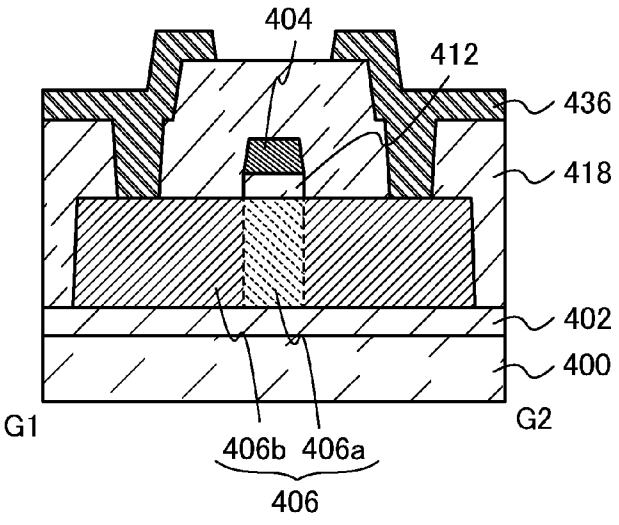


FIG. 14A

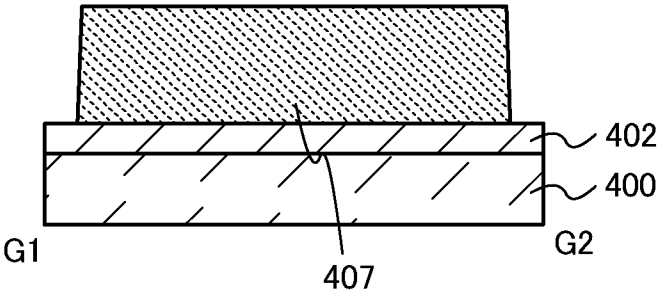


FIG. 14B

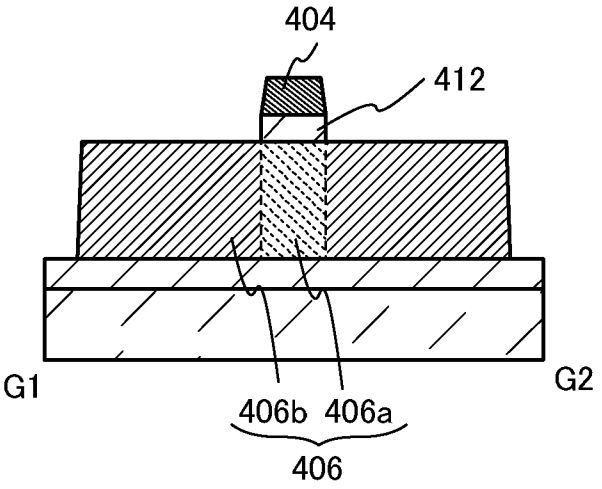


FIG. 14C

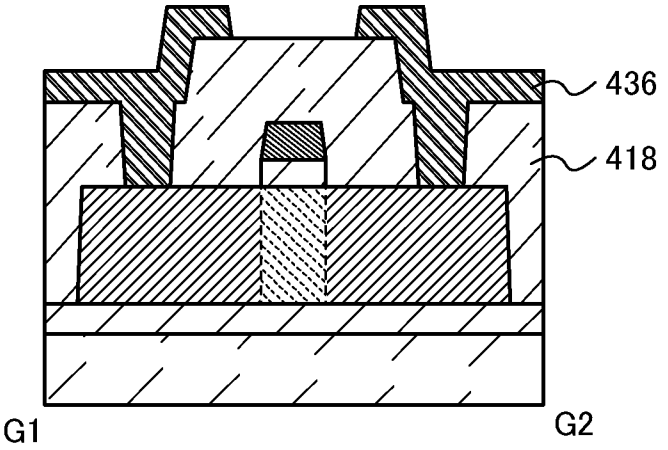


FIG. 15A

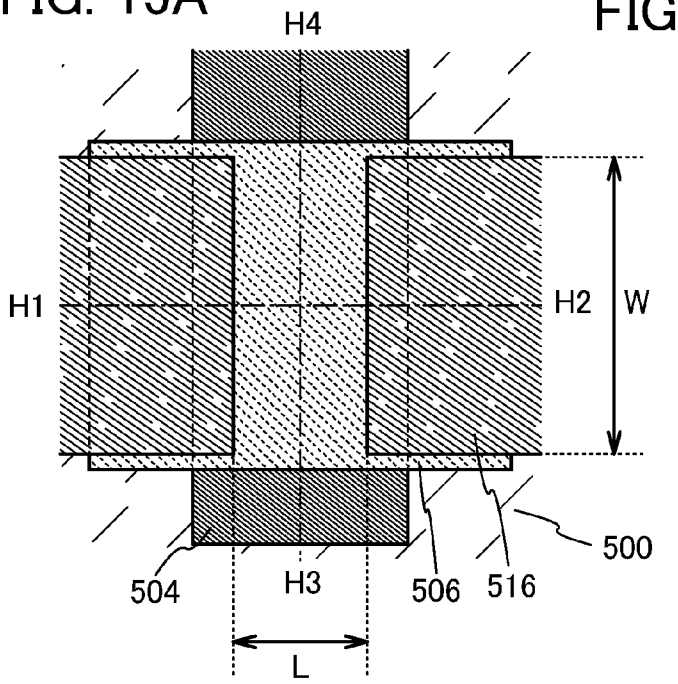


FIG. 15C

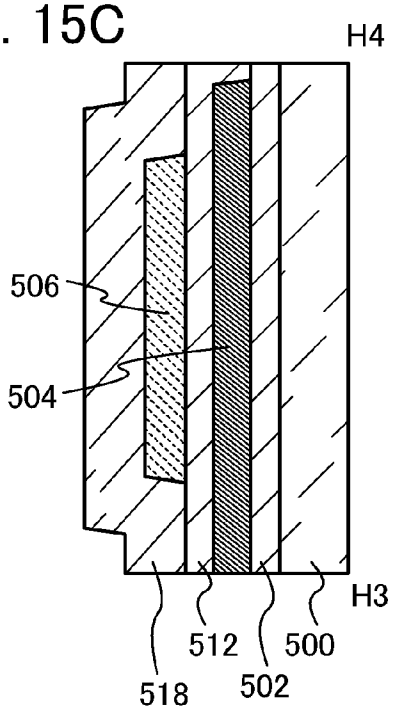


FIG. 15B

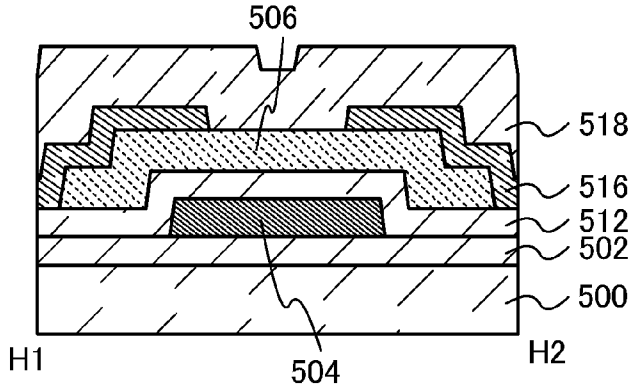


FIG. 16A

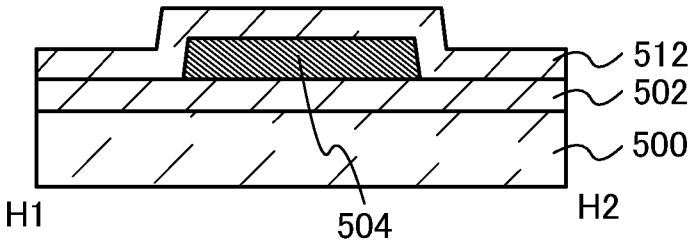


FIG. 16B

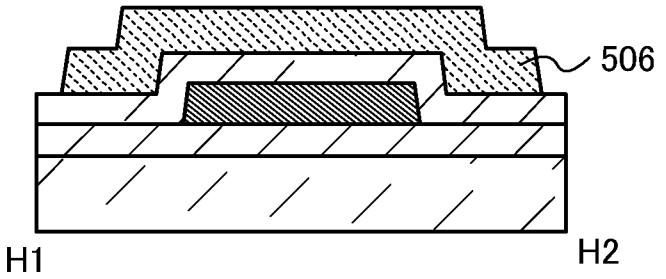


FIG. 16C

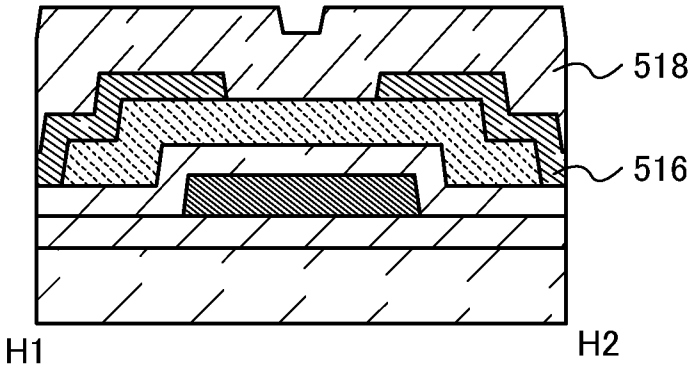


FIG. 17A

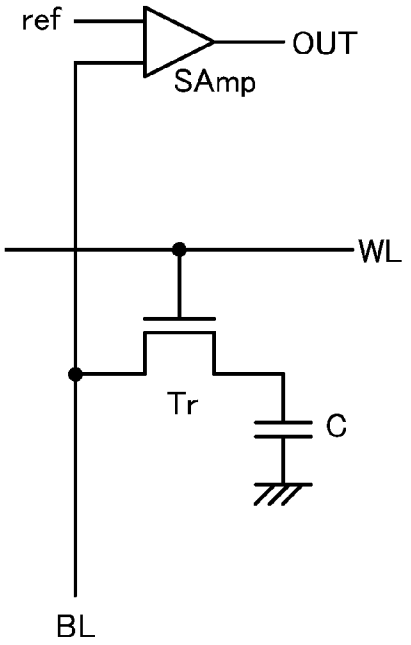


FIG. 17B

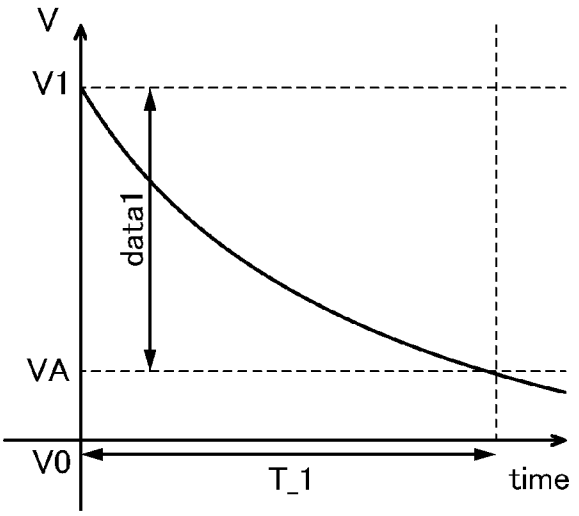


FIG. 17C

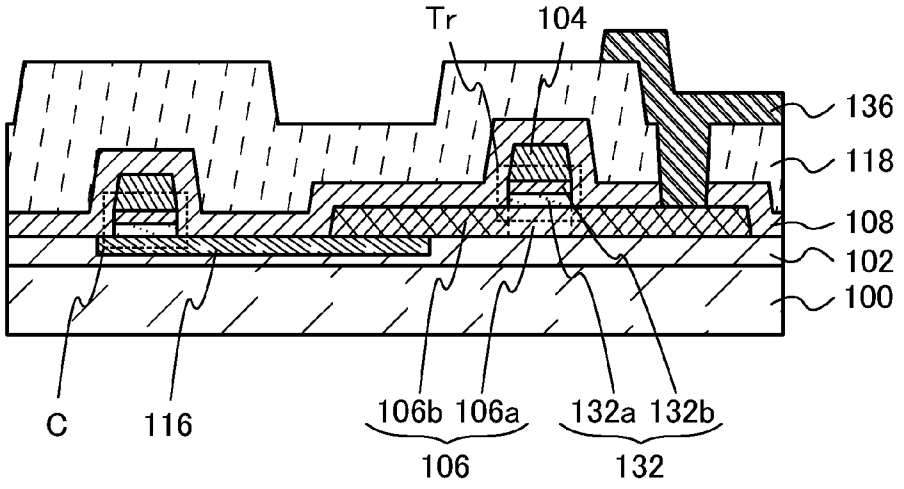


FIG. 18A

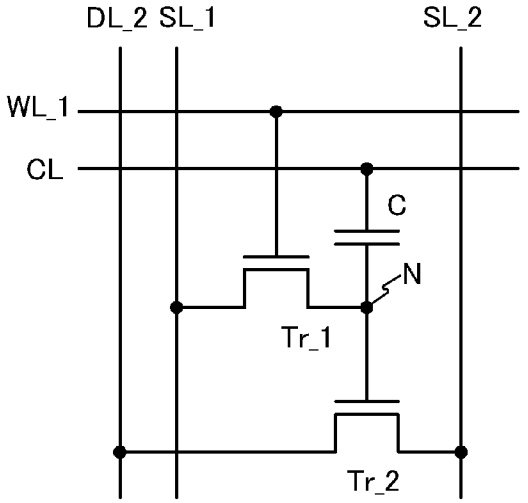


FIG. 18B

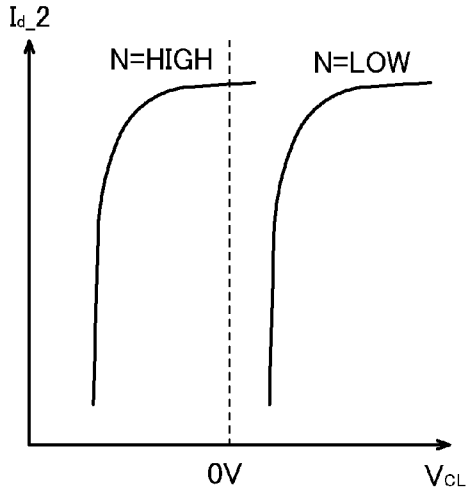


FIG. 18C

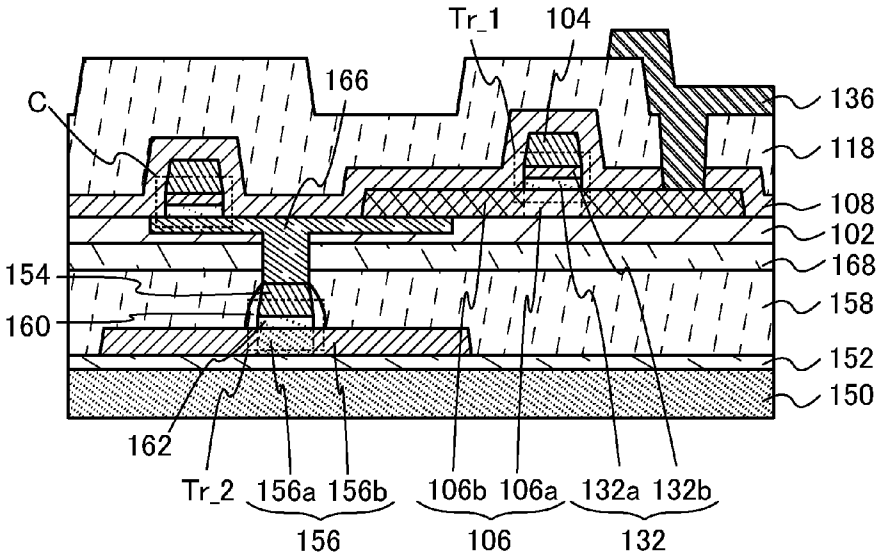


FIG. 19A

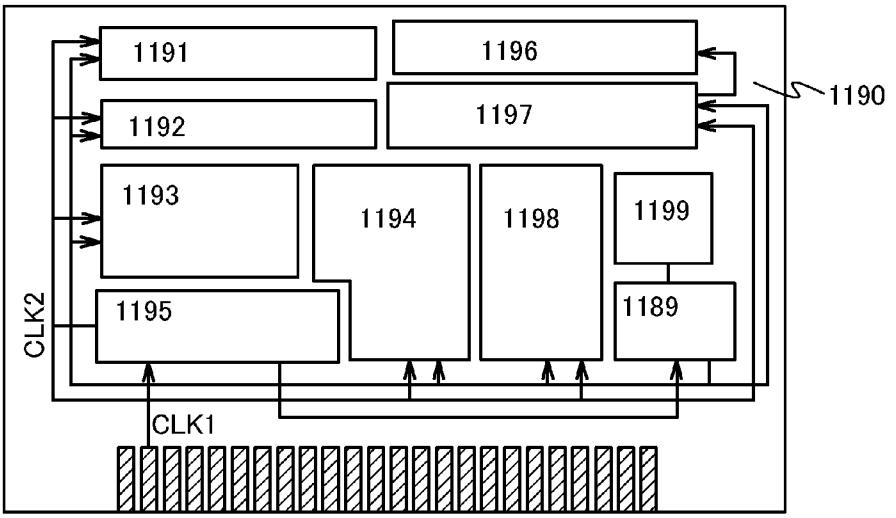


FIG. 19B

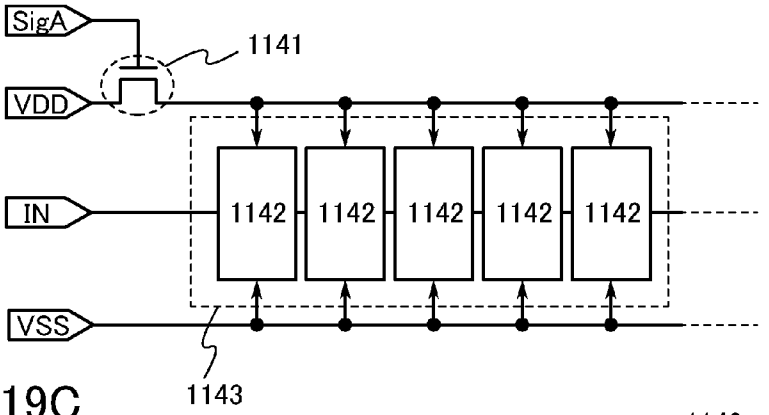


FIG. 19C

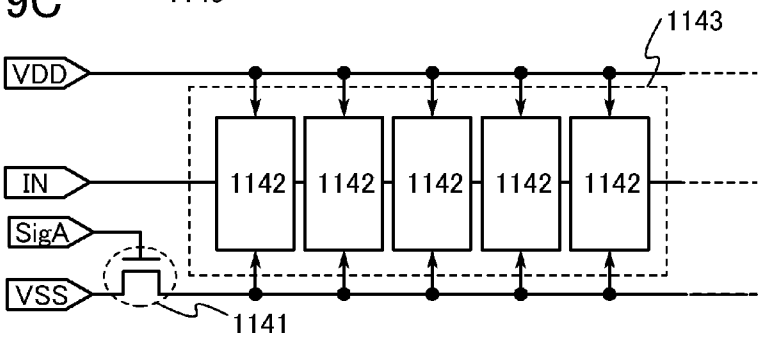


FIG. 20A

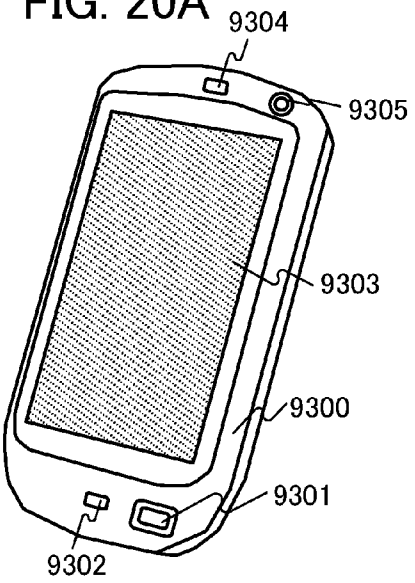


FIG. 20B

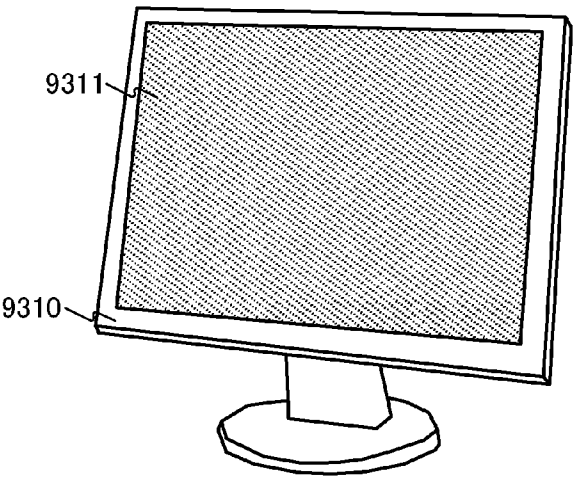


FIG. 20C

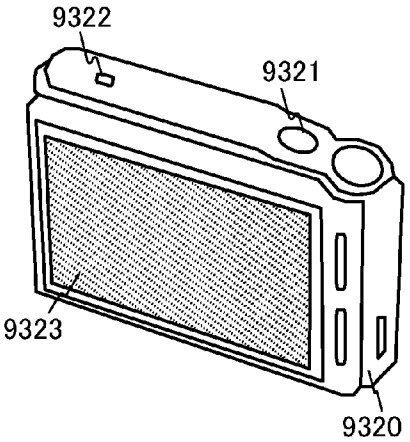


FIG. 20D

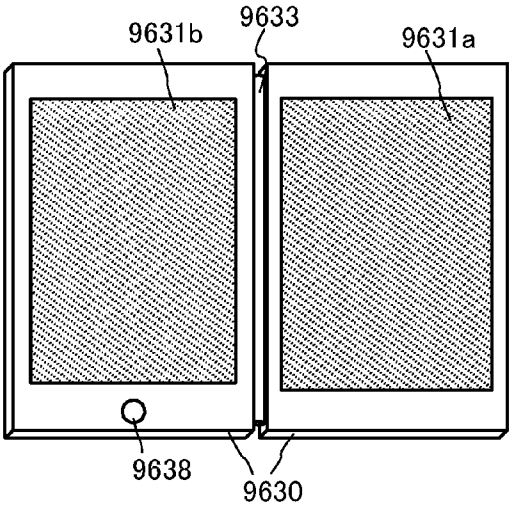


FIG. 21A

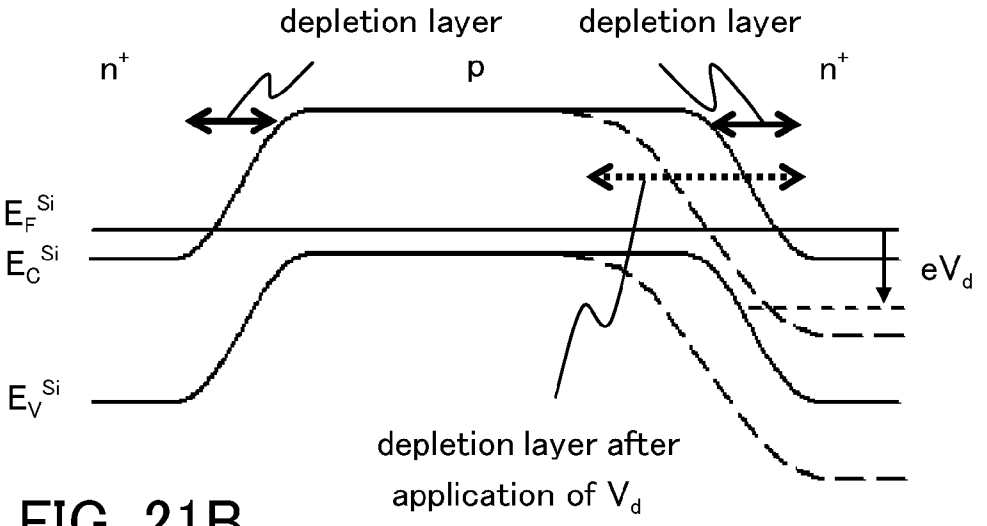


FIG. 21B

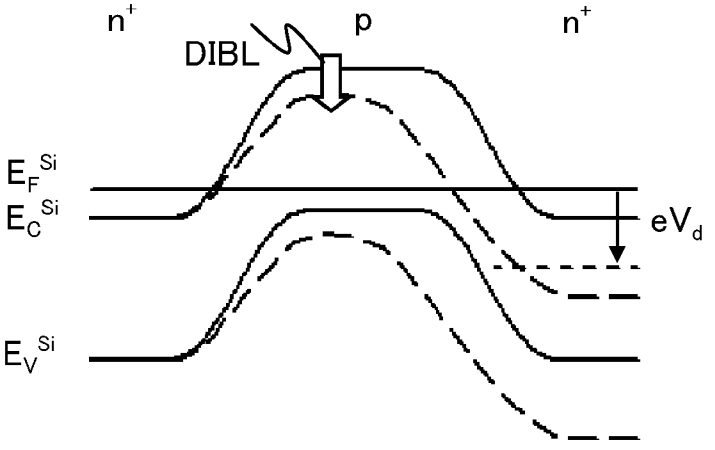


FIG. 22

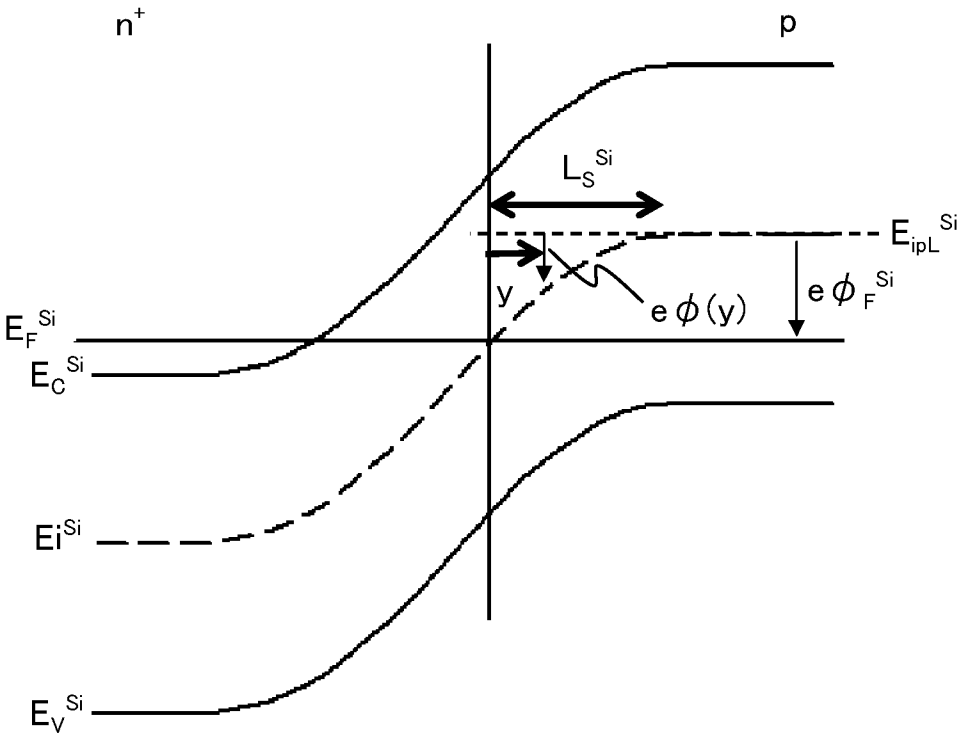
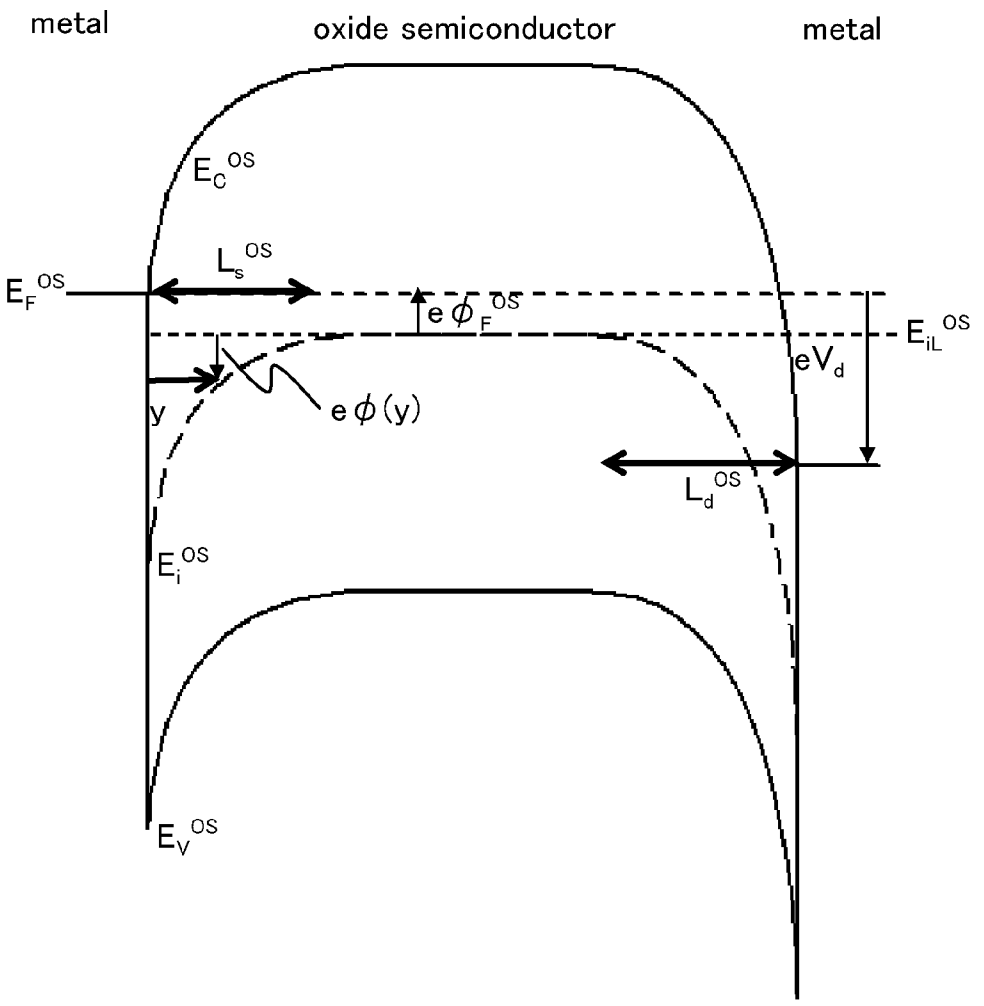


FIG. 23


metal
oxide semiconductor
metal
E_C^{OS}
L_s^{OS}
E_F^{OS}
$e\phi_F^{OS}$
E_{iL}^{OS}
eV_d
y
$e\phi(y)$
L_d^{OS}
E_i^{OS}
E_V^{OS}

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a semiconductor device and a method of manufacturing the semiconductor device.

[0003] Note that in this specification, a semiconductor device refers to any device that can function by utilizing semiconductor characteristics, and an electro-optical device, a semiconductor circuit, an electronic device, and the like are all included in the category of semiconductor devices.

[0004] 2. Description of the Related Art

[0005] The integration degree of a semiconductor device including silicon has been increased with miniaturization obeying the scaling law of a transistor or the like, and thus a reduction in power consumption and an improvement in performance have been achieved.

[0006] However, in recent years, the limit of the scaling law has become a problem. For example, when the channel length is short, a so-called short-channel effect such as a punch-through phenomenon becomes noticeable.

[0007] Further, it is known that a narrow-channel effect is caused when the channel width is small.

[0008] In a miniaturized transistor, the threshold voltage cannot be easily controlled due to an influence of a short-channel effect, a narrow-channel effect, or the like, and thus a variation in characteristics easily occurs. In view of this, a design rule for preventing a shift in threshold voltage due to a short-channel effect and a narrow-channel effect has been proposed (see Patent Document 1).

[0009] In addition, various methods for reducing a short-channel effect due to miniaturization of a transistor have been examined (see Patent Document 2).

REFERENCE

Patent Documents

[0010] [Patent Document 1] Japanese Published Patent Application No. H4-134832

[0011] [Patent Document 2] Japanese Published Patent Application No. 2006-100842

SUMMARY OF THE INVENTION

[0012] A main object of conventional art is to reduce an influence of a short-channel effect that is a major factor of degradation of electrical characteristics of a transistor accompanying miniaturization, and a transistor in which a short-channel effect is not substantially caused has not been proposed.

[0013] An object of one embodiment of the present invention is to provide a transistor in which a short-channel effect is not substantially caused and which has switching characteristics even in the case where the channel length is short.

[0014] Another object is to provide a highly integrated semiconductor device including the transistor.

[0015] The transistor includes an oxide semiconductor film, in which the channel length is greater than or equal to 5 nm and less than 60 nm and the channel width is greater than or equal to 5 nm and less than 200 nm.

[0016] At this time, the channel width is made 0.5 to 10 times as large as the channel length.

[0017] The oxide semiconductor film preferably contains at least In.

[0018] Alternatively, the oxide semiconductor film preferably contains at least In, Ga, and Zn.

[0019] The present inventors have found that a short-channel effect which is caused in a transistor including silicon is not substantially caused in a transistor including an oxide semiconductor film in some cases. This is significantly remarkable. Accordingly, it can be said that a rule for miniaturization which is utterly different from a rule for miniaturization of a transistor obeying the conventional scaling law needs to be established.

[0020] As one factor of a punch-through phenomenon which is one kind of short-channel effect caused in a transistor including silicon, drain induced barrier lowering (DIBL) is known.

[0021] Hereinafter, it is shown that, with a focus on the curve width of a band in the vicinity of junction portions between an oxide semiconductor film and source and drain electrodes, DIBL caused in a transistor including silicon is not easily caused in a transistor including the oxide semiconductor film.

[0022] A band structure between a source and a drain of a transistor including n-type silicon is shown in each of FIGS. **21**A and **21**B. FIG. **21**A is a schematic view of a band structure in the case of a long channel, and FIG. **21**B is a schematic view of a band structure in the case of a short channel. Here, the case where the gate voltage (V_g) is zero (i.e., the transistor is off) is described.

[0023] As shown in each of FIGS. **21**A and **21**B, the band is curved in the vicinity of a p-n junction interface even when the drain voltage (V_d) is zero (shown with a solid line). The reason for this is that carriers are exchanged between n^+ regions and a p region so that the Fermi level of the n^+ regions and that of the p region are equal to each other, which results in formation of depletion layers having donor ions and acceptor ions and generation of an electric field.

[0024] Here, when V_d is applied, the band in the n^+ region on the drain side is lowered by eV_d and the depletion layer is extended from the drain side (shown with a dotted line). At this time, in the case of the long channel, V_d does not affect the source side. On the other hand, in the case of the short channel, the depletion layer from the drain side is extended to the source side due to V_d, whereby a reduction in the potential of the p region is caused (i.e., bank is made to recede). As a result, current easily flows and the threshold voltage shifts in the negative direction.

[0025] Thus, when the channel length of a transistor including n-type silicon is decreased, the width of a depletion layer extended from a drain side, that is, the curve width of a band is increased due to V_d. Hereinafter, the curve width of a band in the vicinity of a junction portion between a channel and a source and a drain (p-n junction interface) of each of a transistor including silicon and a transistor including an oxide semiconductor film will be analytically derived.

[0026] FIG. **22** shows a band structure on a source side of a transistor including n-type silicon. With reference to FIG. **22**, first, the curve width L_s^{Si} of a band on the source side in a p region of the transistor including n-type silicon is obtained. Note that L_s^{Si} is equal to the width of a depletion layer having acceptor ions. Further, $\phi(y)$ represents the potential of a region at a distance of y from a p-n junction interface, and the origin of $\phi(y)$ is the intrinsic level E_{ipL}^{Si} in the p region. Furthermore, $e\phi_F^{Si}$ represents a difference between E_{ipL}^{Si} and

a Fermi level E_F^{Si}, and is defined as follows: $e\phi_F^{Si}=E_{ipL}^{Si}-E_F^{Si}$. Here, e represents elementary charge. The curve width of the band reflects a spatial variance of $\phi(y)$. Formula (1) corresponds to the Poisson equation.

$$\frac{d^2\phi}{dy} = -\frac{\rho}{\varepsilon^{Si}} \tag{1}$$

[0027] Note that $\in^{Si}$ represents a dielectric constant, and ρ represents a charge density. In the case where attention is focused on the depletion layer in the p region, ρ may be determined only in consideration of the acceptor ions having negative charge, and Formula (2) is obtained.

$$\rho=-eN_A^{Si} \tag{2}$$

[0028] Here, N_A^{Si} represents acceptor density. By substituting Formula (2) into Formula (1) and solving it under a boundary condition shown by Formula (3), Formula (4) is obtained.

$$\phi(L_s^{Si}) = \frac{d\phi}{dy}(L_s^{Si}) = 0 \tag{3}$$

$$\phi(y) = \frac{eN_A^{Si}}{2\varepsilon^{Si}} L_s^{Si2}\left(1-\frac{y}{L_s^{Si}}\right)^2 \tag{4}$$

[0029] Here, under a boundary condition shown by Formula (5), L_s^{Si} is obtained as shown in Formula (6).

$$e\phi(0) = \frac{e^2N_A^{Si}}{2\varepsilon^{Si}} L_s^{Si2} = E_{ipL}^{Si} - E_F^{Si} \equiv e\phi_F^{Si} \tag{5}$$

$$L_s^{Si} = \sqrt{\frac{2\varepsilon^{Si}\phi_F^{Si}}{eN_A^{Si}}} \tag{6}$$

[0030] On the other hand, the curve width L_d^{Si} of the band on a drain side at the time of application of V_d is obtained as shown in Formula (7) by a calculation similar to that in the case of L_s^{Si}.

$$L_d^{Si} = \sqrt{\frac{2\varepsilon^{Si}(\phi_F^{Si}+V_d)}{eN_S^{Si}}} \tag{7}$$

[0031] Formula (7) shows that, in the transistor including silicon, L_d^{Si} is increased due to V_d, that is, the depletion layer is extended from the drain side due to V_d. The above is a description on DIBL in the transistor including silicon.

[0032] Next, FIG. **23** shows a band structure between a source and a drain in a transistor including an oxide semiconductor film. With reference to FIG. **23**, the curve width L_s^{OS} of a band on a source side and the curve width L_d^{OS} of the band on a drain side in an oxide semiconductor region in the transistor including the oxide semiconductor film are obtained. Note that, on the assumption that the work function ϕ_m of a metal used for the source and the drain is equal to the electron affinity χ^{OS} of the oxide semiconductor ($\phi_m=\chi^{OS}$), the metal and the oxide semiconductor form an ohmic contact. Further, $\phi(y)$ represents the potential of a region at a distance of y from a metal-oxide semiconductor junction interface on the source side. The origin of $\phi(y)$ is the intrinsic level E_{iL}^{OS} in the oxide semiconductor region. Furthermore, $e\phi_F^{OS}$ represents a difference between E_{iL}^{OS} and a Fermi level E_F^{OS} on the source side, and is defined as follows: $e\phi_F^{OS}=E_{iL}^{OS}-E_F^{OS}$. In this case, the curve width of the band in the oxide semiconductor region is thought to be derived from the electron density $n^{OS}(y)$ (electrons corresponds to majority carriers), so that the charge density ρ is represented by Formula (8).

$$\rho(y) = -en^{OS}(y) = -en_0^{OS}\mathrm{Exp}\left[\frac{e\phi(y)}{kT}\right] \tag{8}$$

[0033] Here, k represents a Boltzmann constant, and T represents an absolute temperature. Note that n_0^{OS} represents the electron density in a bulk region of the oxide semiconductor, and is represented by Formula (9) using an intrinsic carrier density n_i^{OS}.

$$n_0^{OS} = n_i^{OS}\mathrm{Exp}\left[-\frac{e\phi_F^{OS}}{kT}\right] \tag{9}$$

[0034] Accordingly, $\phi(y)$ is obtained using the Poisson equation in Formula (10).

$$\frac{d^2\phi}{dy} = \frac{en_0^{OS}}{\varepsilon^{OS}}\mathrm{Exp}\left[\frac{e\phi}{kT}\right] \tag{10}$$

[0035] By solving this under a boundary condition shown by Formula (11), Formula (12) is obtained.

$$\phi(L_s) = \frac{d\phi}{dy}(L_s) = 0 \tag{11}$$

$$\phi(y) = -\frac{2kT}{e}\mathrm{lnCos}\left[\sqrt{\frac{e^2n_0^{OS}}{2\varepsilon^{OS}kT}}\,(y-L_s^{OS})\right] \tag{12}$$

[0036] Accordingly, under a boundary condition shown by Formula (13), Formula (14) is obtained.

$$e\phi(0) = -2kT\mathrm{lnCos}\left[\sqrt{\frac{e^2n_0^{OS}}{2\varepsilon^{OS}kT}}\,L_s^{OS}\right] = \frac{E_g^{OS}}{2} + e\phi_F^{OS} \tag{13}$$

$$L_s^{OS} = \sqrt{\frac{2\varepsilon^{OS}kT}{e^2n_0^{OS}}}\,\mathrm{ArcCos}\left\{\mathrm{Exp}\left[-\frac{E_g^{OS}/2+e\phi_F^{OS}}{2kT}\right]\right\} \tag{14}$$

[0037] Here, since $E_g^{OS}/2+e\phi_F^{OS}>>2kT$ is satisfied, Formula (14) can approximate to Formula (15).

$$L_s^{OS} \sim \sqrt{\frac{2\varepsilon^{OS}kT}{e^2n_0^{OS}}}\,\mathrm{ArcCos}(0) = \sqrt{\frac{2\varepsilon^{OS}kT}{e^2n_0^{OS}}}\,\frac{\pi}{2} = \pi\sqrt{\frac{\varepsilon^{OS}kT}{2e^2n_0^{OS}}} \tag{15}$$

[0038] On the other hand, L_d^{OS} at the time of application of V_d is obtained by substituting $e\phi_F^{OS}+eV_d$ for $e\phi_F^{OS}$ in Formula (13). Also in this case, $E_g^{OS}/2+e\phi_F^{OS}+eV_d>>2kT$ is satisfied, so that Formula (16) is obtained.

$$L_d^{OS} \sim \pi \sqrt{\frac{\varepsilon^{OS} kT}{2e^2 n_0^{OS}}} \sim L_s^{OS} \tag{16}$$

[0039] From the above, in the case of the transistor including the oxide semiconductor film, L_d^{OS} does not depend on V_d. Therefore, it can be said that DIBL is not caused in the transistor including the oxide semiconductor film.

[0040] A punch-through phenomenon in a transistor including silicon is caused when a depletion layer due to an electric field of a gate is not extended to a deep area of a channel region in some cases. This is because the density of minority carriers in silicon is as high as about $1\times10^{11}/cm^3$. That is, by accumulation of the minority carriers, the electric field of the gate does not enter a deep area; thus, the transistor cannot be completely off, which results in an increase in off-state current.

[0041] On the other hand, thanks to diligent research by the present inventors, it has become clear that the density of minority carriers in an oxide semiconductor film can be as low as about $1\times10^{-9}/cm^3$. That is, in a transistor including an oxide semiconductor film, accumulation of minority carriers hardly occurs, and an electric field of a gate enters a deep area; thus, the transistor can be easily completely off, and thus off-state current can be made small. In this manner, in a transistor including an oxide semiconductor film, a depletion layer is significantly extended due to an electric field of a gate.

[0042] As described above, it can be said that a short-channel effect, which is generally known to be caused in a transistor including silicon, is not substantially caused in a transistor including an oxide semiconductor film.

[0043] Therefore, it can be said that a transistor including an oxide semiconductor film can easily have switching characteristics even in the case where the channel length is short.

[0044] In the case where a transistor including silicon is miniaturized, the channel width is generally decreased when the channel length is decreased.

[0045] However, in a transistor including an oxide semiconductor film, in some cases, the threshold voltage shifts in the negative direction when the channel width is decreased as well as the channel length. This fact also has become clear thanks to the diligent research by the present inventors.

[0046] Accordingly, it can be said that, in a transistor including an oxide semiconductor film, it is important to make the channel width sufficiently large when the channel length is small in order that the transistor has switching characteristics. Further, it can be said that it is important to keep the ratio of the channel width to the channel length constant for miniaturization.

[0047] Here, attention should be paid to the fact that electrons that are carriers are generated due to oxygen vacancies in an oxide semiconductor film.

[0048] When electrons are generated in an oxide semiconductor film, a transistor is likely to have so-called normally-on electrical characteristics, that is, the transistor is likely to be on even at a gate voltage of 0 V. Therefore, oxygen vacancies in the oxide semiconductor film are preferably reduced.

[0049] For example, in order to reduce oxygen vacancies in the oxide semiconductor film, oxygen supplied from the outside of the oxide semiconductor film may be utilized. As a method of supplying oxygen from the outside, specifically, oxidation treatment such as ion doping treatment, ion implantation treatment, or plasma treatment or the like may be performed. Alternatively, a layer containing excess oxygen may be provided so that oxygen is supplied therefrom to the oxide semiconductor film.

[0050] Even with the use of such a method, in some cases, the proportion of oxygen vacancies in the oxide semiconductor film is larger than that of oxygen supplied from the outside in the case where the transistor including the oxide semiconductor film is miniaturized. One reason for this is that the ratio of the surface area to the volume of the oxide semiconductor film is increased with miniaturization. Also in view of this, it can be said that it is important to make the channel width large in the case where the channel length is short.

[0051] However, when the channel width is extremely large, miniaturization of the transistor, which is the original object, cannot be achieved. Therefore, the ratio of the channel width to the channel length is determined realistically. From such a reason, there is a possibility that intent to make the channel length small without particular limitation is not practical because the channel width cannot be made larger than a predetermined value.

[0052] In view of this, it is important to efficiently utilize oxygen supplied from the outside of the oxide semiconductor film. For example, a layer having low oxygen permeability is provided over the transistor including the oxide semiconductor film, whereby outward diffusion of oxygen is suppressed and thus oxygen can be efficiently utilized. Therefore, even when the channel length is short and the channel width is a predetermined value or smaller, the transistor can have switching characteristics.

[0053] Further, in some cases, a parasitic channel is formed on a side surface of the oxide semiconductor film when the transistor including the oxide semiconductor film is miniaturized. This fact also has become clear thanks to the diligent research by the present inventors.

[0054] Since an influence of the parasitic channel is noticeable in a transistor having a short channel in some cases, this influence is likely to be regarded as a short channel effect; however, they are different from each other in a strict sense.

[0055] The threshold voltage for forming the parasitic channel is generally lower than that for forming the original channel of the transistor. Therefore, when the influence of the parasitic channel becomes large, it seems as if the threshold voltage of the transistor shifts in the negative direction. This is because carriers are easily generated on the side surface of the oxide semiconductor film. For that reason, it is important that the side surface of the oxide semiconductor film be supplied with a larger amount of oxygen than the other surfaces of the oxide semiconductor film.

[0056] For example, a layer having low oxygen permeability may be provided on the side surface of the oxide semiconductor film so that oxygen vacancies are not easily generated. Further, a layer containing excess oxygen and the layer having low oxygen permeability may be stacked together to be provided on the side surface of the oxide semiconductor film. At this time, the layer containing excess oxygen is preferably provided in contact with the side surface of the oxide semiconductor film.

[0057] It is known that, in the oxide semiconductor film, electrons that are carriers are generated due to hydrogen as well as oxygen vacancies. Therefore, it is preferable that hydrogen in the oxide semiconductor film be also reduced.

[0058] The transistor including the oxide semiconductor film in which the density of minority carriers is extremely low and a source of carriers such as oxygen vacancies or hydrogen is reduced has extremely small off-state current.

[0059] The transistor including the oxide semiconductor film can be used in combination with a conventional transistor including silicon or the like. For example, in comparison with the transistor including the oxide semiconductor film, a transistor including silicon and a transistor including a compound semiconductor are likely to have improved on-state characteristics. Therefore, the transistor including silicon or the transistor including a compound semiconductor may be used as a transistor for which on-state characteristics are required, and the transistor including the oxide semiconductor film may be used as a transistor for which small off-state current is required. The oxide semiconductor film can be formed by a thin film formation method such as a sputtering method, and thus is not limited so much in combination with another semiconductor material; this is one feature of the oxide semiconductor film.

[0060] Note that the transistor including silicon can have excellent electrical characteristics when dangling bonds on a silicon surface are terminated with hydrogen. Therefore, a hydrogen-containing layer serving as a source of hydrogen for the transistor including silicon is preferably provided. However, as described above, hydrogen serves as a source of carriers for the transistor including the oxide semiconductor film, and is a factor of degrading the electrical characteristics of the transistor including the oxide semiconductor film.

[0061] Accordingly, in the case where the transistor including silicon and the transistor including the oxide semiconductor film are used in combination, the hydrogen-containing layer is preferably provided closer to the transistor including silicon, and a layer having low hydrogen permeability is preferably provided closer to the transistor including the oxide semiconductor film.

[0062] With the use of an oxide semiconductor film, a transistor in which a short-channel effect is not substantially caused and which has switching characteristics even in the case where the channel length is short can be provided.

[0063] Further, a highly integrated semiconductor device including the transistor can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0064] FIGS. **1**A to **1**C are a top view and cross-sectional views illustrating an example of a semiconductor device according to one embodiment of the present invention.

[0065] FIGS. **2**A to **2**C are a top view and cross-sectional views illustrating an example of a semiconductor device according to one embodiment of the present invention.

[0066] FIGS. **3**A to **3**C are a top view and cross-sectional views illustrating an example of a semiconductor device according to one embodiment of the present invention.

[0067] FIGS. **4**A to **4**C are a top view and cross-sectional views illustrating an example of a semiconductor device according to one embodiment of the present invention.

[0068] FIGS. **5**A to **5**C are cross-sectional views illustrating an example of a method of manufacturing the semiconductor device according to one embodiment of the present invention.

[0069] FIGS. **6**A to **6**C are cross-sectional views illustrating the example of the method of manufacturing the semiconductor device according to one embodiment of the present invention.

[0070] FIGS. **7**A to **7**C are a top view and cross-sectional views illustrating an example of a semiconductor device according to one embodiment of the present invention.

[0071] FIGS. **8**A to **8**D are cross-sectional views illustrating an example of a method of manufacturing the semiconductor device according to one embodiment of the present invention.

[0072] FIGS. **9**A to **9**C are a top view and cross-sectional views illustrating an example of a semiconductor device according to one embodiment of the present invention.

[0073] FIGS. **10**A to **10**C are cross-sectional views illustrating an example of a method of manufacturing the semiconductor device according to one embodiment of the present invention.

[0074] FIGS. **11**A to **11**C are cross-sectional views illustrating the example of the method of manufacturing the semiconductor device according to one embodiment of the present invention.

[0075] FIGS. **12**A to **12**C are cross-sectional views illustrating the example of the method of manufacturing the semiconductor device according to one embodiment of the present invention.

[0076] FIGS. **13**A to **13**C are a top view and cross-sectional views illustrating an example of a semiconductor device according to one embodiment of the present invention.

[0077] FIGS. **14**A to **14**C are cross-sectional views illustrating an example of a method of manufacturing the semiconductor device according to one embodiment of the present invention.

[0078] FIGS. **15**A to **15**C are a top view and cross-sectional views illustrating an example of a semiconductor device according to one embodiment of the present invention.

[0079] FIGS. **16**A to **16**C are cross-sectional views illustrating an example of a method of manufacturing the semiconductor device according to one embodiment of the present invention.

[0080] FIGS. **17**A to **17**C are a circuit diagram and a cross-sectional view illustrating an example of a semiconductor memory device according to one embodiment of the present invention, and a graph showing electrical characteristics thereof.

[0081] FIGS. **18**A to **18**C are a circuit diagram and a cross-sectional view illustrating an example of a semiconductor memory device according to one embodiment of the present invention, and a graph showing electrical characteristics thereof.

[0082] FIGS. **19**A to **19**C are a block diagram illustrating a specific example of a CPU according to one embodiment of the present invention, and circuit diagrams each illustrating part of the CPU.

[0083] FIGS. **20**A to **20**D are perspective views each illustrating an example of an electronic device according to one embodiment of the present invention.

[0084] FIGS. **21**A and **21**B are each a band diagram between a source and a drain of a transistor including n-type silicon.

[0085] FIG. **22** is a band diagram on a source side of a transistor including n-type silicon.

[0086] FIG. **23** is a band diagram between a source and a drain of a transistor including an oxide semiconductor film.

DETAILED DESCRIPTION OF THE INVENTION

[0087] Embodiments of the present invention will be described in detail with reference to the accompanying drawings. Note that the present invention is not limited to the description below, and it is easily understood by those skilled in the art that modes and details disclosed herein can be modified in various ways. Further, the present invention is not construed as being limited to the description of the embodiments below. In describing structures of the present invention with reference to the drawings, the same reference numerals are used in common for the same portions in different drawings. The same hatching pattern is applied to similar parts, and the similar parts are not especially denoted by reference numerals in some cases.

[0088] The present invention will be described below; terms used in this specification are briefly explained. First, when one of a source and a drain of a transistor is called a drain, the other is called a source in this specification. That is, they are not distinguished depending on the potential level. Therefore, in this specification, a portion called a source can be alternatively referred to as a drain.

[0089] Note that a voltage refers to a potential difference between a certain potential and a reference potential (e.g., a ground potential (GND) or a source potential) in many cases. Accordingly, a voltage can also be called a potential.

[0090] Further, even when the expression "to be electrically connected" is used in this specification, there is a case in which no physical connection is made and a wiring is just extended in an actual circuit.

[0091] Note that the ordinal numbers such as "first" and "second" in this specification are used for convenience and do not denote the order of steps or the stacking order of layers. In addition, the ordinal numbers in this specification do not denote particular names which specify the present invention.

[0092] Note that a channel length refers to a distance between a source and a drain of a transistor. The shorter the channel length is, the lower the on-state resistance becomes; thus, a transistor having a short channel length is capable of high-speed operation. Note that a channel width refers to the length of opposite sides of a source and a drain of a transistor. The larger the channel width is, the lower the on-state resistance becomes; thus, a transistor having a large channel width is capable of high-speed operation.

Embodiment 1

[0093] In this embodiment, a transistor according to one embodiment of the present invention will be described.

[0094] FIG. **1**A is a top view of a transistor according to one embodiment of the present invention. FIG. **1**B is a cross-sectional view taken along dashed-dotted line A**1**-A**2** in FIG. **1**A. FIG. **1**C is a cross-sectional view taken along dashed-dotted line A**3**-A**4** in FIG. **1**A. Note that a base insulating film **102** and the like are not illustrated in FIG. **1**A for simplicity.

[0095] In FIG. **1**A, the channel length (L) and the channel width (W) of the transistor are shown. Note that the channel region of the transistor corresponds to a region of an oxide semiconductor film **106** overlapping with a gate electrode **104**. At least part of two side surfaces of the oxide semiconductor film **106** overlap with the gate electrode **104**.

[0096] In the transistor illustrated in FIG. **1**A, the channel length is greater than or equal to 5 nm and less than 60 nm, and the channel width is greater than or equal to 5 nm and less than 200 nm.

[0097] Further, in the transistor illustrated in FIG. **1**A, the ratio of the channel width to the channel length is 0.5:1 to 10:1.

[0098] FIG. **1**B illustrates a cross-sectional structure of the transistor including the base insulating film **102** provided over a substrate **100**; the oxide semiconductor film **106** provided over the base insulating film **102**; a gate insulating film **112** provided over the oxide semiconductor film **106**; and the gate electrode **104** provided over the gate insulating film **112** so as to overlap with the oxide semiconductor film **106**.

[0099] Note that in FIG. **1**B, an interlayer insulating film **118** which is provided over the oxide semiconductor film **106** and the gate electrode **104** and has openings reaching the oxide semiconductor film **106**, and wirings **136** provided in contact with the oxide semiconductor film **106** through the openings in the interlayer insulating film **118** are illustrated.

[0100] For the oxide semiconductor film **106**, for example, an In—M—Zn—O-based material may be used. Here, a metal element M is an element whose bond energy with oxygen is higher than that of In and that of Zn. Alternatively, the metal element M is an element which has a function of suppressing desorption of oxygen from the In—M—Zn—O-based material. Owing to the effect of the metal element m, generation of oxygen vacancies in the oxide semiconductor film is suppressed to some extent. It is thus possible to reduce variation in the electrical characteristics of the transistor which is caused by oxygen vacancies, so that a highly reliable transistor can be obtained.

[0101] Specifically, the metal element M may be Al, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Ga, Y, Zr, Nb, Mo, Sn, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, or W, and is preferably Al, Ti, Ga, Y, Zr, Ce, or Hf. For the metal element m, one or more elements may be selected from the above elements. Further, Si or Ge may be used instead of the metal element M.

[0102] Note that generation of oxygen vacancies in the oxide semiconductor film **106** cannot be completely suppressed only by the action of the metal element M in the oxide semiconductor film **106**. Therefore, it is important that oxygen be supplied from at least one of the base insulating film **102** and the gate insulating film **112**.

[0103] The hydrogen concentration in the oxide semiconductor film **106** is 2×10^{20} atoms/cm^3 or lower, preferably 5×10^{19} atoms/cm^3 or lower, more preferably 1×10^{19} atoms/cm^3 or lower. This is because hydrogen in the oxide semiconductor film **106** generates unintentional carriers in some cases. The generated carriers are a factor of changing electrical characteristics of the transistor.

[0104] The oxide semiconductor film **106** is in a single crystal state, a polycrystalline (also referred to as polycrystal) state, an amorphous state, or the like.

[0105] The oxide semiconductor film **106** is preferably a c-axis aligned crystalline oxide semiconductor (CAAC-OS) film.

[0106] The CAAC-OS film is not completely single crystal nor completely amorphous. The CAAC-OS film is an oxide semiconductor film with a crystal-amorphous mixed phase structure where crystal parts are included in an amorphous phase. Note that in most cases, the crystal part fits inside a cube whose one side is less than 100 nm. From an observation image obtained with a transmission electron microscope (TEM), a boundary between an amorphous part and a crystal part in the CAAC-OS film is not clear. Further, with the TEM, a grain boundary in the CAAC-OS film is not found. Thus, in

the CAAC-OS film, a reduction in carrier mobility, due to the grain boundary, is suppressed.

[0107] In each of the crystal parts included in the CAAC-OS film, a c-axis is aligned in a direction perpendicular to a surface where the CAAC-OS film is formed or a top surface of the CAAC-OS film, triangular or hexagonal atomic arrangement which is seen from the direction perpendicular to the a-b plane is formed, and metal atoms are arranged in a layered manner or metal atoms and oxygen atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis. Note that, among crystal parts, the directions of the a-axis and the b-axis of one crystal part may be different from those of another crystal part. In this specification, a simple term "perpendicular" includes a range from 85° to 95°.

[0108] In the CAAC-OS film, distribution of crystal parts is not necessarily uniform. For example, in the formation process of the CAAC-OS film, in the case where crystal growth occurs from a top surface side of the oxide semiconductor film **106**, the proportion of crystal parts on the top surface of the oxide semiconductor film is sometimes higher than that on the surface where the oxide semiconductor film is formed. Further, when an impurity is added to the CAAC-OS film, the crystal part in a region to which the impurity is added becomes amorphous in some cases.

[0109] Since the c-axes of the crystal parts included in the CAAC-OS film are aligned in the direction parallel to a normal vector of a surface where the CAAC-OS film is formed or a normal vector of a top surface of the CAAC-OS film, the directions of the c-axes may be different from each other depending on the shape of the CAAC-OS film (the cross-sectional shape of the surface where the CAAC-OS film is formed or the cross-sectional shape of the top surface of the CAAC-OS film). Note that the direction of c-axis of the crystal part is the direction parallel to a normal vector of the surface where the CAAC-OS film is formed just after the formation of the CAAC-OS film or a normal vector of the top surface of the CAAC-OS film just after the formation of the CAAC-OS film. The crystal part is formed by film formation or by performing treatment for crystallization such as heat treatment after film formation.

[0110] With the use of the CAAC-OS film in a transistor, a change in electric characteristics of the transistor due to irradiation with visible light or ultraviolet light is small. Thus, the transistor has high reliability.

[0111] Note that the oxide semiconductor film **106** includes a region **106***a* and regions **106***b*. The region **106***a* functions as a channel region, and the regions **106***b* function as a source region and a drain region. Therefore, in some cases, the regions **106***b* should be called not a semiconductor but a conductor. For that reason, even when the expression "oxide semiconductor film **106**" is used for simplicity, this means only the region **106***a* and does not include the regions **106***b* in some cases.

[0112] The regions **106***b* have lower resistance than the region **106***a*. The regions **106***b* contain an impurity having a function of reducing the resistance of the oxide semiconductor film. Examples of the impurity having a function of reducing the resistance of the oxide semiconductor film include helium, boron, nitrogen, fluorine, neon, aluminum, phosphorus, argon, arsenic, krypton, indium, tin, antimony, and xenon.

[0113] In the region **106***a* of the oxide semiconductor film **106**, the band gap is approximately 2.8 eV to 3.2 eV, the density of minority carriers is as extremely low as approximately $10^{-9}/cm^3$, and majority carriers flow only from the source of the transistor.

[0114] The oxide semiconductor film **106** has a wider band gap than silicon by approximately 1 eV to 2 eV. For that reason, in the transistor including the oxide semiconductor film **106**, impact ionization is unlikely to occur and avalanche breakdown is unlikely to occur. That is, it can be said that, in the transistor including the oxide semiconductor film **106**, hot-carrier degradation is unlikely to occur.

[0115] In the region **106***a*, the impurity concentration is low and oxygen vacancies are not easily generated. Therefore, in the transistor including the oxide semiconductor film **106**, the region **106***a* can be completely depleted by an electric field of the gate electrode **104** even in the case where the thickness of the oxide semiconductor film **106** is large (for example, greater than or equal to 15 nm and less than 100 nm). For that reason, in the transistor including the oxide semiconductor film **106**, a shift of the threshold voltage in the negative direction due to a puch-through phenomenon is not caused and, when the channel length is, for example, 3 μm, the off-state current can be lower than 10^{-21} A or lower than 10^{-24} A per micrometer of channel width at room temperature.

[0116] The oxide semiconductor film with few oxygen vacancies does not have a signal due to oxygen vacancies, which can be evaluated by electron spin resonance (ESR). Specifically, the spin density attributed to oxygen vacancies of the oxide semiconductor film is lower than 5×10^{16} spins/cm^3. When the oxide semiconductor film has oxygen vacancies, a signal having symmetry is found at a g value of around 1.93 in ESR.

[0117] It is preferable that the base insulating film **102** be sufficiently flat. Specifically, the base insulating film **102** has an average surface roughness (R_a) of 1 nm or less, preferably 0.3 nm or less, further preferably 0.1 nm or less. When R_a is less than or equal to the above value, the oxide semiconductor film **106** can have high crystallinity. Further, when the degree of roughness at the interface between the base insulating film **102** and the oxide semiconductor film **106** is small, the influence of interface scattering can be reduced. Note that R_a is obtained by expanding arithmetic mean surface roughness, which is defined by JIS B 0601: 2001 (ISO4287: 1997), into three dimensions so as to be applied to a curved surface. In addition, R_a can be expressed as "an average value of the absolute values of deviations from a reference surface to a specific surface" and is defined by Formula (17).

$$Ra = \frac{1}{S_0}\int_{y1}^{y2}\int_{x1}^{x2}|f(x, y) - Z_0|dxdy \tag{17}$$

[0118] Here, the specific surface is a surface which is a target of roughness measurement, and is a quadrilateral region which is specified by four points represented by the coordinates $(x_1, y_1, f(x_1, y_1))$, $(x_1, y_2, f(x_1, y_2))$, $(x_2, y_1, f(x_2, y_1))$, and $(x_2, y_2, f(x_2, y_2))$. Moreover, S_0 represents the area of a rectangle which is obtained by projecting the specific surface on the xy plane, and Z_0 represents the height of the reference surface (the average height of the specific surface). Further, R_a can be measured using an atomic force microscope (AFM).

[0119] The base insulating film **102** is preferably an insulating film containing excess oxygen.

[0120] An insulating film containing excess oxygen refers to an insulating film in which the amount of released oxygen which is converted into oxygen atoms is greater than or equal to 1×10^{18} atoms/cm^3, greater than or equal to 1×10^{19} atoms/cm^3, or greater than or equal to 1×10^{20} atoms/cm^3 in thermal desorption spectroscopy (TDS).

[0121] Here, a method for measuring the amount of released oxygen using TDS will be described.

[0122] The total amount of released gas in TDS is proportional to the integral value of the ion intensity of the released gas. Then, this integral value is compared with the reference value of a standard sample, whereby the total amount of the released gas can be calculated.

[0123] For example, the number of released oxygen molecules (N_{O2}) from an insulating film can be calculated according to Formula (18) using the TDS results of a silicon wafer containing hydrogen at a predetermined density, which is the standard sample, and the TDS results of the insulating film. Here, all gasses having a mass number of 32 which are obtained by the TDS are assumed to originate from an oxygen molecule. CH_3OH can be given as a gas having a mass number of 32, but is not taken into consideration on the assumption that CH_3OH is unlikely to be present. Further, an oxygen molecule including an oxygen atom having a mass number of 17 or 18, which is an isotope of an oxygen atom, is also not taken into consideration because the proportion of such a molecule in the natural world is minimal.

$$N_{O2} = \frac{N_{H2}}{S_{H2}} \times S_{O2} \times \alpha \tag{18}$$

[0124] N_{H2} is the value obtained by conversion of the number of hydrogen molecules desorbed from the standard sample into density. S_{H2} is the integral value of ion intensity when the standard sample is analyzed by TDS. Here, the reference value of the standard sample is expressed by N_{H2}/S_{H2}. S_{O2} is the integral value of ion intensity when the insulating film is analyzed by TDS, and α is a coefficient affecting the ion intensity in the TDS. For details of Formula (18), Japanese Published Patent Application No. H6-275697 is referred to. Note that the amount of released oxygen from the insulating film was measured with a thermal desorption spectroscopy apparatus produced by ESCO Ltd., EMD-WA1000S/W using a silicon wafer containing hydrogen atoms at 1×10^{16} atoms/cm^3 as the standard sample.

[0125] Further, in the TDS, oxygen is partly detected as an oxygen atom. The ratio between oxygen molecules and oxygen atoms can be calculated from the ionization rate of oxygen molecules. Note that, since the above α is determined considering the ionization rate of oxygen molecules, the number of released oxygen atoms can be estimated through the evaluation of the number of the released oxygen molecules.

[0126] Note that N_{O2} is the number of released oxygen molecules. When the number of released oxygen molecules is converted into the number of released oxygen atoms, the number of released oxygen atoms is twice the number of released oxygen molecules.

[0127] The insulating film containing excess oxygen may contain a peroxide radical. Specifically, the spin density attributed to a peroxide radical of the insulating film is 5×10^{17} spins/cm^3 or higher. Note that the insulating film containing a peroxide radical has a signal having asymmetry at a g value of around 2.01 in ESR.

[0128] The insulating film containing excess oxygen may be formed using oxygen-excess silicon oxygen (SiO_x (X>2)). In the oxygen-excess silicon oxide (SiO_x (X>2)), the number of oxygen atoms per unit volume is more than twice the number of silicon atoms per unit volume. The number of silicon atoms and the number of oxygen atoms per unit volume are measured by Rutherford backscattering spectrometry.

[0129] The base insulating film **102** may be formed of a single layer or a stacked layer using one or more of the following materials: aluminum oxide, aluminum nitride, magnesium oxide, silicon oxide, silicon oxynitride, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide. In addition to the single layer or the stacked layer, silicon nitride oxide or silicon nitride may be stacked.

[0130] The amount of oxygen is larger than that of nitrogen in silicon oxynitride, and the amount of nitrogen is larger than that of oxygen in silicon nitride oxide.

[0131] The gate insulating film **112** is preferably an insulating film containing excess oxygen.

[0132] The gate insulating film **112** may be formed of a single layer or a stacked layer using one or more of the following materials: aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide.

[0133] "Excess oxygen" contained in at least one of the base insulating film **102** and the gate insulating film **112** means that the oxygen content is in excess of that in the stoichiometric composition. Therefore, "excess oxygen" is released when energy such as heat is applied to the film. Since "excess oxygen" means that the oxygen content is in excess of that in the stoichiometric composition, the film quality is not impaired even when "excess oxygen" is released from the film.

[0134] For example, the oxygen vacancies in the oxide semiconductor film **106** can be reduced by oxygen supplied from at least one of the base insulating film **102** and the gate insulating film **112**. That is, when the oxygen vacancies in the oxide semiconductor film **106** are reduced, a shift of the threshold voltage of the transistor in the negative direction can be prevented. For that purpose, at least one of the base insulating film and the gate insulating film may be an insulating film containing excess oxygen.

[0135] Note that when heat treatment is performed in the state where the oxide semiconductor film **106** is interposed between the base insulating film **102** and the gate insulating film **112**, oxygen released from the base insulating film **102** can be efficiently supplied to the oxide semiconductor film **106**. By performing the heat treatment at a temperature higher than or equal to 250° C. and lower than or equal to 550° C., oxygen can be supplied to the oxide semiconductor film **106**, and in addition, the hydrogen concentration in the oxide semiconductor film **106**, that in the base insulating film **102**, and that in the gate insulating film **112** can be reduced.

[0136] However, excess oxygen contained in at least one of the base insulating film **102** and the gate insulating film **112** might be lost through the heat treatment in some cases. In order to reduce a change in electrical characteristics of the transistor, at least one of the base insulating film **102** and the gate insulating film **112** preferably contains excess oxygen even after the heat treatment is performed.

[0137] There is no particular limitation on the substrate **100** as long as it has heat resistance enough to withstand at least heat treatment performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, or a sapphire substrate may be used as the substrate **100**. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, a silicon-on-insulator (SOI) substrate, or the like may be used. Still alternatively, any of these substrates provided with a semiconductor element may be used as the substrate **100**.

[0138] In the case of using a large glass substrate such as the fifth generation (1000 mm×1200 mm or 1300 mm×1500 mm); the sixth generation (1500 mm×1800 mm); the seventh generation (1870 mm×2200 mm); the eighth generation (2200 mm×2500 mm); the ninth generation (2400 mm×2800 mm); or the tenth generation (2880 mm×3130 mm) as the substrate **100**, microfabrication is difficult in some cases due to the shrinkage of the substrate **100**, which is caused by heat treatment or the like in a manufacturing process of the semiconductor device. Therefore, in the case where the above-described large glass substrate is used as the substrate **100**, a substrate which is unlikely to shrink through the heat treatment is preferably used. For example, a large-sized glass substrate which has a shrinkage of 10 ppm or less, preferably 5 ppm or less, more preferably 3 ppm or less after heat treatment at 400° C., preferably at 450° C., more preferably 500° C. for one hour may be used as the substrate **100**.

[0139] Further alternatively, a flexible substrate may be used as the substrate **100**. Note that as a method for forming a transistor over a flexible substrate, there is a method in which, after a transistor is formed over a non-flexible substrate, the transistor is separated from the non-flexible substrate and transferred to the substrate **100** which is a flexible substrate. In that case, a separation layer is preferably provided between the non-flexible substrate and the transistor.

[0140] The gate electrode **104** may be formed of a single layer or a stacked layer of a simple substance selected from Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W; a nitride containing one or more kinds of the above substances; an oxide containing one or more kinds of the above substances; or an alloy containing one or more kinds of the above substances.

[0141] The interlayer insulating film **118** may be formed of a single layer or a stacked layer using one or more materials containing any of aluminum oxide, aluminum nitride, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide.

[0142] It is preferable that the interlayer insulating film **118** have low relative permittivity and a sufficient thickness. For example, a silicon oxide film having a relative permittivity of approximately 3.8 and a thickness greater than or equal to 200 nm and less than or equal to 1000 nm may be provided. A top surface of the interlayer insulating film **118** has a little fixed charge because of the influence of atmospheric components and the like, which might cause the shift of the threshold voltage of the transistor. Therefore, it is preferable that the interlayer insulating film **118** have relative permittivity and a thickness such that the influence of the charge at the top surface is sufficiently reduced. For the same reason, a resin film of a polyimide resin, an acrylic resin, an epoxy resin, a silicone resin, or the like may be formed over the interlayer insulating film **118** in order to reduce the influence of the charge at the top surface of the interlayer insulating film **118**.

[0143] The wirings **136** may be formed of a single layer or a stacked layer of a simple substance selected from Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W; a nitride containing one or more kinds of the above substances; an oxide containing one or more kinds of the above substances; or an alloy containing one or more kinds of the above substances.

[0144] A transistor having a structure different from that of the transistor illustrated in FIGS. **1**A to **1**C will be described with reference to FIGS. **2**A to **2**C.

[0145] FIG. **2**A is a top view of a transistor according to one embodiment of the present invention. FIG. **2**B is a cross-sectional view taken along dashed-dotted line B**1**-B**2** in FIG. **2**A. FIG. **2**C is a cross-sectional view taken along dashed-dotted line B**3**-B**4** in FIG. **2**A. Note that the base insulating film **102** and the like are not illustrated in FIG. **2**A for simplicity.

[0146] In FIG. **2**A, the channel length (L) and the channel width (W) of the transistor are shown. Note that the channel region of the transistor corresponds to a region of the oxide semiconductor film **106** overlapping with the gate electrode **104**. At least part of two side surfaces of the oxide semiconductor film **106** overlap with the gate electrode **104**.

[0147] In the transistor illustrated in FIG. **2**A, the channel length is greater than or equal to 5 nm and less than 60 nm, and the channel width is greater than or equal to 5 nm and less than 200 nm.

[0148] Further, in the transistor illustrated in FIG. **2**A, the ratio of the channel width to the channel length is 0.5:1 to 10:1.

[0149] FIG. **2**B illustrates a cross-sectional structure of the transistor including the base insulating film **102** provided over the substrate **100**; the oxide semiconductor film **106** provided over the base insulating film **102**; the gate insulating film **112** provided over the oxide semiconductor film **106**; the gate electrode **104** provided over the gate insulating film **112** so as to overlap with the oxide semiconductor film **106**; and a barrier film **108** which is provided over the base insulating film **102**, the oxide semiconductor film **106**, and the gate electrode **104** and has openings reaching the oxide semiconductor film **106**.

[0150] Note that in FIG. **2**B, the interlayer insulating film **118** which is provided over the oxide semiconductor film **106** and the gate electrode **104** and has openings reaching the oxide semiconductor film **106**, and the wirings **136** provided in contact with the oxide semiconductor film **106** through the openings in the interlayer insulating film **118** are illustrated.

[0151] The transistor in FIGS. **2**A to **2**C is different from the transistor in FIGS. **1**A to **1**C only in the presence of the barrier film **108** which is provided over the base insulating film **102**, the oxide semiconductor film **106**, and the gate electrode **104** and has the openings reaching the oxide semiconductor film **106**. Therefore, for structures of the other components, the description with reference to FIGS. **1**A to **1**C can be referred to.

[0152] The barrier film **108** is an insulating film having low oxygen permeability. Specifically, the barrier film **108** is an insulating film through which oxygen does not pass even when heat treatment is performed at 350° C. for one hour.

[0153] The barrier film **108** may be formed of a single layer or a stacked layer using one or more of the following materials: aluminum oxide, aluminum nitride, magnesium oxide,

germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide. In particular, an aluminum oxide film is preferably used.

[0154] In the transistor in FIGS. **2**A to **2**C, outward diffusion of excess oxygen contained in the base insulating film **102** or the gate insulating film **112** can be prevented because of the barrier film **108** which is provided over the base insulating film **102**, the oxide semiconductor film **106**, and the gate electrode **104** and has the openings reaching the oxide semiconductor film **106**. Therefore, excess oxygen contained in the base insulating film **102** or the gate insulating film **112** can be efficiently supplied to the oxide semiconductor film **106**. That is, a shift of the threshold voltage of the transistor in the negative direction can be further suppressed in comparison with the transistor in FIGS. **1**A to **1**C.

[0155] A transistor having a structure different from those of the transistors illustrated in FIGS. **1**A to **1**C and FIGS. **2**A to **2**C will be described with reference to FIGS. **3**A to **3**C.

[0156] FIG. **3**A is a top view of a transistor according to one embodiment of the present invention. FIG. **3**B is a cross-sectional view taken along dashed-dotted line C**1**-C**2** in FIG. **3**A. FIG. **3**C is a cross-sectional view taken along dashed-dotted line C**3**-C**4** in FIG. **3**A. Note that the base insulating film **102** and the like are not illustrated in FIG. **3**A for simplicity.

[0157] In FIG. **3**A, the channel length (L) and the channel width (W) of the transistor are shown. Note that the channel region of the transistor corresponds to a region of the oxide semiconductor film **106** overlapping with the gate electrode **104**. At least part of two side surfaces of the oxide semiconductor film **106** overlap with the gate electrode **104**.

[0158] In the transistor illustrated in FIG. **3**A, the channel length is greater than or equal to 5 nm and less than 60 nm, and the channel width is greater than or equal to 5 nm and less than 200 nm.

[0159] Further, in the transistor illustrated in FIG. **3**A, the ratio of the channel width to the channel length is 0.5:1 to 10:1.

[0160] FIG. **3**B illustrates a cross-sectional structure of the transistor including the base insulating film **102** provided over the substrate **100**; the oxide semiconductor film **106** provided over the base insulating film **102**; a gate insulating film **132** which is provided over the oxide semiconductor film **106** and includes a first layer **132***a* and a second layer **132***b*; and the gate electrode **104** provided over the gate insulating film **132** so as to overlap with the oxide semiconductor film **106**. Note that the first layer **132***a* is closer to the oxide semiconductor film **106** than the second layer **132***b*.

[0161] Note that in FIG. **3**B, the interlayer insulating film **118** which is provided over the oxide semiconductor film **106** and the gate electrode **104** and has openings reaching the oxide semiconductor film **106**, and the wirings **136** provided in contact with the oxide semiconductor film **106** through the openings in the interlayer insulating film **118** are illustrated.

[0162] The transistor in FIGS. **3**A to **3**C is different from the transistor in FIGS. **1**A to **1**C only in that the gate insulating film **132** including the first layer **132***a* and the second layer **132***b* is provided instead of the gate insulating film **112**. Therefore, for structures of the other components, the description with reference to FIGS. **1**A to **1**C can be referred to.

[0163] Here, the first layer **132***a* is formed using an insulating film containing excess oxygen.

[0164] The first layer **132***a* may be formed of a single layer or a stacked layer using one or more of the following materials: aluminum oxide, aluminum nitride, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide.

[0165] The second layer **132***b* is formed using an insulating film having low oxygen permeability. Specifically, an insulating film through which oxygen does not pass even when heat treatment is performed at 350° C. for one hour is used.

[0166] The second layer **132***b* may be formed of a single layer or a stacked layer using one or more of the following materials: aluminum oxide, aluminum nitride, magnesium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide. In particular, an aluminum oxide film is preferably used.

[0167] As illustrated in FIG. **3**C, the first layer **132***a* is provided in contact with parts of the side surfaces of the oxide semiconductor film **106** overlapping with the gate electrode **104**. Therefore, oxygen can be supplied from the first layer **132***a* to the side surfaces of the oxide semiconductor film **106** overlapping with the gate electrode **104**. Since the second layer **132***b* is provided so as to cover the first layer **132***a*, oxygen can be efficiently supplied from the first layer **132***a*.

[0168] A parasitic channel is formed on the side surfaces of the oxide semiconductor film depending on the properties of the side surfaces of the oxide semiconductor film. The threshold voltage for forming the parasitic channel is generally lower than that for forming the original channel of the transistor. Therefore, when the influence of the parasitic channel becomes large, it seems as if the threshold voltage of the transistor shifts in the negative direction. This is because carriers are easily generated on the side surfaces of the oxide semiconductor film. For that reason, it is important that the side surfaces of the oxide semiconductor film be supplied with a larger amount of oxygen than the other surfaces of the oxide semiconductor film.

[0169] The influence of the parasitic channel becomes noticeable in a short-channel transistor in some cases; thus, the structure illustrated in FIGS. **3**A to **3**C is effective for a miniaturized transistor.

[0170] In the transistor in FIGS. **3**A to **3**C, the parasitic channel is unlikely to be formed on the side surfaces of the oxide semiconductor film **106** overlapping with the gate electrode **104**. That is, a shift of the threshold voltage of the transistor in the negative direction can be further suppressed in comparison with the transistor in FIGS. **1**A to **1**C.

[0171] A transistor having a structure different from those of the transistors illustrated in FIGS. **1**A to **1**C, FIGS. **2**A to **2**C, and FIGS. **3**A to **3**C will be described with reference to FIGS. **4**A to **4**C.

[0172] FIG. **4**A is a top view of a transistor according to one embodiment of the present invention. FIG. **4**B is a cross-sectional view taken along dashed-dotted line D**1**-D**2** in FIG. **4**A. FIG. **4**C is a cross-sectional view taken along dashed-dotted line D**3**-D**4** in FIG. **4**A. Note that the base insulating film **102** and the like are not illustrated in FIG. **4**A for simplicity.

[0173] In FIG. **4**A, the channel length (L) and the channel width (W) of the transistor are shown. Note that the channel region of the transistor corresponds to a region of the oxide semiconductor film **106** overlapping with the gate electrode

104. At least part of two side surfaces of the oxide semiconductor film **106** overlap with the gate electrode **104**.

[0174] In the transistor illustrated in FIG. **4**A, the channel length is greater than or equal to 5 nm and less than 60 nm, and the channel width is greater than or equal to 5 nm and less than 200 nm.

[0175] Further, in the transistor illustrated in FIG. **4**A, the ratio of the channel width to the channel length is 0.5:1 to 10:1.

[0176] FIG. **4**B illustrates a cross-sectional structure of the transistor including the base insulating film **102** provided over the substrate **100**; the oxide semiconductor film **106** provided over the base insulating film **102**; the gate insulating film **132** which is provided over the oxide semiconductor film **106** and includes the first layer **132***a* and the second layer **132***b*; the gate electrode **104** provided over the gate insulating film **132** so as to overlap with the oxide semiconductor film **106**; and the bather film **108** which is provided over the base insulating film **102**, the oxide semiconductor film **106**, and the gate electrode **104** and has openings reaching the oxide semiconductor film **106**. Note that the first layer **132***a* is closer to the oxide semiconductor film **106** than the second layer **132***b*.

[0177] Note that in FIG. **4**B, the interlayer insulating film **118** which is provided over the oxide semiconductor film **106** and the gate electrode **104** and has openings reaching the oxide semiconductor film **106**, and the wirings **136** provided in contact with the oxide semiconductor film **106** through the openings in the interlayer insulating film **118** are illustrated.

[0178] The transistor in FIGS. **4**A to **4**C is the same as the transistor in FIGS. **2**A to **2**C in the presence of the barrier film **108** which is provided over the base insulating film **102**, the oxide semiconductor film **106**, and the gate electrode **104** and has the openings reaching the oxide semiconductor film **106**. Further, the transistor in FIGS. **4**A to **4**C is the same as the transistor in FIGS. **3**A to **3**C in that the gate insulating film **132** including the first layer **132***a* and the second layer **132***b* is provided instead of the gate insulating film **112**. Therefore, for the structure of the transistor in FIGS. **4**A to **4**C, the description with reference to FIGS. **1**A to **1**C, FIGS. **2**A to **2**C, and FIGS. **3**A to **3**C can be referred to.

[0179] In the transistor in FIGS. **4**A to **4**C, outward diffusion of excess oxygen contained in the base insulating film **102** or the first layer **132***a* can be prevented because of the barrier film **108** which is provided over the base insulating film **102**, the oxide semiconductor film **106**, and the gate electrode **104** and has the openings reaching the oxide semiconductor film **106**. Therefore, excess oxygen contained in the base insulating film **102** or the first layer **132***a* can be efficiently supplied to the oxide semiconductor film **106**. That is, a shift of the threshold voltage of the transistor in the negative direction can be suppressed.

[0180] As illustrated in FIG. **4**C, the first layer **132***a* is provided in contact with parts of the side surfaces of the oxide semiconductor film **106** overlapping with the gate electrode **104**. Therefore, oxygen can be supplied from the first layer **132***a* to the side surfaces of the oxide semiconductor film **106** overlapping with the gate electrode **104**. Since the second layer **132***b* is provided so as to cover the first layer **132***a*, oxygen can be efficiently supplied from the first layer **132***a*.

[0181] Therefore, in the transistor in FIGS. **4**A to **4**C, the parasitic channel is unlikely to be formed on the side surfaces of the oxide semiconductor film **106** overlapping with the gate electrode **104**. That is, a shift of the threshold voltage of the transistor in the negative direction can be suppressed.

[0182] From the above, a transistor including an oxide semiconductor film with a large channel width (greater than or equal to 5 nm and less than 200 nm) is proposed as a transistor in which a short-channel effect is not substantially caused even when the channel length is short (greater than or equal to 5 nm and less than 60 nm).

[0183] Further, a transistor including an oxide semiconductor film having a constant ratio of a channel width to a channel length is proposed.

[0184] Furthermore, a transistor in which a shift of the threshold voltage in the negative direction due to oxygen vacancies in the oxide semiconductor film **106** and a shift of the threshold voltage in the negative direction due to a parasitic channel are suppressed is proposed.

[0185] From the above, a transistor that can have switching characteristics even when miniaturized can be provided.

[0186] A method of manufacturing the transistor in FIGS. **4**A to **4**C will be described below with reference to FIGS. **5**A to **5**C and FIGS. **6**A to **6**C. Note that the method of manufacturing the transistor in FIGS. **4**A to **4**C may be employed as appropriate for methods of manufacturing the transistors in FIGS. **1**A to **1**C, FIGS. **2**A to **2**C, and FIGS. **3**A to **3**C. Here, only cross-sectional views corresponding to FIG. **4**B are illustrated for simplicity.

[0187] First, the substrate **100** is prepared.

[0188] Next, the base insulating film **102** is formed over the substrate **100** (see FIG. **5**A). The base insulating film **102** may be formed using any of the above materials for the base insulating film **102** by a sputtering method, a chemical vapor deposition (CVD) method, a molecular beam epitaxy (MBE) method, an atomic layer deposition (ALD) method, or a pulsed laser deposition (PLD) method.

[0189] Here, the base insulating film **102** may be subjected to dehydration or dehydrogenation treatment. For example, heat treatment can be performed as the dehydration or dehydrogenation treatment. The heat treatment may be performed at a temperature higher than or equal to 250° C. and lower than or equal to 650° C., preferably higher than or equal to 300° C. and lower than or equal to 500° C. The heat treatment is performed in an inert gas atmosphere, an atmosphere containing an oxidizing gas at 10 ppm or more, preferably 1% or more, more preferably 10% or more, or under reduced pressure. Alternatively, the heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, preferably 1% or more, more preferably 10% or more in order to compensate desorbed oxygen. Alternatively, as the dehydration or dehydrogenation treatment, plasma treatment, UV treatment, or chemical treatment may be performed.

[0190] Then, oxygen may be added to the base insulating film **102** from the upper surface side of the base insulating film **102**. The addition of oxygen may be performed by an ion implantation method or an ion doping method. In that case, the acceleration voltage is made higher than or equal to 5 kV and lower than or equal to 100 kV. The amount of added oxygen is made greater than or equal to 1×10^{14} ions/cm^2 and less than or equal to 1×10^{16} ions/cm^2. Note that oxygen may be further added to the base insulating film **102** from the upper surface side of the base insulating film **102** under a different condition.

[0191] Alternatively, the addition of oxygen may be performed by application of a bias voltage to the substrate side in plasma containing oxygen. In that case, the bias voltage is made higher than or equal to 10 V and lower than 1 kV. The application time of the bias voltage is made longer than or equal to 10 s and shorter than or equal to 1000 s, preferably longer than or equal to 10 s and shorter than or equal to 200 s, more preferably longer than or equal to 10 s and shorter than or equal to 60 s. The higher the bias voltage is and the longer the application time of the bias voltage is, the larger the amount of added oxygen becomes; however, etching of the film accompanying the application of the bias voltage becomes non-negligible.

[0192] By the addition of oxygen, the base insulating film **102** can be an insulating film containing excess oxygen. Note that the formation method of the insulating film containing excess oxygen is not limited to the above. For example, the insulating film containing excess oxygen can be formed also by a sputtering method under an atmosphere containing a high proportion of oxygen with the substrate temperature higher than or equal to room temperature (approximately 25° C.) and lower than or equal to 150° C. Specifically, the proportion of an oxidizing gas such as oxygen in a deposition gas may be set to 20% or higher, preferably 50% or higher, more preferably 80% or higher. The formation methods of the insulating film containing excess oxygen may be combined as appropriate.

[0193] The base insulating film **102** containing excess oxygen may be formed in the above manner. Note that this embodiment is not limited to the case where the base insulating film **102** contains excess oxygen.

[0194] Since the base insulating film **102** preferably has sufficient planarity, the base insulating film **102** may be subjected to planarization treatment. As the planarization treatment, chemical mechanical polishing (CMP) or a dry etching method may be used. Specifically, the base insulating film **102** is provided so as to have an average surface roughness (R_a) of 1 nm or less, preferably 0.3 nm or less, more preferably 0.1 nm or less.

[0195] Next, an oxide semiconductor film is formed. The oxide semiconductor film may be formed using any of the above materials for the oxide semiconductor film **106** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method. The oxide semiconductor film is preferably formed by a sputtering method. At this time, a deposition gas which includes an oxidizing gas such as oxygen at 5% or more, preferably 10% or more, further preferably 20% or more, still further preferably 50% or more is used. As the deposition gas, a gas in which the concentration of impurities such as hydrogen is low is used.

[0196] After the oxide semiconductor film is formed, first heat treatment may be performed. The first heat treatment may be performed at a temperature higher than or equal to 250° C. and lower than or equal to 650° C., preferably higher than or equal to 300° C. and lower than or equal to 500° C. The first heat treatment is performed in an inert gas atmosphere, an atmosphere containing an oxidizing gas at 10 ppm or more, preferably 1% or more, further preferably 10% or more, or under reduced pressure. Alternatively, the first heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, preferably 1% or more, further preferably 10% or more in order to compensate desorbed oxygen. By the first heat treatment, impurities such as hydrogen and water can be removed from the oxide semiconductor film.

[0197] Next, the oxide semiconductor film is processed to form an island-shaped oxide semiconductor film **107** (see FIG. **5**B).

[0198] Then, a first layer **133***a* is formed. The first layer **133***a* may be formed using any of the above materials for the first layer **132***a* by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0199] Here, the first layer **133***a* may be subjected to dehydration or dehydrogenation treatment. For example, heat treatment can be performed as the dehydration or dehydrogenation treatment. The heat treatment may be performed at a temperature higher than or equal to 250° C. and lower than or equal to 650° C., preferably higher than or equal to 300° C. and lower than or equal to 500° C. The heat treatment is performed in an inert gas atmosphere, an atmosphere containing an oxidizing gas at 10 ppm or more, preferably 1% or more, more preferably 10% or more, or under reduced pressure. Alternatively, the heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, preferably 1% or more, more preferably 10% or more in order to compensate desorbed oxygen. Alternatively, as the dehydration or dehydrogenation treatment, plasma treatment, UV treatment, or chemical treatment may be performed.

[0200] Then, oxygen may be added to the first layer **133***a* from the upper surface side of the first layer **133***a*. The addition of oxygen may be performed by an ion implantation method or an ion doping method. In that case, the acceleration voltage is made higher than or equal to 5 kV and lower than or equal to 100 kV. The amount of added oxygen is made greater than or equal to 1×10^{14} ions/cm^2 and less than or equal to 1×10^{16} ions/cm^2. Note that oxygen may be further added to the first layer **133***a* from the upper surface side of the first layer **133***a* under a different condition.

[0201] Alternatively, the addition of oxygen may be performed by application of a bias voltage to the substrate side in plasma containing oxygen. In that case, the bias voltage is made higher than or equal to 10 V and lower than 1 kV. The application time of the bias voltage is made longer than or equal to 10 s and shorter than or equal to 1000 s, preferably longer than or equal to 10 s and shorter than or equal to 200 s, more preferably longer than or equal to 10 s and shorter than or equal to 60 s.

[0202] By the addition of oxygen, the first layer **133***a* can be an insulating film containing excess oxygen. Note that the formation method of the insulating film containing excess oxygen is not limited to the above. For example, the insulating film containing excess oxygen can be formed also by a sputtering method under an atmosphere containing a high proportion of oxygen with the substrate temperature higher than or equal to room temperature and lower than or equal to 150° C. Specifically, the proportion of oxygen may be set to 20% or higher, preferably 50% or higher, more preferably 80% or higher. The formation methods of the insulating film containing excess oxygen may be combined as appropriate.

[0203] The first layer **133***a* containing excess oxygen may be formed in the above manner. Note that this embodiment is not limited to the case where the first layer **133***a* contains excess oxygen.

[0204] Next, a second layer **133***b* is formed. The second layer **133***b* may be formed using any of the above materials for the second layer **132***b* by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0205] Then, a conductive film **105** is formed (see FIG. **5**C). The conductive film **105** may be formed using any of the above materials for the gate electrode **104** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0206] Next, the conductive film **105** is processed to form the gate electrode **104**.

[0207] Next, the second layer **133***b* and the first layer **133***a* are processed with the use of the gate electrode **104** as a mask or with the use of a mask used for the processing for forming the gate electrode **104**, whereby the gate insulating film **132** including the second layer **132***b* and the first layer **132***a* is formed (see FIG. **6**A).

[0208] Then, an impurity is added to the oxide semiconductor film **107** with the gate electrode **104** used as a mask. As the impurity, one or more of helium, boron, nitrogen, fluorine, neon, aluminum, phosphorus, argon, arsenic, krypton, indium, tin, antimony, and xenon may be added. The impurity may be added by an ion implantation method or an ion doping method. At this time, the acceleration voltage is made higher than or equal to 5 kV and lower than or equal to 100 kV. The amount of the added impurity is made greater than or equal to 1×10^{14} ions/cm^2 and less than or equal to 1×10^{16} ions/cm^2. After that, heat treatment may be performed.

[0209] By the addition of the impurity (and the heat treatment), the resistance of part of the oxide semiconductor film **107** is reduced. Here, regions whose resistance is reduced become the regions **106***b*, and a region whose resistance is not reduced becomes the region **106***a*; the regions **106***b* and the region **106***a* are collectively referred to as the oxide semiconductor film **106**.

[0210] Note that a method of adding the impurity to the oxide semiconductor film **107** after the gate insulating film **132** is formed is described in this embodiment; however, the order of the steps is not limited thereto. For example, the impurity may be added to the oxide semiconductor film **107** through the second layer **133***b* and the first layer **133***a* after the gate electrode **104** is formed. By the addition of the impurity through the second layer **133***b* and the first layer **133***a*, damage to the oxide semiconductor film **107** is unlikely to be caused.

[0211] Next, the barrier film **108** is formed (see FIG. **6**B). The barrier film **108** may be formed using any of the above materials for the barrier film **108** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0212] After the barrier film **108** is formed, second heat treatment is performed. By the second heat treatment, oxygen can be released from the base insulating film **102** and/or the gate insulating film **132**. Released oxygen is supplied to the oxide semiconductor film **106**, whereby oxygen vacancies can be reduced. Further, an influence of a parasitic channel can be reduced. The second heat treatment may be performed under a condition similar to that of the first heat treatment.

[0213] There is no particular limitation on the timing of the second heat treatment as long as it is after the formation of the barrier film **108**. Note that the second heat treatment is not necessarily performed.

[0214] In this manner, the transistor in FIGS. **4**A to **4**C can be manufactured.

[0215] In the transistor in FIGS. **4**A to **4**C, the oxide semiconductor film **106** has few oxygen vacancies and an influence of a parasitic channel is small; thus, the transistor can have switching characteristics even when miniaturized.

[0216] Next, the interlayer insulating film **118** is formed over the barrier film **108**. The interlayer insulating film **118** may be formed using any of the above materials for the interlayer insulating film **118** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0217] Then, the openings are provided in the interlayer insulating film **118** and the barrier film **108**, so that the oxide semiconductor film **106** is exposed.

[0218] Then, a conductive film to be the wirings **136** is formed. The conductive film to be the wirings **136** may be formed using any of the above materials for the wirings **136** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0219] Next, the conductive film to be the wirings **136** is processed to form the wirings **136** (see FIG. **6**C).

[0220] According to this embodiment, a transistor that can have switching characteristics even when miniaturized can be provided. Further, a highly integrated semiconductor device including the transistor can be provided.

[0221] This embodiment can be implemented in appropriate combination with any of the other embodiments.

Embodiment 2

[0222] In this embodiment, a transistor having a different structure from any of the transistors in Embodiment 1 will be described.

[0223] FIG. **7**A is a top view of a transistor according to one embodiment of the present invention. FIG. **7**B is a cross-sectional view taken along dashed-dotted line E**1**-E**2** in FIG. **7**A. FIG. **7**C is a cross-sectional view taken along dashed-dotted line E**3**-E**4** in FIG. **7**A. Note that a base insulating film **202** and the like are not illustrated in FIG. **7**A for simplicity.

[0224] In FIG. **7**A, the channel length (L) and the channel width (W) of the transistor are shown. Note that the channel region of the transistor corresponds to a region of an oxide semiconductor film **206** overlapping with a gate electrode **204**. At least two side surfaces of the oxide semiconductor film **206** overlap with the gate electrode **204**.

[0225] In the transistor illustrated in FIG. **7**A, the channel length is greater than or equal to 5 nm and less than 60 nm, and the channel width is greater than or equal to 5 nm and less than 200 nm.

[0226] Further, in the transistor illustrated in FIG. **7**A, the ratio of the channel width to the channel length is 0.5:1 to 10:1.

[0227] FIG. **7**B illustrates a cross-sectional structure of the transistor including the base insulating film **202** provided over a substrate **200**; the oxide semiconductor film **206** provided over the base insulating film **202**; a pair of electrodes **216** provided on the same layer as the oxide semiconductor film **206**; a gate insulating film **212** provided over the oxide semiconductor film **206**; and the gate electrode **204** provided over the gate insulating film **212** so as to overlap with the oxide semiconductor film **206**.

[0228] Note that in FIG. **7**B, an interlayer insulating film **218** which is provided over the oxide semiconductor film **206**, the pair of electrodes **216**, and the gate electrode **204** and has openings reaching the pair of electrodes **216**, and wirings **236** provided in contact with the pair of electrodes **216** through the openings in the interlayer insulating film **218** are illustrated.

[0229] The substrate **200** may be formed using a material similar to that for the substrate **100**.

[0230] The base insulating film **202** may be formed using a material similar to that for the base insulating film **102**.

[0231] The gate electrode **204** may be formed using a material similar to that for the gate electrode **104**.

[0232] The gate insulating film **212** may be formed using a material similar to that for the gate insulating film **112**. Note that the gate insulating film **212** may have a layer structure similar to that of the gate insulating film **132**.

[0233] The oxide semiconductor film **206** may be formed using a material similar to that for the oxide semiconductor film **106**.

[0234] The interlayer insulating film **218** may be formed using a material similar to that for the interlayer insulating film **118**.

[0235] The wirings **236** may be formed using a material similar to that for the wirings **136**.

[0236] The pair of electrodes **216** may be formed of a single layer or a stacked layer of a simple substance selected from Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W; a nitride containing one or more kinds of the above substances; an oxide containing one or more kinds of the above substances; or an alloy containing one or more kinds of the above substances.

[0237] Although not illustrated, a barrier film may be formed over the base insulating film **202**, the pair of electrodes **216**, the oxide semiconductor film **206**, and the gate electrode **204**. The barrier film may be formed using a material similar to that for the barrier film **108**, which enables the barrier film to have a function similar to that of the barrier film **108**.

[0238] From the above, the transistor in FIGS. **7**A to **7**C is different from the transistors in FIGS. **1**A to **1**C, FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, and FIGS. **4**A to **4**C in the shape of the oxide semiconductor film **206** and in the presence of the pair of electrodes **216**. Therefore, for structures of the other components, the description with reference to FIGS. **1**A to **1**C, FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, and FIGS. **4**A to **4**C can be referred to.

[0239] The transistor in FIGS. **7**A to **7**C has a structure in which the pair of electrodes **216** is provided instead of the regions **106***b* of the oxide semiconductor film **106** in the transistor in FIGS. **1**A to **1**C. Therefore, the resistance between a source and a drain can be made lower than that in any of the transistors described in Embodiment 1. Accordingly, such a transistor can have excellent on-state characteristics even when miniaturized.

[0240] A method of manufacturing the transistor in FIGS. **7**A to **7**C will be described below with reference to FIGS. **8**A to **8**D. Here, only cross-sectional views corresponding to FIG. **7**B are illustrated for simplicity.

[0241] First, the substrate **200** is prepared.

[0242] Next, the base insulating film **202** is formed over the substrate **200**. The base insulating film **202** may be formed using a material and a method similar to those for the base insulating film **102**.

[0243] Next, a conductive film to be the pair of electrodes **216** is formed. The conductive film to be the pair of electrodes **216** may be formed using any of the above materials for the pair of electrodes **216** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0244] Then, the conductive film to be the pair of electrodes **216** is processed to form a conductive film **217** having an opening through which the base insulating film **202** is exposed.

[0245] Next, an oxide semiconductor film **207** is formed (see FIG. **8**A). The oxide semiconductor film **207** may be formed using any of the above materials and methods for the oxide semiconductor film **106**.

[0246] After the oxide semiconductor film **207** is formed, first heat treatment may be performed. For the first heat treatment, the first heat treatment described in Embodiment 1 is referred to.

[0247] Next, planarization treatment is performed on the oxide semiconductor film **207** and the conductive film **217**. As the planarization treatment, CMP treatment or the like may be used. Through the planarization treatment, the oxide semiconductor film is provided only in the opening in the conductive film **217**.

[0248] Then, the conductive film **217** and the oxide semiconductor film provided only in the opening in the conductive film **217** are processed into an island shape, so that the oxide semiconductor film **206** and the pair of electrodes **216** are formed (see FIG. **8**B).

[0249] Next, the gate insulating film **212** and the gate electrode **204** over the gate insulating film **212** are formed (see FIG. **8**C). The gate insulating film **212** may be formed using a material and a method similar to those for the gate insulating film **112** or the gate insulating film **132**. The gate electrode **204** may be formed using a material and a method similar to those for the gate electrode **104**.

[0250] Then, a bather film may be formed. The barrier film may be formed using a material and a method similar to those for the barrier film **108**.

[0251] In this manner, the transistor in FIGS. **7**A to **7**C can be manufactured.

[0252] In the transistor in FIGS. **7**A to **7**C, the oxide semiconductor film **206** has few oxygen vacancies and an influence of a parasitic channel is small; thus, the transistor can have switching characteristics even when miniaturized. Further, since the pair of electrodes **216** is provided, the transistor can have excellent on-state characteristics even when miniaturized.

[0253] Next, the interlayer insulating film **218** is formed. The interlayer insulating film **218** may be formed using a material and a method similar to those for the interlayer insulating film **118**.

[0254] Then, the openings are provided in the interlayer insulating film **218**, so that the pair of electrodes **216** is exposed.

[0255] Next, the wirings **236** are formed. The wirings **236** may be formed using a material and a method similar to those for the wirings **136** (see FIG. **8**D).

[0256] According to this embodiment, a transistor that can have switching characteristics and excellent on-state characteristics even when miniaturized can be provided. Further, a highly integrated semiconductor device including the transistor can be provided.

[0257] This embodiment can be implemented in appropriate combination with any of the other embodiments.

Embodiment 3

[0258] In this embodiment, a transistor having a different structure from any of the transistors in Embodiments 1 and 2 will be described.

[0259] FIG. **9**A is a top view of a transistor according to one embodiment of the present invention. FIG. **9**B is a cross-sectional view taken along dashed-dotted line F**1**-F**2** in FIG. **9**A. FIG. **9**C is a cross-sectional view taken along dashed-dotted line F**3**-F**4** in FIG. **9**A. Note that a base insulating film **302** and the like are not illustrated in FIG. **9**A for simplicity.

[0260] In FIG. **9**A, the channel length (L) and the channel width (W) of the transistor are shown. Note that the channel region of the transistor corresponds to a region of an oxide semiconductor film **306** overlapping with a gate electrode **304**. At least two side surfaces of the oxide semiconductor film **306** overlap with the gate electrode **304**.

[0261] In the transistor illustrated in FIG. **9**A, the channel length is greater than or equal to 5 nm and less than 60 nm, and the channel width is greater than or equal to 5 nm and less than 200 nm.

[0262] Further, in the transistor illustrated in FIG. **9**A, the ratio of the channel width to the channel length is 0.5:1 to 10:1.

[0263] FIG. **9**B is a cross-sectional view of the transistor including the base insulating film **302** provided over a substrate **300**; the oxide semiconductor film **306** which is provided over the base insulating film **302** and includes a first region **306***a* and second regions **306***b*; a gate insulating film **312** provided over the oxide semiconductor film **306**; the gate electrode **304** provided over the gate insulating film **312** so as to overlap with the oxide semiconductor film **306**; an insulating film **320** provided over the gate electrode **304**; sidewall insulating films **310** provided in contact with side surfaces of the gate electrode **304** and the insulating film **320**; a pair of electrodes **316** provided over the oxide semiconductor film **306** and in contact with the sidewall insulating films **310** and the second regions **306***b* of the oxide semiconductor film **306**; and an interlayer insulating film **318** which is provided over the pair of electrodes **316** and whose top surface is level with that of the insulating film **320**.

[0264] Note that in FIG. **9**B, an interlayer insulating film **328** provided over the interlayer insulating film **318** and the insulating film **320**, and wirings **336** provided in contact with the pair of electrodes **316** through openings which are provided in the interlayer insulating film **318** and the interlayer insulating film **328** so as to reach the pair of electrodes **316** are illustrated.

[0265] In FIG. **9**B, the shape of the gate electrode **304** is similar to that of the insulating film **320** when seen from above. The shape of the gate insulating film **312** is similar to that of the gate electrode **304** and the sidewall insulating films **310** when seen from above.

[0266] The first region **306***a* of the oxide semiconductor film **306** serves as the channel region of the transistor. The second regions **306***b* of the oxide semiconductor film **306** serve as a source region and a drain region of the transistor.

[0267] In the transistor in FIGS. **9**A to **9**C, the pair of electrodes **316** is provided close to the gate electrode **304** with the sidewall insulating films **310** interposed therebetween. Therefore, the resistance between the source and the drain can be low. Accordingly, the transistor can have excellent on-state characteristics.

[0268] The substrate **300** may be formed using a material similar to that for the substrate **100**.

[0269] The base insulating film **302** may be formed using a material similar to that for the base insulating film **102**.

[0270] The gate electrode **304** may be formed using a material similar to that for the gate electrode **104**.

[0271] The gate insulating film **312** may be formed using a material similar to that for the gate insulating film **112**. Note that the gate insulating film **312** may have a layer structure similar to that of the gate insulating film **132**.

[0272] The oxide semiconductor film **306** may be formed using a material similar to that for the oxide semiconductor film **106**.

[0273] The sidewall insulating films **310** may be formed using one or more of the following materials: aluminum oxide, aluminum nitride, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide.

[0274] The insulating film **320** may be formed using one or more of the following materials: aluminum oxide, aluminum nitride, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide.

[0275] The pair of electrodes **316** may be formed using a material similar to that for the pair of electrodes **216**.

[0276] The interlayer insulating film **318** may be formed using a material similar to that for the interlayer insulating film **218**.

[0277] The interlayer insulating film **328** may be formed using a material similar to that for the interlayer insulating film **218**.

[0278] The wirings **336** may be formed using a material similar to that for the wirings **136**.

[0279] Although not illustrated, a barrier film may be formed over the base insulating film **302**, the pair of electrodes **316**, the oxide semiconductor film **306**, the insulating film **320**, and the gate electrode **304**. The barrier film may be formed using a material similar to that for the barrier film **108**, which enables the barrier film to have a function similar to that of the barrier film **108**.

[0280] A method of manufacturing the transistor in FIGS. **9**A to **9**C will be described below with reference to FIGS. **10**A to **10**C, FIGS. **11**A to **11**C, and FIGS. **12**A to **12**C. Here, only cross-sectional views corresponding to FIG. **9**B are illustrated for simplicity.

[0281] First, the substrate **300** is prepared.

[0282] Next, the base insulating film **302** is formed. The base insulating film **302** may be formed using a material and a method similar to those for the base insulating film **102**.

[0283] Next, an oxide semiconductor film **307** is formed. The oxide semiconductor film **307** may be formed using a material and a method similar to those for the oxide semiconductor film **107**.

[0284] Next, a gate insulating film **313** is formed. The gate insulating film **313** may be formed using a material and a method similar to those for the gate insulating film **112** or the gate insulating film **132**.

[0285] Next, a conductive film **305** is formed. The conductive film **305** may be formed using any of the above materials for the gate electrode **304** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0286] Then, an insulating film **321** is formed (see FIG. **10**A). The insulating film **321** may be formed using any of the above materials for the insulating film **320** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0287] Next, the insulating film **321** and the conductive film **305** are processed, whereby an insulating film **322** and the

gate electrode **304** are formed (see FIG. **10**B). The shape of the insulating film **322** is similar to that of the gate electrode **304** when seen from above.

[0288] Then, an impurity is added to the oxide semiconductor film **307** with the insulating film **322** and the gate electrode **304** used as masks. Specifically, as the impurity, one or more of helium, boron, nitrogen, fluorine, neon, aluminum, phosphorus, argon, arsenic, krypton, indium, tin, antimony, and xenon may be added. The impurity may be added by an ion implantation method or an ion doping method. Preferably, an ion implantation method is used. At this time, the acceleration voltage is made higher than or equal to 5 kV and lower than or equal to 100 kV. The amount of the added impurity is made greater than or equal to 1×10^{14} ions/cm^2 and less than or equal to 1×10^{16} ions/cm^2. After that, heat treatment may be performed.

[0289] The resistance of regions to which the impurity is added is reduced, and the regions become the second regions **306***b*. A region to which the impurity is not added becomes the first region **306***a*. Thus, the oxide semiconductor film **306** including the first region **306***a* and the second regions **306***b* is formed (see FIG. **10**C).

[0290] Next, an insulating film to be the sidewall insulating films **310** is formed. The insulating film to be the sidewall insulating films **310** may be formed using any of the above materials for the sidewall insulating films **310** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method. Then, highly anisotropic etching treatment is performed on the insulating film to be the sidewall insulating films **310**, whereby the sidewall insulating films **310** can be formed in contact with side surfaces of the insulating film **322** and the gate electrode **304**.

[0291] Processing of the gate insulating film **313** with the sidewall insulating films **310** and the gate electrode **304** used as masks is performed at the same time as the formation of the sidewall insulating films **310**, whereby the gate insulating film **312** is formed (see FIG. **11**A).

[0292] Then, a conductive film **317** is formed (see FIG. **11**B). The conductive film **317** may be formed using any of the above materials for the pair of electrodes **316** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0293] After the conductive film **317** is formed, second heat treatment is performed. By the second heat treatment, oxygen can be released from the base insulating film **302** and/or the gate insulating film **312**. Released oxygen is supplied to the oxide semiconductor film **306**, whereby oxygen vacancies can be reduced. The second heat treatment may be performed under a condition similar to that of the second heat treatment described in Embodiment 1.

[0294] The second heat treatment is not necessarily performed just after the formation of the conductive film **317**; there is no particular limitation on the timing of the second heat treatment as long as it is after the formation of the conductive film **317**.

[0295] Next, an interlayer insulating film **319** is formed (see FIG. **11**C). The interlayer insulating film **319** may be formed using any of the above materials for the interlayer insulating film **318** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0296] Next, planarization treatment (such as CMP treatment or dry etching treatment) is performed from the upper surface side of the interlayer insulating film **319**, whereby the pair of electrodes **316**, the interlayer insulating film **318**, the sidewall insulating films **310**, and the insulating film **320** are formed (see FIG. **12**A).

[0297] By performing the planarization treatment from the upper surface side of the interlayer insulating film **319**, only a region of the conductive film **317** overlapping with the insulating film **322** (and the gate electrode **304**) can be removed. At that time, the insulating film **322** is also subjected to the planarization treatment to be the insulating film **320** with a smaller thickness.

[0298] By the formation of the pair of electrodes **316** in this manner, the pair of electrodes **316** can be provided close to the gate electrode **304** with the sidewall insulating films **310** interposed therebetween.

[0299] In this manner, the transistor in FIGS. **9**A to **9**C can be manufactured.

[0300] In the transistor in FIGS. **9**A to **9**C, the oxide semiconductor film **306** has few oxygen vacancies and an influence of a parasitic channel is small; thus, the transistor can have switching characteristics even when miniaturized. Further, since the pair of electrodes **316** is provided, the transistor can have excellent on-state characteristics even when miniaturized.

[0301] Then, the interlayer insulating film **328** is formed (see FIG. **12**B). The interlayer insulating film **328** may be formed using any of the above materials for the interlayer insulating film **328** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0302] Next, the interlayer insulating film **328** and the interlayer insulating film **318** are processed, so that the openings through which the pair of electrodes **316** is exposed are formed.

[0303] Next, the wirings **336** are formed (see FIG. **12**C). The wirings **336** may be formed using a material and a method similar to those for the wirings **136**.

[0304] According to this embodiment, a transistor that can have switching characteristics and excellent on-state characteristics even when miniaturized can be provided. Further, a highly integrated semiconductor device including the transistor can be provided.

[0305] This embodiment can be implemented in appropriate combination with any of the other embodiments.

Embodiment 4

[0306] In this embodiment, a transistor having a different structure from any of the transistors in Embodiments 1 to 3 will be described.

[0307] FIG. **13**A is a top view of a transistor according to one embodiment of the present invention. FIG. **13**B is a cross-sectional view taken along dashed-dotted line G**1**-G**2** in FIG. **13**A. FIG. **13**C is a cross-sectional view taken along dashed-dotted line G**3**-G**4** in FIG. **13**A. Note that a base insulating film **402** and the like are not illustrated in FIG. **13**A for simplicity.

[0308] In FIG. **13**A, the channel length (L) and the channel width (W) of the transistor are shown. Note that the channel region of the transistor corresponds to a region of an oxide semiconductor film **406** overlapping with a gate electrode **404**. At least two side surfaces of the oxide semiconductor film **406** overlap with the gate electrode **404**.

[0309] In the transistor illustrated in FIG. **13**A, the channel length is greater than or equal to 5 nm and less than 60 nm, and the channel width is greater than or equal to 5 nm and less than 200 nm.

[0310] Further, in the transistor illustrated in FIG. **13**A, the ratio of the channel width to the channel length is 0.5:1 to 10:1.

[0311] FIG. **13**B illustrates a cross-sectional structure of the transistor including the base insulating film **402** provided over a substrate **400**; the oxide semiconductor film **406** which is provided over the base insulating film **402** and whose thickness is 1 to 5 times as large as the channel width; a gate insulating film **412** provided over the oxide semiconductor film **406**; and the gate electrode **404** provided over the gate insulating film **412** so as to overlap with the oxide semiconductor film **406**.

[0312] Note that in FIG. **13**B, an interlayer insulating film **418** which is provided over the oxide semiconductor film **406** and the gate electrode **404** and has openings reaching the oxide semiconductor film **406**, and wirings **436** provided in contact with the oxide semiconductor film **406** through the openings in the interlayer insulating film **418** are illustrated.

[0313] The transistor in FIGS. **13**A to **13**C is a so-called fin transistor. The fin transistor can have a large conduction path of carriers because of its thick channel region, and can have excellent on-state characteristics even in the case where the channel width is small.

[0314] In the case of a fin transistor including silicon, a depletion layer due to an electric field of a gate is not completely extended because of its thick channel region; thus, there is a problem in that it is difficult to completely turn off the transistor. On the other hand, in the case of a fin transistor including an oxide semiconductor film, a depletion layer due to an electric field of a gate can be sufficiently extended even when a channel region is thick; thus, the transistor can be turned off.

[0315] The substrate **400** may be formed using a material similar to that for the substrate **100**.

[0316] The base insulating film **402** may be formed using a material similar to that for the base insulating film **102**.

[0317] The gate electrode **404** may be formed using a material similar to that for the gate electrode **104**.

[0318] The gate insulating film **412** may be formed using a material similar to that for the gate insulating film **112**. Note that the gate insulating film **412** may have a layer structure similar to that of the gate insulating film **132**.

[0319] The oxide semiconductor film **406** may be formed using a material similar to that for the oxide semiconductor film **106**. The thickness of the oxide semiconductor film **406** is greater than or equal to 100 nm and less than 2 μm.

[0320] The interlayer insulating film **418** may be formed using a material similar to that for the interlayer insulating film **118**.

[0321] The wirings **436** may be formed using a material similar to that for the wirings **136**.

[0322] Although not illustrated, a barrier film may be formed over the base insulating film **402**, the oxide semiconductor film **406**, and the gate electrode **404**. The barrier film may be formed using a material similar to that for the barrier film **108**, which enables the barrier film to have a function similar to that of the barrier film **108**.

[0323] A method of manufacturing the transistor in FIGS. **13**A to **13**C will be described below with reference to FIGS. **14**A to **14**C. Here, only cross-sectional views corresponding to FIG. **13**B are illustrated for simplicity.

[0324] First, the substrate **400** is prepared.

[0325] Next, the base insulating film **402** is formed over the substrate **400**. The base insulating film **402** may be formed using a material and a method similar to those for the base insulating film **102**.

[0326] Next, an oxide semiconductor film **407** is formed (see FIG. **14**A). The oxide semiconductor film **407** may be formed using a material and a method similar to those for the oxide semiconductor film **107**.

[0327] Next, the gate insulating film **412** and the gate electrode **404** over the gate insulating film **412** are formed (see FIG. **14**B). The gate insulating film **412** may be formed using a material and a method similar to those for the gate insulating film **112** or the gate insulating film **132**. The gate electrode **404** may be formed using a material and a method similar to those for the gate electrode **104**.

[0328] Then, an impurity is added to the oxide semiconductor film **407** with the gate electrode **404** used as a mask. Specifically, as the impurity, one or more of helium, boron, nitrogen, fluorine, neon, aluminum, phosphorus, argon, arsenic, krypton, indium, tin, antimony, and xenon may be added. The impurity may be added by an ion implantation method or an ion doping method. Preferably, an ion implantation method is used. At this time, the acceleration voltage is made higher than or equal to 5 kV and lower than or equal to 100 kV. The amount of the added impurity is made greater than or equal to 1×10^{14} ions/cm^2 and less than or equal to 1×10^{16} ions/cm^2. After that, heat treatment may be performed.

[0329] Then, a bather film may be formed. The barrier film may be formed using a material and a method similar to those for the barrier film **108**.

[0330] In this manner, the transistor in FIGS. **13**A to **13**C can be manufactured.

[0331] In the transistor in FIGS. **13**A to **13**C, the oxide semiconductor film **406** has few oxygen vacancies and an influence of a parasitic channel is small; thus, the transistor can have switching characteristics even when miniaturized. Further, since the thickness of the oxide semiconductor film **406** is 1 to 5 times as large as the channel width, the transistor can have excellent on-state characteristics even when miniaturized.

[0332] Next, the interlayer insulating film **418** is formed. The interlayer insulating film **418** may be formed using a material and a method similar to those for the interlayer insulating film **118**.

[0333] Then, the openings are provided in the interlayer insulating film **418**, so that the oxide semiconductor film **406** is exposed.

[0334] Next, the wirings **436** are formed. The wirings **436** may be formed using a material and a method similar to those for the wirings **136** (see FIG. **14**C).

[0335] According to this embodiment, a transistor that can have switching characteristics and excellent on-state characteristics even when miniaturized can be provided. Further, a highly integrated semiconductor device including the transistor can be provided.

[0336] This embodiment can be implemented in appropriate combination with any of the other embodiments.

Embodiment 5

[0337] In this embodiment, a transistor having a different structure from any of the transistors in Embodiments 1 to 4 will be described.

[0338] FIG. **15**A is a top view of a transistor according to one embodiment of the present invention. FIG. **15**B is a cross-sectional view taken along dashed-dotted line H**1**-H**2** in FIG. **15**A. FIG. **15**C is a cross-sectional view taken along dashed-dotted line H**3**-H**4** in FIG. **15**A. Note that a base insulating film **502** and the like are not illustrated in FIG. **15**A for simplicity.

[0339] In FIG. **15**A, the channel length (L) and the channel width (W) of the transistor are shown. Note that the channel region of the transistor corresponds to a region of the oxide semiconductor film **506** which is located between a pair of electrodes **516** when seen from above. At least two side surfaces of the oxide semiconductor film **506** overlap with the gate electrode **504**.

[0340] In the transistor illustrated in FIG. **15**A, the channel length is greater than or equal to 5 nm and less than 60 nm, and the channel width is greater than or equal to 5 nm and less than 200 nm.

[0341] Further, in the transistor illustrated in FIG. **15**A, the ratio of the channel width to the channel length is 0.5:1 to 10:1.

[0342] FIG. **15**B is a cross-sectional view of the transistor including the base insulating film **502** provided over a substrate **500**; the gate electrode **504** provided over the base insulating film **502**; a gate insulating film **512** provided over the gate electrode **504**; the oxide semiconductor film **506** provided so as to overlap with the gate electrode **504** with the gate insulating film **512** therebetween; the pair of electrodes **516** provided over the oxide semiconductor film **506**; and an interlayer insulating film **518** provided over the pair of electrodes **516**.

[0343] The substrate **500** may be formed using a material similar to that for the substrate **100**.

[0344] The base insulating film **502** is provided in order that an impurity due to the substrate **500** is prevented from affecting the oxide semiconductor film **506**. Note that in the case where the substrate **500** does not include an impurity, the base insulating film **502** is not necessarily provided. Further, in the case where an impurity can be prevented from being diffused by the gate insulating film **512**, the base insulating film **502** is not necessarily provided.

[0345] The base insulating film **502** may be formed of a single layer or a stacked layer using one or more of the following materials: aluminum oxide, aluminum nitride, magnesium oxide, silicon oxide, silicon oxynitride, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide. In addition to the single layer or the stacked layer, silicon nitride oxide or silicon nitride may be stacked.

[0346] The gate electrode **504** may be formed using a material similar to that for the gate electrode **104**.

[0347] The gate insulating film **512** may be formed using a material similar to that for the gate insulating film **112** or the gate insulating film **132**.

[0348] The oxide semiconductor film **506** may be formed using a material similar to that for the oxide semiconductor film **106**.

[0349] The pair of electrodes **516** may be formed using a material similar to that for the pair of electrodes **216**.

[0350] The interlayer insulating film **518** may be formed of a single layer or a stacked layer using one or more of the following materials: aluminum oxide, aluminum nitride, magnesium oxide, silicon oxide, silicon oxynitride, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide. In addition to the single layer or the stacked layer, silicon nitride oxide or silicon nitride may be stacked.

[0351] It is preferable that the interlayer insulating film **518** have low relative permittivity and a sufficient thickness. For example, a silicon oxide film having a relative permittivity of approximately 3.8 and a thickness greater than or equal to 200 nm and less than or equal to 1000 nm may be provided. A top surface of the interlayer insulating film **518** has a little fixed charge because of the influence of atmospheric components and the like, which might cause the shift of the threshold voltage of the transistor. Therefore, it is preferable that the interlayer insulating film **518** have relative permittivity and a thickness such that the influence of the charge at the top surface is sufficiently reduced. For the same reason, a resin film of a polyimide resin, an acrylic resin, an epoxy resin, a silicone resin, or the like may be formed over the interlayer insulating film **518** in order to reduce the influence of the charge at the top surface of the interlayer insulating film **518**.

[0352] A method of manufacturing the transistor in FIGS. **15**A to **15**C will be described below with reference to FIGS. **16**A to **16**C. Here, only cross-sectional views corresponding to FIG. **15**B are illustrated for simplicity.

[0353] First, the substrate **500** is prepared.

[0354] Next, the base insulating film **502** is formed over the substrate **500**. The base insulating film **502** may be formed using any of the above materials for the base insulating film **502** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0355] Next, the gate electrode **504** is formed. The gate electrode **504** may be formed using a material and a method similar to those for the gate electrode **104**.

[0356] Next, the gate insulating film **512** is formed (see FIG. **16**A). The gate insulating film **512** may be formed using a material and a method similar to those for the gate insulating film **112** or the gate insulating film **132**.

[0357] Next, the oxide semiconductor film **506** is formed (see FIG. **16**B). The oxide semiconductor film **506** may be formed using a material and a method similar to those for the oxide semiconductor film **107**.

[0358] Next, a conductive film to be the pair of electrodes **516** is formed. The conductive film to be the pair of electrodes **516** may be formed using any of the above materials for the pair of electrodes **516** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0359] Then, the conductive film to be the pair of electrodes **516** is processed to form the pair of electrodes **516**. For part of the processing of the conductive film to be the pair of electrodes **516**, an electron beam drawing equipment (also referred to as electron beam (EB) lithography system) is preferably used. An EB lithography system enables extremely minute processing, and thus is suitable for manufacturing a miniaturized transistor.

[0360] Next, the interlayer insulating film **518** is formed (see FIG. **16**C). The interlayer insulating film **518** may be formed using any of the above materials for the interlayer insulating film **518** by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method.

[0361] In this manner, the transistor in FIGS. **15**A to **15**C can be manufactured.

[0362] In the transistor in FIGS. **15**A to **15**C, the oxide semiconductor film **506** has few oxygen vacancies and an influence of a parasitic channel is small; thus, the transistor can have switching characteristics even when miniaturized.

Further, since the pair of electrodes **516** is provided, the transistor can have excellent on-state characteristics even when miniaturized.

[0363] According to this embodiment, a transistor that can have switching characteristics and excellent on-state characteristics even when miniaturized can be provided. Further, a highly integrated semiconductor device including the transistor can be provided.

[0364] This embodiment can be implemented in appropriate combination with any of the other embodiments.

Embodiment 6

[0365] In this embodiment, an example of manufacturing a semiconductor memory device using any of the transistors described in Embodiments 1 to 5 will be described.

[0366] Typical examples of a volatile semiconductor memory device include a dynamic random access memory (DRAM) which stores data by selecting a transistor included in a memory element and accumulating an electric charge in a capacitor, and a static random access memory (SRAM) which holds stored data using a circuit such as a flip-flop.

[0367] Typical examples of a nonvolatile semiconductor memory device include a flash memory which has a floating gate between a gate and a channel region of a transistor and stores data by holding an electric charge in the floating gate.

[0368] Any of the transistors described in Embodiments 1 to 5 can be applied to some of transistors included in the above-described semiconductor memory device.

[0369] First, a specific example of a memory cell included in a semiconductor memory device to which any of the transistors described in Embodiments 1 to 5 is applied will be described with reference to FIGS. **17**A to **17**C.

[0370] A memory cell includes a bit line BL, a word line WL, a sense amplifier SAmp, a transistor Tr, and a capacitor C (see FIG. **17**A).

[0371] Note that it is known that the voltage held in the capacitor C is gradually decreased with time as shown in FIG. **17**B owing to the off-state current of the transistor Tr. A voltage originally charged from V**0** to V**1** is decreased with time to VA that is a limit for reading out data **1**. This period is called a holding period T_**1**. In the case of a two-level memory cell, refresh operation needs to be performed within the holding period T_**1**.

[0372] Here, when any of the transistors described in Embodiments 1 to 5 is used as the transistor Tr, the holding period T_**1** can be increased because the off-state current of the transistor is extremely small. That is, frequency of the refresh operation can be reduced; thus, power consumption can be reduced. For example, in the case where a memory cell is formed using the transistor Tr having an off-state current of 1×10^{-21} A to 1×10^{-25} A, data can be held for several days to several decades without supply of electric power.

[0373] When any of the transistors described in Embodiments 1 to 5 is used as the transistor Tr, the area of the memory cell can be made smaller because the transistor is miniaturized. Accordingly, the integration degree of the semiconductor memory device can be increased.

[0374] FIG. **17**C illustrates an example of a cross-sectional structure of the memory cell. Note that in FIG. **17**C, the transistor in FIGS. **4**A to **4**C is used as the transistor Tr. Therefore, for components of the transistor Tr which are not described below, the description in Embodiment 1 or the like can be referred to.

[0375] Here, the capacitor C over the base insulating film **102** includes an electrode **116** which is in contact with the region **106***b* of the transistor Tr; an insulating layer which is formed from the same layer and the same material as the gate insulating film **132**; and an electrode (capacitor electrode) which is formed from the same layer and the same material as the gate electrode **104**. Note that the electrode **116** is embedded in the base insulating film **102** in FIG. **17**C; however, the shape of the electrode **116** is not limited thereto. The electrode **116** may have any shape as long as the electrode **116** is provided over the base insulating film **102** and in contact with the region **106***b* of the transistor Tr.

[0376] The electrode **116** may be formed of a single layer or a stacked layer of a simple substance selected from Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W; a nitride containing one or more kinds of the above substances; an oxide containing one or more kinds of the above substances; or an alloy containing one or more kinds of the above substances.

[0377] The word line WL is electrically connected to the gate electrode **104**. The bit line BL is electrically connected to the wiring **136**.

[0378] In the memory cell in FIG. **17**C, the transistor Tr and the capacitor C include the electrodes formed from the same layer and the same material and the insulating films formed from the same layer and the same material; thus, the number of manufacturing steps can be reduced and the productivity can be improved. However, the transistor Tr and the capacitor C do not necessarily include the electrodes formed from the same layer and the same material and the insulating films formed from the same layer and the same material. For example, the area of the memory cell may be made smaller by providing the transistor Tr and the capacitor C so as to overlap with each other.

[0379] As described above, according to one embodiment of the present invention, a semiconductor memory device with high degree of integration and low power consumption can be provided.

[0380] Next, a memory cell in a semiconductor device including any of the transistors in Embodiments 1 to 5, which is a different example from FIGS. **17**A to **17**C, will be described with reference to FIGS. **18**A to **18**C.

[0381] FIG. **18**A is a circuit diagram of a memory cell. The memory cell includes a transistor Tr_**1**, a word line WL_**1** electrically connected to a gate of the transistor Tr_**1**, a source line SL_**1** electrically connected to a source of the transistor Tr_**1**, a transistor Tr_**2**, a source line SL_**2** electrically connected to a source of the transistor Tr_**2**, a drain line DL_**2** electrically connected to a drain of the transistor Tr_**2**, a capacitor C, a capacitor line CL electrically connected to one terminal of the capacitor C, and a node N electrically connected to the other terminal of the capacitor C, a drain of the transistor Tr_**1**, and a gate of the transistor Tr_**2**.

[0382] The semiconductor memory device described in this embodiment utilizes variation in the apparent threshold voltage of the transistor Tr_**2**, which depends on the potential of the node N. For example, FIG. **18**B shows a relation between a voltage V_{CL} of the capacitor line CL and a drain current I_{d}_**2** flowing through the transistor Tr_**2**.

[0383] The potential of the node N can be controlled through the transistor Tr_**1**. For example, the potential of the source line SL_**1** is set to VDD. In this case, when the potential of the word line WL_**1** is set to be higher than or equal to a potential obtained by adding VDD to the threshold voltage Vth of the transistor Tr_**1**, the potential of the node N can be

HIGH. Further, when the potential of the word line WL_**1** is set to be lower than or equal to the threshold voltage Vth of the transistor Tr_**1**, the potential of the node N can be LOW.

[0384] Thus, either a V_{CL}-$I_{d\_}$**2** curve (N=LOW) or a V_{CL}-$I_{d\_}$**2** curve (N=HIGH) can be obtained. That is, when N=LOW, $I_{d\_}$**2** is small at a V_{CL} of 0V; accordingly, data **0** is stored. Further, when N=HIGH, $I_{d\_}$**2** is large at a V_{CL} of 0V; accordingly, data **1** is stored. In such a manner, data can be stored.

[0385] Here, when any of the transistors described in Embodiments 1 to 5 is used as the transistor Tr_**1**, the off-state current of the transistor can be significantly reduced; therefore, unintentional leakage of an electric charge accumulated in the node N by flowing between the source and the drain of the transistor Tr_**1** can be suppressed. As a result, data can be held for a long time. Since high voltage is not needed in data writing, power consumption can be made small and operation speed can be high as compared to a flash memory or the like.

[0386] When any of the transistors described in Embodiments 1 to 5 is used as the transistor Tr_**1**, the area of the memory cell can be made smaller because the transistor is miniaturized. Accordingly, the integration degree of the semiconductor memory device can be increased.

[0387] FIG. **18**C illustrates an example of a cross-sectional structure of the memory cell. Note that in FIG. **18**C, the transistor in FIGS. **4**A to **4**C is used as the transistor Tr_**1**. Therefore, for components of the transistor Tr_**1** which are not described below, the description in Embodiment 1 or the like can be referred to.

[0388] In this embodiment, the case where a transistor including silicon is used as the transistor Tr_**2** will be described. Note that any of the transistors described in Embodiments 1 to 5 may be used as the transistor Tr_**2**.

[0389] The transistor including silicon has an advantage that on-state characteristics can be easily improved in comparison with the transistors described in Embodiments 1 to 5. Therefore, it can be said that the transistor including silicon is suitable for not the transistor Tr_**1** for which small off-state current is required but the transistor Tr_**2** for which excellent on-state characteristics are required.

[0390] Here, the transistor Tr_**2** includes a base insulating film **152** provided over a substrate **150**; a silicon film **156** which is provided over the base insulating film **152** and includes a region **156***a* and regions **156***b*; a gate insulating film **162** provided over the silicon film **156**; a gate electrode **154** which is provided over the gate insulating film **162** so as to overlap with the silicon film **156**; and a sidewall insulating films **160** in contact with sidewalls of the gate insulating film **162** and the gate electrode **154**.

[0391] Note that an interlayer insulating film **158** is provided over the transistor Tr_**2**, and a hydrogen-containing layer **168** is provided over the interlayer insulating film **158**.

[0392] The substrate **150** may be formed using a material similar to that for the substrate **100**.

[0393] The base insulating film **152** may be formed using a material similar to that for the base insulating film **102**.

[0394] A silicon film such as a single crystal silicon film or a polycrystalline silicon film may be used as the silicon film **156**.

[0395] The region **156***a* functions as a channel region. The regions **156***b* function as a source region and a drain region.

[0396] Note that the silicon film is used for the channel region and the source and drain regions in this embodiment; however, in the case where the substrate **150** is a semiconductor substrate such as a silicon wafer, the channel region and the source and drain regions may be provided in the semiconductor substrate.

[0397] The gate insulating film **162** may be formed using a material similar to that for the gate insulating film **112**.

[0398] The gate electrode **154** may be formed using a material similar to that for the gate electrode **104**.

[0399] The sidewall insulating films **160** may be formed using a material similar to that for the sidewall insulating films **310**.

[0400] The interlayer insulating film **158** may be formed using a material similar to that for the interlayer insulating film **118**. Note that a resin film of a polyimide resin, an acrylic resin, an epoxy resin, a silicone resin, or the like may be formed over the interlayer insulating film **158**.

[0401] The hydrogen-containing layer **168** is formed using an insulating film in which the hydrogen concentration measured by secondary ion mass spectrometry (SIMS) is 1×10^{21} atoms/cm^3 or higher.

[0402] The hydrogen-containing layer **168** may be formed using, for example, a silicon nitride oxide film or a silicon nitride film.

[0403] Since the transistor Tr_**2** is a transistor including silicon, the electric characteristics of the transistor Tr_**2** can be improved by terminating dangling bonds on a surface of the silicon film **156** with hydrogen. For that reason, hydrogen is preferably supplied from the hydrogen-containing layer **168**. Note that this embodiment is not limited to the structure where the hydrogen-containing layer **168** is provided. For example, hydrogen may be supplied to the transistor Tr_**2** without using the hydrogen-containing layer **168**.

[0404] Although not illustrated, a layer having low hydrogen permeability may be provided between the hydrogen-containing layer **168** and the base insulating film **102**. The transistor Tr_**1** is a transistor including an oxide semiconductor film. Since hydrogen serves as a source of carriers in the oxide semiconductor film, hydrogen is preferably prevented from entering the oxide semiconductor film as much as possible. For that reason, in the case where the hydrogen-containing layer **168** is provided, diffusion of hydrogen to the transistor Tr_**1** is preferably prevented by the layer having low hydrogen permeability.

[0405] Note that the layer having low hydrogen permeability is formed using, for example, an insulating film through which hydrogen does not pass even when heat treatment is performed at 350° C. for one hour.

[0406] The capacitor C over the base insulating film **102** includes an electrode **166** which is in contact with the region **106***b* of the transistor Tr_**1**; an insulating layer which is formed from the same layer and the same material as the gate insulating film **132**; and an electrode (capacitor electrode) which is formed from the same layer and the same material as the gate electrode **104**. The electrode **166** is in contact with the gate electrode **154** of the transistor Tr_**2** through an opening provided in the base insulating film **102**, the hydrogen-containing layer **168**, and the interlayer insulating film **158**. Note that the electrode **166** is embedded in the base insulating film **102** in FIG. **18**C; however, the shape of the electrode **166** is not limited thereto. The electrode **166** may have any shape as long as the electrode **166** is provided over the base insulating film **102** and in contact with the region **106***b* of the transistor Tr_**1** and the gate electrode **154** of the transistor Tr_**2**.

[0407] The electrode **166** may be formed of a single layer or a stacked layer of a simple substance selected from Al, Ti, Cr,

Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W; a nitride containing one or more kinds of the above substances; an oxide containing one or more kinds of the above substances; or an alloy containing one or more kinds of the above substances.

[0408] The word line WL_**1** is electrically connected to the gate electrode **104**. The source line SL_**1** is electrically connected to the wiring **136**. The capacitor line CL is electrically connected to the capacitor electrode.

[0409] In the memory cell in FIG. **18**C, the transistor Tr_**1** and the capacitor C include the electrodes formed from the same layer and the same material and the insulating films formed from the same layer and the same material; thus, the number of manufacturing steps can be reduced and the productivity can be improved. However, the transistor Tr_**1** and the capacitor C do not necessarily include the electrodes formed from the same layer and the same material and the insulating films formed from the same layer and the same material. For example, the area of the memory cell may be made smaller by providing the transistor Tr_**1** and the capacitor C so as to overlap with each other.

[0410] As described above, according to one embodiment of the present invention, a semiconductor memory device with high degree of integration and low power consumption can be provided.

[0411] This embodiment can be implemented in appropriate combination with any of the other embodiments.

Embodiment 7

[0412] A central processing unit (CPU) can be formed using any of the transistors described in Embodiments 1 to 5 or the semiconductor memory device described in Embodiment 6 for at least part of the CPU.

[0413] FIG. **19**A is a block diagram illustrating a specific structure of the CPU. The CPU illustrated in FIG. **19**A includes an arithmetic logic unit (ALU) **1191**, an ALU controller **1192**, an instruction decoder **1193**, an interrupt controller **1194**, a timing controller **1195**, a register **1196**, a register controller **1197**, a bus interface (Bus I/F) **1198**, a rewritable ROM **1199**, and a ROM interface (ROM I/F) **1189** over a substrate **1190**. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate **1190**. The ROM **1199** and the ROM interface **1189** may be provided over a separate chip. Obviously, the CPU shown in FIG. **19**A is just an example in which the configuration has been simplified, and an actual CPU may have various configurations depending on the application.

[0414] An instruction that is input to the CPU through the bus interface **1198** is input to the instruction decoder **1193** and decoded therein, and then, input to the ALU controller **1192**, the interrupt controller **1194**, the register controller **1197**, and the timing controller **1195**.

[0415] The ALU controller **1192**, the interrupt controller **1194**, the register controller **1197**, and the timing controller **1195** conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller **1192** generates signals for controlling the operation of the ALU **1191**. While the CPU is executing a program, the interrupt controller **1194** determines an interrupt request from an external input/output device or a peripheral circuit on the basis of its priority or a mask state, and processes the request. The register controller **1197** generates an address of the register **1196**, and reads/writes data from/to the register **1196** in accordance with the state of the CPU.

[0416] The timing controller **1195** generates signals for controlling operation timings of the ALU **1191**, the ALU controller **1192**, the instruction decoder **1193**, the interrupt controller **1194**, and the register controller **1197**. For example, the timing controller **1195** includes an internal clock generator for generating an internal clock signal CLK**2** based on a reference clock signal CLK**1**, and supplies the clock signal CLK**2** to the above circuits.

[0417] In the CPU illustrated in FIG. **19**A, a memory element is provided in the register **1196**. As the memory element in the register **1196**, for example, the semiconductor memory device described in Embodiment 6 can be used.

[0418] In the CPU illustrated in FIG. **19**A, the register controller **1197** selects operation of retaining data in the register **1196** in accordance with an instruction from the ALU **1191**. That is, the register controller **1197** selects whether data is retained by a flip-flop or a capacitor in the memory element included in the register **1196**. When data is retained by the flip-flop, a power supply voltage is supplied to the memory element in the register **1196**. When data is retained by the capacitor, the data in the capacitor is rewritten, and supply of the power supply voltage to the memory element in the register **1196** can be stopped.

[0419] A switching element provided between a memory element group and a node to which a power supply potential VDD or a power supply potential VSS is supplied, as illustrated in FIG. **19**B or FIG. **19**C, allows the power supply voltage to be stopped. Circuits illustrated in FIGS. **19**B and **19**C will be described below.

[0420] FIGS. **19**B and **19**C each illustrate an example of a structure including any of the transistors described in Embodiments 1 to 5 as a switching element for controlling supply of a power supply potential to a memory element.

[0421] The memory device illustrated in FIG. **19**B includes a switching element **1141** and a memory element group **1143** including a plurality of memory elements **1142**. Specifically, as each of the memory elements **1142**, the semiconductor memory device described in Embodiment 6 can be used. Each of the memory elements **1142** included in the memory element group **1143** is supplied with the high-level power supply potential VDD through the switching element **1141**. Further, each of the memory elements **1142** included in the memory element group **1143** is supplied with a potential of a signal IN and a potential of the low-level power supply potential VSS.

[0422] In FIG. **19**B, a transistor with an extremely small off-state current is used as the switching element **1141**, and the switching of the transistor is controlled by a signal SigA supplied to a gate thereof.

[0423] Note that FIG. **19**B illustrates the structure in which the switching element **1141** includes only one transistor; however, without limitation thereon, the switching element **1141** may include a plurality of transistors. In the case where the switching element **1141** includes a plurality of transistors which serves as switching elements, the plurality of transistors may be connected to each other in parallel, in series, or in combination of parallel connection and series connection.

[0424] In FIG. **19**C, an example of a memory device in which each of the memory elements **1142** included in the memory element group **1143** is supplied with the low-level power supply potential VSS through the switching element **1141** is illustrated. The supply of the low-level power supply potential VSS to each of the memory elements **1142** included in the memory element group **1143** can be controlled by the switching element **1141**.

[0425] When a switching element is provided between a memory element group and a node to which the power supply potential VDD or the power supply potential VSS is supplied, data can be retained even in the case where an operation of a CPU is temporarily stopped and the supply of the power supply voltage is stopped; accordingly, power consumption can be reduced. For example, while a user of a personal computer does not input data to an input device such as a keyboard, the operation of the CPU can be stopped, so that the power consumption can be reduced.

[0426] Although the CPU is given as an example, the transistor and the semiconductor memory device can also be applied to an LSI such as a digital signal processor (DSP), a custom LSI, or a field programmable gate array (FPGA).

[0427] This embodiment can be implemented in appropriate combination with any of the other embodiments.

Embodiment 8

[0428] In this embodiment, examples of an electronic device to which any of Embodiments 1 to 7 is applied will be described.

[0429] FIG. **20**A illustrates a portable information terminal. The portable information terminal illustrated in FIG. **20**A includes a housing **9300**, a button **9301**, a microphone **9302**, a display portion **9303**, a speaker **9304**, and a camera **9305**, and has a function as a mobile phone. One embodiment of the present invention can be applied to an arithmetic unit, a wireless circuit, or a memory circuit in a main body.

[0430] FIG. **20**B illustrates a display, which includes a housing **9310** and a display portion **9311**. One embodiment of the present invention can be applied to an arithmetic unit, a wireless circuit, or a memory circuit in a main body.

[0431] FIG. **20**C illustrates a digital still camera. The digital still camera illustrated in FIG. **20**C includes a housing **9320**, a button **9321**, a microphone **9322**, and a display portion **9323**. One embodiment of the present invention can be applied to an arithmetic unit, a wireless circuit, or a memory circuit in a main body.

[0432] FIG. **20**D illustrates a double-foldable portable information terminal. The double-foldable portable information terminal illustrated in FIG. **20**D includes a housing **9630**, a display portion **9631***a*, a display portion **9631***b*, a hinge **9633**, and an operation switch **9638**. One embodiment of the present invention can be applied to an arithmetic unit, a wireless circuit, or a memory circuit in a main body.

[0433] Part or the whole of the display portion **9631***a* and/or the display portion **9631***b* can function as a touch panel. By touching an operation key displayed on the touch panel, a user can input data, for example.

[0434] By using a semiconductor device according to one embodiment of the present invention, the performance of an electronic device can be improved and the power consumption of the electronic device can be reduced.

[0435] This embodiment can be implemented in appropriate combination with any of the other embodiments.

[0436] This application is based on Japanese Patent Application serial no. 2012-009722 filed with Japan Patent Office on Jan. 20, 2012, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. A semiconductor device comprising:
an oxide semiconductor film including a channel region;
a gate electrode overlapping with the oxide semiconductor film; and
a gate insulating film between the gate electrode and the oxide semiconductor film,
wherein a channel length is greater than or equal to 5 nm and less than 60 nm, and a channel width is greater than or equal to 5 nm and less than 200 nm.

2. The semiconductor device according to claim **1**, further comprising an interlayer insulating film having low oxygen permeability over the oxide semiconductor film and the gate electrode.

3. The semiconductor device according to claim **1**,
wherein the gate insulating film is in contact with at least part of a side surface of the oxide semiconductor film.

4. The semiconductor device according to claim **1**,
wherein the gate insulating film includes at least a first layer and a second layer, and
wherein the second layer has lower oxygen permeability than the first layer.

5. The semiconductor device according to claim **4**,
wherein the second layer is an aluminum oxide film.

6. The semiconductor device according to claim **4**,
wherein the first layer contains excess oxygen, and is in contact with the oxide semiconductor film.

7. The semiconductor device according to claim **1**,
wherein the channel width is 0.5 to 10 times as large as the channel length.

8. The semiconductor device according to claim **1**,
wherein the oxide semiconductor film is a CAAC-OS film.

9. The semiconductor device according to claim **1**,
wherein the oxide semiconductor film contains at least In.

10. The semiconductor device according to claim **1**,
wherein the oxide semiconductor film contains at least In, Ga, and Zn.

11. The semiconductor device according to claim **1**, further comprising a base insulating film, wherein the base insulating film, the oxide semiconductor film, the gate insulating film, and the gate electrode are stacked in this order.

12. The semiconductor device according to claim **11**, wherein the base insulating film contains excess oxygen.

13. A semiconductor device comprising:
a first transistor comprising:
an oxide semiconductor film in contact with a pair of electrodes;
a first gate electrode overlapping with the oxide semiconductor film; and
a gate insulating film between the first gate electrode and the oxide semiconductor film;
a second transistor comprising a second gate electrode; and
a capacitor comprising:
one of the pair of electrodes; and
a capacitor electrode overlapping with the one of the pair of electrodes,
wherein the second gate electrode and the one of the pair of electrodes are electrically connected to each other, and
wherein a channel length of the first transistor is greater than or equal to 5 nm and less than 60 nm, and a channel width of the first transistor is greater than or equal to 5 nm and less than 200 nm.

14. The semiconductor device according to claim **13**,
wherein the gate insulating film is in contact with at least part of a side surface of the oxide semiconductor film.

15. The semiconductor device according to claim **13**, further comprising a barrier film including a layer having low oxygen permeability over the oxide semiconductor film and the first gate electrode.

16. The semiconductor device according to claim **13**,
wherein the gate insulating film includes at least a first layer and a second layer, and
wherein the first layer has lower oxygen permeability than the second layer.

17. The semiconductor device according to claim **16**,
wherein the second layer is an aluminum oxide film.

18. The semiconductor device according to claim **16**,
wherein the first layer contains excess oxygen, and is in contact with the oxide semiconductor film.

19. The semiconductor device according to claim **13**,
wherein the second transistor includes a channel region containing silicon.

20. The semiconductor device according to claim **13**,
wherein the first transistor and the second transistor are provided in different layers,
wherein a hydrogen-containing layer and a layer containing excess oxygen are provided between the first transistor and the second transistor,
wherein the hydrogen-containing layer is closer to the second transistor than the layer containing excess oxygen, and
wherein a hydrogen concentration in the hydrogen-containing layer measured by secondary ion mass spectrometry is 1×10^{21} atoms/cm^3 or more.

21. The semiconductor device according to claim **20**,
wherein the hydrogen-containing layer is a silicon nitride oxide film or a silicon nitride film.

22. The semiconductor device according to claim **20**, further comprising a layer having low hydrogen permeability between the hydrogen-containing layer and the layer containing excess oxygen.

23. The semiconductor device according to claim **13**,
wherein the channel width is 0.5 to 10 times as large as the channel length.

24. The semiconductor device according to claim **13**,
wherein the oxide semiconductor film is a CAAC-OS film.

25. The semiconductor device according to claim **13**,
wherein the oxide semiconductor film contains at least In.

26. The semiconductor device according to claim **13**,
wherein the oxide semiconductor film contains at least In, Ga, and Zn.

27. The semiconductor device according to claim **13**,
wherein an off-state current of the first transistor is lower than 1×10^{-21} A per micrometer of the channel width at room temperature.

28. The semiconductor device according to claim **13**,
wherein the oxide semiconductor film, the gate insulating film, and the second gate electrode are stacked in this order.

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