United States Patent

[11] **3,611,348**

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[21] Appl. No. **847,612**
[22] Filed **Aug. 5, 1969**
[45] Patented **Oct. 5, 1971**
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[54] **CHARACTER DISPLAY SYSTEM**
11 Claims, 2 Drawing Figs.

[52] **U.S. Cl.** ..... **340/324 A,** 340/154, 340/339
[51] **Int. Cl.** **G06f 3/14**
[50] **Field of Search** ..... 340/324.1, 324 A, 154, 339, 324 R

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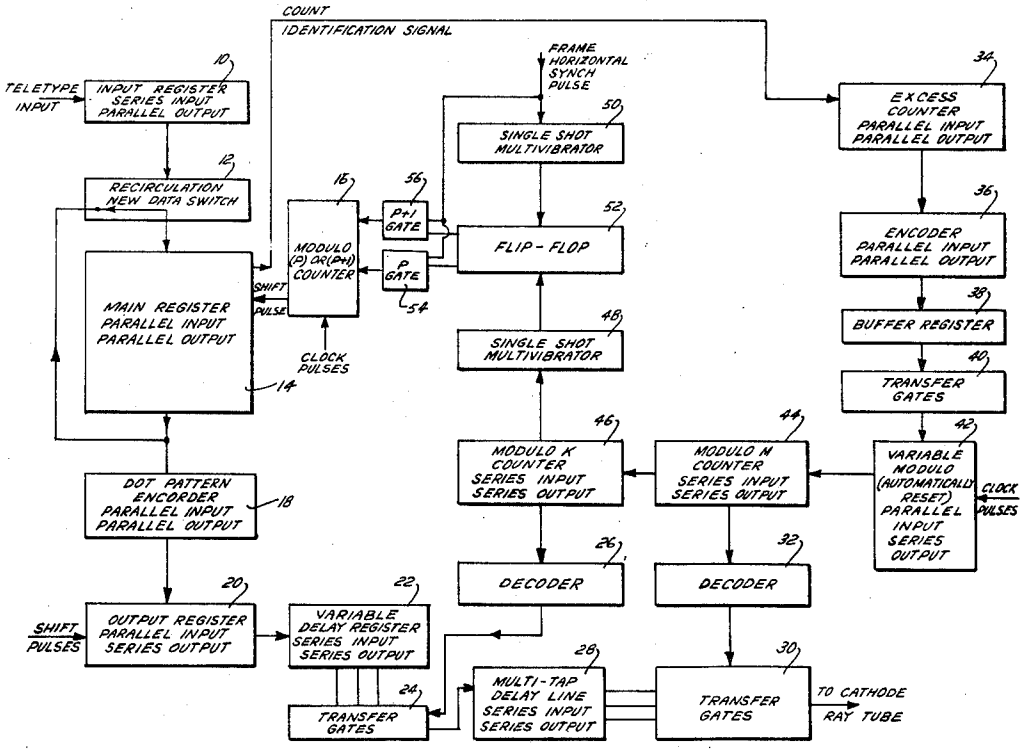
ABSTRACT: A system responsive to incoming electrical digital signals representing alpha-numeric characters and supplied in series character format at a varying rate. The system is adapted to display these characters in the form of dot matrices and to move such displayed characters in a video line across the face of a cathode-ray tube. The rate of character movement is varied in accordance with changes in the rate at which the signals are supplied to the system to eliminate visually apparent changes in the speed of movement of the displayed characters.



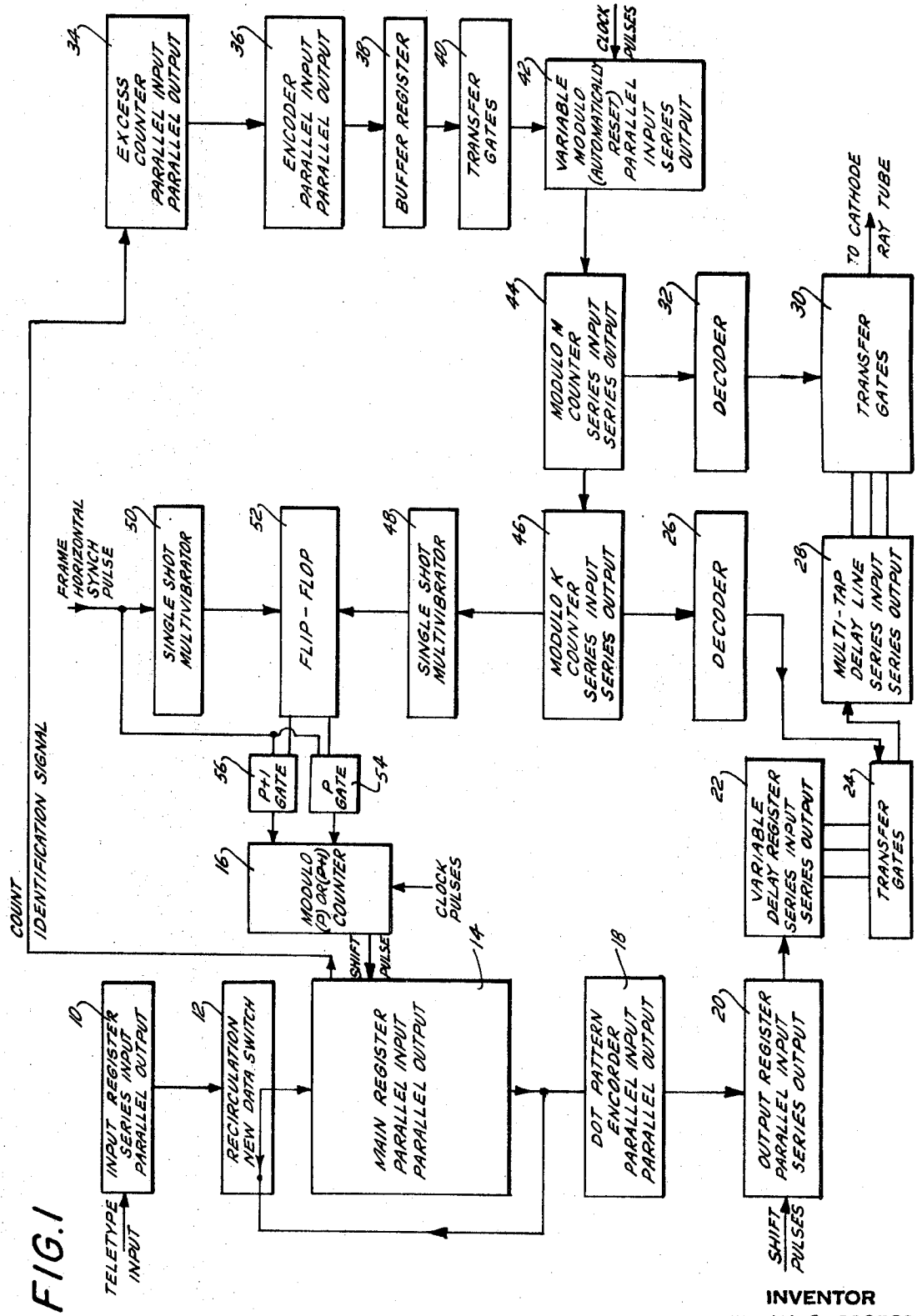


FIG. 1

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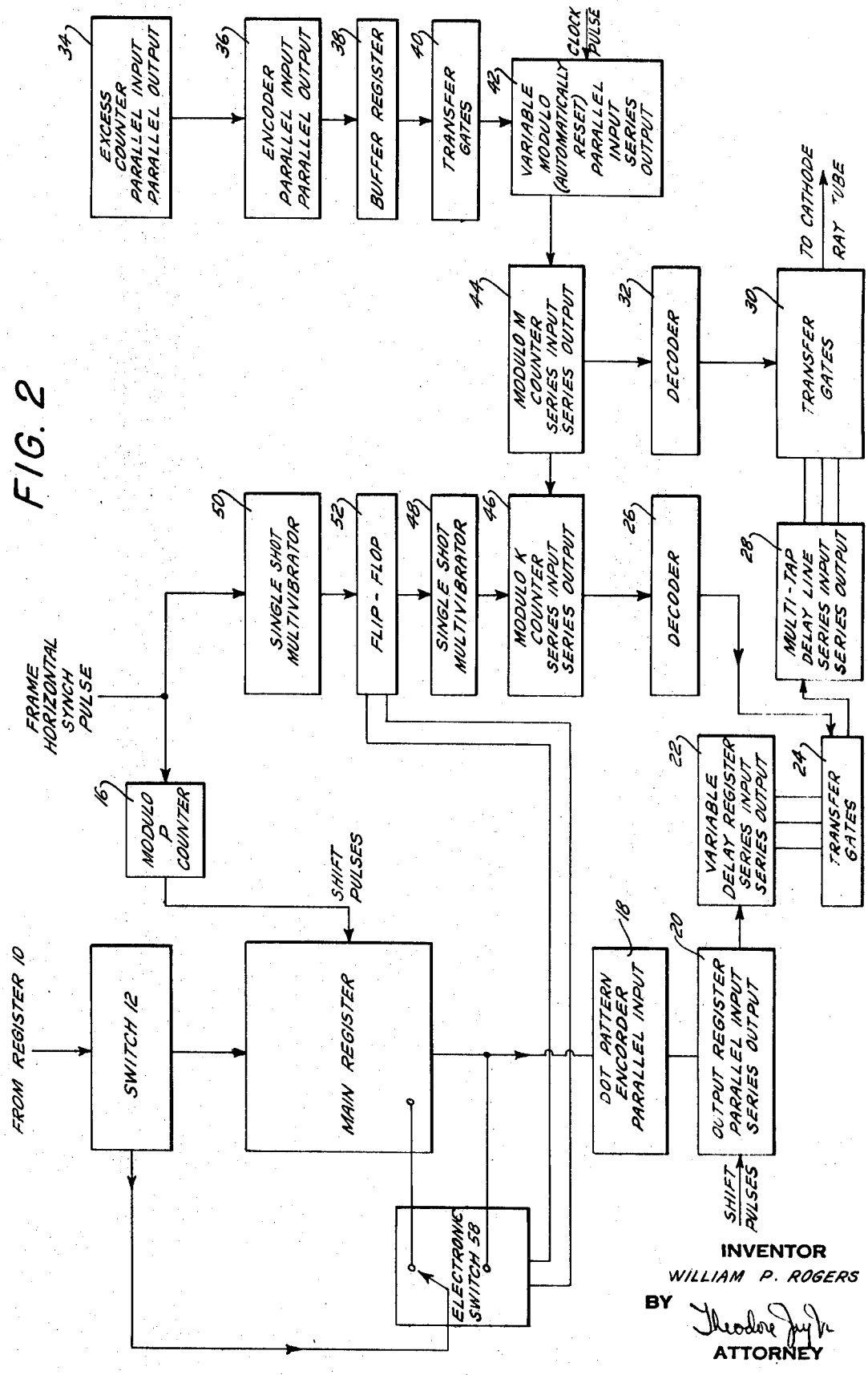

FIG. 2

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CHARACTER DISPLAY SYSTEM

BACKGROUND OF THE INVENTION

The securities and exchange markets utilize a variety of different systems for receiving transaction information from ticker lines in the form of electrical equivalents of alpha-numeric characters and reproducing these characters as a moving or apparently moving display. The information on the ticker input lines characteristically exhibit sudden starts and stops. Viewers of the moving display find such starts and stops to be uncomfortable to the eye.

My invention is adapted to receive such transaction information and to reproduce same as a moving display in a cathode-ray tube. In my invention, the rate of character movement along a video line is varied in accordance with changes in the rate of arrival of transaction information in such manner that the displayed characters, which take the form of dot matrices, can be advanced less than one integral dot per display frame. As a result visually apparent rapid changes in the speed of the display cannot occur and viewer visual discomfort is eliminated.

SUMMARY OF THE INVENTION

In accordance with the principles of my invention, I provide a system responsive to incoming digital signals representing alpha-numeric characters and supplied in series character format at a varying rate. The system is adapted to display said characters in the form of dot matrices and move same serially in a video line across the face of a cathode-ray tube. The rate of character movement is varied in accordance with changes in the rate at which said digital signals are supplied to the system to eliminate visually apparent rapid changes in speed of movement of the displayed characters.

To this end, I provide a register having a predetermined number of storage stages and adapted to receive and store said characters prior to display in series character format, wherein the stored characters are automatically shifted from stage to stage between an input and an output.

First means is coupled to the output of said register and is responsive to each character appearing successively thereat to process same and thereafter to deliver same to the cathode-ray tube for display.

Second means is coupled to said register and is rendered responsive during each period between the end of a display of a video line and the beginning of the display of the next video line to provide a count signal in the form of a pulse train containing a variable number of pulses, the number of pulses varying monotonically with the number of full undisplayed stages in the register during this period.

Third means is responsive to each pulse in each train to produce an output signal upon receipt of each Nth pulse where N is a selected integer.

Fourth means coupled to the register is responsive to the output signals. During each period between adjacent video line displays, when the output signals are absent, the fourth means repositions the characters stored in the register in such manner that each character to be displayed in the next video line is maintained in the same relative position as in the immediately preceding video line. When output signals are present during each such period, the fourth means repositions the characters stored in the register in such manner that each character to be displayed in the next video line is advanced one character position relative to its position in the preceding video line.

The system thus far described changes the relative character position in increments of entire character positions. Typically, each character position represents K integral dot positions where K is an integer representing the sum of the number of dot positions required for a character length plus the number of dot positions in the space between adjacent characters.

In order to change relative character positions in integral number of dots less than K and thus provide more gradual changes in the speed of display, the first means can include first additional means responsive to said pulse train to advance the characters in the next video line by an integral number of dot positions ranging from zero to K, depending upon the number of pulses in the train.

In order to change relative character positions in fractions of an integral dot position and thus provide even more gradual changes in the speed of the display, the first means can include second additional means responsive to the pulse train to advance the characters in the next video line by a fraction of an integral dot position, the fraction ranging from zero to one, depending upon the number of pulses in the train.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a block diagram of one embodiment of my invention; and

FIG. 2 is a block diagram of a second embodiment of my invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A cathode-ray tube (not shown) is actuated by conventional horizontal and vertical drive circuitry to produce a succession of display fields. Typically, the field can consist of one horizontal video line of a plurality of alpha-numeric characters disposed side by side and representing current and changing stock market transactions. Each characters is defined by either a five by seven or five by 10 dot matrix. As a result, as many as 10 scan lines are required for complete display of a characters, each line providing a different horizontal slice of the same character. Consequently each video line is composed of 10 adjacent scan lines.

Since the display fields are to represent a moving ticker-type display, each character is to be shifted incrementally in position on one video line as compared to its position or the previous video line. To avoid visually apparent rapid changes in character position, the speed of the incremental shifts is varied in accordance with the changes in the rate of arrival of transaction information. The variation in speed, as described in more detail below, can be zero or a change of a fraction of an integral dot position, or an integral number of dot positions or an entire character position.

Referring now to FIG. 1, transaction information as supplied for example by teletype arrives in series bit, series character format at an input register **10**. Register **10** stores each bit until a complete character is stored and then releases each stored character to the new data input of a recirculation—new data switch **12** in parallel bit, series character format. As long as switch **12** is in the position shown, each such character is loaded into a main register **14** wherein each character in parallel bit format is shifted from stage to stage, under the control of shift pulses, from the input to the output of the register. When switch **12** is in the reverse position, new information cannot be entered into the register **14**, but the output of register **14** is connected to its input whereby the stored information is recirculated. The timing of transfer of information from stage to stage is such that either the characters stored therein for display of a video line will be maintained in the same relative position as in the preceding line or will be advanced one character position relative to that of the preceding line, depending upon the numbers of shift pulses supplied during selected intervals to the individual register stages from a modulo P or (P+1) counter **16**.

Information appearing in parallel bit, series character format at the output of register **14** is transferred to the input of dot pattern encoder **18**. Encoder **18** is actuated by suitable timing pulses and has a built in code whereby the encoder responds to any character supplied to it to derive therefrom that portion of the corresponding dot matrix of said character required by the particular one of the ten scan lines which is then in use.

The output of the encoder, which represents a selected horizontal slice of the dot matrix for the character encoded is supplied to the input of an output register **20**. This register **20** converts the slice of the dot matrix supplied to it in parallel dot format into serial dot format, this serial output being supplied to the input of a variable delay register **22**. Each stage in register is not only connected to the immediately following stage but is also connected to the input of a corresponding gate in a first matrix of transfer gates **24**. Depending upon whichever gate is opened, the information in any of the stages of register **22** can be transferred directly to the output of gates **24**. Thus the relative transfer timing can be varied in accordance with the gate selection signals supplied to gates **24** from decoder **26**. Variable delay register **22** has K different stages (where K is an integer) and is adapted to advance the relative character positions in a video line, as compared to the positions in the previous video line, by an integral number of dot positions ranging from zero to K, depending upon the signals yielded by decoder **26**.

The output of gates **24** is supplied to the input of a multitap delay line having M different equidistantly spaced output taps, where M is an integer herein chosen to have a value of twelve. All output taps are connected to the inputs of corresponding gates in a second matrix of transfer gates **30**. The output of the second matrix is supplied to the input of cathode-ray tube **10** to produce the display. Depending upon which particular gate is opened, the information at any of the taps of line **28** can be transferred directly to the cathode-ray tube. Hence the relative transfer timing can be varied in accordance with gate selection signals supplied to gates **30** from decoder **32**. Delay line **28** is adapted to advance the relative character positions in a video line, as compared to the positions in the previous video line, by a fraction of an integral dot position ranging from zero to one in increments of 1/M (from one-twelfth to one) depending upon the signals yielded by decoder **32**.

In order for register **14** to be capable of changing relative character positions along a video line to speed up or slow down the display in accordance with changes in the rate of arrival of transaction information, the number of stages in the register must be greater than the number of character positions along a line. Some stages will necessarily contain no information and be empty while other stages are full. Speed control is obtained by varying character positions in accordance with the number of full stages. More particularly, for each character stored but not yet displayed, there is a corresponding velocity of motion of the displayed data. This velocity is converted into dots plus fractions of dots of advance of characters per line. To accomplish this conversion, during each period between the end of the display of one video line and the beginning of the display of the next video line, a pulse train is produced. This train contains a variable number of pulses, this number varying monotonically with the number of full undisplayed stages in the register during this period. To this end, each stage in register **14** can be provided with separate means (such as a flip-flop) to indicate whether the stage is full or empty. All of such means are connected in parallel to an excess counter **34** which produces a continuous count of the number of full undisplayed stages. This count appears at the parallel output of counter **34** and is supplied to encoder **36**. Encoder **36** produces a coded equivalent of this count which is held in a buffer register **38**. The output of register **38** is connected via a third matrix of gates **40** to enable a variable modulo counter **42**. Control pulses supplied to register **38** and gates **40** at different selected instants in each period between the end of a display of one video line and the beginning of a display of the next video line initiate the transfer of this coded equivalent to the counter **42** to preset this counter accordingly. Counter **42** is then automatically decremented to zero, passing one incident clock pulse for each integral decrement whereby the output of counter **42** is desired pulse train.

The number of pulses in the train determines the number of fractions of dots as well as the integral number of dots as well as the integral number of dots by which the characters are to be shifted during the display of the next video line. To this end, the pulse train is supplied to a modulo M counter **44** which is an accumulator and is not automatically reset. When the total number of pulses received after the counter **44** was last recycled through zero corresponds to a fractional shift of one dot or less, decoder **32** converts the output of counter **44** to the signals required to actuate gate matrix **32** as previously described.

When the number of pulses corresponds to a shift or more than one integral dot, counter **44** is recycled through zero and the overflow generates a corresponding number of pulses which are supplied to a modulo K counter **46** which is also an accumulator and is not automatically reset. When the total number of pulses received after counter **46** was last recycled through zero corresponds to a shift of more than one integral dot, decoder **26** converts the output of counter **46** to the signals required to actuate gate matrix **24** as previously described.

During each of the periods between successive video line displays, counter **16** either sends P successive pulses (where P is an integer) to register **14** or sends (P+1) pulses; i.e., counter **66** either is a modulo P or modulo P+1 counter which is automatically reset. When P successive pulses are received, characters to be displayed in the next video line retain, in the register **14**, the same relative positions as in the previous video line. When (P+1) successive pulses are received, characters to be displayed in the next video line are shifted one integral character position as relative to corresponding positions in the previous video line.

When there is no overflow from counter **46**, single shot multivibrator **48** is quiescent, and incident frame horizontal synchronizing pulses (produce at a selected instant during each period between successive video line displays) actuate single shot multivibrator **50** to set flip-flop **52** to open P gate **54** and close (P+1) gate **56**, whereby counter **16** is placed in the modulo P mode and passes P clock pulses. Upon overflow from counter **46**, multivibrator **48** is actuated, resetting flip-flop **52**, closing gate **54** and opening (P+1) gate **56** whereby counter **16** is placed in the modulo (P+1) and passes (P+1) clock pulses.

In the modification of FIG. **2**, the register **14** receives P shift pulses from counter **16** during each of the period between successive line displays at all times. Counter **16** remains in the modulo P mode. However, overflow from counter **46** actuates single shot multivibrator **48** to reset flip-flop **52** and actuate electronic switch **58** to permit interconnection of the stage in register **14** immediately adjacent the output stage to the input. If there is no overflow, multivibrator **48** is quiescent and the synchronizing pulses actuate single shot multivibrator to set flip-flop **52** and actuate switch **58** to to set flip-flop **52** and actuate switch **59** to permit the output of register **14** to be connected to the input in conventional manner. The variable feedback connection between the input and either the output or the stage adjacent the output in register **14** varies the relative timing in this register in the same manner as the variable mode counter technique of FIG. **2** whereby the embodiments of FIGS. **2** and **3** are electronically equivalent in function.

While I have described my invention with particular reference to the drawings, my protection is to be limited only by the terms of the claims which follow.

What is claimed is:

1. A system responsive to incoming digital signals representing alpha-numeric characters and supplied in series character format at a varying rate, said system being adapted to display said characters serially and move same in a video line across the face of a cathode-ray tube, the visual speed of character movement varying in accordance with changes in the incoming signal rate to eliminate visually apparent rapid changes in said speed, said system comprising:

a register having a predetermined number of storage stages and adapted to receive and store said signals prior to display in series character format, the stored characters being automatically shifted from stage to stage between an input and an output;

first means coupled to the output of said register and responsive to each stored character appearing successively thereat to process same and thereafter to deliver same to said tube for display;

second means coupled to said register and rendered responsive during each period between the end of the display of a video line and the beginning of the display of the next video line to provide a count signal in the form of a pulse train containing a variable number of pulses, the number of pulses varying in a predetermined manner with the number of full undisplayed stages in said register during said period;

third means responsive to each pulse in each train to produce an output signal upon receipt of each Nthe pulse, N is a selected integer; and

fourth means coupled to said register and responsive to said output signals, said fourth means, during each said period when the output signals are absent, repositioning the stored characters in the register in a manner at which each character to be displayed in the next video line is maintained in the same relative position as in the immediately preceding video line, said fourth means, during each said period when the output signals are present, repositioning the stored characters in the register in a manner at which each character to be displayed in the next video line is advanced one character position relative to its position in the preceding video line.

2. A system as set forth in claim 1 wherein the characters are displayed in the form of dot matrices, each shift of one character position representing a shift of K integral dot positions where K is a selected integer, said first means including first additional means responsive to said pulse train to advance the characters in the next video line by an integral number of dot positions ranging from zero to K, depending upon the number of pulses in the train.

3. A system as set forth in claim 2 wherein said first means includes second additional means responsive to said pulse train to advance the characters in the next video line by a fraction of an integral dot position, said fraction ranging from zero to one, depending upon the number of pulses in the train.

4. A system as set forth in claim 3 wherein said first means includes a dot encoder coupled to the output of said register and an additional register having an output at which each encoded character appears in series dot format and coupled at its input to said encoder.

5. A system as set forth in claim 4 wherein said first additional means includes a first variable delay device coupled at its input to the output of the additional register.

6. A system as set forth in claim 5 wherein said second additional means includes a second variable delay device coupled at its input to the output of the first device.

7. A system as set forth in claim 6 wherein N is equal to K+1.

8. A system as set forth in claim 7 wherein the fraction of a dot position can attain any one of M different values.

9. A system as set forth in claim 8 wherein said third means includes a variable counter operative to decrease to zero in increments from any number inserted therein.

10. A system as set forth in claim 9 wherein said fourth means includes a first counter coupled at its input to the variable counter output and at its output to said second device and being operative to divide output signals from said variable counter by a factor M.

11. A system as set forth in claim 10 wherein said fourth means includes a second counter coupled at its input to said first counter output and its output to said first means and said first device and being operative to divide a signal at its input by a factor K.