United States Patent [19]

Colin

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[54] **CONTROL CIRCUITRY FOR ELECTRONIC MUSICAL INSTRUMENT**

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[73] Assignee: **ARP Instruments, Inc.,** Newton Upper Falls, Mass.

[22] Filed: **July 11, 1973**

[21] Appl. No.: **378,350**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 220,914, Jan. 26, 1972, abandoned.

[52] **U.S. Cl.** **84/1.01,** 84/1.24

[51] **Int. Cl.** **G10h 1/00**

[58] **Field of Search** ..... 84/1.01, 1.13, 1.24, 1.26, 84/DIG. 7, DIG. 8, DIG. 20, 1.11

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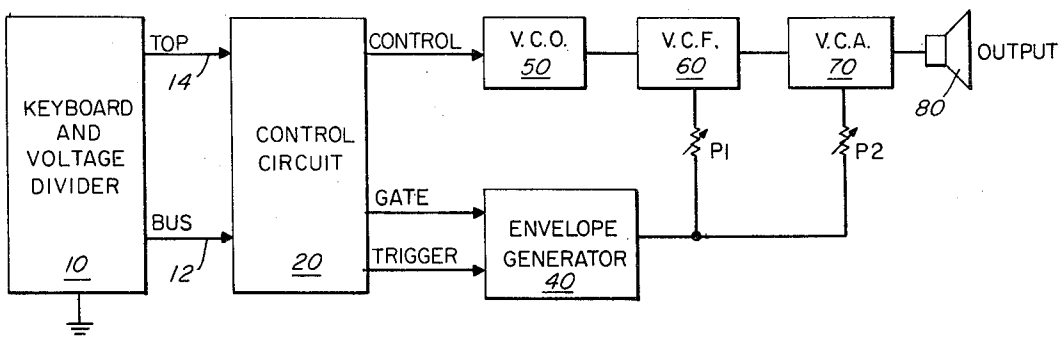
Primary Examiner—Richard B. Wilkinson
Assistant Examiner—U. Weldon

[57] **ABSTRACT**

In an electronic musical instrument of the type including a keyboard and a resistor voltage divider having points there along respectively coupled by way of actuable keys associated with the keyboard to a single output bus, there is provided improved control electronics having output signals that control, for example, an envelope generator and a voltage controlled oscillator. The control electronics includes an oscillator and gate circuit coupled to the bus for providing a gate output signal which is present as long as at least one key is actuated, a sample/hold circuit coupled to the bus for providing a control voltage signal the amplitude of which is a function of the position of the actuated key, and a trigger signal means coupled to the keyboard and responsive to the gate circuit and the actuation of two or more keys for providing a trigger signal of shorter duration than the gate signal and occurring near the commencement of the gate signal.

25 Claims, 8 Drawing Figures



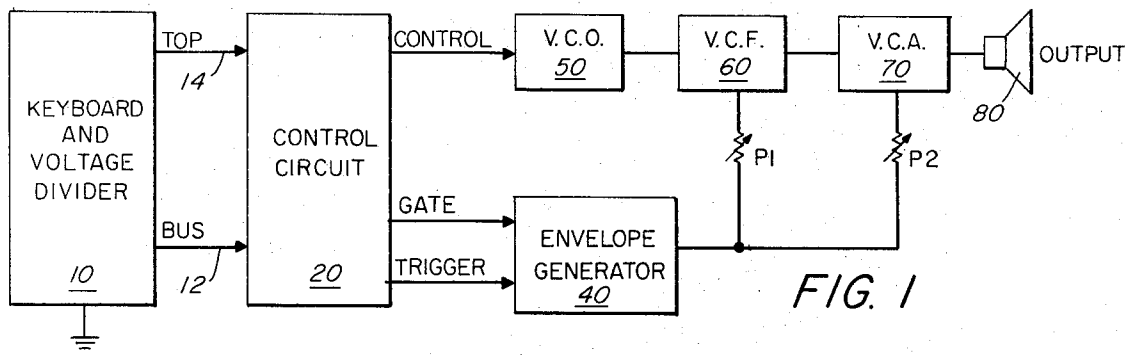


FIG. 1

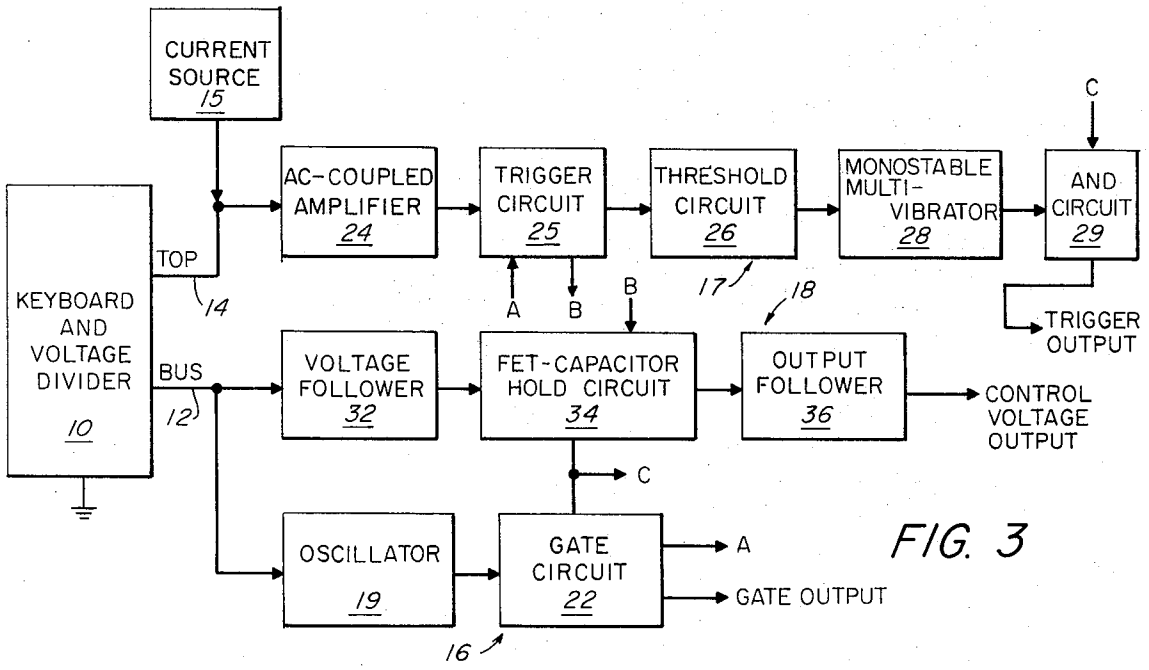


FIG. 3

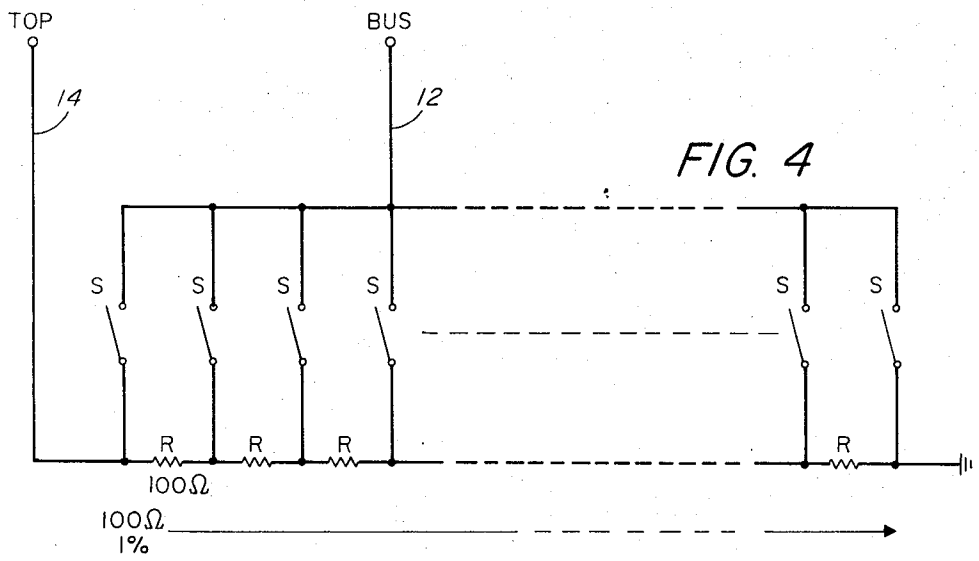


FIG. 4

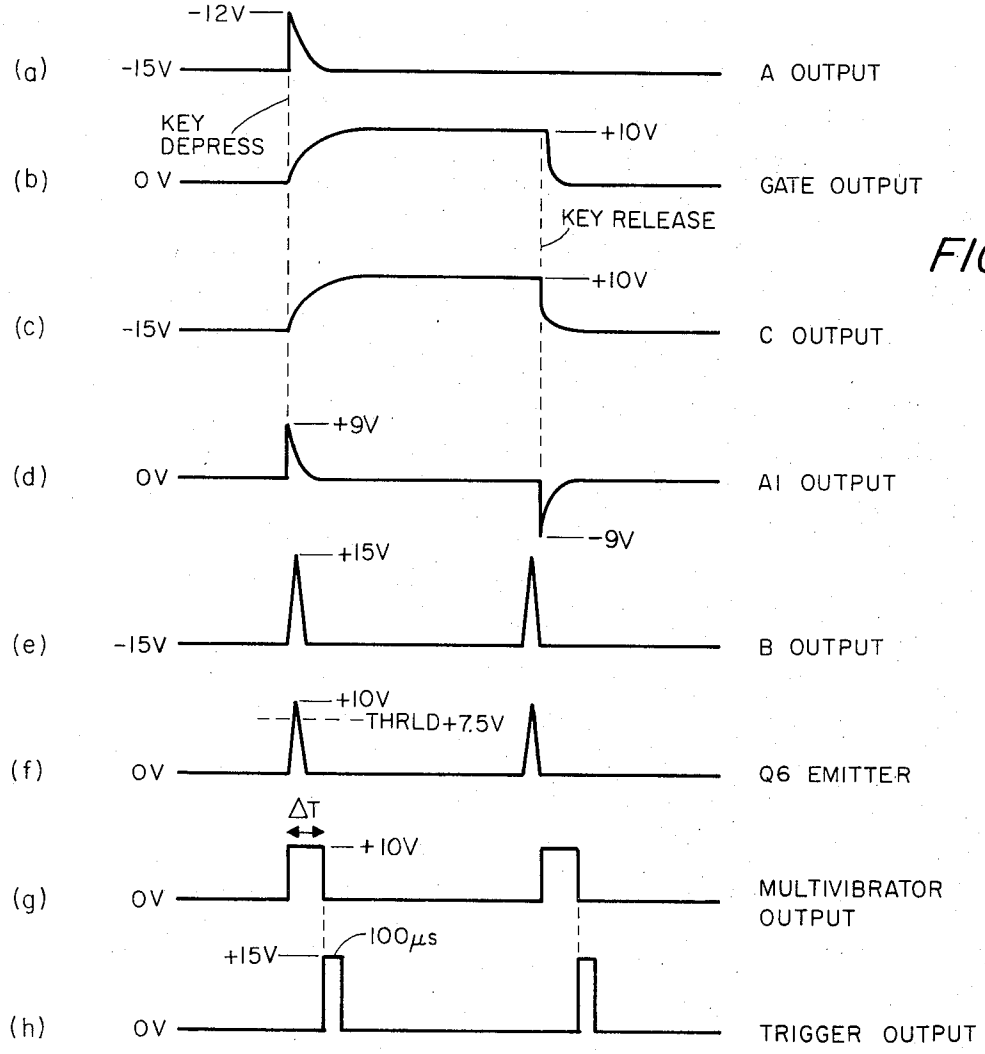

-12V
(a)
-15V
A OUTPUT
KEY DEPRESS
+10V
(b)
0 V
GATE OUTPUT
KEY RELEASE
+10V
(c)
-15V
C OUTPUT
+9V
(d)
0V
A1 OUTPUT
-9V
+15V
(e)
-15V
B OUTPUT
+10V
THRLD+7.5V
(f)
0V
Q6 EMITTER
ΔT
+10V
(g)
0V
MULTIVIBRATOR OUTPUT
+15V
100μs
(h)
0V
TRIGGER OUTPUT

FIG. 7

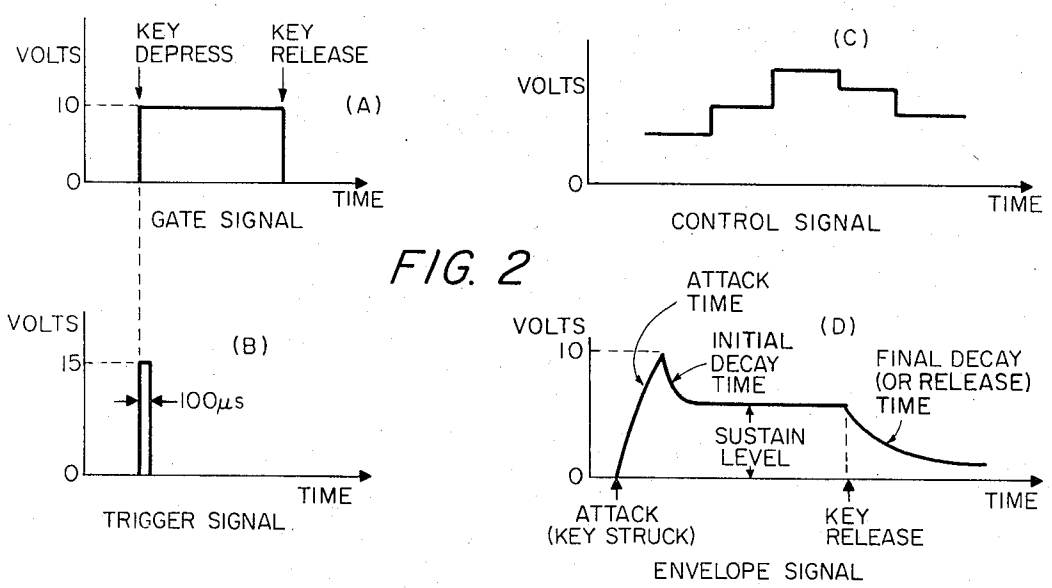

VOLTS
KEY DEPRESS
KEY RELEASE
10
(A)
0
TIME
GATE SIGNAL
(C)
VOLTS
0
TIME
CONTROL SIGNAL
VOLTS
15
(B)
100μs
0
TIME
TRIGGER SIGNAL
ATTACK TIME
VOLTS
10
(D)
INITIAL DECAY TIME
FINAL DECAY (OR RELEASE) TIME
SUSTAIN LEVEL
0
TIME
ATTACK (KEY STRUCK)
KEY RELEASE
ENVELOPE SIGNAL

FIG. 2

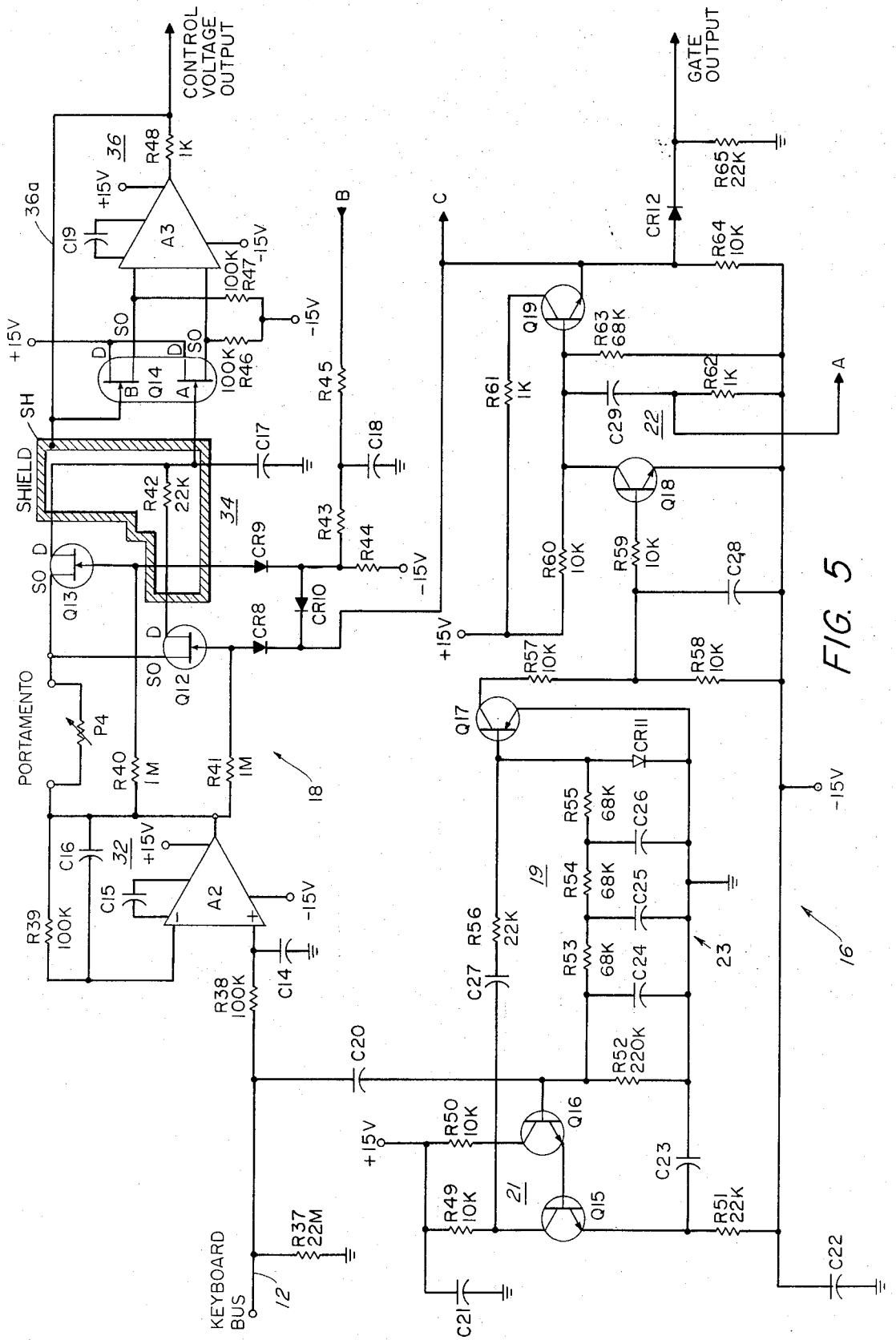

CONTROL VOLTAGE OUTPUT
GATE OUTPUT
KEYBOARD BUS
PORTAMENTO
SHIELD
A3
A2
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
CR8
CR9
CR10
CR11
CR12
+15V
-15V
A
B
C
18
19
21
22
23
16
12
34
36
36a
32

FIG. 5

FIG. 6

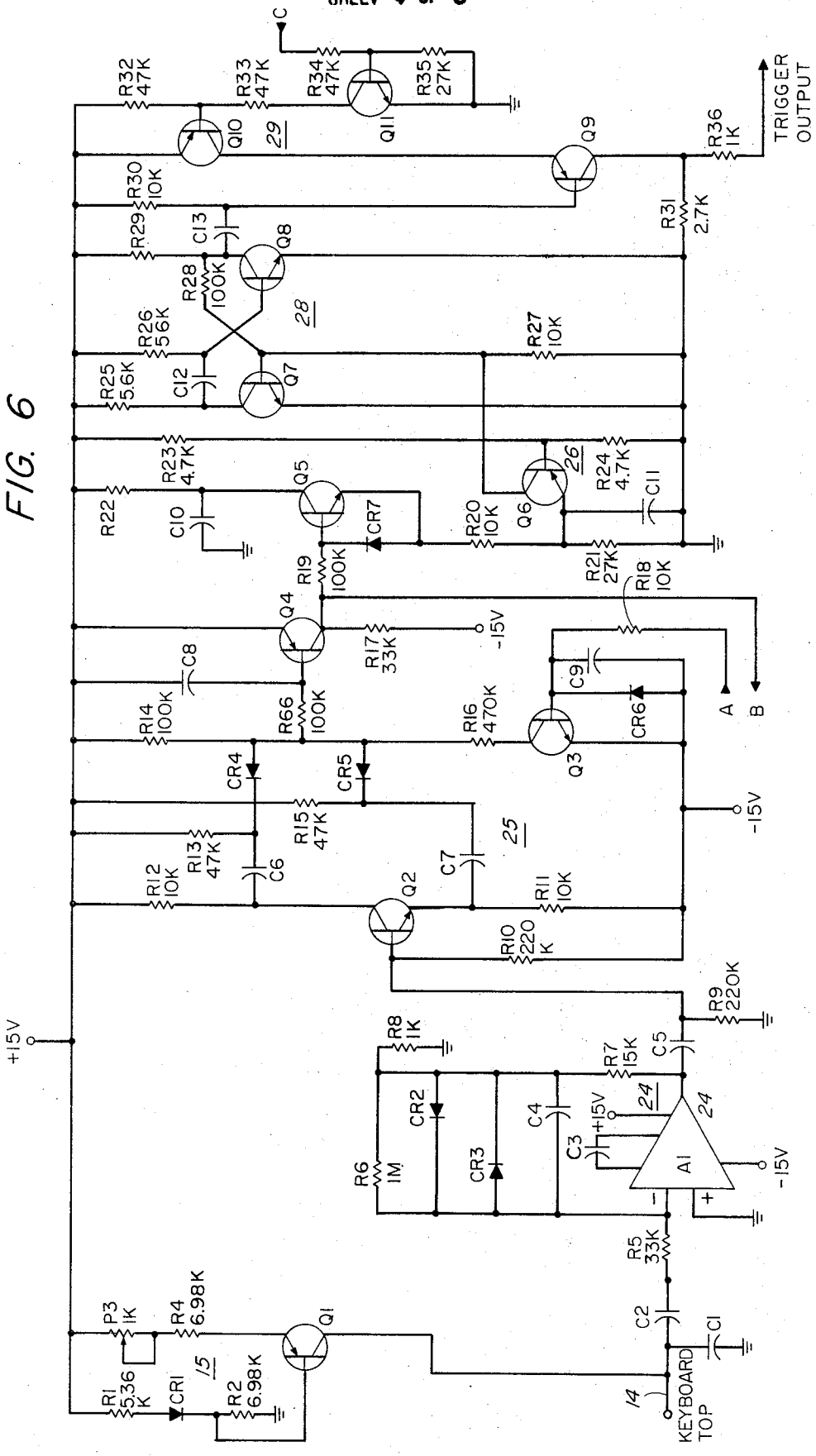
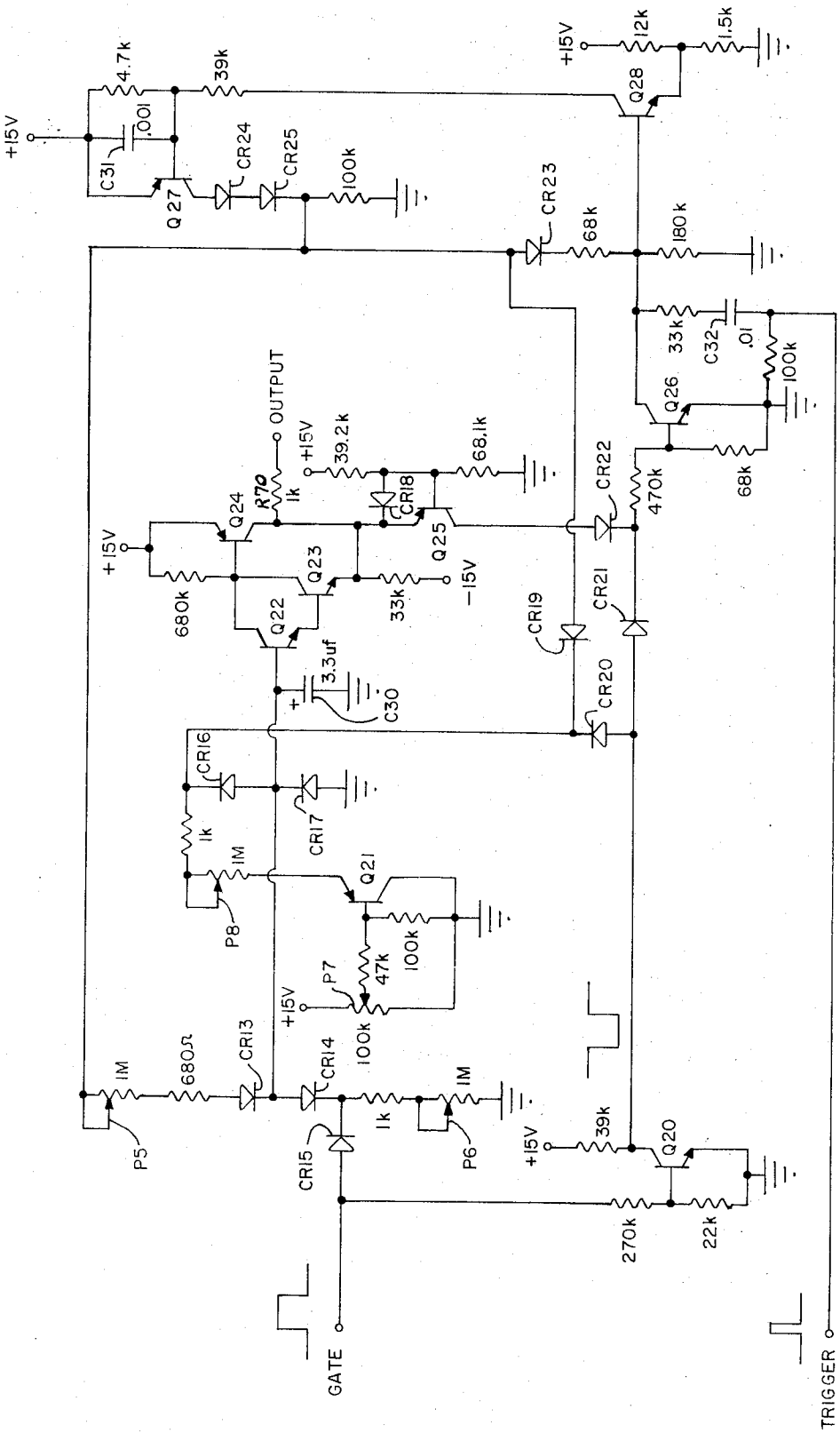

C
R32 47K
R33 47K
R34 47K
R35 27K
Q10
Q11
29
Q9
R36 1K
TRIGGER OUTPUT
R30 10K
R29
C13
Q8
R28 100K
28
R31 2.7K
R26 56K
R27 10K
R25 5.6K
C12
Q7
R23 4.7K
Q5
26
Q6
R24 4.7K
C11
R22
C10
CR7
R20 10K
R21 27K
R18 10K
R19 100K
Q4
R17 33K
-15V
C8
C9
CR6
A
B
R14 100K
R66 100K
R16 470K
Q3
CR4
CR5
R15 47K
25
R13 47K
R12 10K
C6
C7
Q2
R11 10K
R10 220 K
R9 220K
+15V
R8 1K
R7 15K
C5
CR2
C4
24
R6 1M
CR3
C3
A1
R5 33K
P3 1K
R4 6.98K
Q1
C2
C1
R1 5.36 K
CR1
15
R2 6.98K
14
KEYBOARD TOP

FIG. 8


+15V
4.7k
39k
.001
C31
Q27
CR24
CR25
100k
+15V
12k
1.5k
Q28
CR23
68k
180k
33k
C32
.01
100k
Q26
68k
470k
CR22
OUTPUT
+15V
39.2k
68.1k
R70
1k
Q24
CR18
Q25
+15V
680k
Q23
Q22
33k
-15V
CR19
CR21
3.3uf
C30
CR20
CR16
CR17
1k
1M
P8
Q21
100k
47k
P7
+15V
100k
CR13
CR14
680Ω
1M
1M
P5
CR15
1k
P6
+15V
39k
Q20
270k
22k
GATE
TRIGGER

CONTROL CIRCUITRY FOR ELECTRONIC MUSICAL INSTRUMENT

RELATED APPLICATION

This is a continuation-in-part of U.S. Pat. application Ser. No. 220,914 filed Jan. 26, 1972 now abandoned.

FIELD OF THE INVENTION

The present invention relates in general to an electronic musical instrument preferably of the keyboard type. More particularly, the present invention is directed to a new and improved control circuit for an electronic musical instrument. The present invention preferably employs a single bus which couples from an associated voltage divider means of the keyboard to the control circuitry, and the control circuitry includes means for providing a gate signal, a trigger signal, and a control voltage signal. These signals may couple to other conventional utilization circuits such as a voltage controlled oscillator or envelope generator.

BACKGROUND OF THE INVENTION

In known electronic musical instruments the control circuitry is usually coupled from at least two bus lines associated with the keyboard of the instrument. Each bus in turn has a voltage divider associated therewith. The voltages impressed on each bus are selectively coupled, upon actuation of the key or keys of the keyboard, to the control circuitry and the control circuitry includes means coupled to one bus for providing a gate signal and second means coupled to the other bus for providing a trigger signal. One disadvantage to this prior art scheme is that additional circuitry is needed to provide the two bus output. This also means that two voltage dividers have to be used. In the present invention, preferably a single bus is employed and is coupled from a single voltage divider to the control circuitry of the present invention.

Known control circuitry also has certain other disadvantages associated therewith such as not providing sufficient noise and switch bounce immunity, not providing an accurate control voltage signal, and an inaccurate time relationship between the gate, trigger, and control voltage signals. These and other disadvantages of the prior control circuits are believed to be overcome by the circuitry of the present invention.

OBJECTS OF THE INVENTION

Accordingly, one important object of the present invention is to provide improved control circuitry for use in an electronic musical instrument preferably of the keyboard type.

Another object of the present invention is to provide improved control circuitry as set forth in the preceding object and employing preferably a single bus coupled from the keyboard to the control circuitry.

A further object of the present invention is to provide a musical instrument having improved control circuitry as set forth in the preceding objects, that may be constructed relatively inexpensively, that is not unnecessarily complex, and that is characterized by other additional features set forth hereinafter.

SUMMARY OF THE INVENTION

To accomplish the foregoing and other objects of the invention, the electronic musical instrument is characterized by improved control circuitry preferably employing a single bus coupling from the keyboard to the control circuitry. The keyboard has means associated therewith for generating a signal, preferably of a voltage amplitude, corresponding to an actuated key of the keyboard, and a second signal or voltage level change indicative of the actuation of at least two keys or the release of at least one key. The control circuitry of this invention generally comprises gate signal means which may include an oscillator and gate circuit, sample/hold means for establishing a control voltage proportional to the voltage of the bus coupled from the keyboard, and trigger signal means preferably including an amplifier, trigger circuit, and threshold circuit.

One feature of the present invention is the novel sample/hold circuit. This sample/hold circuit preferably includes a pair of field effect transistors (FETs) and an output voltage follower.

Other features of the present invention reside in the use of an oscillator circuit as part of the gate signal means and in the use of a threshold circuit and multivibrator delay circuit as part of the trigger signal means.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of the present invention should now become apparent upon a reading of the following detailed description when read in conjunction with the following drawings in which:

FIG. **1** is a block diagram of an electronic musical instrument embodying the control circuitry of the present invention;

FIG. **2** shows a number of waveforms that are associated with the block diagram of FIG. **1**;

FIG. **3** shows a block diagram of a preferred embodiment for the control circuitry of the present invention;

FIG. **4** shows a detailed circuit schematic diagram of the keyboard and voltage divider of FIG. **3**;

FIG. **5** shows a circuit diagram of a portion of the control circuitry of the present invention including the gate signal means and the sample/hold means;

FIG. **6** shows a circuit diagram of the remainder of the control circuitry of the present invention including the trigger signal means;

FIG. **7** shows various waveforms associated with the circuitry of FIGS. **5** and **6**; and

FIG. **8** is a circuit diagram for the envelope generator of FIG. **1**.

DETAILED DESCRIPTION

Referring now to the drawings and in particular to FIG. **1**, there is shown a block diagram of an electronic musical system employing the improved control circuit of the present invention and associated single bus which is coupled from the keyboard to the control circuit.

The system of FIG. **1** in general comprises a keyboard and voltage divider **10**, control circuit **20**, envelope generator **40**, voltage controlled oscillator (V.C.O.) **50**, voltage controlled filter (V.C.F.) **60**, voltage controlled amplifier (V.C.A.) **70**, and output speaker **80**. Most of the blocks shown in FIG. **1** may be of conventional design with the exception, of course, of control circuit **20**. The keyboard and voltage divider **10** is shown in more detail in FIG. **4** and includes a resistor voltage divider and associated key actuated switches

for coupling respective voltage levels to the bus line **12.** Keyboard and voltage divider **10** may be of conventional design and preferably includes a second output line **14** coupled from a top end of the resistor voltage divider to control circuit **20.** When a key of the keyboard is depressed a corresponding voltage is coupled via line **12** to control circuit **20.** When at least two keys are depressed or a key is released with another being held, a level change occurs on output line **14,** as discussed in more detail hereinafter.

Control circuit **20** generates a control voltage signal having a voltage level at any given time which is proportional to the position of the key that is actuated. The purpose of the control voltage signal is to control the frequency of V.C.O. **50.** A typical control signal is shown in FIG. **2C** for one particular predetermined sequence of key actuations.

Control circuit **20** also generates a gate signal and a trigger signal both of which are coupled to envelope generator **40** which may be of conventional design. A gate signal is shown in FIG. **2A.** The gate signal is at its high state when a key is depressed and remains in this state as long as at least one key remains depressed. The gate signal controls the output of envelope generator **40** and generally sustains the signal transfer through another device such as voltage controlled filter **60.**

FIG. **2B** shows a trigger signal that may be generated by control circuit **20** and which is coupled to envelope generator **40** to initiate the attack of the note by the envelope generator. The trigger signal preferably commences at about the same time the gate signal goes high, or slightly thereafter, and as shown in FIG. **2B,** has a width of about **100** microseconds and an amplitude of +15 volts. The trigger signal appears momentarily at the start of each key depression.

A typical output of envelope generator **40** is depicted in FIG. **2D** and the particular waveform shown is controlled by the gate and trigger signals of shown in FIG. **1.** The attack time, initial decay time, and release time of the envelope generator output waveform may be conventionally controlled by RC time constant networks or the like of generator **40.** The output waveform shown in FIG. **2D** is coupled through potentiometers **P1** and **P2,** to voltage controlled filter **60** and voltage controlled amplifier **70,** respectively, to control the outputs from these two devices. The output of voltage controlled amplifier **70** then couples to output loudspeaker **80** in a conventional manner.

Referring now to FIG. **3,** there is shown a block diagram of a preferred embodiment of the control circuit **20** of FIG. **1.** Control circuit **20** generally includes keyboard and voltage divider **10** having bus **12** and current source **15** associated therewith, gate signal means **16,** trigger signal means **17,** and control voltage signal means **18.** A circuit schematic diagram of the keyboard and voltage divider **10** is shown in detail in FIG. **4,** and includes an output bus **12** which couples to the gate signal means **16** and the control voltage signal means **18.** The keyboard and voltage divider **10** also includes an output line **14** taken at the top of the voltage resistor string and which couples to the trigger signal means **17.**

The gate signal means includes an oscillator **19** and a gate circuit **22.** Oscillator **19** is free-running prior to depression of a key of the keyboard, and the output of oscillator **19** does not energize gate circuit **22.** When one of the keys of the keyboard is depressed the voltage impressed on bus **12** causes oscillator **19** to stop oscillating. This action causes the gate circuit **22** to be enabled and a gate output signal, such as the one shown in FIG. **7B** commences. In FIG. **7B** this signal is shown as rising to a positive level at a predetermined time constant upon depression of the key and reverting negatively when the key is released. The gate circuit **22** also generates an A output upon depression of the key as shown in FIG. **7A.** This A output is a positive going pulse that is coupled to trigger signal means **17** for generating a trigger output signal as discussed hereinafter. The gate circuit **22** also generates a C output which is coupled to control voltage signal means **18** and to trigger signal means **17.** The C output signal is shown in FIG. **7C** and is similar to the gate output signal of FIG. **7B** but has a different amplitude swing.

Trigger signal means **17** shown in FIG. **3** generally include an AC coupled amplifier **24,** a trigger circuit **25,** a threshold circuit **26,** a monostable multivibrator **28,** and an AND circuit **29.** As previously indicated when at least two keys are depressed, or a key is released with another being held, the total voltage across the voltage divider string changes and a voltage fluctuation is AC coupled from output line **14** to amplifier **24.** FIG. **7D** indicates the waveform at the output of amplifier **24** which shows a positive spike when the key is depressed and a negative spike when it is released. Trigger circuit **25** may be a full wave rectifier type circuit and also receives an input signal, namely signal A, from gate circuit **22** for enabling trigger circuit **25.** The B output shown in FIG. **7E** is a typical trigger output from trigger circuit **25** and couples to control voltage signal means **18.** The output of trigger circuit **25** couples to threshold circuit **26** which is only responsive to a pulse of a predetermined amplitude, such as the pulse shown in FIG. **7F,** in order to set monostable multivibrator **28.** Monostable multivibrator **28** delays the trigger pulse from trigger circuit **25** to assume that a trigger output signal is generated only when the gate output signal is still present, and the output of multivibrator **28** is coupled to AND circuit **29.** If the C output is still high the AND circuit **29** generates a trigger output signal as indicated in FIG. **7H,** for example. The trigger output signal is shown as having a relatively narrow pulse width and commences after the beginning of the gate output signal with the delay being determined by the multivibrator **28.**

The control voltage signal means **18** shown in FIG. **3** generally comprises a voltage follower **32,** an FET-capacitor hold circuit **34** and an output follower **36.** The voltage follower **32** is coupled to bus **12** and is responsive to the voltage impressed thereon for coupling a signal to circuit **34.** The circuit **34** is responsive to both the B and C signals for controlling the charging of a sample capacitor. The B signal controls the charging of the capacitor by way of a fast charge FET and the C signal sustains the capacitor charge via a second FET. The output of the capacitor is sensed by output follower **36** and the output of follower **36** is a control voltage signal such as the one shown in FIG. **2C.**

Referring now to FIG. **4** there is shown the keyboard and voltage divider **10** of FIGS. **1** and **3.** The keyboard includes a plurality of manually operable switches S which are actuable to couple different voltages from the resistive voltage divider to bus **12.** The resistive voltage divider comprises a plurality of resistors R connected in series from the top output line **14** to ground.

The current source **15** shown in FIG. **3** also couples to output line **14** and provides a constant current for each of the resistors R. In one embodiment each of these resistors is a 100 ohm resistor. When a single key is depressed the corresponding voltage from the voltage divider is coupled to bus **12.** When two or more keys are depressed the resistors therebetween are shunted and the voltage on line **14** shifts negatively, a value which is depended upon the positions of the actuated switches. When the switches are released, the output line **14** goes positive.

Referring now to FIGS. **5** and **6** there is shown a circuit diagram of the control circuit of FIG. **3** showing, in particular, the gate signal means **16,** the trigger signal means **17** and the control voltage signal means **18.** As previously indicated the gate signal means **16** comprises an oscillator **19** and a gate circuit **22.**

Oscillator **19** is a phase shift type oscillator and generally comprises an amplifier section **21,** a phase shift section **23,** and an output transistor Q17. The input to oscillator **19** is coupled by way of coupling capacitor C20 from bus **12** to the base of transistor Q16. The output of oscillator **19** may be taken at the collector of transistor Q17 and couples to an input transistor of gate circuit **22.**

When there is no key depressed the bus **12** is essentially floating with the exception of resistor R37 (high resistance), and transistors Q15 and Q16 of amplifier **21** are permitted to cyclically conduct at a preselected frequency of, for example, 200 KHz. The amplifier **21** also includes resistors R49 and R50 which couple from the collectors of transistors Q15 and Q16, respectively, to the +15 volt supply. Resistor R51 couples from the emitter of transistor Q15 to the −15 volt supply. Capacitors C21, C22, and C23 are coupling capacitors.

The phase shifter network **23** includes three filter sections including resistors R53–R55 and capacitors C24–C26. A feedback connection including capacitor C27 and resistor R56 is coupled from the collector of transistor Q15 to the base of transistor Q17. The three section filter network **23** provides an essentially 180° phase shift thus providing the regenerative feedback for oscillator **19.** While the oscillator is oscillating, transistor Q17 cyclically conducts and a current is provided by way of resistor R57 to capacitor C28 of gate circuit **22** thereby causing capacitor C28 to charge, holding transistor Q18 on.

When one of the keys of the keyboard is depressed, a relatively low impedance to ground on the order of hundreds of ohms is coupled by way of capacitor C20 to transistor Q16 holding transistors Q16 and Q15 off and preventing further oscillation of oscillator **19.** When this action occurs, transistor Q17 receives insufficient base current and is no longer conductive. Capacitor C28 discharges causing transistor Q18 to eventually turn off.

In addition to transistor Q18 the gate circuit **22** also includes transistor Q19. As previously indicated resistor R57 couples from the collector of transistor Q17 by way of resistor R59 to the base of transistor Q18. Resistor R58 couples from the junction between resistors R57 and R59 to the −15 volt supply and has capacitor C28 connected in parallel thereacross. Both transistors Q18 and Q19 have resistors R60 and R61 connected from their collectors, respectively, to the +15 volt supply. The collector of transistor Q18 also couples to the base of transistor Q19, by way of resistor R63 to the −15 volt supply, and by way of capacitor C29 and resistor R62 also to the −15 volt supply. The emitter of transistor Q19 couples to the C output and also by way of diode CR12 to the gate output. The gate output includes a terminating resistor R65 coupled to ground. The A output is taken between resistor R62 and capacitor C29.

When oscillator **19** is oscillating and transistor Q18 is conductive, capacitor C29 is charged and the A output is at essentially −15 volts (see FIG. 7A). At that time the conduction of transistor Q18 prevents transistor Q19 from conducting, the gate output is essentially at ground and the C output is at −15 volts (see FIGS. 7B and 7C). When the oscillator ceases oscillating transistor Q18 turns off fairly rapidly and as the charge across capacitor C29 cannot instantaneously change, the voltage at point A goes to −12 volts causing transistor Q19 to conduct. This action causes the gate output signal to reverse from a ground level to a +10 volt level with a time constant of about 2 milliseconds as determined at least in part by capacitor C29 and resistors R60 and R63. Similarly, the C output goes from −15 volts to +10, approximately. When the key is released transistor Q19 turns off farily rapidly and the gate signal reverts to ground in about 0.1 milliseconds.

Referring now to FIG. **6** there is shown a circuit diagram of the trigger signal means **17** which generally comprises amplifier **24,** trigger circuit **25,** threshold circuit **26,** multivibrator **28,** and AND circuit **29.** The output line **14** of keyboard and voltage divider **10** couples by way of capacitor C2 and resistor R5 to the negative input of operational amplifier A1. The positive input of amplifier A1 is grounded. As previously indicated, when two or more keys are depressed the voltage on line **14** decreases slightly, and when a key is released with another being held the voltage on line **14** increases.

FIG. **6** also shows the current source **15** which generally comprises transistor Q1 and associated resistors. Resistors R1 and R2 and diode CR1 couple in series from the +15 volt supply to ground and establish a bias for the base of transistor Q1. Resistor R4 and potentiometer P3 couple in series from the emitter of transistor Q1 to the +15 volt supply, and potentiometer P3 may be used for varying the constant current at the collector of transistor Q1, which current is coupled by way of output line **14** to the resistive voltage divider of FIG. **4.**

The fluctuations on output line **14** are AC coupled to the negative input of amplifier A1, and amplifier A1 may be a conventional operational amplifier. The amplifier A1 has, coupled between its input and output, a pair of oppositely poled diodes CR2 and CR3 which prevent saturation of amplifier A1 and enable a faster operation of the amplifier. Resistor R6 is coupled in series with resistor R7 between the input and output of amplifier A1 and resistor R6 together with resistor R5 define the AC gain of the amplifier which is on the order of **30** in one particular embodiment. Capacitor C4 which also couples between the input and output of amplifier A1 stabilizes the operation of the amplifier. The DC gain of the amplifier is controlled by resistors R7 and R8 and the output of the amplifier is limited to a + or −9 volts. Normally, when no key is being depressed the output of amplifier A1 is at approximately ground. When two or more keys are depressed the output of amplifier A1 is shown in FIG. 7D as a positive

impulse, and when a key is released FIG. 7D shows the negative impulse that occurs at the output which is coupled to trigger citcuit **25** by way of capacitor **C5.**

The trigger citcuit **25** generally comprises transistors **Q2, Q3** and **Q4.** Transistor **Q2** is normally (no key depressed) biased by resistors **R9–R12** and is in the active operating area. Resistors **R9** and **R10** provide a bias voltage of approximately −7.5 volts for the base of transistor **Q2.** Thus, when a positive pulse is coupled by way of capacitor **C5** from amplifier **A1,** transistor **Q2** tends to conduct harder. Alternatively, when a negative pulse is coupled to the base of transistor **Q2** it tends to conduct less current between its emitter and collector.

The collector of transistor **Q2** couples by way of capacitor **C6** and diode **CR4** to the base of transistor **Q4.** Similarly, the emitter of transistor **Q2** is coupled by way of capacitor **C7** and diode **CR5** to the base of transistor **Q4.** When transistor **Q2** is normally biased both diodes **CR4** and **CR5** are back-biased and transistor **Q4** is nonconducting. As indicated in FIG. **7E,** the B output is then at −15 volts. The B output is taken at the collector of transistor **Q4.** When transistor **Q2** is caused to change its conduction and, for example, conducts more current the collector voltage decreases, diode **CR4** instantaneously conducts, and transistor **Q4** also conducts via capacitor **C8** providing a positive pulse at the B output of approximately +15 volts. Similarly, when transistor **Q2** decreases in conduction diode **CR5** conducts, transistor **Q4** conducts and a similar B output is generated at the collector of transistor **Q4.**

As previously indicated with reference to FIG. **3** the trigger circuit **25** also produces a B output when only a single key is depressed by means of the A output signal from gate circuit **22.** For this purpose the trigger circuit **25** comprises transistor **Q3** whose collector couples by way of resistor **R16** and resistor **R66** to the base of transistor **Q4,** whose emitter is coupled to −15 volts, and whose base couples by way of resistor **R18** from the A output of gate circuit **22.** A diode **CR6** also couples from the base to emitter of transistor **Q3** and protects the transistor from excess negative voltages which may occur upon release of a key when the A output goes as negative as possibly to −30 volts.

When the A signal goes from −15 to −12 volts, transistor **Q3** is caused to instantaneously conduct thereby causing a momentary conduction of transistor **Q4** and the generation of a B output pulse like the one shown in FIG. **7E.**

The collector of transistor **Q4** (B output signal) couples to threshold circuit **26** which comprises transistors **Q5** and **Q6.** Transistor **Q5** has its collector coupled by way of resistor **R22** to to the +15 volt supply and also couples by way of storage capacitor **C10** to ground. A diode **CR7** couples between the emitter and base of transistor **Q5** and is used to protect the transistor against negative impulses. Resistors **R20** and **R21** connect in series between ground and the emitter of transistor **Q5** and the junction between these resistors couples to the emitter of transistor **Q6.** Resistors **R23** and **R24** which are of equal value bias the base of transistor **Q6** to approximately +7.5 volts. Resistors **R23** and **R24** establish a threshold level which may be varied by making one resistor variable. The output of the threshold circuit may be taken at the collector of transistor **Q6.**

When a B output signal occurs transistor **Q5** conducts and capacitor **C10** which was previously charged by way of resistor **R22** discharges rapidly through transistor **Q5** causing a positive pulse at the emitter of transistor **Q6.** The resistors **R20** and **R21** provide a voltage divider and if the B output pulse is a true pulse, and not a noise pulse possibly caused by switch bounce, the pulse at the emitter of transistor **Q6** should be on the order of +10 volts in maximum amplitude. With the base of transistor **Q6** at +7.5 volts transistor **Q6** will conduct and an output signal is coupled to multivibrator **28.** If the pulse at the emitter of transistor **Q6** is not sufficiently positive, transistor **Q6** will not conduct and a trigger output signal will not be subsequently generated. The effects of contact bounce are minimized by requiring capacitor **C10** to be charged to produce the trigger pulse, and by the +7.5 volt threshold required to turn on transistor **Q6.**

FIG. **6** also shows the monostable multivibrator **28** which is of conventional design and includes transistors **Q7** and **Q8** along with approximate biasing resistors and timing capacitor **C12.** In its unexcited state the multivibrator **28** has transistor **Q7** off and transistor **Q8** conducting with its output emitter at approximately ground. When transistor **Q6** conducts transistor **Q7** also goes into conduction temporarily and transistor **Q8** automatically turns off with its emitter reverting to a positive voltage. The "on" time or delay time provided by multivibrator **28** is controlled by capacitor **C12** and resistors **R25** and **R26.** After this delay has elapsed transistor **Q8** automatically conducts and its emitter goes back to ground. It is this ground-going signal that is coupled by way of capacitor **C13** to the base of transistor **Q9** which causes conduction of transistor **Q9,** but only if transistor **Q10** is also conducting.

The AND circuit **29** comprises transistors **Q10** and **Q11.** Transistor **Q11** has its emitter coupled to ground and its base coupled by way of resistor **R34** from the C output of gate circuit **22.** Resistor **R35** couples from the base to the emitter of transistor **Q11,** and resistors **R33** and **R32** couple in series from the collector of transistor **Q11** to the +15 volt supply. The base of transistor **Q10** connects intermediate resistor **R32** and **R33.** Transistor **Q10** provides a conduction path for transistor **Q9** but only when transistor **Q10** is conducting. Transistor **Q10** will be conducting when the C output is present and transistor **Q11** is thus conducting. For this condition the base of transistor **Q10** is more negative than the emitter and transistor **Q10** is on. If the C output is not present transistor **Q10** remains off and a trigger signal on the trigger output line will not be generated by way of resistor **R36.** A typical trigger output is shown in FIG. **7H** as going from approximately ground to a +15 volt level and lasting approximately 100 microseconds. One of the reasons for coupling the C output to the AND circuit **29,** and in fact for providing the AND circuit **29,** is to prevent a trigger output upon release of the key. Upon the release of a key, by the time that the ground-going signal is present at the collector of transistor **Q8,** the C signal is no longer present and thus no trigger output signal is generated.

Referring again to FIG. **5** there is shown the control voltage signal means **18** which generally comprises voltage follower **32,** FET capacitor hold circuit **34,** and output follower **36.** The voltage follower **32** includes operational amplifier **A2** which may be of conventional

design and has its positive input coupled by way of resistor R38 from bus 12. The input voltage on bus 12 which occurs when one or more keys are depressed is coupled by way of resistor R38 and capacitor C14 which together form a low pass filter. Amplifier A2 has a capacitor C16 coupled between its negative input and its output for stabilizing amplifier A2. The amplifier A2 is designed with unity gain and its output is coupled by way of resistors R40 and R41, and also portamento potentiometer P4 to circuit 34.

The FET capacitor hold circuit 34 generally comprises FET transistors Q12 and Q13 and sample capacitor C17. Resistor R41 couples to the gate of transistor Q12 and resistor 40 couples to the gate of transistor Q13. The gates of transistor Q12 and Q13 also couple by way of diodes CR8 and CR9 to the C and B outputs, respectively. The sources (SO) of transistors Q12 and Q13 couple together to potentiometer P4. The drain of transistor Q13 couples directly to capacitor C17 and the drain of transistor Q12 couples by way of high impedance resistance R42 to capacitor C17. The output of circuit 34 may be considered as taken at the ungrounded side of capacitor C17.

Circuit 34 also includes resistors R43 and R45 which are coupled in series between the cathode of diode DR9 and the B input from trigger circuit 25. Resistor R44 couples from the cathode of diode CR9 to the −15 volt supply and capacitor C18 couples to ground providing a slight delay of the B input pulse.

When a single key is depressed, the A signal is generated, the B output trigger is coupled to the cathode of diode CR9, and the output of amplifier A2, which is positive, is coupled by way of resistor R40, potentiometer P4, and FET 13 to cause a rapid charging of capacitor C17 to a voltage level corresponding to the voltage on bus 12. The portamento potentiometer P4 provides a variable time constant for the FET charging if this is desired. An ON-OFF switch may be associated with potentiometer P4 for including this feature or not. The C signal which is coupled to the cathode of diode CR8 keeps transistor Q12 on providing a trickle charge for capacitor C17 even after the B output pulse has terminated. Resistor R42 which is in series with capacitor C17 and FET transistor Q12 provides a slight lag so that the sudden change in the output of amplifier A2 upon release of a key does not affect the voltage across capacitor C17 before the decrease of the C output signal which shuts off transistor Q12. In addition, a diode CR10 prevents a B output signal from turning on transistor Q13 unless a gate signal is present. This feature adds further contact bounce immunity to the circuitry.

The output follower 36 includes a dual FET pair Q14 and amplifier A3 which may be a differential or operational amplifier. In the embodiment shown amplifier A3 operates as a differential amplifier and has a first input coupled from the source of transistor Q14A and a second input coupled from the source of transistor Q14B. The drain electrodes of both transistors Q14A and Q14B couple to the +15 volt supply. The gate electrode of transistor Q14A couples to capacitor C17 and the gate electrode of transistor Q14B couples to shield SH. The shield also couples by way of line 36A to the control voltage output terminal. By providing a feedback line 36A there should ideally be no current in the shield SH, thus stabilizing the voltage across capacitor C17.

Amplifier A3 receives a voltage from capacitor C17 and couples this signal from its output by way of resistor R48 to the control voltage output terminal. A typical control voltage is shown in FIG. 2C for a predetermined series of key depressions.

FIG. 8 shows one circuit diagram of an envelope generator that may be employed in the block diagram of FIG. 1. As previously indicated, this envelope generator receives a gate input signal as shown in FIG. 2A and a trigger input signal as shown in FIG. 2B and generates an output control waveform as shown in FIG. 2D. The gate signal controls the initiation of the attack and also the initiation of the release as depicted in FIG. 2, and the trigger signal, especially one that does not occur initially but occurs during the gate signal, controls additional attack-decay peaks.

In FIG. 8 the gate signal couples to diode CR15 and also to transistor Q20. The trigger signal couples via capacitor C32 to a bistable latch circuit including transistors Q27 and Q28. The output from the circuit FIG. 8 is tekan by way of resistor R70 from the collector of transistor Q24.

When the gate signal goes high diode (CR15) is forward-biased, diode CR14 is reversed-biased and a charging current is provided by way of potentiometer P5 and diode CR13 to integrating capacitor C30.

The trigger signal also goes positive at the same time approximately that the gate signal goes positive. This signal is coupled by way of capacitor C32 to the base of transistor Q28 causing that transistor to conduct. This action also causes transistor Q27 to conduct thereby providing the initial attack current by way of potentiometer P5 and diode CR13 to capacitor C30. When the trigger signal ends the transistors Q27 and Q28 remain conductive by the feedback path including diode CR23.

Thus the capacitor C30 is permitted to charge at a rate determined in part by potentiometer P5. As capacitor C30 charges the voltage at the emitter of transistor Q25 exponentially increases. When the voltage at the emitter of transistor Q25 exceeds the threshold voltage set at the base of transistor Q25, that transistor conducts thereby terminating the attack time interval. When transistor Q25 conducts transistor Q26 also conducts thereby causing the bistable latch circuit to reset. In other words, transistors Q27 and Q28 cease conduction. The initial attack current to potentiometer P5 then stops and the voltage across capacitor C30 no longer increases. The voltage across capacitor C30 then decays through diode CR16 potentiometer P8 and transistor Q21. The rate of decay of the voltage across capacitor C30 is controlled primarily by the setting of potentiometer P8. When this voltage has decayed sufficiently transistor Q21 stops conduction and the sustain interval commences wherein the voltage across capacitor C30 is maintained at a predetermined voltage as set by potentiometer P7 which couples to the base of transistor Q21.

When the gate signal reverts back to its low level, capacitor C30 is permitted to continue its discharge by way of diode CR14 and potentiometer P6. Thus, potentiometer P6 controls the release time constant as depicted in FIG. 2D. When the gate signal goes to its low-level the output of transistor Q20 goes to its high level thereby turning on transistor Q26 and assuring that the bistable latch circuit is reset.

At this point, only the initial trigger signal has been considered. If a trigger signal occurs at a later point during the gate signal another attack peak is generated. This trigger signal causes the bistable latch circuit to set again causing temporary attack current by way of potentiometer P5 and, thereafter, a decay current by way of potentiometer P8 until the voltage cross capacitor C30 reverts to its previous sustain level as set by potentiometer P7.

From the foregoing it can be seen that the output voltage coupled from the collector of transistor Q24 is a waveform of the type shown in FIG. 2D.

Having described one embodiment of the present invention other embodiments and modifications thereof are contemplated as falling within the spirit and scope of the present invention. The invention is thus to be limited only by the appended claims.

What is claimed is:

1. In an electronic musical instrument of the type having keyboard means including a keyboard, means for providing a first signal coupled from the keyboard the amplitude of which corresponds to the actuated key, and means for providing a second signal coupled from the keyboard indicative of the actuation of at least two keys or the release of a key, control circuitry coupled from the means for providing the first and second, signals and comprising, in combination:

first circuit means coupled from said first signal providing means for providing a gating signal which is present as long as at least one key is actuated;

second circuit means including delay means and coupled from said second signal providing means for providing a triggering signal which is generally of shorter duration than the gating signal and is present at about the commencement of the gating signal;

sample and hold means coupled from said first signal providing means and enabled by the gating signal derived from said first circuit means for establishing a control signal proportional to the first signal,

and means coupled from said second circuit means for controlling operation of said sample and hold means.

2. The circuitry of claim **1** wherein said keyboard circuitry includes a voltage divider having a plurality of resistors coupled in series and a current source feeding the voltage divider,

said first signal being coupled from said voltage divider at a point corresponding to the actuated key,

and said second signal being coupled from an end of said voltage divider.

3. The circuitry of claim **2** wherein said keyboard has a number of key actuated switches and said keyboard and voltage divider are arranged with each key actuated switch coupled to a corresponding resistor of the voltage divider so that actuation of two keys bypasses the associated resistors therebetween causing said second signal to decrease, and releasing a key causes said second signal to increase.

4. The circuitry of claim **1** wherein said first circuit means comprises an oscillator and a gate circuit for generating a gate pulse upon the actuation of at least one key which is coupled to the second circuit means for providing the triggering signal when one key is actuated, and wherein said oscillator couples from said first signal providing means to said gate circuit.

5. The circuitry of claim **4** wherein said oscillator includes an amplifier section and a phase shift section, said oscillator including means defining a low impedance path for inhibiting said amplifier section to stop oscillator operation upon actuation of a key.

6. The circuitry of claim **4** wherein said sample and hold means includes a capacitor charge network and means copuling said gating signal to said capacitor charge network to provide a charging current thereto for the approximate duration of the gating signal.

7. The circuitry of claim **6** wherein said charging current is a holding current.

8. The circuitry of claim **1** wherein said second circuit means comprises an AC coupled amplifier coupled from the second signal providing means, and a trigger circuit coupled from the AC coupled amplifier and responsive to actuation of at least two keys or the release of a key to provide the triggering signal.

9. The circuitry of claim **8** wherein said first circuit means comprises a gate circuit for generating a gate pulse upon the actuation of a key, said trigger circuit comprises an input circuit for receiving said gate pulse for providing the triggering signal when one key is actuated.

10. The circuitry of claim **9** wherein said trigger circuit comprises a phase splitter network and an output transistor which is conductive when the output of the AC coupled amplifier goes positive or negative from a predetermined reference level.

11. The circuitry of claim **1** wherein said second circuit means includes a trigger circuit coupled from the second signal providing means for providing the triggering signal and said first circuit means comprises a gate circuit for generating a gate impulse, said trigger circuit also including means responsive to the gate impulse for providing the triggering signal.

12. The circuitry of claim **11** wherein said sample and hold means includes a capacitor charge network and means coupling said triggering signal to said capacitor charge network to provide an initial charging current thereto for the duration of the triggering signal.

13. The circuitry of claim **12** comprising means coupling said gating signal to said capacitor charge network to provide a sustaining charging current thereto for the approximate duration of the gating signal.

14. The circuitry of claim **13** wherein said capacitor charge network includes a pair of transistors, one being controlled by the gating signal and the other being controlled by the triggering signal.

15. The circuitry of claim **14** wherein said transistors are field effect transistors and comprising a capacitor having one side coupled to both said transistors.

16. The circuitry of claim **1** wherein said second circuit means comprises a trigger circuit coupled from the second signal providing means and a threshold circuit coupled from the trigger circuit and responsive to a triggering signal of a predetermined amplitude or greater for activating the threshold circuit.

17. The circuitry of claim **16** comprising a delay circuit coupled from said threshold circuit for delaying the triggering signal.

18. The circuitry of claim **17** comprising an AND circuit coupled from the delay circuit and the first circuit means for generating a trigger output signal when said

delayed triggering signal is present and said gating signal is present.

19. The circuitry of claim **18** wherein said delay circuit includes a monostable multivibrator.

20. The circuitry of claim **16** wherein said threshold circuit includes a transistor and resistor means for biasing the control electrode of the transistor at a fixed threshold level.

21. The circuitry of claim **1** wherein said sample and hold means includes an input voltage follower coupled from the first signal providing means, a capacitor charging network coupled from the voltage follower and responsive to both the gating and triggering signals, and an output follower coupled from the capacitor charging network and having a control voltage output terminal.

22. The circuitry of claim **21** wherein said output follower includes a pair of field effect transistors coupled from the capacitor charging network and a different circuit coupled from the transistors to the output terminal.

23. The circuitry of claim **1** wherein said sample and hold means includes a charging network coupled from the first signal providing means and including a capacitor means, and first and second field effect transistors coupling from an input of the network to the capacitor means, said first transistor having a control electrode responsive to said gating signal for controlling the conduction of said first transistor to sustain the charge on said capacitor means while a key is being actuated, said second transistor having a control electrode responsive to said triggering signal for controlling the conduction of said second transistor to initially quick charge said capacitor means upon actuation of a key.

24. In an electronic musical instrument of the type having keyboard circuitry including a keyboard means for providing a first signal the amplitude of which corresponds to the actuated key, and means for providing a second signal indicative of the actuation of at least two keys or the release of a key, control circuitry coupled from the means for providing the first and second signals and comprising, in combination;

a first circuit means coupled from said first signal providing means for providing a gating signal;

a second circuit means coupled from said second signal providing means for providing a triggering signal which is generally shorter in duration than the gating signal and is present at about the commencement of the gating signal;

third circuit means coupled from said first signal providing means for establishing a control signal proportional to the first signal,

means coupled from said second circuit means for controlling operation of said third circuit means,

and means coupled from said first circuit means to said second circuit means for providing the triggering signal when one key is actuated.

25. The circuitry of claim **24** comprising means responsive to said gating signal for enabling the output of said second circuit means.

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