May 19, 1970 D. W. SCHLICHER 3,512,405

ANNUNCIATOR AND CONTROL SYSTEM WITH SPECIFIC APPLICATION TO INTERNAL COMBUSTION ENGINES

Original Filed July 24, 1967 2 Sheets-Sheet 1

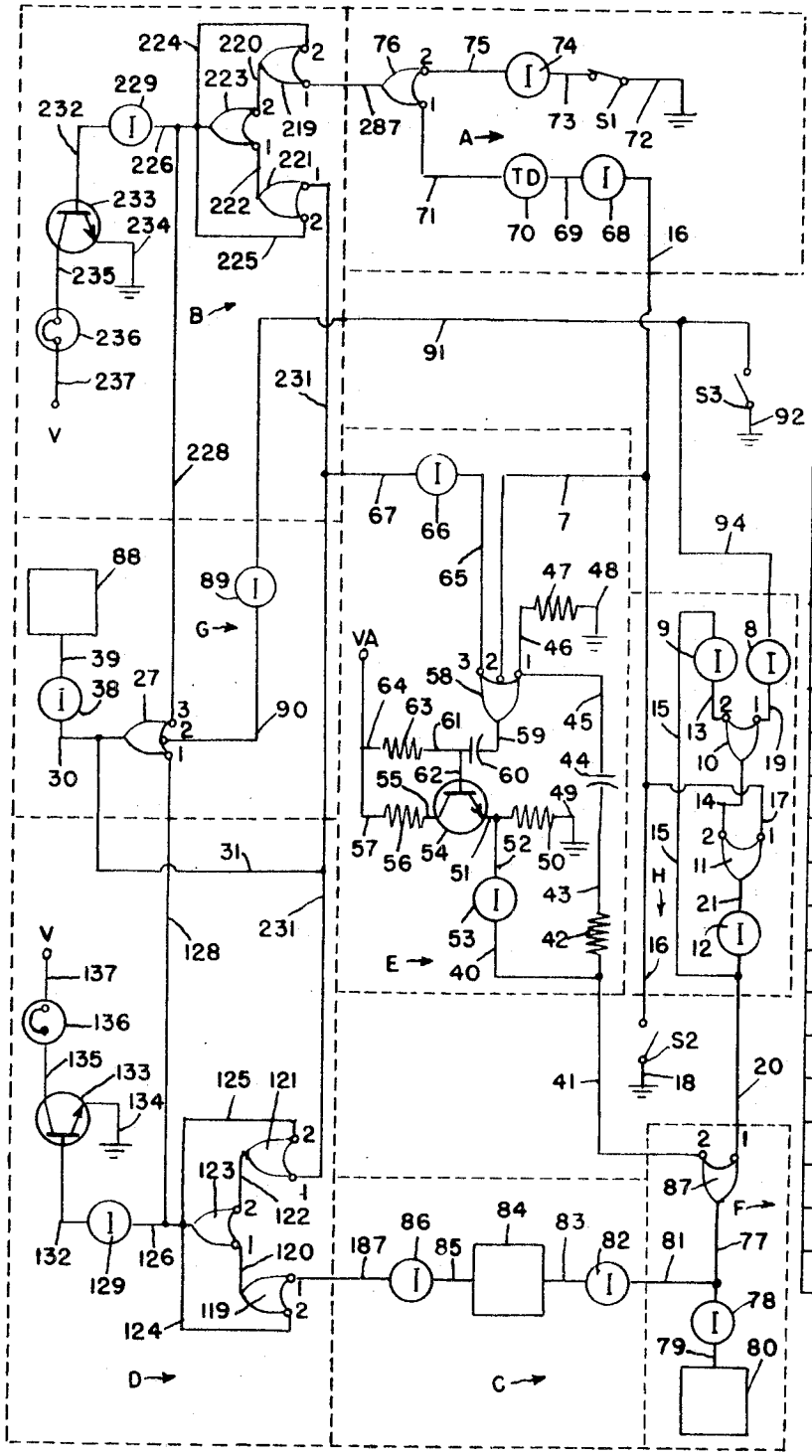


FIG. 1

FIG. 2

LOGIC NO.	INPUTS 1	2	3	OUTPUT
8	0			1
9	0			1
10	1	1		0
11	0	0		1
12	1			0
27	0	1	0	0
38	0			1
53	0			1
58	0	0	1	0
66	0			1
68	0			1
74	1			0
76	1	0		0
78	0			1
82	0			1
86	1			0
87	0	1		0
89	0			1
119	0	0		1
121	0	0		1
123	1	1		0
129	0			1
219	0	0		1
221	0	0		1
223	1	1		0
229	0			1

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FIG. 3

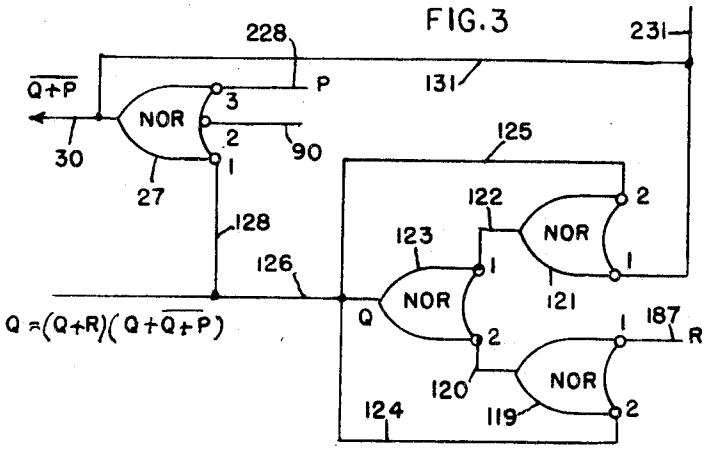


FIG. 4

TRUTH TABLE

INPUTS		OUTPUTS	
R	P	Q	$\overline{Q+P}$
0	0	Q_n	$\overline{Q_n}$
1	0	1	0
0	1	Q_n	0
1	1	Q_n	0

FIG. 5

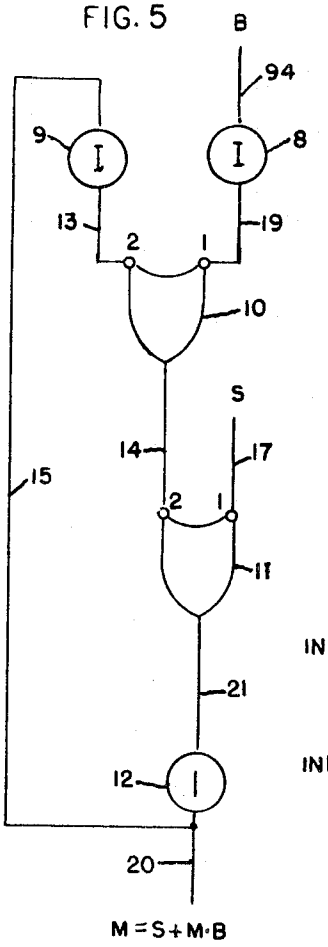
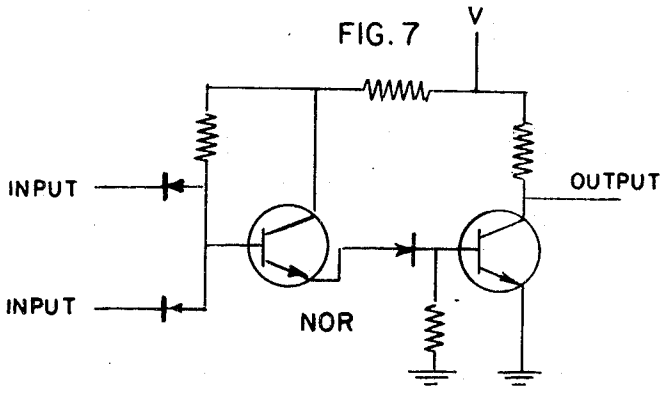


FIG. 6

TRUTH TABLE

INPUTS		OUTPUT
B	S	M
0	0	0
1	0	M_n
1	1	1
0	1	1

FIG. 7



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ANNUNCIATOR AND CONTROL SYSTEM WITH SPECIFIC APPLICATION TO INTERNAL COMBUSTION ENGINES

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Int. Cl. G01m 15/00

U.S. Cl. 73—116 2 Claims

ABSTRACT OF THE DISCLOSURE

An annunciator and control system including annunciators adapted to indicate faults in internal combustion engine operation and a control means for shutting down the system or correcting the fault together with lockout means for rendering the first to act annunciator operative and to lock out all the other annunciators prior to resetting of the system.

CROSS REFERENCES

A division of application for patent of David W. Schlicher for Annunciator and Control System With Specific Application to Internal Combustion Engines, Ser. No. 655,591, filed July 24, 1967.

FIELD OF THE INVENTION

Annunciators adapted to indicate faults in the operation of internal combustion engines together with a control for shutting down the engine or correcting the fault.

PRIOR ART

Annunciators in which the circuits therefor are independent of one another.

SUMMARY OF THE INVENTION

The invention resides in providing intercommunicating circuits between the annunciators and by means of which the operation of one annunciator locks out all the other annunciators thereby indicating only the first fault to occur.

To simplify the drawings and description of the invention symbolic logic has been used and Boolean expressions for the various outputs are employed along with truth tables. In the instant case negative logic is employed and NOR gates and inverters have been used. A logical 1 thus represents a low voltage state while a logical 0 represents a high voltage state. It will, however, become evident that other gates may be used.

In the drawings:

FIG. 1 is a schematic diagram using Boolean gates and inverters and disclosing the invention in use for controlling the operation of a diesel engine.

FIG. 2 is a table showing the initial logic states of the various logic devices of the circuits disclosed in FIG. 1.

FIG. 3 is a schematic diagram of the engine starting annunciator section of the invention.

FIG. 4 is a truth table for the inputs and outputs of the circuits shown in FIG. 3.

FIG. 5 is a schematic diagram of the engine crank termination and lockout section.

FIG. 6 discloses the truth table for the crank termination circuit shown in FIG. 5.

FIG. 7 is a wiring diagram of the components of one of the NOR gates used in the invention.

As an example of the use of the invention it is assumed that the invention is to be used with a diesel engine. For controlling the operation of the engine one method is to

control the flow of fuel to the same and an electrically operated valve not illustrated may be used for the purpose. Such an engine requires a starting motor for turning over the engine and in the event that the engine does not start, the usual practice is to shut off the starting motor, wait for a short time and make another try. If after several tries the engine will not start it is customary to cease trying and ascertain and correct the fault. In addition, numerous other engine faults may occur such as oil failure, excessive temperature at various localities such as bearings, windings, etc., low voltage, low speed, low fuel, etc. One fault such as improper lubrication may cause several other faults such as reduced speed, low voltage, and temperature increase, thus making it impossible to readily ascertain the cause of the faults. The instant invention overcomes this disadvantage by maintaining the indication of the first fault to occur and locking out the indications of all the other faults. To simplify the disclosure only the indicating means for failure of the engine to start and oil failure have been disclosed though it will be readily comprehended that as many faults as desired may be indicated by the use of additional fault circuits.

The structure disclosed comprises a lubrication fault sensitive section A which operates a lubrication fault indicating section B. Similarly an engine overcrank detection section C operates an overcrank fault indicating section D. Both the sections B and D operate a control section G which stops the engine whenever B or D indicate a fault. A multivibrator section E provides alternate crank-rest timing periods and energizes the starting motor through the crank control section F. Section H controls crank termination and lockout after the engine starts.

The section A comprises a normally closed oil pressure switch S1 which is connected to ground by means of a conductor **72**. This switch is further connected by means of a conductor **73** to an inverter **74**, which, in turn, is connected by a conductor **75** to input **2** of a two input NOR gate **76**. Input **1** of this gate is connected to a time delay device **70** by means of conductor **71** which in turn is connected to inverter **68** by conductor **69**. A conductor **16** connects inverter **68** to a centrifugally operated switch S2 which is grounded by conductor **18**.

The section B includes three two input NOR gates **219**, **221**, and **223**. The output of gate **76** is connected by a conductor **287** to input **1** of gate **219**. The output of gate **219** is connected by means of a conductor **220** to the input **2** of gate **223**. Input **1** of this gate is connected by a conductor **222** to the output of gate **221** while the output of gate **223** is connected by means of a conductor **226** to inverter **229**. The output of gate **223** is further connected by means of conductors **224** and **225** to the inputs **2** of gates **219** and **221**. This inverter is connected by means of a conductor **232** to the base of a transistor **233**. A conductor **234** connects the emitter of said transistor to ground. The collector of said transistor is connected by means of a conductor **235** to a lamp **236** which, in turn, is connected by means of a conductor **237** to a source of direct current V. The lamp **236** constitutes the lubrication fault annunciator.

The overcrank detection section C consists of two inverters **82** and **86** and a binary counter **84**. This counter may be of ordinary construction and has not been shown in detail. Inverter **82** is connected by means of conductor **83** to the binary counter **84**. This counter is connected by a conductor **85** to inverter **86**.

The overcrank indicator D indcludes 3 NOR gates **119**, **121**, and **123**. The input **1** of NOR gate **121** is connected to the conductor **231**, which, in turn, is connected to input **1** of NOR gate **221**. Input **2** of NOR gate **121** is connected by means of a conductor **125** to the output of NOR gate **123**. The input **2** of NOR gate **119** is connected

by means of a conductor **124** to the output of NOR gate **123**. Input **1** of NOR gate **119** is connected by means of conductor **187** to inverter **86** previously referred to. The output of NOR gate **119** is connected by means of a conductor **120** to the input **1** of NOR gate **123**. The output of NOR gate **121** is connected by means of a conductor **122** to the input **2** of NOR gate **123**. The output of NOR gate **123** is connected by means of a conductor **126** to an inverter **129**. This inverter is connected by means of a conductor **132** to the base of a transistor **133**. The emitter of this transistor is connected by a conductor **134** to ground. The collector of transistor **133** is connected by means of a conductor **135** to a lamp **136** which serves as the annunciator for the section D of the invention. This lamp is further connected by conductor **137** to a source of voltage v.

The crank-rest timing section E utilizes a multivibrator which may be of ordinary construction. This multivibrator utilizes a NOR gate **58** having 3 inputs. Input **1** of this gate is connected by means of a conductor **46** to a resistor **47** which, in turn, is connected by a conductor **48** to ground. Input **2** of the gate **58** is connected by means of a conductor **7** to the conductor **16** previously referred to. Input **3** of this gate is connected by means of a conductor **65** to an inverter **66** which is connected by a conductor **67** to the conductor **231**. The output of NOR gate **58** is connected by means of a conductor **59** to a capacitor **60** which, in turn, is connected by means of a conductor **61** to a resistor **63**. This resistor is connected by a conductor **64** to a source of voltage VA. The conductor **61** is connected by means of another conductor **62** to the base of a transistor **54**. The emitter of this transistor is connected by means of a conductor **51** to a resistor **50** which, in turn, is connected by means of a conductor **49** to ground. The emitter is further connected to inverter **53** by means of conductor **52**. The collector of transistor **54** is connected by means of conductor **55** to resistor **56**. This resistor is connected by a conductor **57** to said source of voltage VA. Said inverter **53** is further connected by means of conductor **40** to resistor **42** which is connected by a conductor **43** to capacitor **44**. This capacitor is further connected to said input **1** of NOR gate **58**.

The crank control section F utilizes a two input NOR gate **87**. Input **2** of this gate is connected by a conductor **41** to conductor **40** previously referred to. The output of NOR gate **87** is connected by a conductor **77** to an inverter **78**. This inverter is connected by means of a conductor **79** to a solenoid and other mechanism **80** for cranking the engine.

The control section G of the invention utilizes a triple input NOR gate **27**. Input **1** of this gate is connected by means of a conductor **128** to conductor **126**. Input **3** of this gate is connected by means of a conductor **228** to the conductor **226**. The output of gate **27** is connected by means of a conductor **30** to an inverter **38**. Inverter **38** is connected by a conductor **39** to a solenoid and mechanism **88** for controlling the flow of fuel to the engine. A conductor **31** is connected to conductor **30** and also to conductor **231**.

For starting up the system a switch **S3** is employed which is connected by means of a conductor **92** to ground. The switch S3 is further connected by a conductor **91** to an inverter **89** which is connected by means of a conductor **90** to the input **2** of NOR gate **27**.

The crank termination section H includes two inverters, **8** and **9**. The output of the inverter **9** is connected by means of a conductor **13** to the input **2** of a NOR gate **10**. The output of inverter **8** is similarly connected by means of a conductor **19** to input **1** of said NOR gate **10**. The output of NOR gate **10** is connected by means of a conductor **14** to the input **2** of a NOR gate **11**. The output of this NOR gate is connected by means of a conductor **21** to an inverter **12**. A conductor **15** connects the output of inverter **12** to the input of inverter **9**. The input **1** of NOR gate **11** is connected by means of a conductor **17** to conductor **16** previously referred to.

The operation of the invention is as follows: The table shown in FIG. 2 gives the initial state of all of the logic elements shown in FIG. 1. To crank the engine switch S3 is closed which applies a logical 1 to inverters **8** and **89**. Referring to the diagram in FIG. 5 and the truth table in FIG. 6 it is seen that with the input at switch S3 changing from 0 to 1 and with the input at switch S2 equal to 0 the output of inverter **12** remains in its previous state which was a logical 0. The logical 0. The logical 1 input to NOR **89** causes the following changes of state to occur: NOR **89** output becomes a logical 0 which in effect makes the P input of FIG. 3 equal to a logical 0 and unlocks all the fault indicator circuits. Specifically in FIG. 1, input **2** of NOR **27** is a logical 0 which changes the output to logical 1. This output is applied to inverter **38** which changes state and causes the solenoid and accessories **88** to be energized and changes inputs **1** of NOR **121** and **221** to a logical 0. This now places control of NOR **123** and **223** upon a change of state or NOR **119** and **219** respectively and this will occurs anytime a fault indication is obtained. The logical 1 output of NOR **27** is also applied to inverter **66** which applies a logical 0 to input **3** of NOR **58** and starts the astable multivibrator E. The output of the multivibrator is applied to the input **2** of NOR **87** where a logical 0 represents a period of cranking and logical 1 represents a period of resting. Cranking is accomplished by applying the changing output of NOR **87** to inverter **78** which controls the crank energization. The crank period which is the order of 10 to 20 seconds is controlled by resistor **63** and capacitor **60**. The rest period is determined by values of resistor **42** and capacitor **44**. These alternate crank-rest periods continue until the engine starts or until the binary counter **84** counts the preset number of cranks at which time a logical 0 is applied to inverter **86** which, in turn, applies a logical 1 to input **1** of NOR **119**. This represents the R input to NOR **119** of FIGS. 1 and 3 and the truth table of FIG. 4 shows that the indication output Q now goes to a logical 1 and the control output $\overline{Q+P}$ goes to a logical 0.

The indication output from NOR **123** is applied to inverter **129** which causes the overcrank lamp **136** to light and to input **2** of NOR **119** and NOR **121** which latches on this fault circuit. The control output from NOR **27** deenergizes the engine through inverter **38** and locks out the low-oil-presure fault circuit A through NOR **221**. This can be seen more clearly by referring to the truth table in FIG. 4. It will become evident with respect to the over crank circuit that the input P is 0, so after R once becomes **1**, the input remains latched in the 1 state. With reference to the low-oil-pressure fault circuit, the P input is the Q output of the over crank circuit and since this is 1 the Q output remains in the same state regardless of the R input.

The operation just described was based on the assumption that three was no engine start. In the event of a start, speed switch S2 closes when the engine reaches the desired speed. A logical 1 is then applied to input **1** of NOR **11**, input **2** of NOR **58** and inverter **68**. This terminates cranking, stops the multivibrator and starts the time delay device **70** operating. The oil pressure switch S1 must now open before time device **70** times out or NOR **76** would change state and indicate a low oil pressure fault. Operation would then be the same as with the overcrank fault except that the function of the two fault circuits would be reversed. With switch S1 opening before the time delay device **60** times out NOR **76** would not change state and the engine would continue running until shut down was desired and switch S3 was opened or until some monitored fault shut it down.

Although only two fault circuits are shown, any number of similar fault circuits could be added with the outputs feeding the corresponding number of inputs of NOR **27**.

The advantages of the invention are manifest. The first fault to occur would indicate the origin of the same, and said fault corrected. Frequently one fault causes one or more other faults and an indication of the first fault and correction thereof might remove one or more of the other faults.

Changes in the specific form of the invention, as herein described, may be made within the scope of what is claimed without departing from the spirit of the invention.

Having described the invention, that is claimed as new and desired to be protected by Letters Patent is:

1. An annunciator and control system adapted to be used in an engine control system comprising:

(a) a first fault detecting means detecting failure of the engine to start,

(b) a first annunciating means operated by said first fault detecting means,

(c) a second fault detecting means,

(d) a second annunciating means operated by said second fault detecting means,

(e) control means operable by either of said fault detecting means,

(f) lock-out means actuated by said first or second fault detecting means and upon occurrence of the first fault, rendering the fault detecting means therefor operative to actuate the corresponding annunciating means and the control means operable and upon subsequent occurrence of a different fault rendering the corresponding annunciating means inoperative,

(g) said first fault detecting means including,

(h) engine cranking means,

(i) timing means producing alternating starting and rest periods periodically actuating said engine cranking means,

(j) over cranking monitoring means actuated upon cranking of the engine a predetermined number of times, and

(k) cranking terminating means actuated by said over cranking monitoring means and operating said first annunciating means.

2. An annunciator and control system according to claim **1** in which the timing means is an astable multivibrator producing a square wave and periodically operating said engine cranking means.

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JERRY W. MYRACLE, Primary Examiner

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