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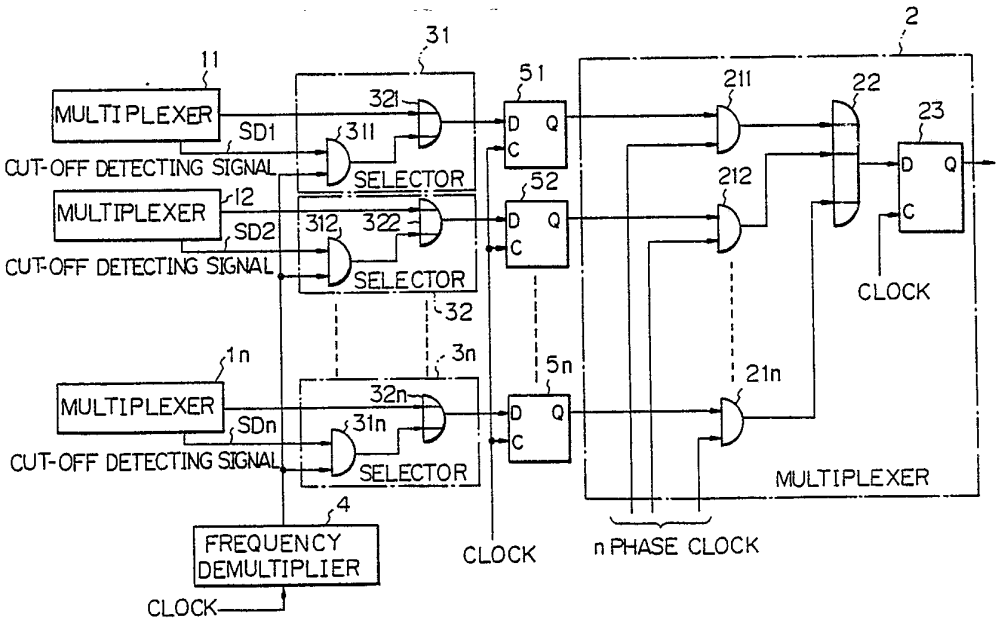

(57) Abstract

A multiplex system for further multiplexing signals output by low group multiplexers (11-1N) by means of a high group multiplexer (2). In this system, when at least one of the low group multiplexers is in a fault state, an alternating pattern signal is supplied to the high group multiplexer instead of the signal output by the faulty low group multiplexer, whereby the ratio of '0' and '1' of the signal output by the high group multiplexer becomes almost 1:1.

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DESCRIPTION

TITLE OF THE INVENTION

Multiplex System

TECHNICAL FIELD

The present invention relates to an improvement of a multiplex system used in a hierarchical data transmission system in which a plurality of signals output by multiplexers are further multiplexed and transmitted to a transmission line, especially an optical transmission line.

BACKGROUND ART

A hierarchical transmission system is known in which, for example, 9-channel data trains, each having a transmission rate of 45 Mb/s, are multiplexed by low group multiplexers to obtain a multiplexed data train of 405 Mb/s and , for example, two of these multiplexed data trains are further multiplexed by a high group multiplexer to obtain a multiplexed data train of 810 Mb/s, and this high group multiplexed data train is electro-optic converted by an optical interface circuit and transmitted to an optical transmission line, whereby a large amount of data transmission is performed. In this system, the output signals of the low group multiplexers are scrambled at the highest speed now possible, whereby the ratio of "1" and "0" of the output signal becomes almost equal.

In such a system, when one of the low group multiplexers becomes unavailable through a fault occurrence, the unavailable multiplexer outputs "0" or "1" continuously. Accordingly, the ratio of "0" and "1" of the output signal does not become equal.

However, when the unavailable low group multiplexer outputs, for example, "0" continuously, if the transmission rate of the system is very high and the number of low group multiplexers is small, for example, two, it is difficult to extract a timing clock from a received

signal in the receiver side, therefore normal reception becomes impossible. On the other hand, when the unavailable low group multiplexer outputs "1" continuously, if this system is used in the optical transmission system, the lighting time of a light emission element, for example a semiconductor laser, becomes long in comparison with the case in which a fault does not occur, and accordingly, the life time of the light emission element is shortened.

Accordingly, an object of the present invention is to provide an improved multiplex system which can facilitate the extraction of the timing clock at the receiver side and prolong the life time of the light emission element at the transmitter side.

DISCLOSURE OF THE INVENTION

According to a fundamental aspect of the present invention, there is provided a multiplex system comprising a plurality of first multiplexers, a second multiplexer for further multiplexing signals output by the first multiplexers, means for generating an alternating pattern in synchronization with the signals output by the first multiplexer, and switching means provided for each of the first multiplexers for selectively outputting the signals output by the related first multiplexer or the alternating pattern to the second multiplexer, wherein the switching means related to the first multiplexer, the output signal of which is cut off, outputs the alternating pattern signal in place of the signal output by the first multiplexer.

According to another aspect of the present invention, there is provided a multiplex system comprising a plurality of first multiplexers, a second multiplexer for further multiplexing signals output by the first multiplexers, a generator for generating an alternating pattern signal in synchronization with the signals output by the first multiplexers, and a plurality of selectors provided for each of the first multiplexers

for selecting the signal output by the related first multiplexer when the related first multiplexer assumes a normal state, and selecting the alternating pattern signal when the related first multiplexer assumes a fault state and outputting the selected signal to the second multiplexer.

According to another aspect of the present invention, there is provided a multiplex system comprising a plurality of first multiplexers, a second multiplexer for further multiplexing signals output by the first multiplexers, and means for supplying a selected signal to the second multiplexer, which means is provided for each of the first multiplexers, wherein the signal output by the related first multiplexer is selected when the related first multiplexer assumes a normal state, and an internally generated alternating pattern signal is selected when the related first multiplexer assumes a fault state.

According to another aspect of the present invention, there is provided a signal supplying circuit being capable of selectively outputting an external input signal or an internally generated alternating pattern signal, the circuit comprising a D type flip-flop, the output signal thereof being available as the output signal of the supplying circuit, a NOR gate having two input terminals, wherein the output signal of the D type flip-flop is input to one terminal and a mode changing signal is input to the other, and an OR gate having two input terminals, wherein the external input signal is input to one terminal and the output signal of the NOR gate is input to the other.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of a multiplex system according to the present invention will be described with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a prior art multiplex system;

Fig. 2 is a block diagram of an embodiment of a multiplex system according to the present invention;

Fig. 3 and Fig. 4 show time charts of signal-waveforms for explaining the operation of the system shown in Fig. 2;

Fig. 5 is a block diagram of another embodiment according to the present invention;

Fig. 6 is a time chart of the signal-waveform of the Fig. 5 system; and

Fig. 7 and Fig. 8 are block diagrams of further embodiments according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Before describing the embodiments of the present invention, a prior art and the disadvantages therein will be described. Figure 1 is a block diagram of a multiplex system of the prior art. In Fig. 1, 11 to 1n are n number of low group digital multiplexers, 2 a high group multiplexer. The multiplexer 2 comprises AND gates 211 to 21n, an OR gate 22, and a flip-flop 23. Each of AND gates 211 to 21n has two input terminals, to one of which a data signal output by the related multiplexer is led and to the other a clock having an n multiplied clock rate of the timing clock of multiplexers 11 to 1n, i.e. n phase clock of multiplexers 11 to 1n. Output signals of the AND gates 211 to 21n are led to the flip-flop 23 for shaping the waveform.

In the Fig. 1 system, a further multiplex of the output signals of multiplexers 211 to 21n is performed by opening AND gates 211 to 21n in sequence to send these data signals of the multiplexers 211 to 21n in sequence to the flip-flop 23 to shape the waveform.

However, in the Fig. 1 system, if one of multiplexers 11 to 1n becomes unavailable due to a fault, that unavailable multiplexer outputs "0" or "1" sequentially, as a result, the ratio of "0" and "1" of the signal output by the multiplexer 2 does not become equal. Therefore, extraction of the timing clock at the

receiver side becomes difficult and the life time of the light emission element at the transmitter side is shortened.

Figure 2 illustrates an embodiment of a multiplex system according to the present invention. In Fig. 2, 11 to 1n are n units of digital low group multiplexers, 2 a high group multiplexer, 31 to 3n n units of selector, 4 a 1/2 frequency demultiplier as a pattern generator, and 51 to 5n D type flip-flops for shaping the waveform. In all later figures, the same references represent the same components.

The multiplexers 11 to 1n output a multiplexed data train of a low group as an output signal respectively. These multiplexed data trains are scrambled by each of the multiplexers respectively, therefore, the ratio of "0" and "1" of the output signal in a normal state becomes almost 1:1. When these multiplexers 11 to 1n become unavailable due to a fault, these multiplexers 11 to 1n output "0" continuously. These multiplexers 11 to 1n are provided with a fault detector which detects the fault and outputs an output cut-off detecting signal at a continuous "1" level. Of course, this fault detector may be equipped outside of the multiplexers 11 to 1n.

Selectors 31 to 3n are provided for each of the multiplexers 11 to 1n respectively, and comprises AND gates 311 to 31n and OR gates 321 to 32n respectively. In selectors 31 to 3n, the AND gates 311 to 31n have two input terminals. The detecting signals SD1 to SDn from multiplexers 11 to 1n are respectively led to one of the input terminals of the AND gates 311 to 31n, and the alternating pattern signal from the frequency demultiplier 4 is input to the other input terminal thereof. Also, OR gates 321 to 32n have two input terminals, and the data signals output by the multiplexers 11 to 1n are respectively led to one of the input terminals and output signals of the AND gates 311 to 31n are respectively led to the other terminal thereof.

These selectors 31 to 3n select the data signals output by multiplexers 11 to 1n when the detecting signals SD1 to SDn are "0" respectively, select the alternating pattern signal from the frequency demultiplier 4 when the detecting signals are "1" respectively, and supply the selected signals to the multiplexer 2 via flip-flops 51 to 5n respectively.

The 1/2 frequency demultiplier 4 divides the timing clock of the multiplier by 2 in frequency, thereby outputting the alternating patterns signal which alternates "0" and "1" in a 1/2 frequency of the timing clock. The flip-flops 51 to 5n are operated by the timing clock of the multipliers 11 to 1n to shape the waveform of the input signal.

The multiplexer 2 is the same as that shown in Fig. 1. The output signal of the multiplexer 2 is supplied to the optical interface circuit (not shown) which includes a light emission element such as the semiconductor laser, and then transmit it to the optical transmission line.

The mode of operation of the system shown in Fig. 2 will now be described by referring to Fig. 3 and Fig. 4. In the normal state, multiplexers 11 to 1n output a data signal, and the output cut-off detecting signals SD1 to SDn are "0". Accordingly, selectors 31 to 3n select the data signals from the multiplexers 11 to 1n, and supply them to the multiplexer 2 via the flip-flop 51 to 5n. In this case, as shown in Fig. 3 (a) and Fig. 4 (a), the output signal of the multiplexer 2 repeats the data signals from the multiplexers 11 to 1n in sequence. Figure 3 shows the time chart of the signal output by the multiplexer 2 when the number n of the multiplexers 1 to 1n is 2, and Fig. 4 shows the same when the number n is 4. The ratios of "0" and "1" of the signals output by the multiplexers 11 to 1n are 1:1, since these signals are scrambled.

Now if, for example, the multiplexer 11 becomes

unavailable due to a fault, the signal data output by the multiplexer 11 becomes "0" and at the same time the detecting signal SD1 becomes "1". Therefore, the selector 31 selects the alternating pattern signal of the frequency demultiplier 4 instead of the output signal of the multiplexer 11 and supplies it to the multiplexer 2 via the flip-flop 51.

As a result, as shown in Fig. 3(b) and Fig. 4(b), the data portion of the multiplexer 11 in the output signal of the multiplexer 2 alternates "0" and "1" in sequence, and therefore the ratio of "0" and "1" of the signal output by the multiplexer 2 becomes almost 1:1 in spite of the fault at the multiplexer 11. Accordingly, the extraction of the timing clock at the receiver side becomes easy, and if this system is used in the optical data transmission system, the life time of the light emission element becomes longer in comparison with the case where a continuous "1" is output from the unavailable multiplexer 1.

Figure 5 illustrates another embodiment of the multiplex system according to the present invention. In the system shown in Fig. 5, the selection function of the selectors, the alternating pattern generating function of the frequency demultiplier, and the waveform shaping function of the flip-flop in the Fig. 2 system are realized by one circuit, i.e., a signal supplying circuit, thereby reducing the number of components and adapting for a high transmission rate. In Fig. 5, the system comprises multiplexers 11 to 1n, signal supplying circuits 61 to 6n provided for each of the multiplexers 11 to 1n, and the multiplexers 2. The multiplexers 11 to 1n and multiplexer 2 have the same function as those of Fig. 2 except that the output cut-off detecting signals SD1 to SDn from the multiplexers 11 to 1n are "1" level in the normal state and "0" level in the fault state.

Signal supplying circuits 61 to 6n comprise OR

gates 61 to 6n, NOR gates 621 to 62n, and flip-flops 631 to 63n respectively. Data signals output by the multiplexers 11 to 1n are led to one of the input terminals of the OR gates 611 to 61n respectively. Output signals of the OR gates 611 to 61n are led to data input terminals of the flip-flops 631 to 63n respectively. Output signals Q of the flip-flop 631 to 63n are led to the multiplexer 2 at the same time to one of the input terminals of the NOR gates 621 to 62n respectively. The detecting signals SD1 to SDn are led to the other input terminals of the NOR gates 621 to 62n respectively. Output signals of the NOR gates 621 to 62n are led to the other input terminals of the OR gates 611 to 61n respectively. The timing clock of the multiplexers 11 to 1n is led to the clock input terminals of the flip-flops 631 to 63n.

The operation of the system shown in Fig. 5 will be described hereinafter. As an example, the operation of the signal supplying circuit 61 will be described. Figure 6 is a time chart of the signal waveforms of the circuit 61. In Fig. 6, (a) represents the date output signal from the multiplexer 11, (b) a low group timing clock, (c) an output cut-off detecting signal SD1 from the multiplexer 11, (d) an output signal of the flip-flop 631, (e) an output signal of the OR gate 611, and (f) an output signal of the NOR gate 621.

In the normal state, the NOR gate 621 is closed, since the output cut-off detecting signal SD1 is "1". Therefore, the data signal output by the multiplexer 11 is input to the flip-flop 631 via the OR gate 611. The flip-flop 631 shapes the waveform of the date output signal and then sends it to the multiplexer 2.

On the other hand, when the multiplexer 11 becomes unavailable due to a fault at time t1, the data output signal thereof is cut-off, i.e., becomes "0" continuously, and at the same time, the detecting signal SD1 changes from "1" to "0", whereby the NOR gate 621 is

opened. Therefore, the output signal Q of the flip-flop 631 is reversed by the NOR gate 621 and fed back to the data input terminal D of the flip-flop 631 via the OR gate 611. As a result, the flip-flop 631 operates as a 1/2 frequency demultiplier,i.e., a binary counter, and outputs an alternating signal, obtained by dividing in frequency the timing clock by 2, to the multiplexer 2 instead of the data signal output by the multiplexer 11.

Accordingly, the output signal of the signal supplying circuit 61 has the ratio of "0" and "1" of almost 1:1. Using this signal supplying circuit, a single flip-flop is commonly used as the flip-flop for frequency dividing and the flip-flop for waveform shaping, whereby the number of the components is reduced in comparison with the Fig. 2 system, and the system may be adapted for the high rate transmission system.

Figure 7 illustrates another embodiment of the signal supplying circuit according to the present invention. In Fig. 7, an inverted output signal $\bar{Q}$ of a flip-flop 73 is fed back to a data input terminal thereof via an AND gate 72 and OR gate 71. The output cut-off detecting signal SD is led to an inverting input terminal of the AND gate 72. This signal supplying circuit also outputs the alternating pattern signal instead of the data signal from the low group multiplexer when the detecting signal SD becomes "0".

Figure 8 illustrates another embodiment of the multiplex system according to the present invention in which the signal supplying circuit of Fig. 6 is utilized as the alternating pattern generator. In Fig. 8, 8 is an AND gate, 6 the signal supplying circuit, and 91 and 92 selectors. As shown in Fig. 8, the output cut-off detecting signals SD1 and SD2 are led to the AND gate 8 to obtain the logical product thereof, and the output signal of the AND gate 8 is led to the input terminals of OR gate 61 and NOR gate 62. This signal supplying circuit outputs the alternating signal to the selec-

tors 91 and 92 when at least one of the detecting signals SD1 and SD2 become "0".

Although preferred embodiments have been described, various modifications and alterations are possible within the scope of the present invention.

CAPABILITY OF EXPLOITATION IN INDUSTRY

As can be seen from the above description, a multiplex system according to the present invention can be used in a hierarchical data transmission system in which a plurality of signals output by multiplexers are further multiplexed and transmitted to a transmission line, especially an optical transmission line.

CLAIMS

1. A multiplex system comprising;

a plurality of first multiplexers;

a second multiplexer for further multiplexing signals output by the first multiplexers;

means for generating an alternating pattern in synchronization with the signals output by the first multiplexers; and

and switching means provided for each of the first multiplexers for selectively outputting one of the signals output by the related first multiplexer and the alternating pattern to the second multiplexer,

wherein the switching means related to the first multiplexer having an output signal which is cut off, outputs the alternating pattern in place of the output signal of the first multiplexer.

2. A multiplex system comprising:

a plurality of first multiplexers;

a second multiplexer for further multiplexing signals output by the first miltiplexers;

a generator for generating an alternating pattern signal in synchronization with the signals output by the first multiplexers; and

a plurality of selectors provided for each of the first multiplexers for selecting the signal output by the related first multiplexer when the related first multiplexer assumes a normal state and selecting the alternating pattern signal when the related first multiplexer assumes a fault state and outputting the selected signal to the second multiplexer.

3. A multiplex system according to claim 2 wherein the pattern generator is comprised of a frequency demultiplier for dividing a timing clock of the first multiplexers by two.

4. A multiplex system according to claim 2 wherein each of the selectors comprised;

an AND gate having two input terminals,

the alternation pattern signal of the pattern generator being input to one terminal and the fault indicating signal of the related first multiplexer being input to the other; and

an OR gate having two input terminals, the output signal of the AND gate being input to one terminal and the output signal of the related first multiplexer being input to the other.

5. A multiplex system according to claim 2 wherein each of the signals output by the selectors is input to the second multiplexer via a D flip-flop for shaping a waveform.

6. A multiplex system comprising:

a plurality of first multiplexers;

a second multiplexer for further multiplexing signals output by the first multiplexers; and

means for supplying a selected signal to the second multiplexer, which means is provided for each of the first multiplexers, wherein the signal output by the related first multiplexer is selected when the related first multiplexer assumes a normal state, and an internally generated alternating pattern signal is selected when the related first multiplexer assumes a fault state.

7. A multiplex system according to claim 6 wherein the supplying means includes D type flip-flop operated by a timing clock of the first multiplexers, and constituted so that the signal output by the related first multiplexer is wave-shaped by the D type flip-flop and supplied to the second multiplexer when the related first multiplexer assumes a normal state, and the alternating pattern signal having 1/2 timing clock rate of the first multiplexers is generated by leading the polarity-reversed output signal of the D type flip-flop to a data input terminal thereof and supplied to the second multiplexer when the related first multiplexer falls into a fault state.

8. A multiplex system according to claim 7 wherein the supplying means comprises;

a D type flip-flop having an output signal which is supplied to the second multiplexer;

a NOR gate having two input terminals, the output signal of the D type flip-flop being input to one terminal and the fault indicating signal of the related first multiplexer being input to the other; and

an OR gate having two input terminals, the output signal of the related first multiplexer being input to one terminal and the output signal of the NOR gate being input to the other, and supplying the output signal thereof to the data input terminal of the D type flop-flop.

9. A signal supplying circuit being capable of selectively outputting one of an external input signal and an internally generated alternating pattern signal, the circuit comprising:

a D type flip-flop, an output signal therof being available as the output signal of the supplying circuit;

a NOR gate having two input terminals the output signal of the D type flip-flop being input to one terminal and a mode changing signal being input to the other; and

an OR gate having two input terminals, the external input signal being input to one terminal and the output signal of the NOR gate being input to the other.

AMENDED CLAIMS

[received by the International Bureau on 19 August 1986 (19.08.86)
original claims 1-9 replaced by amended claims 1-8 (4 pages)]

1. (amended) A multiplex system comprising:

a plurality of first multiplexers;

a second multiplexer for further multiplexing signals output from the first multiplexers by simply converting parallel input signals to a serial output signal;

a generator for generating an alternating pattern signal in synchronization with the signals output by the first multiplexers; and

a plurality of selectors provided for each of the first multiplexers for selecting the signal output by the related first multiplexer when the related first multiplexer assumes a normal state and selecting the alternating pattern signal when the related first multiplexer assumes a fault state and outputting the selected signal to the second multiplexer.

2. (amended) A multiplex system according to claim 1 wherein the pattern generator is comprised of a frequency demultiplier for dividing a timing clock of the first multiplexers by two.

3. (amended) A multiplex system according to claim 1 wherein each of the selectors comprised:

an AND gate having two input terminals, the alternation pattern signal of the pattern generator

being input to one terminal and the fault indicating signal of the related first multiplexer being input to the other; and

an OR gate having two input terminals, the output signal of the AND gate being input to one terminal and the output signal of the related first multiplexer being input to the other.

4. (amended) A multiplex system according to claim 1 wherein each of the signals output by the selectors is input to the second multiplexer via a D flip-flop for shaping a waveform.

5. (amended) A multiplex system comprising:

a plurality of first multiplexers;

a second multiplexer for further multiplexing signals output from the first multiplexers by simply converting parallel input signals to a serial output signal; and

means for supplying a selected signal to the second multiplexer, which means is provided for each of the first multiplexers, wherein the signal output by the related first multiplexer is selected when the related first multiplexer assumes a normal state, and an internally generated alternating pattern signal is selected when the related first multiplxer assumes a fault state.

6. (amended) A multiplex system according to claim 5 wherein the supplying means includes D type flip-flop operated by a timing clock of the first

multiplexers, and constituted so that the signal output by the related first multiplexer is wave-shaped by the D type flip-flop and supplied to the second multiplexer when the related first multiplexer assumes a normal state, and the alternating pattern signal having 1/2 timing clock rate of the first multiplexers is generated by leading the polarity-reversed output signal of the D type flip-flop to a data input terminal thereof and supplied to the second multiplexer when the related first multiplexer falls into a fault state.

7. (amended) A multiplex system according to claim 6 wherein the supplying means comprises:

a D type flip-flop having an output signal which is supplied to the second multiplexer;

a NOR gate having two input terminals, the output signal of the D type flip-flop being input to one terminal and the fault indicating signal of the related first multiplexer being input to the other; and

an OR gate having two input terminals, the output signal of the related first multiplexer being input to one terminal and the output signal of the NOR gate being input to the other, and supplying the output signal thereof to the data input terminal of the D type flip-flop.

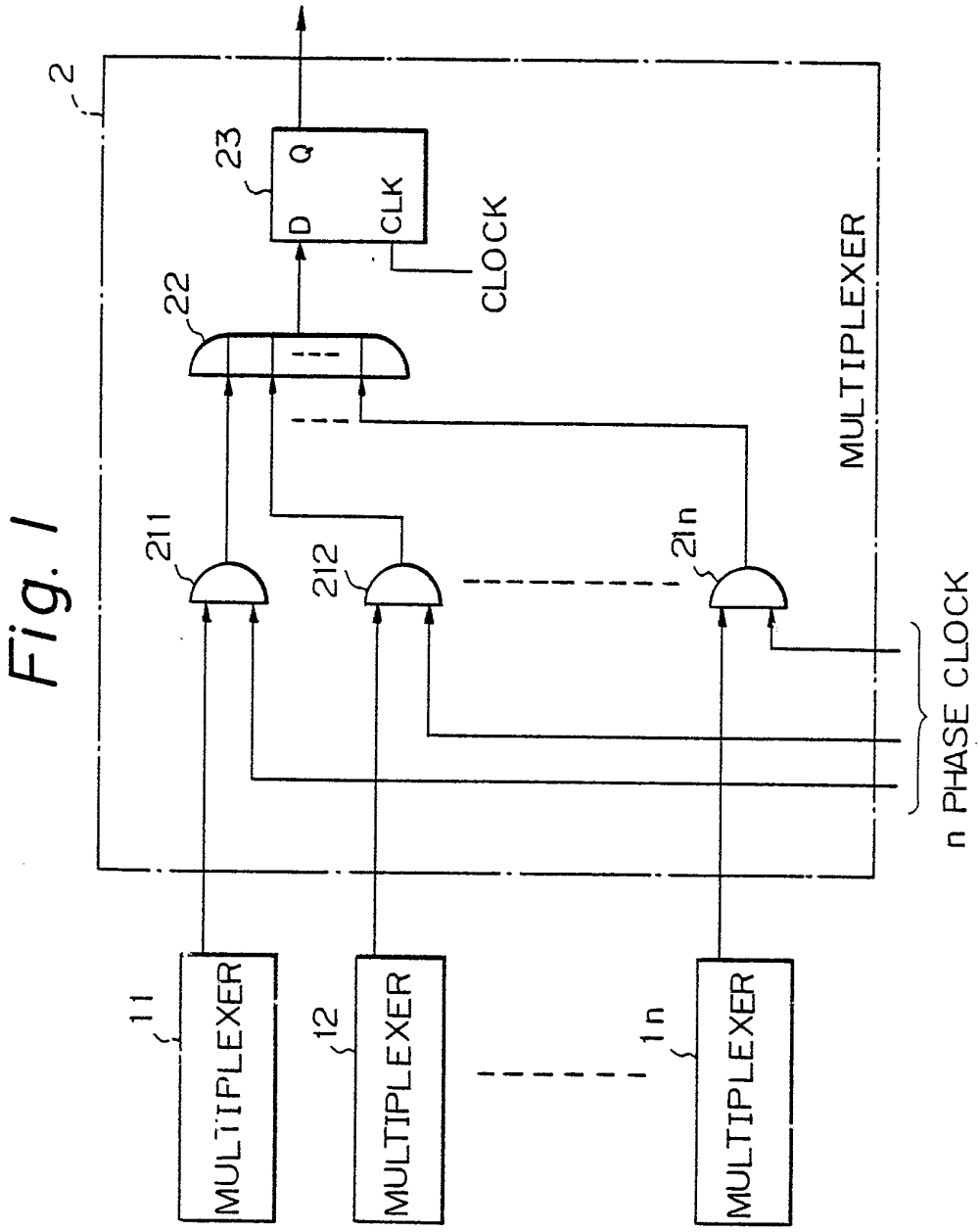
8. (amended) A signal supplying circuit being capable of selectively outputting one of an external input signal and an internally generated alternating pattern signal, the circuit comprising:

a D type flip-flop, an output signal thereof being available as the output signal of the supplying circuit;

a selecting gate having two input terminals the polarity-reversed output signal of the D type flip-flop being input to one terminal and a mode changing signal being input to the other; and

an OR gate having two input terminals, the external input signal being input to one terminal and the output signal of the NOR gate being input to the other.

Fig. 1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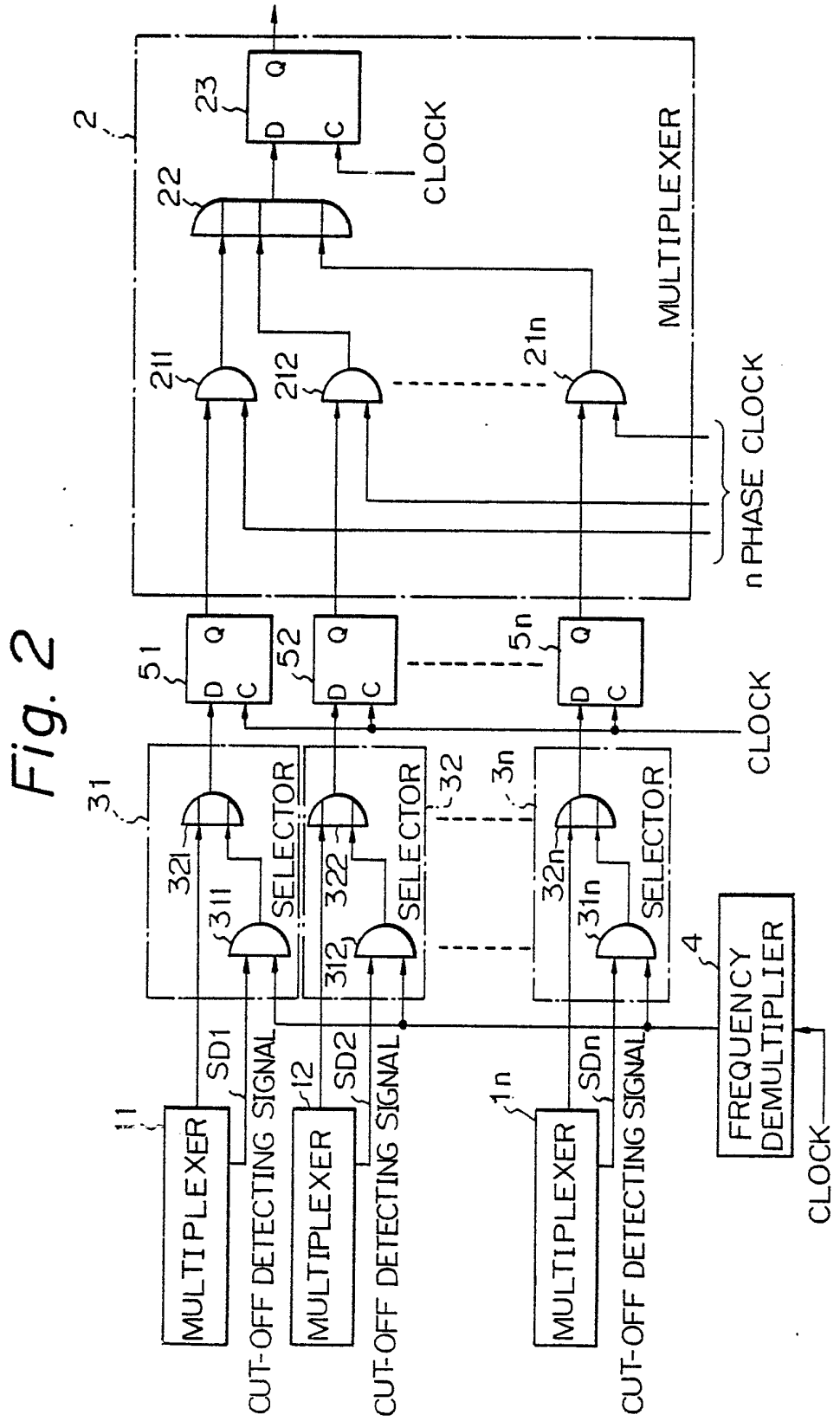
MULTIPLEXER

Fig. 2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212
21n
31
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Fig. 3

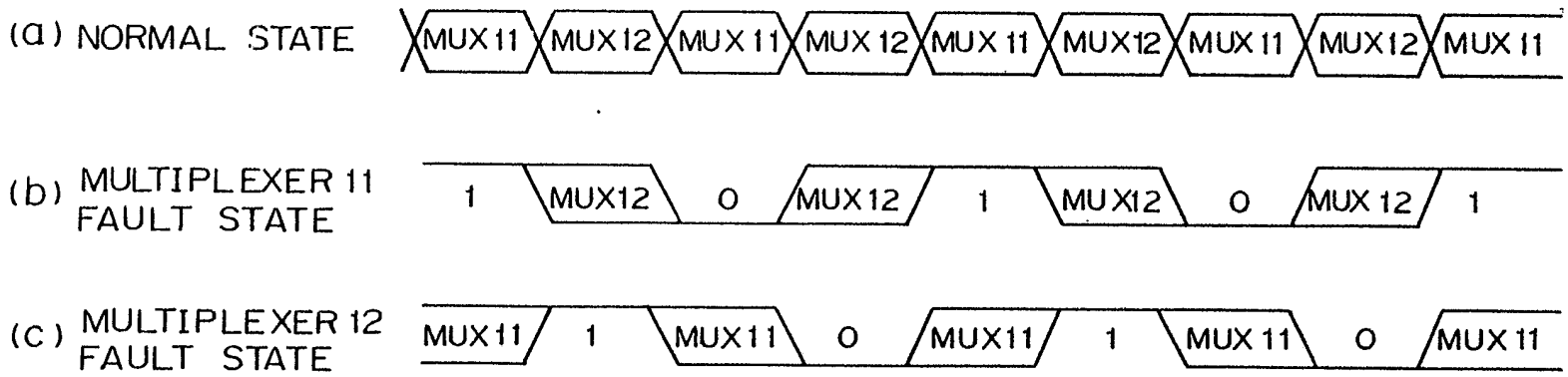
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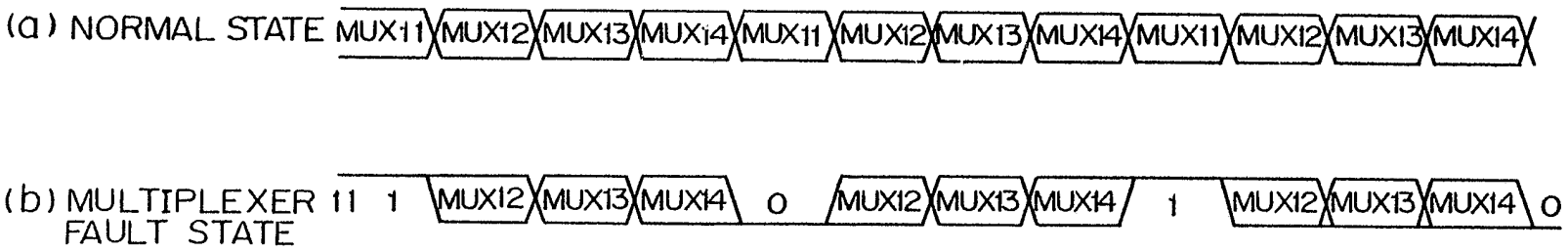
Fig. 4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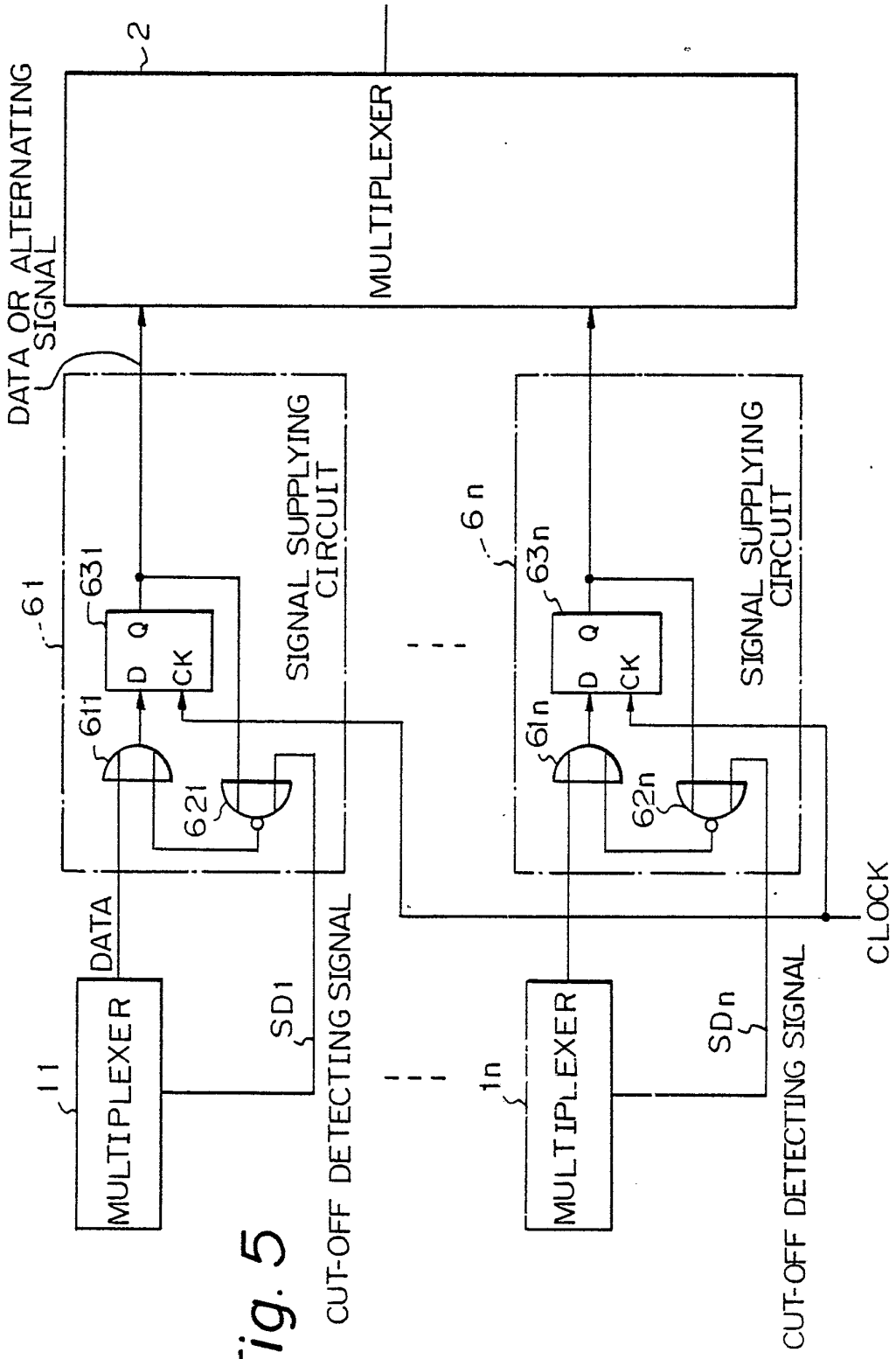
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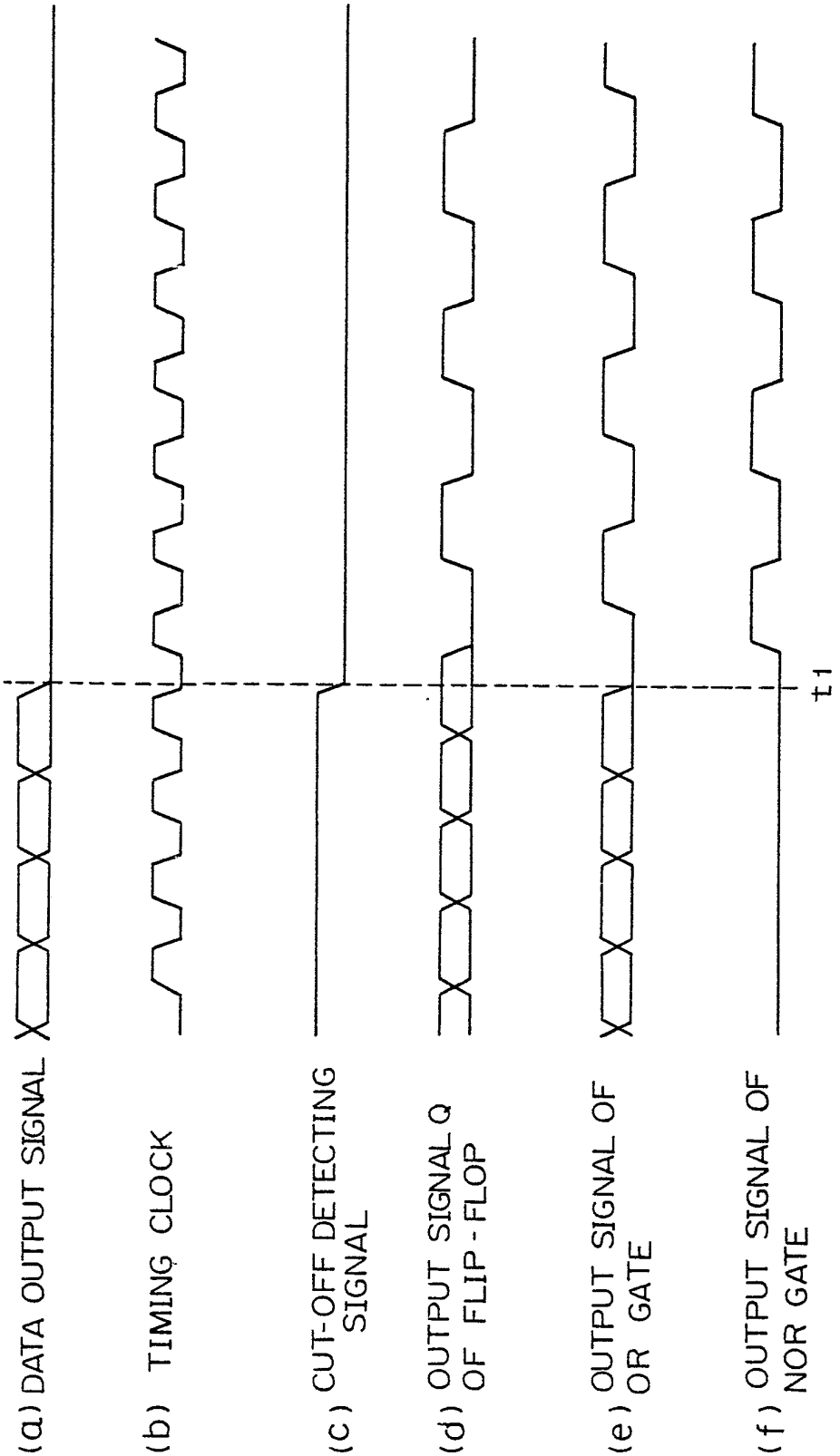
Fig. 5

Fig. 6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(d) OUTPUT SIGNAL Q OF FLIP-FLOP
(e) OUTPUT SIGNAL OF OR GATE
(f) OUTPUT SIGNAL OF NOR GATE

Fig. 7

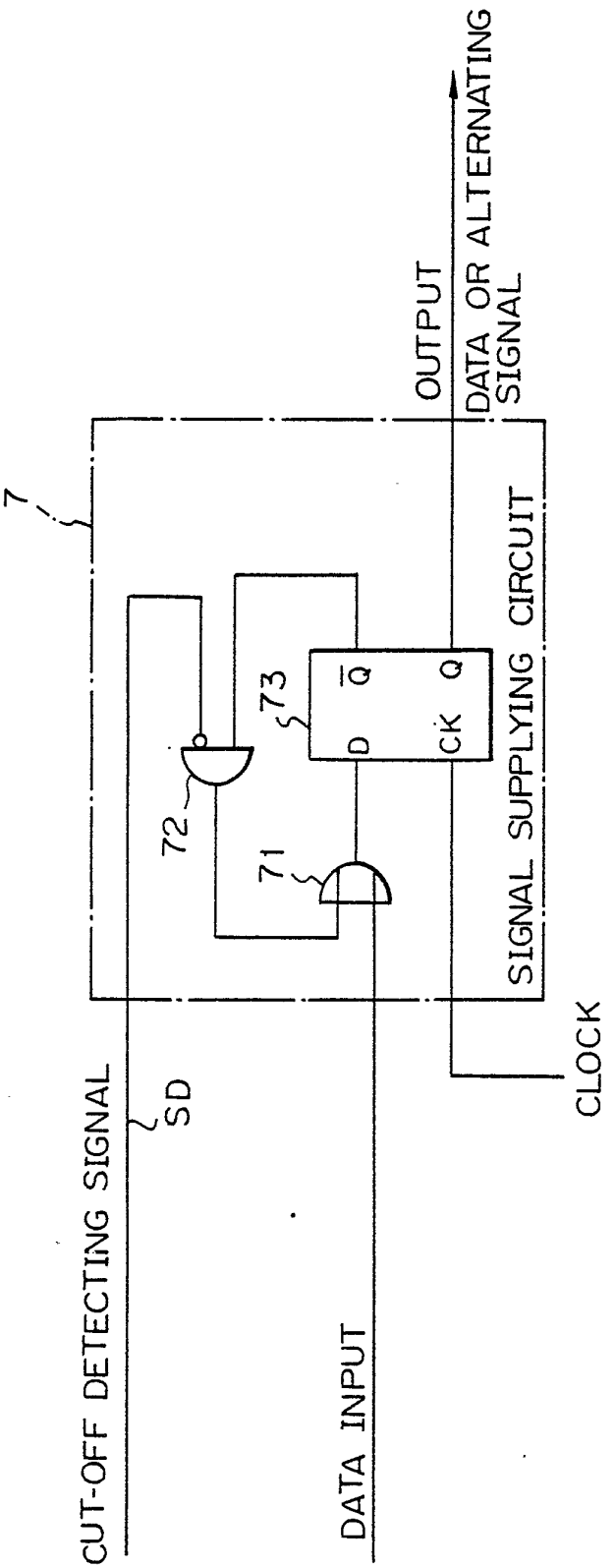
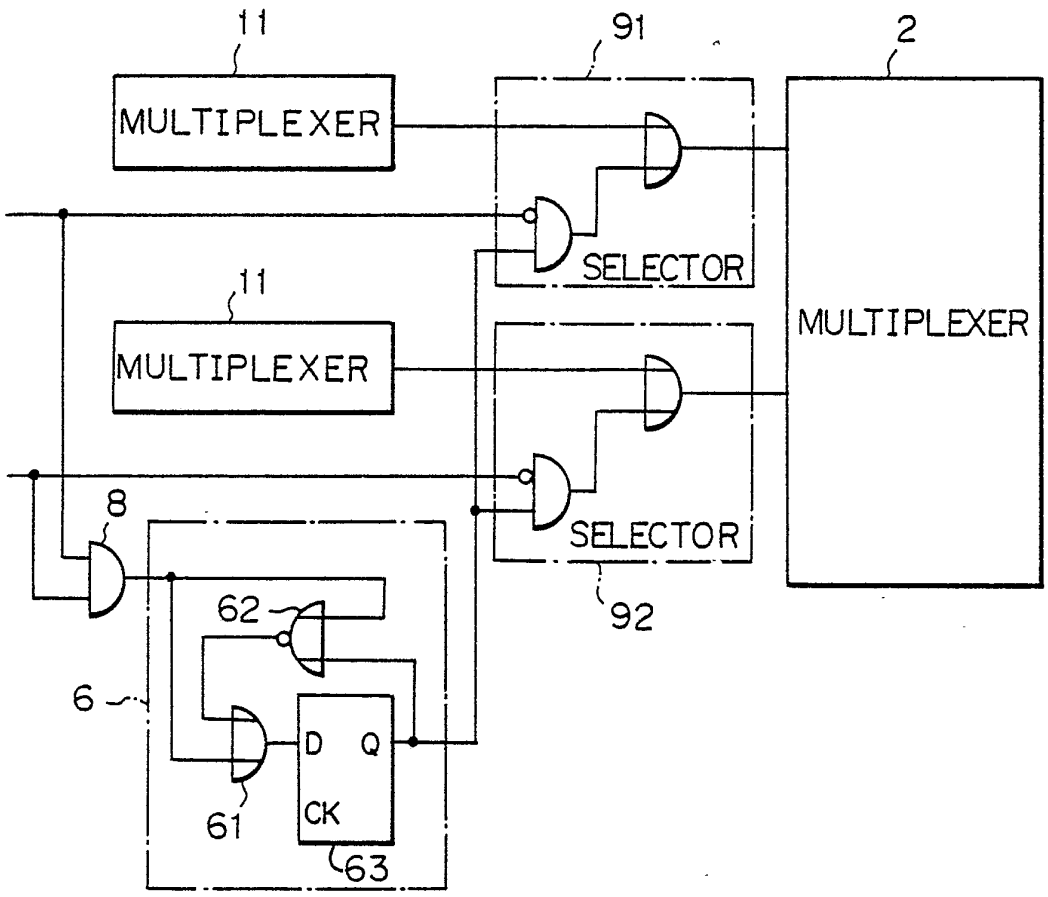

7
OUTPUT
DATA OR ALTERNATING SIGNAL
SIGNAL SUPPLYING CIRCUIT
73
Q̄
Q
D
CK
72
71
CUT-OFF DETECTING SIGNAL
SD
DATA INPUT
CLOCK

Fig. 8


11
MULTIPLEXER
91
2
SELECTOR
11
MULTIPLEXER
MULTIPLEXER
8
SELECTOR
92
62
6
D
Q
CK
61
63

INTERNATIONAL SEARCH REPORT

International Application No PCT/JP 86/00148

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 04 J 3/04

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 04 J H 04 B

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	IEEE International Conference on Communications, 14-17 May 1984, New York, (US) Stevenson et al.:"A 280Mbit/s monomode optical trunk transmission system", pages 790-795, see page 791, right-hand column, lines 1-35	1,6
A		2
	--	
Y	FR, A, 2295650 (SIEMENS) 16 July 1976, see page 2, lines 11-20	1,6
A		2,4
	--	
A	Elektronik, volume 31, no. 22, November 1982, München, (DE) Marten:"Optische Sender mit Halbleiterlasern für hohe Bitraten", pages 89-94, see page 92, right-hand column, line 38 - page 93, left-hand column, line 32	1,6
	-----	

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
27th May 1986	23 JUIN 1986
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	L. ROSSI

Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/JP 86/00148 (SA 12679)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 06/06/86

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
FR-A- 2295650	16/07/76	BE-A-	836880	16/04/76
		LU-A-	73830	11/06/76
		NL-A-	7514830	22/06/76
		DE-A-	2460234	24/06/76
		GB-A-	1528900	18/10/78
		JP-A-	51088118	02/08/76