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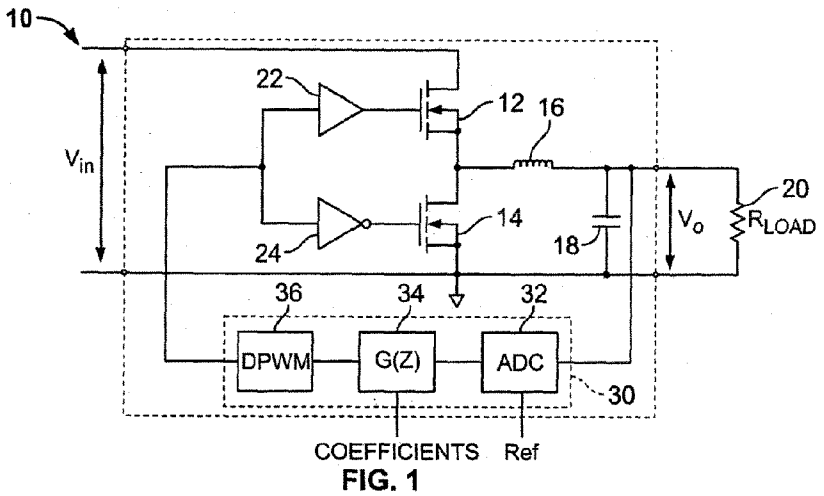

FIG. 1

(57) Abstract: A method and system for optimizing the digital filter compensation coefficients of a digitally controlled switched mode power supply within a distributed power system is disclosed A power control system comprises at least one point-of-load (POL) regulator having a power conversion circuit adapted to convey power to a load and a digital controller coupled to the power conversion circuit though a feedback loop The digital controller includes a digital filter having a transfer function defined by plural filter coefficients The digital controller periodically stores samples of the feedback measurement The system controller retrieves stored samples from the digital controller via a seπal data bus After retπeving a pre-determined number of the samples, the system controller calculates optimized filter coefficients for the digital filter and communicates the optimized filter coefficients to the digital controller for use in the digital filter

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METHOD AND SYSTEM FOR OPTIMIZING FILTER COMPENSATION COEFFICIENTS FOR A DIGITAL POWER CONTROL SYSTEM

RELATED APPLICATION DATA

This patent application claims priority as a continuation-in-part pursuant to 35 U.S.C. § 120 to patent application Serial No. 10/889,806, filed July 12, 2004, issued as U.S. Patent No. 7,249,267 on July 24, 2007, which claimed priority pursuant to 35 U.S.C. § 119(c) to provisional patent application Serial No. 60/544,553, filed February 12, 2004, and also claimed priority as a continuation-in-part pursuant to 35 U.S.C. § 120 to patent applications Serial No. 10/361,667, filed February 10, 2003, and Serial No. 10/326,222, filed December 21, 2002.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to power supply circuits, and more particularly to digital power control systems and methods for optimizing and programming filter compensation coefficients of switched mode power supply circuits.

2. Description of Related Art

Switched mode power supplies are known in the art to convert an available direct current (DC) or alternating current (AC) level voltage to another DC level voltage. A buck converter is one particular type of switched mode power supply that provides a regulated DC output voltage to a load by selectively storing energy in an output inductor coupled to the load by switching the flow of current into the output inductor. It includes two power switches that are typically provided by MOSFET transistors. A filter capacitor coupled in parallel with the load reduces ripple of the output current. A pulse width modulation (PWM) control circuit is used to control the gating of the power switches in an alternating manner to control the flow of current in the output inductor. The PWM control circuit uses

signals communicated via a feedback loop reflecting the output voltage and/or current level to adjust the duty cycle applied to the power switches in response to changing load conditions.

Conventional PWM control circuits are constructed using analog circuit components, such as operational amplifiers, comparators and passive components like resistors and capacitors for loop compensation, and some digital circuit components like logic gates and flip-flops. But, it is desirable to use entirely digital circuitry instead of the analog circuit components since digital circuitry takes up less physical space, draws less power, and allows the implementation of programmability features or adaptive control techniques.

A conventional digital control circuit includes an analog-to-digital converter (ADC) that converts an error signal representing the difference between a signal to be controlled (e.g., output voltage (V_o)) and a reference into a digital signal having n bits. The digital control circuit uses the digital error signal to control a digital pulse width modulator, which provides control signals to the power switches having a duty cycle such that the output value of the power supply tracks the reference. The digital control circuit may further include a digital filter, such as an infinite impulse response (IIR) filter having an associated transfer function. The transfer function includes compensation coefficients that define the operation of the IIR filter. It is desirable to have the ability to alter or program these compensation coefficients in order to optimize the operation of the digital filter for particular load conditions.

Since electronic systems frequently need power provided at several different discrete voltage and current levels, it is known to distribute an intermediate bus voltage throughout the electronic system, and include an individual point-of-load ("POL") regulator, e.g., a switched mode DC/DC converter, at the point of power consumption within the electronic system. Particularly, a POL regulator would be included with each respective electronic circuit to convert the intermediate bus voltage to the level required by the electronic circuit. An electronic system may include multiple POL regulators to convert the intermediate bus voltage into each of the multiple voltage levels. Ideally, the POL regulator

would be physically located adjacent to the corresponding electronic circuit so as to minimize the length of the low voltage, high current lines through the electronic system. The intermediate bus voltage can be delivered to the multiple POL regulators using low current lines that minimize loss.

With this distributed approach, there is a need to coordinate the control and monitoring of the POL regulators of the power system. The POL regulators generally operate in conjunction with a power supply controller that activates, programs, and monitors the individual POL regulators. It is known in the art for the controller to use a multi-connection parallel bus to activate and program each POL regulator. For example, the parallel bus may communicate an enable/disable bit for turning each POL regulator on and off, and voltage identification (VID) code bits for programming the output voltage set-point of the POL regulators. The controller may further use additional connections to monitor the voltage/current that is delivered by each POL regulator so as to detect fault conditions of the POL regulators. A drawback with such a control system is that it adds complexity and size to the overall electronic system.

Thus, it would be advantageous to provide a system and method for digitally controlling a switched mode power supply that overcomes these and other drawbacks of the prior art. It would further be advantageous to provide a system and method for controlling and monitoring the operation of a digitally controlled switched mode power supply within a distributed power system. More particularly, it would be advantageous to provide a system and method for optimizing the digital filter compensation coefficients of a digitally controlled switched mode power supply within a distributed power system.

SUMMARY OF THE INVENTION

The present invention overcomes the drawbacks of the prior art to provide a system and method for optimizing the digital filter compensation coefficients of a digitally controlled switched mode power supply within a distributed power system.

In an embodiment of the invention, a power control system comprises at least one point-of-load (POL) regulator having a power conversion circuit adapted

to convey power to a load and a digital controller coupled to the power conversion circuit trhough a feedback loop. The digital controller is adapted to provide a pulse width modulated control signal to the power conversion circuit responsive to a feedback measurement of an output of the power conversion circuit. The digital controller further comprises a digital filter having a transfer function defined by plural filter coefficients. The digital controller periodically stores a successive one of a plurality of samples of the feedback measurement. A serial data bus operatively connects the POL regulator to a system controller. The system controller retrieves each successive stored sample from the digital controller via the serial data bus. After retrieving a pre-determined number of the samples, the system controller calculates optimized filter coefficients for the digital filter and communicates the optimized filter coefficients to the digital controller. The digital controller thereafter uses the optimized filter coefficients in the digital filter.

More particularly, the digital controller further includes a noise source adapted to periodically inject a symmetrical noise signal into the pulse width modulated control signal. The symmetrical noise signal may be provided by a pseudo-random binary sequence. The pre-determined number of samples relates to a sequence length of the pseudo-random binary sequence. The digital controller further includes a register adapted to store the successive samples of the feedback measurement. The system controller includes a memory array adapted to store the samples retrieved from the digital controller. The system controller calculates a transfer function of the feedback loop based on the samples retrieved from the digital controller. The system controller thereby calculates the optimized filter coefficients based on the calculated transfer function.

A more complete understanding of the system and method of optimizing filter coefficients for a digital power control system will be afforded to those skilled in the art, as well as a realization of additional advantages and objects thereof, by a consideration of the following detailed description of the preferred embodiment. Reference will be made to the appended sheets of drawings, which will first be described briefly.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 depicts a switched mode power supply having a digital control circuit;

Fig. 2 depicts a windowed flash ADC that provides high and low saturation signals;

Fig. 3 depicts a digital controller having an infinite impulse response filter and error controller;

Fig. 4 depicts an exemplary control system for communicating filter compensation coefficients in accordance with an embodiment of the present invention;

Fig. 5 depicts an exemplary POL regulator of the POL control system;

Fig. 6 depicts an exemplary system controller of the POL control system;

Fig. 7 is an exemplary screen shot depicting a graphical user interface (GUI) for simulating operation of a POL regulator;

Fig. 8 is an exemplary screen shot depicting a GUI for programming the compensation coefficients of the digital controller;

Fig. 9 depicts an exemplary POL regulator of the POL control system in accordance with an alternative embodiment of the invention;

Fig. 10 is a schematic diagram illustrating interactions between an exemplary POL regulator and an exemplary system controller in accordance with the alternative embodiment of the invention;

Fig. 11 is a flow chart illustrating interactions between an exemplary POL regulator and an exemplary system controller in accordance with the alternative embodiment of the invention; and

Fig. 12 is a block diagram illustrating a structure of an output voltage feedback loop within a digital controller in accordance with the alternative embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention provides a method for digitally controlling a switched mode power supply. More particularly, the invention provides a system and method for optimizing and programming the digital filter compensation coefficients

of a digitally controlled switched mode power supply within a distributed power system. In the detailed description that follows, like element numerals are used to describe like elements illustrated in one or more figures.

Fig. 1 depicts an exemplary switched mode power supply 10 having a digital control circuit in accordance with an embodiment of the present invention. The power supply 10 comprises a buck converter topology to convert an input DC voltage V_{in} to an output DC voltage V_o applied to a resistive load 20 (R_{load}). The power supply 10 includes a pair of power switches 12, 14 provided by MOSFET devices. The drain terminal of the high side power switch 12 is coupled to the input voltage V_{in}, the source terminal of the low side power switch 14 is connected to ground, and the source terminal of the high side power switch 12 and the drain terminal of the low side power switch 14 are coupled together to define a phase node. An output inductor 16 is coupled in series between the phase node and the terminal providing the output voltage V_o, and a capacitor 18 is coupled in parallel with the resistive load R_{load}. Respective drivers 22, 24 alternatingly drive the gate terminals of the power switches 12, 14. In turn, the drivers 22, 24 are controlled by a digital control circuit 30 (described below). The opening and closing of the power switches 12, 14 provides an intermediate voltage having a generally rectangular waveform at the phase node, and the filter formed by the output inductor 16 and capacitor 18 converts the rectangular waveform into a substantially DC output voltage V_o.

The digital control circuit 30 receives a feedback signal from the output portion of the power supply 10. As shown in Fig. 1, the feedback signal corresponds to the output voltage V_o, though it should be appreciated that the feedback signal could alternatively (or additionally) correspond to the output current drawn by the resistive load R_{load} or any other signal representing a parameter to be controlled by the digital control circuit 30. The feedback path may further include a voltage divider (not shown) to reduce the detected output voltage V_o to a representative voltage level. The digital control circuit 30 provides a pulse width modulated waveform having a duty cycle controlled to regulate the output voltage V_o (or output current) at a desired level. Even though the exemplary

power supply 10 is illustrated as having a buck converter topology, it should be understood that the use of feedback loop control of the power supply 10 using the digital control circuit 30 is equally applicable to other known power supply topologies, such as boost and buck-boost converters in both isolated and non-isolated configurations, and to different control strategies known as voltage mode, current mode, charge mode and/or average current mode controllers.

More particularly, the digital control circuit 30 includes analog-to-digital converter (ADC) 32, digital controller 34, and digital pulse width modulator (DPWM) 36. The ADC 32 further comprises a windowed flash ADC that receives as inputs the feedback signal (i.e., output voltage V_o) and a voltage reference (Ref) and produces a digital voltage error signal (VEd_k) representing the difference between the inputs (Ref - V_o). The digital controller 34 has a transfer function G(z) that transforms the voltage error signal VEd_k to a digital output provided to the DPWM 36, which converts the signal into a waveform having a proportional pulse width (PWM_k). The digital controller 34 receives as inputs filter compensation coefficients used in the transfer function G(z), as will be further described below. As discussed above, the pulse-modulated waveform PWM_k produced by the DPWM 36 is coupled to the gate terminals of the power switches 12, 14 through the respective drivers 22, 24.

Fig. 2 depicts an exemplary windowed flash ADC 40 for use in the digital control circuit 30. The ADC 40 receives as inputs the voltage reference Ref and the output voltage V_o. The voltage reference is applied to the center of a resistor ladder that includes resistors 42A, 42B, 42C, 42D connected in series between the reference voltage terminal and a current source connected to a positive supply voltage (V_{DD}), and resistors 44A, 44B, 44C, 44D connected in series between the reference voltage terminal and a current source connected to ground. The resistors each have corresponding resistance values to define together with the current sources a plurality of voltage increments ranging above and below the voltage reference Ref. The magnitude of the resistance values and/or current sources can be selected to define the LSB resolution of the ADC 40. An array of comparators is connected to the resistor ladder, including a plurality of positive

side comparators 46A, 46B, 46C, 46D and a plurality of negative side comparators 48A, 48B, 48C, 48D. The positive side comparators 46A, 46B, 46C, 46D each have a non-inverting input terminal connected to the output voltage V_o, and an inverting input terminal connected to respective ones of the resistors 42A, 42B, 42C, 42D. Likewise, the negative side comparators 48A, 48B, 48C each have a non-inverting input terminal connected to the output voltage V_o, and an inverting input terminal connected to respective ones of the resistors 44A, 44B, 44C, 44D. Negative side comparator 48D has a non-inverting input terminal connected to ground and the inverting input terminal connected to the output voltage V_o. It should be appreciated that a greater number of resistors and comparators may be included to increase the number of voltage increments and hence the range of the ADC 40, and that a limited number of resistors and comparators is shown in Fig. 2 for exemplary purposes only.

The ADC 40 further includes a logic device 52 coupled to output terminals of comparators 46A, 46B, 46C and 48A, 48B, 48C. The logic device 52 receives the comparator outputs and provides a multi-bit (e.g., 4-bit) parallel output representing the voltage error VEd_k. By way of example, an output voltage V_o that exceeds the reference voltage Ref by one voltage increment (e.g., 5 mV) would cause the outputs of comparators 46B, 46A, 48A, 48B, and 48C to go high, while the outputs of comparators 46C, 46D and 48D remain low. The logic device 52 would interpret this as logic level 9 (or binary 1001) and produce an associated voltage error signal VEd_k. It should be understood that the voltage reference Ref is variable so as to shift the window of the ADC 40. If the output voltage V_o exceeds the highest voltage increment of the resistor ladder, the output terminal of comparator 46D provides a HIGH saturation signal. Similarly, if the output voltage V_o is lower than the lowest voltage increment of the resistor ladder, the output terminal of comparator 48D provides a LOW saturation signal.

In Fig. 3, a digital controller having a digital filter and ADC 40 is depicted. The digital filter further comprises an infinite impulse response (IIR) filter that produces an output PWM'_k from previous voltage error inputs VEd_k and previous outputs PWM'_k. As discussed above, ADC 40 provides the voltage error inputs

VEd_k. The digital filter outputs PWM'_k are provided to the digital pulse width modulator (DPWM) 36, which provides the pulse width modulated control signal (PWM_k) to the power supply power switches.

The IIR filter is illustrated in block diagram form and includes a first plurality of delay registers 72, 74, ..., 76 (each labeled z^{-1}), a first plurality of mathematical operators (multipliers) with coefficients 71, 73, ..., 77 (labeled C0, C1, ..., Cn), a second plurality of mathematical operators (adders) 92, 94, 96, a second plurality of delay registers 82, 84, ..., 86 (each labeled z^{-1}), and a third plurality of mathematical operators (multipliers) with coefficients 83, 87 (labeled B1, ..., Bn). Each of the first delay registers 72, 74, 76 holds a previous sample of the voltage error VEd_k, which is then weighted by a respective one of the coefficients 71, 73, 77. Likewise, each of the second delay registers 82, 84, 86 holds a previous sample of the output PWM'_k, which is then weighted by a respective one of the coefficients 83, 87. The adders 92, 94, and 96 combine the weighted input and output samples. It should be appreciated that a greater number of delay registers and coefficients may be included in the IIR filter, and that a limited number is shown in Fig. 3 for exemplary purposes only. The digital filter structure shown in Fig. 3 is an exemplary implementation of the following transfer function G(z):

$$G(z) = \frac{PWM(z)}{VEd(z)} = \frac{C_0 + C_1 \cdot z^{-1} + C_2 \cdot z^{-2} + ... + C_n \cdot z^{-n}}{1 - B_1 \cdot z^{-1} - B_2 \cdot z^{-2} - ... - B_n \cdot z^{-n}}$$

The error controller 62 receives a plurality of input signals reflecting error conditions of the ADC 40 and the digital filter. Specifically, the error controller 62 receives the HIGH and LOW saturation signals from the ADC 40 reflecting that the output voltage V_o is above and below the voltage window of the ADC, respectively. Each of the mathematical operators (adders) 92, 94, 96 provides an overflow signal to the error controller 62 reflecting an overflow condition (i.e., carry bit) of the mathematical operators. The digital filter further includes a range limiter 81 that clips the output PWM'_k if upper or lower range limits are reached. In that situation, the range limiter 81 provides the error controller 62 with a corresponding limit signal.

The error controller 62 uses these input signals to alter the operation of the digital filter in order to improve the responsiveness of the digital filter to changing load conditions. The error controller 62 is coupled to each of the first plurality of delay registers 72, 74, 76 and second plurality of delay registers 82, 84, 86 to enable the resetting and/or presetting of the value stored therein. As used herein, "resetting" refers to the setting of the value to an initial value (e.g., zero), whereas "presetting" refers to the setting of the value to another predetermined number. Particularly, the error controller 62 can replace the previous samples of the voltage error VEd_k and output PWM'_k with predetermined values that change the behavior of the power supply. The error controller 62 receives as external inputs data values to be used as coefficients 71, 73, ..., 77 and 83, ..., 87. It should be appreciated that the characteristics of the digital filter can be programmed by selection of appropriate data values for the coefficients 71, 73, ..., 77 and 83, ..., 87.

The digital controller further includes multiplexer 64 that enables selection between the PWM'_k output signal and a predetermined output signal provided by the error controller 62. A select signal provided by the error controller 62 determines which signal passes through the multiplexer 64. When the ADC 40 goes into HIGH or LOW saturation, the error controller 62 sets the PWM'_k signal to a specific predetermined value (or sequence of values that are dependent in part on the previous samples) by controlling the multiplexer 64. In order to recover smoothly from such a condition, the error controller can also alter the delayed input and output samples by reloading the first plurality of delay registers 72, 74, 76, and second plurality of delay registers 82, 84, 86. This will assure a controlled behavior of the feedback loop as the ADC 40 recovers from saturation.

By way of example, if the ADC 40 experiences a positive saturation, i.e., the LOW signal changing from a low state to a high state, the PWM'_k sample can be reset to zero to help to reduce the error. By resetting the PWM'_k sample to zero, the pulse width delivered to the high side power switch 12 of the power supply 10 goes to zero, effectively shutting off power to the resistive load 20 (see Fig. 1). In order to recover from this situation smoothly, the samples PWM'_{k-1},

PWM'_{k-2}, ..., PWM'_{k-n} can also be reset to zero or preset to another value in order to allow a smooth recovery. Likewise, if the ADC 40 experiences a negative saturation, i.e., the HIGH signal changing from a low state to a high state, the PWM'_k sample can be preset to a maximum value to increase the pulse width delivered to the high side power switch 12 to reduce the error. Also, when an internal numeric overflow of the digital filter occurs, the error controller 62 can take actions to prevent uncontrolled command of the power switches of the power supply, such as altering the input and output samples of the digital filters.

In an embodiment of the invention, the switched mode power supply of Fig. 1 further comprises a point-of-load ("POL") regulator located at the point of power consumption within the electronic system. A power control system includes a plurality of like POL regulators, at least one data bus operatively connecting the plurality of POL regulators, and a system controller connected to the data bus and adapted to send and receive digital data to and from the plurality of POL regulators. The system controller would communicate data over the serial bus in order to program the digital filter transfer function G(z) with the values of the coefficients 71, 73, ..., 77 and 83, ..., 87.

Referring now to Fig. 4, a POL control system 100 is shown in accordance with an embodiment of the present invention. Specifically, the POL control system 100 includes a system controller 102, a front-end regulator 104, and a plurality of POL regulators 106, 108, 110, 112, and 114 arranged in an array. The POL regulators depicted herein include, but are not limited to, point-of-load regulators, power-on-load regulators, DC/DC converters, voltage regulators, and all other programmable voltage or current regulating devices generally known to those skilled in the art. An intra-device interface is provided between individual ones of the POL regulators to control specific interactions, such as current share or paralleling, e.g., current share interface (CS1) provided between POL0 106 and POL1 108, and CS2 provided between POL4 112 and POLn 114. In the exemplary configuration shown in Fig. 4, POL0 106 and POL1 108 operate in parallel mode to produce output voltage V_{O1} with increased current capability, POL2 110 produces output voltage V_{O2}, and POL4 112 and POLn 114 operate in

parallel mode to produce output voltage V_{O3}, though it should be appreciate that other combinations and other numbers of POL regulators could be advantageously utilized.

The front-end regulator 104 provides an intermediate voltage to the plurality of POL regulators over an intermediate voltage bus, and may simply comprise another POL regulator. The system controller 102 and front-end regulator 104 may be integrated together in a single unit, or may be provided as separate devices. Alternatively, the front-end regulator 104 may provide a plurality of intermediate voltages to the POL regulators over a plurality of intermediate voltage buses. The system controller 102 may draw its power from the intermediate voltage bus.

The system controller 102 communicates with the plurality of POL regulators by writing and/or reading digital data (either synchronously or asynchronous) via a uni-directional or bi-directional serial bus, illustrated in Fig. 4 as the synch/data bus. The synch/data bus may comprise a two-wire serial bus (e.g., I^2C) that allows data to be transmitted asynchronously or a single-wire serial bus that allows data to be transmitted synchronously (i.e., synchronized to a clock signal). In order to address any specific POL in the array, each POL is identified with a unique address, which may be hardwired into the POL or set by other methods. For example, the system controller 102 communicates data over the synch/data bus to program the digital filter transfer function G(z) coefficients of each POL regulator. The system controller 102 also communicates with the plurality of POL regulators for fault management over a second uni-directional or bi-directional serial bus, illustrated in Fig. 4 as the OK/fault bus. By grouping plural POL regulators together by connecting them to a common OK/fault bus allows the POL regulators have the same behavior in the case of a fault condition. Also, the system controller 102 communicates with a user system via a user interface bus for programming, setting, and monitoring of the POL control system 10. Lastly, the system controller 102 communicates with the front-end regulator 104 over a separate line to disable operation of the front-end regulator.

An exemplary POL regulator 106 of the POL control system 10 is illustrated in greater detail in Fig. 5. The other POL regulators of Fig. 4 have substantially identical configuration. The POL regulator 106 includes a power conversion circuit 142 (e.g., the switched mode power supply 10 of Fig. 1), a serial interface 144, a POL controller 146, default configuration memory 148, and hardwired settings interface 150. The power conversion circuit 142 transforms an input voltage (V_I) to the desired output voltage (V_O) according to settings received through the serial interface 144, the hardwired settings 150 or default settings. The power conversion circuit 142 may also include monitoring sensors for output voltage, current, temperature and other parameters that are used for local control and also communicated back to the system controller through the serial interface 144. The power conversion circuit 142 may also generate a Power Good (PG) output signal for stand-alone applications in order to provide a simplified monitoring function. The serial interface 144 receives and sends commands and messages to the system controller 102 via the synch/data and OK/fault serial buses. The default configuration memory 148 stores the default configuration for the POL regulator 106 in cases where no programming signals are received through the serial interface 144 or hardwired settings interface 150. The default configuration is selected such that the POL regulator 106 will operate in a "safe" condition in the absence of programming signals.

The hardwired settings interface 150 communicates with external connections to program the POL regulator without using the serial interface 144. The hardwired settings interface 150 may include as inputs the address setting (Addr) of the POL to alter or set some of the settings as a function of the address (i.e., the identifier of the POL), e.g., phase displacement, enable/disable bit (En), trim, VID code bits, and selecting different (pre-defined) sets of digital filter coefficients optimized for different output filter configurations. Further, the address identifies the POL regulator during communication operations through the serial interface 144. The trim input allows the connection of one or more external resistors to define an output voltage level for the POL regulator. Similarly, the VID code bits can be used to program the POL regulator for a desired output

voltage/current level. The enable/disable bit allows the POL regulator to be turned on/off by toggling a digital high/low signal.

The POL controller 146 receives and prioritizes the settings of the POL regulator. If no settings information is received via either the hardwired settings interface 150 or the serial interface 144, the POL controller 146 accesses the parameters stored in the default configuration memory 148. Alternatively, if settings information is received via the hardwired settings interface 150, then the POL controller 146 will apply those parameters. Thus, the default settings apply to all of the parameters that cannot be or are not set through hard wiring. The settings received by the hardwired settings interface 150 can be overwritten by information received via the serial interface 144. The POL regulator can therefore operate in a stand-alone mode, a fully programmable mode, or a combination thereof. This programming flexibility enables a plurality of different power applications to be satisfied with a single generic POL regulator, thereby reducing the cost and simplifying the manufacture of POL regulators.

By way of example, the system controller 102 communicates data values to a particular POL regulator 106 via the synch/data bus for programming the digital filter coefficients. The data values are received by the serial interface 144 and communicated to the POL controller 146. The POL controller then communicates the data values to the power conversion circuit 142 along with suitable instructions to program the digital filter coefficients.

An exemplary system controller 102 of the POL control system 100 is illustrated in Fig. 6. The system controller 102 includes a user interface 122, a POL interface 124, a controller 126, and a memory 128. The user interface 122 sends and receives messages to/from the user via the user interface bus. The user interface bus may be provided by a serial or parallel bi-directional interface using standard interface protocols, e.g., an I^2C interface. User information such as monitoring values or new system settings would be transmitted through the user interface 122. The POL interface 124 transforms data to/from the POL regulators via the synch/data and OK/fault serial buses. The POL interface 124 communicates over the synch/data serial bus to transmit setting data and receive

monitoring data, and communicates over the OK/fault serial bus to receive interrupt signals indicating a fault condition in at least one of the connected POL regulators. The memory 128 comprises a non-volatile memory storage device used to store the system set-up parameters (e.g., output voltage, current limitation set-point, timing data, etc.) for the POL regulators connected to the system controller 102. Optionally, a secondary, external memory 132 may also be connected to the user interface 122 to provide increased memory capacity for monitoring data or setting data.

The controller 126 is operably connected to the user interface 122, the POL interface 124, and the memory 128. The controller 126 has an external port for communication a disable signal (FE DIS) to the front-end regulator 104. At start-up of the POL control system 100, the controller 126 reads from the internal memory 128 (and/or the external memory 132) the system settings and programs the POL regulators accordingly via the POL interface 124. Each of the POL regulators is then set up and started in a prescribed manner based on the system programming. During normal operation, the controller 126 decodes and executes any command or message coming from the user or the POL regulators. The controller 126 monitors the performance of the POL regulators and reports this information back to the user through the user interface 122. The POL regulators may also be programmed by the user through the controller 126 to execute specific, autonomous reactions to faults, such as over current or over voltage conditions. Alternatively, the POL regulators may be programmed to only report fault conditions to the system controller 102, which will then determine the appropriate corrective action in accordance with predefined settings, e.g., shut down the front-end regulator via the FE DIS control line.

A monitoring block 130 may optionally be provided to monitor the state of one or more voltage or current levels of other power systems not operably connected to the controller 102 via the synch/data or OK/fault buses. The monitoring block 130 may provide this information to the controller 126 for reporting to the user through the user interface in the same manner as other information concerning the POL control system 10. This way, the POL control

system 10 can provide some backward compatibility with power systems that are already present in an electronic system.

As discussed above, the system controller 102 has an interface for communicating with a user system for programming and monitoring performance of the POL control system. The user system would include a computer coupled to the interface, either directly or through a network, having suitable software adapted to communicate with the system controller 102. As known in the art, the computer would be equipped with a graphics-based user interface (GUI) that incorporates movable windows, icons and a mouse, such as based on the Microsoft Windows™ interface. The GUI may include standard preprogrammed formats for representing text and graphics, as generally understood in the art. Information received from the system controller 102 is displayed on the computer screen by the GUI, and the user can program and monitor the operation of the POL control system by making changes on the particular screens of the GUI.

Fig. 7 illustrates an exemplary screen shot of a GUI used for simulating operation of a POL regulator. The screen shot illustrates a POL regulator having a topology corresponding to the exemplary switched mode power supply 10 described above with respect to Fig. 1. The POL regulator includes a pair of power switches provided by MOSFET devices, an output inductor L_O, and a capacitor C_O 18. Output terminals of the POL regulator are coupled to a load resistance R_L through a pi-filter defined by a series inductance L_1 and internal resistance RL_1, capacitance C_1 and internal resistance RC_1 at a first end of the pi-filter, and capacitance C_2 and internal resistance RC_2 at a second end of the pi-filter. The POL regulator further includes a control circuit that provides a PWM drive signal to the power switches, and receives as feedback signals the output current IL_O and output voltage V_O. The output voltage may be sensed from either end of the transmission line by setting a switch.

The GUI permits a user to define values of various parameters of the POL regulator in order to simulate its operation. Each user definable parameter includes a field that permits a user to enter desired data values. The user can select parameters of the output voltages, such as by defining the voltage at the

first end of the pi-filter V_1, the voltage at the second end of the pi-filter V_2, voltage delay, rise and fall times, and power switch drive pulse width and period. The user can also select load distribution parameters, including defining the resistances, capacitances and inductance of the pi-filter. The user can also define the load resistance and load current characteristics.

Once the user has selected desired parameters for the POL regulator, the GUI can run a simulation based on the selected parameters. Fig. 8 illustrates an exemplary screen shot of a GUI in which the transfer function G(z) for the POL regulator is shown graphically. The transfer function is illustrated graphically in terms of variations of gain magnitude and phase with respect to frequency. As part of the simulation, the filter coefficients are calculated for the digital filter of the digital PWM and displayed on the screen. The user can alter the shape of the gain plots using slide potentiometers that adjust the poles and zeros of the transfer function, and can repeat the simulation of the POL regulator until satisfied with the performance results. The user can then opt to apply the selected digital filter coefficients to an individual POL regulator or group of POL regulators or all groups of POL regulators on a particular printed circuit board by selection of an appropriate button. This action would cause the selected filter coefficients to be stored in non-volatile memory contained within the system controller 102, and in turn communicated to each appropriate POL regulator via the synch/data bus as discussed above.

In an alternative embodiment of the invention, optimal filter coefficients could be obtained using an in-circuit network analyzer. The network analyzer could be adapted to measure the open loop transfer function of the POL regulator main voltage feedback loop, and then calculate the filter coefficients based on this measurement. This allows the feedback loop to be optimized for the actual load conditions rather than estimating the filter coefficients based on circuit simulations. More particularly, the POL regulator may be provided with a circuit to inject a noise component into the pulse width modulated control signal (PWM_k) used to drive the power switches. The resulting error value may then be periodically sampled and communicated to the system controller (or user system) through the

synch/data bus, which would then calculate the loop transfer function and the optimal filter coefficients. The system controller may then communicate the filter coefficients back to the POL regulator for programming the digital filter, as discussed above.

Fig. 9 illustrates an exemplary POL regulator 200 of the POL control system that implements a noise injection and sampling system. The POL regulator 200 includes a power conversion circuit 230 and a feedback loop including analog-to-digital converter (ADC) 232, digital filter 234, and digital pulse width modulator (DPWM) 236. The POL regulator 200 also includes a serial interface 244, a POL controller 246, default configuration memory 248, and hardwired settings interface 250. A subtractor 242 subtracts the output of the ADC 232 from a reference value supplied by the POL controller 246 in order to produce a voltage error signal (VEd_k). The function and operation of these systems are substantially as described above. The power conversion circuit 230 transforms an input voltage (V_i) to the desired output voltage (V_O) according to settings received through the serial interface 244, the hardwired settings 250 or default settings. The POL controller 246 may also generate a Power Good (PG) output signal for stand-alone applications in order to provide a simplified monitoring function.

The POL regulator 200 additionally includes a loop response detection circuit 220 coupled to the feedback loop. The loop response detection circuit 220 includes a noise source 222 that produces noise to be injected into the PWM_k control signal. In an embodiment of the invention, the noise source 222 produces a pseudo-random binary sequence (PRBS), although it should be appreciated that other symmetric noise signal sources could also be advantageously utilized. A summer 226 combines the PWM_k control signal with the noise signal, and provides the combined signal to the power conversion circuit 230. The loop response detection circuit 220 further includes a register 224 coupled to the output of the summer 242 in order to store a sample of the voltage error signal. The serial interface 244 is coupled to each of the noise source 222 and the register 224. The samples stored by the register 224 are periodically communicated to the

system controller via the serial interface 244 (as discussed in further detail below). Also, operational parameters of the noise source 220 can be programmed by the system controller through the serial interface 244.

Hence, for every PWM cycle, a single measurement of the loop error is recorded. Whenever the system controller retrieves this value from the register 224 through the serial interface 244, the noise source 222 is re-initialized. Then, the noise source 222 again injects noise into the PWM_k control signal and the loop error corresponding to that cycle is sampled and stored in the register 224 so that it can be read through the serial interface. Since the PRBS noise source is deterministic (i.e., repeatable), the loop error values will correspond to samples k, k+1, k+2, ... k+N, even though there was some amount of delay between adjacent samples and they were not directly contiguous.

The interleaved measurement of the loop response to the noise injection is illustrated in Fig. 10. A measurement cycle begins with initialization of a counter synchronously with the operation of the PRBS noise source 222. Then, a sample of the voltage error is taken and stored in the register 224 so that it can be communicated to the system controller through the serial interface 244. This is shown in Fig. 10 as the initial sample k being stored and then read out through the serial interface 244. Once the sample is taken, the noise source 222 can be temporarily stopped to minimize the exposure of the load to the noise. The system controller then retrieves the single loop error value through the serial bus, increments the counter for the next sample, and restarts the noise source 222, which now runs up to the k+1 sample. This cycle is repeated for N times, whereas N corresponds to the length of the PRBS sequence. Within each cycle, the noise source 222 may run for a period of time before a sample is taken to enable settling of the feedback loop. For example, the noise source 222 may run for a time period corresponding to sixty-three samples, with the sixty-fourth such sample being taken and stored in the register 224. Hence, this stored sample would have a data character as if the noise source 222 had been operating continuously. Over the course of N cycles, a sufficient number of samples would be taken to produce an accurate calculation of the loop gain.

More particularly, Fig. 11 provides a flow chart illustrating the loop gain measurement cycle from the perspective of the system controller as well as the POL regulator. The process begins at step 302 in which the POL regulator 200 communicates the current filter coefficients used by the digital filter 234 to the system controller. As discussed above, all communications between the POL regulator 200 and the system controller pass through the synch/data bus. The system controller receives the current digital filter coefficients at step 332. Then, at step 334, the system controller begins the loop gain measurement cycle (also referred to as a system identification (ID) cycle) and initializes a counter (k=0). The system controller communicates a signal to the POL regulator to instruct it to initiate the loop gain measurement cycle. At step 304, the POL regulator receives the initiation signal and sets the noise source amplitude to a selected level. The POL regulator also initializes a counter (k=0). Thereafter, processing loops are begun within both the system controller and the POL regulator.

At the POL regulator, the processing loop begins at step 306 in which the noise source 222 is reset and started. As discussed above, noise is injected into the PWM_k control signal. Meanwhile, the system controller executes step 346 in which it polls the POL regulator periodically to see if a sample is available. At step 308, the POL regulator will continue to operate the noise source 222 for a period of time to enable the feedback loop to settle. Prior to the k^{th} sample time, the POL regulator returns the answer NO to the system controller via step 312. This causes the system controller to loop back and repeat step 346. Eventually, at step 310, upon reaching the k^{th} sample time, a voltage error sample is stored in the register 224 and the POL regulator returns the answer YES to the system controller via step 312. Then, at step 314, the POL regulator sends the voltage error sample to the system controller, which retrieves the sample and stores it into a memory array at step 348. Thereafter, both the system controller and the POL regulator increments the counter (k=k+1) at steps 350, 316. If that sample was the last (i.e., N) sample, then both processing loops end at steps 318, 352. Otherwise, they return to the beginning of the processing loops to collect the next sample. Alternatively, the POL regulator could also mark the data sample as

being the last one. This way, the system controller wouldn't need to keep track of the counter k.

Once the system controller has collected all of the samples and loaded them into a memory array, at step 354, the system controller begins the process of calculating the open loop response as a function of the error samples and current digital filter coefficients. The open loop response is calculated by cross-correlating the noise and the loop response values, and transforming the result in the frequency domain using a Fourier transform. The system controller then calculates optimized digital filter coefficients based on the open loop response at step 356. The system control then communicates the optimized digital filter coefficients to the POL regulator, which receives and applies the digital filter coefficients to the digital filter at step 320. The system controller (or user) may periodically repeat this entire process to adapt the POL feedback loop to variations of the open loop response, such as due to aging of components, temperature induced variation of component performance, or load characteristic changes. Instead of calculating the open loop response, the system controller could calculate the transfer function of the power conversion circuit 230 followed by a calculation of the optimized controller.

An advantage of the foregoing method is that the POL regulator does not have to include a large capacity memory array for retaining all the samples or an arithmetic processing capability to calculate the open loop gain and digital filter coefficients. This minimizes the complexity and cost of the POL regulator. Instead, the additional memory and processing capability can be located at the system controller (or the user) end, where it can provide digital filter coefficient optimizations for all POL regulators of a power control system.

Referring now to Fig. 12, an exemplary process for calculating the open loop gain of the output voltage feedback loop is described. In a digital implementation of the output voltage feedback loop, the transfer function G(z) is fully deterministic and described by its z-transform with the filter coefficients. The output of G(z) is the duty cycle that is applied to the power conversion circuit. As

described above, the loop gain is measured by injecting some PWM noise u and measuring the loop error value e. The transfer function corresponds to:

$$T(z) = \frac{e(z)}{u(z)} = -\frac{k_{ADC} \cdot z^{-1} \cdot H(z)}{1 + k_{ADC} \cdot z^{-1} \cdot G(z) \cdot H(z)}$$

The loop gain is defined as:

$$LG(z) = k_{ADC} \cdot z^{-1} \cdot G(z) \cdot H(z)$$

When T(z) is measured and identified, the loop gain can be calculated together with the known controller transfer function G(z) according to:

$$LG(z) = -\frac{T(z) \cdot G(z)}{1 + T(z) \cdot G(z)}$$

The ADC scaling factor could be, for example:

$$k_{ADC} = \frac{1}{5mV} = 200V^{-1}$$

In a preferred embodiment of the invention, the noise injected into the feedback has a white notes characteristic. A pseudo random binary sequence (PRBS) approximates white noise. It has the additional advantage that its amplitude is bound, and even though it is close to white noise, the noise is fully deterministic and therefore doesn't need to be measured (i.e., it can be predicted). The PRBS may be generated using a shift register having a length selected such that the sequence generates noise in a frequency band of interest. The maximum frequency is given by the switching frequency ($F_s/2$), the minimum frequency by the length of the binary sequence (F_s/N). For example, for a nine bit length and a switching frequency of 500 kHz, the noise bandwidth is:

$$F_{NOISE} = \frac{1}{N \cdot T_S} \ldots \frac{1}{2 \cdot T_S} = 978Hz \ldots 250kHz$$

The sequence length is:

$$N = 2^n - 1 = 511$$

The noise injected into the PWM signal has the amplitude ±u.

Since the injected noise signal is pseudo-white noise, the cross correlation function r_{ue} corresponds to the impulse response of the measured system:

$$\hat{r}_{ue}(k) = \frac{1}{|u|^2} \cdot \sum_{n=0}^{N-1} u(n) \cdot e(k+n)$$

A further advantage of using a PRBS as the noise source is that the noise repeats after N cycles and therefore an average of the cross-correlation function over M complete sequences can be taken to minimize quantization and loop noise effects in the measured samples, as shown by:

$$\overline{\hat{r}_{ue}(k)} = \frac{1}{M} \cdot \sum_{m=0}^{M-1} (\hat{r}_{ue}(k))_m$$

The discrete Fourier transform (DFT) of the averaged cross-correlated function yields the transfer function T(z) in the z-domain, as shown by:

$$T(k) = \frac{1}{N} \cdot \sum_{n=0}^{N-1} \overline{\hat{r}_{ue}(n)} \cdot e^{-j \cdot \frac{2\pi}{N} \cdot n \cdot k}$$

whereas k corresponds to the discrete frequencies:

$$F(k) = \frac{k}{N \cdot T_S}$$

for k=1...N/2. Once T(k) is calculated, the loop gain LG(z) is calculated with the known controller transfer function G(k) as:

$$LG(k) = -\frac{k_P \cdot T(k) \cdot G(k)}{1 + k_P \cdot T(k) \cdot G(k)}$$

Having thus described a preferred embodiment of a system and method for optimizing the digital filter compensation coefficients of a digitally controlled switched mode power supply within a distributed power system, it should be apparent to those skilled in the art that certain advantages of the system have been achieved. It should also be appreciated that various modifications, adaptations, and alternative embodiments thereof may be made within the scope and spirit of the present invention. The invention is further defined by the following claims.

CLAIMS

What is Claimed is:

1. A power control system comprising:

at least one point-of-load (POL) regulator having a power conversion circuit adapted to convey power to a load and a digital controller coupled to the power conversion circuit through a feedback loop, the digital controller being adapted to provide a pulse width modulated control signal to said power conversion circuit responsive to a feedback measurement from an output of the power conversion circuit, said digital controller further comprising a digital filter having a transfer function defined by plural filter coefficients, the digital controller periodically storing a successive one of a plurality of samples of said feedback measurement;

a serial data bus operatively connected to said at least one POL regulator; and

a system controller connected to said serial data bus and adapted to communicate with said at least one POL regulator via said serial data bus, said system controller retrieving each said successive stored sample from said digital controller via said serial data bus;

wherein, after retrieving a pre-determined number of said samples, said system controller calculates optimized filter coefficients for said digital filter and communicates said optimized filter coefficients to said digital controller via said serial data bus, said digital controller thereafter using said optimized filter coefficients in said digital filter.

2. The power control system of Claim 1, wherein said digital controller further comprises a noise source adapted to periodically inject a symmetrical noise signal into said pulse width modulated control signal.

3. The power control system of Claim 2, wherein said symmetrical noise signal further comprises a pseudo-random binary sequence.

4. The power control system of Claim 3, wherein said pre-determined number of samples corresponds to a sequence length of said pseudo-random binary sequence.

5. The power control system of Claim 1, wherein said digital controller further comprises a register adapted to store the successive samples of said feedback measurement.

6. The power control system of Claim 1, wherein said system controller includes a memory array adapted to store the samples retrieved from the digital controller.

7. The power control system of Claim 1, wherein the system controller is adapted to calculate an open loop transfer function of the feedback loop based on the samples retrieved from the digital controller.

8. The power control system of Claim 1, wherein the system controller is adapted to calculate the transfer function of the power conversion circuit based on the samples retrieved from the digital controller.

9. The power control system of Claim 7, wherein the system controller calculates the optimized filter coefficients based on the open loop transfer function of the feedback lop.

10. The power control system of Claim 8, wherein the system controller calculates the optimized filter coefficients based on the transfer function of the power conversion circuit.

11. The power control system of Claim 1, wherein said digital controller further comprises:

an analog-to-digital converter providing a digital error signal representing a difference between the output of the power conversion circuit and a reference, said digital error signal providing said feedback measurement; and

a digital pulse width modulator providing said pulse width modulated control signal.

12. The power control system of Claim 1, wherein the said digital controller further comprises:

an analog-to-digital converter providing an absolute digital representation of the output of the power conversion circuit, a digital subtractor generating a digital error signal representing a difference between said digital output representation and a digital reference, said digital error signal providing said feedback measurement; and

a digital pulse width modulator providing said pulse width modulated control signal.

13. The power control system of Claim 1, wherein said digital filter further comprises an infinite impulse response filter.

14. The power control system of Claim 13, wherein said infinite impulse response filter provides the following transfer function G(z):

$$G(z) = \frac{PWM(z)}{VEd(z)} = \frac{C_0 + C_1 \cdot z^{-1} + C_2 \cdot z^{-2} + ... + C_n \cdot z^{-n}}{1 - B_1 \cdot z^{-1} - B_2 \cdot z^{-2} - ... - B_n \cdot z^{-n}}$$

wherein PWM(z) is the digital control output, VEd(z) is the error signal, $C_0 \ldots C_n$ are input side coefficients, and $B_1 \ldots B_n$ are output side coefficients.

15. The power control system of Claim 1, wherein said power conversion circuit further comprises at least one power switch.

16. A method of controlling at least one point-of-load (POL) regulator coupled to a system controller via a common data bus, the at least one POL regulator having a power conversion circuit adapted to convey power to a load and a digital controller coupled to the power conversion circuit in a feedback loop, the digital controller being adapted to provide a pulse width modulated control signal to said power conversion circuit responsive to a voltage error measurement, said digital controller further comprising a digital filter having a transfer function defined by plural filter coefficients, the method comprising:

injecting a symmetric noise signal into the pulse width modulated control signal for a predetermined period of time;

storing a sample of the voltage error measurement after allowing sufficient time for the noise signal to settle;

transmitting said sample via the common data bus to the system controller;

repeating the injecting, storing, and transmitting steps a predetermined number of times corresponding to a characteristic of the noise signal;

calculating a transfer function for the feedback loop based on plural ones of said samples;

calculating optimal filter coefficients based on the calculated feedback loop transfer function;

transmitting said optimal filter coefficients to said at least one POL regulator via the common data bus; and

programming said digital filter using said optimal filter coefficients.

17. The method of Claim 16, wherein said injecting step further comprises injecting a pseudo-random binary sequence signal into the pulse width modulated control signal.

18. The method of Claim 17, wherein the repeating step further comprises repeating the injecting, storing, and transmitting steps a number of times corresponding to a sequence length of said pseudo-random binary sequence.

19. The method of Claim 16, wherein said calculating a transfer function further comprises cross-correlating the samples with a noise signal, and transforming the cross-correlation result in frequency domain using a Fourier transform.

20. The method of Claim 16, further comprising calculating a transfer function of the power conversion circuit based on plural ones of said samples.

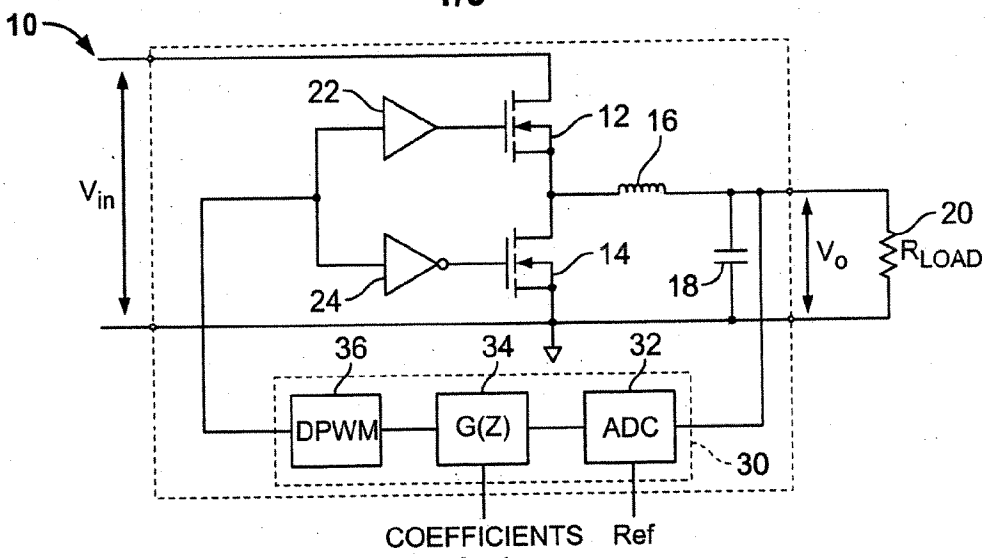
10
22
12
16
V_{in}
20
V_o
R_{LOAD}
14
18
24
36
34
32
DPWM
G(Z)
ADC
30
COEFFICIENTS
Ref

FIG. 1

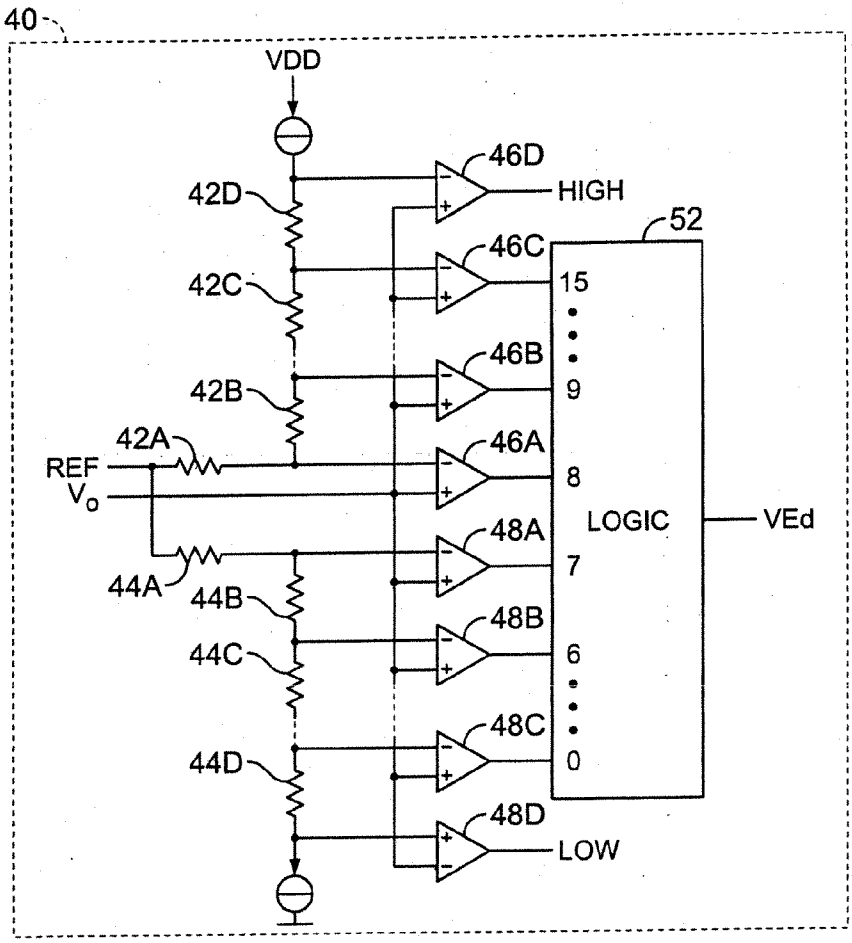
40
VDD
46D
HIGH
42D
52
46C
42C
15
46B
42B
9
42A
46A
REF
V_o
8
LOGIC
VEd
48A
44A
7
44B
48B
44C
6
48C
44D
0
48D
LOW

FIG. 2

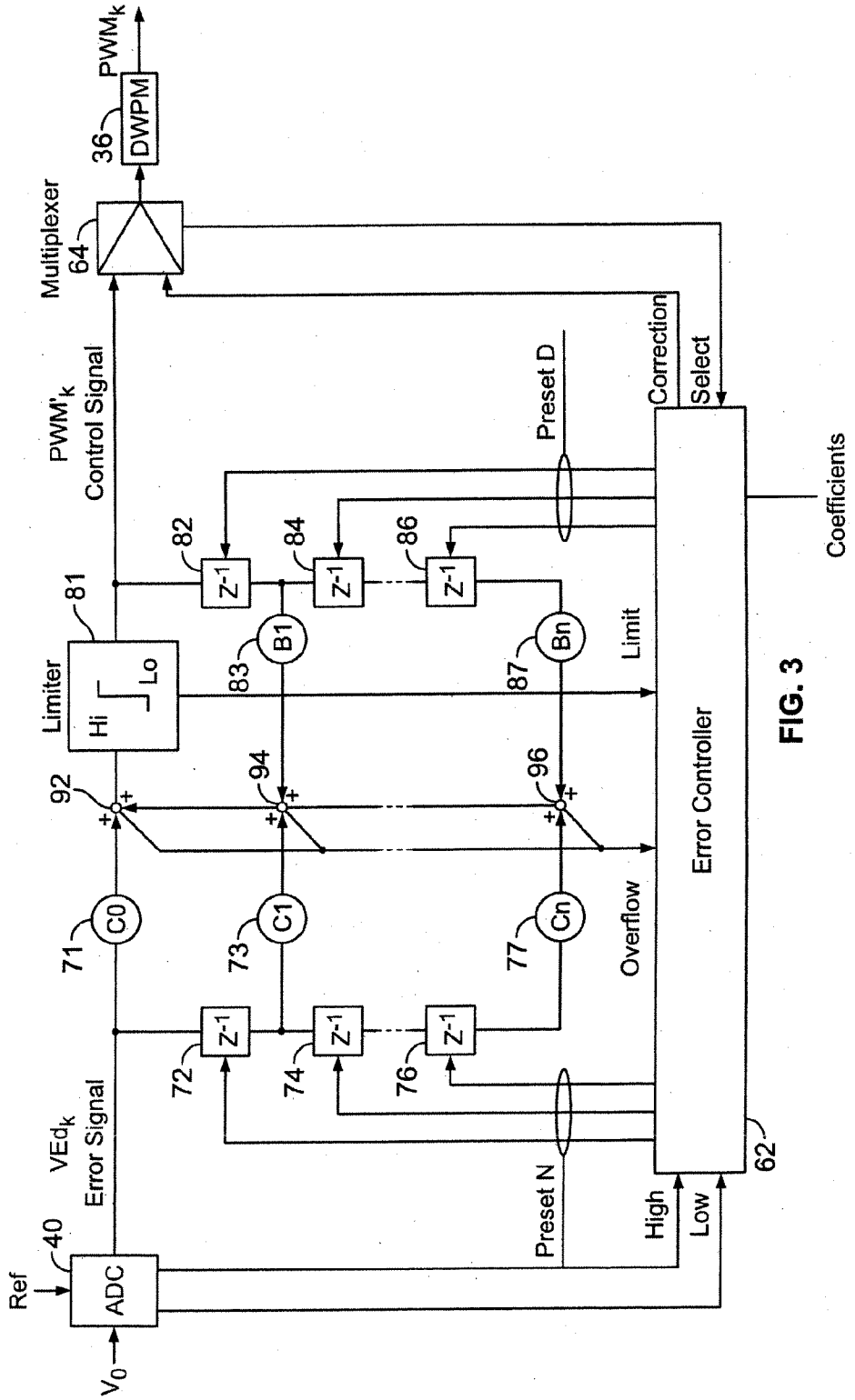
PWM$_k$
36
DWPM
Multiplexer
64
PWM'$_k$
Control Signal
Correction
Select
Preset D
Coefficients
82
84
86
Z^{-1}
81
Limiter
Hi
Lo
B1
Bn
83
87
Limit
92
94
96
+
C0
C1
Cn
71
73
77
Overflow
Error Controller
72
74
76
VEd$_k$
Error Signal
Preset N
High
Low
62
40
Ref
ADC
V$_0$

FIG. 3

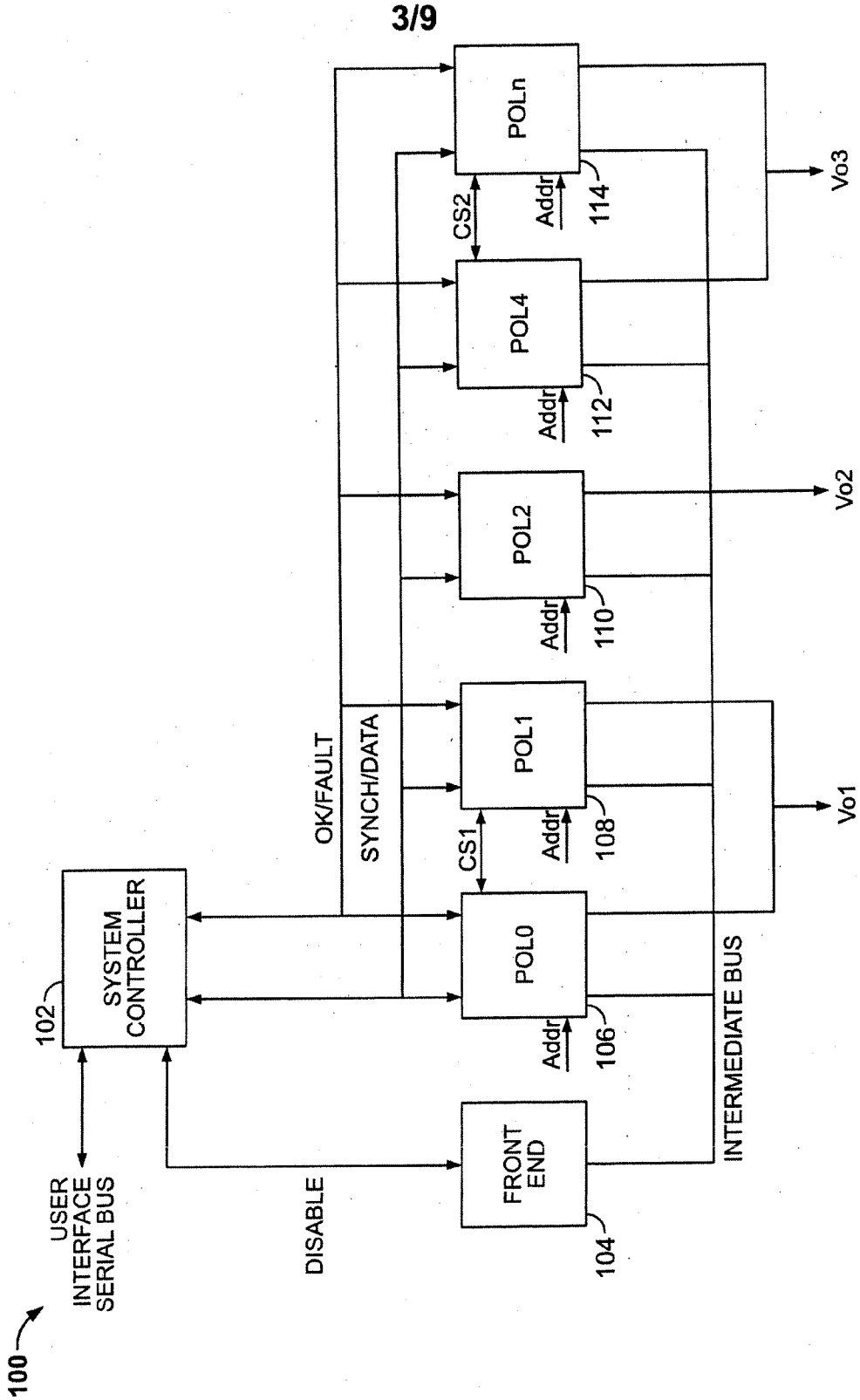
100
USER INTERFACE SERIAL BUS
SYSTEM CONTROLLER
102
FRONT END
104
POL0
106
POL1
108
POL2
110
POL4
112
POLn
114
Addr
CS1
CS2
OK/FAULT
SYNCH/DATA
DISABLE
INTERMEDIATE BUS
Vo1
Vo2
Vo3

FIG. 4

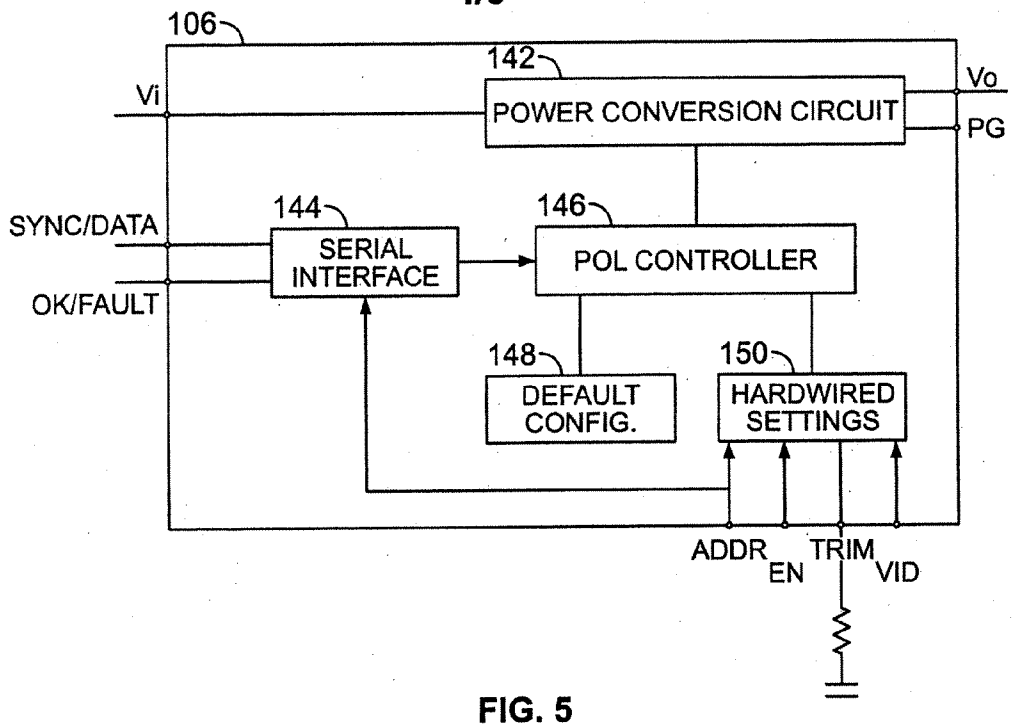
106
142
Vi
POWER CONVERSION CIRCUIT
Vo
PG
SYNC/DATA
144
SERIAL INTERFACE
146
POL CONTROLLER
OK/FAULT
148
DEFAULT CONFIG.
150
HARDWIRED SETTINGS
ADDR
EN
TRIM
VID

FIG. 5

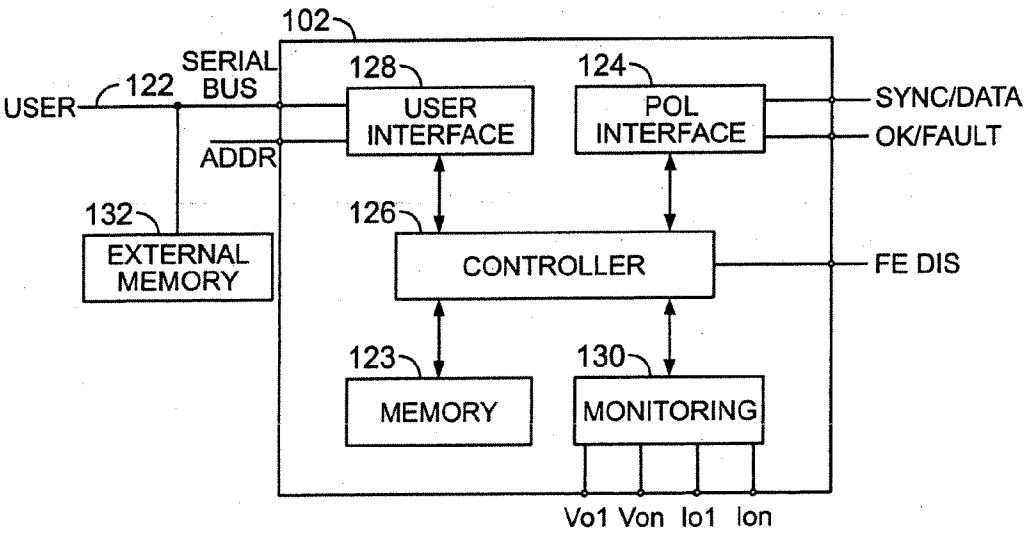
102
SERIAL BUS
USER
122
128
USER INTERFACE
124
POL INTERFACE
SYNC/DATA
OK/FAULT
ADDR
132
EXTERNAL MEMORY
126
CONTROLLER
FE DIS
123
MEMORY
130
MONITORING
Vo1 Von Io1 Ion

FIG. 6

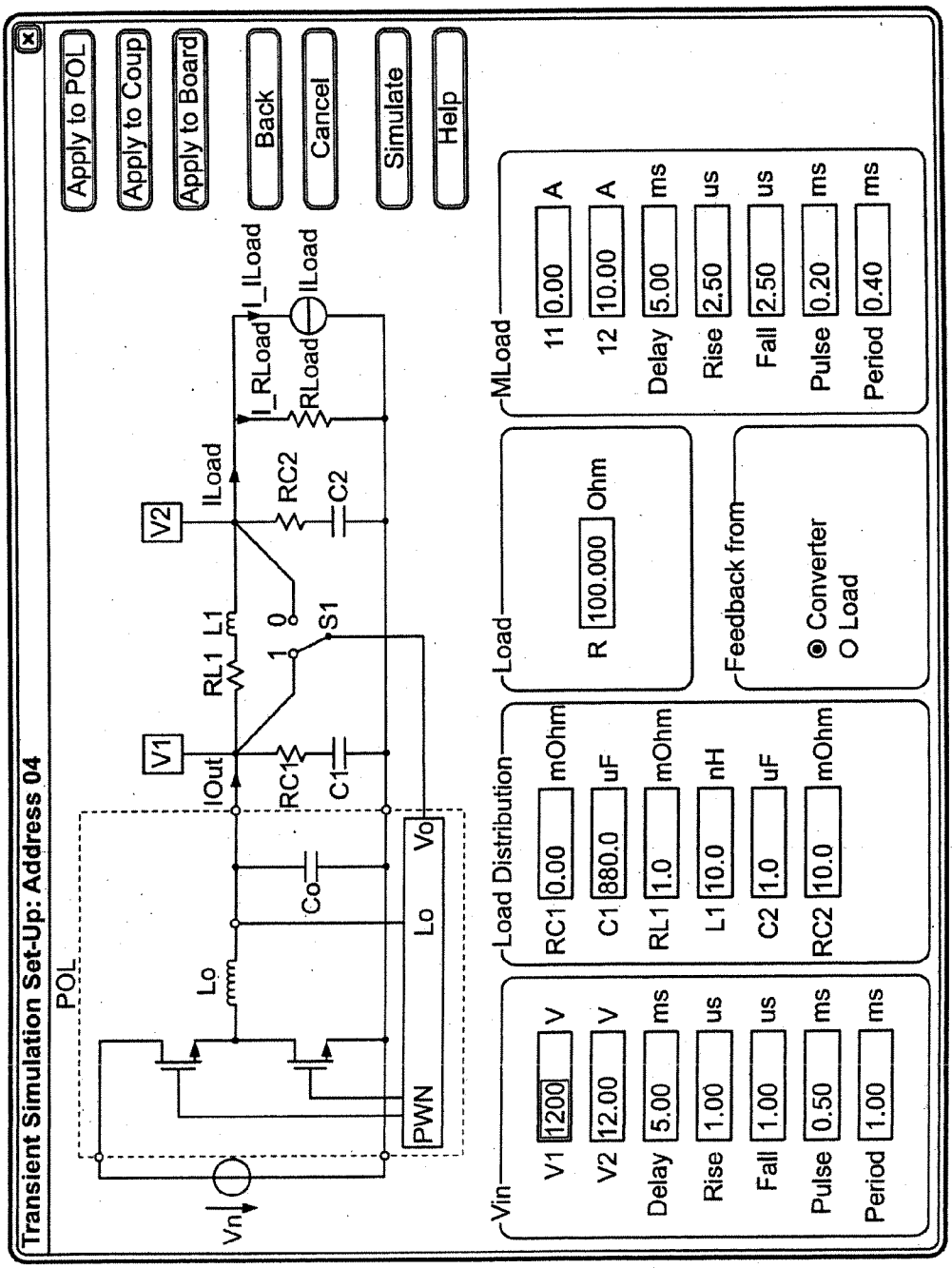
Transient Simulation Set-Up: Address 04
Apply to POL
Apply to Coup
Apply to Board
Back
Cancel
Simulate
Help
POL
Vn
Lo
Co
IOut
V1
RC1
C1
RL1
L1
1
0
S1
V2
ILoad
RC2
C2
I_RLoad
RLoad
I_ILoad
ILoad
PWN
Lo
Vo
Vin
V1 1200 V
V2 12.00 V
Delay 5.00 ms
Rise 1.00 us
Fall 1.00 us
Pulse 0.50 ms
Period 1.00 ms
Load Distribution
RC1 0.00 mOhm
C1 880.0 uF
RL1 1.0 mOhm
L1 10.0 nH
C2 1.0 uF
RC2 10.0 mOhm
Load
R 100.000 Ohm
Feedback from
Converter
Load
MLoad
I1 0.00 A
I2 10.00 A
Delay 5.00 ms
Rise 2.50 us
Fall 2.50 us
Pulse 0.20 ms
Period 0.40 ms

FIG. 7

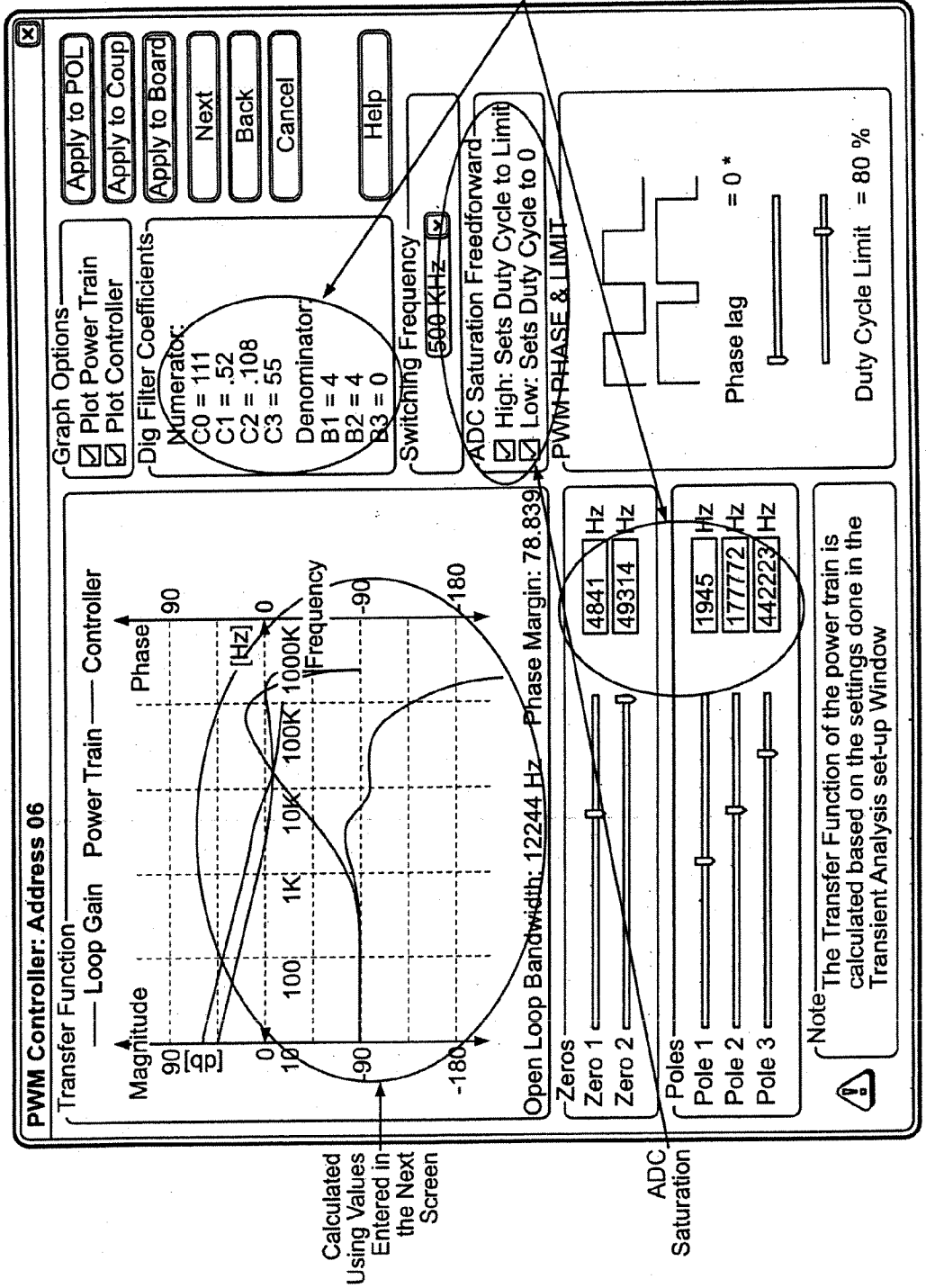
PWM Controller: Address 06
Transfer Function
Loop Gain
Power Train
Controller
Magnitude
Phase
[db]
[Hz]
Frequency
Graph Options
Plot Power Train
Plot Controller
Dig Filter Coefficients
Numerator:
C0 = 111
C1 = .52
C2 = .108
C3 = 55
Denominator:
B1 = 4
B2 = 4
B3 = 0
Switching Frequency
500 KHz
ADC Saturation Freedforward
High: Sets Duty Cycle to Limit
Low: Sets Duty Cycle to 0
PWM PHASE & LIMIT
Phase lag = 0 *
Duty Cycle Limit = 80 %
Apply to POL
Apply to Coup
Apply to Board
Next
Back
Cancel
Help
Poles and Zeroes are Calculated Based on Digital Filter Coefficients
Open Loop Bandwidth: 12244 Hz Phase Margin: 78.839
Zeros
Zero 1
Zero 2
4841 Hz
49314 Hz
Poles
Pole 1
Pole 2
Pole 3
1945 Hz
177772 Hz
442223 Hz
Note
The Transfer Function of the power train is calculated based on the settings done in the Transient Analysis set-up Window
Calculated Using Values Entered in the Next Screen
ADC Saturation

FIG. 8

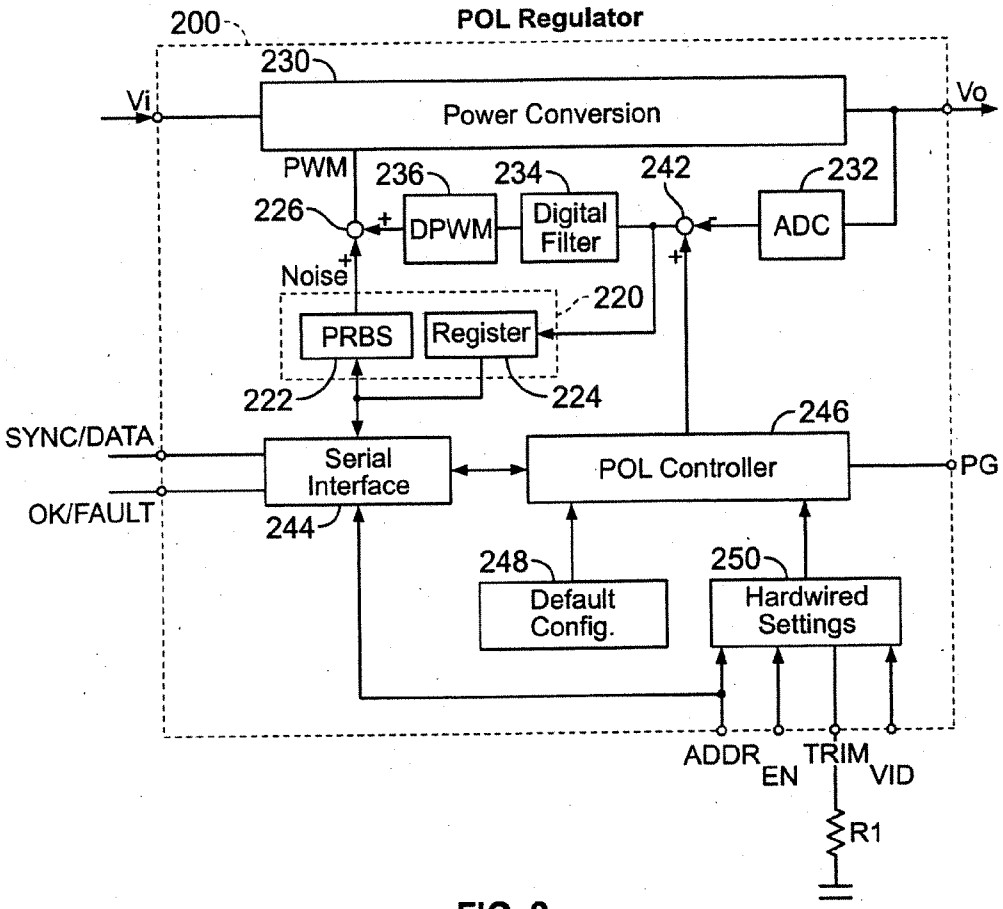
200
POL Regulator
230
Vi
Power Conversion
Vo
PWM
236
234
242
232
226
DPWM
Digital Filter
ADC
Noise
220
PRBS
Register
222
224
246
SYNC/DATA
Serial Interface
POL Controller
PG
OK/FAULT
244
248
250
Default Config.
Hardwired Settings
ADDR
EN
TRIM
VID
R1

FIG. 9

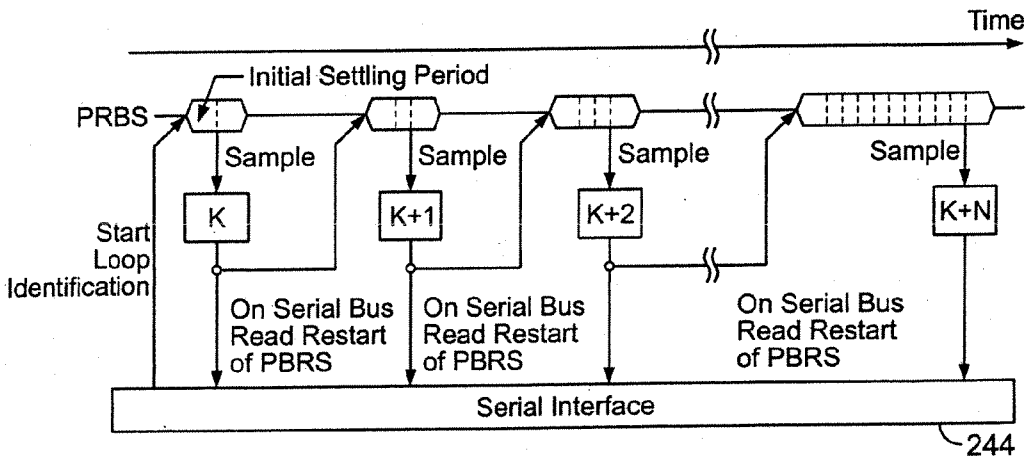
Time
Initial Settling Period
PRBS
Sample
Sample
Sample
Sample
K
K+1
K+2
K+N
Start Loop Identification
On Serial Bus Read Restart of PBRS
On Serial Bus Read Restart of PBRS
On Serial Bus Read Restart of PBRS
Serial Interface
244

FIG. 10

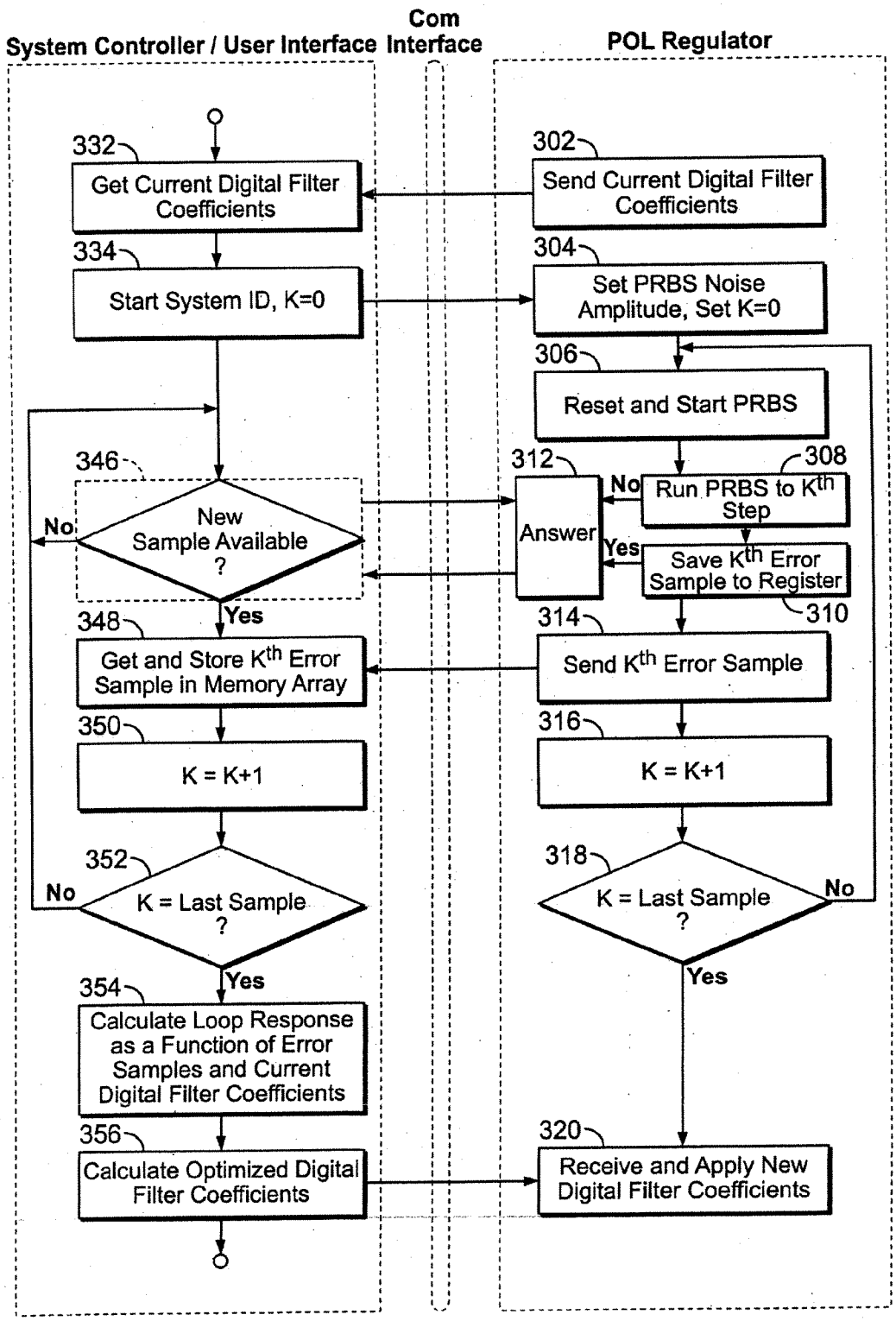
System Controller / User Interface
Com Interface
POL Regulator
332
Get Current Digital Filter Coefficients
334
Start System ID, K=0
346
New Sample Available ?
No
Yes
348
Get and Store Kth Error Sample in Memory Array
350
K = K+1
352
K = Last Sample ?
No
Yes
354
Calculate Loop Response as a Function of Error Samples and Current Digital Filter Coefficients
356
Calculate Optimized Digital Filter Coefficients
302
Send Current Digital Filter Coefficients
304
Set PRBS Noise Amplitude, Set K=0
306
Reset and Start PRBS
312
Answer
No
Yes
308
Run PRBS to Kth Step
Save Kth Error Sample to Register
310
314
Send Kth Error Sample
316
K = K+1
318
K = Last Sample ?
No
Yes
320
Receive and Apply New Digital Filter Coefficients

FIG. 11

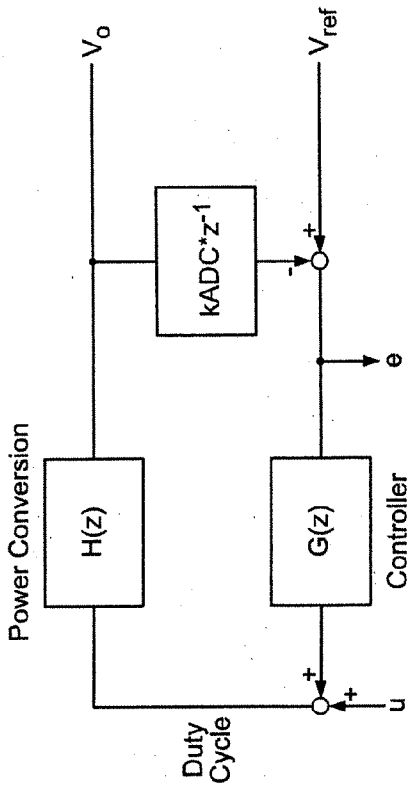
V_o
V_{ref}
kADC*z^{-1}
+
-
e
Power Conversion
H(z)
G(z)
Controller
+
+
u
Duty Cycle

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 08/70117

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 1/26; H02M 7/68 (2008.04)
USPC - 713/300
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 713/300

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 713/300; 708/300, 400 (keyword limited - see search terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST (PGPB, USPT, USOC, EPAB, JPAB); GOOGLE
Terms: infinite, finite, impulse, response, IIR, point, load, power, regulator, digital, feedback, transfer, function, serial, data, bus, filter, coefficient, fourier, transform, controller

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2004/0246754 A1 (Chapuis) 09 December 2004 (09.12.2004), entire document especially, abstract, para [0006], [0012], [0014], [0027], [0028], [0031], [0032], [0034], [0037], [0041], [0042], [0045].	16-20 -------- 1-15
Y	US 2003/0090255 A1 (Bassett et al.) 15 May 2003 (15.05.2003), entire document especially, figure 5, para [0046].	1-15

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 September 2008 (26.09.2008)	03 OCT 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)