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(54) **THREE-DIMENSIONAL PACKAGING SCHEME FOR PACKAGE TYPES UTILIZING A SACRIFICIAL METAL BASE**

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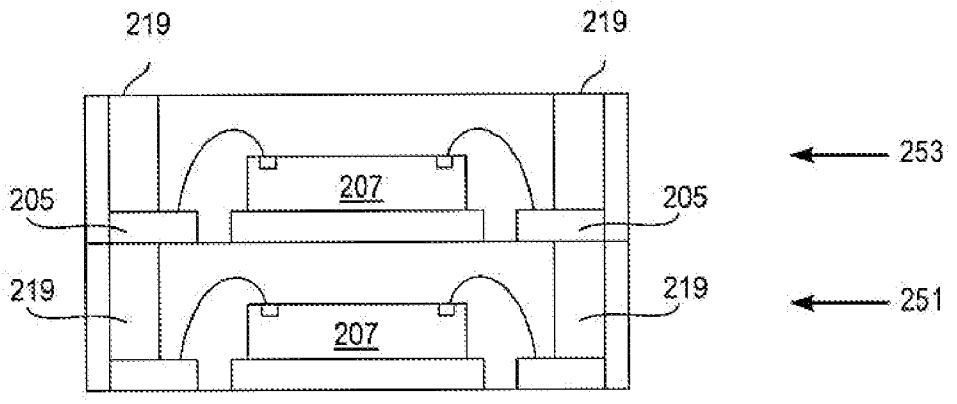
(57) **ABSTRACT**

An apparatus and a method for packaging semiconductor devices. The apparatus is applicable to many types of contemporary packaging schemes that utilize a sacrificial metal base strip. Tunnels formed through an encapsulation area surrounding the device and associated bond wires are filled with a metallic conductor by, for example, electroplating, and extend bottom contact pads to an uppermost portion of the encapsulated area. The sacrificial metal base strip serves as a plating bus and is etch-removed after plating. The filled tunnels allow components to be stacked in a three-dimensional configuration.



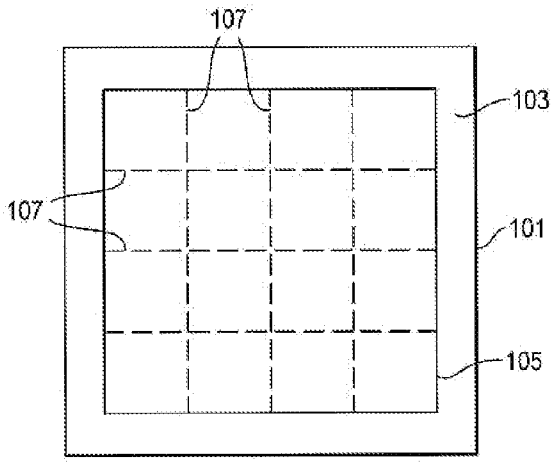


Fig._1A (Prior Art)

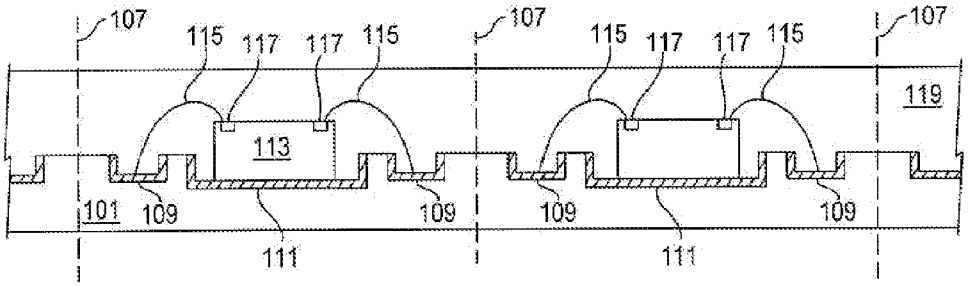


Fig._1B (Prior Art)

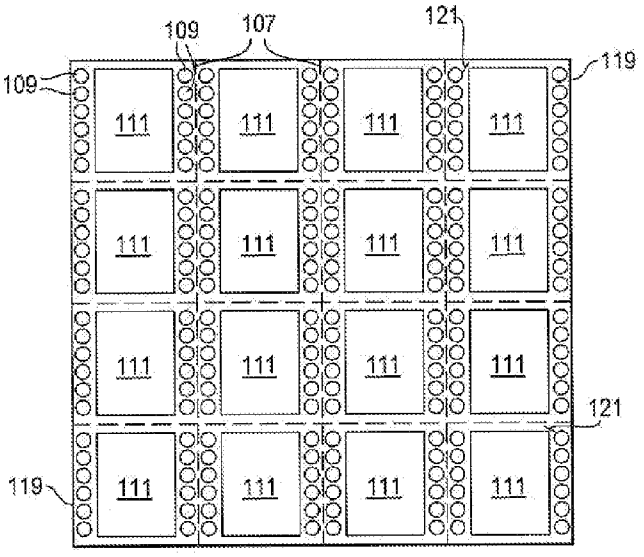


Fig._1C (Prior Art)

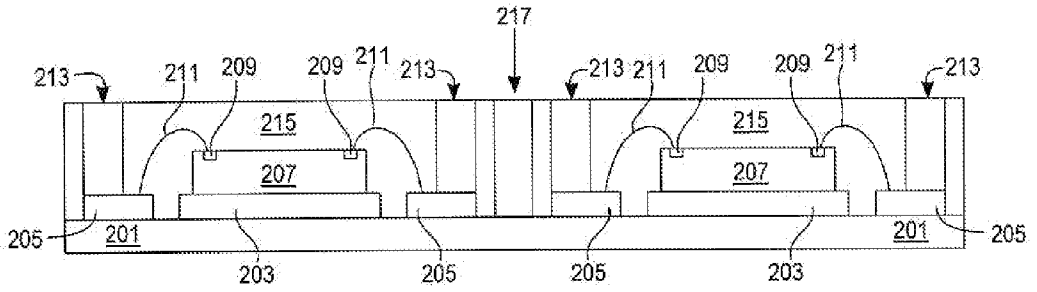


Fig._2A

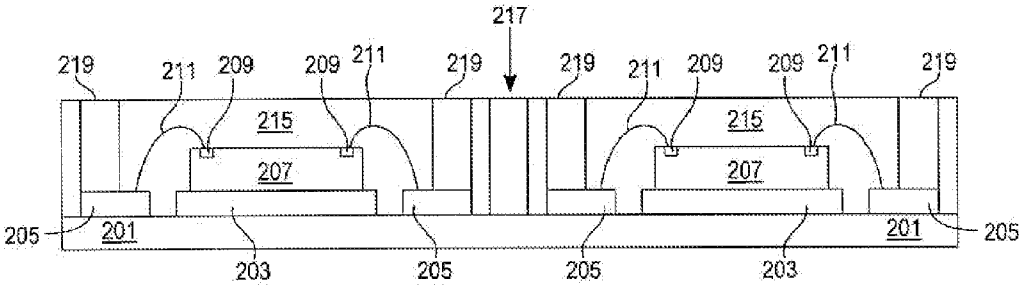

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Fig._2B

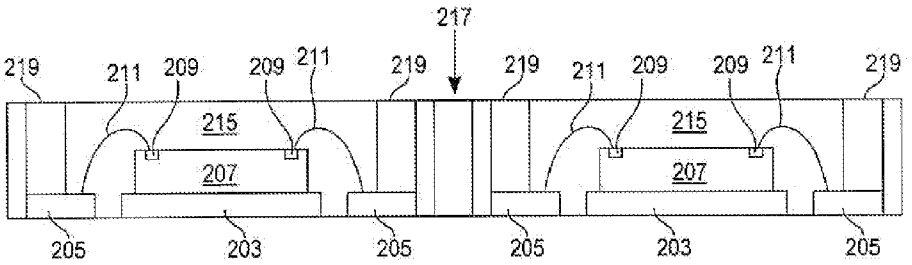
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Fig._2C

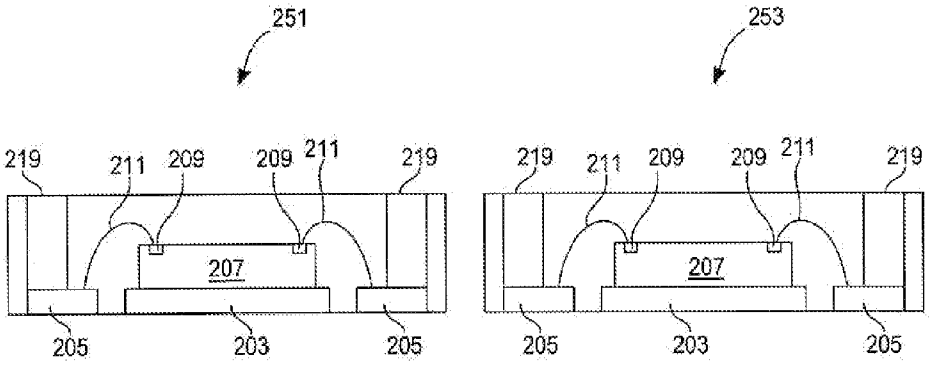
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Fig._ 2D

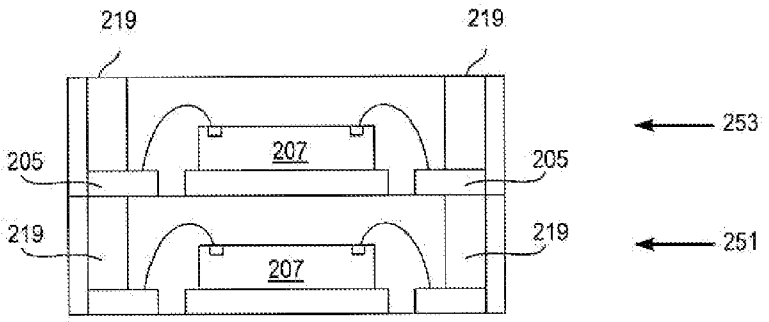
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Fig._ 2E

THREE-DIMENSIONAL PACKAGING SCHEME FOR PACKAGE TYPES UTILIZING A SACRIFICIAL METAL BASE

TECHNICAL FIELD

[0001] The invention relates to a three-dimensional stackable semiconductor package, and more particularly, to a three-dimensional stackable semiconductor package for package types having a sacrificial metal base.

BACKGROUND ART

[0002] As semiconductor integrated circuit chips become more multi-functional and highly integrated, the chips include more bonding pads (or terminal pads), and thus packages for the chips have more external terminals (or leads). When a conventional plastic package that has its leads along the perimeter of the package must accommodate a large number of leads, the footprint of the package increases. However, a goal in many electronic systems is to minimize an overall size of the systems. Thus, to accommodate a large number of pins without increasing the footprint of package, pin pitch (or lead pitch) of the package must decrease. However, a pin pitch of less than about 0.4 mm gives rise to many technical concerns. For example, trimming of a package having a pin pitch less than 0.4 mm requires expensive trimming tools, and the leads are prone to bending during handling of the package. In addition, surface-mounting of such packages demands a costly and complicated surface-mounting process due to a required critical alignment step.

[0003] Thus, to avoid technical problems associated with conventional fine-pitch packages, packages that have area array external terminals have been suggested. Among these packages are ball grid array packages and chip scale packages. The semiconductor industry presently uses a number of chip scale packages. A micro ball grid array package (μBGA) and a bump, chip carrier (BCC) are examples of the chip scale packages. The μBGA package includes a polyimide tape on which a conductive pattern is formed and employs a totally different manufacturing process from a conventional plastic packaging. The bump chip carrier package includes a substrate having grooves formed around a central portion of a top surface of a copper alloy plate and an electroplating layer formed in the grooves. Accordingly, chip scale packages use specialized packaging materials and processes that increase package manufacturing costs.

[0004] FIGS. **1**A through **1**C illustrate plan and cross-sectional views of a conventional apparatus for manufacturing leadless BCC packages. With reference to the plan view of FIG. **1**A, a conventional metal carrier matrix array **101** has an upper surface **103**, which includes an encapsulating matrix **105** with a plurality of sawing lines **107**.

[0005] The cross-sectional view of FIG. **13** includes a plurality of bump pads **109** and a plurality of die pads **111** formed on the upper surface **103** of the metal carrier **101** by plating. Back surfaces of integrated circuit dice **113** are attached to corresponding die pads **111**, and a plurality of bonding wires **115** connect a plurality of bonding pads **117** on active surfaces of the dice **113** to corresponding bump pads **109**. A encapsulant **119** encapsulates the encapsulating matrix **105** including the dice **113** and the bonding wires **115**.

[0006] With reference to the underside plan view of FIG. **10**, after etching away the metal carrier **101** (not shown in FIG. **1**C, the bump pads **109** and the die pads **111** are exposed from the bottom surface **121** of the encapsulant **119**. Then, the encapsulant **119** is singulated by sawing along the sawing lines **107** to form a plurality of individual BCC packages.

[0007] Therefore, a integrated circuit package that uses conventional packaging materials and processes can only be accessed for electrical interconnection, for example, to a printed circuit board, by the bump pads on the bottom surface **121** of the package. Consequently, what is needed to provide for a higher density of integrated circuit packaging into a given printed circuit board footprint is a means of allowing the integrated circuit packages to be stacked, one atop another.

SUMMARY

[0008] The present invention is an apparatus and a method for packaging semiconductor devices. The apparatus is applicable to many types of contemporary packaging schemes that utilize a sacrificial metal base strip. Tunnels formed through an encapsulation volume surrounding the device and associated bond wires are filled with a metallic conductor by, for example, electroplating. The filled tunnels extend bottom contact pads to an uppermost portion of the encapsulated area.

[0009] The sacrificial metal base strip serves as a plating bus and is etch-removed after plating. The filled tunnels allow components to be stacked in a three-dimensional configuration. In a specific exemplary embodiment, the invention may be applied to multiple dice or combinations of circuits and dice within stackable packages. Each of the stackable packages may then be stacked three-dimensionally while not increasing an overall footprint size of a mounting area on, for example, a printed circuit board.

[0010] The present invention is thus, in one exemplary embodiment, a semiconductor package matrix. The semiconductor package matrix includes a plurality of three-dimensional stackable semiconductor packages arranged side-by-side in an array within the matrix and separated by kerf regions. The kerf regions are located at an outermost periphery of each of the plurality of three-dimensional stackable semiconductor packages. Each of the plurality of three-dimensional stackable semiconductor packages includes an area for mounting an integrated circuit die and/or one or more discrete electrical components and a plurality of wirebond pads substantially coplanar with a die mounting area. Each of the plurality of wirebond pads allows a bonding wire to provide electrical communication from either the integrated circuit die and/or the one or more discrete electrical components to outside of the packaged device.

[0011] A mold cap has a lowermost portion and an uppermost portion. The lowermost portion is at a level substantially coplanar with the die mounting area and the plurality of wirebond pads. The mold cap has a plurality of conducting contact tunnels, each of which is associated and arranged to be in electrical communication with a corresponding one of the plurality of wirebond pads once a conducting material fills the conducting contact tunnel. The plurality of conduct-

ing contact tunnels extend from an uppermost portion of the plurality of wirebond pads to the uppermost portion of the mold cap.

[0012] The present invention is also a method of packaging a semiconductor device (or plurality of devices within a single package). An exemplary embodiment of the method includes mounting an electrical component to a die mounting area and securing a plurality of bond wires from a plurality of bond pads on the electrical component to corresponding ones of a plurality of wirebond pads. A mold cavity is provided which has a plurality of conducting contact tunnels. The contact tunnels are arranged such that the plurality of conducting contact tunnels are disposed over the plurality of wirebond pads. The electrical component and the bond wires are encapsulated with a mold compound, substantially filling the mold cavity. The plurality of conducting contact tunnels are then filled with an electrically conductive material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIGS. **1**A-**1**C show a bumped chip carrier of the prior art.

[0014] FIGS. **2**A-**2**E show exemplary cross-sections of stackable integrated circuit die and discrete component carriers in accord with the present invention.

DETAILED DESCRIPTION

[0015] In FIG. **2**A, a cross-sectional view of a potentially-stackable integrated circuit die and discrete component carriers includes a sacrificial metal base strip **201**, a plurality of die mounting areas **203**, and a plurality of wirebond pads **205**. As shown, a plurality of integrated circuit dice **207** are mounted to corresponding ones of the plurality of die mounting areas **203**. Alternatively, the plurality of integrated circuit dice **207** may also be discrete components (not shown) or a combination of integrated circuit dice and discrete components mounted to a plurality of die mounting areas.

[0016] Also, the sacrificial metal base layer may be constructed from an electrically conducting non-metallic material such as, for example, polypropylene with embedded carbon particles or a polymer strip overplated with metal.

[0017] As known in the art, a thermally-conductive adhesive or adhesive tape (neither of which is shown) is commonly used for mounting the plurality of dice **207** to associated die mounting areas **203**. As one skilled in the art will recognize, other types of adhesives (e.g., non-thermally conducting, electrically and non-electrically conducting, etc.) or other mounting techniques may be used as well. The plurality of dice **207** each include a plurality of bonding pads **209**. Once the plurality of dice **207** are mounted, a plurality of bonding wires **211** are used to electrically connect the plurality of bonding pads **209** to selected ones of the plurality of wirebond pads **205**.

[0018] The plurality of wirebond pads **205**, dice **207**, and bonding wires **211** are typically encapsulated in a molding compound. The molding compound is introduced into a molding cavity (not shown) by a mold gate located at an edge of the sacrificial metal base strip **201**. The molding compound is typically a polymeric precursor comprised of an epoxy base material filled with silica and anhydrides, requiring thermal energy for curing to form a polymeric encapsulant **215**. The encapsulant **215** protects the fragile plurality of bonding wires **211** and their associated electrical connections, as well as the plurality of dice **207**. In this embodiment, tubes are located above each of the plurality of wirebond pads **205**, thus forming tunnels **213** after the encapsulant **215** is poured and formed. The tubes may be formed by placing pins or other structures either into the mold or added afterwards (e.g., machined or welded into place into a mold cavity). Streets **217** indicate where the saw kerf is to run during a subsequent dicing operation.

[0019] With reference to FIG. **2**E, the tunnels **213** have been filled with a conductor to produce a plurality of conducting metal contacts **219**. In a specific exemplary embodiment the sacrificial metal base strip **201** provides electrical continuity required for an electrolytic plating process so the plurality of conducting metal contacts **219** (e.g., copper) can be fabricated by filling the tunnels **213** (FIG. **2**A). Copper, or virtually any other metal, used for fabricating the plurality of conducting metal contacts **219** may then optionally be capped with, for example, nickel-gold alloy caps or another noble metal. Alternatively, the plurality of conducting metal contacts **219** may be fabricated by, for example, plating with materials such as tungsten or tantalum into the tunnels **213**. Additionally, a conductive epoxy or polymer may be used to fill the tunnels **213**. The conductive epoxy is then cured in place.

[0020] The sacrificial metal base strip **201** is then etch removed (FIG. **2**C) by processes known in the art. Die mounting areas and wirebond pads may be plated with, for example, gold-nickel-gold or palladium-gold such that only the alloy bonding areas are left intact after etch. The dice are then singulated (FIG. **2**D), for example, by a die saw or laser, producing a first **251** and a second **253** packaged product.

[0021] With reference to FIG. **2**E, the singulated first **251** and second **253** packaged products are mechanically stacked. The plurality of conducting metal contacts **219** allow each of the wirebond pads **205** at one level (e.g., at the first packaged product **251**) to be interconnected to another level (e.g., to the second packaged product **253**) to be electrically connected through the use of solder (e.g., solder paste), conductive epoxy, metal bonding (e.g., through an application of ultrasonic or thermal forces), and so on. Thus, there is no limit on the number of packages than can be stacked.

[0022] In the foregoing specification, the present invention has been described with reference to specific embodiments thereto. It will, however, be evident to a skilled artisan that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims, For example, skilled artisans will appreciate that embodiments of the present invention may be readily applied to TAPP® (thin array plastic package), ULGA® (ultra-thin land grid array), BCC® (bumped chip carrier), or other similar packages types. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A three-dimensional stackable semiconductor package comprising:

at least one die mounting area, the at least one die mounting area configured either to accept an integrated circuit die or one or more discrete electrical components;

a plurality of wirebond pads substantially coplanar with the at least one die mounting area, each of the plurality of wirebond pads configured to accept a bonding wire thereby providing electrical communication from either the integrated circuit die or the one or more discrete electrical components; and

a mold cap having a lowermost portion and an uppermost portion, the lowermost portion being at a level substantially coplanar with the at least one die mounting area and the plurality of wirebond pads, the mold cap also having a plurality of conducting contact tunnels, each of the plurality of conducting contact tunnels associated and arranged to be in electrical communication with a corresponding one of the plurality of wirebond pads once a conducting material fills the conducting contact tunnel, the plurality of conducting contact tunnels extending from an uppermost portion of the plurality of wirebond pads to the uppermost portion of the mold cap.

2. The three-dimensional stackable semiconductor package of claim 1 further comprising a sacrificial metal base layer, the sacrificial metal base layer serving as a mounting base and electrical contact for the at least one die mounting area and the plurality of wirebond pads.

3. The three-dimensional stackable semiconductor package of claim 2 wherein the sacrificial metal base layer is configured to be etch removed once an encapsulating mold compound is formed within the mold cap.

4. A three-dimensional stackable semiconductor package comprising:

at least one die mounting area, the at least one die mounting area configured either to accept an integrated circuit die or one or more discrete electrical components;

a plurality of wirebond pads substantially coplanar with the at least one die mounting area, each of the plurality of wirebond pads configured to accept a bonding wire thereby providing electrical communication from either the integrated circuit die or the one or more discrete electrical components;

a sacrificial base layer, the sacrificial base layer serving as a mounting base for the at least one die mounting area and the plurality of wirebond pads; and

a mold cap having a lowermost portion and an uppermost portion, the lowermost portion being at a level substantially coplanar with an uppermost surface of the sacrificial base layer, the mold cap also having a plurality of conducting contact tunnels, each of the plurality of conducting contact tunnels associated and arranged to be in electrical communication with a corresponding one of the plurality of wirebond pads once a conducting material fills the conducting contact tunnel, the plurality of conducting contact tunnels extending from an uppermost portion of the plurality of wirebond pads to the uppermost portion of the mold cap.

5. The three-dimensional stackable semiconductor package of claim 4 wherein the sacrificial base layer is comprised of a metallic material.

6. The three-dimensional stackable semiconductor package of claim 4 wherein the sacrificial base layer is comprised of a non-metallic electrically conducting material.

7. The three-dimensional stackable semiconductor package of claim 4 wherein the sacrificial base layer is configured to be etch removed once an encapsulating mold compound is formed within the mold cap.

8. A semiconductor package matrix comprising:

a plurality of three-dimensional stackable semiconductor packages arranged side-by-side in an array within the matrix and separated by kerf regions, the kerf regions being located at an outermost periphery of each of the plurality of three-dimensional stackable semiconductor packages, each of the plurality of three-dimensional stackable semiconductor packages including:

at least one die mounting area, the at least one die mounting area configured either to accept an integrated circuit die or one or more discrete electrical components;

a plurality of wirebond pads substantially coplanar with the at least one die mounting area, each of the plurality of wirebond pads configured to accept a bonding wire thereby providing electrical communication from either the integrated circuit die or the one or more discrete electrical components; and

a mold cap having a lowermost portion and an uppermost portion, the lowermost portion being at a level substantially coplanar with the at least one die mounting area and the plurality of wirebond pads, the mold cap also having a plurality of conducting contact tunnels, each of the plurality of conducting contact tunnels associated and arranged to be in electrical communication with a corresponding one of the plurality of wirebond pads once a conducting material fills the conducting contact tunnel, the plurality of conducting contact tunnels extending from an uppermost portion of the plurality of wirebond pads to the uppermost portion of the mold cap.

9. The semiconductor package matrix of claim 8 further comprising a sacrificial base layer, the sacrificial base layer serving as a mounting base for the at least one die mounting area and the plurality of wirebond pads.

10. The semiconductor package matrix of claim 9 wherein the sacrificial base layer is configured to be etch removed once an encapsulating mold compound is formed within the mold cap.

11. The semiconductor package matrix of claim 9 wherein the sacrificial base layer is comprised of metal.

12. A method of packaging a semiconductor device, the method comprising:

mounting an electrical component to a die mounting area;

securing a plurality of bond wires from a plurality of bond pads on the electrical component to corresponding ones of a plurality of wirebond pads;

providing a mold cavity having a plurality of conducting contact tunnels such that a first end of each of the plurality of conducting contact tunnels are disposed over and in contact with associated ones of the plurality of wirebond pads;

encapsulating the electrical component and the plurality of bond wires with a mold compound, the mold compound substantially filling the mold cavity; and

filling the plurality of conducting contact tunnels with an electrically conductive material.

13. The method of claim 12 further comprising selecting the electrically conductive fill material to be substantially comprised of copper.

14. The method of claim 12 further comprising providing an electrically conductive capping material to be disposed over exposed ends of the filled conducting contact tunnels.

15. The method of claim 14 wherein the capping material is selected to be a nickel-gold alloy.

16. The method of claim 12 further comprising etch-removing a sacrificial base material from the packaged semiconductor device.

17. The method of claim 12 further comprising stacking a plurality of semiconductor device packages, one atop another.

18. The method of claim 17, further comprising electrically coupling each of the plurality of filled conducting contact tunnels on a first packaged semiconductor device to each of the plurality of filled conducting contact tunnels on a second packaged semiconductor device.

* * * * *