

[54] **MULTIPLE CHANNEL ALPHANUMERIC RESIDENTIAL TELEVISION VIDEO SIGNAL GENERATOR**

[75] Inventors: **James A. Dalke**, Bellevue; **Wayne E. Hough**, Seattle, both of Wash.

[73] Assignee: **MetroData Corporation**, Seattle, Wash.

[22] Filed: **Sept. 14, 1973**

[21] Appl. No.: **397,288**

[52] U.S. Cl. **340/324 AD; 340/152**

[51] Int. Cl.² **G06F 3/14**

[58] Field of Search **340/324 AD, 152, 154**

[56] **References Cited**

UNITED STATES PATENTS

3,453,384	7/1969	Donner et al.	340/324 AD
3,500,327	3/1970	Belcher et al.	340/324 AD
3,500,335	3/1970	Cuccio	340/324 AD
3,555,520	1/1971	Helbig et al.	340/324 AD
3,569,617	3/1971	Allen et al.	340/324 AD
3,624,632	11/1971	Ophir	340/324 AD
3,641,559	2/1972	Hogan et al.	340/324 AD
3,685,038	8/1972	Flanagan	340/324 AD

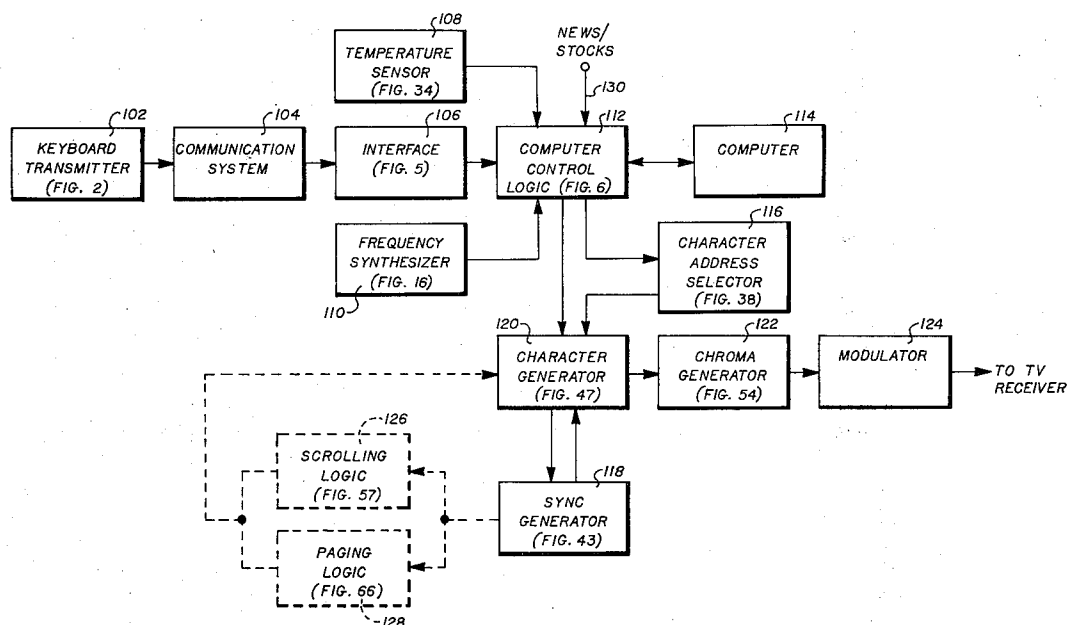
Primary Examiner—Marshall M. Curtis

Attorney, Agent, or Firm—Christensen, O'Connor, Garrison & Havelka

[57] **ABSTRACT**

A multiple channel television display system suitable for receiving information (data) from a variety of sources and selectively displaying the information as alphanumeric characters on a plurality of television channels is disclosed. The information sources may be newswires, stock report wires, remote or local keyboards, temperature probes, etc. The information is received by computer control logic which feeds information to and receives instructions from a suitably programmed general purpose digital computer. The computer, in accordance with the information received by it relating to the receipt of information by the computer control logic from the various information sources, selectively interrogates the computer control logic to receive, in accordance with a priority arrangement, the information from the various information sources. The information from the various sources received by the computer is edited, if necessary. The computer instructs the computer control logic in a manner such that a different alphanumeric character display is generated on the picture tubes of connected television sets for each of the plurality of channels. In addition, the alphanumeric character displays can be made to appear to move (scroll) upwardly or downwardly, or they can be made to appear as consecutive pages on the display.

29 Claims, 66 Drawing Figures



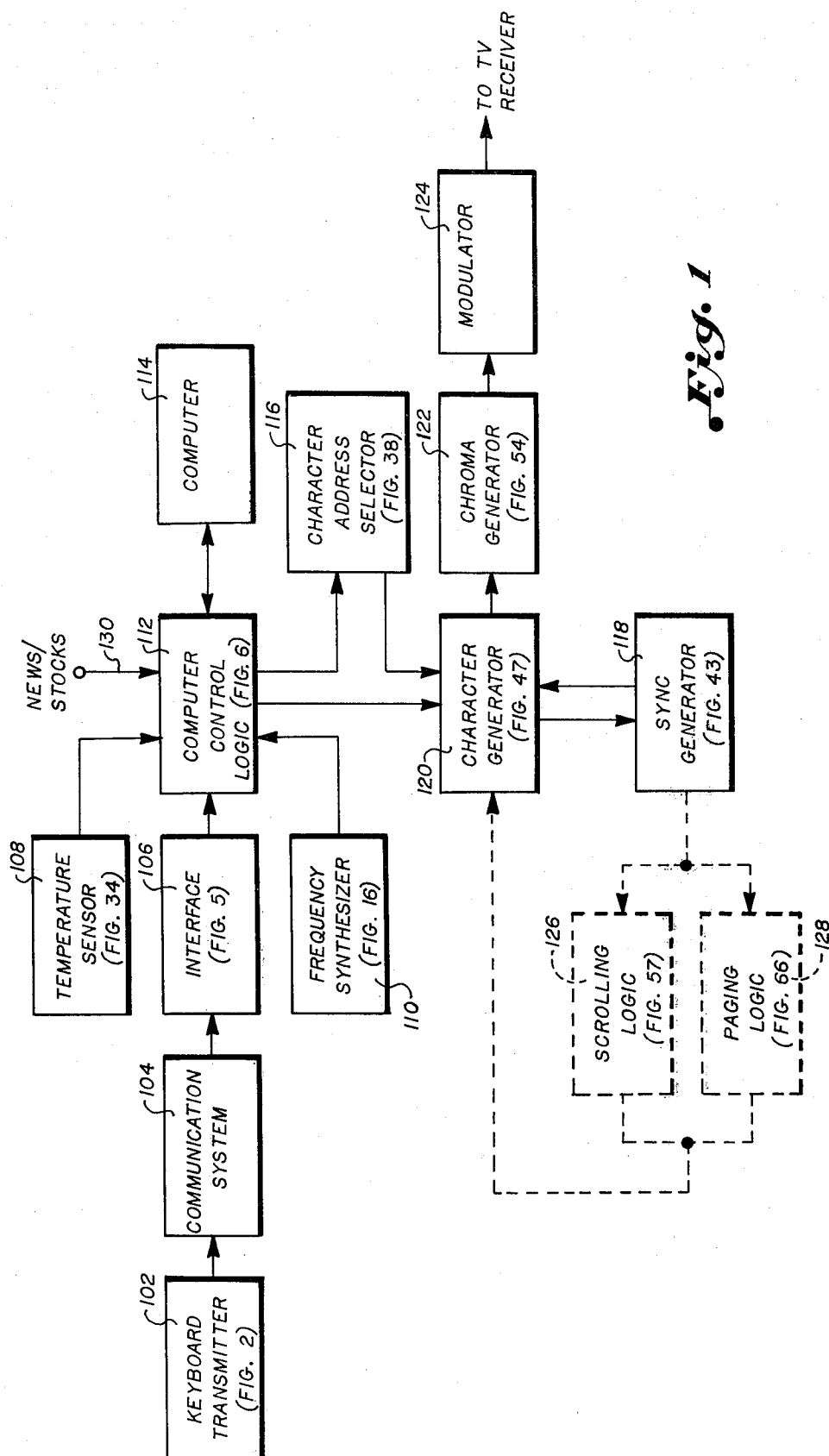


Fig. 1

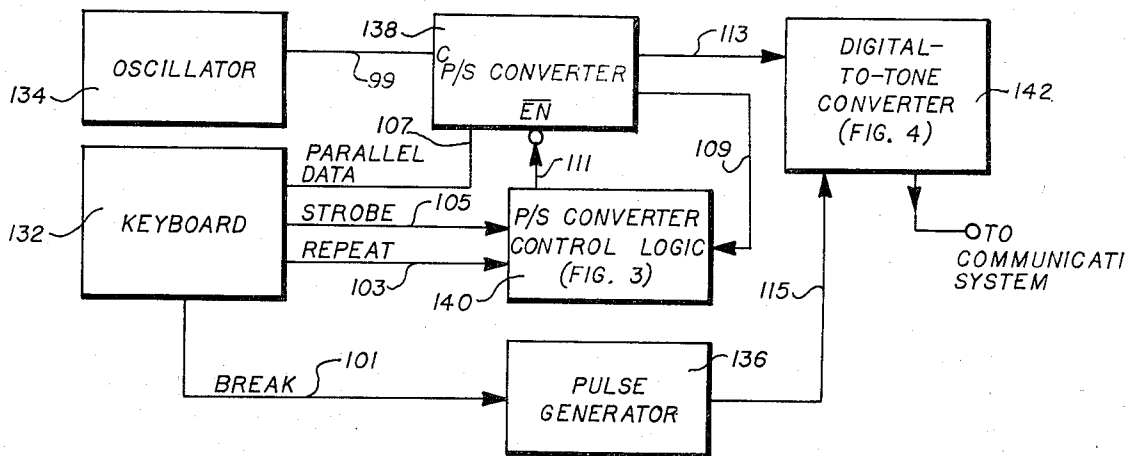


Fig. 2

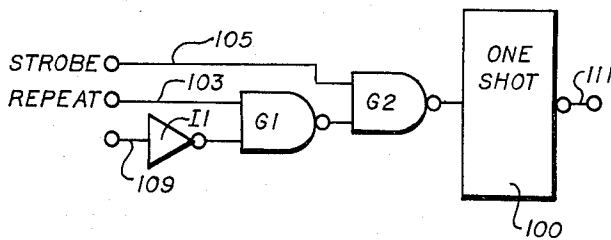


Fig. 3

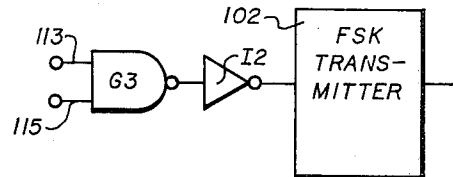


Fig. 4

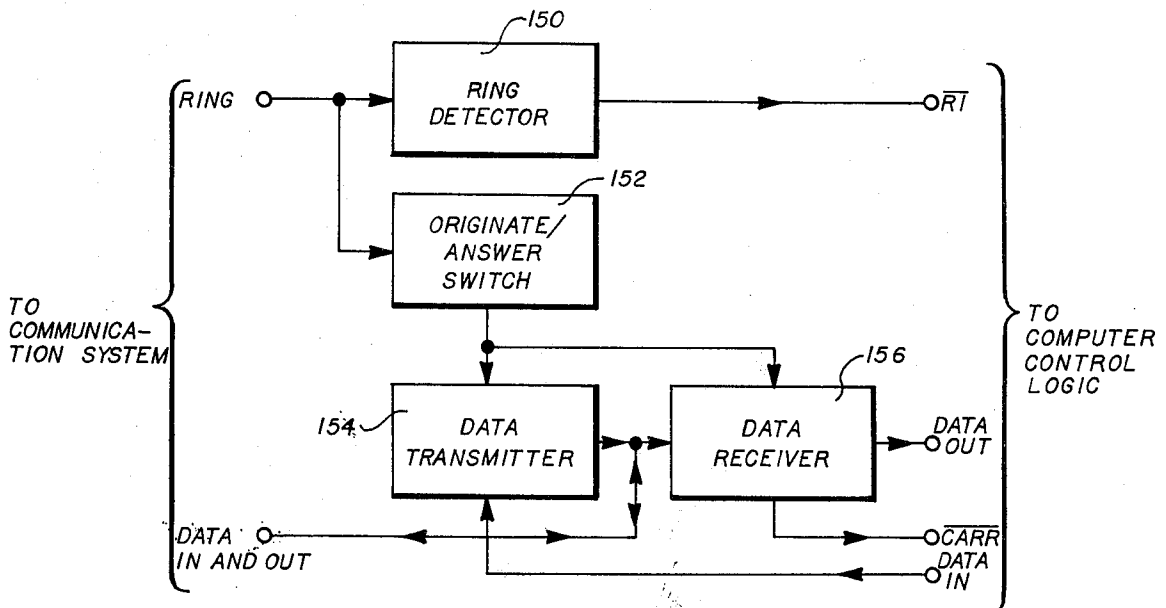
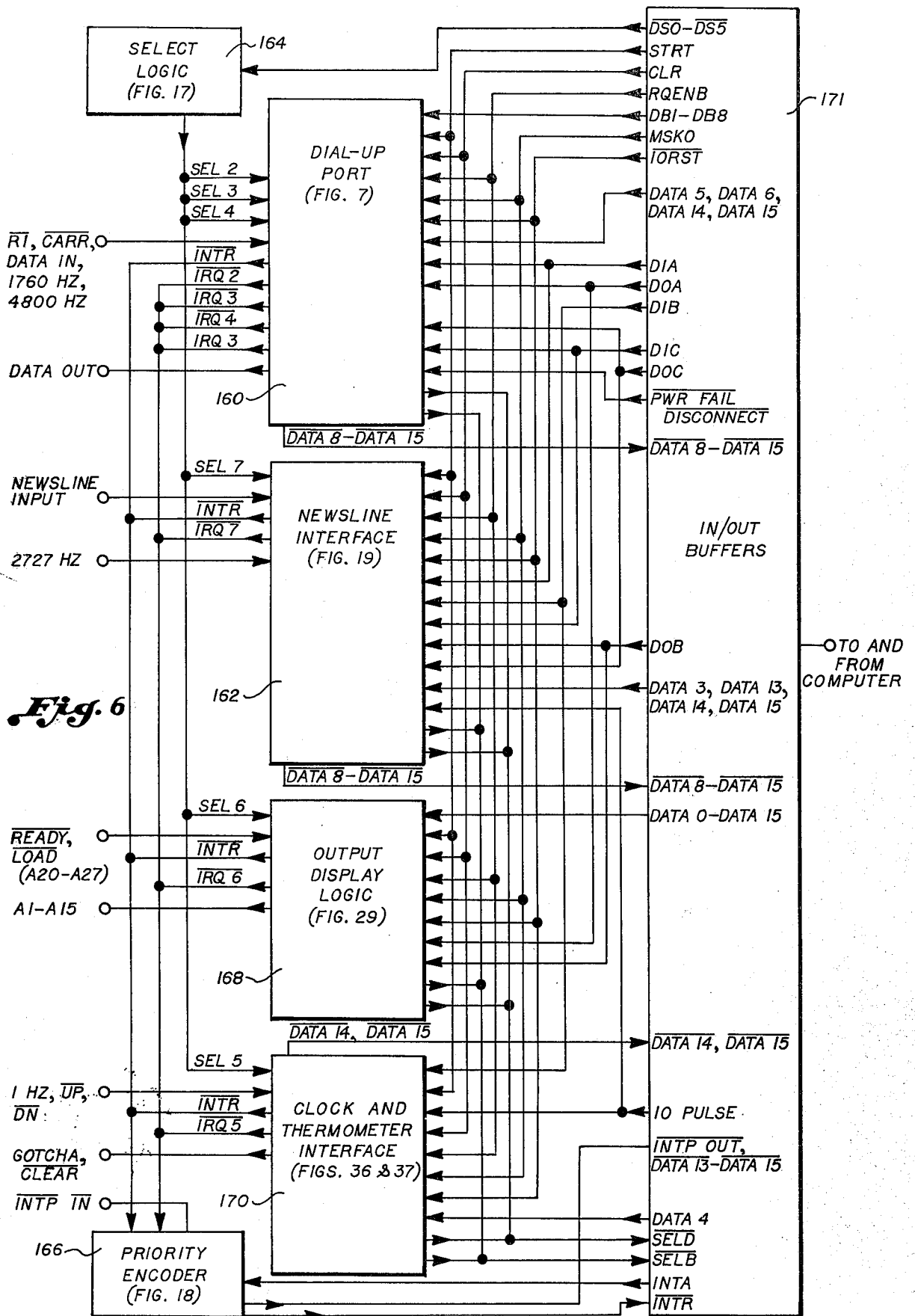


Fig. 5



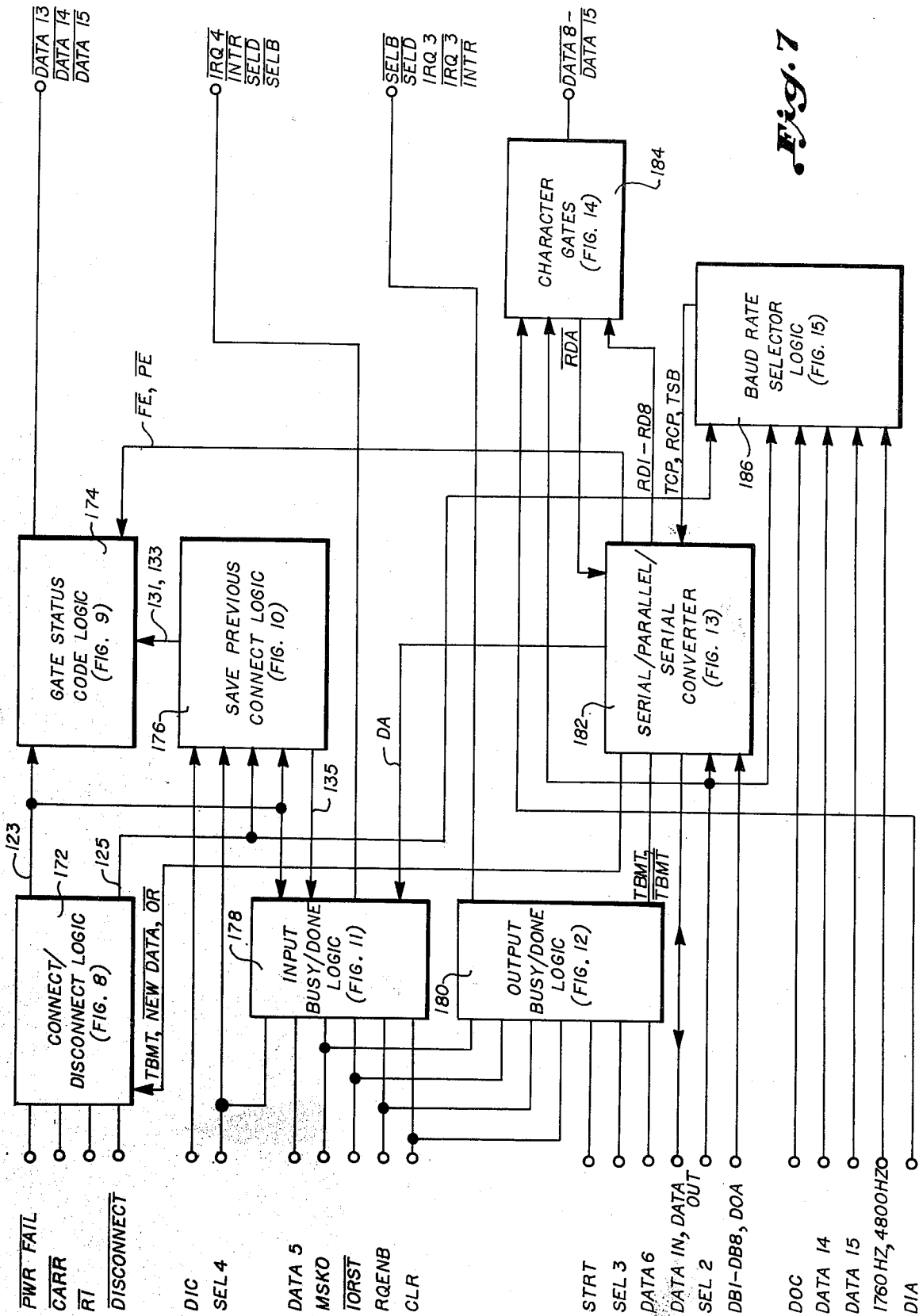


Fig. 7

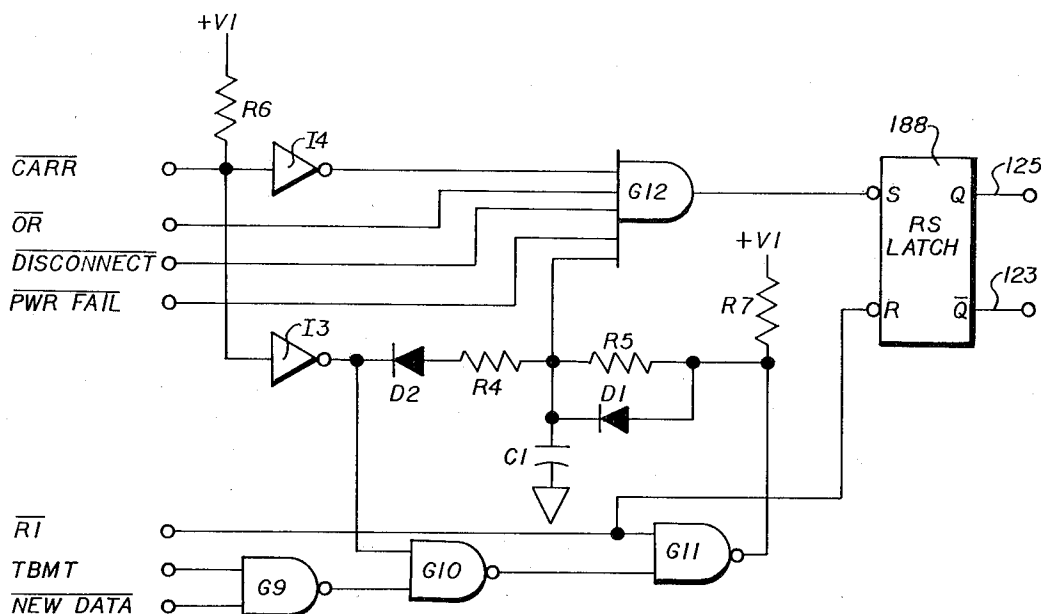


Fig. 8

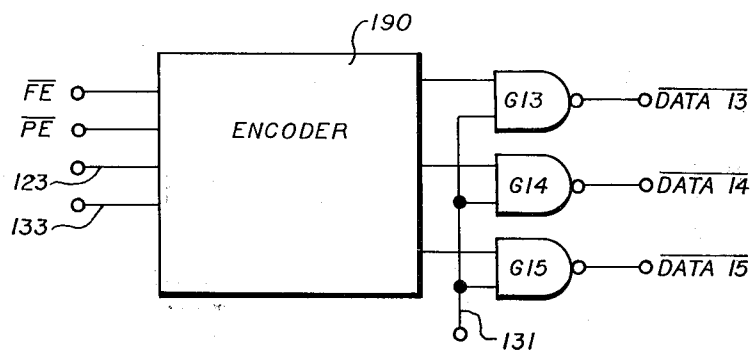


Fig. 9

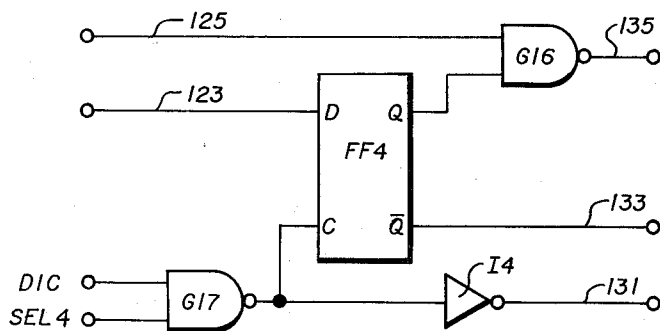


Fig. 10

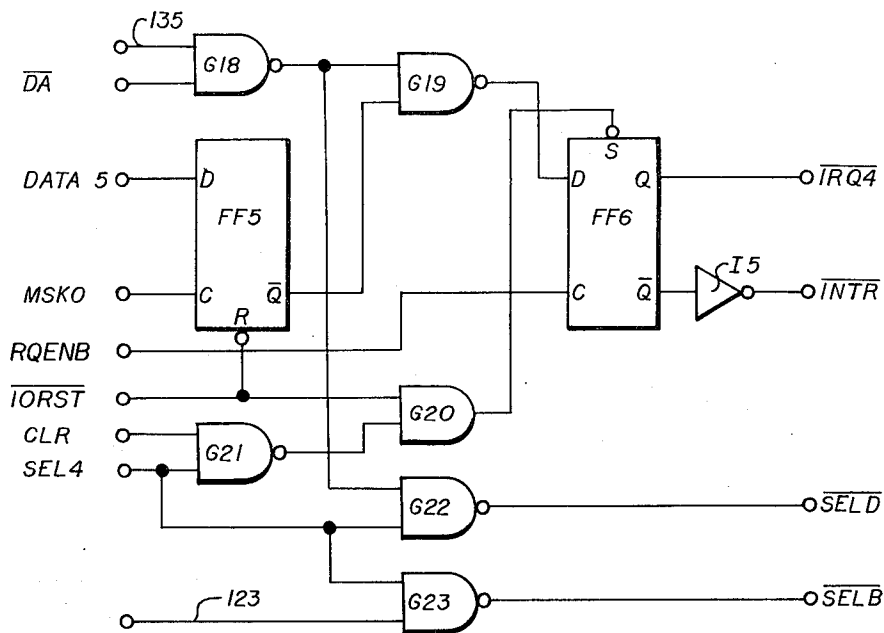


Fig. 11

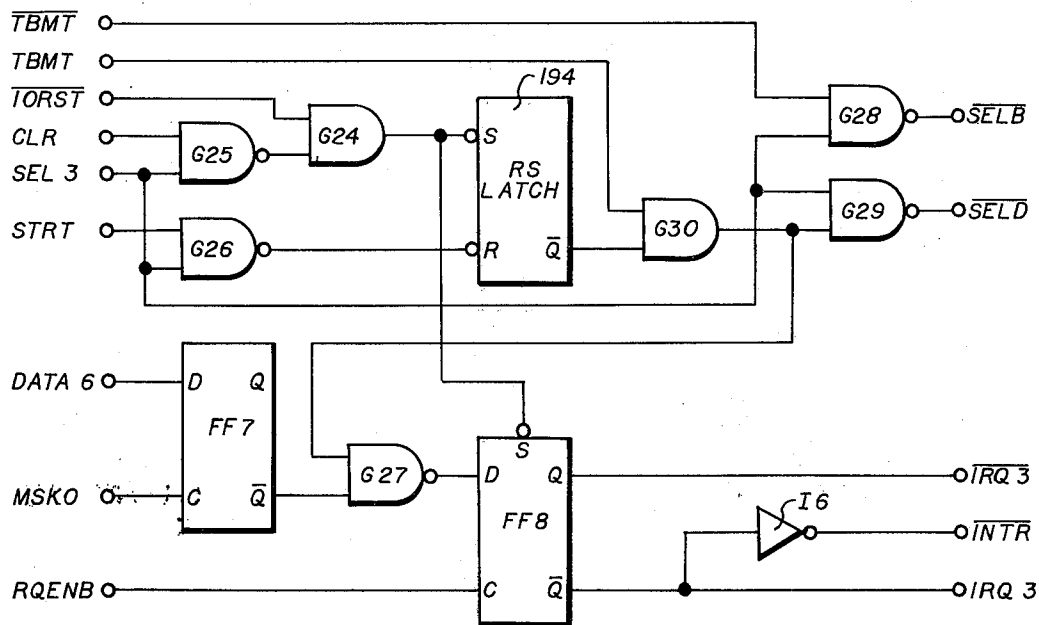


Fig. 12

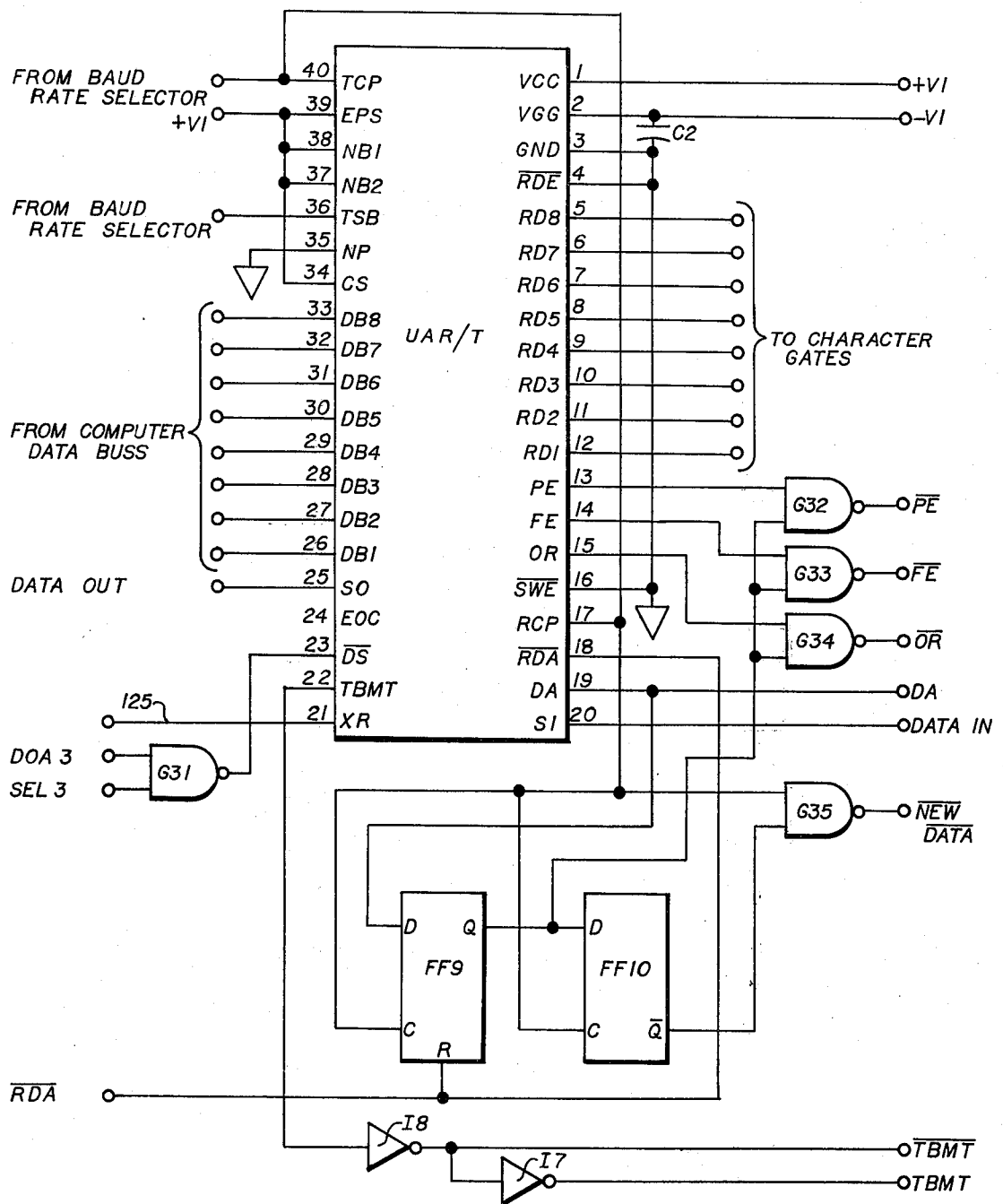


Fig. 13

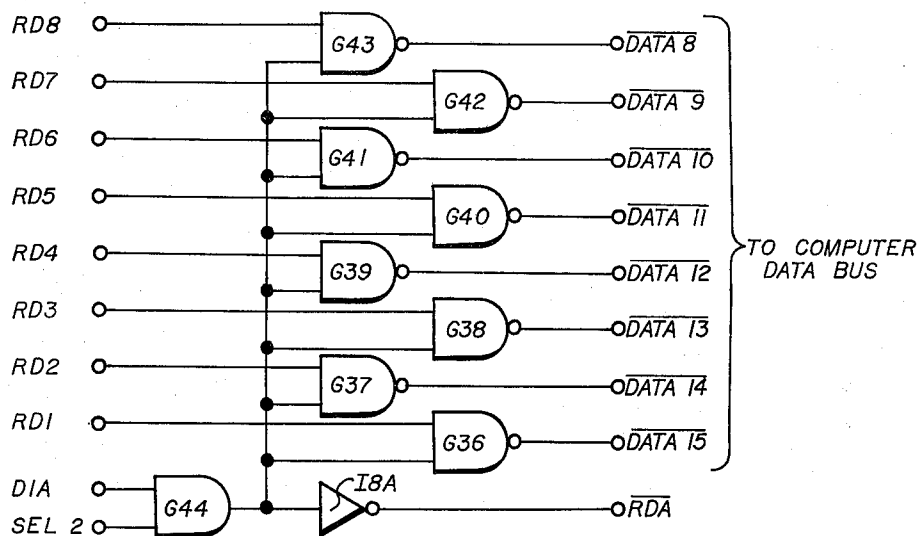


Fig. 14

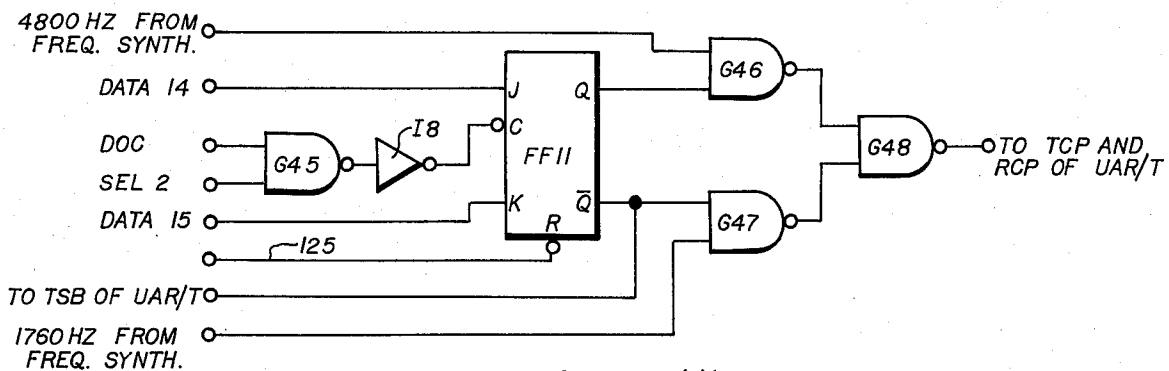


Fig. 15

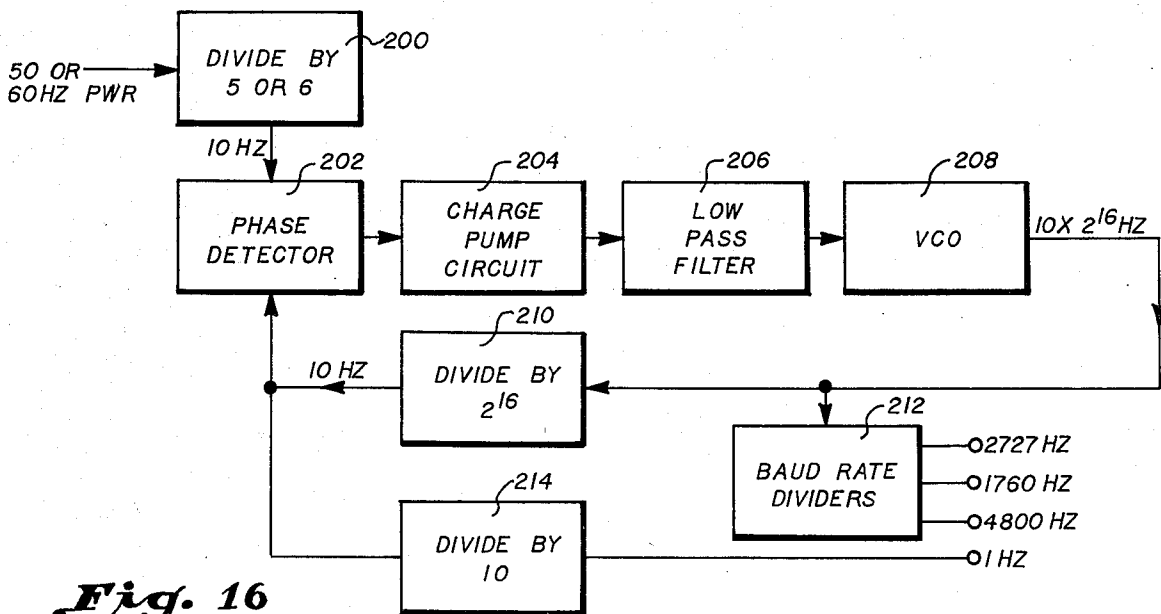
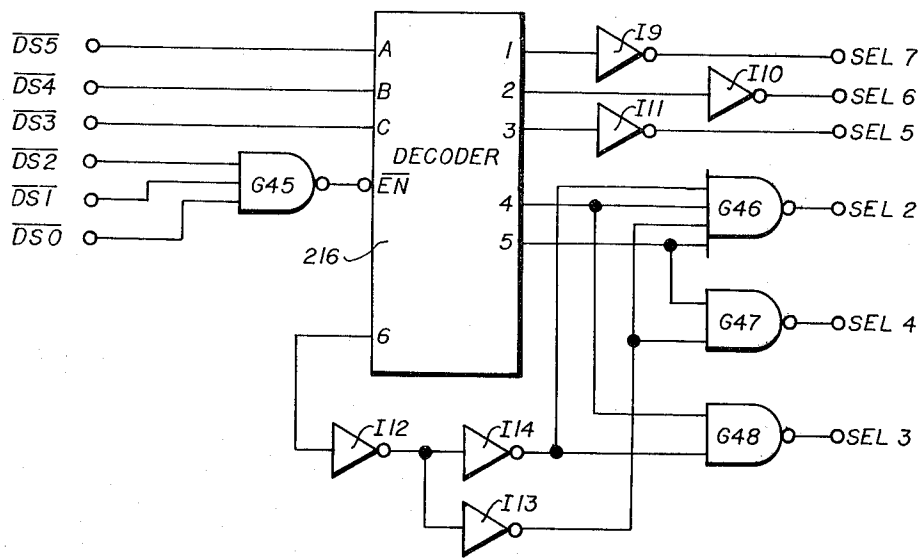
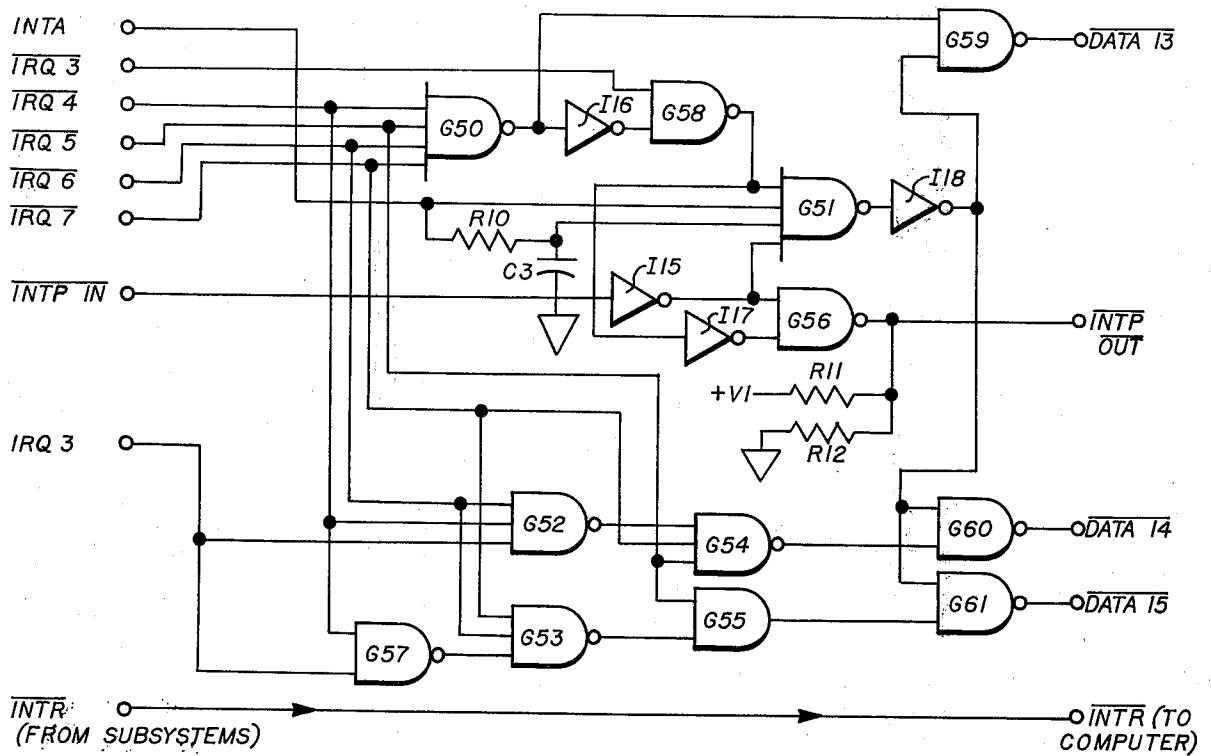
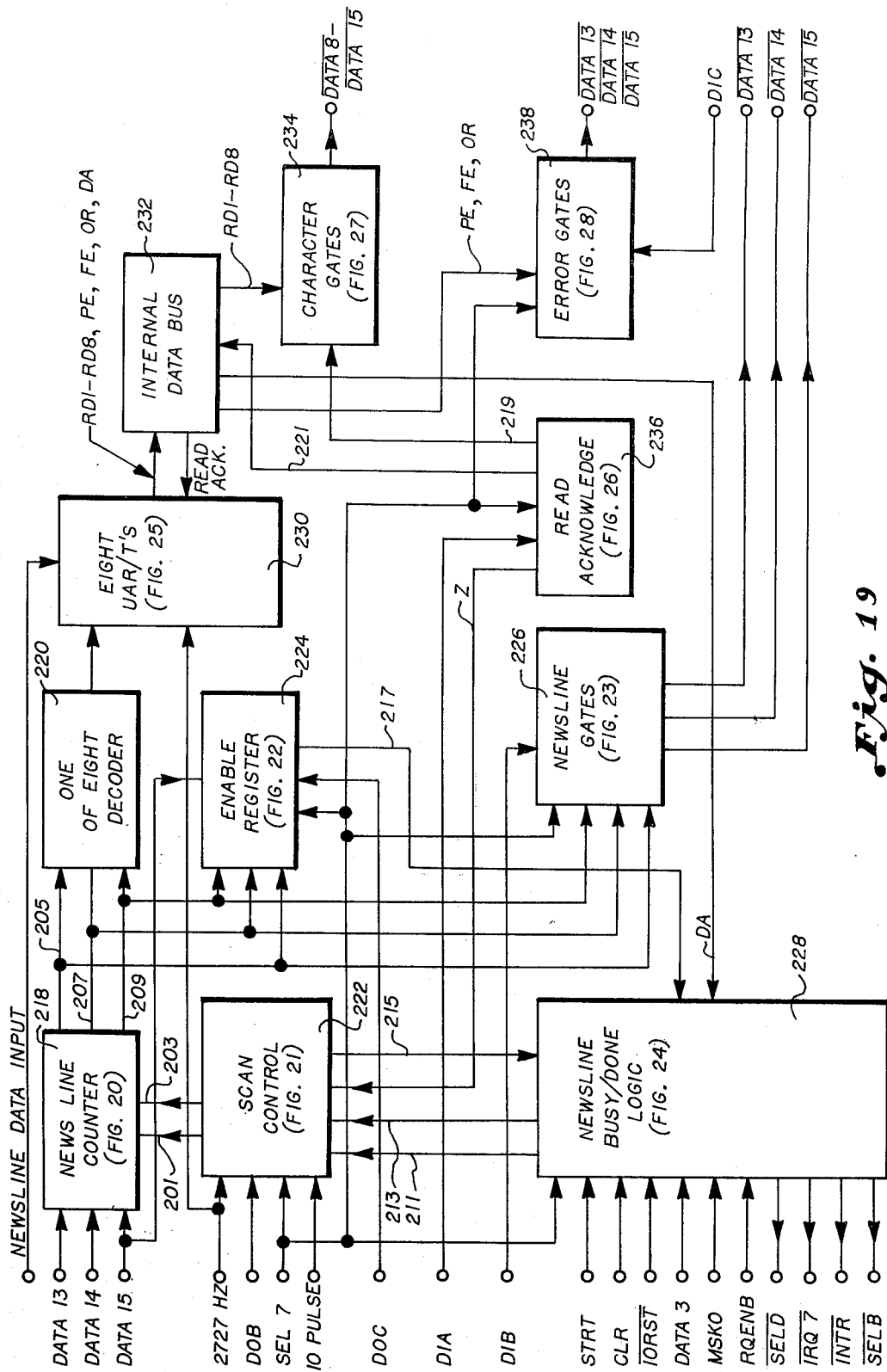


Fig. 16

*Fig. 17**Fig. 18*



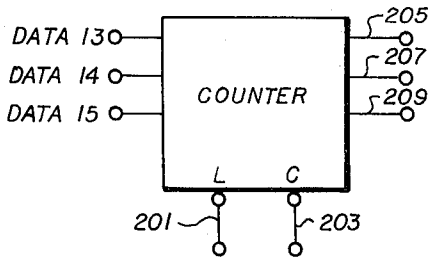


Fig. 20

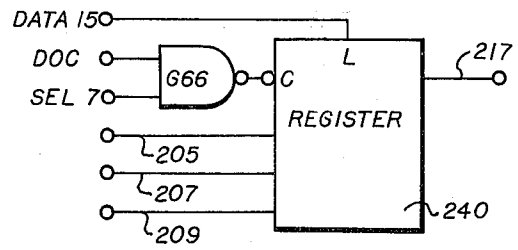


Fig. 22

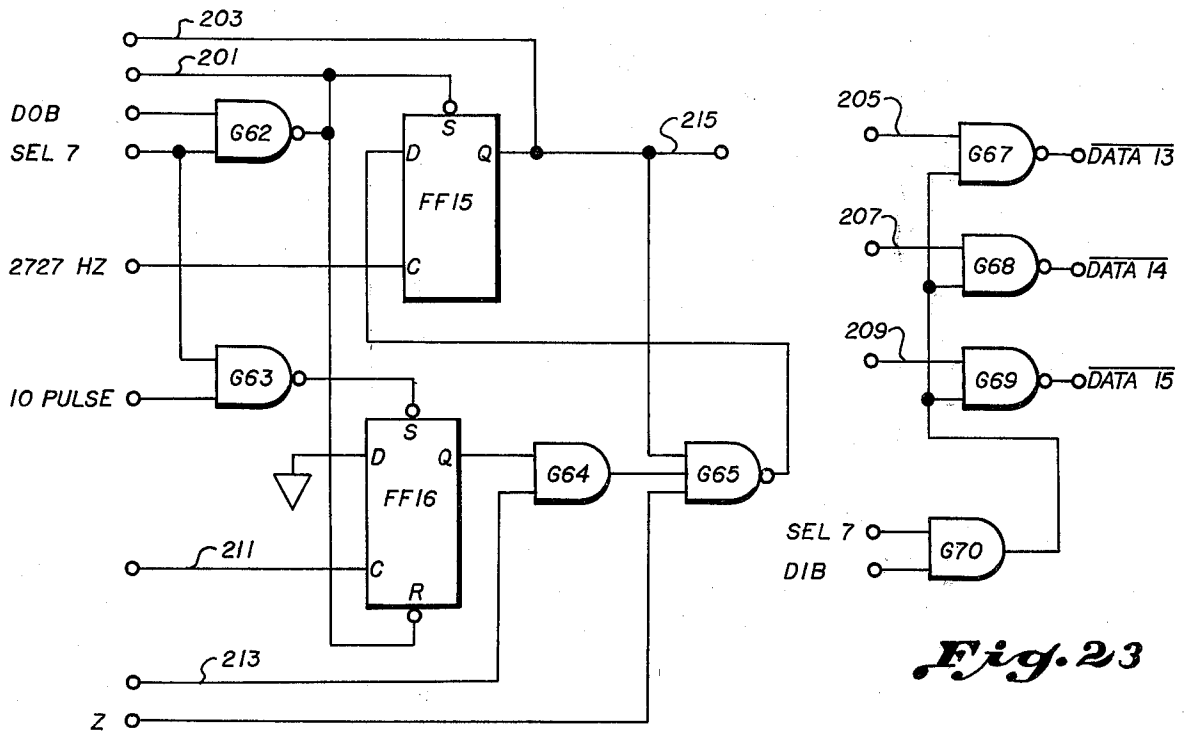


Fig. 21

Fig. 23

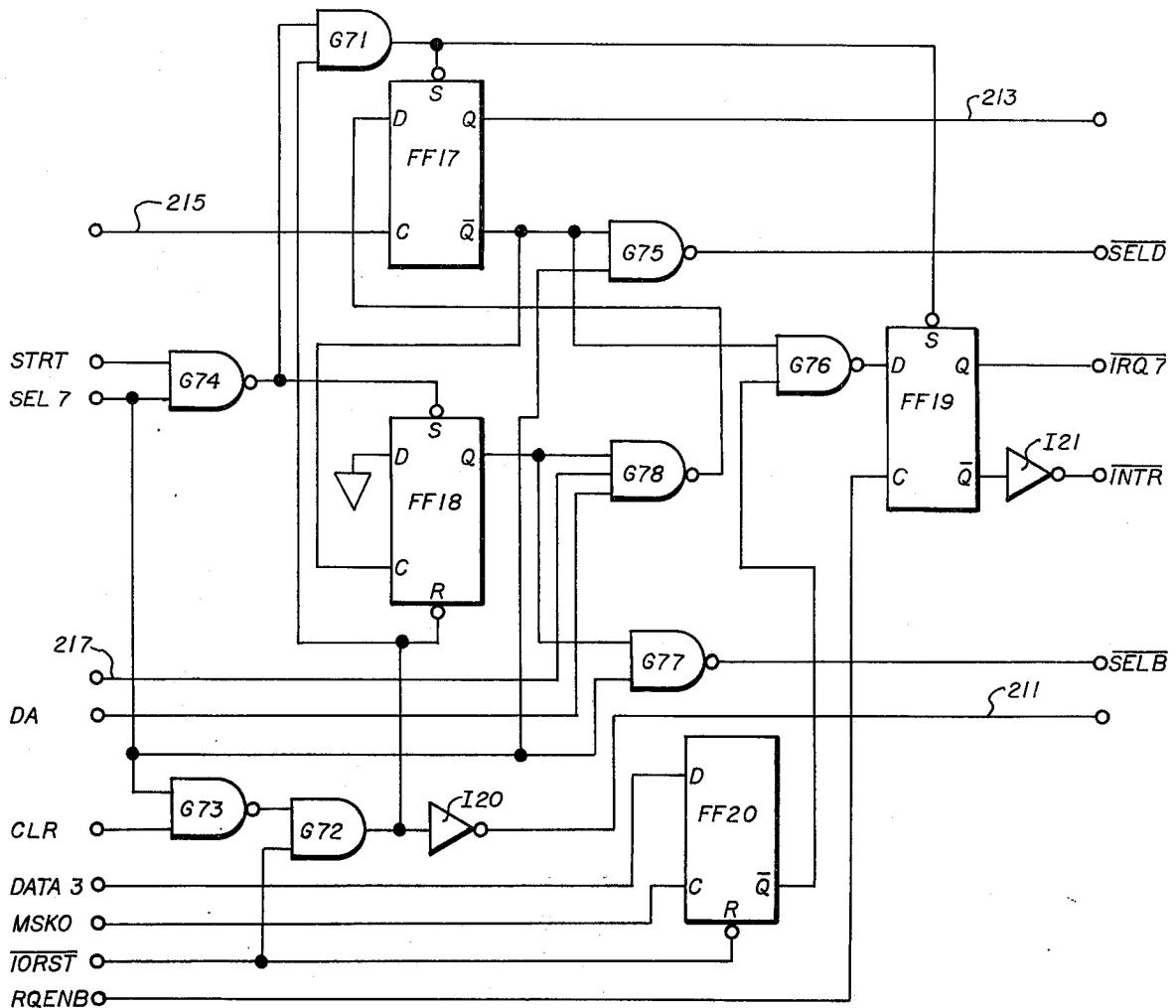
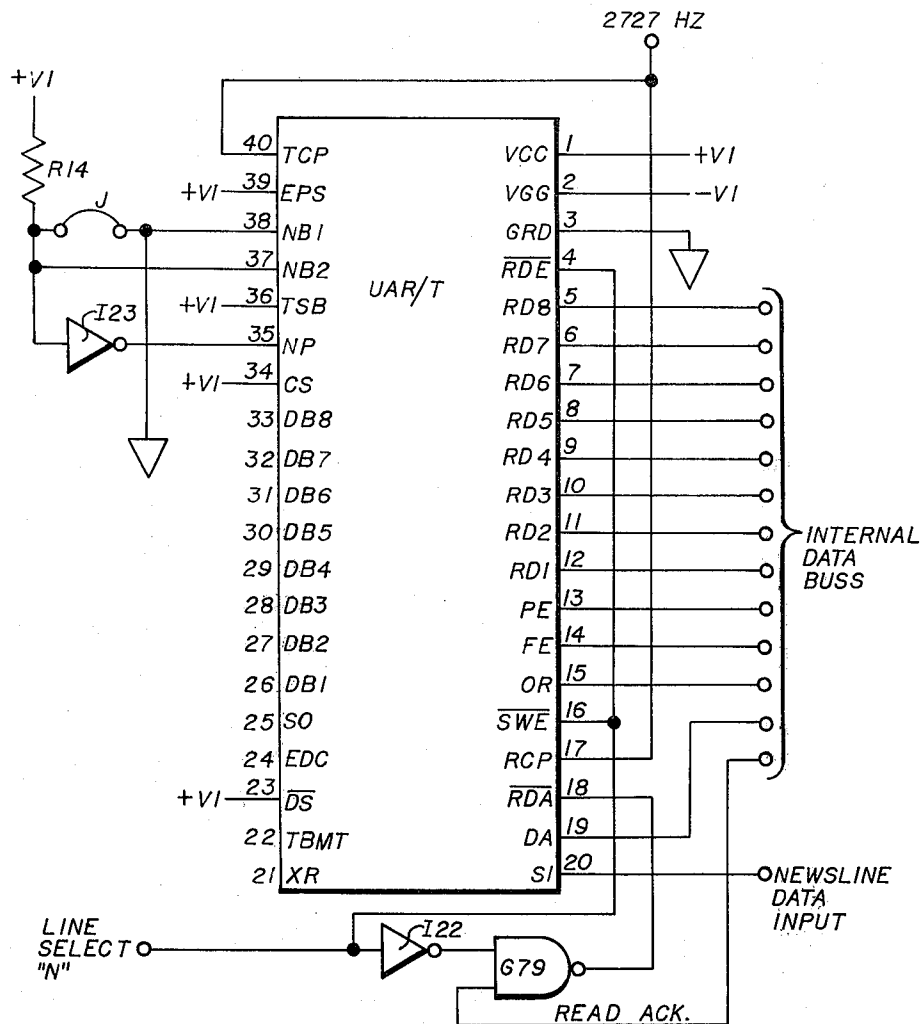
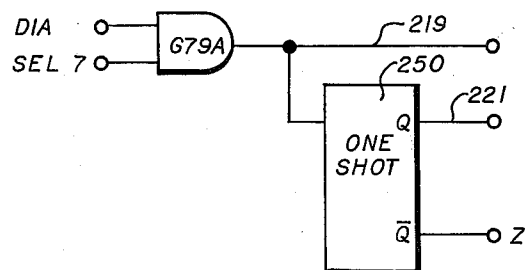


Fig. 24

*Fig. 25**Fig. 26*

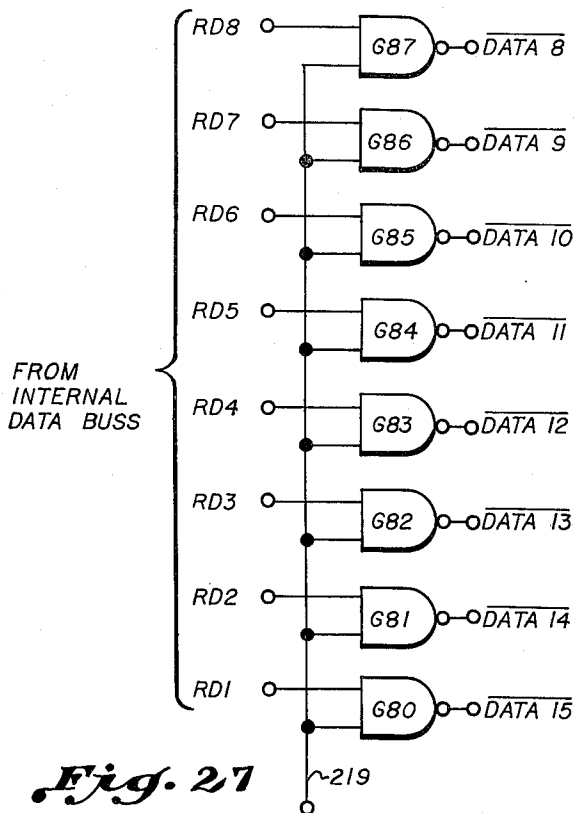


Fig. 27

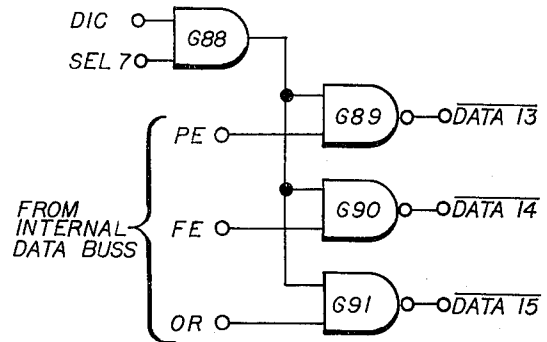


Fig. 28

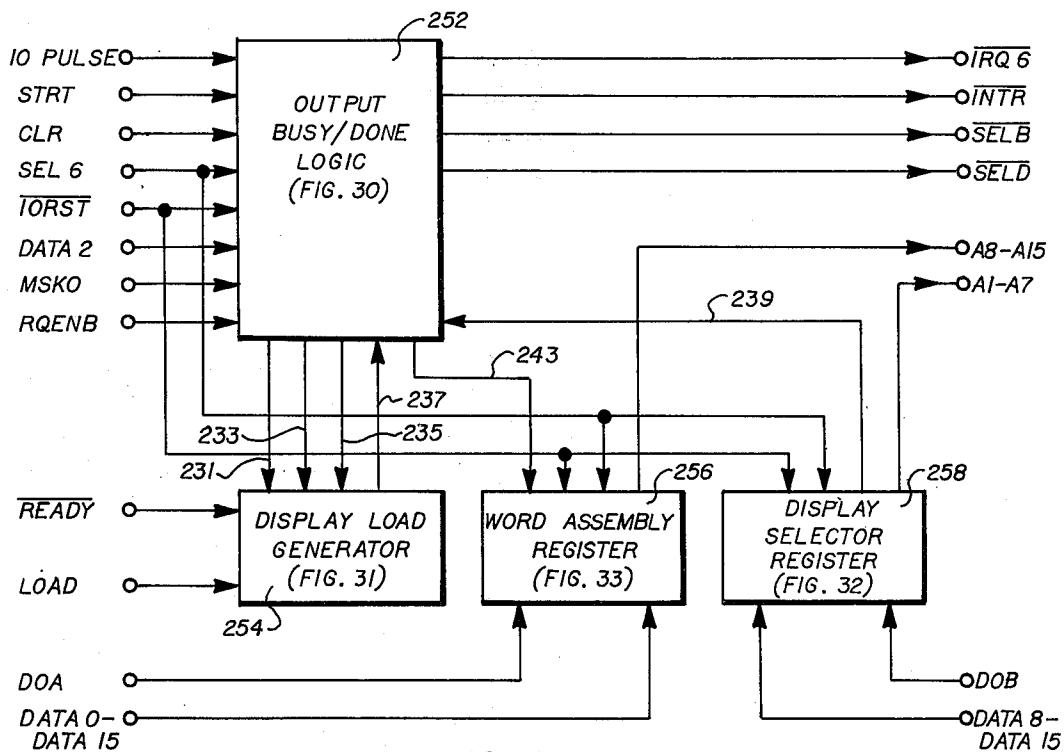
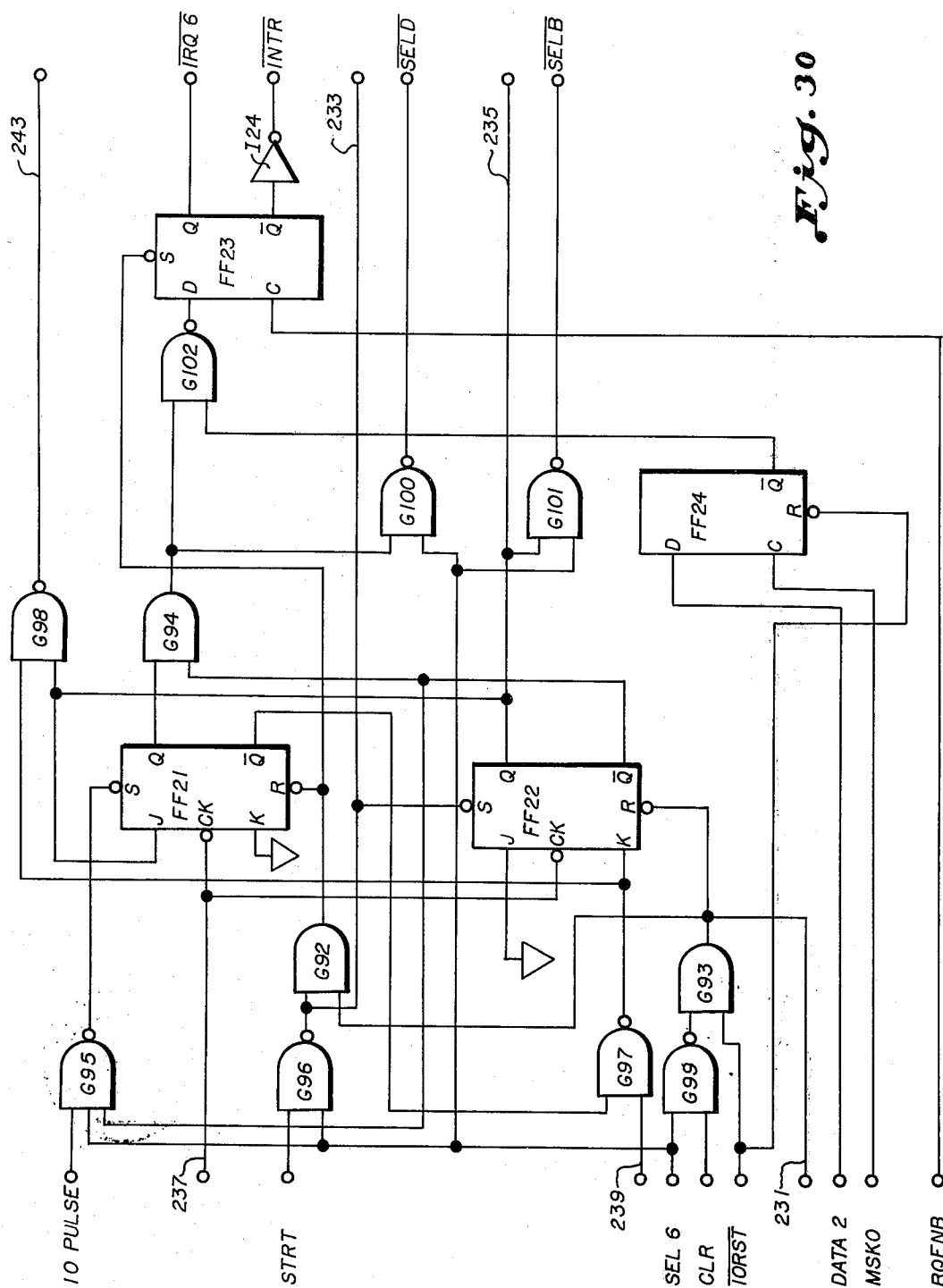


Fig. 29



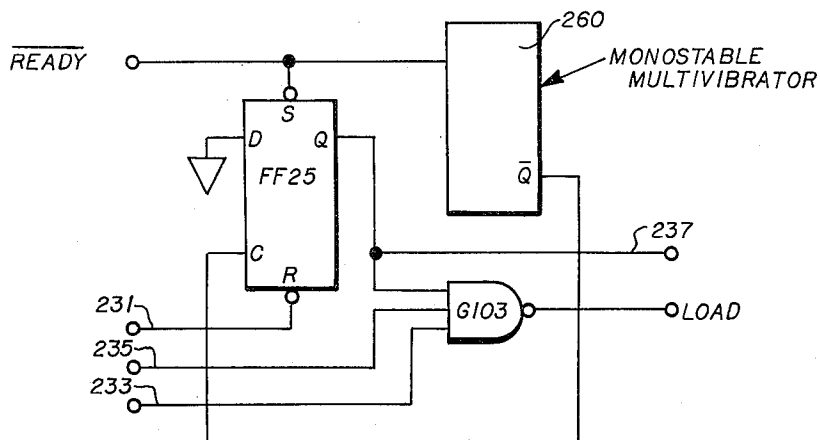


Fig. 31

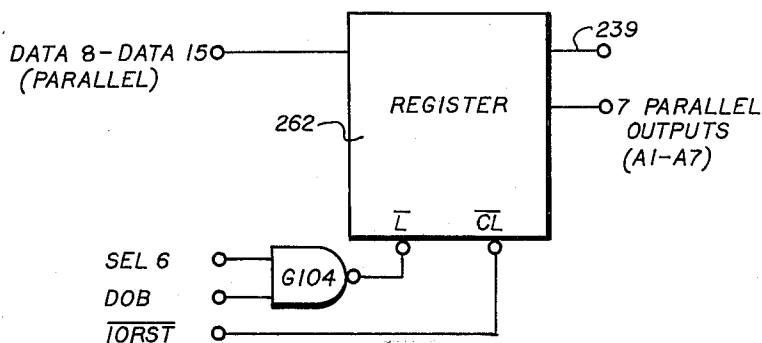


Fig. 32

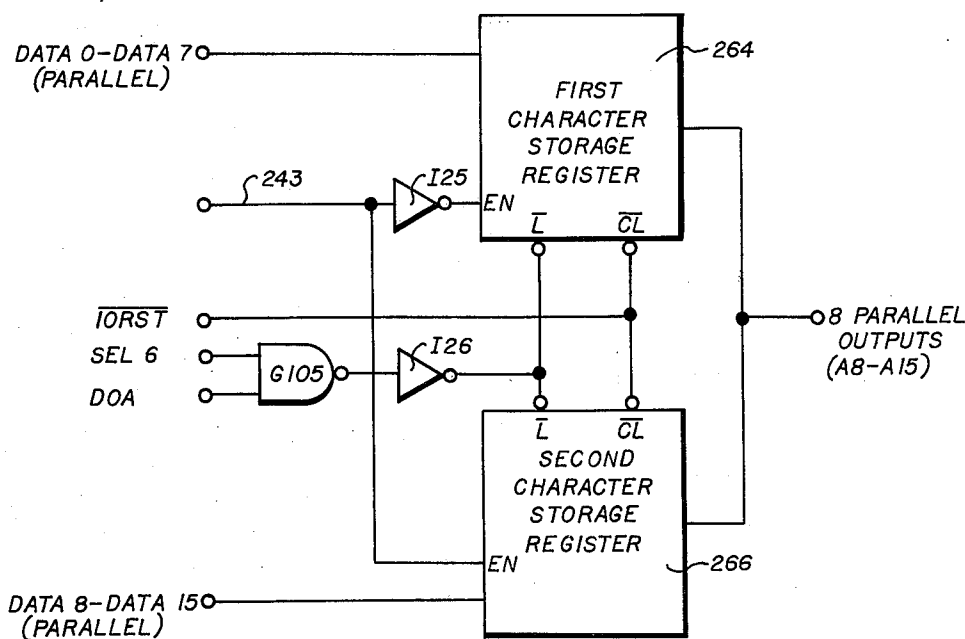


Fig. 33

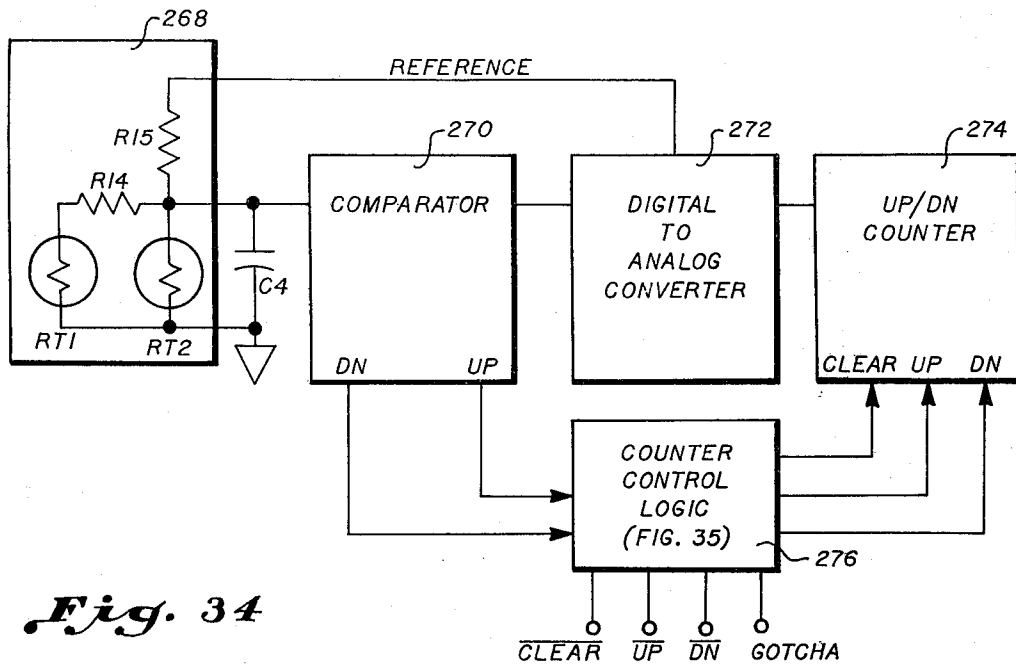


Fig. 34

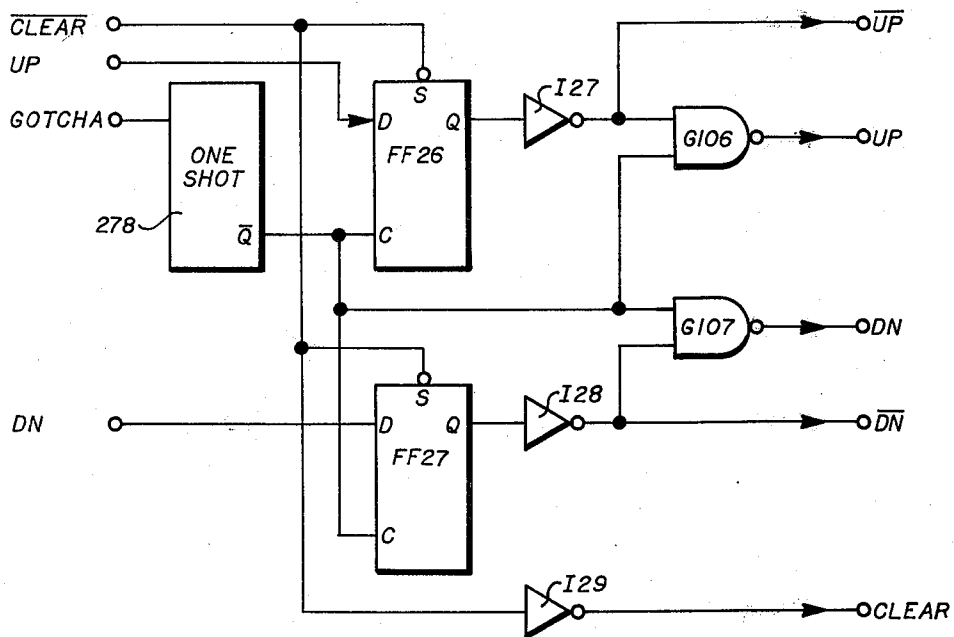


Fig. 35

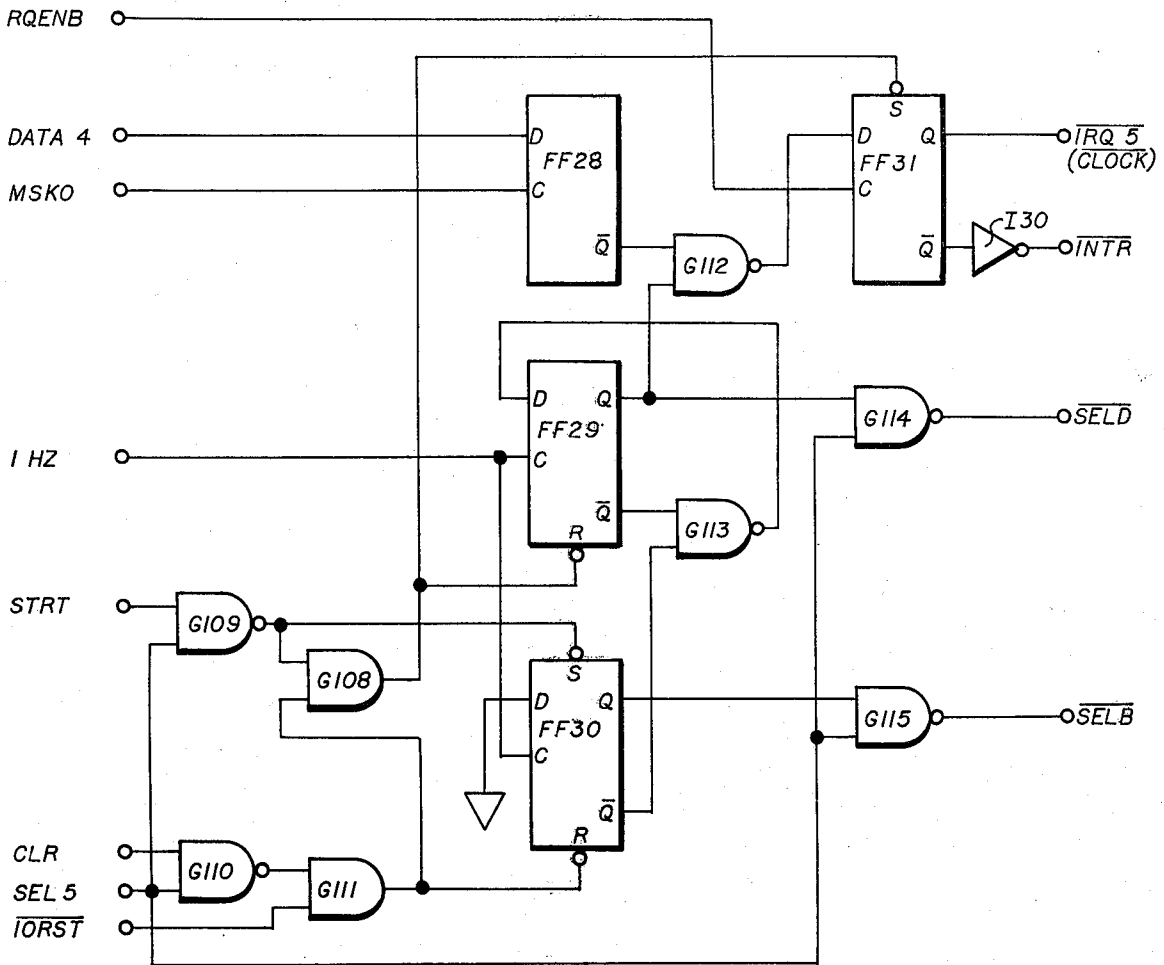


Fig. 36

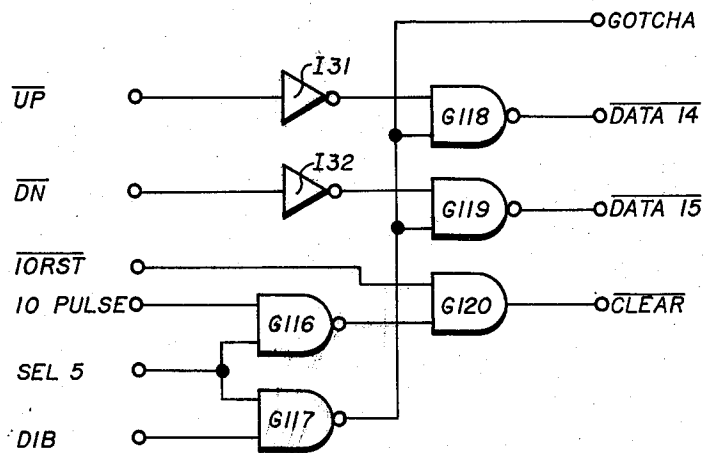


Fig. 37

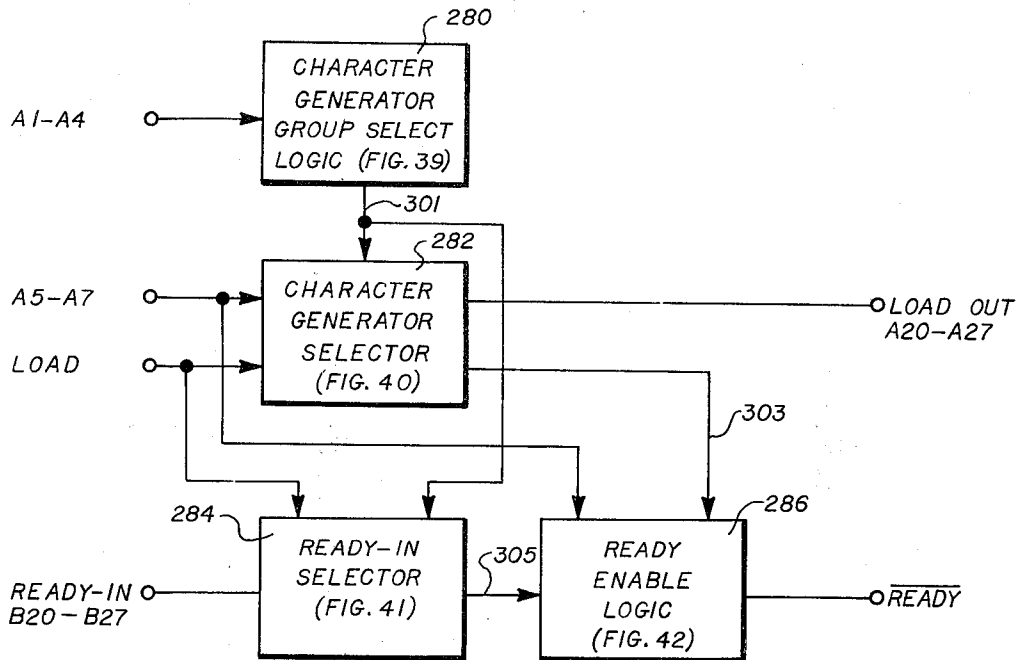


Fig. 38

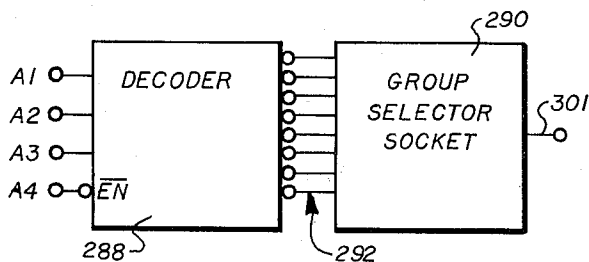


Fig. 39

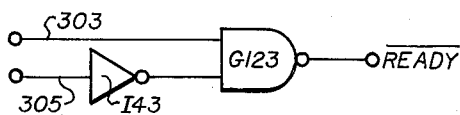


Fig. 42

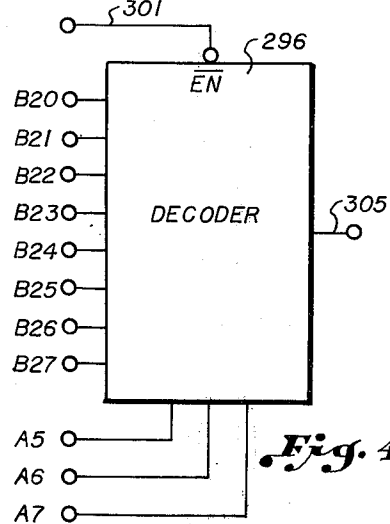


Fig. 41

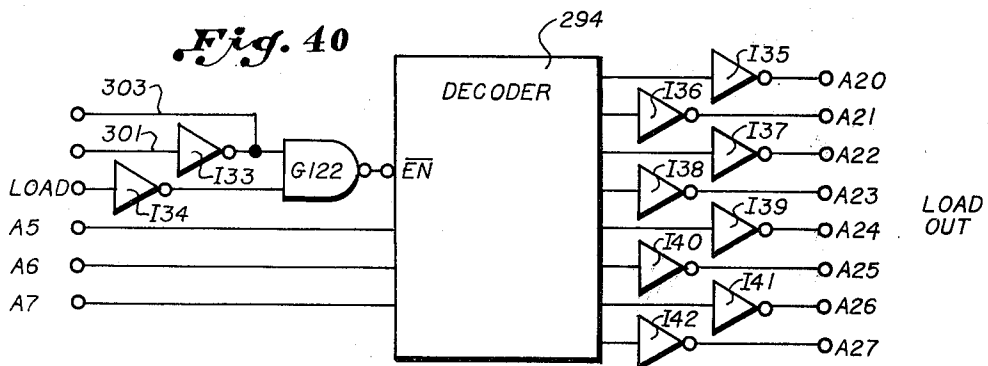
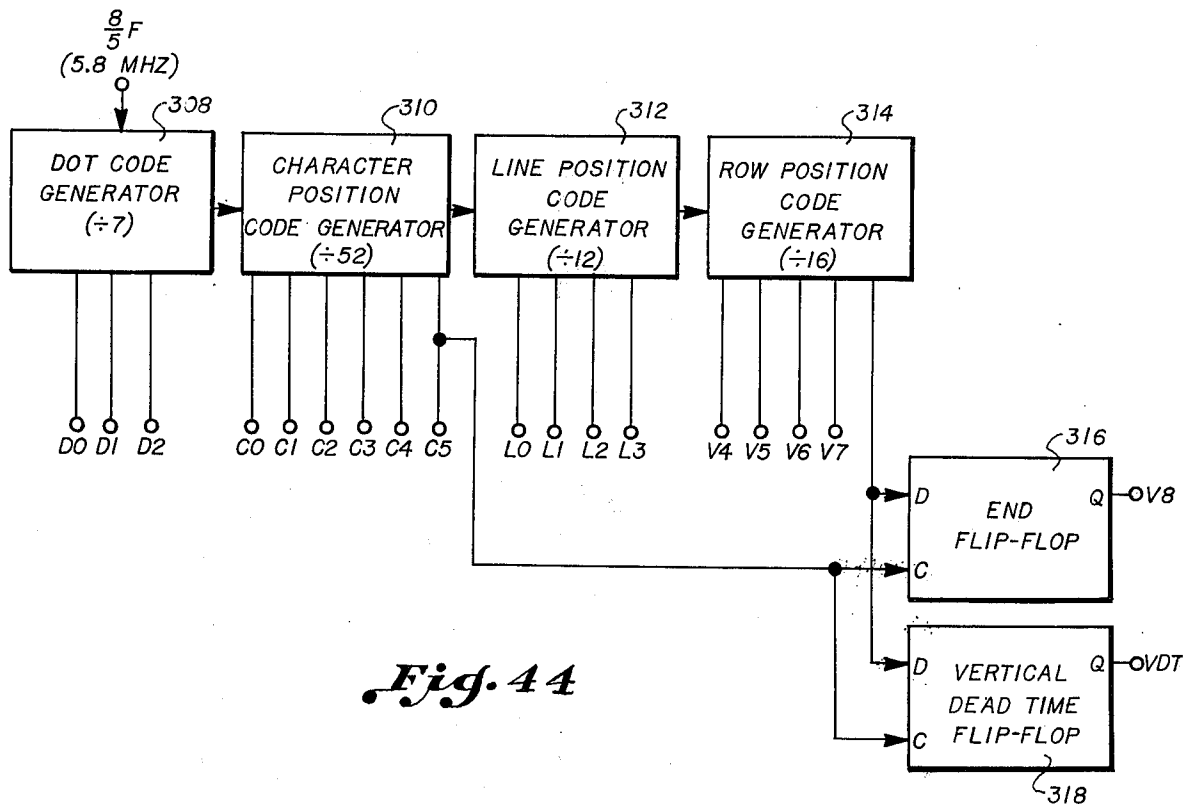
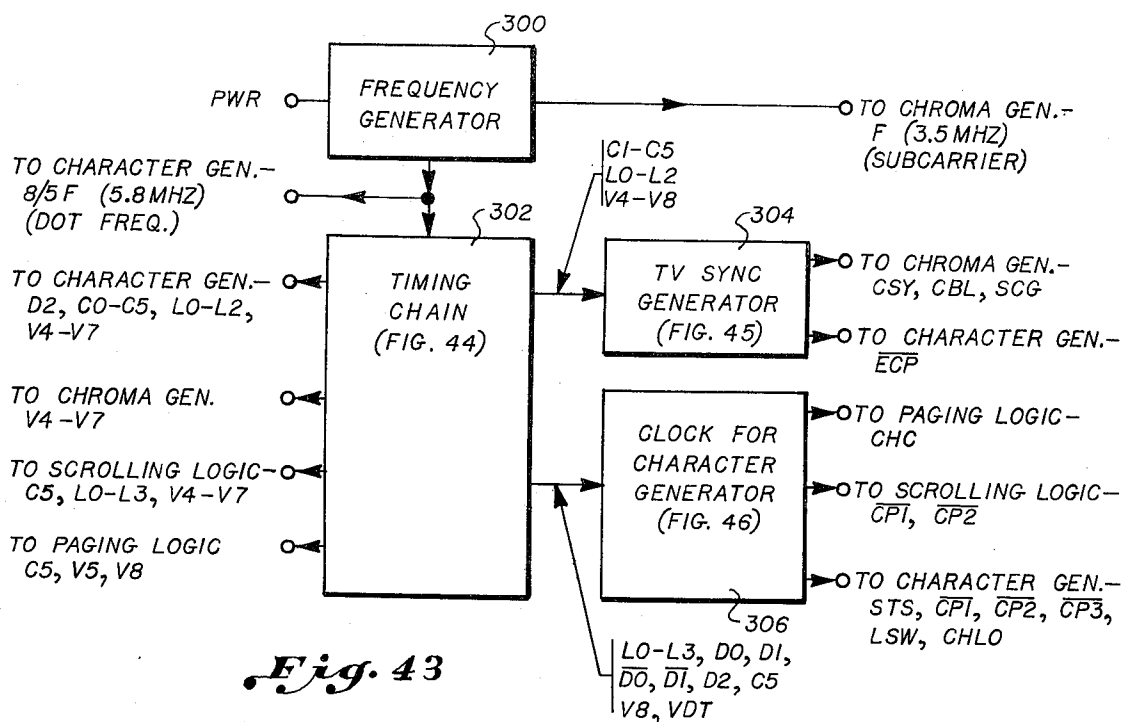


Fig. 40



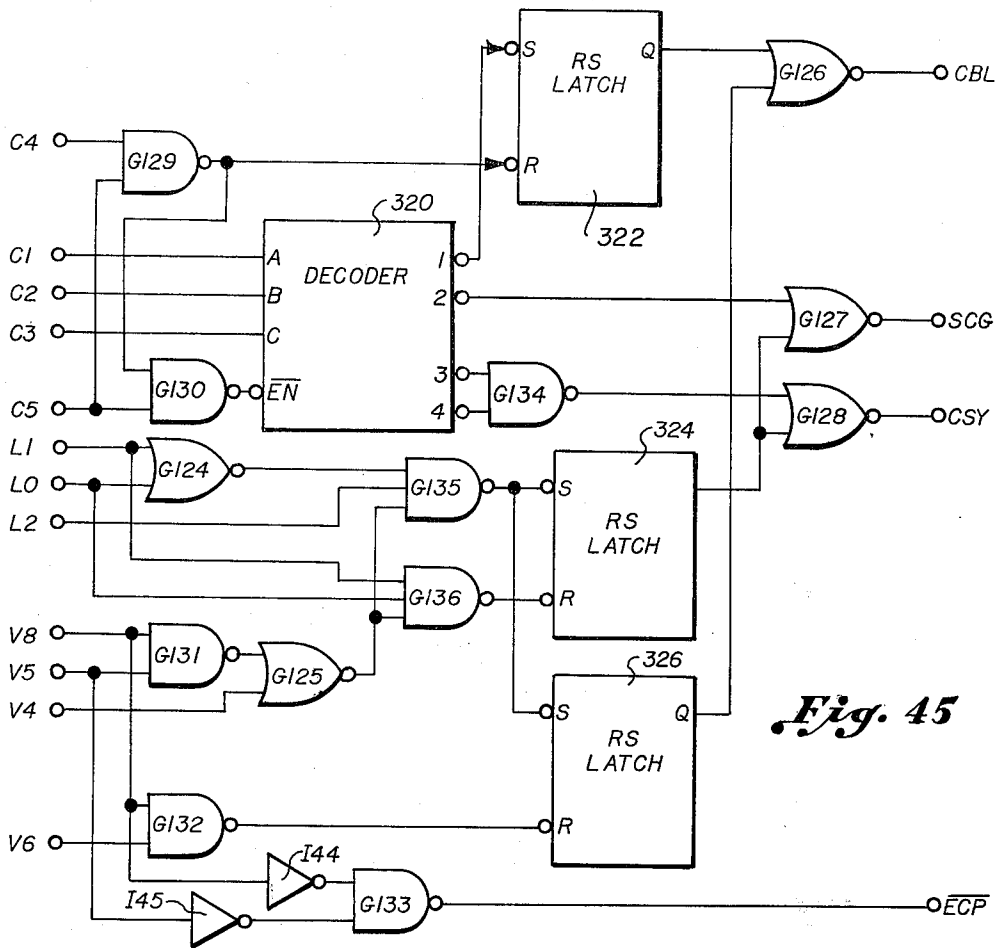


Fig. 45

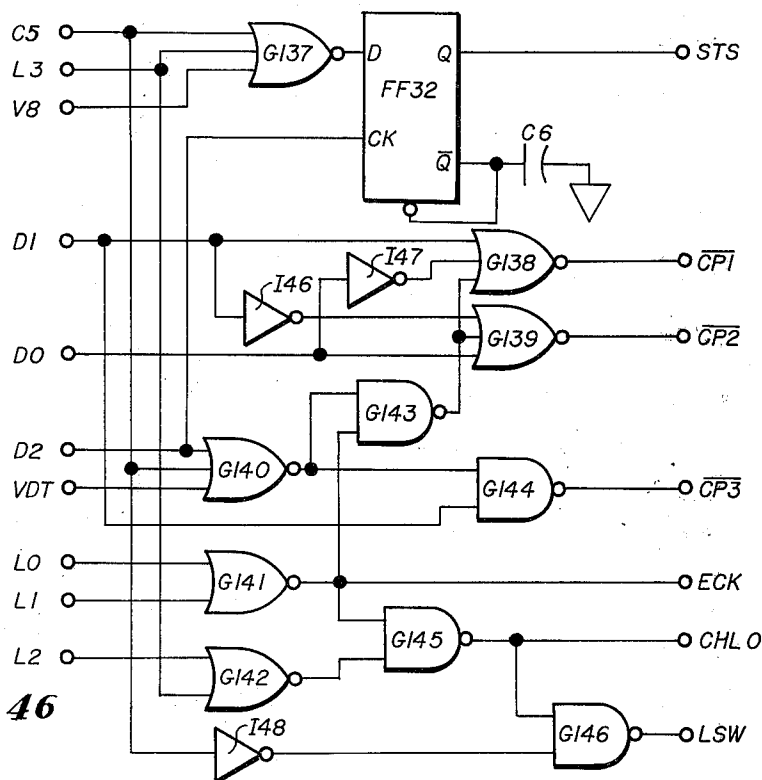


Fig. 46

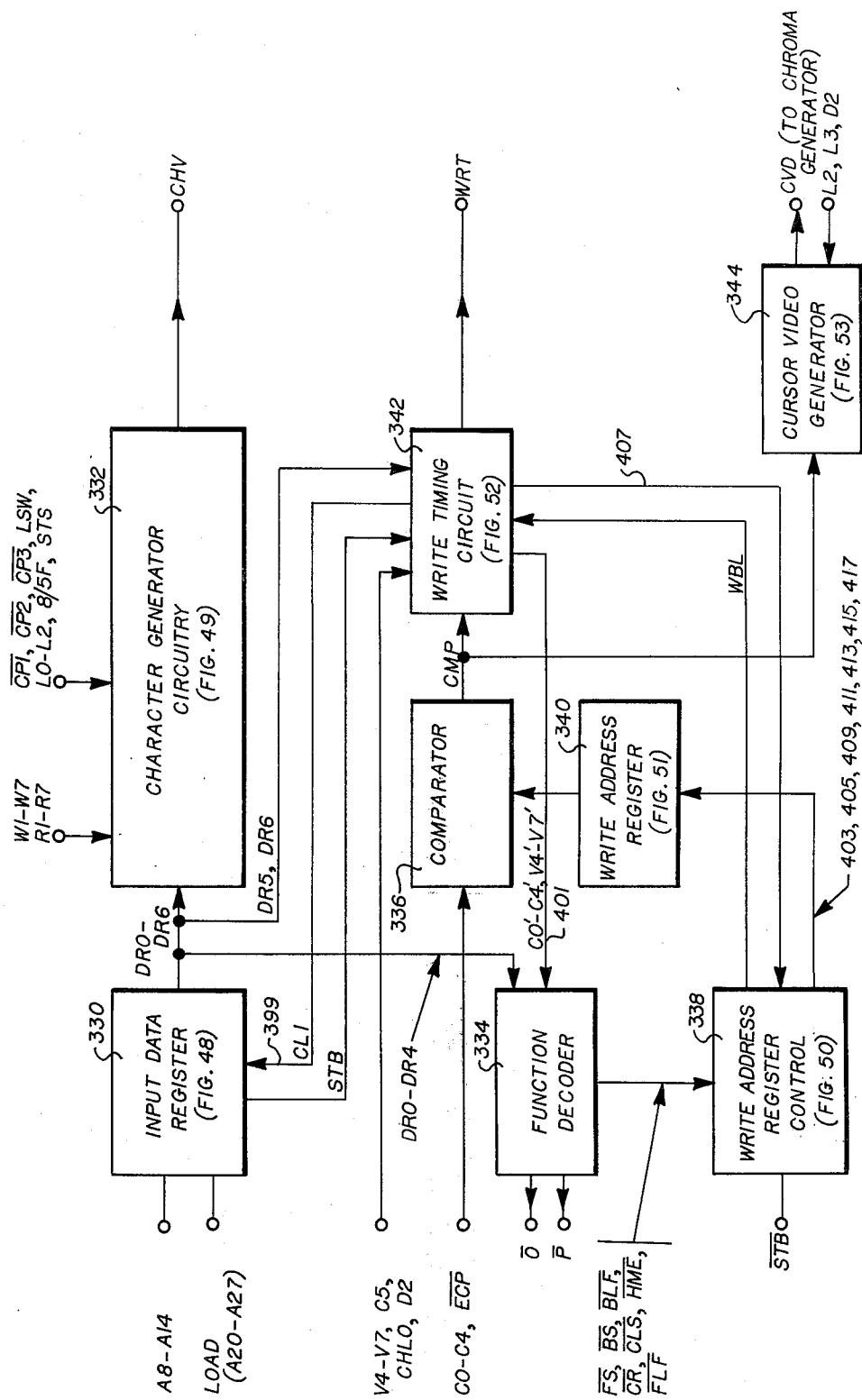


Fig. 47

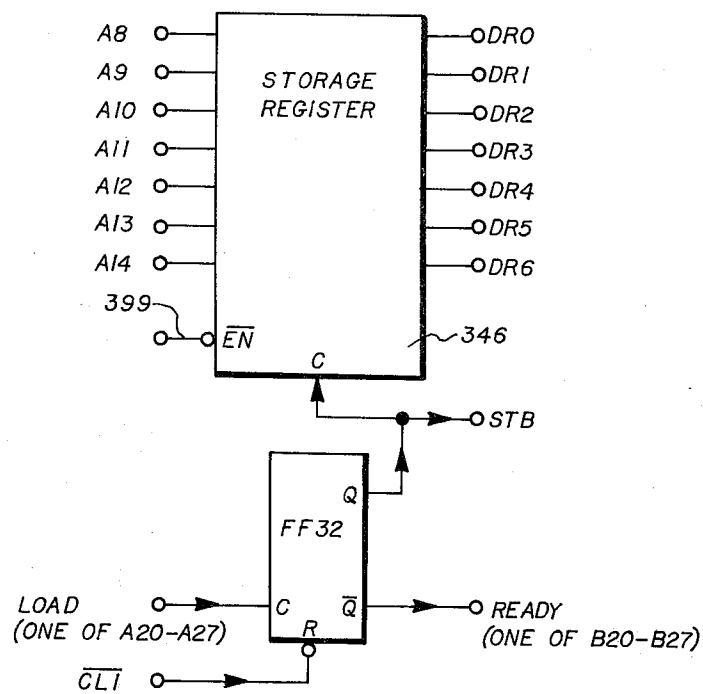


Fig. 48

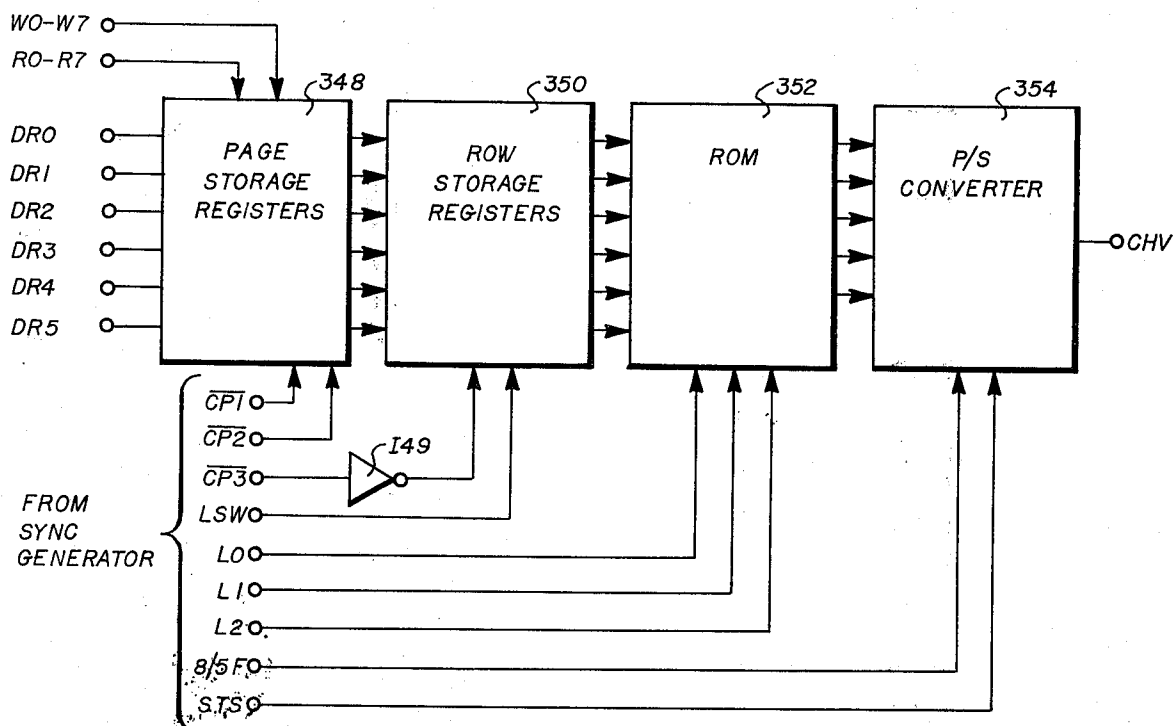


Fig. 49

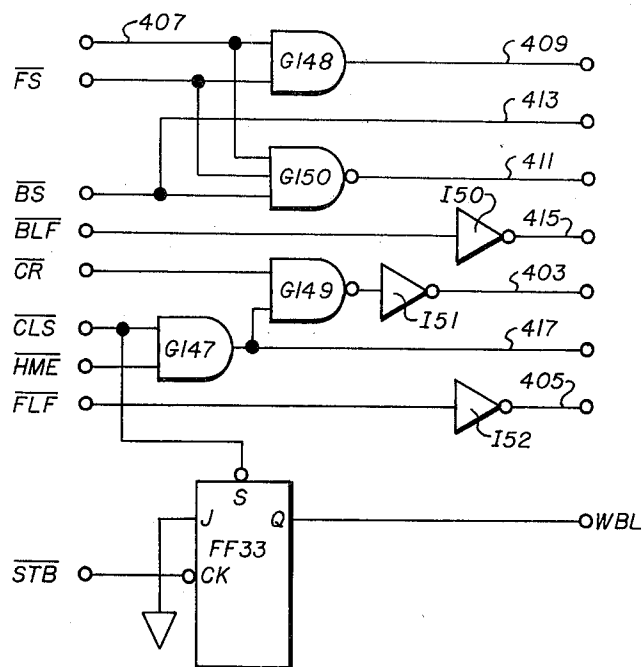
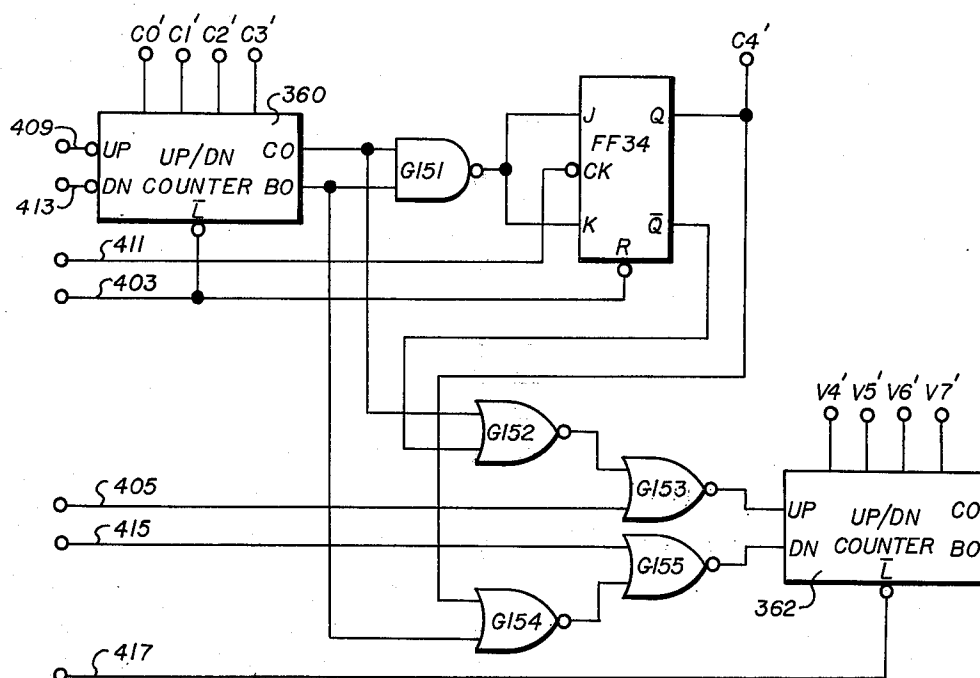
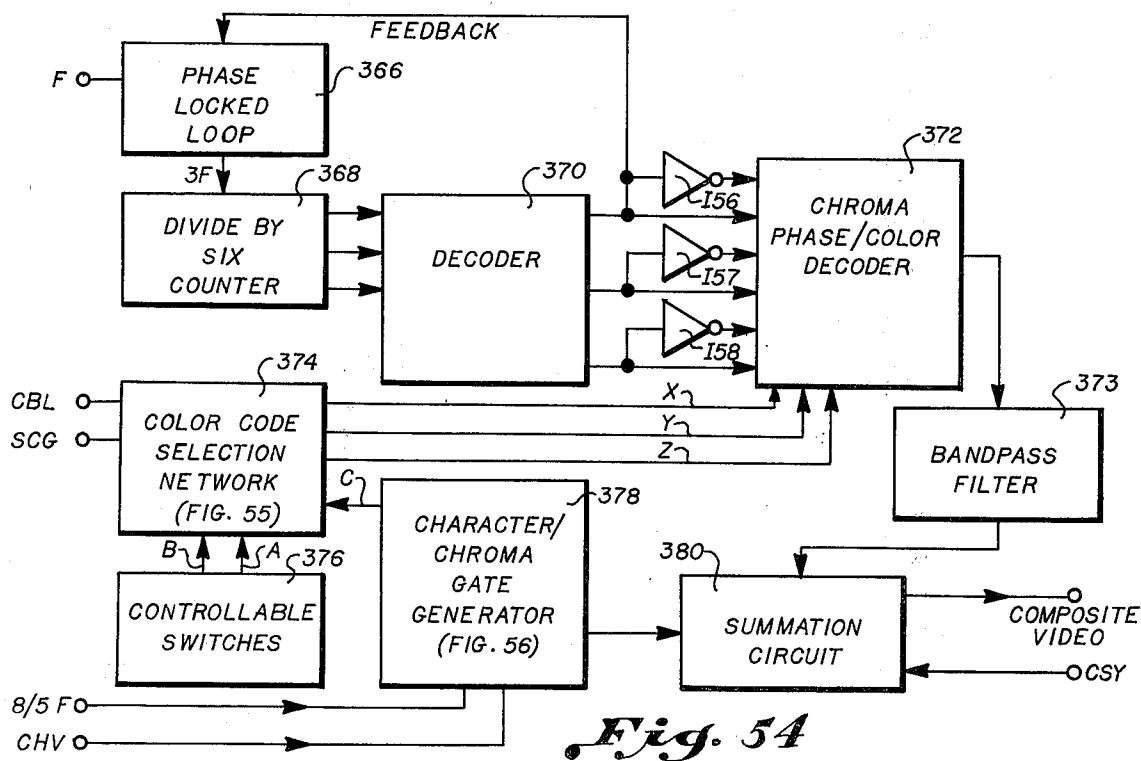
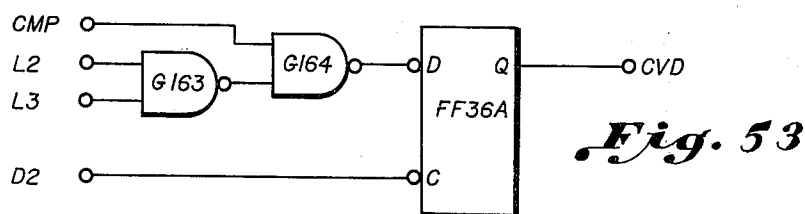
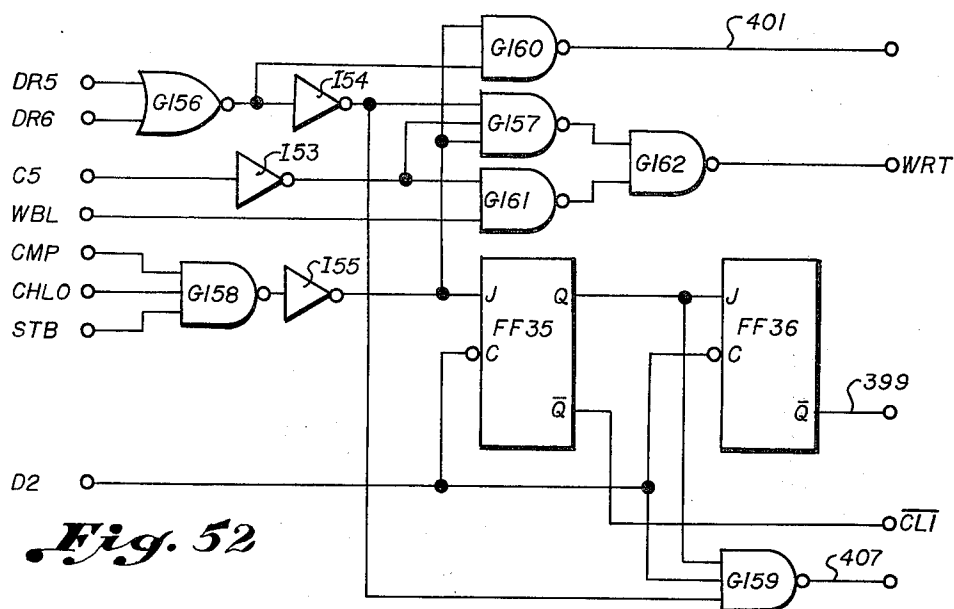


Fig. 50





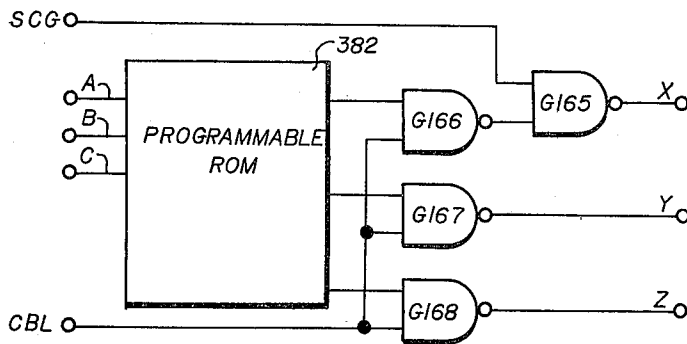


Fig. 55

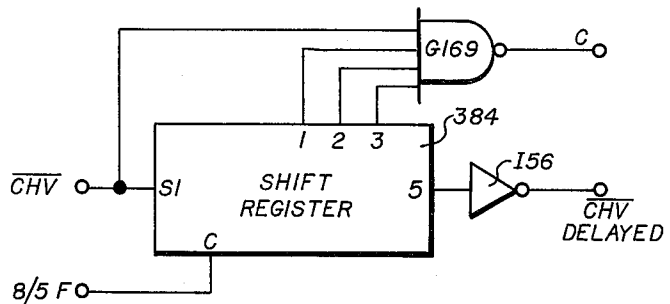


Fig. 56

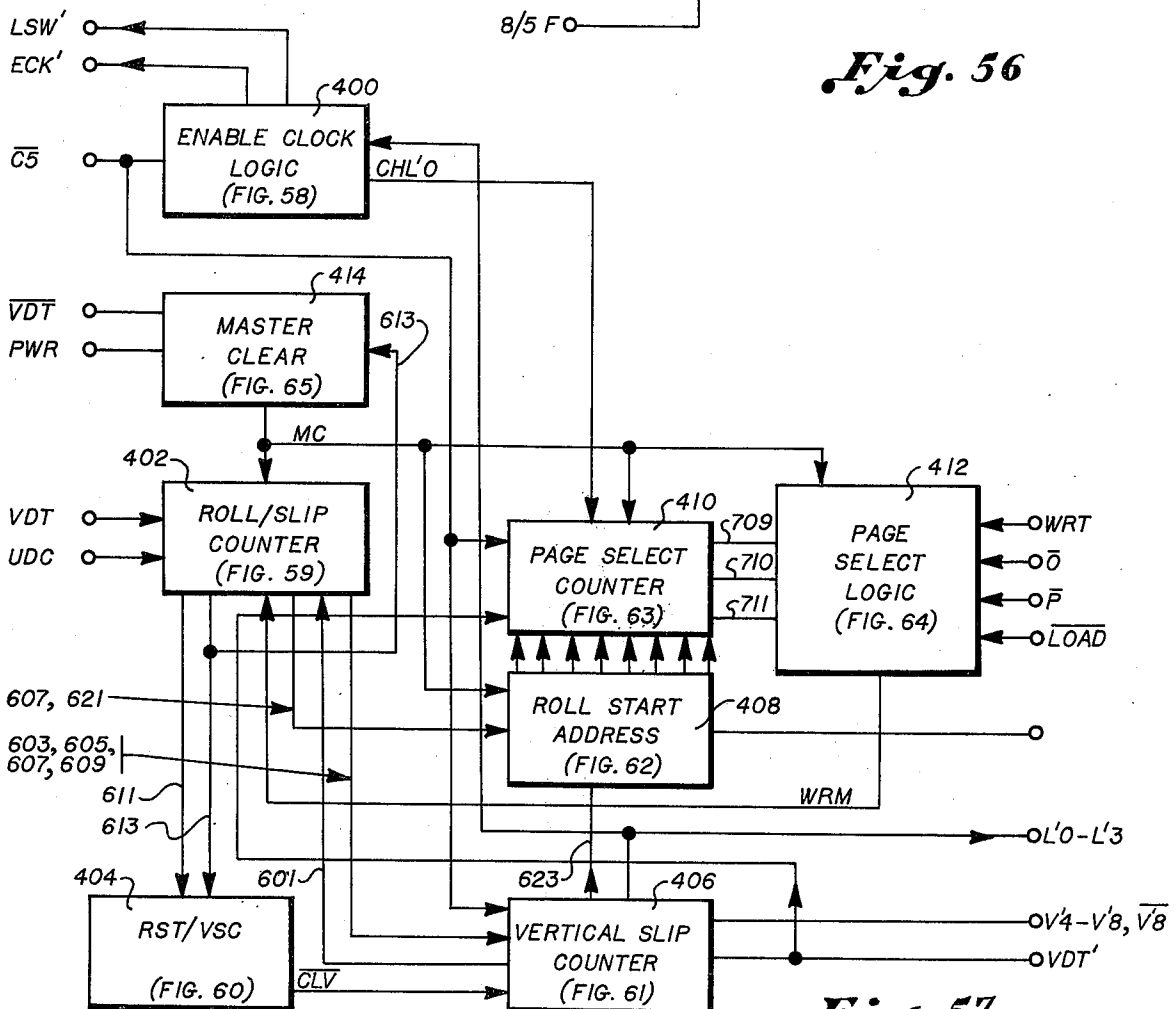


Fig. 57

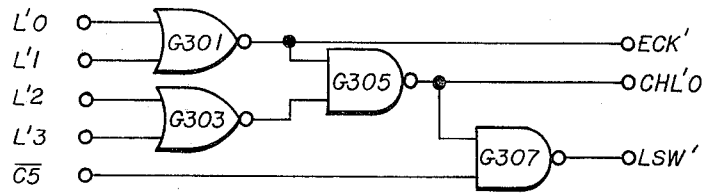


Fig. 58

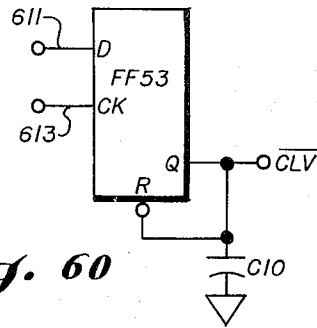


Fig. 60

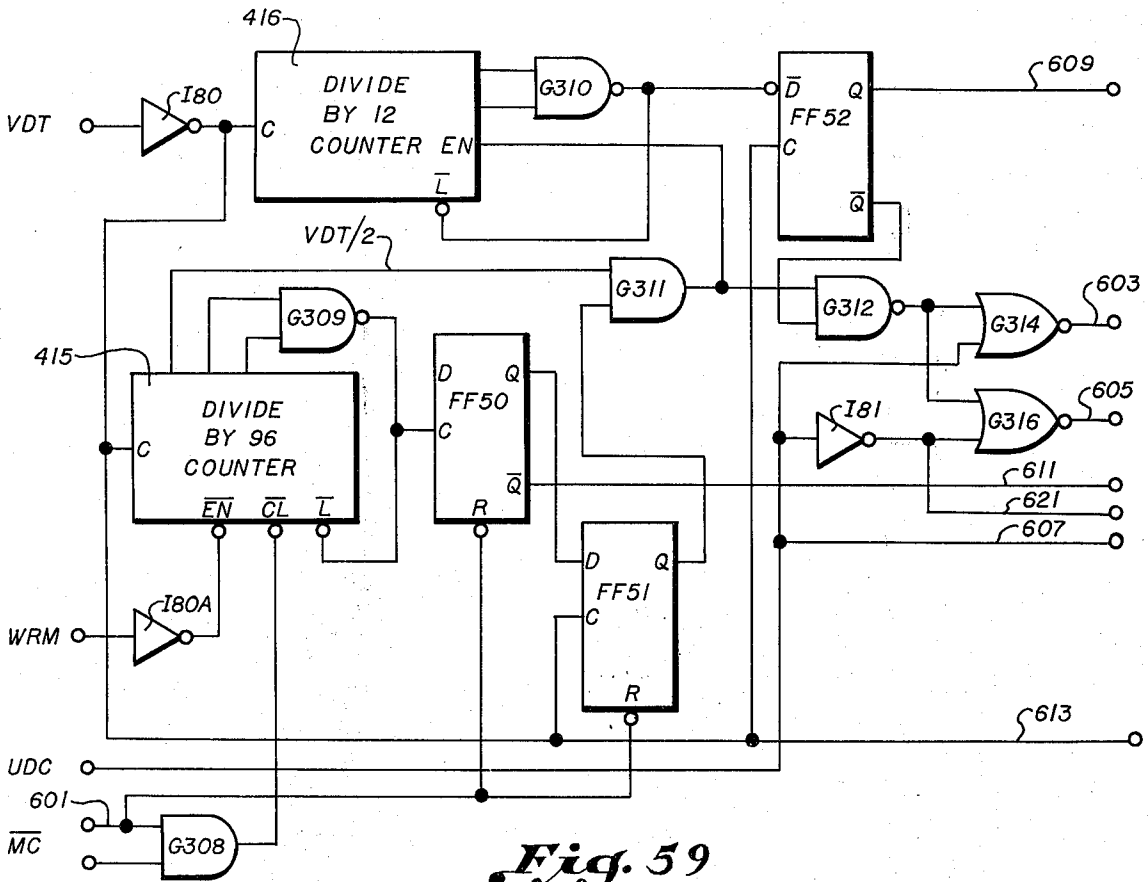


Fig. 59

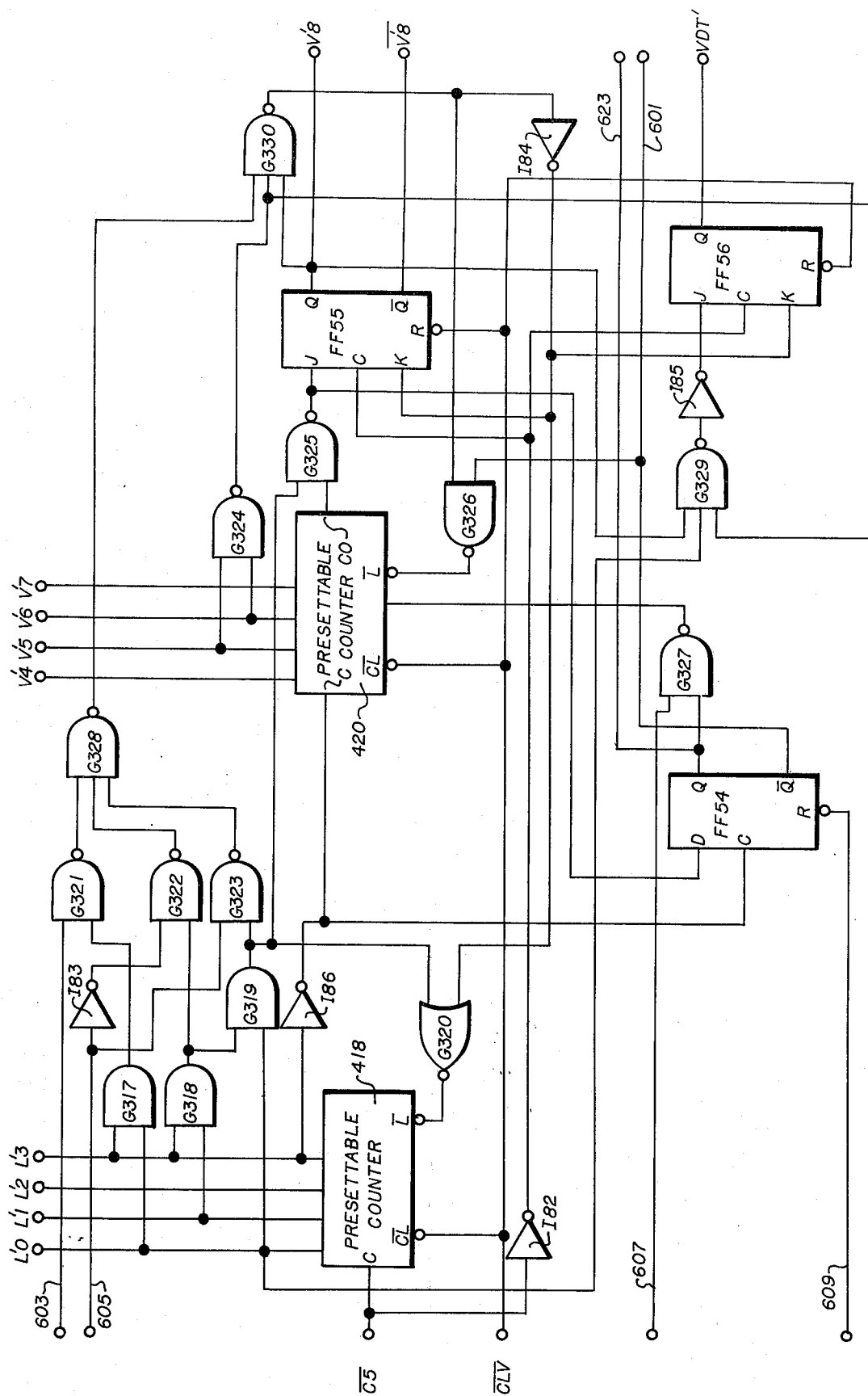


Fig. 61

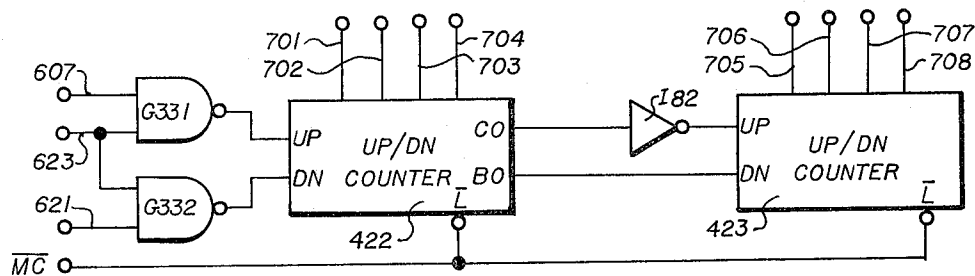


Fig. 62

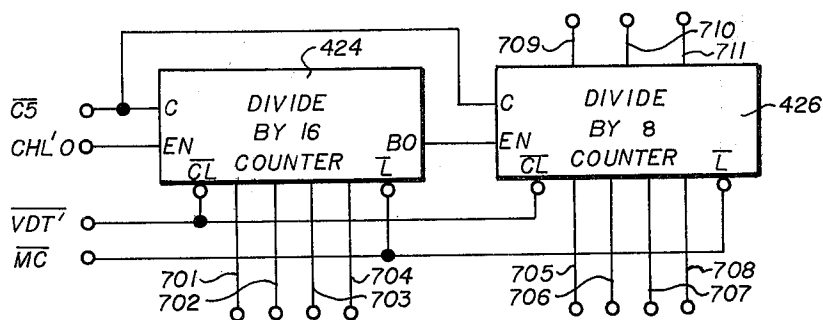


Fig. 63

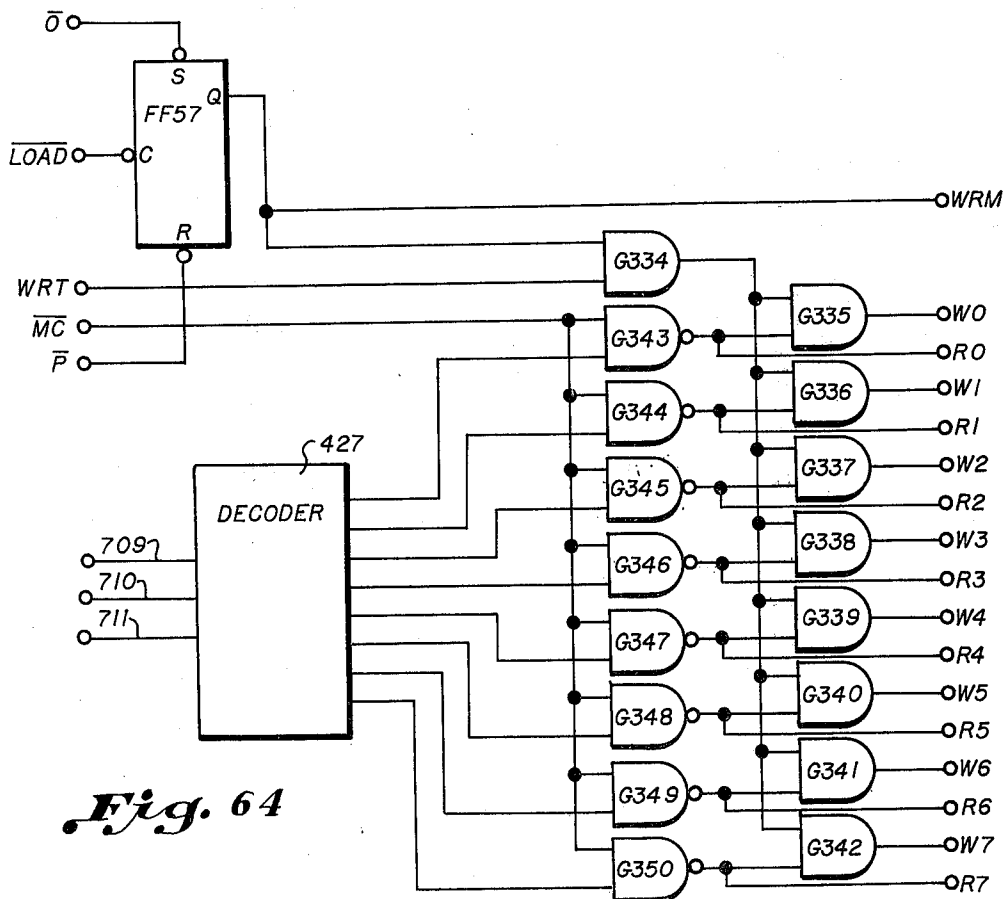


Fig. 64

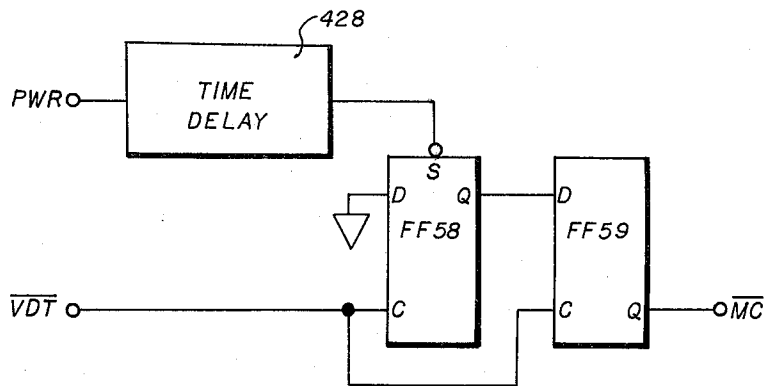


Fig. 65

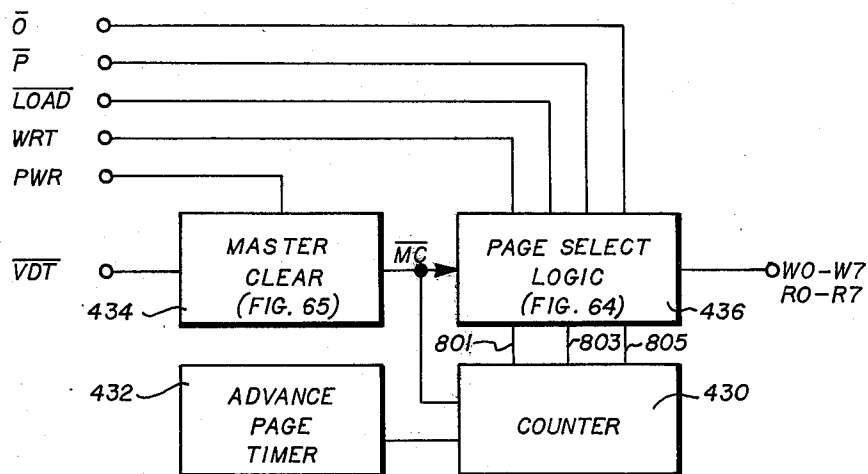


Fig. 66

MULTIPLE CHANNEL ALPHANUMERIC RESIDENTIAL TELEVISION VIDEO SIGNAL GENERATOR

BACKGROUND OF THE INVENTION

This invention is directed to television display systems and, more particularly, to multiple channel television display systems wherein different alphanumeric character displays are presented to a viewer on each channel of the multiple channel display system.

In the past because of the expense involved in creating television programs, television systems for the residential viewer have generally been limited to displaying commercially generated programs and a limited number of educational programs. Thus, the public has been restricted to viewing a limited number of programs. Moreover, the public has been restricted to viewing these programs at the time they are broadcast whether or not that time is convenient to a particular viewer. Thus, if a viewer desires to view news information, he must wait until news programs are broadcast. Moreover, if he is only interested in viewing certain types of news, he must watch an entire news report in order to view what he desires to view. Hence, not only is the viewer "locked" into a particular news time slot, he is also required to view a variety of news reports that are not of interest to him in order to view a particular news report that is of interest to him.

In addition to the foregoing restrictions applied to television viewers, there is the further restriction that much news of interest to the viewer is not broadcast due to the expense involved in broadcasting TV signals. For example, in general, information regarding local civic meetings and the like are not normally broadcast by commercial (or educational, for that matter) television stations. Further, other information, such as road conditions, local sports scores, special sale information by local stores, etc, is also not normally broadcast by commercial television stations. In order to obtain information on these subjects, the viewer is required to refer to the local newspaper or make numerous telephone calls. In either case, these alternatives are bothersome to say the least. Newspapers are normally only published once a day, and the information contained therein is not available prior to the publication time. Further, making a plurality of telephone calls to obtain certain desired information is often time-consuming, because often the same information is desired by a plurality of individuals at the same time. For example, road reports or ski condition reports are often desired by a number of people at the same time. When this occurs, the telephone lines are often saturated, whereby a number of telephone calls are required to obtain the desired information.

It will be appreciated from the foregoing brief discussion of the present limits on television systems that it would be desirable to expand the type and variety of information available to television viewers. In addition, it will be appreciated that it would be desirable for television viewers to have some control over the times during which they can view the information they desire to view.

Therefore, it is an object of this invention to provide a new and improved multiple channel television display system.

It is a further object of this invention to provide a multiple channel television display system wherein in-

formation related to common areas of subject matter are displayed on the separate channels of the multiple channel television display system.

It is a further object of this invention to provide a multiple channel television display system wherein information related to common areas of subject matter are continuously displayed, and continuously updated, on the various channels of the multiple channel television display system.

It is yet another object of this invention to provide a new and improved multiple channel television display system wherein information is obtained from newswire sources, remote and local keyboards, and other sources, and displayed on the various channels of a multiple channel television display system as alphanumeric character displays.

It is a still further object of this invention to provide a multiple channel television display system wherein the displays are pages.

It is yet another object of this invention to provide a multiple channel television display system wherein the displays are in color.

It is a still further object of this invention to provide a multiple channel alphanumeric television display system wherein alphanumeric displays can be continuously scrolled.

SUMMARY OF THE INVENTION

In accordance with principles of this invention, a multiple channel television display system suitable for receiving information from a variety of sources and displaying the information as alphanumeric character displays on a plurality of television channels is disclosed. The information sources may be newswires, stock report wires, remote and local keyboards, temperature probes, etc. The information (data) received by the system is edited by a general purpose digital computer. The computer, in performing its editing function, correlates related information and presents the related information as a part of a composite display on a single channel of the television display system. For example, sports scores, such as baseball scores, may be displayed on one channel, even though these scores are obtained from different sources, such as the Associated Press (AP) Newswire Service and the United Press International (UPI) Newswire Service. In addition, information related to local meeting notices, local temperature, etc., are displayed on different channels, as desired. Moreover, advertising information may be separately displayed on separate channels or may be combined with other information displays, such as a temperature information display, for example.

In accordance with further principles of this invention, the multiple channel television display system includes a suitably programmed general purpose digital computer and a computer control logic system. The computer control logic system receives the information from a variety of sources and, in accordance with instructions from the computer, controls the flow of information from the sources to the computer. The computer control logic, also in accordance with instructions from the computer, controls the flow of information from the computer to a plurality of character generation systems which create the resultant alphanumeric displays.

The signals between the invention and the viewers' television receivers preferably flow over cables. How-

ever, any suitable form of wireless transmitting and receiving communication system may also be used. In any event, the signals received by the viewers' television receivers are suitable for creating alphanumeric displays in readable configurations. The displays may be in color if a particular television receiver is a color receiver.

In accordance with still further principles of this invention, the alphanumeric character displays may be scrolled (moved) upwardly or downwardly. Alternatively, the displays may appear to be paged onto the face of the TV screens.

In accordance with still further principles of this invention, the alphanumeric character displays are in the form of a 5-by-7 dot array and comprise a maximum of 15 512 characters in 16 rows.

It will be appreciated from the foregoing brief summary that the invention provides a multiple channel television display system wherein information from a variety of sources can be displayed on a plurality of channels, each channel being "dedicated" to displaying information related to a particular subject matter, with or without additional advertising information. Thus, one channel may be dedicated to information relating to local news, a second dedicated to displaying regional news, and a third dedicated to displaying national and international news. Further channels may be dedicated to displaying weather forecast information, regional weather information, sports news and sports scores, either major or local, or both. Further channels may be dedicated to displaying public school administration news, city hall and public safety news, etc. Still further channels may be dedicated to displaying information about theater and civic events, department store shopping information, super market shopping information, etc. Still further channels may be dedicated to displaying classified ads of a specific nature, such as real estate, vehicles, employment, etc. In addition, combined with the overall system, standard commercial and educational TV signals can be carried on a common cable and displayed in a conventional manner.

It will also be appreciated from the foregoing brief summary that the invention overcomes the above-noted disadvantage of present television systems wherein a television viewer is restricted to viewing news and other information at a particular time. Moreover, the invention eliminates the present requirement that a viewer view undesired information in order to be able to view desired information. All the viewer need do to obtain information on a desired subject is to "switch" to the channel displaying that information. Since the invention provides a recirculating source of information, in a very short period of time he will have available to him the exact information desired.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing objects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description when taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a block diagram illustrating, in simplified form, a preferred embodiment of the invention;

FIG. 2 is a block diagram illustrating a keyboard transmitter suitable for use by the invention to form either a remote or a local keyboard transmitter;

FIG. 3 is a block diagram of parallel-to-series converter control logic suitable for use in the keyboard transmitter illustrated in FIG. 2;

FIG. 4 is a block diagram of a digital-to-tone converter suitable for use in the keyboard transmitter illustrated in FIG. 2;

FIG. 5 is a block diagram of an interface system suitable for use in the embodiment of the invention illustrated in FIG. 1;

FIG. 6 is a block diagram of computer control logic suitable for use in the embodiment of the invention illustrated in FIG. 1;

FIG. 7 is a block diagram of a dial-up port suitable for use in the computer control logic illustrated in FIG. 6;

FIG. 8 is a block diagram of connect/disconnect logic suitable for use in the dial-up port illustrated in FIG. 7;

FIG. 9 is a block diagram of gate status code logic suitable for use in the dial-up port illustrated in FIG. 7;

FIG. 10 is a block diagram of save previous connect logic suitable for use in the dial-up port illustrated in FIG. 7;

FIG. 11 is a block diagram of input busy/done logic suitable for use in the dial-up port illustrated in FIG. 7;

FIG. 12 is a block diagram of output busy/done logic suitable for use in the dial-up port illustrated in FIG. 7;

FIG. 13 is a block diagram of a serial/parallel/serial converter suitable for use in the dial-up port illustrated in FIG. 7;

FIG. 14 is a block diagram of character gates suitable for use in the dial-up port illustrated in FIG. 7;

FIG. 15 is a block diagram of BAUD rate selector logic suitable for use in the dial-up port illustrated in FIG. 7;

FIG. 16 is a block diagram of a frequency synthesizer suitable for use in the embodiment of the invention illustrated in FIG. 1;

FIG. 17 is a block diagram of select logic suitable for use in the computer control logic illustrated in FIG. 6;

FIG. 18 is a block diagram of a priority encoder suitable for use in the computer control logic illustrated in FIG. 6;

FIG. 19 is a block diagram of a newswire interface suitable for use in the computer control logic illustrated in FIG. 6;

FIG. 20 is a block diagram of a newswire counter suitable for use in the newswire interface illustrated in FIG. 19;

FIG. 21 is a block diagram of a scan control suitable for use in the newswire interface illustrated in FIG. 19;

FIG. 22 is a block diagram of an enable register suitable for use in the newswire interface illustrated in FIG. 19;

FIG. 23 is a block diagram of newswire gates suitable for use in the newswire interface illustrated in FIG. 19;

FIG. 24 is a block diagram of newswire busy/done logic suitable for use in the newswire interface illustrated in FIG. 19;

FIG. 25 is a block diagram of a universal asynchronous receiver/transmitter suitable for use in the newswire interface illustrated in FIG. 19;

FIG. 26 is a block diagram of a read acknowledge circuit suitable for use in the newswire interface illustrated in FIG. 19;

FIG. 27 is a block diagram of character gates suitable for use in the newswire interface illustrated in FIG. 19;

FIG. 28 is a block diagram of error gates suitable for use in the newswire interface illustrated in FIG. 19;

FIG. 29 is a block diagram of output display logic suitable for use in the computer control logic illustrated in FIG. 6;

FIG. 30 is a block diagram of output busy/done logic suitable for use in the output display logic illustrated in FIG. 29;

FIG. 31 is a block diagram of a display load generator suitable for use in the output display logic illustrated in FIG. 29;

FIG. 32 is a block diagram of a display selector register suitable for use in the output display logic illustrated in FIG. 29;

FIG. 33 is a block diagram of a word assembly register suitable for use in the output display logic illustrated in FIG. 29;

FIG. 34 is a block diagram of a temperature sensor suitable for use in the embodiment of the invention illustrated in FIG. 1;

FIG. 35 is a block diagram of counter control logic suitable for use in the temperature sensor illustrated in FIG. 34;

FIG. 36 is a block diagram of a clock suitable for use as part of the clock and thermometer interface in the computer control logic illustrated in FIG. 6;

FIG. 37 is a block diagram of a thermometer interface suitable for use as part of the clock and thermometer interface in the computer control logic system illustrated in FIG. 6;

FIG. 38 is a block diagram of a character address selector suitable for use in the embodiment of the invention illustrated in FIG. 1;

FIG. 39 is a block diagram of character generator group select logic suitable for use in the character address selector illustrated in FIG. 38;

FIG. 40 is a block diagram of a character generator group selector suitable for use in the character address selector illustrated in FIG. 38;

FIG. 41 is a block diagram of a ready-in selector suitable for use in the character address selector illustrated in FIG. 38;

FIG. 42 is a block diagram of ready enable logic suitable for use in the character address selector illustrated in FIG. 38;

FIG. 43 is a block diagram of a sync generator suitable for use in the embodiment of the invention illustrated in FIG. 1;

FIG. 44 is a block diagram of a timing chain suitable for use in the sync generator illustrated in FIG. 43;

FIG. 45 is a block diagram of a TV sync generator for use in the sync generator illustrated in FIG. 43;

FIG. 46 is a block diagram of a clock for character generator suitable for use in the sync generator illustrated in FIG. 43;

FIG. 47 is a block diagram of a character generator suitable for use in the embodiment of the invention illustrated in FIG. 1;

FIG. 48 is a block diagram of an input data register suitable for use in the character generator illustrated in FIG. 47;

FIG. 49 is a block diagram of character generator circuitry suitable for use in the character generator illustrated in FIG. 47;

FIG. 50 is a block diagram of a write address register control suitable for use in the character generator illustrated in FIG. 47;

FIG. 51 is a block diagram of a write address register suitable for use in the character generator illustrated in FIG. 47;

FIG. 52 is a block diagram of a write timing circuit suitable for use in the character generator illustrated in FIG. 47;

FIG. 53 is a block diagram of a cursor video generator suitable for use in the character generator illustrated in FIG. 47;

FIG. 54 is a block diagram of a chroma generator suitable for use in the embodiment of the invention illustrated in FIG. 1;

FIG. 55 is a block diagram of a color code selection network suitable for use in the chroma generator illustrated in FIG. 54;

FIG. 56 is a block diagram of a character/chroma gate generator suitable for use in the chroma generator illustrated in FIG. 54;

FIG. 57 is a block diagram of scrolling logic suitable for use in the preferred embodiment of the invention illustrated in FIG. 1;

FIG. 58 is a block diagram of enable clock logic suitable for use in the scrolling logic illustrated in FIG. 57;

FIG. 59 is a block diagram of a roll/slip counter suitable for use in the scrolling logic illustrated in FIG. 57;

FIG. 60 is a block diagram of an RST/VSC suitable for use in the scrolling logic illustrated in FIG. 57;

FIG. 61 is a block diagram of a vertical slip counter suitable for use in the scrolling logic illustrated in FIG. 57;

FIG. 62 is a block diagram of a roll-start address suitable for use in the scrolling logic illustrated in FIG. 57;

FIG. 63 is a block diagram of a page select counter suitable for use in the scrolling logic illustrated in FIG. 57;

FIG. 64 is a block diagram of page select logic suitable for use in the scrolling logic illustrated in FIG. 57;

FIG. 65 is a block diagram of a master clear suitable for use in the scrolling logic illustrated in FIG. 57; and,

FIG. 66 is a block diagram of paging logic suitable for use in the preferred embodiment of the invention illustrated in FIG. 1.

DESCRIPTION OF A PREFERRED EMBODIMENT

Prior to describing a preferred embodiment of the invention, certain background information, directed to aiding the understanding of the preferred embodiment, is hereinafter set forth.

As will be better understood from the following description, the invention is directed to providing a digital logic system that controls the flow of binary signals. The preferred embodiment of the invention is described in conjunction with a Nova computer. However, it will be appreciated by those skilled in the art and others that other types of computers can also be used. Nova computers are produced by the Data General Corporation of Southboro, Massachusetts. Information with regard to these computers is described in a document entitled "How to Use the Nova Computer" published by Data General Corporation, April, 1971. This document is incorporated herein by reference. The Nova computer utilizes certain mnemonics to define its instructions. The mnemonics described herein, as far as practicable, have been made to correspond to the mnemonics set forth in the foregoing publication. In addition, in order to better understand the mnemon-

ics utilized in this application, a mnemonics table is set forth below.

In addition to the foregoing, it should be noted that conventional symbology is used. In general, positive logic is utilized by the invention. A small 0 at an input terminal designates that the particular function occurs on a 0 input (1-0 transition). The lack of a small 0 indicates the opposite effect, i.e., that the function occurs on a 1 input (0-1 transition). Standard D and JK flip-flops, and RS latches, are utilized. An open D input of a D flip-flop indicates that the flip-flop is placed in a set state upon the occurrence of a clock pulse. A grounded D input indicates that the flip-flop is reset upon the occurrence of a clock pulse. Open and grounded inputs to JK flip-flops have similar effects. In general, signals from the computer are referred to as instruction signals which instruct either the computer control logic or, through the computer control logic, instruct the character generation circuitry in a manner such that the character generator receives instructions relating to the type and location of a particular character to be displayed. Signals to the computer are generally referred

to as information signals. It should be noted that this use of the words instruction and information only applies to this application.* In addition, a line over a particular instruction or information signal designates that instruction or information signals carries information in the inverted state. Finally, all gates feeding information to the computer are open collector gates.

* The Nova instruction booklet referenced above uses the terms "information" and "instruction" in a different manner.

MNEMONICS TABLE

General	
BO	Down overflow output of up/down counters.
C	Clock input of flip-flops, counters, registers, etc.
CL	Clear input of counters and registers.
CO	Up overflow output of up/down counters.
D	Data input of D flip-flops.
DN	Down input of up/down counters.
EN	Enable input of registers, decoders, counters, etc.
J	J input of JK flip-flops.
K	K input of JK flip-flops.
L	Load input of counters, registers, etc.
R	Reset input of D flip-flops, JK flip-flops and RS latches.
S	Set input of D flip-flops, JK flip-flops and RS latches.
UP	Up input of up/down counters.

Computer Instructions and Information Signals

CARR	Carrier. Goes to a binary zero state when a carrier frequency signal is detected by the privileged dial-up port.
CLR	Clear. Computer instruction causing the clearing of certain flip-flops of the busy/done logic systems to certain predetermined states.
CS	Control strobe. Applied to terminal 34 of the UAR/T's.
DA	Data available. The output of terminal 19 of the UAR/T's.
DATA0- DATA15	Data instructions from the computer
DATA8- DATA15	Information signals applied to the computer by the control logic system which either relates to information from remote sources, keyboards, newswires, etc., or information which relates to the operating status of the subsystems of the computer control logic. The particular information being applied to the computer at any particular point in time being determined by which of the subsystems of the computer control logic has been selected for read-out.
DB1-DB8	Parallel data input to the UAR/I of the privileged dial-up port from the computer.
DIA	Data instruction which loads the A in buffer of the computer.
DIB	Data instruction which loads the B in buffer of the computer.
DIC	Data instruction which loads the C in buffer of the computer.
DOA	Data instruction which reads the A out buffer of the computer.
DOB	Data instruction which reads the B out buffer of the computer.
DOC	Data instruction from the C out buffer of the computer.
DS	Data strobe input to the UAR/T's.
DS0-DS5	Device selection instructions from the computer.
EOC	End of character output from the UAR/T's.
EPS	Odd/even parity select to the UAR/T's.
FE	Framing error output of the UAR/T's.
GOTCHA	Interrogating pulse applied to the temperature sensor.
INTA	Interrupt acknowledge instruction from the computer applied to the computer control logic to acknowledge an interrupt.
INTR	Interrupt signal generated by the various subsystems of the computer control logic.
INTR OUT	Interrupt signal applied to the computer by the computer control logic to inform the computer that interrupt has been requested by at least one of the subsystems of the computer control logic.
IO PULSE	Computer instruction applied to the clock and thermometer interface, and to the newswire interface of the computer control logic.

Computer Instructions and Information Signals—Continued.

IORST	General reset instruction from the computer applied to the various subsystems of the computer control logic.
IRQ3-IRQ7	Interrupt request identification signals from the various subsystems of the computer control logic.
MSKO	Mask out instruction signal from the computer.
NB1, NB2	Number of data bits input terminals of the UAR/T's.
NP	No parity input terminal of the UAR/T's.
OR	Overflow error output of the UAR/T's.
PE	Parity error output of the UAR/T's.
RCP	Receive clock pulse input of the UAR/T's.
RD1-RD8	Parallel output of the UAR/T's.
RDA	Reset data available input to the UAR/T's.
RI	Ring input signal to the privileged dial-up port. When this signal drops to a binary zero state, it indicates that data is about to be applied to the privileged dial-up port from a remote keyboard.
RQENB	Request enable instruction from the computer generated at the beginning of every memory cycle to allow the subsystems of the computer control logic to request an interrupt.
SEL2-SEL7	Select signals generated by the select logic of the computer control logic to select a particular subsystem for applying or receiving signals from the computer.
SELB	Selected busy signal generated by the various subsystems of the computer control logic.
SELD	Selected done signal generated by the various subsystems of the computer control logic.
SI	Serial input terminal of the UAR/T's.
SO	Serial output terminal of the UAR/T's.
STRT	Start instruction generated by the computer.
SWE	Status word enable input of the UAR/T's.
TBMT	Transmitter buffer empty output signal from the UAR/T's.
TCP	Transmitter clock input of the UAR/T's.
TSB	Transmitter stop bit input to the UAR/T's.
XR	External reset input of the UAR/T's.
Character Generation	
A1-A15	Character location and character nature instruction signal generated by the output display logic of the computer control logic.
BLF	Back line feed signal generated by the function decoder of the character generator.
BS	Back space signal generated by the function decoder of the character generator.
C0-C5	Character position code signals (horizontal) generated by the sync generator.
CBL	Composite blanking signal generated by the sync generator.
CHLO	Character line zero clock signal generated by the sync generator.
CHV	Cursor video signal generated by the character generator.
CL1	Clear horizontal signal used in the character generator.
CLS	Clear screen signal generated by the character generator.
CLV	Clear video slip counter generated by the scrolling logic.
CMP	Comparison signal generated in the character generator.
CP1, CP2, CP3	Clock pulses generated by the sync generator.
CR	Carriage return signal generated by the function decoder of the character generator.
CSY	Composite sync signal generated by the sync generator.
D0-D2	Dot position code generated by the sync generator.
DR0-DR6	Data output of character generator input data register which determine the nature of a particular alphanumeric character to be displayed.
ECK	Enable clocks timing signal generated by the sync generator.
ECP	Enable comparison signal generated by the sync generator.
FLF	Forward line feed signal generated by the function decoder of the character generator.
FS	Forward space signal generated by the function decoder of the character generator.
HME	Home signal generated by the function decoder of the character generator.
L0-L3	Line position code generated by the sync generator.
LSW	Load line storage shift register timing signal generated by the sync generator.
MC	Master clear signal generated in the scrolling logic.
R0-R7	Read timing signals applied to the character generator by the scrolling or paging logic.
SCG	Sub carrier burst gate timing signal generated by the sync generator.
STS	Strobe shift register signal generated by the sync generator.
STB	Strobe input data register signal generated in the character generator.
UDC	Up-down control signal applied to the scrolling logic.

Computer Instructions and Information Signals—Continued

V4-V7	Character row position code generated by the sync generator.
V8	Most significant bit of read address occurs on the eleventh line of character row twenty-two of the display.
VDT	Vertical dead time signal generated by the sync generator.
WBL	Write blank signal generated in the character generator.
WRM	Write mode signal applied to the paging or scrolling logic to enable read-in.
WRT	Write timing signal applied to the paging and scrolling logic to denote time at which character may be written.
W0-W7	Write timing signals applied to the character generator by the scrolling or paging logic.

Turning now to a description of the preferred embodiment of the invention, FIG. 1 is a block diagram illustrating a simplified preferred embodiment of the invention. That is, FIG. 1 is a block diagram of the invention wherein only a single keyboard transmitter is illustrated, a single news or stock line input is illustrated, and a single temperature sensor is illustrated. However, it will be appreciated from the following description that a plurality of both remote and local keyboard transmitters can be utilized in an actual embodiment of the invention, as well as a plurality of news and stock line information inputs. In addition, while only a single output channel is illustrated in FIG. 1, it will be appreciated that a plurality of channels, each dedicated to a particular type of subject matter, are to be utilized in an actual embodiment of the invention.

The simplified embodiment of the invention illustrated in FIG. 1 comprises a keyboard transmitter 102; a communication system 104; an interface 106; a temperature sensor 108; a frequency synthesizer 110; computer control logic 112; a computer 114; a character address selector 116; a sync generator 118; a character generator 120; a chroma generator 122; a modulator 124. In addition, enclosed by dash lines to illustrate their optional character are illustrated scrolling logic 126; and paging logic 128.

The keyboard transmitter 102 includes a keyboard similar to a typewriter keyboard. Each time a key is depressed, a suitable binary code signal defining the depressed key is generated. If necessary, the binary code signal is converted into a signal suitable for long distance transmission and transmitted by the communication system 104 to the interface 106. The communication system, if the keyboard transmitter is local, may merely be a coupling cable. If so, conversion into a signal suitable for long distance transmission will not be necessary. Alternatively, if the keyboard transmitter is remote from the interface, the communication system 104 may be a telephone communication system. Or, the communication system 104 may be the up-stream path of a two-way cable system. Or, still further, a wireless communication system, such as a microwave communication system.

In any event, the signals generated by the keyboard transmitter 102 are received by the interface 106 and applied to the computer control logic 112. The computer control logic 112 also receives signals from the temperature sensor 108 and signals from a news/stock input on line 130.

The news/stocks input line designates a plurality of suitable signal sources, such as an Associated Press (AP) wire-service line, a United Press International (UPI) wireservice line, a stock report wireservice line

from the New York or American Stock Exchanges, etc.

The computer control logic 112 receives timing signals from the frequency synthesizer 110. Further, the computer control logic 112 is connected to a general purpose digital computer 114, such as a Nova computer described in the publication referenced above and incorporated herein by reference, to apply information to the computer 114 received from its various inputs and receive instructions from the computer 114 to apply to its various outputs.

The computer control logic 112, for each display channel, controls a character address selector 116. The character address selector 116 controls the address of display characters, i.e., the channel on which they are to be displayed. In addition, the computer control logic 112 controls a plurality of character generators 120. The character generators control the nature of the resultant alphanumeric displays. The timing necessary to display the correct characters on the correct channels is provided by the sync generator 118. Thus, the signals ultimately generated by the character generator 120 include information regarding both the location and the nature of the characters to be displayed. These signals are applied to the chroma generator 122. The chroma generator 122 controls both background and character color. The resultant signals which contain character nature information, and color information, in TV form, are modulated by the modulator 124 prior to being applied to a cable or other transmission system for transmission to the TV sets of the ultimate viewers. Though not shown, a suitable demodulator is provided at the viewers' TV sets for demodulating the signal. The demodulated signal is then displayed on the TV screen as an alphanumeric character display on a chosen channel.

If desired, the resultant character displays can be made to appear to scroll (move) upwardly or downwardly by scrolling logic 126. The scrolling logic in essence modifies the signals generated by the sync generator to cause the display to appear to move upwardly or downwardly. Alternatively, paging logic 128 can be used to cause a paging effect, wherein "pages" of information appear to be sequentially displayed.

KEYBOARD TRANSMITTER

FIG. 2 illustrates a keyboard transmitter suitable for use in the embodiment of the invention illustrated in FIG. 1. The keyboard transmitter illustrated in FIG. 2 comprises a keyboard 132; an oscillator 134; a pulse generator 136; a parallel-to-serial (P/S) converter 138; parallel-to-serial (P/S) control logic 140; and a digital-to-tone converter 142. The keyboard 132 is a standard electronic keyboard wherein each time a particular key

is depressed, a parallel code of binary signals representing the depressed key is generated and conveyed via conductor 107 to the P/S converter 138. In addition, each time a key is depressed, a strobe signal is generated. The strobe signal is applied along a conductor designated 105 to the P/S converter control logic 140. Suitable P/S converter control logic is illustrated in FIG. 3 and hereinafter described.

The oscillator 134 is a standard timing oscillator that generates clock pulses which are applied via a suitable conductor 99 to a clock (C) input of the P/S converter 138. The P/S converter control logic also receives a "repeat" signal from the keyboard via a conductor 103 whenever a particular key code is to be repeated. A break signal generated by the keyboard to designate a "space" between depressed keys is applied to the pulse generator 136 via a conductor 101. In accordance therewith, the pulse generator generates a pulse which is applied to the digital-to-tone converter via a conductor 115.

The P/S converter control logic controls the loading of the P/S converter. That is, when the P/S converter control logic receives a strobe signal it applies a binary zero enable signal to the P/S converter. When this signal is received the P/S converter converts its parallel input to a serial output at the oscillator frequency. The serial output is applied to the digital-to-tone converter via a conductor 113. During the conversion a binary zero on conductor 109 inhibits the operation of the P/S converter control logic unless both a strobe one and a repeat zero simultaneously occur. Upon completion of the conversion of a binary one is applied via conductor 109 to the P/S converter control logic. If a "repeat" signal exists at this point in time, the P/S converter is enabled and performs a second conversion. Of not the sequence terminates until another key is depressed.

FIG. 3 illustrated P/S converter control logic suitable for use in the keyboard transmitter illustrated in FIG. 2 and comprises: two two-input NAND gates designated G1 and G2; an inverter designated I1; and a one shot 100. Conductor 103 is connected to one input of G1 and conductor 109 is connected through I1 to the second input of G1. The output of G1 is connected to one input of G2. Conductor 105 is connected to the second input of G2. The output of G2 is connected to the input of the one-shot 100. The output of the one-shot is connected to conductor 111.

In operation, when a strobe pulse occurs, the one-shot is fired, by the binary zero occurring on the output of G2. The firing of the one-shot enables the P/S converter, as previously described, and a conversion takes place. If a repeat zero pulse and a strobe one pulse occur during the conversion, the conversion is repeated.

FIG. 4 is a block diagram of a digital-to-tone converter suitable for use in the keyboard transmitter illustrated in FIG. 2 and comprises: a two-input NAND gate designated G3; an inverter designated I2; and an FSK transmitter 102. Conductors 113 and 115 are connected to the two inputs of G3 and the output of G3 is connected through I2 to the input of the FSK transmitter 102. The FSK transmitter generates one of two audio tones depending upon whether its input is a binary zero or a binary one. The usual output (in the absence of a break signal) of the pulse generator, is a binary one. Thus, zero/one binary signals on conductor 113 cause one or the other of the tones to be generated

by the FSK transmitter as they occur. The break zero pulse generated by the pulse generator merely "holds" the output of G3 in a one state until it terminates. This action maintains one of the tones constant for this period of time to designate the occurrence of the break signal.

It should be noted that the serial binary output of the P/S converter could be directly applied to the dial-up port hereinafter described if the keyboard transmitter is "local" as opposed to "remote" from the dial-up port. On the other hand, as illustrated, if the keyboard transmitter is remote, preferably, audio tones suitable for transmission by a conventional telephone communication system, using suitable acoustical couplers are created. Alternatively, however, other types of communication systems including a variety of wireless systems could be used by the invention. In either event (wireless or telephone), the transmitted signals are received by the interface 105.

INTERFACE

FIG. 5 illustrates an embodiment of an interface 105 suitable for use by the preferred embodiment of the invention illustrated in FIG. 1. The interface illustrated in FIG. 5 comprises a ring detector 150; an originate answer switch 152; a data transmitter 154; and, a data receiver 156.

The ring detector, assuming the communication system is a standard telephone communication system, senses a ring signal when the telephone initially is used to "dial" the apparatus of the invention. The ring detector, when it detects a ring signal, generates a signal designated RI, meaning that its output drops to a binary zero state. This binary zero indicates that keyboard information is forthcoming. Obviously, the ring detector 150, if an alternate type of communication system is utilized by the invention, will be adapted to detect an initially generated signal indicating that keyboard information is to be forthcoming and, in accordance therewith, generate a binary zero signal similar to RI. The ring signal, or other initial signal indicating forthcoming keyboard information, is also sensed by the originate/answer switch 152. When this switch is activated, it deactivates the data transmitter 154 and activates the data receiver 156.

The data transmitter 154 receives serial data instructions from the computer control logic 112 at the terminal designated DATA IN. The data transmitter converts these signals into a form suitable for transmission and applies them to the communication system via a terminal designated DATA IN and OUT. If it is not desired to communicate with a suitable display system located at the keyboard, the data transmitter may be eliminated.

The data receiver 156 receives signals from the communication system at the DATA IN and OUT terminal. These signals, if the communication system is a telephone communication system, are the two-tone signals generated by the digital-to-tone converter of the keyboard transmitter. The data receiver converts the received signal into a serial chain of binary signals and applies the chain to a terminal designated DATA OUT. In addition, while the receiver is receiving either of the two tones a binary zero is applied to an output terminal designated CARR. The CARR binary zero state exists as long as the output of keyboard transmitter indicates that it is "on line." Thus, the DATA OUT outputs from

the data receiver comprise a series of binary signals similar to the series of binary signals generated at the output of the parallel-to-serial converter of the keyboard transmitter and a binary zero $\overline{\text{CARR}}$ signal indicating that a keyboard is coupled to the system. These information signals are applied to the hereinafter described computer control logic 112.

COMPUTER CONTROL LOGIC

FIG. 6 is a block diagram of a computer control logic system suitable for use in the embodiment of the invention illustrated in FIG. 1 and comprises a dial-up port 160; a newswire interface 162; select logic 164; a priority encoder 166; output display logic 168; a clock and thermometer interface 170; and In/Out buffers 171.

The RI, CARR, DATA IN and DATA OUT signals from the interface illustrated in FIG. 5 are applied to the dial-up port 160. In addition, the dial-up port also receives clock pulses at two different frequencies from frequency synthesizer 110, designated 1760Hz and 4800Hz for purposes of description. Further, the dial-up port receives the following instruction signals from the computer: MSKO, IORST, RQENB, CLR, PWR FAIL, DISCONNECT, STRT, DIA, DATA 14, DATA 15, DOC, DB1-DB8, DOA, DIC DATA5, and DATA6. Further, the dial-up port 160 applies the following information signals to the computer: DATA8-DATA15, SELB, and SELD.

The dial-up port applies the following information signals to the priority encoder: $\overline{\text{INTR}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ4}}$ and $\overline{\text{IRQ2}}$. In addition, the dial-up port receives instructions designated SEL2, SEL3, and SEL4 from the select logic 164. The purpose of these signals and the operation of the dial-up port is hereinafter described.

The newswire interface 162 receives serial data on an input cable designated NEWS LINE INPUT. In addition the news line interface receives a suitable clock signal from the frequency synthesizer 110 designated 2727Hz in FIG. 6 for purposes of illustration. Further, the newswire interface receives the following instructions from the computer via the In/Out buffer 171: STRT CLR, IORST, MSKO, RQENB, DIC, IO PULSE, DATA3, DATA13, DATA14, DATA15, DOB, DOC, DIA, AND DIB. The newswire interface generates computer information signals designated DATA8-DATA15, SELB and SELD. Further, the newswire interface applies information signals designated $\overline{\text{INTR}}$, and $\overline{\text{IRQ7}}$ to the priority encoder 166 and receives an instruction signal designated SEL7 from the select logic 164.

The select logic 164 receives $\overline{\text{DSO}}-\overline{\text{DS5}}$ instruction signals from the computer via the In/Out buffers and generates the herein described SEL2-SEL7 instructions.

The priority encoder 166, in addition to receiving the $\overline{\text{INTR}}$, $\overline{\text{IRQ}}$, and $\overline{\text{IRQ}}$ signals herein described, also receives an instruction signal from the computer designated INTA and generates information signals to the computer designated DATA13, DATA14, DATA15, and $\overline{\text{INTR}}$ and $\overline{\text{INTP}}$ OUT OUT. The priority encoder also receives a signal designated $\overline{\text{INTP}}$ IN created in the manner hereinafter described.

The output display logic 168 receives computer instruction signals designated DOA, DOB, STRT, CLR, RQENB, MSKO, IORST and DATA0-DATA15 and generates computer information signals

designated SELB and SELD. The output display logic also applies information signals designated $\overline{\text{INTR}}$ and $\overline{\text{IRQ6}}$ to the priority encoder 166 and receives an instruction signal designated SEL6 from the select logic 164. Further, the output display logic receives information signals designated $\overline{\text{READY}}$ and $\overline{\text{LOAD}}$ (A20-A27) generated by the hereinafter described character address selector. Finally, the output display logic generates a plurality of instruction signals designating both the address and the nature of a particular character. These signals are designated A1-A15 in FIG. 6 and are applied to the hereinafter described character address selector 116 (A1-A7) and character generator 120 (A8-A15).

The clock and thermometer interface 170 receives information signals designated UP and DN from the temperature sensor 108 and applies an instruction signal designated $\overline{\text{CLEAR}}$ to the temperature sensor 108. In addition, the clock and thermometer interface receives a 1Hz signal from the sync frequency synthesizer 110 and applies an instruction signal designated COTCHA to the temperature sensor 108. Further, the clock and thermometer interface receives computer instruction signals via the In/Out buffers 171 designated DATA4, MSKO, RQENB, STRT, CLR, IORST, IO PULSE, and DIB. Moreover, the clock and thermometer interface generates computer information signals designated SELD, SELB, DATA14, and DATA15. Finally, the clock and thermometer interface receives an instruction signal designated SEL5 from the select logic and applies information signals designated $\overline{\text{INTR}}$ and $\overline{\text{IRQ5}}$ to the priority encoder 166.

The actual nature and operation of the various subsystems of the computer control/logic illustrated in FIG. 6 are described below. In general, however, these subsystems receive information and, in accordance with computer instructions, transmit the information to the computer. In accordance with the received information, the computer generates instructions which cause the generation of alphanumeric displays. More specifically, the dial-up port receives keyboard information and informs the priority encoder 166 when such information is being received. Similarly, the newswire interface informs the priority encoder when it starts to receive information. The clock and thermometer interface inform the priority encoder at preset intervals that they have information to transmit. The priority encoder "informs" the computer of these situations. The computer then through the select logic controls the receipt of the information from these sources. In addition, the computer, through the select logic 164, controls the output display logic which in turn controls the alphanumeric displays carried by the various channels of the overall multiple channel TV display system.

It is pointed out here that many of the information (DATA0-DATA15) signals from the various subsystems of the computer control logic have similar "names," as do many of the computer instruction signals (IORST, CLR, STRT, etc.). These signals are designated by similar terms because they are applied to common inputs and outputs of the computer, as will be better understood by reference to the document entitled "How to Use the Nova Computer" published by the Data General Corporation of Southboro, Massachusetts, and referenced above. In all case whether an instruction is actually applied to or information received from a particular subsystem at a particular point in time depends upon whether that subsystem has been

"selected" by the select logic at that point in time. If a subsystem has not been selected, the information it is generating is not received by the computer at that point in time (even though it will be received at a later point in time). Nor is an instruction received by a subsystem until it has been selected to receive the instruction.

DIAL-UP PORT

A preferred embodiment of a dial-up port suitable for use in the computer control logic illustrated in FIG. 6 is illustrated in FIG. 7 and comprises: connect/disconnect logic 172; gate status code logic 174; save previous connect logic 176; input busy/done logic 178; output busy/done logic 180; a serial/parallel/serial converter 182; character gates 184; and BAUD rate selector logic 186.

In general, the connect/disconnect logic 172 receives the $\overline{RI}$ and $\overline{CARR}$ information signals from the interface illustrated in FIG. 5, computer instructions $\overline{PWR\ FAIL}$ and $\overline{DISCONNECT}$, and $\overline{TBMT}$, $\overline{NEW\ DATA}$ and $\overline{OR}$ signals from the serial/parallel/serial converter 182, and in accordance therewith controls the operation of the gate status code logic 174, the save previous connect logic 176, the input busy/done logic 178, and the BAUD rate selector logic.

The input busy/done logic 178 basically determines whether the dial-up port is or is not receiving information from a keyboard and, in accordance therewith, generates certain information signals for the computer ($\overline{SELD}$ and $\overline{SELB}$) and the select logic ($\overline{INTR}$ and $\overline{IRQ4}$). The output busy/done logic determines whether the dial-up port is or is not transmitting information signals and so informs the computer ($\overline{SELB}$ and $\overline{SELD}$) and the priority encoder ($\overline{INTR}$, $\overline{IRQ3}$ and $\overline{IEQ3}$).

The serial/parallel/serial converter 180 converts the keyboard serial data signals into parallel signals ($\overline{RD1}$ – $\overline{RD8}$) which are applied through the character gates 184 to the computer ($\overline{DATA8}$ – $\overline{DATA15}$). In addition, the serial/parallel/serial converter converts computer generated parallel instruction signals ($\overline{DB1}$ – $\overline{DB8}$) into serial signals suitable for transmission to a keyboard for read out via a printer or the like.

The BAUD rate selector logic 186, in accordance with instruction signals from the computer ($\overline{DOC}$, $\overline{DATA14}$, and $\overline{DATA15}$) generates timing and control signals utilized by the serial/parallel/serial converter 182. The BAUD rate selector logic receives clock signals (1760Hz, 4800Hz) from the frequency synthesizer.

The gate status code logic 174 determines the status of certain gates in the connect/disconnect logic and, in accordance therewith, generates computer information signals designated $\overline{DATA13}$, $\overline{DATA14}$, and $\overline{DATA15}$. The save previous connect logic 176, in accordance with an instructions from the computer ($\overline{DIC}$) controls whether or not the information applied to the connect/disconnect logic is to be temporarily retained.

FIG. 8 illustrates connect/disconnect logic suitable for use in the dial-up port illustrated in FIG. 7 and comprises: three two-input NAND gates designated G9, G10 and G11; a five-input AND gate designated G12; two inverters designated 13 and 14; four resistors designated R4–R7; two diodes designated D1 and D2; a capacitor designated C1; and an RS latch 188. The $\overline{CARR}$ signal from the interface is connected through I4 to one input of G12 and through R6 to a voltage source designated +V1. $\overline{OR}$ is applied to the second input of G12,

$\overline{DISCONNECT}$ is applied to the third input of G12 and $\overline{PWR\ FAIL}$ is applied to the fourth input of G12. $\overline{CARR}$ is also applied through I3 to one input of G10 and to the cathode of D2. The anode of D2 is connected through R4 to the fifth input of G12. The fifth input of G12 is also connected through C1 to ground and to the cathode of D1. R5 is connected in parallel with D1.

The output of G12 is connected to the S input of the RS latch 188. $\overline{RI}$ is applied to one input of G11 and to the R input of the RS latch. $\overline{TBMT}$ is applied to one input of G9. $\overline{NEW\ DATA}$ is applied to the second input of G9. The output of G9 is connected to the second input of G10. The output of G10 is connected to the second input of G11. The output of G11 is connected to the cathode of D1 through R7 to +V1. The Q output of the RS latch is connected to a conductor designated 125. The Q output of the RS latch 188 is connected to a conductor designated 123.

Initially, the RS latch 188 is in a set state, usually because the output of I4 went through a one-to-zero transition when $\overline{CARR}$ went from zero to one at the termination of the previous information input from the keyboard. When the interface 106 receives a subsequent ring, $\overline{RI}$ goes from one state to a zero state. This transition places the RS latch in its reset state as hereinafter described.

Turning now to a more complete description of the operation of FIG. 8, assuming initially that $\overline{OR}$, $\overline{DISCONNECT}$ and $\overline{POWER\ FAIL}$ are all in one states because none of their related conditions exist and that $\overline{TBMT}$ and $\overline{NEW\ DATA}$ are in one states (as they would be if there is no new data in the serial/parallel/serial converter and if the transmitter buffer of the serial/parallel/serial converter is empty), the transition of $\overline{RI}$ from one to zero, which occurs when a ring signal is sensed in the manner previously described, resets the RS latch 188. In addition, the output of I3 shifts from zero to one because $\overline{CARR}$ shifts from one to zero. Termination of the $\overline{RI}$ pulse (i.e., its return to one) does not set the RS latch 188 via G11 and D1 because at this point in time C1 is charged (by the previous one on the output of G11). Moreover, there is now a one on the output of I3 preventing an immediate discharge via R4 and D2. Thus, the RS latch cannot be set by the output of G11 until C1's charge is dissipated to a predetermined level determined mainly by the time constant of R5 and C1. During this period of time, $\overline{NEW\ DATA}$ will shift from one to zero, because data will be received by the serial/parallel/serial converter 182. Thus, the output of G9 will shift from zero to one causing the output of G10 to shift from one to zero. This shift, because $\overline{RI}$ is returned to its one state, causes the output of G11 to shift from a zero to one and maintain C1 charged. C1 remains thusly charged, while data is being received and converted by the serial/parallel/serial converter in the manner hereinafter described. When the $\overline{CARR}$ signal returns to its one state, indicating the end of the input information, it (through I4 and G12) causes the RS latch 188 to be set. Thus, $\overline{RI}$ resets the RS latch and the termination of $\overline{CARR}$ sets the RS latch 188. The time constant circuit (mainly C1 and R5) is included to set the RS latch 188 if a keyboard should remain "on" without applying additional information to the dial-up port. When this situation occurs, the RS latch is set when the charge on C1 dissipates to an essentially zero level. Thus, the time constant circuit

prevents "tying up" the telephone line and comes into operation if a keyboard is "mistakenly" left on.

Should any of certain undesirable conditions occur to the computer, it causes the DISCONNECT instruction to set the RS latch 188. Alternatively, an overrun indication by the serial/parallel/serial converter or a power failure can set the RS latch 188.

When the RS latch is set, its $\bar{Q}$ output is in a zero state and its Q output is in a one state, and vice versa when it is reset. These signals are applied by conductors 123 and 125, respectively, as illustrated in FIG. 7, to other logic circuits of the overall dial-up port.

FIG. 9 is a block diagram of gate status code logic suitable for use in the dial-up port illustrated in FIG. 7 and comprises: an encoder 190; and, three two-input NAND gates designated G13, G14 and G15. One input to the encoder 190 is conductor 123. The encoder also receives $\bar{FE}$ and $\bar{PE}$ signals from the serial/parallel/serial converter. The fourth input to the encoder is a conductor 133 which carries a signal related to the status of the save previous connect logic illustrated in FIG. 10 and hereinafter described.

The encoder 190 essentially places a binary code on three output lines, the output code being related to the zero or one status of its four inputs. One of the three output lines is connected to an input of G13, another to an input of G14, and the third to an input of G15. The other inputs of G13, G14 and G15 are connected to a conductor designated 131. Conductor 131 carries a gating signal generated by the save previous connect logic illustrated in FIG. 10. The outputs of G13 and G14 and G15 are designated DATA13, DATA14 and DATA15 and are information signals applied to the computer for interpretation.

FIG. 10 is a block diagram of save previous connect logic circuit suitable for use in the dial-up port and comprises a D flip-flop designated FF4; two two-input NAND gates designated G16 and G17; and, an inverter designated I4. Conductor 123 is connected to the D input of FF4. The DIC instruction signal from the computer is applied to one input of G17. The other input of G17 receives the signal designated SEL4, generated by the select logic of the computer control logic illustrated in FIG. 6. The output of G17 is connected to the C input of FF4 and through I4 to the conductor designated 131. Conductor 131 is connected to the gate status code logic illustrated in FIG. 9 and previously described. The Q output of FF4 is connected to one input of G16. Conductor 125 is connected to the second input of G16. The output of G16 is applied to a conductor which is connected to the input busy/done logic illustrated in FIG. 11 and hereinafter described. The $\bar{Q}$ output of FF4 is connected to conductor 133.

In operation, the D input of FF4 senses the status of the RS latch 188 of the connect/disconnect logic. When SEL4 and the RS latch 188 of the connect/disconnect logic. When SEL4 and DIC both achieve one states at the same time, the output of I4 (conductor 131) gates G13, G14 and G15 of the gate status code logic "on" so that they can pass the information signals on their other inputs. At this point, FF4 is not clocked because the output of G17 shifted from one to zero, not zero to one. When either or both DIC and SEL4 return to their zero states, FF4 is clocked. If data is still being received at this point in time, the Q output of FF4 applies a one to its associated input of G16, allowing G16 to sense when the RS latch becomes set at the end of

the receipt of data, and vice versa if the RS latch has been set at this point in time. The signal on conductor 135, as will be better understood from the following description, inhibits a gate which senses the occurrence of a new connection.

FIG. 11 is a block diagram of input busy/done logic suitable for use by the dial-up port illustrated in FIG. 7 and comprises: two D flip-flops designated FF5 and FF6; five two-input NAND gates designated G18, G19 and G21-G23; a two-input AND gate designated G20; and an inverter designated I5.

$\bar{DA}$ is applied to one input of G18, and conductor 135 is connected to the second input of G18. The output of G18 is connected to one input of G19 and to one input of G22. DATA5 is applied to the D input of FF5 and MSKO is applied to the C input of FF5. The $\bar{Q}$ output of FF5 is connected to the second input of G19. The output of G19 is connected to the D input of FF6. RQENB is applied to the C input of FF6. The Q output of FF6 is the signal designated IRQ4 and is connected to the priority encoder 166. The $\bar{Q}$ output of FF6 is connected to the input of I5. The output of I5 is a signal designated INTR and is also connected to the priority encoder.

IORST is applied to the R input of FF5 and to one input of G20. CLR is applied to one input of G21. SEL4 is applied to the second input of G21, the second input of G22, and one input of G23. The output of G21 is connected to the second input of G20 and the output of G20 is connected to S input of FF6. Conductor 123 is connected to the second input of G23. The output of G22 is a signal designated SEL $\bar{D}$ and the output of G23 is a signal designated SELB.

In general, the input busy/done logic detects when the dial-up port is about to receive information and informs the computer of this fact. In addition, it informs the computer whether or not the input to the privileged dial-up port is busy, i.e., receiving data. IORST instructions resets FF5 and sets FF6 at intervals selected by the computer and MSKO and RQENB instructions clock FF5 and FF6, respectively, for interrogation purposes at intervals selected by the computer.

FF5 and FF6 are in their reset states when data is first received by the dial-up port. Whenever a complete data character is received and assembled by the serial/parallel/serial converter 182, $\bar{DA}$ goes from one to zero, and the output of G18 goes from zero to one. This output shift causes the output of G19 to shift to a zero state. Thus, the next time a RQENB instruction occurs and the device's mask bit, FF5, is clear, the Q output of FF6 and the output of I5 shift to zero states to inform the priority logic that the dial-up port has received new information (IRQ4) and to request an interrupt (INTR). The computer controls a subsystem's ability to request interrupts by setting or resetting the subsystem's mask bit as described in the reference "How To Use The Nova."

The computer is directly informed of the busy/done status of the input of the dial-up port when SEL4 shifts from zero to one. This signal interrogates the output of G18 through G22 and the $\bar{Q}$ output of the RS latch 188 through G23. If this subsystem is busy, the output of G23 is in a zero state and the output of G22 is in a one state when SEL4 shifts from zero to one, and vice versa if this subsystem is not busy. A CLR and a simultaneous SEL4 clear FF6 without clearing FF5. Thus, the subsystems busy/done states is made available to the Nova

computer in the manner specified by its manufacturer, and the program can therefore test this status.

FIG. 12 is a block diagram of output busy/done logic suitable for use in the dial-up port illustrated in FIG. 7 and comprises: an RS latch 194; five two-input NAND gates designated G25-G29; two two-input AND gates designated G24 and G30; two D flip-flops designated FF7 and FF8; and, an inverter designated I6.

TBMT is applied to one input of G28 and TBMT is applied to one input of G30. $\overline{\text{IORST}}$ is applied to one input of G24. CLR is applied to one input of G25. SEL3 is applied to the second input of G25, one input of G26, one input of G28 and one input of G29. STRT is applied to the second input of G26. DATA6 is applied to the D input of FF7. MSKO is applied to the C input of FF7 and RQENB is applied to the C input of FF8.

The output of G25 is connected to the second input of G24 and the output of G24 is connected to the S input of RS latch 194. The output of G24 is also connected to the S input of FF8. The output of G26 is connected to the R input of RS latch 194. The Q output of latch 194 is connected to the second input of G30. The output of G30 is connected to the second input of G29 and to one input of G27. The $\overline{\text{Q}}$ output of FF7 is connected to the second input of G27. The output of G27 is connected to the D input of FF8.

The output of G28 is designated SELB and the output of G29 is designated SELD. The Q output of FF8 is designated IRQ3 and the $\overline{\text{Q}}$ output of FF8 is designated $\overline{\text{IRQ3}}$. The $\overline{\text{Q}}$ output of FF8 is applied to the input of I6 and the output of I6 is designated INTR. SELB and SELD are applied to the computer and IRQ3, $\overline{\text{IRQ3}}$ and INTR are applied to the priority encoder.

In operation, the output busy/done logic essentially performs the same function as the input busy/done logic in that it senses the status of the transmitter output of the serial/parallel/serial converter and, in accordance therewith, controls the binary states of the IRQ3, $\overline{\text{IRQ3}}$, INTR, SELB and SELD outputs. More specifically, when the serial/parallel/serial converter is converting parallel data signals from the computer into a serial output for transmission to the remote keyboard, TBMT signal is in a zero state and $\overline{\text{TBMT}}$ is in a one state. Because TBMT is in a zero state, the output of G30 is in a zero state. At the end of transmission, when RQENB clocks FF8, $\overline{\text{IRQ3}}$ goes to a zero state, IRQ3 goes to a one state and INTR goes to a zero state. Thus, the priority encoder is presented with an interrupt request (INTR) and information (IRQ3 and $\overline{\text{IRQ3}}$) regarding the location of the interrupt request. In addition, when an SEL3 one interrogates TBMT and the output of G30, SELB goes to zero and SELD goes to one if the transmitter is busy and vice versa if it is done. Thus, the computer is directly informed of the busy (or done) state of the output of the serial/parallel/serial converter (that is, the output to the remote keyboard). $\overline{\text{IORST}}$ sets RS latch 194 and FF8. CLR and SEL3 in combination also set the RS latch 194, and STRT and SEL3 in combination reset the RS latch. By combination is meant that if the select logic places SEL3 in a one state when the computer causes STRT or CLR to achieve one states, the associated set or reset operation occurs.

FIG. 13 illustrates a serial/parallel/serial converter suitable for use by the dial-up port and comprises: a

universal asynchronous receiver/transmitter designated UAR/T; five two-input NAND gates designated G31-G35; two inverters designated I7 and I8; a capacitor designated C2; and two D flip-flops designated FF9 and FF10. A universal asynchronous receiver/transmitter of the type illustrated in FIG. 13 is available from different sources. One source is the General Instruments Corporation, Integrated Circuits Division, 600 West John Street, Hicksville, New York, 11802. For ease of understanding, a UAR/T of the type produced by General Instruments Corporation has been illustrated in FIG. 13. The device is housed in a 40 pin DIP package and the output terminals of the package are set forth in FIG. 13. Without going into the matter in great detail, a UAR/T is a device that can receive either parallel or serial binary information and transmit either parallel or serial information. In other words, the device can receive a serial input and generate an associated parallel output or it may receive a parallel input and generate a serial output. The rate of conversion of the signals from parallel to serial or vice versa is determined by clocking signals applied to the serial/parallel/serial converter at both TCP (transmitter clock pulse) and RCP (receiver clock pulse) inputs. In accordance with the rate of receipt of clock pulses, the output is converted from parallel to serial form or vice versa. For a more complete description of UAR/T, reference is hereby made to an article entitled "One-Chip 'UAR/Ts' for Telecommunications" contained in a publication entitled EDN/EDE and dated November 1, 1971, Volume 16, No. 21, on page 53.

The VCC input of the UAR/T is connected to +V1 and the VGG input is connected to a negative voltage source designated -V1. A capacitor C2 is connected between VGG and ground. The RDE input of the UAR/T is connected to ground, and outputs RD1 to RD8 are connected to the character gates 184 of the dial-up port. The PE output of the UAR/T is connected to one input of G32 and the FE output is connected to one input of G33. The OR output of the UAR/T is connected to one input of G34. The $\overline{\text{SWE}}$ input of UAR/T is connected to ground. The RCP and TCP inputs are connected to the output of the BAUD rate selector 186 of the privileged dial-up port. The BAUD rate selector input is also connected to the C inputs of FF9 and FF10 and to one input of G35. An RDA conductor from the character gates is connected to the RDA terminal of the UAR/T and to the R input of FF9. The DA output is connected to the D input of FF9 and to a conductor designated DA. The SI input of the UAR/T is connected to a conductor designated DATA IN and receives serial keyboard data from the interface circuit previously described.

The XR input of the UAR/T is connected to conductor 125 (from the connect/disconnect logic 172 of the dial-up port). The TBMT output of the UAR/T is connected through I8 to a conductor designated TBMT. The output of I8 is connected through I7 to a conductor designated TBMT. TBMT and $\overline{\text{TBMT}}$ are applied to the output busy/done logic previously described.

A DOA instruction from the computer is applied to one input of G31. An SEL2 signal from the select logic 164 is applied to the second input of G31. The output of G31 is connected to the $\overline{\text{DS}}$ input of the UAR/T. The EOC terminal of the UAR/T is unconnected. The SO terminal of the UAR/T is connected to a conductor designated DATA OUT which is connected to the in-

terface illustrated in FIG. 5 and previously described. The DB1-DB8 inputs of the UAR/T are connected so as to receive parallel data from the computer. This data, if it is to be transmitted to the remote keyboard location, is converted by the UAR/T into a serial output generated at the SO terminal. The CS, NB1, NB2 and EPS inputs of the UAR/T are connected to +V1. The NP terminal is connected to ground and the TSB input is connected to a second output of the BAUD rate selector.

The Q output of FF9 is connected to the second inputs of G32-G34 and to the D input of FF10. The outputs of G32-G34 are designated $\overline{PE}$, $\overline{FE}$ and $\overline{OR}$ respectively. The $\overline{Q}$ output of FF10 is connected to the second input of G35. The output of G35 is designated NEW DATA.

In operation, the UAR/T operates in a conventional manner in accordance with its control inputs and the timing signals generated by the BAUD rate selector. Serial data from the interface is received at the SI terminal and is converted into parallel outputs on RD1-RD8 in a timed manner. If a parity error, framing error or overrun condition is sensed, $\overline{PE}$, $\overline{FE}$ or $\overline{OR}$ achieve zero states, as the case may be, as G32-G34 are gated by the Q output of FF9. In addition, when new data is being received, after a time delay caused by the shifting of FF9 and FF10, NEW DATA achieves a zero state. The TBMT and $\overline{TBMT}$ signals are sensed by the output busy/done logic and used in the manner previously described. DA is inverted and applied to the input busy/done logic.

FIG. 14 is a block diagram illustrating character gates suitable for use in the dial-up port and comprises: eight two-input NAND gates designated G36-G43; a two-input AND gate designated G44; and, an inverter designated I8A. The RD1-RD8 outputs of the UAR/T of the serial/parallel/serial converter are connected each to one input of G36-G43. The second inputs of G36-G43 are connected to the output of G44. DIA is applied to one input of G44 and SEL2 is applied to the second input of G44. The output of G44 is also applied to the input of I8A. The output of I8A is the signal designated $\overline{RDA}$ applied to the serial/parallel/serial converter 182.

It will be appreciated from viewing FIG. 14 that the character gates merely gate the RD1-RD8 outputs of the UAR/T to a plurality of output lines designated DATA8-DATA15 in accordance with a signal generated by G44. That is, when DIA and SEL2 both shift to one state, the output of G44 achieves a one state and gates G36-G43 "on." I8A then applies a zero to the UAR/T.

FIG. 15 is a block diagram of BAUD rate selector logic suitable for use in the dial-up port. The BAUD rate selector logic illustrated in FIG. 15 comprises: a JK flip-flop designated FF11; four two-input NAND gates designated G45-G48; and, an inverter designated I8. Computer instructions designated DATA14 and DATA15 are applied to the J and K inputs, respectively, of FF11. A DOC instruction is applied to one input of G45 and SEL2 is applied to the second input of G45. The output of G45 is connected through I8 to the C input of FF11. The Q output of FF11 is connected to one input of G46. The second input of G46 is a 4,800Hz timing signal generated by the frequency synthesizer in the manner hereinafter described. The $\overline{Q}$ output of FF11 is connected to the TSB terminal of the UAR/T of the serial/parallel/serial converter. The $\overline{Q}$

output of FF11 is also connected to one input of G47. The second input of G47 is a 1,760Hz timing signal also generated by the frequency synthesizer. The outputs of G46 and G47 are, respectively, connected to the two inputs of G48. The output of G48 is connected to the TCP and RCP terminals of the UAR/T. Conductor 125 is connected to the R input of FF11.

In addition, DATA14 and DATA15 define the status of FF11 when it is clocked by DOC, as gated by SEL2. FF11 is reset when the RS latch 188 of the connect/disconnect logic is reset. Depending upon the status of the Q and $\overline{Q}$ of FF11, either G46 or G47 passes its associated timing signals from the frequency synthesizer to G48 which in turn applies them to the TCP and RCP inputs of the UAR/T. The TSB signal controls the number of stop bits to be appended to each transmitted character.

FREQUENCY SYNTHESIZER

FIG. 16 is a block diagram of a frequency synthesizer suitable for use by the preferred embodiment of the invention illustrated in FIG. 1 and comprises: a divide-by-five or six circuit 200; a phase detector 202; a charge pump circuit 204; a low pass filter 206; a voltage control oscillator (VCO) 208; a divide-by- 2^{16} circuit 210; BAUD rate dividers 212; and, a divide-by-10 circuit 214.

In operation, standard commercially generated 50 or 60 Hz power is applied to the divide-by-five or six circuit. In accordance with this frequency, the divide-by-five or six circuit divides by either five or six, as determined by a switch setting, so that a 10Hz output signal is created. This 10Hz signal is applied to one input of the phase detector 202. The output of the phase detector is connected to the charge pump circuit which senses a voltage level generated in the phase detector and related to the frequency difference between its two inputs. This voltage is applied through the low pass filter 206 to the input of the VCO 208. In accordance with the voltage value applied to its input, the VCO generates an output signal having a predetermined frequency. That is, the frequency of the output of the VCO is related to and changes with the voltage value of its input voltage. The desired output frequency is 10×2^{16} Hz. In this regard, reference is hereby made to "Phase Locked Loop Data" published by Motorola, Inc., 1973.

The output of the VCO is applied to the input of the divide-by- 2^{16} circuit 210 and to the input of the BAUD rate dividers 212. The output of the divide-by- 2^{16} is a 10Hz signal, which is applied to the second input of the phase detector 202 and to one input of the divide-by-10 circuit 214. Thus, the two inputs of the phase detector are 10Hz signals when the phase lock loop is locked. When it is locked, the VCO is generating the desired 10×2^{16} Hz signal. This signal is divided by the BAUD rate dividers 212 to generate the 1760Hz and 4800Hz signals needed by the BAUD rate selector logic of the dial-up port. In addition, a 2727 signal is generated and utilized by the newline interface in the manner hereinafter described. In addition, other timing signals of different frequencies may be generated, if desired.

The divide-by-10 circuit divides the 10Hz output of the divide-by- 2^{16} circuit into a 1Hz output which is utilized by the clock and thermometer interface 170 of the computer control logic illustrated in FIG. 6 and hereinafter described.

SELECT LOGIC

FIG. 17 illustrates a select logic circuit suitable for use by the computer control logic illustrated in FIG. 6 and comprises: a three-input NAND gate designated G45; a four-input NAND gate designated G46; two two-input NAND gates designated G47 and G48; a decoder 216; and six inverters designated I9-I14.

It should be noted that a plurality of select logic circuits of the type illustrated in FIG. 17 are used in an actual embodiment of the invention to select from the various subsystems of which there are many more than the few illustrated herein for description purposes. The computer generated $\overline{DS0}$ - $\overline{DS5}$ instructions are received by each select logic circuit. One of them is enabled and creates one of six select signals SEL2-SEL7. The generated SEL signal (zero-to-one shift) is utilized in the manner heretofore and hereinafter described to control the operation of one of the various subsystems of the control logic.

Turning now to a description of the select logic illustrated in FIG. 17, $\overline{DS0}$ - $\overline{DS2}$ are applied to the three inputs of G45. The output of G45 is connected to the enable input of the decoder 216. Thus, in the illustrated select logic, $\overline{DS0}$ - $\overline{DS2}$ form the selection code for selecting the illustrated select logic. In other words, when the output of G45 is in a zero state, it enables the applied 216 so that it decodes the signals applied to its other inputs. $\overline{DS3}$ - $\overline{DS5}$ are applied to the other inputs (A, B and C) of the decoder. In accordance with the status of the $\overline{DS3}$ - $\overline{DS5}$ signals, the decoder 216 generates a zero/one code on its six outputs (1-6). One output (6) is applied through I12 in series with I13 to one input of G46 and one input of G47. The junction between I12 and I13 is connected through I14 to one input of G48 and a second input of G46. Another output (4) of the decoder is applied to a third input of G46 and a second input of G48. A third output (5) of the decoder is applied to the fourth input of G46 and a second input of G47.

The output of G48 is SEL3 and is applied to the dial-up port in the manner heretofore described. The output of G47 is SEL4 and is also applied to the dial-up port in the manner previously described. The output of G46 is SEL2 and is applied to the dial-up port in the manner previously described.

The fourth output (3) of the decoder is applied to the input of I11. The output of I11 is SEL5 and is applied to the clock and thermometer interface 170 in the manner described hereinafter. The fifth output (2) of the decoder is applied to the input of I10. The output of I10 is SEL6 and is applied to the output display logic 168 of the computer control logic as hereinafter described. The sixth output (1) of the decoder is applied to the input of I9. The output of I9 is SEL7 and is applied to the newline interface 162 as hereinafter described.

In summary, the select logic illustrated in FIG. 17 is enabled if $\overline{DS0}$, $\overline{DS1}$ and $\overline{DS2}$ are all in one states. When this code occurs, $\overline{DS3}$, $\overline{DS4}$ and $\overline{DS5}$ cause one of the SEL2-SEL7 signals to enable the circuitry to which it is connected for performance of the function or functions related to that SEL signal.

PRIORITY ENCODER

A priority encoder suitable for use in the computer control logic illustrated in FIG. 6 is illustrated in FIG. 18 and comprises: two four-input NAND gates desig-

nated G50 and G51; three three-input NAND gates designated G52, G53 and G54; a two-input AND gate designated G55; six two-input NAND gates designated G56-G61; four inverters designated I15-I18; a capacitor designated C3; and, three resistors designated R10, R11 and R12. The $\overline{IRQ}$ outputs of all of the heretofore and hereinafter described subsystems of the computer control logic are connected to one of the inputs of G56 through I17. Thus any of these outputs gate G56 into a signal passing state. $\overline{INTP\ IN}$ is from a previous logic board and indicates the status of the previous logic boards, i.e., those having a higher priority.

More specifically, $\overline{IRQ3}$ is applied to one input of G58. $\overline{IRQ3}$ is applied to one input of G52 and one input of G57. $\overline{IRQ4}$ is applied to one input of G50, a second input of G52 and one input of G57. $\overline{IRQ5}$, which is generated by the clock and thermometer interface in the manner hereinafter described, is applied to a second input of G50, one input of G54 and one input of G58. $\overline{IRQ6}$, which is generated by the output display logic in the manner hereinafter described, is applied to the third input of G50, the third input of G52 and one input of G53. $\overline{IRQ7}$, which is generated by the newline interface in the manner hereinafter described, is applied to the fourth input of G50, one input of G54 and the second input of G53.

A computer-generated instruction designated INTA, to designate interrupt acknowledge, is applied to the second input of G51 and through R10 in series with C3 to ground. The junction between R10 and C3 is connected to the third input of G51.

The output of G50 is connected to one input of G59 and through I16 to a second input of G58. The output of G58 is connected to the fourth input of G51 and through I17 to the second input of G56. The output of G51 is connected through I18 to one input each of G59, G60 and G61. The output of G56 is a signal designated $\overline{INTP\ OUT}$ and is passed on to lower priority boards. The output of I56 is also connected through R11 to +V1 and through R12 to ground. R11 and R12 have slightly different resistive values. The output of G54 is connected to the second input of G60, and the output of G55 is connected to the second input of G61.

The output of G59 is designated DATA13 and is applied to the computer. The output of G60 is designated DATA14 and is applied to the computer. The output of G61 is designated DATA15 and is also applied to the computer.

Initially, assuming there are not interrupts generated and no interrupt identification signals being generated, i.e., $\overline{INTP\ IN}$ is in a zero state, and $\overline{IRQ3}$ - $\overline{IRQ7}$ are all in one states, $\overline{IRQ3}$ being in a zero state, the output of I17 is in a one state, and the output of I15 is in a one state. Thus, $\overline{INTP\ OUT}$ is in a zero state. When any interrupt signal ($\overline{INTR}$) is generated, the computer is directly informed of an interrupt request. Assuming the illustrated priority encoder is causing the interrupt (i.e., one of its $\overline{IRQ}$ inputs is in a zero state), the output of G58 through I17 identifies this priority encoder as the one creating the interrupt.

In accordance with the status of the $\overline{IRQ}$ signals, the other inputs to G59-G61 create a specific DATA13-DATA15 code. The computer interprets this information and, in accordance therewith, generates a $\overline{DS0}$ - $\overline{DS5}$ selection code, which creates one of the SEL one's in the manner previously described. If more than one interrupt simultaneously occurs, the DATA1-

3-DATA15 code relates to the subsystem having the highest "priority;" as determined by the logic of the priority encoder.

It should be noted that the priority encoder illustrated in FIG. 18 is only one of a plurality of such systems located in an overall system formed in accordance with the invention. That is, as previously indicated, the presently described system as illustrated in FIG. 1 is a simplification of an overall system incorporating the invention. As such, there are additional newswire interfaces, dial-up ports, etc., in an actual embodiment. The interrupts created by these systems may be connected to other priority encoders similar to that illustrated in FIG. 18. $\overline{\text{INTP}} \overline{\text{IN}}$ provides information from higher order priority encoders to the illustrated priority encoder regarding their requests for interrupts. If a higher priority encoder is requesting an interrupt, this encoder's $\overline{\text{INTP}} \overline{\text{IN}}$ will be in a one state and it will be unable to respond to an INTA. When an interrupt occurs, the computer interrogates all of the subsystems by the generation of an INTA, which as described above will elicit response from only the highest priority subsystem presently requesting an interrupt. The subsystem's response enables the computer to locate the exact cause or causes of the interrupt, and it takes action to eliminate the causes, i.e., receives data or transmits it, as the case may be. In this regard, attention is directed to the publication entitled "How to Use the Nova Computers" referenced above.

NEWSLINE INTERFACE

FIG. 19 is a block diagram of a newswire interface suitable for use in the computer control logic illustrated in FIG. 6 and comprises: a newswire counter 218; a one of eight decoder 220; a scan control 222; an enable register 224, newswire gates 226; newswire busy/done logic 228; eight UAR/T's 230; an internal data bus 232; character gates 234; a read acknowledge circuit 236; and, error gates 238.

Basically, the newswire counter receives DATA13-DATA15 instructions from the computer. The newswire counter may be set by these instructions to enable through the one of eight decoder 220 a particular one of the UAR/T's. In accordance therewith, one of the eight UAR/T's 230 informs the newswire busy/done logic if it has a "character" ready for readout. The parallel output of the chosen UAR/T is applied by character gates 234 to the computer (DATA8-DATA15).

If an overflow, parity error or framing error occurs, the error gates 238 sense this information and generate a computer information code (DATA13-DATA15) to indicate the relevant condition. The read acknowledge circuit 236 acknowledges the receipt of data by the computer. The enable register 224 senses the identity of the chosen UAR/T and acts to terminate scanning.

The newswire gates inform the computer of the identity of the chosen UAR/T at any particular point in time (DATA13-DATA15).

A preferred embodiment of a newswire counter suitable for use in the newswire interface illustrated in FIG. 19 is illustrated in FIG. 20 and comprises a counter adapted to receive DATA13-DATA15. The counter includes a load input, which receives signals on a conductor designated 201 and a clock input which receives signals on a conductor designated 203. When the signal on line 201 drops to zero, DATA13-DATA15 are loaded into the newswire counter. Zero clock pulses on

line 203 thereafter cause the scanning of these inputs which create related signals on three output conductors designated 205, 207 and 209. These signals, in turn, cause the one of eight decoder 220 to sequentially enable the eight UAR/T's 230.

FIG. 21 is a block diagram of a scan control suitable for use in the newswire interface illustrated in FIG. 19 and comprises: two two-input NAND gates designated G62 and G63; a two-input AND gate designated G64; a three-input NAND gate designated G65; and, two D flip-flops designated FF15 and FF16. DOB is applied to one input of G62. SEL7 is applied to the second input of G62 and to one input of G63. The output of G62 is applied via conductor 201 to the load input of the newswire counter illustrated in FIG. 20. In addition, the output of G62 is applied to the S input of FF15 and to the R input of FF16. The 2727Hz signal generated by the frequency synthesizer is applied to the C input of FF15. IO PULSE is applied to the second input of G63. The output of G63 is applied to the S input of FF16. The D input of FF16 is connected to ground, and the clock input of FF16 receives clock pulses occurring on a conductor designated 211. Conductor 211 carries signals generated by the newswire busy/done logic illustrated in FIG. 24 and hereinafter described.

The Q output of FF15 is applied to conductor 203 and, thus, to the clock input of the newswire counter illustrated in FIG. 20. The Q output of FF15 is also applied via a conductor designated 215 to the newswire busy/done logic. Further, the Q output of FF15 is connected to one input of G65. The Q output of FF16 is applied to one input of G64. A conductor designated 213 is connected to the second input of G64. Conductor 213 also carries a signal generated by the newswire busy/done logic. The output of G64 is connected to the second input of G65. A conductor designated Z is connected to the third input of G65. Conductor Z carries a signal generated by the read/acknowledge circuit (FIG. 26) in the manner hereinafter described.

In operation, when SEL7 shifts from zero to one, in accordance with the computer instructions applied to the select logic, and DOB achieves a one state, the output of G62 causes the DATA13-DATA15 inputs to be loaded into the newswire counter. In addition, FF15 is set and FF16 is reset. Thereafter, the 2727Hz signal continuously clocks FF15, and the Q output of FF15 changes state each time a 2727Hz clock signal occurs. This action takes place because the state of the output of G65 is dependent on the state of the Q output of FF15 as long as the signal on line Z is a one and the output of G64 is a one. Thus, the Q output of FF15 clocks the newswire counter at onehalf the 2727Hz frequency rate, or any other chosen rate.

The signal on conductor 213 reflects the busy state of the newswire busy/done logic. As long as the newswire is busy, i.e., receiving data without having a completed character ready for transmission to *, i.e., receiving data, the signal on conductor 213 is in a one state, as will be better understood from the following description of the newswire busy/done logic. When scanning is to terminate, the signal on conductor 213 shifts to zero and ends the application of pulses to conductor 203. The signal on conductor Z is normally a one, except during the period of time that the computer is acknowledging the receipt of data. When this instruction occurs, as determined by the read acknowledge circuit 236, the signal on conductor Z drops to zero, which event inhibits the operation of G65 until the read acknowledge period ends. If an IO PULSE

instruction occurs (along with an SEL7 one) at any time during the operation of the newswire subsystem, FF16 is set. This action through G64 also inhibits the operation of G65. A clock pulse on conductor 211 following this action resets FF16 because the D input of FF16 is connected to ground. Or, FF16 can be reset by the SEL7, DOB combination described above.

*the computer

FIG. 22 illustrates an enable register suitable for use in the newswire interface illustrated in FIG. 19. The enable register illustrated in FIG. 22 comprises a register 240; and, a two-input NAND gate designated G66. DATA15 is applied to the load input of the register 240. In addition, conductors 205, 207 and 209 are connected to sense inputs of register 240. SEL7 is applied to one input of G66 and DOC is applied to the second input of G66. When SEL7 and DOC simultaneously achieve one states, the register 240 is clocked. If DATA15 has loaded the register at this time, the state of the signals on conductors 205, 207 and 209 determines whether a zero or a one is applied to a conductor designated 217. A one on this conductor enables the newswire busy/done logic, so that it can receive a DA one from the internal data bus. Thus, the enable register provides an enabling function controlled by computer instructions.

FIG. 23 is a block diagram illustrating newswire gates 226 suitable for use in the newswire interface illustrated in FIG. 19. The newswire gates illustrated in FIG. 23 comprise three two-input NAND gates designated G67, G68, and G69; and, one two-input AND gate designated G70. Conductors 205, 207 and 209 are respectively connected each to one input of G67, G68 and G69. SEL7 is applied to one input of G70 and DIB is applied to the second input of G70. The output of G70 is connected to the second inputs of G67 and G68 and G69. The output of G67 is a signal designated $\overline{\text{DATA13}}$, the output of G68 is a signal designated $\overline{\text{DATA14}}$, and the output of G69 is a signal designated $\overline{\text{DATA15}}$.

It will be appreciated from reviewing FIG. 23 that the newswire gates control the application of DATA13, DATA14 and DATA15 to the computer when called for by SEL7 and DIB. These signals are directly related to the signals defining the chosen UAR/T.

FIG. 24 is a block diagram illustrating newswire busy/done logic suitable for use in the newswire interface illustrated in FIG. 19 and comprises: two two-input AND gates designated G71 and G72; five two-input NAND gates designated G73-G77; one three-input NAND gate designated G78; two inverters designated I20 and I21; and, four D flip-flops designated FF17-FF20.

Conductor 215 from the scan control (FIG. 21) is connected to the C input of FF17. STRT is applied to one input of G74 and SEL7 is applied to the second input of G74. SEL7 is also applied to one input of G73, one input of G77, and one input of G75. CLR is applied to the second input of G73. $\overline{\text{IORST}}$ is applied to one input of G72 and the R input of FF20. The output of G73 is connected to the second input of G72. The output of G72 is connected to the input of I20. The output of I20 is connected to the conductor 211 which is connected to the C input of FF16 of the scan control, as previously described. The output of G72 is also connected to the T input of FF18 and to one input of G71.

The output of G74 is connected to the second input of G71 and to the S input of FF18. The output of G71 is connected to the S inputs of FF17 and FF19. The Q output of FF17 is applied to conductor 213 which is

connected to one input of G64 of the scan control, as previously described. The $\overline{\text{Q}}$ output of FF17 is connected to the C input of FF18, the second input of G75 and one input of G76. The Q output of FF18 is connected to one input of G78 and the second input of G77. Conductor 217 from the enable register is connected to the second input of G78. DA (from the chosen UAR/T via the internal data bus 232) is applied to the third input of G78. DA is the opposite state of $\overline{\text{DA}}$.

The output of G78 is connected to the D input of FF17. The output of G76 is connected to the D input of FF19. RQENB is applied to the C input of FF19. DATA3 is applied to the D input of FF20 and MSKO is applied to the C input of FF20. The Q output of FF20 is connected to the second input of G76. The output of G75 is a $\overline{\text{SELD}}$ signal. The Q output of FF19 is the $\overline{\text{IRQ7}}$ signal which is applied to the priority encoder for use in the manner previously described. The $\overline{\text{Q}}$ output of FF19, through I21, creates the $\overline{\text{INTR}}$ signal, which is also applied to the priority encoder for use in the manner previously described. The output of G77 in SELB.

In operation, the newswire busy/done logic operates in a manner generally similar to the busy/done logic systems previously described -- that is, when the NEWSLINE DATA INPUT receives suitable signals, such as AP or UPI signals in a suitable format such as ASCII (American Standard Code for Information Interchange), the newswire busy/done logic indicates that the newswire interface is busy (scan in progress). When a character is ready for transmission to the computer, the newswire busy/done logic indicates that the newswire interface is done.

Initially, the input of G78 from Q of FF18 is in a one state. When the selected UAR/T causes DA to shift to a one state, the output of G78 shifts to a zero state, if conductor 217 carries a one. This shift is clocked into FF17, causing its Q output to go to a one state. The next RQENB one pulse clocks the now zero output of G76 into FF19, creating an $\overline{\text{IRQ7}}$ zero and an $\overline{\text{INTR}}$ zero. These zeros are sensed by the priority encoder and used in the manner previously described. If an SEL7 one now interrogates DA, through G78, the output of G75 will be a zero to indicate the done (DA) status of the enabled (selected) UAR/T. When the Q output of FF17 shifts to zero, it inhibits further scanning via conductor 213.

STRT and SEL7 reaching one states together initially set FF18, and CLR and SEL7 reaching one states together reset FF18 and clock FF16 of the scan control. $\overline{\text{IORST}}$ also resets FF18 and clocks FF16 of the scan control. $\overline{\text{IORST}}$ also resets FF20. DATA3 and MSKO provide for the selective masking interrogation of the newswire busy/done logic.

It will be appreciated from the foregoing brief discussion that the newswire busy/done logic provides an indication of the busy or done status of the newswire interface illustrated in FIG. 19. In addition, it provides a signal to the priority encoder requesting an interrupt when data is available. In addition, it applies a signal to the priority encoder which identifies the location of the interrupt.

FIG. 25 is a diagram of a UAR/T suitable for use in the newswire interface. As previously stated, eight similar UAR/T's are utilized by the newswire interface, or more or less, as necessary. The UAR/T illustrated in FIG. 25 is the same as the UAR/T device previously described as produced by General Instrument Corpora-

tion of Southboro, Massachusetts. However, only its serial to parallel conversion function is used, rather than both serial to parallel and parallel to serial. The 2727 Hz signal from the frequency synthesizer is applied to the TCP and RCP inputs of the illustrated UAR/T. The VCC terminal is connected to +V1 and the VGG terminal is connected to -V1. The ground terminal is connected to ground. The $\overline{\text{RDE}}$ and $\overline{\text{SWE}}$ terminals are connected to receive a select signal from the one of eight decoder 220. In other words, the signal on this input determines whether or not the illustrated UAR/T has been chosen. The DA, OR, FE, PE and RD1-RD8 terminals are all connected to an internal data bus. The internal data bus is connected to similar terminals of all of the UAR/T's. However, only the chosen UAR/T causes signals to pass through the internal data bus to the character gates 234 and the other related subsystems. The $\overline{\text{RDA}}$ terminal is connected to the output of a two-input NAND gate designated G79. One input of G79 is connected to the internal data bus and receives a read acknowledgement signal from the read acknowledgment circuit 236. The second input of G79 is connected to the output of an inverter designated I22. The input of I22 is the select conductor.

The SI terminal of the UAR/T is connected to the NEWSLINE DATA INPUT conductor. On the transmit side of the UAR/T, EPS is connected to +V1, and NB1 is connected to ground. NB2 is connected through a resistor R14 to +V1. In addition, NB2 is connected to the input of a second inverter designated I23 and through a jumper J to ground. The jumper is used when the incoming information is not in ASCII format. If the incoming information is in ASCII format, the jumper is eliminated. The output of I23 is connected to the NP terminal of the UAR/T. The TSB and CS terminals are connected to +V1, as in the DS terminal. The remaining terminals are uncorrected.

In operation, as previously indicated, the UAR/T operates as a serial-to-parallel converter. It receives new-line information, and when such information becomes available, it causes a signal to be applied to the new-line busy/done logic which, in turn, requests an interrupt. In a standard manner, the UAR/T transfers the serial input information into parallel information at the chosen 2727Hz rate, and applied this information to the internal data bus. DA provides an indication that data is available and OR, FE and PE provide overrun, framing error and parity error information.

A read acknowledge circuit suitable for use by the new-line interface is illustrated in FIG. 26 and comprises a two-input AND gate designated G79A and a one-shot 250. SEL7 is applied to one input of G79A and DIA is applied to the second input of G79A. The output of G79A is connected to a conductor designated 219, which is connected to the character gates illustrated in FIG. 27 and hereinafter described. The output of G79A is also applied to the input of the one-shot 250, to cause it to shift its output status for a short period of time, as is well known by those skilled in the art. The Q output of the one-shot is connected to a conductor designated 221, which is connected through the internal data bus to the UAR/T's. The $\overline{\text{Q}}$ output of the one-shot 250 is connected to the conductor designated Z whereby it is applied to the scan control illustrated in FIG. 26 and previously described.

In operation, when the computer is informed that data is available, it causes DIA and SEL7 to simultaneously achieve one states. This action triggers the one

shot 250. Triggering the one shot causes a one on conductor 221 which triggers the $\overline{\text{RDA}}$ input of the chosen UAR/T allowing it to receive the next set of new-line information and convert it into DB1-DB8 signals. The zero on conductor Z during this period of time inhibits G65 of the scan control.

FIG. 27 is a block diagram illustrating character gates suitable for use in the new-line interface and comprises eight two-input NAND gates designated G80-G87. The RD1-RD8 outputs of the internal data bus from the UAR/T's are connected each to one input of G80-G87, respectively. The other inputs of G80-G87 are connected to conductor 219, which is connected to the output of G79A of the read acknowledgment circuit illustrated in FIG. 26. Thus, when the output of G79A is in a one state, RD1-RD8 are applied, in inverted form, to a plurality of parallel output conductors as signals designated DATA8-DATA15.

FIG. 28 is a block diagram illustrating error gates suitable for use in the new-line interface and comprises a two-input AND gate designated G88; and, three two-input NAND gates designated G89-G91. G88 receives SEL7 and DIC signals. The output of G88 is connected to one input of each of G89-G91. The second input of G89 is connected to the PE terminal of the internal data bus to receive parity error signals generated by the UAR/Ts. The second input of G90 is connected to the FE terminal of the internal data bus to receive framing error signals generated by the UAR/Ts. The second input of G91 is connected to the OR terminal of the internal data bus to receive overrun error signals generated by the UAR/Ts. The output of G89 is a signal designated DATA13. The output of G90 is a signal designated DATA14, and the output of G91 is a signal designated DATA15. These signals, thus, provide the computer with notice of parity, framing and overrun error conditions, should they occur.

OUTPUT DISPLAY LOGIC

FIG. 29 is a block diagram illustrating output display logic suitable for use by the computer control logic illustrated in FIG. 6. The output display logic illustrated in FIG. 29 comprises: output display busy/done logic 252; a display load generator 254; a word assembly register 256; and a display selector register 258.

The output display busy/done logic 252, as with previously described busy/done logic, determines whether the output display logic is busy or idle and generates an interrupt request ($\overline{\text{INTR}}$) when it desires to perform its function. In addition, the output busy/done logic display generates an $\overline{\text{IRQ6}}$ signal to designate the location of the interrupt request. Further, it generates $\overline{\text{SELB}}$ and $\overline{\text{SELD}}$ signals to indicate the busy/done status of the output display logic.

The display load generator senses the status of the character generation subsystems and generates a load signal when the character generation subsystem are ready to receive instructions. The word assembly register passes computer instructions which define characters to the character generator. The display selector register passes computer instructions to the character address selector. These instructions define the location of the particular characters on the output of the word assembly register. Thus, the output display logic generally controls the formation and location of characters to be displayed.

FIG. 30 is a block diagram illustrating output display busy/done logic suitable for use by the output display logic illustrated in FIG. 29. The output display busy/-

done logic illustrated in FIG. 30 comprises: one three-input NAND gate designated G95; three two-input AND gates designated G92, G93 and G94; two-input NAND gates designated G96-G102; an inverter designated seven I24; two JK flip-flops designated FF21 and FF22; and, two D flip-flops designated FF23 and FF24. SEL6 is applied to one input of G95, one input of G96, one input of G99, one input of G100 and one input of G101. IO PULSE is applied to the second input of G95. STRT is applied to the second input of G96. CLR is applied to the second input of G99. IORST is applied to one input of G93 and the R input of FF24.

The output of G95 is connected to the S input of FF21. The output of G92 is connected to the R input of FF21 and the S input of FF23. The output of G96 is connected to one input of G92. The output of G93 is connected to the second input of G92, the reset input of FF22 and a conductor designated 231. Conductor 231 is connected to the display load generator illustrated in FIG. 31 and hereinafter described. The output of G96 is also connected to the set input of FF22 and to a conductor designated 233, which is also connected to the display load generator as hereinafter described. The K input of FF21 is grounded.

A conductor designated 237, from the display load generator, is connected to the C input of FF21 and to the C input of FF22. A conductor designated 239, from the display selector register, is connected to one input of G97. The $\bar{Q}$ output of FF21 is connected to the second input of G97. The output of G97 is connected to the K input of FF22 and to one input of G98. The J input of FF22 is connected to ground. The Q output of FF21 is connected to one input of G94. The $\bar{Q}$ output of FF21 is connected to the second input of G97. The Q output of FF22 is connected to the J input of FF21 and the second input of G98. The Q output of FF22 is also connected to one input of G101 and to a conductor designated 235. Conductor 235 is connected to the display load generator. The $\bar{Q}$ output of FF22 is connected to the second input of G94 and to the third input of G95. The output of G98 is applied to a conductor designated 243 connected to the word assembly register hereinafter described. The output of G94 is connected to one input of G102 and to the second input of G100. DATA2 is applied to the D input of FF24, and MSKO is applied to the C input of FF24. The $\bar{Q}$ output of FF24 is connected to the second input of G102. The output of G102 is connected to the D input of FF23. ROENB is applied to the C input of FF23. The Q output of FF23 is the $\overline{IRQ6}$ signal. The $\bar{Q}$ output of FF23 is connected to the input of I24. The output of I24 is the $\overline{INTR}$ signal. The output of G100 is the $\overline{SELD}$ signal. The output of G101 is the $\overline{SELB}$ signal. In the manner previously described, $\overline{INTR}$ and $\overline{IRQ6}$ are applied to the priority encoder 166 to request an interrupt and to identify the source of the interrupt. $\overline{SELB}$ and $\overline{SELD}$ signals are applied to the computer to indicate the busy/done status of the output display logic.

The signal on conductor 239 controls whether or not an interrupt is to be requested by the output display busy/done logic. That is, conductor 239 senses the status of the hereinafter described display selector register 258. When that register is loaded, a one appears on conductor 239. This one is clocked into FF22 by the next clock pulse appearing on conductor 237. The clock pulses on conductor 237 are created by the display

load generator interrogating the character address selector (FIG. 38) in the manner hereinafter described.

Initially IORST resets FF21, FF22 and FF24, and sets FF23. The next conductor 237 clock pulse following a one appearing on conductor 239 causes FF21 to be set if it hasn't previously been set by a previous clock pulse.

IO PULSE and SEL7 achieving one states simultaneously cause FF21 to set if FF22 is set. STRT and SEL6 achieving one states during the same period of time set FF22, reset FF21 and set FF23. SEL6 and CLR achieving one states during the same period of time reset FF22. FF24 acts to follow the masking technique when FF24 is clocked by MSKO with DATA2 being in a one state.

FIG. 31 is a block diagram illustrating a display load generator suitable for use by the output display logic illustrated in FIG. 29. The display load generator illustrated in FIG. 31 comprises: a monostable multivibrator 260; a D flip-flop designated FF25; and a three-input NAND gate designated G103.

A signal designated READY is applied to the input of the monostable multivibrator 260. This signal is also applied to the S input of FF25. Conductor 231 is connected to the R input of FF25. The D input of FF25 is connected to ground. The Q output of FF25 is applied to conductor 237, which, as previously described, is connected to the C inputs of FF21 and FF22 of the output display busy/done logic. The Q output of FF25 is also connected to one input of G103. Conductors 233 and 235 are, respectively, connected to the second two inputs of G103. The output of G103 is a signal designated LOAD. The $\bar{Q}$ output of the monostable multivibrator is connected to the C input of FF25.

In operation, a READY signal, generated by the hereinafter described character address selector, triggers the monostable multivibrator causing its $\bar{Q}$ output to temporarily achieve a zero state. When this state ends FF25 is clocked. Prior thereto, however, the READY signal set FF25. Thus, clocking of FF25 causes (because of the grounded D input) the Q output of FF25 to drop to zero. This transition clocks FF21 and FF22 of the output display busy/done logic in the manner previously described. In addition, Q going to zero causes LOAD to shift from zero to one. When LOAD returns to zero it creates a load instruction for the character address selector illustrated in FIG. 38 and hereinafter described. This in turn creates another READY zero pulse when the character address selector is ready to receive more information. Hence, the display load generator is essentially a recirculating pulse generator.

FIG. 32 is a block diagram illustrating a display selector register suitable for use in the output display logic illustrated in FIG. 29 and comprises a decoder 262, and a two-input NAND gate designates G104. The register receives eight instruction signals in parallel designated DATA8-DATA15 from the computer. These data signals define the location of a particular character display i.e. its channel. In addition, decoder enable information is contained in these signals. SEL6 is applied to one input of G104 and DOB is applied to the second input of G104. The output of G104 is connected to the load ($\bar{L}$) input of the register 262. The clear ($\bar{CL}$) input of the register receives IORST. Thus, when SEL6 and DOB are both in one states the register, if it is enabled by the DATA8-DATA15 instructions is loaded with

DATA8-DATA15. DATA8-DATA15 is stored by the register and as a result one of the seven parallel outputs achieves a one state. The selected output controls the flow of word assembly information to a particular display channel. In addition, the register generates a one on conductor 239, which, as previously explained is applied to the output display busy/done logic to provide an indication of the busy nature of the display selector register.

FIG. 33 is a block diagram illustrating a word assembly register suitable for use by the output display logic and comprises a first character storage register 264; a second character storage register 266; two inverters designated I25 and I26; and, a two-input NAND gate designated G105.

The first character storage register 264 receives eight parallel character instructions from the computer designated DATA0-DATA7. The second parallel storage register simultaneously receives eight parallel character instructions from the computer designated DATA8-DATA15. Each register has eight outputs. The eight outputs are connected to eight parallel output conductors designated A8-A15 on a one-to-one basis. That is, one output of each register is connected to each output conductor.

Conductor 243 from the output display busy/done logic is connected through I25 to the enable (EN) input of the first character storage register and directly to the enable input of the second character register. IORST is applied to the clear ($\overline{CL}$) input of both registers. DOA is applied to one input of G105 and SEL6 is applied to the second input of G105. The output of G105 is connected through I26 to the load inputs of both the first and the second character registers.

In operation, when SEL6 and DOA both reach one states, the first and second character storage registers are loaded. They are, however, sequentially enabled to apply their inputs to output conductors by pulses occurring on conductor 243. In other words, one character storage register is first enabled, and then the second character storage register is enabled. Thus, the output conductors sequentially carry signals first from one and then from the other of the registers.

TEMPERATURE SENSOR

FIG. 34 is a block diagram of a temperature sensor suitable for generating temperature signals utilized by the preferred embodiment of the invention illustrated in FIG. 1. The temperature sensor illustrated in FIG. 34 comprises an outside temperature probe 268; a comparator 270; a digital-to-analog converter 272; an up-down counter 274; and, counter control logic 276.

As illustrated in FIG. 34, the outside temperature probe 268 comprises two temperature sensitive resistors designated RT1 and RT2 and a pair of resistors designated R14 and R15. One end of RT1 and RT2 are connected together and to ground. R14 is connected between the other ends of RT1 and RT2. The other end of RT2 is also connected through R15 to an input conductor designated REFERENCE. A capacitor designated C4 is connected in parallel with RT2. The junction between R15 and RT2 is also connected to one input of the comparator 270. The reference conductor is connected to the digital-to-analog converter 272 and applies a reference voltage to the temperature probe.

The analog output of the digital-to-analog converter is connected to the second input of the comparator

270. The input of the digital-to-analog converter 272 is connected to the output of the up-down counter 274. The up-down inputs of the up-down counter are connected to outputs of the counter control logic 276 illustrated in FIG. 35 and hereinafter described. In addition, the counter control logic generates a CLEAR output which is applied to the clear input of the up-down counter 274. The counter control logic receives a CLEAR signal from the clock and thermometer interface and generates $\overline{UP}$ and $\overline{DN}$ information signals which are applied to the computer. In addition, a signal designated GOTCHA is received by the counter control logic. This signal is generated by the clock and thermometer interface in the manner hereinafter described. The UP and DN outputs of the comparator are applied to two inputs of the counter control logic 276.

FIG. 35 illustrates counter control logic suitable for use in the temperature sensor illustrated in FIG. 34 and comprises: a one-shot 278; two D flip-flops designated FF26 and FF27; three inverters designated I27, I28 and I29; and, two two-input NAND gates designated G106 and G107. The UP output from the comparator is connected to the D input of FF26, and the DN output from the comparator is connected to the D input of FF27. The input to the one-shot 278 is the signal designated GOTCHA. The Q output of the one-shot is connected to the C inputs of FF26 and FF27 and to one input each of G106 and G107. CLEAR is applied to the S inputs of FF26 and FF27 and through I29 to create the CLEAR signal applied to the up-down counter 274. The Q output of FF26 is connected through I27 to create $\overline{UP}$. The output of I27 is also connected to the second input of FF26. The Q output of FF27 is connected through I28 to create $\overline{DN}$. The output of I28 is also connected to the second input of G107. The output of G106 is applied to the UP input of the up-down counter 274, and the output of G107 is applied to the DN input of the up-down counter 274.

Turning now to a description of the operation of the temperature sensor; initially, a one to zero transition of CLEAR sets FF26 and FF27 and clears the up-down counter 274. At this point, the output from the digital-to-analog converter is also zero because the up-down counter is cleared to zero by CLEAR. The reference voltage applied to the temperature probe 268, however, creates a certain analog voltage. Because of this difference, assuming it is positive, the UP output of the comparator 270 is in a one state. This one is clocked through FF26 by the output from the one-shot 278 which shifts states for a period of time each time GOTCHA goes from zero to one, as hereinafter described. Since DN is zero at this point in time, the one on the Q output of FF26 is applied to the UP input of the up-down counter 274, which starts to count up. After several such cycles, the up-down counter reaches a level such that both comparator outputs are at zero states. The number of such cycles is related to the specific temperature sensed by the probe. Thereafter, each time the clock and thermometer interface is interrogated by the computer, in the manner hereinafter described, the one-shot is operated to clock FF26 and FF27. If the comparator output indicates that no temperature change has occurred, the previous count is neither increased nor decreased. On the other hand, if the temperature has changed, either up or down, the comparator up or down output, as the case may be, is clocked through FF26 or FF27 to vary the count re-

corded by the computer. In this manner, the temperature information to the comparator is continuously updated. It should be noted that the comparator is formed such that there is a "window" between the UP and DN outputs of the comparator so as to prevent any oscillation of the system.

CLOCK AND THERMOMETER INTERFACE

FIG. 36 illustrates the clock portion of a clock and thermometer interface suitable for use by the invention and comprises four D flip-flops designated FF28, FF29, FF30 and FF31; one inverter designated I30 one two-input AND gate designated G108; and, seven two-input NAND gates designated G109-G115. DATA4 is applied to the D input of FF28 and MSKO is applied to the C input of FF29. The 1Hz output from the frequency synthesizer is applied to the C input of FF29. STRT is applied to one input of G109. CLR is applied to one input of G110. SEL5 is applied to the second input of G109, the second input of G110, one input of G114 and one input of G115. IORST is applied to one input of G111. The output of G110 is connected to the second input of G111. The outputs of G109 and G111 are connected, respectively, to the two inputs of G108. The output of G108 is connected to the R input of FF29 and the S input of FF31. The output of G109 is also connected to the S input of FF30. The output G111 is also connected to the R input of FF30. The D input of FF30 is connected to ground. The $\bar{Q}$ output of FF28 and the Q output of FF29, respectively, are connected to the two inputs of G112.

The output of G112 is connected to the D input of FF31. RQENB is applied to the C input of FF31. The $\bar{Q}$ outputs of FF29 and FF30 are connected, respectively, to the two inputs of G113. The output of G113 is connected to the D input of FF29. The Q output of FF29 is connected to the second input of G114, and the Q output of FF30 is connected to the second input of G115. The Q output of FF31 is $\overline{IRQ5}$. This signal, in addition to containing interrupt information, also contains clock information. That is, the computer is adapted to generate an alphanumeric character signal on one channel designating the time of day. The 1Hz signal generated by the frequency synthesizer is utilized to create the updating of this display, as hereinafter described. The $\bar{Q}$ output of FF31 is connected through I30 to create an $\overline{INTR}$ signal.

The output from G114 is designated SELD. This signal indicates the done condition of the clock and thermometer interface. The output of G115 is a signal designated SELB, which designates the busy condition of the clock and thermometer interface.

It will be appreciated from viewing FIG. 36 and the foregoing description that the clock illustrated in FIG. 6 basically comprises busy/done logic. The clock, in addition to providing time of day information also creates an interrupt that causes the computer to interrogate the temperature sensor via the hereinafter described temperature interface.

IORST initially resets FF29 and FF30, and sets FF31. Thereafter simultaneous STRT and SEL5 ones set FF30. This action causes the output of G115 to achieve a zero state each time it is interrogated by a SEL5 one pulse. The next 1Hz pulse resets FF30 and sets FF29 by clocking the one on the output of G113 into FF29. The following RQENB pulse causes $\overline{IRQ5}$ and $\overline{INTR}$ to drop to zero states whereby an interrupt is requested and the

computer is instructed to update its time of day display by one second. DATA4 and MSKO provide for the use of the mask out technique used by the NOVA computer to interrogate its input subsystems. CLR and SEL5 when in simultaneous one states reset FF29 and FF30 and set FF31.

FIG. 37 is a block diagram illustrating a thermometer interface and comprises two inverters designated I31 and I32, a two-input AND gate designated G120 and four two-input NAND gates designated G116-G119. The UP output of the temperature sensor is applied through I31 to one input of G118. The DN output of the temperature sensor is applied through I32 to one input of G119. IORST is applied to one input of G120. 10 PULSE is applied to one input of G116. DIB is applied to one input of G117. SEL5 is applied to the second inputs of G116 and G117, respectively. The output of G116 is connected to the second input of G120. The output of G117 is connected to the second inputs of G118 and G119. The output of G117 is the signal designated GOTCHA.

In general, the thermometer interface is merely a gating circuit which gates the output of the temperature sensor to the computer. The output of G118 is DATA14, and the output of G119 is designated DATA15. The output of G120 is the CLEAR signal. When the clock illustrated in FIG. 36 causes an interrupt request, the select logic, in accordance with its computer instructions, generates an SEL5 signal. This signal in conjunction with DIB interrogates UP and DN via G118 and G119. Thus, the computer is informed as to whether or not it should increase or decrease its temperature related pulse count. In addition, this same signal causes the output of G17 to pulse the one-shot 278 of the counter control logic illustrated in FIG. 35 so that the outputs of the comparator can be interrogated by FF26 and FF27. IO PULSE in conjunction with SEL5 and IORST creates the CLEAR zero pulse which clears the up-down flip-flops, FF26 and FF27, of the counter control logic, as well as the up-down counter 274, causing the temperature sensor to recycle from a zero state. Recycling occurs when it appears as though the output from the comparator is in error. This "apparent" error occurs when a rapid change in temperature is sensed, and the computer desires to find out whether or not such a change in temperature actually happened.

CHARACTER ADDRESS SELECTOR

FIG. 38 illustrated a character address selector suitable for use by the preferred embodiment of the invention illustrated in FIG. 1. The character address selector illustrated in FIG. 38 comprises: character generator group select logic 280; a character generator selector 282; a ready-in selector 284; and, ready enable logic 286.

The A1-A4 conductors from the display selector register of the output display logic are connected to the four inputs of the character generator group select logic 280. In accordance with the binary code on these parallel input conductors, the character generator group select logic selects one of a plurality of character generator selectors 282 for receipt of the signals on the conductors A5-A7. The selector character generator selector, in accordance with the binary code on conductors A5-A7, generates a load signal which is applied to one of a plurality of input data registers, form-

ing a part of the hereinafter described character generator. This selection is made when LOAD from the output display logic, also applied to the selected character generator selector, is in a zero state.

The ready-in selector 284 receives a READY IN signal from the selected register and informs the ready enable logic of this condition. The ready enable logic then generates a READY signal (zero state) to cycle the display load generator of the output display logic in the manner heretofore described.

FIG. 39 is a block diagram illustrating character generated group select logic suitable for use in the character address selector illustrated in FIG. 38 and comprises a decoder 288 and a group selector socket 290. The decoder is enabled by a zero on conductor A4. When this zero occurs, the decoder 288 decodes the signals on conductors A1-A3 and, in accordance therewith, chooses one of eight outputs 292; that is, one of the eight outputs drops to zero. The group selector socket connects the outputs to a plurality of character generator selectors 282. Thus, one of these selectors is enabled by the chosen output of the decoder, identified by the conductor 301 in FIG. 93 for illustration purposes. The selected character generator selector decodes the signals on conductors A5-A7 if its LOAD input is in a zero state (or when its LOAD input achieves a zero state, as the case may be).

FIG. 40 is a block diagram illustrating a character generator selector suitable for use by the character address selector illustrated in FIG. 38 and comprises a decoder 294; a two-input NAND gate designated G122; and, ten inverters designated I33-I42. Conductor 301 is connected through I33 to one input of G122. The output of I33 is also connected to a conductor designated 303, which is connected to the ready enable logic 286 of the character address selector hereinafter described. LOAD is applied through I34 to the second input of G122. The output of G122 is connected to the enable input of the decoder 294.

When the signals on lines 301 and the load input achieve simultaneous zero states, the inputs of G122 both achieve one states, causing a zero to be applied to the enable input of the decoder 294. The information on conductors A5-A7 is then decoded by the decoder 294. In accordance with the binary code conductors A5-A7, one of the eight outputs of the decoder drops from its normal one state to a zero state. The eight outputs are connected through the eight inverters designated I35-I42. And the outputs of the decoders are connected to eight conductors designated A20-A27, which are connected to the character generator in the manner hereinafter described. Thus, normally the signals on conductors A20-A27 are zeros. When a selection occurs one conductor signal shifts to a one state.

FIG. 41 is a block diagram illustrating a ready-in selector suitable for use in the character address selector illustrated in FIG. 38. The ready-in selector illustrated in FIG. 41 comprises a decoder 296. Conductor 301 is connected to the enable input of the decoder 296. In addition, the decoder receives eight inputs on conductors designated B20-B27. These conductors sense signals generated by the character generators in the manner hereinafter described. Specifically, the conductors carry signals from the character generators which indicate their ready or busy states. In this regard B20 relates to A20, B21 relates to A21, etc. In addition, conductors A5-A7 are applied to the decoder. The signals

on conductors A5-A7 cause the decoder 296 to "look" at the signal on one of conductors B20-B27 when the decoder is enabled. The B conductor "looked" at corresponds to the A conductor selected by the character generator selector illustrated in FIG. 40. The "looked" at B conductor signal is applied to an output conductor designated 305.

FIG. 42 is a block diagram illustrating ready enable logic suitable for use by the character address selector illustrated in FIG. 38 and comprises an inverter designated I43 and a twoinput NAND gate designated G123. Conductor 303, from the character generator selector, is connected to one input of G123. Conductor 305, from the ready-in selector, is connected to the second input of G123 through I43. The output of G123 is the signal READY. Essentially, the ready enable logic is merely a gate which gates the output from the decoder of the ready-in selector back to the output display logic to inform it of the ready or busy state of the chosen character generator.

SYNC GENERATOR

In general, the syn generator is adapted to generate synchronizing signals for use by the character generator and the chroma generator, so that the character displays on the various channels are readable. In addition, the sync generator generates some signals that are utilized by the scrolling and paging logic hereinafter described, if these subsystems are included in an actual embodiment of the invention.

FIG. 43 is a block diagram illustrating a sync generator suitable for use by the preferred embodiment of the invention illustrated in FIG. 1 and comprises a frequency generator 300; a timing chain 302; a TV sync generator 304; and a clock for character generator 306.

The frequency generator is powered from a suitable source and generates a 3.5MHz subcarrier signal designated F which is applied to the chroma generator. In addition, the frequency generator generates an (8/5) F (5.8MHz) signal which is applied to the character generator and to the timing chain 302 of the sync generator. The frequency generator may be a phase locked loop or any other suitable type of frequency source adapted to generate the desired signals.

The timing chain generates a plurality of signals which are applied, as necessary, to other subsystems of the invention, and in particular to the character generator and the chroma generator, and the scrolling logic and the paging logic, if either of the latter two logic systems are included in an actual embodiment of the invention. In addition, the timing chain applies timing signals to the TV sync generator 304 and to the clock for character generator 306. The TV sync generator generates chroma control signals (CSY, CBL and SCG) which are applied to the chroma generator and an ECP enabling signal which is applied to the character generator. The clock for character generator generates clock pulses which are applied to the character generator. Further, the clock for character generator generates clock signals for use by the paging or scrolling logic, if either of the latter two logic systems are included.

In accordance with the preferred embodiment of the invention, the maximum possible number of rows of characters that can be displayed on a TV screen are sixteen. Each of the sixteen possible rows includes twelve TV lines. Of the twelve lines, seven are utilized for

character display and the remaining five are utilized to provide space between the rows of characters. In each row, there is a potential 52 character positions from one side of the screen to the other side. However, in accordance with the preferred embodiment of the invention only 32 of the 52 possible positions are used in an actual display. In each character position, there are seven horizontal dot positions in each of the 12 lines (seven being used for character display). Of these seven positions, only five are used to provide a character display. The other two dot positions provide spaces between characters. In addition, the invention utilizes a single 263-line TV raster, rather than two interlaced fields of 262½ lines each, as is common in standard commercial television broadcast systems. However, this scanning technique will operate a conventional TV receiver without modification because suitable synchronizing information is included with the display information ultimately transmitted on the various channels of an overall multiple channel television display system formed in accordance with the invention.

A timing chain suitable for use in the sync generator illustrated in FIG. 43 is illustrated in FIG. 44. The timing chain illustrated in FIG. 44 comprises a dot code generator 308; a character position code generator 310; a line position code generator 312; a row position code generator 314; an end flip-flop 316; a vertical dead time flip-flop 318.

Basically, the dot code generator, the character position code generator, the line position code generator and the row position code generator form a dividing chain adapted to divide the (8/5) F signal generated by the frequency generator into timing signals suitable for creating the display previously described. The dot code generator 308 is a divide-by-seven counter adapted to generate signals designated D0, D1 and D2. The coding of these signals designates each position of the seven positions of a particular dot portion of a line of a row of characters. That is, as previously described, each character position along a TV line is defined by seven dot positions. The D0, D1 and D2 outputs in a binary manner define each of the seven positions.

Each time the dot code generator cycles it sends a pulse to the character position code generator 310. The character position code generator is a divide-by-fifty-two counter which divides each TV (including retrace) into 52 character positions. As previously indicated, only 32 of these positions are actually used for a character display, the other positions being located on either side of the actual characters being displayed or in retrace. The outputs of the character position code generator are designated C0-C5. The binary code on these outputs uniquely identifies each of the 52 character positions.

The character position code generator generates a pulse once each TV line and applies the pulse to the line position code generator 312. The line position code generator is a divide-by-twelve counter whose outputs define in a binary manner the twelve lines making up each row of characters. The outputs from the line position code generator are designated L0, L1, L2 and L3.

Once each cycle the line position code generator applies a pulse to the row position code generator 314. The row position code generator is a divide-by-sixteen counter whose binary outputs define the 16 lines of the character display. These outputs are designated V4,

V5, V6 and V7. The output of the last stage of the row position code generator is connected to the D input of the end flip-flop 316 and to the D input of the vertical dead time flip-flop 318. C5 is applied to the C inputs of both of these flip-flops. Thus, once each "frame" the end and vertical dead time flip-flops are triggered with a one on their inputs. The output from the end flip-flop 316 is designated V8 and the output from the vertical dead time flip-flop 318 is designated VDT. V8 lasts from the first TV line of row 17 to the eleventh line of the twenty-second row (line 263 of the scan) and is used to reset the timing chain for the next frame which is the same as the first frame (i.e., no "interlacing" occurs). V8 is also used to perform other functions as hereinafter described.

FIG. 45 is a block diagram of a TV sync generator suitable for use by the sync generator illustrated in FIG. 43. The TV sync generator illustrated in FIG. 45 comprises: a decoder 320; three RS latches 322, 324 and 326; five two-input NOR gates designated G124 - G128; six two-input NAND gates designated G129 - G134; two three-input NAND gates designated G135 and G136; and, two inverters designated I44 and I45.

C4 is applied to one input of G129. C1, C2 and C3 are applied to the signal inputs A, B and C of the decoder 320. C5 is applied to the second input of G129 and to one input of G130. The output of G129 is connected to the R input of the first RS latch 322. The output of G129 is also connected to the second input of G130. The output of G130 is connected to the enable input of the decoder 320. Thus, when C4 and C5 are in appropriate states (C4-zero, C5-one or vice versa) the decoder 320 is enabled to "read" the C1, C2 and C3 signals. These signals are decoded and create binary signals on four outputs (1, 2, 3 and 4). The first output (1) of the decoder is connected to the S input of the first RS latch 322. The second output (2) of the decoder 320 is connected to one input of G127. The other two outputs (3 and 4) of the decoder are connected to the two inputs of G134, respectively. The output of G134 is connected to one input of G128. The Q output of the first RS latch 322 is connected to one input of G126.

L0 and L1 are applied to the two inputs of G124 and two of the inputs of G136. L2 is applied to one input of G135. The output of G124 is connected to a second input of G135. V4 is applied to one input of G125. V5 is applied to one input of G131, and through I45 to one input of G133. V6 is applied to one input of G132. V8 is applied to one input of G131, the second input of G132 and through I44 to the second input of G133.

The output of G131 is connected to the second input of G125. The output of G125 is connected to the third inputs of G135 and G136, respectively. The output of G135 is connected to the S input of the second RS latch 324 and to the S input of the third RS latch 326. The output of G136 is connected to the R input of the second RS latch 324. The output of G132 is connected to the R input of the third RS latch 326. The Q output of the second RS latch is connected to the second inputs of G127 and G128, respectively. The Q output of the third RS latch 326 is connected to the second input of G126.

The output of G126 is a signal designated CBL which stands for composite blanking. The signal occurs at predetermined intervals, determined by the nature of its input signals, to cause blanking of the screen of the

TV display. Without going into the matter in detail, because the logic is apparent from the FIG. 45, CBL achieves a one state when characters are not to be displayed, i.e., around the edges of the 16 line display, between the characters, and between the rows.

The output from G127 is a signal designated SCG and is utilized by the character generator hereinafter described. This signal is a subcarrier burst gate signal. The output of G128 is a signal designated CSY and provides composite sync. CSY is inserted into the resultant video signal in the manner hereinafter described. The output of G133 is a signal designated ECP. ECP is applied to the character generator to enable a comparator in the manner hereinafter described.

FIG. 46 is a block diagram of a clock for character generator suitable for use in a sync generator illustrated in FIG. 43. In essence, the clock for character generator in reality is a decoder which decodes the pulses generated by the timing chain in a manner such that clock and other instruction pulses are generated for use by the character generator at appropriate times and in appropriate sequences.

The clock for character generator illustrated in FIG. 46 comprises: a D flip-flop designated FF32; four three-input NOR gates designated G137 - G140; two two-input NOR gates designated G141 and G142; four two-input NAND gates designated G143 - G146; and, three inverters designated I46, I47 and I48. C5, L3 and V8 are applied to the three inputs of G137. The output of G137 is connected to the D input of FF32. D2 is applied to the C input of FF32. The Q output of FF32 is designated STS and is connected to the hereinafter described character generator. The $\bar{Q}$ output of FF32 is connected to the reset input of FF32, but is delayed from applying a reset pulse to FF32 by virtue of a capacitor C6 connected between $\bar{Q}$ and ground.

D1 is applied to one input of G138 and through I46 to one input of G139. D0 is applied to the second input of G139 and through I47 to the second input of G138. C5, D2 and VDT are applied to the three inputs of G140. The output of G140 is connected to one input of G143 and to one input of G144. D1 is applied to the second input of G144. L0 and L1 are applied to the two inputs of G141. The output of G141 is connected to the second input of G143 and to one input of G145. The output of G141 is designated ECK and is herein used to identify a point wherein a substitute signal may be applied by the scrolling logic.

L2 and L3 are applied to the two inputs of G142. The output of G142 is connected to the second input of G145. The output of G145 is designated CHL0 (Character line zero) and is connected to one input of G145. C5 is applied to the second input of G146, through I48. The output of G146 is designated LSW. The output of G138 is designated $\bar{CP1}$, the output of G139 is designated $\bar{CP2}$ and the output of G144 is designated $\bar{CP3}$.

As previously indicated, all of the outputs of the clock for the character generator illustrated in FIG. 46 are applied to character generators of the type hereinafter described. In general, these signals provide timing for the character generators so that they will operate in the hereinafter described manner.

CHARACTER GENERATOR

FIG. 47 is a block diagram of a character generator suitable for use in the preferred embodiment of the invention illustrated in FIG. 1. It should be noted that a

plurality of character generators, one for each channel, are used in an actual embodiment of the invention. In general, the character generators receive timing and display instruction from the indicated sources and, in accordance with those instructions, control the generation of characters to be displayed by the TV receivers "tuned" to the channel associated with a particular character generator. In other words, the character generators, in essence, generate signals which, when received by a standard TV receiver, create a character display. These signals, like any other standard TV signal include information regarding the positioning of characters and the color of the characters (and background) as the TV screen is scanned in a standard manner. That is, as scanning occurs, the guns of the picture tube emit electron beams whose intensity is controlled so that the end result is that a colored character display is provided.

The character generator illustrated in FIG. 47 comprises: an input data register 330; character generator circuitry 332; a function decoder 334; a comparator 336; a write address register control 338; a write address register 340; a write timing circuit 342; and a cursor video generator 344. The input data register 330 receives instructions, A8 - A14 and LOAD from the output display logic which identify the particular characters to be displayed. This character identification information is sequentially applied to the character generator circuitry 332 wherein it is stored and utilized to create television signals designated CHV (character video) which control the intensity of the electron beam(s) at each point on the face of the TV picture. The beam(s) scan the picture tube face.

In addition, the instructions related to the nature of the characters to be displayed are decoded by a function decoder whose output is utilized to control the write address register control 338. In addition, the function decoder generates two signals, $\bar{O}$ and $\bar{P}$, to indicate whether or not the input data register is receiving new instructions. These signals are used by the hereinafter described paging and scrolling logic. $\bar{O}$ denotes that character instructions are not being received. $\bar{P}$ denotes that character instructions are being received.

The write address register control controls the write address register whose output is compared in the comparator with certain outputs from the sync generator related to the "position" of the electron beam. Assuming suitable comparisons are found, the output from the comparator controls the write timing circuit 342 which generates a WRT signal used by the paging and scrolling logic to enable "writing" into the character generator circuitry.

In this manner synchronization between beam position and character position is achieved. The cursor video generator, in accordance with the output from the comparator, provides a cursor to indicate character position.

FIG. 48 is a block diagram illustrating an input data register suitable for use in the character generator illustrated in FIG. 47. The input data register illustrated in FIG. 48 comprises a storage register 346; and a D flip-flop designated FF32. Conductors A8 - A14 from the output display logic heretofore described are connected to the seven inputs of the storage register 346. A15 is not connected and, thus, not utilized because the signals on A15 are parity error information signals

and are ignored by this invention. A conductor designated 399 from the write timing circuit 342 is connected to the enable input of the storage register. LOAD (one of conductors A20 - A27, previously described) is connected to the C input of FF32. That is, as previously described, a plurality of character generators are used in an actual embodiment of the invention. One of them is chosen by the character address selector to receive the character instructions in accordance with computer instructions. The chosen one is determined by which A20 - A27 conductor carries the LOAD signal. The D input of FF32 is unconnected. Thus, when FF32 is clocked by a LOAD one pulse, it is set. FF32 is reset by $\overline{\text{CL1}}$. The Q output of FF32 is designated STB and is connected to the clock (C) input of the storage register 346. The $\overline{\text{Q}}$ output of FF32 generates the READY signal which flows on one of conductors B20 - B27 and is applied to the character address selector, as previously described. This signal, thus, indicates the ready or not ready status of a particular character generator. When it is being loaded it is not ready and after its load is "read out" it is ready to receive additional signals on conductors A8 - A14.

The seven outputs of the storage register are designated DR0 - DR6. DR0 - DR5 are applied to the character generator circuitry 332. DR0 - DR4 are applied to the function code generator 334 and DR6 and DR5 are applied to the write timing circuit 342. In operation, the storage register 346 merely stores the character information on conductors A8 - A14 which information, in addition to character information per se also includes control functions informations such as spacing (forward and back), line spacing (up and down), etc., in a form suitable for decoding by the function code generator. In addition, DR5 and DR6 include timing information suitable for use by the write timing circuit to control the writing of the associated display.

Character generator circuitry suitable for use by the character generator illustrated in FIG. 47 is illustrated in FIG. 49 and comprises page storage registers 348; row storage registers 350; a read-only memory 352; and a parallel-to-serial converted 354. In addition, an inverter designated 149 is included in the character generator circuitry.

The page storage register is, preferably, made up of eight sets of six, 512 bit recirculating shift registers. These registers, each of which represent a page, i.e., a complete display of information, are under the control of W0 - W7 and R0 - R7 instructions generated by the hereinafter described page or scrolling logic, if these logic circuits are included. If these logic circuits are not included and only a single page of information is to be illustrated then only one set of six, 512 bit recirculating shift registers is included in the character generator circuitry. In other situations more or less than eight sets of six, 512 bit recirculating shift registers may be included, as desired. In any event, the capacity of one set of registers is adequate to store all the information necessary to display a complete page of information. The six outputs of each of the six, 512 bit recirculating shift registers are connected to the inputs of the row storage registers 350 on a one-by-one basis. That is, one output of each of the 512 bit storage registers is connected to one input of the row storage registers. The R0 - R7 signals determine at any particular period of time which of the sets of six, 512 bit recirculating shift registers is applying signals to the row storage registers.

The row storage registers is made up of six, 32 bit shift registers. Thus, the row storage registers have the capacity to store instructions adequate to define a row of characters.

The six outputs of the row storage registers 350 are connected to the six inputs of the read-only memory 352. In accordance with the binary code on the outputs of the row storage registers at any particular period of time, the read-only memory generates five binary output signals which are applied to the parallel-to-series converter 354. These signals define, in parallel form, the nature of the characters. That is, these signals control the emissions from the electron guns of the receiving television sets, as their screens are swept. Thus, these signals control the nature of the display.

The parallel-to-series converter converts its input signals into serial pulse signals to form a signal designated CHV. Thus, CHV signal contains all of the intensity information necessary to create a character display on the TV receivers.

The page storage registers 348 are clocked by the CP1 and CP2 pulses generated by the clock for character generator forming part of the sync generator illustrated in FIG. 43. The CP3 signal through 149 clocks the row storage registers 350. LSW controls loading of the row storage registers 350. The L0, L1 and L2 signals are applied to the read-only memory 352 to define each TV line so that the ROM generates signals related to the character for the particular line that will be swept by the TV scan. The parallel-to-serial converter is enabled by the STS signal generated by the clock for character generator forming a portion of the sync generator. And, the parallel-to-serial converter is clocked by the (8/5) F signal output from the frequency generator portion of the sync generator. (8/5) F is, of course, the dot frequency rate.

As previously indicated, the function decoder decodes the DR0-DR4 outputs from the input data register as they occur to determine certain information. More specifically, the function decoder decodes these outputs into seven signals designated $\overline{\text{FS}}$ (forward space), $\overline{\text{BS}}$ (back space), BLF (back line feed), $\overline{\text{CR}}$ (carriage return), CLS (clear screen), HME (home), and $\overline{\text{FLF}}$ (forward line feed). These signals, obviously, relate to certain functions generated by a keyboard or by a newswire teletype or the like. Thus, these signals in essence contain information about the nature of the character display. These signals are applied to the write address register control which, in accordance therewith, controls the write address register.

A write address register control suitable for use in the character generator illustrated in FIG. 47 is illustrated in FIG. 50 and comprises: two two-input AND gates designated G147 and G148; one three-input NAND gate designated G150; one two-input NAND gate designated G149; three inverters designated I50, I51 and I52; and, a JK flip-flop designated FF33. A conductor designated 407, from the write timing circuit hereinafter described, is connected to one input of G148 and one input of G150. $\overline{\text{FS}}$ is applied to the second input of G148 and the second input of G150. The output of G148 is applied to a conductor designated 409. $\overline{\text{BS}}$ is applied to the third input of G150 and to a conductor designated 413. The output of G150 is applied to a conductor designated 411. BLF is applied through I50 to a conductor designated 415. CR is applied to one input of G149.

CLS is applied to one input of G147 and to the S terminal of FF33. HME is applied to the second input of G147. The output of G147 is connected to a conductor designated 417 and to the second input of G149. The output of G149 is connected through I51 to a conductor designated 403. FLF is applied through I52 to a conductor designated 405. The J input of FF33 is connected to ground. STB, which is the inverted output of FF32 of the input data register, is applied to the C input of FF33. The Q output of FF33 is a signal designated WBL (write blank page). When this signal occurs, a blanking of the screen of the TV receiver occurs.

In general, the write address register control decodes the various outputs from the function decoder so that these outputs can be used to control counters making up the write address register hereinafter described. That is, the write address register is formed of two up/down counters and associated logic, as will be better understood from the following description. These counters and the logic are preset, and pulsed up and down by the signals on the conductors 403, 405, 409, 411, 413, 415 and 417 to create character position signals that correspond to C0-C4 and V4-V7 for comparison purposes.

FIG. 51 illustrates a preferred embodiment of a write address register suitable for use by the character generator. The write address register illustrated in FIG. 51 comprises: two up/down counters 360 and 362; a two-input NAND gate designated G151; four two-input NOR gates designated G152-G155; and, a JK flip-flop designated FF34. Conductor 409 is connected to the up input of the first up/down counter 360 and conductor 413 is connected to the down input of the first up/down counter 360. Conductor 403 is connected to the load input of the first up/down counter 360 and to the R input of FF34.

The first up/down counter 360 is four outputs designated C0', C1', C2' and C3' which, as will be better understood from the following description are used for comparison with C0, C1, C2 and C3 signals generated by the sync generator.

The up overflow output (C0) and the down overflow output (B0) of the first up/down counter are, respectively, connected to the two inputs of G151. The output of G151 is connected to both the J and the K inputs of FF34. C0 is also connected to one input of G152 and B0 is also connected to one input of G154. Conductor 411 is connected to the C input of FF34. The Q output of FF34 is designated C4' and is applied to the second input of G154. C4', as with C0'-C3', is utilized for comparison with the C4 signal generated by the sync generator. The $\bar{Q}$ output of FF34 is connected to the second input of G152. The output of G152 is connected to one input of G153 and the output of G154 is connected to one input of G155. Conductor 405 is connected to the second input of G153 and conductor 415 is connected to the second input of G155.

The output of G153 is connected to the up input of the second up/down counter 362 and the output of G155 is connected to the down input of the second up/down counter 362. Conductor 417 is connected to the load input of the second up/down counter 362. Four outputs of the second up/down counter are designated V4', V5', V6' and V7'. These signals are utilized for comparison with the V4-V7 signals, respectively, generated by the sync generator.

In general, the write address register is controlled such that its outputs vary in accordance with the various space, line, etc., outputs of the function decoder 334. For example, when a forward space ($\bar{FS}$) zero pulse is generated by the function decoder, the zero on conductor 409 causes the first up/down counter to count up by one clock pulse. When a back space ($\bar{BS}$) occurs, a zero on conductor 413 causes the first up/down counter to count down by one clock pulse. Thus, the binary C0'-C4' outputs which relate to character position move up or down by one count. When a carriage return signal occurs, a zero on conductor 403 resets both the up/down counter 360 and FF34. The up/down counter 360 is reset by loading it with a preset number. Thus, the entire line of characters as defined by C0'-C4' is reset to zero. When forward line feed (FLF) occurs, a zero on conductor 405 causes the second up/down counter to count up by an entire row of characters. Similarly, when back line feed (BLF) occurs, a zero on conductor 415 causes the second up/down counter to count down by one row of characters. The other outputs of the function decoder cause their related actions in a similar manner.

Thus, in conclusion, the decoded outputs from the input register cause the generation of C0'-C4' and V4'-V7' signals, should correspond to the timing signals from the sync generator at some particular time.

The signals C0'-C4' and V4'-V7' are then compared in the comparator 336 with the C0-C4 signals and the V4-V7 signals from the sync generator. If a comparison occurs, CMP is applied to the write timing circuit 342 and the cursor video generator 344.

The comparison is enabled when ECP drops to a zero state.

FIG. 52 is a block diagram of a write timing circuit suitable for use in the character generator illustrated in FIG. 47. The write timing circuit illustrated in FIG. 52 comprises: two JK flip-flops designated FF35 and FF36; a two-input NOR gate designated G156; three three-input NAND gates designated G157, G158 and G159; three two-input NAND gates designated G160, G161 and G162; and, three inverters designated I53, I54 and I55.

DR5 and DR6 are applied to the two inputs of G156 and detect the status of the outputs of the input data register. C5 is applied through I53 to one input of G157 and to one input of G161. WBL, from the write address register control, is applied to the second input of G161. CMP, from the comparator; CHL0, from the sync generator; and, STB, from the input data register are applied to the three inputs of G158. D2 is applied to the C inputs of FF35 and FF36 and to one input of G159.

The output of G156 is connected to one input of G160 and through I54 to the second input G157 and to the second input of G159. The output of G158 is connected through I55 to the J input of FF35, the second input of G160 and the third input of G157. The outputs of G157 and G161 are connected to the two inputs of G162. The Q output of FF35 is connected to the J input of FF36 and to the third input of G159.

The output of G160 is connected to a conductor designated 401 which is connected to the function decoder for enable timing purposes. The output of G162 is designated WRT and is also applied to the hereinafter described paging and scrolling logic to control writing by the character generator. The $\bar{Q}$ output of FF36 is connected to the conductor designated 399 and is applied

to the input data register for clearing the storage register as heretofore described. The Q output of FF35 (CL1) is also applied to the input data register to reset FF32. Thus, FF32 is reset before the storage register is enabled. The output of G159 is applied to the conductor designated 407 and is, thus, applied to the write address register control for enabling purposes, i.e., it enables the application $\overline{FS}$ and $\overline{BS}$ to the up or down inputs of the first up/down counter of the write address register.

Turning now to a description of the operation of the write timing circuit illustrated in FIG. 52 assuming that a comparison exists between the outputs of the write address register (C'-C4', V4'-V7') and the other inputs to the comparator (C0-C4, V4-V7), CMP is in a one state. When a chosen character generator receives a load signal, STB achieves a one state. Thereafter, CHLO from the clock for the character generator illustrated in FIG. 43 reaches a one state when the first row of characters of the display is to occur. When all of these ones are applied to the input of G158, its output goes to a zero. Thus, the output of I55 places a one on the J input of FF35. Thereafter, the next D2 one pulse causes FF35 to be set. A subsequent D2 one pulse sets FF36. The first D2 pulse reset FF32 of the input data register, and the second D2 pulse clears the storage register of the input data register.

Assuming the signals on lines DR5 and DR6 are in appropriate one states, the output of G160 gates the output of I55 to the function decoder on conductor 401. This signal enables the function decoder. Assuming that WBL is in a zero state, the inverted C5 pulse causes the generation of a WRT instruction. WRT is generated by C5.WBL or CMP.CHLO.STB.DATA CHARACTER (output of I54).

FIG. 53 is a block diagram of a cursor video generator suitable for use by the character generator and comprises: a D flip-flop designated FF36A; and, two two-input NAND gates designated G163 and G164. CMP is applied to one input of G164. L2 and C3, from the sync generator, are applied, respectively, to the two inputs of G163. The output of G163 is connected to the second input of G164. The output of G164 is connected to the D output of FF36A. D2, from the sync generator, is applied to the C input of the FF36A. The Q output of FF36A is a signal designated CVD to represent cursor video. Thus, the cursor video signal needed for a TV display is generated.

CHROMA GENERATOR

FIG. 54 is a block diagram illustrating a chroma generator suitable for use by the preferred embodiment of the invention illustrated in FIG. 1. The chroma generator illustrated in FIG. 54 comprises: a phase-locked loop 366; a divide-by-six counter 368; a decoder 370; a chroma phase/color decoder 372; a bandpass filter 373; a color code selection network 374; controllable switches 376; a character/chroma gate generator 378; and a summation circuit 380. In addition, the chroma generator illustrated in FIG. 54 includes three inverters designated I56, I57 and I58.

In operation, the phase-locked loop 366 receives the F signal generated by the sync generator and is designed such that it generates a signal at three times the frequency of F, i.e., 3F. 3F is applied to the divide-by-six counter 368, which generates three output signals related to the frequency of the input signal (3F). In this

manner, the decoder receives a plurality of digital input signals. It decodes these signals into three signals having different phases but all being at the input frequency (F). In other words, the outputs from the decoder are three digital signals at the frequency F having 0°, 60° and 120° phase relationships. These signals are applied to the chroma phase/color decoder 372. In addition, one of these signals (0° phase) is used as a feedback signal to the phase-locked loop 366. Further, the three outputs from the decoder are inverted and the inverted outputs are also applied to the chroma phase/color decoder. Thus, the decoder receives six input signals, each of which is related by phase to a particular display color. The chroma phase/color decoder, under the control of the color code selection network 374, selects one of these signals for application to its output conductor, thus, to the summation circuit 380 via the bandpass filter which eliminates unwanted frequency components from the essentially digital output of the chroma phase/color decoder.

The color code selection network 374 is a presettable and controllable device which creates a binary code on conductors X, Y, and Z. This binary code controls color selection by means of the chroma phase/color decoder. The controllable switches 376 control a portion of the color code selection network via two conductors designated A and B. In addition, the character/chroma gate generator 378 also provides a control signal to the color code selection network via a conductor designated C. CBL (composite blanking), controls the gating of the output of the color code selection network, so that during the vertical blanking interval, the chroma phase/color decoder does not generate a color signal.

The input to the character/chroma gate generator is CHV (character video), and the output is essentially the same, i.e. also character video modified by a delay. This signal is also applied to the summation circuit 380. In addition, the summation circuit receives the composite sync signal (CSY) from the sync generator. Thus, the summation circuit receives all the information necessary to create a video signal. Hence, the output from the summation circuit is designated composite video. This signal is subsequently applied to a modulator which modulates the signal at the appropriate channel frequency. Thereafter, when the signal is received by the television viewer, his television set, which incorporates an appropriate demodulator, demodulates the signal to obtain the resultant video signal. The resultant video signal causes the appropriate alphanumeric character display to be created on the TV set tuned to the associated channel.

FIG. 55 is a block diagram of a color code selection network suitable for use by the chroma generator illustrated in FIG. 54 and comprises a programmable read-only memory 382; and, four two-input NAND gates designated G165, G166, G167 and G168. Conductors A and B are connected to two of the program inputs of the programmable read-only memory 382. C is connected to the third input of the programmable read-only memory 382. In accordance with the signals (zero or one) on conductors A, B and C, the programmable read-only memory generates three digital output signals. These signals are applied to one input of each of the three gates G166, G167 and G168. The other input of each of the three gates is CBL. Thus, the blanking pulse controls whether or not the output from the three

gates is a fixed one or is a controlled signal. The output from G166 is connected to one input of G165. SCG is applied to the second input of G165. The output of G165 is applied to a conductor designated X; the output of G167 is applied to a conductor designated Y; and the output of G168 is applied to a conductor designated Z. X, Y and Z are connected to the chroma phase/color decoder 372. The binary code on these conductors controls decoding by the chroma phase/color decoder, causing it to apply the signal on one of its six input conductors to its output conductor.

FIG. 56 is a block diagram illustrating a character/chroma gate generator suitable for use in the chroma generator illustrated in FIG. 54 and comprises a five-stage shift register 384; a four-input NAND gate designated G169; and, an inverter designated I56. CHV, from the character generator, is applied to the serial input (SI) of the shift register 384. The 8/5F signal from the sync generator is applied to the C input of the shift register. CHV and the outputs of the first three stages of the shift register (1, 2 and 3) are applied to the inputs of G169.

The output of G169 is applied to conductor C. Thus, CHV controls color selection. More specifically, in accordance with the A, B and C inputs to the color code selection network, the output of the chroma phase/color designates a color. A and B are fixed and C is variable. Normally, the output of G169 is a zero. A character, however, causes the output of G169 to achieve a one state. This one, through the color code selection network, changes the output of the chroma phase/color decoder so that a different color is generated. Thus, the background is in one color and the characters are in a different color. The output of the highest stage (5) of the shift register is applied through I56 to the summation circuit 380. Thus, the output of I56 remains CHV, delayed by five dot times.

SUMMARY

It will be appreciated at this point that a complete system has been described. As illustrated in FIG. 1, the computer control logic 112 receives data from a variety of sources. In addition, it receives timing information from a frequency synthesizer 110. In accordance with its inputs, the computer control logic informs the computer 114 when the various sources are generating input data. In accordance with this information, the computer, in accordance with a selection code, receives the incoming data. The data or information is received by the computer where it is stored in a suitable memory. The computer either uses the information directly or in accordance with its program edits the information into predetermined areas of subject matter, such as information related to sports events, information related to local news, information related to national news, etc. The computer then, through the output control logic of the computer control logic, applies its stored and/or edited instructions to the different channels of the overall system. A chosen channel receives its instructions in digital form and utilizes them to control an alphanumeric character display related to a particular subject matter. The characters are in one color and the background is in a different color. In fact, if desired, the system can be modified, so that a TV screen can be split into two different background colors with different colored characters being located in each background. Thus, information, such as a temper-

ature display, as well as a message, such as an advertising message, can be simultaneously displayed on different areas of a single TV screen.

SCROLLING LOGIC

In many cases, it is desirable for reading purposes to have the alphanumeric displays appear to scroll upward or downward, as desired. That is, if a particular channel desires to display more information that can be included in a single sixteen line display, it may be desirable to make the display appear to move upward as the display is switched from "page-to-page." A block diagram of this optional feature of the invention is illustrated in FIG. 57.

The scrolling logic illustrated in FIG. 57 comprises enable clock logic 400; a roll/slip counter 402; an RST/VSC circuit 404; a vertical slip counter 406; a roll start address 408; a page select counter 410; page select logic 412; and, a master clear 414. In essence, the scrolling logic illustrated in FIG. 57 generates signals designated L'0-L'3 and V'4-V'8 which are substituted for the L0-L3 and V4-V8 signals generated by the sync generator. Additional pulses are added to or deleted from these standard sync signals to provide new sync signals which cause the display to appear to move upward, or downward. In addition, the page select counter, in accordance with an output from the roll start address 408, controls switching from one page to another page of the page storage register of the character generator. Thus, as one page scrolls upwardly (or downwardly) the next page moves onto the screen to provide a continuously scrolling display. Hence, there appears to be sixteen rows of characters on the screen at all times, even though some rows may be portions of one "page" and the other rows portions of the following "page."

Enable clock logic suitable for use in the scrolling logic illustrated in FIG. 57 is illustrated in FIG. 58 and comprises two two-input NOR gates designated G301 and G303; and, two two-input NAND gates designated G305 and G307. L'0 and L'1 generated by the vertical slip counter 406 in the manner hereinafter described are connected, respectively, to the two inputs of G301. L'2 and L'3, also generated by the vertical slip counter, are applied to the two inputs of G303, respectively. The output of G301 is designated ECK', which is substituted by a suitable switching means for the ECK signal previously described.

The outputs from G301 and G303 are each connected to one of the inputs of G305. The output of G305 is designated CHL'0. This signal is substituted for the CHL0 signal previously described. CHL'0 is also applied to one input of G307. $\overline{C5}$ is applied to the second input of G307. The output of G307 is designated LSW' signal. LSW' is substituted for the LSW signal previously described.

It will be appreciated from viewing FIG. 58 that the enable clock logic generates substitute ECK, CHL0 and LSW signals in accordance with the generation of substitute L0, L1, L2 and L3 signals generated by the vertical slip counter. These "new" signals are necessary in order for functions related to the display to be appropriately timed.

A roll/slip counter suitable for use in the scrolling logic illustrated in FIG. 57 is illustrated in FIG. 59 and comprises a divide-by-96 counter 415; a divide-by-12 counter 416; three D flip-flops designated FF50, FF51

and FF52; an AND gates designated G308; three two-input NAND gates designated G309, G310, and G312; an AND gate designated G311; two two-input NOR gates designated G314 and G316; and, three inverters designated I80, I80A and I81.

VDT through I80 is applied to the C input of the divide-by-96 counter 415 and to the C input of the divide-by-12 counter 416. WRM, generated by the hereinafter described page select logic 412 is applied to the enable input of the divide-by-96 counter. UDC, which is a up/down control signal that controls whether or not the display is to scroll up or down depending upon whether or not it is a one or a zero state, is applied to one input of G314 and through I81 to one input of G316. A conductor designated 601, from the vertical slip counter, is connected to one input of G308. In addition, a signal designated $\overline{MC}$ is applied to the second input of G308. The output of G308 is applied to the clear input of the divide-by-96 counter 415.

The output of the first stage of the divide-by-96 counter 415 (VDT/2) is applied to one input of G311. The 96 count outputs of appropriate stages of the divide-by-96 counter are applied to the inputs of G309. Thus, when the divide-by-96 counter counts 96 VDT pulses the output of G309 drops from one-to-zero. This output is applied to the clock input of FF50 and to the load input of the divide-by-96 counter causing it to reset to an initial state whereby 96 additional VDT pulses causes it to again be reset, i.e., the divide-by-96 counter is a presettable counter.

The D input of FF50 is always high. Thus, when FF50 is clocked it is set. The Q output of FF50 is applied to the D input of FF51. The output of I80 is applied to the C input of FF51. Conductor 601 is connected to the R inputs of FF50 and FF51. The $\overline{Q}$ output of FF50 is applied to a conductor designated 611 which is connected to the RST/VSC 404, hereinafter described. The Q output of FF51 is applied to the second input of G311.

The output of G311 is applied to one input of G312 and to the enable input of the divide-by-12 counter 416. The 12 pulse count outputs of the divide-by-12 counter are applied to the inputs of G310. The output of G310 is applied to the D input of FF52 (FF52 is an inverted D flip-flop; that is a zero on the D input of FF52 when it is clocked creates a one on its Q output). The output of G310 is also applied to the load input of the divide-by-12 counter 416 causing it to load a preset value each time a zero occurs on the output of G310, i.e., the divide-by-12 counter is also a presettable counter.

FF52 is clocked by the output of I80. The output of I80 is also applied to a conductor designated 613 which is connected to the RST/VSC and to the master clear, the signal on this conductor is $\overline{VDT}$.

The Q output of FF52 is applied to a conductor designated 609 and connected to the vertical slip counter. The $\overline{Q}$ output of FF52 is connected to the second input of G312. The output of G312 is applied to the second inputs of G314 and G316. The output of G314 is applied to a conductor designated 603 and the output of G316 is applied to a conductor designated 605. Conductors 603 and 605 are connected to the vertical slip counter. The input of I81 is applied to a conductor designated 607 and connected to the vertical slip counter and to the roll start address. The output of I81 is applied to a conductor designated 621 and connected to the roll start address.

The divide-by-96 counter 415 is basically a timer that determines the time between roll sequences. A new roll sequence is started after 96 frames have been displayed subsequent to the termination of the previous roll sequence. That is, after 96 VDT pulses have occurred the divide-by-96 counter generates an output pulse which resets it and clocks FF50. Since the D input of FF50 is high, the clock pulse sets FF50. The next VDT pulse clocks FF51, setting it. When this occurs the divide-by-12 counter is enabled to count VDT pulses. The number 12 is used to relate the output to the number of lines making up a row of characters. At this time, the $\overline{Q}$ output of FF52 is in a one state. Thus, the VDT/2 pulses passing through G311 clock the output of G312 which in turn clocks G314 and G316. Depending upon the status of UDC (one or zero) either the output of G314 or the output of G316 carries pulses. These pulses are applied to the vertical slip counter to cause the display to slip up or down one line each frame. If pulses occur on the output of G314 the display appears to slip up and if the pulses occur on the output of G316 the image appears to slip down. After twelve slip frames, a zero is presented to the D input of FF52 to cause its Q output to drop to one, thus, terminating the pulse outputs of G314 or G316. The next VDT pulse clocks a one into FF52. This one causes a one to zero shift in the Q output of FF52 causing the vertical slip counter to be brought back into synchronization with the overall system, as hereinafter described. After the divide-by-96 counter has counted 96 or more VDT pulses the sequence repeats.

FIG. 60 is a block diagram illustrating an RST/VSC suitable for use in the scrolling logic illustrated in FIG. 57. RST/VSC designates reset vertical slip counter. The RST/VSC illustrated in FIG. 60 comprises a D-flip-flop designated FF53. Conductor 611 is connected to the D input of FF53 and conductor 613 is connected to the C input of FF53. The $\overline{Q}$ output of FF53 is designated $\overline{CLV}$ and is applied to the hereinafter described vertical slip counter. $\overline{CLV}$ resets the vertical slip counter when it shifts down from one to zero. The Q output of FF53 is connected to the R input of FF53; however, there is a delay created by C10.

As will be appreciated from viewing FIG. 60, when FF50 of the roll/slip counter is reset by the vertical slip counter as hereinafter described and $\overline{VDT}$ clocks FF53, the Q output of FF53 resets the vertical slip counter, and thereafter, resets itself.

FIG. 61 is a block diagram illustrating a vertical slip counter suitable for use in the scrolling logic illustrated in FIG. 57 and comprises first and second presettable counters 418 and 420; a D flip-flop designated FF54; two JK flip-flops designated FF55 and FF56; three two-input AND gates designated G317, G318 and G319; a two-input NOR gate designated G320; six two-input NAND gates designated G321-G326; three-input NAND gates designated G328, G329 and G330; and four inverters designated I82, I83, I84 and I85.

Conductor 603 from the roll/slip counter is connected to one input of G321 and conductor 605 also from the roll/slip counter is connected to one input of G323 and through I83 to one input of G322. The signals on these conductors are the up or down slip pulses from G314 and G316, respectively.

The first presettable counter 418 is adapted to generate signals designated L'0, L'1, L'2 and L'3. These signals are substituted for the L1-L3 signals when the in-

vention is in a scrolling mode of operation. $\overline{C5}$ is applied to the clock input of the first presettable counter 418. L'0 is applied to one input of G317. L'3 is applied to the second input of G317. The output of G317 is connected to the second input of G321. L'1 is applied to one input of G318 and L'2 is applied to the second input of G318. The output of G318 is connected to one input of G319 and to the second input of G322. L'0 is also applied to the second input of G319. The output of G319 is connected to the second input of G323, one input of G325 and one input of G320.

The outputs of G321, G322 and G323 are connected to the three inputs of G328. The output of G328 is connected to an input of G330. The output of G330 is connected through I84 to the K input of FF55, the K input of FF56, and one input of G320. The output of G320 is connected to the load input of the first presettable counter 418. The output of G330 is also connected to one input of G326, and the output of G326 is connected to the load input of the second presettable counter 420. Thus, it will be appreciated that the output of G328 in essence forms a signal adapted to reset FF55 and FF56, and the first and second presettable counters when appropriately clocked with other signals.

L'3 is also connected through I86 to the clock (C) input of the second presettable counter 420. Thus, L'3 clocks the second presettable counter. The output of I86 is also connected to the C input of FF54. The outputs of certain stages of the second presettable counter 420 are designated V'4, V'5, V'6 and V'7. These signals are substituted for the V4-V7 signals generated by the sync generator when the apparatus of the invention is in the scrolling mode of operation. V'5 and V'6 are also connected to the two inputs of G324. The output of G324 is connected to the second input of G330 and to the second input of G329. The overflow output (CO) of the second presettable counter is connected to the second input of G325. The output of G325 is connected to the J input of FF55 and the D input of FF54. $\overline{C5}$ is applied through I82 to the C inputs of FF55 and FF56. Thus, in addition to clocking the first presettable counter 418, $\overline{C5}$ also clocks FF55 and FF56.

The output of I84 provides a reset signal at the K inputs of these flip-flops when in a one state and they are clocked. The output of FF55 is connected to the third input of G330 and to an output terminal designated V'8. The Q output of FF55 is designated V'8. V'8 and V'8 are substitutes for the V8 and V8 signals, generated by the sync generator, when the apparatus of the invention is in a scrolling mode of operation. CLV from the RST/VSC flip-flop (FF53) illustrated in FIG. 60 is applied to the clear inputs of the first and second presettable counters, the reset input of FF55 and the reset input of FF56. Thus, all of these counters and flip-flops are reset when the RST/VSC flip-flop is clocked with a one on its data input. As previously indicated, FF53 is a reset flip-flop that resets the vertical sync counter after the roll/slip counter has created twelve up or down slip pulses. FF54 is reset by a pulse on conductor 609 generated by FF52 of the roll/slip counter after 12 frames during a slip as counted by the divide-by-12 counter 416.

L'0 is applied to the third input of G329. The output of G329 is connected through I85 to the J input of FF56. The Q output of FF56 is a signal designated VDT' which is substituted for the VDT signal normally

generated by the sync generator. It should be noted, however, that VDT' is not a substitute for the VDT signal applied to the herein described scrolling logic. Rather, the VDT' signal is applied to the other subsystems of the invention which require a VDT signal for correct operation.

In general, it will be appreciated from viewing FIG. 61 that the up/down pulses on lines 603 and 605 add to or subtract from the pulse count controlling the loading of the preset inputs to the first and second presettable counters. More specifically, the output of G319 through G320 loads the preset inputs to the first presettable counter 418 once each twelve TV lines. In addition, ignoring the action of the pulses on conductors 603 and 605 for the moment, on the eleventh TV line of the twentysecond row (TV line $263 - 12 \times 21 + 11$), the output of G330 loads the preset inputs to both presettable counters. To provide up or down slip, this normal method of operation is modified by causing loading of the presettable counters one TV line earlier or one TV line later. The pulses on conductors 603 and 605 create this effect. Thus, once each "frame," the TV display slips up or down one line, as the case may be. In addition, at the end of twelve such slip frames, FF54 is reset to change one of the preset inputs to the second presettable counter. Thus, the next time the second presettable counter is loaded, it is brought back into synchronization, i.e., back to the timing point it would have been without the roll sequence. Thereafter, the sequence is repeated in the manner previously described. It should be noted that the resetting of FF54 causes resetting of FF50 and FF51 of the roll/slip counter allowing these flip-flops to be cleared for the start of the next roll sequence.

FIG. 62 is a block diagram illustrating a roll/start address counter suitable for use by the scrolling logic and comprises: first and second up/down counters 422 and 423; and two two-input NAND gates designated G331, G332, and an inverter designated I82. Conductor 607 from the roll/slip counter (carrying up indication pulses) is connected to one input of G331. Conductor 621 (carrying down indication pulses) is connected to one input of G332. Conductor 623 is connected to the second inputs of both G331 and G332. The output of G331 is connected to the UP of the first up/down counter 422 and the output of G332 is connected to DN of the first up/down counter 422. Thus, during a roll sequence, the first up/down counter counts up or down one row of TV characters, depending upon whether G331 or G332 is gated to pass the zero pulse occurring on the Q output of FF54 when it is reset. The first up/down counter has four outputs applied to four conductors designated 701, 702, 703 and 704. These conductors carry a character row code which represents the sixteen character lines of the display and are connected to the page select counter hereinafter described. When an up or a down pulse is counted by the first UP/DN counter 422, the code on conductors 701-704 changes to indicate a rolling up or down of one row of characters. The up overflow output (CO) of the first up/down counter 422 is connected through I82 to the up input of the second up/down counter 423. Thus, each time sixteen rows have been rolled up to designate a complete page scroll, the second up/down counter counts up by one pulse.

The down overflow (BO) of the first up/down counter 422 is connected to the down input of the sec-

ond up/down counter 423. Thus, when sixteen rows of characters have been rolled down, the second up/down counter is decremented by one pulse.

The outputs of the stages of the second up/down counter 423 are applied to a plurality of conductors designated 705, 706, 707 and 708. The signals on these conductors contain a page code which defines the pages of the page storage register of the character generator. Conductors 705, 706, 707 and 708 are connected to the page select counter and, thus, control the selection of a particular page of the character generator. More specifically, as previously indicated, the character generator includes eight sets of six, 512 bit recirculating shift registers, each set of which defines a particular page of characters. The outputs of the second up/down counter when decoded properly select one of these "pages" for display (or parts of two pages if the display is being scrolled).

FIG. 63 is a block diagram illustrating a page select counter suitable for use by the scrolling logic illustrated in FIG. 57 and comprises a presettable divide-by-16 counter 424 and a presettable divide-by-8 counter 426. Conductors 701-704 are connected to the preset inputs on the presettable divide-by-16 counter. Conductors 705-708 are connected to the preset inputs of the divide-by-8 presettable counter. The load inputs of both counters receive a signal designated $\overline{MC}$, generated by the master clear hereinafter described. $\overline{CHLO}$ ' (designates character line zero), generated by the enable clock logic illustrated in FIG. 58, is applied to the enable input of counter 424. $\overline{C5}$ is applied to the clock inputs of both counters and $\overline{VDT}$ is applied to the clear inputs of both counters.

The divide-by-16 counter is a presettable counter and is clocked by $\overline{C5}$. Thus, each time $\overline{VDT}$ occurs, the inputs on conductors 701-704 are "looked at." When the state of the outputs of the first up/down counter 422 indicates that 16 rows of characters (sixteen rows minus the start address) have been counted, the overflow output of the divide-by-16 counter generates an enable signal which enables the divide-by-8 counter to receive a $\overline{C5}$ pulse. This pulse causes the divide-by-8 counter to increment the output code on conductors 709, 710 and 711. The signals on conductors 709, 710 and 711 are decoded by the page select logic, as hereinafter described, and used to control which of the sets of six 512 bit shift registers is being used to generate characters at any particular period of time. Because the divide-by-16 counter can enable the divide-by-8 counter at any time, depending upon the start address that was preset, it will be appreciated that the change from one page to a second page can occur at any point on the display. In other words, part of one page can be shown at the top and part of the second page can be shown at the bottom of the display and, the split position will move up or down as the display is scrolled up or down.

Page select logic suitable for use by the scrolling logic is illustrated in FIG. 64 and comprises a decoder 427; nine AND gates designated G334-G342; eight NAND gates designated G343-G350; and, a D flip-flop designated FF57.

Conductors 709, 710 and 711 are connected to the three inputs of the decoder 427. In accordance with the binary code carried by these conductors, the decoder selects one of its eight outputs to carry a zero. The eight outputs are separately connected each to one input of

G343-G350. The other inputs of G343-G350 are connected to receive a signal designated $\overline{MC}$. $\overline{MC}$ is generated by a master clear logic hereinafter described and controls the gating of G343-G350. $\overline{WRT}$, generated by the write timing circuit of the character generator, is applied to one input of G334. The second input of G334 receives a signal designated $\overline{WRM}$. $\overline{WRM}$ is a signal which designates that new information can be written into the sets of six 512 bit shift registers. $\overline{WRM}$ is generated by FF57. The D input FF57 is unconnected. $\overline{LOAD}$ is applied to the C input of FF57, $\overline{O}$ is applied to the S input of FF57 and $\overline{P}$ is applied to the R input of FF57. $\overline{O}$ and $\overline{P}$ are generated by the decoder of the character generator and, as heretofore described, determine whether or not instructions are being applied to the sets of six 512 bit recirculating shift registers. Thus, they determine whether $\overline{WRM}$ is in a one or a zero state. $\overline{LOAD}$ clocks a one into FF57 at the end of each load cycle.

The output of G334 is connected to one input of each of G335-G342. The second inputs of G335-G342 are connected to the outputs of G343-G350 on a one-to-one basis. The outputs of G335-G342 are the $\overline{WO}$ - $\overline{W7}$ signals applied to the eight sets of six, 512 bit shift registers of the character generator. The outputs of G343-G350, respectively, are the $\overline{RO}$ - $\overline{R7}$ signals applied to the eight sets of six, 512 bit shift registers. Thus, the outputs of G343-G350 control the reading out from the sets of six, 512 bit shift registers and the outputs of G335-G340 control the writing into these registers.

FIG. 65 is a block diagram illustrating a master clear suitable for use by the scrolling logic and comprises a time delay 428; and, two D flip-flops designated FF58 and FF59. $\overline{PWR}$ is applied to the S input of FF58 via the time delay. The D input FF58 is connected to ground. $\overline{VDT}$ is applied to the C inputs of FF58 and FF59. The Q output of FF58 is applied to the C input of FF59.

When power is first applied to the system, it sets FF58 after a delay created by the time delay 428. Thereafter, a $\overline{VDT}$ pulse clocks FF58, causing its grounded data input to place it in a reset state. The first $\overline{VDT}$ pulse clocks FF59 setting it. The next $\overline{VDT}$ pulse resets FF59 because the Q output of FF58 is now zero. The Q output of FF59 is the $\overline{MC}$ signal applied to the various subsystems previously described for initial clearing purposes. Unless power fails or is shut off, the master clear has no additional effect on the overall system.

PAGE LOGIC

FIG. 66 is a block diagram of a page logic suitable for use as an alternate to the scrolling logic illustrated in FIG. 57. The page logic illustrated in FIG. 66 comprises a counter 430; an advance page timer 432; a master clear 343 (similar to the master clear illustrated in FIG. 65); and, page select logic 436 (similar to the page select logic illustrated in FIG. 64). The page select logic controls the readout from the eight sets of six, 512 bit recirculating shift registers of the character generator by switching from one page to the next page each time the advance page timer 432 applies a pulse to the counter 430. As these pulses are counted, the binary code carried by three conductors designated 801, 803 and 805 changes. In accordance with change, a "new" page is chosen for display. That is, this change is de-

coded by a page select logic of the type illustrated in FIG. 64 and is utilized to control which of the particular pages stored in the character address selector is to be displayed until the output from the counter changes again, when a new page is chosen.

It will be appreciated from the foregoing description that a system for controlling the display on a plurality of television channels is provided by the invention. The displays are alphanumeric displays and can relate to a variety of different subject matter. One channel can be dedicated to one type of subject matter, and other channels dedicated to different types of subject matter. The character displays are all controlled by a digital mechanism under the control of a computer. The computer receives information from a variety of sources in a priority manner. In accordance with this information, it generates instructions which control the character displays. If desired, the computer can be programmed to edit the input information into different areas of subject matter and then cause the display of the edited information. Alternatively, information can be fed directly through the computer without editing, such as, for example, temperature information, and displayed on a single channel. However, this information can be updated at predetermined intervals, as desired. In addition, the displays, if desired, can be combined in a manner such that a portion of the display represents information, such as meeting information, and another portion of the display represents another type of information, such as advertising information. Thus, the invention has widespread flexibility without being unduly complicated.

It will be appreciated by those skilled in the art and others that various changes can be made in the preferred embodiment herein described without departing from the spirit and scope of the invention. Hence, the invention can be practiced otherwise than is specifically described herein.

The embodiments of the invention in which an exclusive property or privilege is claimed as defined as follows:

1. A multiple channel alphanumeric residential television video signal generator for receiving information from a variety of sources, such as keyboard, newswire, weather service and stockline sources, and creating video signals suitable for creating a plurality of channel related alphanumeric displays on residential television receivers, each alphanumeric display being dedicated to information related to a particular subject matter, such as weather, sports, general news, local news, stocks, etc., said multiple channel alphanumeric residential television video signal generator comprising:

1. a digital computer suitable for receiving information related to a variety of subjects, manipulating that information and, in accordance therewith, generating a variety of control instructions;
2. computer control logic connected to said digital computer, said computer control logic comprising:
 - a. at least one dial-up port adapted to receive keyboard generated information from a keyboard source, and dialup port control instructions from said computer, and apply said received keyboard information to said computer in accordance with said dial-up port control instructions;
 - b. at least one newswire interface adapted to receive newswire information, such as news information, weather information, and stock information,

tion from a newswire source, and newswire control instructions from said computer, and apply said received newswire information to said computer in accordance with said newswire control instructions;

- c. output display logic for receiving character generation instructions and output display logic instructions from said computer, and apply said character generation instructions to a multiple channel character generation means in accordance with said output display logic instructions; and,
- d. select logic means for:
 - i. receiving select logic instructions from said computer;
 - ii. selecting one of said at least one dial-up port, said at least one newswire interface, and said output display logic; and,
 - iii. controlling the application of said keyboard generated information, said newswire information and said character generation instructions to one of said computer and said multiple channel character generation means in accordance with said selection; and
3. multiple channel character generation means connected to said control logic means for receiving said character generation instructions and for creating, in accordance therewith, a plurality of video signals, one video signal related to one of a plurality of channels, said video signals being suitable for forming an alphanumeric display dedicated to a particular subject matter on the screen of residential television receivers adapted to receive said video signals.
2. A multiple channel alphanumeric residential television video signal generator as claimed in claim 1, wherein each of said at least one dial-up port, said at least one newswire interface, and said output display logic is adapted to apply an interrupt signal to said computer and generate an interrupt location identification signal when said at least one dial-up port, said at least one newswire interface and said output display logic is ready to transmit information to or receive instructions from said computer; and, wherein said computer control logic includes a priority encoder connected to said at least one dial-up port, said at least one newswire interface and said output display logic for receiving said interrupt signals and said interrupt location identification signals and for applying a digital information priority code to said computer in accordance with said received interrupt location identification signals, said priority code identifying the one of said at least one dial-up port, said at least one newswire interface and said output display logic ready to transmit information to or receive instructions from said computer having the highest priority when compared with the others of said at least one dial-up port, said at least one newswire interface and said output display logic.
3. A multiple channel alphanumeric residential television video signal generator as claimed in claim 2, wherein said keyboard generated information received by said at least one dial-up port and said newswire information received by said at least one newswire interface are in series digital form and wherein said computer control logic includes serial-to-parallel conversion means for converting said series digital keyboard generated and said newswire information from series form

to parallel form and applying said parallel form of said keyboard generated and said newline information to said computer.

4. A multiple channel alphanumeric residential television video signal generator as claimed in claim 3, wherein each of said at least one dial-up port, said at least one newline interface and said output display logic includes busy/done logic for applying signals to said computer indicating the busy status of its associated system when it is busy and the done status of its associated system when it is idle.

5. A multiple channel alphanumeric residential television video signal generator as claimed in claim 4, wherein said computer control logic includes a clock and thermometer interface adapted to receive a digital signal related to the time of day and temperature information in digital form related to the weather temperature, and clock and thermometer interface instructions from said computer, and apply said digital signal related to the time of day and said digital information related to weather temperature to said computer in accordance with said clock and thermometer interface control instructions, said clock and thermometer interface also generating an interrupt signal and an interrupt location identification signal and applying said signals to said computer and said priority encoder, respectively, said clock and thermometer interface further being connected to said select logic for receiving a selection signal from said select logic.

6. A multiple channel alphanumeric residential television video signal generator as claimed in claim 5 including a frequency synthesizer: connected to said clock and thermometer interface for generating said timing signals related to the time of day; connected to said at least one dial-up port for applying clock pulses to said at least one dial-up port, said clock pulses being used by said dial-up port to control the rate of conversion of the serially received keyboard information into parallel information suitable for application to said computer; and, connected to said at least one newline interface for applying clock pulses to said at least one newline interface, said clock pulses being used by said at least one newline interface to control the rate of conversion of the serially received newline information into parallel information suitable for application to said computer.

7. A multiple channel alphanumeric residential television video signal generator as claimed in claim 6, wherein said character generation instructions include character address instructions and character nature instructions and wherein said multiple channel character generator generation means includes, for each of said plurality of channels:

A. a character address selector for receiving said character address instructions and for generating a character address signal in accordance therewith; and

B. a character generator connected to said character address selector in a manner such that said character generator is selectively made operative to receive said character is selectively made operative to receive said character nature instructions.

8. A multiple channel alphanumeric residential television video signal generator as claimed in claim 7, wherein the video signals are adapted to form a noninterlaced display on residential television receivers

adapted to receive and display in alphanumeric form the information contained in said video signals.

9. A multiple channel alphanumeric residential television video signal generator as claimed in claim 8 including a sync generator connected to said character generator, said sync generator generating a plurality of timing signals suitable for use by said character generator, said plurality of timing signals including a set of binary code signals, said code signals uniquely identifying dot points on the face of the cathode ray tube of a residential television receiver.

10. A multiple channel alphanumeric residential television video signal generator as claimed in claim 9 wherein said binary code which uniquely identifies dot points on the face of the cathode ray tube of a residential television receiver is broken into dot position identification codes, character position identification codes, TV line identification codes and character row position identification codes, each code being defined in a binary manner.

11. A multiple channel alphanumeric residential television video signal generator as claimed in claim 10, wherein said dot position identification codes identify seven dots on a television receiver for each of said character positions; wherein said character position codes identify 52 character positions on a TV scan line; wherein said TV line identification codes identify 12 lines for each of said row position codes; and, wherein said row position identification codes identify a plurality of character rows.

12. A multiple channel alphanumeric residential television video signal generator as claimed in claim 11, wherein said noninterlaced scan produces 263 television lines, said 263 television lines creating an entire alphanumeric display produced as a result of the receipt of one of said plurality of video signals.

13. A multiple channel alphanumeric residential television video signal generator as claimed in claim 12, wherein 16 rows of characters are displayed on said cathode ray tube of a residential television receiver receiving one of said video signals and producing an alphanumeric display in accordance therewith, and wherein only 32 of the 52 character positions on a TV scan line are utilized in a single display.

14. A multiple channel alphanumeric residential television video signal generator as claimed in claim 7, wherein at least one of said character generators includes a page storage means suitable for storing all of the character instructions necessary to identify the characters to be displayed on a complete display, said character generator further including row storage registers connected to the output of said page storage register to read out and store all of the information related to a particular row of characters at one time.

15. A multiple channel alphanumeric residential television video signal generator as claimed in claim 14, including a plurality of chroma generators, one being connected to the output of each of said character generators for adding color information to the video signal output of its associated character generator.

16. A multiple channel alphanumeric residential television video signal generator as claimed in claim 14, wherein said page storage means is adapted to store all of the character nature instructions necessary to display a plurality of complete displays; and, including means to switch the display from page-to-page of the

character nature instructions stored by said page storage means in a sequential manner.

17. A multiple channel alphanumeric residential television video signal generator as claimed in claim 16 including at least one scrolling logic connected to at least one of said plurality of character generators for causing the television display of the associated channel to appear to scroll as the display switches from page-to-page of the pages stored in said page storage register, whereby a complete display made up of one of more pages is always displayed on a residential television receiver receiving the video signal related to said at least one of said plurality of character generators.

18. A multiple channel alphanumeric residential television video signal generator as claimed in claim 1, wherein said computer control logic includes a clock and thermometer interface adapted to receive a digital signal related to the time of day and temperature information in digital form related to the weather temperature, and clock and thermometer interface instructions from said computer, and apply said digital signal related to the time of day and said digital information related to weather temperature to said computer in accordance with said clock and thermometer interface control instructions, said clock and thermometer interface also generating an interrupt signal and an interrupt location identification signal and applying said signals to said computer and said priority encoder, respectively, said clock and thermometer interface further being connected to said select logic for receiving a selection signal from said select logic.

19. A multiple channel alphanumeric residential television video signal generator as claimed in claim 18, wherein said keyboard generated information received by said at least one dial-up port and said newswire information received by said at least one newswire interface are in series digital form and wherein said computer control logic includes serial-to-parallel conversion means for converting said series digital keyboard generated and said newswire information from series form to parallel form and applying said parallel form of said keyboard generated and said newswire information to said computer.

20. A multiple channel alphanumeric residential television video signal generator as claimed in claim 19 including a frequency synthesizer: connected to said clock and thermometer interface for generating said timing signals related to the time of day; connected to said at least one dial-up port for applying clock pulses to said at least one dial-up port, said clock pulses being used by said dial-up port to control the rate of conversion of the serially received keyboard information into parallel information suitable for application to said computer; and, connected to said at least one newswire interface for applying clock pulses to said at least one newswire interface, said clock pulses being used by said at least one newswire interface to control the rate of conversion of the serially received newswire information into parallel information suitable for application to said computer.

21. A multiple channel alphanumeric residential television video signal generator as claimed in claim 1, wherein said character generation instructions include character address instructions and character nature instructions and wherein said multiple channel character generator generation means includes, for each of said plurality of channels:

A. a character address selector for receiving said character address instructions and for generating a character address signal in accordance therewith; and,

B. a character generator connected to said character address selector in a manner such that said character generator is selectively made operative to receive said character nature instructions.

22. A multiple channel alphanumeric residential television video signal generator as claimed in claim 21, wherein at least one of said character generators includes a page storage means suitable for storing all of the character instructions necessary to identify the characters to be displayed on a complete display, said character generator further including row storage registers connected to the output of said page storage register to read out and store all of the information related to a particular row of characters at one time.

23. A multiple channel alphanumeric residential television video signal generator as claimed in claim 22, wherein said page storage means is adapted to store all of the character nature instructions necessary to display a plurality of complete displays; and, including means to switch the display from page-to-page of the character nature instructions stored by said page storage means in a sequential manner.

24. A multiple channel alphanumeric residential television video signal generator as claimed in claim 23 including at least one scrolling logic connected to at least one of said plurality of character generators for causing the television display of the associated channel to appear to scroll as the display switches from page-to-page of the pages stored in said page storage register, whereby a complete display made up of one or more pages is always displayed on a residential television receiver receiving the video signal related to said at least one of said plurality of character generators.

25. A multiple channel alphanumeric residential television video signal generator as claimed in claim 21, including a plurality of chroma generators, one being connected to the output of each of said character generators for adding color information to the video signal output of its associated character generator.

26. A multiple channel alphanumeric residential television video signal generator as claimed in claim 25, wherein the video signals are adapted to form a noninterlaced display on residential television receivers adapted to receive and display in alphanumeric form the information contained in said video signals.

27. A multiple channel alphanumeric residential television video signal generator as claimed in claim 26, wherein said noninterlaced scan produces 263 television lines, said 263 television lines covering the entire face of the cathode ray tube of a residential television receiver creating an alphanumeric display produced as a result of the receipt of one of said plurality of video signals.

28. A multiple channel alphanumeric residential television video signal generator as claimed in claim 1, wherein the video signals are adapted to form a noninterlaced display on residential television receivers adapted to receive and display in alphanumeric form the information contained in said video signals.

29. A multiple channel alphanumeric residential television video signal generator as claimed in claim 28, wherein said noninterlaced scan produces 263 television lines, said 263 television lines covering the entire face of the cathode ray tube of a residential television receiver creating an alphanumeric display produced as a result of the receipt of one of said plurality of video signals.

* * * * *

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,909,818
DATED : September 30, 1975
INVENTOR(S) : James A. Dalke et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Specification:

Column 2, line 21, delete "televison" and insert therefor
--television--.

line 67, delete "televison" and insert therefor
--television--.

Column 3, line 51, delete "switch"" and insert therefor
--"switch"--.

Column 4, line 36, after the word "illustrated" add the
word --in--.

Columns 7 and 8, in the Computer Instructions and Information
Signals table, in the line that starts "DB1-DB8" delete
"UAR/I" and insert therefor --UAR/T--.

Column 11, line 66, delete "wire-service" and insert therefor
--wireservice--.

Column 13, line 35, delete "Of" and insert therefor --If--.
line 37, delete "illustrated" and insert therefor
--illustrates--.

Column 14, line 37, delete "adpated" and insert therefor
--adapted--.

Column 17, line 2, delete "be" and insert therefor --been--.
line 35, delete "IEQ3" and insert therefor --IRQ3--
line 56, delete "instructions" and insert therefor
--instruction--.

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Page - 2

PATENT NO. : 3,909,818
DATED : September 30, 1975

INVENTOR(S) : James A. Dalke et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 18, line 16, delete " $\bar{Q}$ " and insert therefor --Q--.
line 18, delete "Q" and insert therefor -- $\bar{Q}$ --.
line 25, after the word "from" add the word --a--.
line 30, delete "POWER FAIL" and insert therefor
--POWER FAIL--.

Column 19, lines 56 and 57, delete the sentence "When SEL4 and the RS latch 188 of the connect/disconnenct logic."

Column 20, line 40, delete "instructinos" and insert therefor
--instructions--.

Column 21, line 22, delete "Q" and insert therefor -- $\bar{Q}$ --.

Column 22, line 37, delete "gaes" and insert therefor --gates--.

Column 24, line 8, delete "addition" and insert therefor
--operation--.

Column 25, line 20, after the word "the" add the word
--computer--.
line 27 and 28, delete "applied" and insert therefor
--decoder--.

line 37, delete "applid" and insert therefor
--applied--.

Column 26, line 49, delete "not" and insert therefor --no--.

Column 27, line 49, delete "chose" and insert therefor
--chosen--.

Column 30, line 22, delete "ooutput of G77 in" and insert
therefor --output of G77 is--.

line 61, delete "encloder" and insert therefor
--encoder--.

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. 3,909,818

DATED September 30, 1975

INVENTOR(S) James A. Dalke et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 31, line 37, delete "uncorrected" and insert therefor
--unconnected--.

line 45, delete "applied" and insert therefor
--applies--.

line 59, delete "pperiod" and insert therefor
--period--.

line 62, delete "UAR/I's." and insert therefor
--UAR/T's.--

Column 32, line 19, delete "ilustrating" and insert therefor
--illustrating--.

line 56, delete "subsystem" and insert therefor
--subsystems--.

line 57, delete "reeive" and insert therefor
--receive--.

Column 33, line 36, delete "F22" and insert therefor --FF22--.

Column 34, after line 7, add the paragraph:

--Thus, the output of G94 reaches a one state. The next RQENB one clocks the now zero output of G102 into FF23 creating a zero IRQ6 and a zero INTR. These signals are sensed by the priority encoder and used in the manner previously described. Further, the output of G100 is now in a zero state (when SEL6 is one) to indicate that the output display logic is done and the output display logic is "not" busy. The outputs of the word assembly register and the display selector register are transferred to the character generator and the character address selector at this time.--

line 54, delete "registor" and insert therefor
--register--.

line 56, delete "designates" and insert therefor
--designated--.

Page - 4

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,909,818
DATED : September 30, 1975
INVENTOR(S) James A. Dalke et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 37, line 2, delete "comparator" and insert therefor
--computer--.

line 16, delete "FF29" and insert therefor --FF28--

Column 38, line 64, delete "selector" and insert therefor
--selected--.

Column 39, line 23, delete "illustrtion" and insert therefor
--illustration--.

line 38, delete "G22" and insert therefor --G122--.

line 41, delete "of" and insert therefor --to--.

Column 40, line 3, delete "B" and insert therefor --"B"--.

line 4, delete "A" and insert therefor --"A"--.

line 11, delete "twoinput" and insert therefor
--two input--.

line 23, delete "syn" and insert therefor --sync--.

Column 41, line 2, delete "characterss" and insert therefor
--characters--.

line 26, delete "genertor" and insert therefor
--generator--.

line 46, after the word "TV" add the word --line--.

Column 42, line 64, delete "the" and insert therefor --The--.

Column 43, line 41, delete "otput" and insert therefor
--output--.

line 50, delete "ouptout" and insert therefor
--output--.

line 59, delete "charcter" and insert therefor
--character--.

Page - 5

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,909,818

DATED : September 30, 1975

INVENTOR(S) : James A. Dalke et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 44, line 25, delete "LOAD from" and insert therefor
--LOAD, from--.

Column 45, line 32, delete "informations" and insert therefor
--information--.

line 42, delete "converted" and insert therefor
--converter--.

Column 47, line 21, delete "signlas" and insert therefor
--signals--.

Column 48, line 9, delete "cound" and insert therefor --count--.
line 25, delete "intput" and insert therefor
--input--.

Column 50, line 17, after the word "conductor" insert --and,--

Column 55, line 46, after the word "The" insert --Q--.

Column 56, line 16, delete "twentysecond" and insert therefor
--twenty-second--.

line 64, delete "deisgnate" and insert therefor
--designate--.

line 66, after the word "overflow" add the word
--output--.

Column 58, line 36, after the word "input" add the word --of--
line 39, delete "Ff59" and insert therefor --FF59--

In the Claims:

Column 59, line 62, delete "dialup" and insert therefor
--dial-up--.

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,909,818
DATED : September 30, 1975
INVENTOR(S) : James A. Dalke et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 61, line 12, delete "alphanumeric" and insert therefor --alphanumeric--.

lines 20 and 21, delete "relalted" and insert therefor --related--.

line 58, after "and" insert therefor --,--.

lines 62 and 63, delete "said character is selectively made operative to receive".

Column 63, line 10, delete "of" and insert therefor --or--.

Signed and Sealed this

sixth Day of January 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks