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(71) Applicant: **APPLIED MATERIALS, INC.** [US/US];
3050 Bowers Avenue, Santa Clara, California 95054 (US).

(71) Applicant (for AG only): **FANG, Jun** [CN/CN]; Applied
Materials Xi'an Co. Ltd; No. 28 Xinx Road; Xi'an Hi-tech
Industrial Development Zone, Xi'an, Shaanxi 710119 (CN).

(72) Inventors: **FANG, Jun**; Applied Materials Xi'an Co. Ltd;
No. 28 Xinx Road; Xi'an Hi-tech Industrial Development
Zone, Xi'an, Shaanxi 710119 (CN). **CHI, Hyo-In**; c/o Ap-
plied Materials, Inc., Law Dept., M/S 1269 3050 Bowers
Avenue, Santa Clara, CA 95054 (US). **HO, Dustin W.**; Rm
904, No. 2, Alley 99; FangLi Road, Shanghai; 86928 Shang-
hai (CN).

(74) Agent: **LECOME INTELLECTUAL PROPERTY
AGENT LTD.**; 3rd Floor, Office Building, Tylfull Hotel,
No.1 Building, No.1-, Xitucheng Road, Haidian District,
Beijing 100088 (CN).

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ON MICROELECTRONIC STRUCTURES

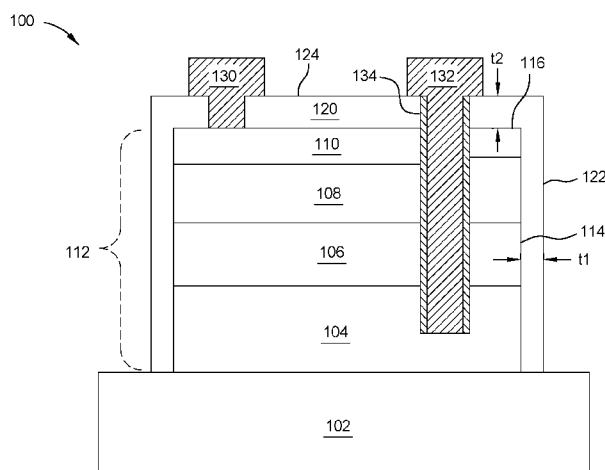


FIG. 1

(57) Abstract: A method to produce the microelectronic and display devices (e.g., micro-LEDs) which are coated with a passivation film is provided. In this method, a plasma-enhanced chemical vapor deposition (PE-CVD) process is provided and includes maintaining a flow of a deposition gas while pulsing an RF power between on and an off positions while simultaneously depositing a passivation film (120) on sidewall and top surfaces of a micro-LED structure or other display devices. The passivation film (120) contains silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof. The passivation film (120) has a step coverage of greater than 70% or greater than 80%, such that the step coverage is a ratio of an average thickness of a sidewall portion (122) of the passivation film (120) to an average thickness of a top portion (124) of the passivation film (120).



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PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION PROCESSES FOR DEPOSITING PASSIVATION FILMS ON MICROELECTRONIC STRUCTURES

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to vapor deposition processes, and in particular to plasma-enhanced chemical vapor deposition processes for depositing dielectric materials.

Description of the Related Art

[0002] The size of microelectronic and display devices, such as micro-light emitting diodes (LEDs), liquid crystal displays (LCDs), and other devices, becomes smaller with each generation of technology. As the devices become smaller, common deposition techniques become limited in ability to deposit the needed materials on various surfaces of the device.

[0003] Thermal chemical vapor deposition (CVD) of material films typically require high temperatures (e.g., about 200°C to about 500°C) which can deteriorate or destroy underlying materials which make-up smaller and more sophisticated devices. Also, CVD processes are generally not capable of forming conformal layers, especially when the underlying surfaces have both vertical and horizontal surfaces. Instead, CVD processes tend to deposit relatively thick films on the horizontal surfaces while leaving the vertical surfaces bare or with a relatively thin films, which may be magnitudes times thinner than the horizontal films. This lacks of step coverage is very undesirable for producing microelectronic and display devices.

[0004] Atomic layer deposition (ALD) can be used to produce conformal films on both horizontal and vertical surfaces. However, ALD, like CVD, also suffers from requiring high thermal budgets which can deteriorate or destroy sensitive materials within the underlying structure. In addition, ALD has a very slow deposition rate which increases production time and costs to a level that ALD is not practical to use for deposited films thicker than a few angstroms.

[0005] Therefore, there is a need for improved vapor deposition processes and microelectronic and display devices produced by such methods.

SUMMARY

[0006] Embodiments of the present disclosure generally relate to plasma-enhanced chemical vapor deposition (PE-CVD) processes for depositing dielectric materials on microelectronic and display devices, such as micro-light emitting diodes (LEDs), liquid crystal displays (LCDs). Embodiments are also related to the devices produced by these deposition processes.

[0007] In one or more embodiments, a method for depositing a silicon-containing passivation film on a micro-LED structure is provided and includes introducing one or more silicon precursors and one or more reagent gases into a processing chamber containing a substrate, generating a plasma within the processing chamber by a radio frequency (RF) power, and exposing the micro-LED structure disposed on the substrate to a deposition gas containing one or more silicon precursors and one or more reagent gases. The method also includes maintaining a flow of the deposition gas while pulsing the RF power between an on-position and an off-position and simultaneously depositing a passivation film on a sidewall surface and a top surface of the micro-LED structure. The passivation film contains silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof. A sidewall portion of the passivation film is deposited on the sidewall surface of the micro-LED structure and a top portion of the passivation film is deposited on the top surface of the micro-LED structure. The passivation film has a step coverage of greater than 70%, such that the step coverage is a ratio of an average thickness of the sidewall portion of the passivation film to an average thickness of the top portion of the passivation film.

[0008] In some embodiments, a micro-LED structure includes a film stack disposed on a substrate and a passivation film disposed on a sidewall surface and a top surface of the film stack. The film stack contains a multiple quantum well (MQW) layer disposed between an n-doped layer and a p-doped layer and an indium tin oxide (ITO) layer disposed on the p-doped layer. The passivation film contains silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof. A sidewall portion of the passivation film is disposed on the sidewall surface of the micro-LED structure and a top portion of the passivation film is disposed on the top surface of the micro-LED

structure. The passivation film has a step coverage of greater than 70%, such that the step coverage is a ratio of an average thickness of the sidewall portion of the passivation film to an average thickness of the top portion of the passivation film. Each of the average thicknesses of the sidewall portion and the top portion is independently about 50 nm to about 700 nm.

[0009] In one or more examples, the passivation film contains silicon oxide, the step coverage is greater than 78%, and the reagent gas is or contains nitrous oxide. In other examples, the passivation film contains silicon nitride, the step coverage is greater than 80%, and the reagent gas is or contains ammonia. In some examples, the passivation film contains silicon oxynitride, the step coverage is greater than 78%, and the reagent gas is or contains nitrous oxide and ammonia.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope, may admit to other equally effective embodiments.

[0011] Figure 1 is a schematic cross-sectional view of a micro-LED structure containing a passivation film, according to one or more embodiments described and discussed herein.

[0012] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the Figures. It is contemplated that elements and features of one or more embodiments may be beneficially incorporated in other embodiments.

DETAILED DESCRIPTION

[0013] Embodiments of the present disclosure generally relate to pulsed plasma-enhanced chemical vapor deposition (PE-CVD) processes for depositing silicon-containing passivation film on microelectronic and display devices. Embodiments are also related to the microelectronic and display devices, such as micro-light emitting

diodes (LEDs), liquid crystal displays (LCDs), having passivation films produced by the pulsed PE-CVD processes.

[0014] In one or more embodiments, a method for depositing a silicon-containing passivation film on a micro-LED structure is provided and includes placing a substrate containing one or more device structures into a processing chamber, such as a PE-CVD chamber, introducing one or more silicon precursors and one or more reagent gases into the processing chamber containing the substrate, generating a plasma within the processing chamber by a radio frequency (RF) power, and exposing the one or more device structures disposed on the substrate to a deposition gas containing one or more silicon precursors and one or more reagent gases. The method also includes maintaining a flow of the deposition gas while pulsing the RF power between an on-position and an off-position and simultaneously depositing a passivation film on a sidewall surface and a top surface of the device structure. The passivation film contains silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof. A sidewall portion of the passivation film is deposited on the sidewall surface of the device structure and a top portion of the passivation film is deposited on the top surface of the device structure. The passivation film has a step coverage of greater than 70%, greater than 75%, or greater than 80%, such that the step coverage is a ratio of an average thickness of the sidewall portion of the passivation film to an average thickness of the top portion of the passivation film.

[0015] Figure 1 is a schematic cross-sectional view of a micro-LED structure 100 containing a film stack 112 disposed on a substrate 102. In one or more embodiments, the substrate 102 may be a material such as crystalline silicon (e.g., Si<100> or Si<111>), silicon oxide, strained silicon, silicon germanium, doped or undoped polysilicon, doped or undoped silicon substrates and patterned or non-patterned substrates silicon on insulator (SOI), carbon doped silicon oxides, silicon carbide, silicon nitride, doped silicon, germanium, gallium arsenide, gallium nitride, glass, sapphire, quartz, one or more polymeric materials, or any combination thereof. The substrate 102 may have various dimensions, such as 200 mm, 300 mm, 450 mm, or other diameter substrates, as well as, rectangular or square panels. Unless otherwise noted, embodiments and examples described herein are conducted on substrates with a 200 mm diameter, a 300 mm diameter, or a 450 mm diameter. In the embodiment wherein a SOI structure is utilized for the substrate 102, the substrate

102 can include a buried dielectric layer disposed on a silicon crystalline substrate. In some examples, the SOI substrate contains a film or layer of gallium nitride. In one or more examples, the substrate 102 can be or include a sapphire. In some examples, the substrate 102 can be or include a silicon carbide substrate containing gallium nitride. In other examples, the substrate 102 can be or include a crystalline silicon substrate.

[0016] The film stack 112 contains at least an n-doped layer 104, a multiple quantum well (MQW) layer 106, a p-doped layer 108, and an indium tin oxide (ITO) layer 110. The MQW layer 106 is disposed between the n-doped layer 104 and the p-doped layer 108 and the ITO layer 110 is disposed on the p-doped layer 108. In one or more examples, the n-doped layer 104 contains n-doped gallium nitride, the MQW layer 106 contains a film stack of alternating indium gallium nitride layers and gallium nitride layers, the p-doped layer 108 contains p-doped gallium nitride, and the ITO layer 110 contains indium tin oxide.

[0017] A passivation film 120 is deposited, formed, or otherwise disposed on and over the film stack 112. As such, the passivation film 120 is disposed on a sidewall surface 114 of the film stack 112 and on a top surface 116 of the film stack 112. A sidewall portion 122 of the passivation film 120 is disposed, deposited, or otherwise formed on the sidewall surface 114 of the film stack 112 and a top portion 124 of the passivation film 120 is disposed, deposited, or otherwise formed on the top surface 116 of the film stack 112, as depicted in Figure 1. In one or more examples, the passivation film 120 contains silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof.

[0018] Two or more electrodes, such as a positive electrode 130 and a negative electrode 132, extend through the passivation film 120 and make contact to the film stack 112. The positive electrode 130 extends through the passivation film 120 and contacts the ITO layer 110. The negative electrode 132 extends through the passivation film 120, the ITO layer 110, the p-doped layer 108, the MQW layer 106, and into or in contact with the n-doped layer 104. An isolation layer 134 separates the side surface of the negative electrode 132 from the passivation film 120, the ITO layer 110, the p-doped layer 108, the MQW layer 106, and the n-doped layer 104. The isolation layer 134 can be a barrier layer and/or an electrically insulating layer so

to keep the negative electrode 132 physically and/or electrically isolated from the neighboring layers and materials of the film stack 112.

[0019] The sidewall portion 122 of the passivation film 120 has an average thickness t_1 and the top portion 124 of the passivation film 120 has an average thickness t_2 . As depicted in Figure 1, the sidewall portion 122 can have a consistent or substantially consistent thickness t_1 across the sidewall surface 114 of the film stack 112. In some examples, the sidewall portion 122 is thinner near or at the n-doped layer 104 and thicker near or at the ITO layer 110. In other examples, the sidewall portion 122 is thicker near or at the n-doped layer 104 and thinner near or at the ITO layer 110. The top portion 124 of the passivation film 120 can also have a consistent or inconsistent thickness t_2 across the upper surface of the ITO layer 110.

[0020] Each of the average thickness t_1 of the sidewall portion 122 and the average thickness t_2 of the top portion 124 is independently about 50 nm, about 65 nm, about 80 nm, about 90 nm, about 95 nm, about 100 nm, about 110 nm, about 115 nm, about 120 nm, about 130 nm, about 135 nm, about 140 nm, about 150 nm, about 165 nm, or about 180 nm to about 200 nm, about 220 nm, about 250 nm, about 300 nm, about 350 nm, about 400 nm, about 500 nm, about 600 nm, about 700 nm, about 800 nm, about 900 nm, about 1,000 nm, or thicker. For example, each of the average thickness t_1 of the sidewall portion 122 and the average thickness t_2 of the top portion 124 is independently about 50 nm to about 1,000 nm, about 50 nm to about 800 nm, about 50 nm to about 700 nm, about 50 nm to about 600 nm, about 50 nm to about 500 nm, about 50 nm to about 400 nm, about 50 nm to about 300 nm, about 50 nm to about 200 nm, about 50 nm to about 180 nm, about 50 nm to about 150 nm, about 50 nm to about 130 nm, about 50 nm to about 120 nm, about 50 nm to about 110 nm, about 50 nm to about 100 nm, about 50 nm to about 90 nm, about 50 nm to about 80 nm, about 50 nm to about 65 nm, about 100 nm to about 1,000 nm, about 100 nm to about 800 nm, about 100 nm to about 700 nm, about 100 nm to about 600 nm, about 100 nm to about 500 nm, about 100 nm to about 400 nm, about 100 nm to about 300 nm, about 100 nm to about 200 nm, about 100 nm to about 180 nm, about 100 nm to about 150 nm, about 100 nm to about 130 nm, about 100 nm to about 120 nm, about 100 nm to about 110 nm, about 200 nm to about 1,000 nm, about 200 nm to about 800 nm, about 200 nm to about 700 nm, about 200 nm to about 600 nm, about 200

nm to about 500 nm, about 200 nm to about 400 nm, about 200 nm to about 300 nm, or about 200 nm to about 250 nm.

[0021] In one or more examples, the average thickness t_1 of the sidewall portion 122 is about 70 nm to about 130 nm and the average thickness t_2 of the top portion 124 is about 100 nm to about 150 nm. In some examples, the average thickness t_1 of the sidewall portion 122 is about 80 nm to about 120 nm and the average thickness t_2 of the top portion 124 is about 110 nm to about 140 nm. In other examples, the average thickness t_1 of the sidewall portion 122 is about 90 nm to about 110 nm and the average thickness t_2 of the top portion 124 is about 115 nm to about 135 nm.

[0022] The passivation film 120 has a greater step coverage and also a greater conformality compared to passivation films deposited by conventional deposition methods. The step coverage is a ratio of an average thickness t_1 of the sidewall portion 122 of the passivation film 120 to an average thickness t_2 of the top portion 124 of the passivation film 122. As such, the step coverage is equal to t_1/t_2 .

[0023] In one or more embodiments, the passivation film 120 has a step coverage t_1/t_2 of about or greater than 70%, about or greater than 75%, about or greater than 78%, about or greater than 80%, or about or greater than 85%, such as about 88%, about 90%, about 92%, about 95%, about 96%, about 97%, about 98%, about 99%, or about 100%,. For example, the passivation film 120 has a step coverage t_1/t_2 of about or greater than 70% to about 100%, about or greater than 70% to about 98%, about or greater than 70% to about 96%, about or greater than 70% to about 95%, about or greater than 72% to about 95%, about or greater than 75% to about 95%, about or greater than 78% to about 95%, about or greater than 80% to about 95%, about or greater than 82% to about 95%, about or greater than 84% to about 95%, about or greater than 85% to about 95%, about or greater than 86% to about 95%, about or greater than 88% to about 95%, about or greater than 90% to about 95%, or about or greater than 92% to about 95%. In one or more examples, the passivation film 120 contains silicon oxide and has a step coverage t_1/t_2 of greater than 75%, such as about 78% to about 95%, about 80% to about 92%, or greater than 80%, such as about 82% to about 90%. In other examples, the passivation film 120 contains silicon nitride and has a step coverage t_1/t_2 of greater than 75%, about 76% to about 95%, about 78% to about 92%, about 80% to about 90%, or greater than 80%.

[0024] The passivation film 120 can be deposited or otherwise formed at a rate of about 1,500 Å/min, about 2,000 Å/min, about 2,200 Å/min, or about 2,500 Å/min to about 2,800 Å/min, about 3,000 Å/min, about 3,200 Å/min, about 3,300 Å/min, about 3,400 Å/min, about 3,500 Å/min, about 3,700 Å/min, about 3,850 Å/min, about 4,000 Å/min, about 4,200 Å/min, about 4,500 Å/min, about 5,000 Å/min, or greater. For example, the passivation film 120 can be deposited or otherwise formed at a rate of about 1,500 Å/min to about 5,000 Å/min, about 2,200 Å/min to about 5,000 Å/min, about 2,500 Å/min to about 5,000 Å/min, about 3,000 Å/min to about 5,000 Å/min, about 4,000 Å/min to about 5,000 Å/min, about 1,500 Å/min to about 4,000 Å/min, about 2,200 Å/min to about 4,000 Å/min, about 2,500 Å/min to about 4,000 Å/min, about 3,000 Å/min to about 4,000 Å/min, about 1,500 Å/min to about 3,500 Å/min, about 2,200 Å/min to about 3,500 Å/min, about 2,500 Å/min to about 3,500 Å/min, or about 3,000 Å/min to about 3,500 Å/min.

[0025] The passivation film is a silicon-containing passivation film and is deposited or otherwise formed by a pulsed PE-CVD process. The substrate containing one or more device structures is placed into and positioned with a processing chamber, such as a PE-CVD chamber. Exemplary devices and structures, such as microelectronic and display devices, can be or include an LED (e.g., micro-LED), an LCD, active matrix LCD (AMLCD), thin film transistors (TFT), low-temperature polysilicon (LTPS) transistors, low-temperature polysilicon oxide (LTPO) transistors, one or more metal oxide transistors (e.g., indium-gallium-zinc-oxide (IGZO) transistors), or the like. In one or more examples, the device structure is a micro-LED film stack which optionally can include an upper or top layer, such as an indium tin oxide (ITO) layer. In devices or structures having a top layer or surface containing ITO, the passivation film is deposited on and or over the ITO.

[0026] One or more silicon precursors and one or more reagent gases are flowed or otherwise introduced into the processing chamber containing the substrate. In some examples, the silicon precursor and the reagent gas can be independently and separately introduced into the processing chamber. The silicon precursor and the reagent gas can be combined in the processing chamber to form a deposition gas. In other examples, the silicon precursor and the reagent gas can be combined outside or while being introduced into the processing chamber, such that the deposition gas is flowed into the processing chamber.

[0027] The silicon precursor can be or include silane, disilane, trisilane, or any combination thereof. The reagent gas can be or include one or more oxidizing agents, one or more nitriding agents, or a mixture of one or more oxidizing agents and one or more nitriding agents. Exemplary oxidizing agents can be or include nitrous oxide, oxygen gas (O₂), ozone, water vapor, or any combination thereof. Exemplary nitriding agents can be or include ammonia, hydrazine, dinitrogen (N₂), nitric oxide, or any combination thereof. In one or more examples, the reagent gas is an oxidizing agent which contains nitrous oxide. In some examples, the reagent gas is a nitriding agent which contains ammonia. In other examples, the reagent gas contains a mixture of nitrous oxide and ammonia. The silicon precursor, the reagent gas, and/or the deposition gas can independently include one or more carrier gases and/or diluent gases. Exemplary carrier gases and/or diluent gases can be or include dinitrogen (N₂), argon, helium, neon, or any combination thereof.

[0028] The silicon precursor is introduced into the processing chamber at a flow rate of about 100 sccm, about 150 sccm, about 200 sccm, or about 250 sccm to about 300 sccm, about 350 sccm, about 400 sccm, about 500 sccm, about 650 sccm, or about 800 sccm. For example, the silicon precursor can have a flow rate of about 100 sccm to about 800 sccm, about 100 sccm to about 500 sccm, about 100 sccm to about 400 sccm, about 100 sccm to about 350 sccm, about 100 sccm to about 300 sccm, about 100 sccm to about 250 sccm, about 100 sccm to about 200 sccm, about 100 sccm to about 150 sccm, about 200 sccm to about 800 sccm, about 200 sccm to about 500 sccm, about 200 sccm to about 400 sccm, about 200 sccm to about 350 sccm, about 200 sccm to about 300 sccm, about 200 sccm to about 250 sccm, about 300 sccm to about 800 sccm, about 300 sccm to about 500 sccm, about 300 sccm to about 400 sccm, or about 300 sccm to about 350 sccm.

[0029] The reagent gas is introduced into the processing chamber at a flow rate of about 100 sccm, about 150 sccm, about 200 sccm, about 250 sccm, about 300 sccm, about 400 sccm, or about 500 sccm to about 800 sccm, about 1,000 sccm, about 1,500 sccm, about 2,000 sccm, about 3,000 sccm, about 5,000 sccm, about 8,000 sccm, or about 10,000 sccm. For example, the reagent gas can have a flow rate of about 100 sccm to about 10,000 sccm, about 100 sccm to about 5,000 sccm, about 100 sccm to about 2,500 sccm, about 100 sccm to about 1,000 sccm, about 100 sccm to about 800 sccm, about 100 sccm to about 500 sccm, about 100 sccm to about 400

sccm, about 100 sccm to about 350 sccm, about 100 sccm to about 300 sccm, about 100 sccm to about 250 sccm, about 100 sccm to about 200 sccm, about 100 sccm to about 150 sccm, about 500 sccm to about 10,000 sccm, about 500 sccm to about 5,000 sccm, about 500 sccm to about 2,500 sccm, about 500 sccm to about 1,000 sccm, about 500 sccm to about 800 sccm, about 500 sccm to about 600 sccm, about 1,000 sccm to about 10,000 sccm, about 1,000 sccm to about 7,000 sccm, about 1,000 sccm to about 5,000 sccm, about 1,000 sccm to about 3,000 sccm, about 1,000 sccm to about 2,000 sccm, or about 1,000 sccm to about 1,500 sccm.

[0030] The carrier gases or the diluent gases is introduced into the processing chamber at a flow rate of about 500 sccm, about 650 sccm, about 800 sccm, about 1,000 sccm, or about 1,500 sccm to about 2,000 sccm, about 3,000 sccm, about 4,000 sccm, about 5,000 sccm, about 5,500 sccm, about 6,500 sccm, about 8,000 sccm, or about 10,000 sccm. For example, the carrier gases or the diluent gases can have a flow rate of about 500 sccm to about 10,000 sccm, about 500 sccm to about 8,000 sccm, about 500 sccm to about 5,000 sccm, about 500 sccm to about 3,500 sccm, about 500 sccm to about 2,500 sccm, about 500 sccm to about 2,000 sccm, about 500 sccm to about 1,500 sccm, about 500 sccm to about 1,000 sccm, about 500 sccm to about 800 sccm, about 500 sccm to about 650 sccm, about 1,000 sccm to about 10,000 sccm, about 1,000 sccm to about 8,000 sccm, about 1,000 sccm to about 5,000 sccm, about 1,000 sccm to about 3,500 sccm, about 1,000 sccm to about 2,500 sccm, about 1,000 sccm to about 2,000 sccm, about 1,000 sccm to about 1,500 sccm, about 1,000 sccm to about 1,200 sccm, about 3,000 sccm to about 10,000 sccm, about 3,000 sccm to about 8,000 sccm, about 3,000 sccm to about 7,000 sccm, about 3,000 sccm to about 5,000 sccm, or about 3,000 sccm to about 3,500 sccm.

[0031] During the pulsed PE-CVD process, a plasma is ignited or otherwise generated within the processing chamber and one or more device structures disposed on the substrate are exposed to the deposition gas and the plasma. The flow of the deposition gas is maintained while an RF power is pulsed between an on-position and an off-position during the pulsed PE-CVD process. The passivation film is simultaneously deposited or otherwise formed on the sidewall surface and the top surface of the one or more device structures. For example, a sidewall portion of the passivation film is deposited on the sidewall surface of the micro-LED structure and a

top portion of the passivation film is deposited on the top surface of the micro-LED structure.

[0032] The radio frequency (RF) power, such as both the high frequency (HF) power and the low frequency (LF) power, is independently controlled to switch or pulse between "on" and "off" positions for generating the plasma during the pulsed PE-CVD process. Specifically, the HF power can be sequentially pulsed on and then pulsed off to generate a pulsing HF plasma and the LF power can be sequentially pulsed on and then pulsed off to generate a pulsing LF plasma. In one or more examples, the HF power and the LF power are synchronized to be pulsed on and pulsed off at the same time during the pulsed PE-CVD process. In other examples, the HF power and the LF power are not synchronized such that either the HF or LF power is on or off continuously while to the other HF or LF power is pulsed on and pulsed off during the pulsed PE-CVD process. The plasma excitation frequency for RF power can be at one, two, or more frequencies. In one or more examples, the plasma excitation frequencies are set at 13.56 KHz for the HF power and at 350 KHz for the LF power.

[0033] Each of the HF plasma and the LF plasma can independently be generated at a power of about 50 W, about 75 W, about 90 W, or about 100 W to about 120 W, about 150 W, about 175 W, about 200 W, about 250 W, about 300 W, about 400 W, or about 500 W. For example, each of the HF plasma and the LF plasma can independently be generated at a power of about 50 W to about 500 W, about 50 W to about 400 W, about 50 W to about 300 W, about 50 W to about 250 W, about 50 W to about 200 W, about 50 W to about 175 W, about 50 W to about 150 W, about 50 W to about 100 W, about 75 W to about 500 W, about 75 W to about 400 W, about 75 W to about 300 W, about 75 W to about 250 W, about 75 W to about 200 W, about 75 W to about 175 W, about 75 W to about 150 W, about 75 W to about 100 W, about 100 W to about 500 W, about 100 W to about 400 W, about 100 W to about 300 W, about 100 W to about 250 W, about 100 W to about 200 W, about 100 W to about 175 W, or about 100 W to about 150 W.

[0034] In one or more examples, the HF plasma is generated at a power of about 100 W to about 500 W and the LF plasma is generated at a power of about 50 W to about 150 W. In other examples, the HF plasma is generated at a power of about 150 W to about 300 W and the LF plasma is generated at a power of about 60 W to about

100 W. In one or more examples, the HF plasma is generated at a power of about 180 W to about 220 W and the LF plasma is generated at a power of about 75 W to about 90 W.

[0035] The substrate is exposed to the plasma and the precursors, the reagent gases, the process gases, and/or other gases are ignited by and/or exposed to the plasma when the RF power is at the on-position during the pulsed PE-CVD process. The HF plasma is generated when the HF power is at the on-position and the HF plasma is terminated when the HF power is at the off-position. Similarly, the LF plasma is generated when the LF power is at the on-position and the LF plasma is terminated when the LF power is at the off-position. Each of the HF power on-position, the HF power off-position, the LF power on-position, the LF power off-position can independently have a pulse time of about 0.1 milliseconds (ms), about 0.5 ms, about 1 ms, about 5 ms, about 10 ms, about 20 ms, about 35 ms, about 50 ms, about 80 ms, about 0.1 seconds (s), about 0.2 s, about 0.5 s, about 0.8 s, about 1 s, about 1.2 s, about 1.4 s, or about 1.5 s to about 1.6 s, about 1.8 s, about 2 s, about 2.2 s, about 2.5 s, about 2.8 s, about 3 s, about 3.5 s, about 4 s, about 5 s, about 6 s, about 8 s, or about 10 s. For example, each of the HF power on-position, the HF power off-position, the LF power on-position, the LF power off-position can independently have a pulse time of about 0.1 ms to about 10 s, about 0.5 ms to about 10 s, about 1 ms to about 10 s, about 5 ms to about 10 s, about 10 ms to about 10 s, about 20 ms to about 10 s, about 50 ms to about 10 s, about 80 ms to about 10 s, about 0.1 ms to about 1 s, about 0.5 ms to about 1 s, about 1 ms to about 1 s, about 5 ms to about 1 s, about 10 ms to about 1 s, about 20 ms to about 1 s, about 50 ms to about 1 s, about 80 ms to about 1 s, about 0.1 s to about 10 s, about 0.5 s to about 10 s, about 1 s to about 10 s, about 1.2 s to about 10 s, about 1.5 s to about 10 s, about 1.8 s to about 10 s, about 2 s to about 10 s, about 2.5 s to about 10 s, about 3 s to about 10 s, about 4 s to about 10 s, about 5 s to about 10 s, about 6 s to about 10 s, about 0.1 s to about 5 s, about 0.5 s to about 5 s, about 1 s to about 5 s, about 1.2 s to about 5 s, about 1.5 s to about 5 s, about 1.8 s to about 5 s, about 2 s to about 5 s, about 2.5 s to about 5 s, about 3 s to about 5 s, about 0.1 s to about 3 s, about 0.5 s to about 3 s, about 1 s to about 3 s, about 1.2 s to about 3 s, about 1.5 s to about 3 s, about 1.8 s to about 3 s, about 2 s to about 3 s, or about 2.5 s to about 3 s.

[0036] The substrate and/or the processing region of the processing chamber is heated to and/or maintained at a relatively low temperature while depositing the passivation film during the pulsed PE-CVD process. The temperature of the substrate and/or the processing region of the processing chamber can be less than 200°C, less than 190°C, or less than 180°C, such as about 20°C, about 25°C, about 30°C, about 40°C, about 50°C, or about 60°C to about 80°C, about 90°C, about 100°C, about 120°C, about 135°C, about 140°C, about 150°C, about 165°C, about 170°C, about 175°C, about 180°C, about 185°C, about 190°C, or about 195°C. For example, the temperature can be about 20°C to about 175°C, about 50°C to about 175°C, about 80°C to about 175°C, about 100°C to about 175°C, about 120°C to about 175°C, about 130°C to about 175°C, about 140°C to about 175°C, about 150°C to about 175°C, about 160°C to about 175°C, about 20°C to about 170°C, about 20°C to about 160°C, about 20°C to about 150°C, about 20°C to about 140°C, about 20°C to about 120°C, about 20°C to about 100°C, about 20°C to about 80°C, about 20°C to about 50°C, about 50°C to about 170°C, about 100°C to about 165°C, or about 140°C to about 160°C.

[0037] The processing region of the processing chamber is maintained at a pressure of less than 760 Torr while depositing the passivation film during the pulsed PE-CVD process. In some embodiments, the processing region of the processing chamber is maintained at a pressure of about 0.1 Torr, about 0.5 Torr, or about 1 Torr to about 1.5 Torr, about 2 Torr, about 2.5 Torr, about 2.7 Torr, about 3 Torr, about 3.2 Torr, about 5 Torr, about 10 Torr, about 50 Torr, or about 100 Torr.

Experimental Section

[0038] Example 1 – Silicon Oxide: A passivation film containing silicon oxide was deposited during the pulsed PE-CVD process with the following conditions: substrate was about 140°C to about 160°C; chamber pressure was about 2.8 Torr to about 3.2 Torr; the HF plasma had a power of about 180 W to about 220 W and the LF plasma had a power of about 80 W to about 100 W; the pulsing time for the HF power on-position was about 1.3 s to about 1.7 s, the HF power off-position was about 1.3 s to about 1.7 s, the LF power on-position was about 1.3 s to about 1.7 s, the LF power off-position was about 1.3 s to about 1.7 s; the flow rate of the silicon precursor (e.g., silane) was about 230 sccm to about 270 sccm; and the flow rate of the reagent gas

(e.g., nitrous oxide) was about 4,000 sccm to about 6,000 sccm. The passivation film containing silicon oxide was deposited to a thickness of about 1,100 Å to about 1,300 Å at a deposition rate of about 3,200 Å/min to about 3,800 Å/min; had a standard deviation (1σ , 5 mm EE) of about 0.3% to about 0.5%; had a refractive index (at 633 nm) of about 1.45 to about 1.48, and had a stress of about -30 MPa to about -36 MPa.

[0039] Example 2 – Silicon Nitride: A passivation film containing silicon nitride was deposited during the pulsed PE-CVD process with the following conditions: substrate was about 140°C to about 160°C; chamber pressure was about 2.5 Torr to about 3 Torr; the HF plasma had a power of about 180 W to about 220 W and the LF plasma had a power of about 60 W to about 90 W; the pulsing time for the HF power on-position was about 1.3 s to about 1.7 s, the HF power off-position was about 1.3 s to about 1.7 s, the LF power on-position was about 1.3 s to about 1.7 s, the LF power off-position was about 1.3 s to about 1.7 s; the flow rate of the silicon precursor (e.g., silane) was about 350 sccm to about 400 sccm; the flow rate of the reagent gas (e.g., ammonia) was about 150 sccm to about 200 sccm, and the flow rate of the carrier gas (e.g., dinitrogen) was about 5,000 sccm to about 9,000 sccm. The passivation film containing silicon nitride was deposited to a thickness of about 900 Å to about 1,100 Å at a deposition rate of about 2,200 Å/min to about 2,800 Å/min; had a standard deviation (1σ , 5 mm EE) of about 0.65% to about 0.85%; had a refractive index (at 633 nm) of about 1.80 to about 2.20, and had a stress of about -35 MPa to about -50 MPa.

[0040] Example 3 – Silicon Oxynitride: A passivation film containing silicon oxynitride was deposited during the pulsed PE-CVD process with the following conditions: substrate was about 140°C to about 160°C; chamber pressure was about 3.0 Torr to about 3.5 Torr; the HF plasma had a power of about 180 W to about 220 W and the LF plasma had a power of about 70 W to about 110 W; the pulsing time for the HF power on-position was about 1.3 s to about 1.7 s, the HF power off-position was about 1.3 s to about 1.7 s, the LF power on-position was about 1.3 s to about 1.7 s, the LF power off-position was about 1.3 s to about 1.7 s; the flow rate of the silicon precursor (e.g., silane) was about 375 sccm to about 430 sccm; the flow rate of the a first reagent gas (e.g., nitrous oxide) was about 100 sccm to about 200 sccm, the flow rate of a second reagent gas (e.g., ammonia) was about 400 sccm to about 600 sccm, and the flow rate of the carrier gas (e.g., dinitrogen) was about 4,000 sccm to about

7,000 sccm. The passivation film containing silicon oxynitride was deposited to a thickness of about 900 Å to about 1,200 Å at a deposition rate of about 3,000 Å/min to about 3,500 Å/min; had a standard deviation (1σ , 5 mm EE) of about 0.70% to about 0.90%; had a refractive index (at 633 nm) of about 1.62 to about 1.90, and had a stress of about -40 MPa to about -60 MPa.

[0041] Embodiments of the present disclosure further relate to any one or more of the following paragraphs 1-42:

[0042] 1. A method for depositing a silicon-containing passivation film on a micro-LED structure, comprising: generating a plasma within a processing chamber by an RF power; exposing the micro-LED structure disposed on a substrate within the processing chamber to a deposition gas comprising a silicon precursor and a reagent gas; maintaining a flow of the deposition gas while pulsing the RF power between an on-position and an off-position; and simultaneously depositing a passivation film on a sidewall surface and a top surface of the micro-LED structure, wherein: a sidewall portion of the passivation film is deposited on the sidewall surface of the micro-LED structure and a top portion of the passivation film is deposited on the top surface of the micro-LED structure; the passivation film has a step coverage of greater than 70%; and the step coverage is a ratio of an average thickness of the sidewall portion of the passivation film to an average thickness of the top portion of the passivation film.

[0043] 2. A method for depositing a silicon-containing passivation film on a micro-LED structure, comprising: introducing a silicon precursor and a reagent gas into a processing chamber containing a substrate; generating a plasma within the processing chamber by an RF power; exposing the micro-LED structure disposed on the substrate to a deposition gas comprising the silicon precursor and the reagent gas; maintaining a flow of the deposition gas while pulsing the RF power between an on-position and an off-position; and simultaneously depositing a passivation film on a sidewall surface and a top surface of the micro-LED structure, wherein: the passivation film comprises silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof; a sidewall portion of the passivation film is deposited on the sidewall surface of the micro-LED structure and a top portion of the passivation film is deposited on the top surface of the micro-LED structure; the passivation film has a step coverage of greater than 75%; the step coverage is a ratio of an average

thickness of the sidewall portion of the passivation film to an average thickness of the top portion of the passivation film; and each of the average thicknesses of the sidewall portion and the top portion is independently about 50 nm to about 700 nm.

[0044] 3. A micro-LED structure, comprising: a film stack disposed on a substrate, wherein the film stack comprises: a multiple quantum well (MQW) layer disposed between an n-doped layer and a p-doped layer; and an indium tin oxide layer disposed on the p-doped layer; and a passivation film disposed on a sidewall surface of the film stack and a top surface of the film stack, wherein: the passivation film comprises silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof; a sidewall portion of the passivation film is disposed on the sidewall surface of the micro-LED structure and a top portion of the passivation film is disposed on the top surface of the micro-LED structure; the passivation film has a step coverage of greater than 70%; the step coverage is a ratio of an average thickness of the sidewall portion of the passivation film to an average thickness of the top portion of the passivation film; and each of the average thicknesses of the sidewall portion and the top portion is independently about 50 nm to about 700 nm.

[0045] 4. The method and/or the micro-LED structure according to any one of paragraphs 1-3, wherein the passivation film comprises silicon oxide.

[0046] 5. The method and/or the micro-LED structure according to paragraph 4, wherein the step coverage of the passivation film is greater than 75%.

[0047] 6. The method and/or the micro-LED structure according to paragraph 4, wherein the step coverage of the passivation film is greater than 80%.

[0048] 7. The method and/or the micro-LED structure according to paragraph 4, wherein the step coverage of the passivation film is about 78% to about 95%.

[0049] 8. The method and/or the micro-LED structure according to paragraph 4, wherein the step coverage of the passivation film is about 80% to about 92%.

[0050] 9. The method and/or the micro-LED structure according to paragraph 4, wherein the step coverage of the passivation film is about 82% to about 90%.

[0051] 10. The method of method and/or the micro-LED structure according to paragraph 4-9, wherein each of the average thickness of the sidewall portion of the passivation film and the average thickness of the top portion of the passivation film is independently about 50 nm to about 700 nm.

[0052] 11. The method of method and/or the micro-LED structure according to paragraph 10, wherein the average thickness of the sidewall portion of the passivation film is about 70 nm to about 130 nm and the average thickness of the top portion of the passivation film is about 100 nm to about 150 nm.

[0053] 12. The method of method and/or the micro-LED structure according to paragraph 11, wherein the average thickness of the sidewall portion of the passivation film is about 80 nm to about 120 nm and the average thickness of the top portion of the passivation film is about 110 nm to about 140 nm.

[0054] 13. The method of method and/or the micro-LED structure according to paragraph 12, wherein the average thickness of the sidewall portion of the passivation film is about 90 nm to about 110 nm and the average thickness of the top portion of the passivation film is about 115 nm to about 135 nm.

[0055] 14. The method and/or the micro-LED structure according to any one of paragraphs 4-13, wherein the reagent gas comprises nitrous oxide.

[0056] 15. The method and/or the micro-LED structure according to any one of paragraphs 4-14, wherein the reagent gas comprises an oxidizing agent, and wherein the oxidizing agent comprises nitrous oxide, oxygen gas, ozone, water vapor, or any combination thereof.

[0057] 16. The method and/or the micro-LED structure according to any one of paragraphs 4-15, wherein the silicon precursor comprises silane, disilane, trisilane, or any combination thereof.

[0058] 17. The method and/or the micro-LED structure according to any one of paragraphs 1-3, wherein the passivation film comprises silicon nitride.

[0059] 18. The method of method and/or the micro-LED structure according to paragraph 17, wherein the step coverage of the passivation film is greater than 75%.

[0060] 19. The method of method and/or the micro-LED structure according to paragraph 17, wherein the step coverage of the passivation film is greater than 80%.

[0061] 20. The method of method and/or the micro-LED structure according to paragraph 17, wherein the step coverage of the passivation film is about 76% to about 95%.

[0062] 21. The method of method and/or the micro-LED structure according to paragraph 17, wherein the step coverage of the passivation film is about 78% to about 92%.

[0063] 22. The method of method and/or the micro-LED structure according to paragraph 17, wherein the step coverage of the passivation film is about 80% to about 90%.

[0064] 23. The method of method and/or the micro-LED structure according to any one of paragraphs 17-22, wherein each of the average thickness of the sidewall portion of the passivation film and the average thickness of the top portion of the passivation film is independently about 50 nm to about 700 nm.

[0065] 24. The method of method and/or the micro-LED structure according to paragraph 23, wherein the average thickness of the sidewall portion of the passivation film is about 50 nm to about 150 nm and the average thickness of the top portion of the passivation film is about 50 nm to about 150 nm.

[0066] 25. The method of method and/or the micro-LED structure according to paragraph 24, wherein the average thickness of the sidewall portion of the passivation film is about 55 nm to about 120 nm and the average thickness of the top portion of the passivation film is about 60 nm to about 100 nm.

[0067] 26. The method of method and/or the micro-LED structure according to paragraph 25, wherein the average thickness of the sidewall portion of the passivation film is about 60 nm to about 80 nm and the average thickness of the top portion of the passivation film is about 70 nm to about 90 nm.

[0068] 27. The method of method and/or the micro-LED structure according to any one of paragraphs 17-26, wherein the reagent gas comprises ammonia.

[0069] 28. The method of method and/or the micro-LED structure according to any one of paragraphs 17-27, wherein the reagent gas further comprises dinitrogen.

[0070] 29. The method of method and/or the micro-LED structure according to any one of paragraphs 17-28, wherein the reagent gas comprises a nitriding agent, and wherein the nitriding agent comprises ammonia, hydrazine, dinitrogen, nitric oxide, or any combination thereof.

[0071] 30. The method of method and/or the micro-LED structure according to any one of paragraphs 17-29, wherein the silicon precursor comprises silane, disilane, trisilane, or any combination thereof.

[0072] 31. The method and/or the micro-LED structure according to any one of paragraphs 1-30, wherein the micro-LED structure comprises a micro-LED film stack and the top surface of the micro-LED structure comprises an indium tin oxide (ITO) layer, and wherein the passivation film is deposited on the ITO layer.

[0073] 32. The method and/or the micro-LED structure according to any one of paragraphs 1-31, wherein the micro-LED film stack further comprises an n-doped layer, a multiple quantum well (MQW) layer, and a p-doped layer, wherein the MQW layer is disposed between the n-doped layer and the p-doped layer, and wherein the ITO layer is disposed on the p-doped layer.

[0074] 33. The method and/or the micro-LED structure according to any one of paragraphs 1-32, wherein the substrate comprises sapphire, quartz, glass, crystalline silicon, or a polymeric material.

[0075] 34. The method and/or the micro-LED structure according to any one of paragraphs 1-33, wherein the substrate is maintained at a temperature of less than 200°C while depositing the passivation film.

[0076] 35. The method and/or the micro-LED structure according to any one of paragraphs 1-34, wherein the substrate is maintained at a temperature of less than 180°C.

[0077] 36. The method and/or the micro-LED structure according to any one of paragraphs 1-35, wherein the substrate is maintained at a temperature of about 20°C to about 175°C.

[0078] 37. The method and/or the micro-LED structure according to any one of paragraphs 1-36, wherein the substrate is maintained at a temperature of about 50°C to about 170°C.

[0079] 38. The method and/or the micro-LED structure according to any one of paragraphs 1-37, wherein the substrate is maintained at a temperature of about 100°C to about 165°C.

[0080] 39. The method and/or the micro-LED structure according to any one of paragraphs 1-38, wherein the substrate is maintained at a temperature of about 140°C to about 160°C.

[0081] 40. The method and/or the micro-LED structure according to any one of paragraphs 1-39, wherein the passivation film comprises silicon oxide, wherein the step coverage is greater than 78%, and wherein the reagent gas comprises nitrous oxide.

[0082] 41. The method and/or the micro-LED structure according to any one of paragraphs 1-40, wherein the passivation film comprises silicon nitride, wherein the step coverage is greater than 80%, and wherein the reagent gas comprises ammonia.

[0083] 42. The method and/or the micro-LED structure according to any one of paragraphs 1-41, wherein the passivation film comprises silicon oxynitride.

[0084] While the foregoing is directed to embodiments of the disclosure, other and further embodiments may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow. All documents described herein are incorporated by reference herein, including any priority documents and/or testing procedures to the extent they are not inconsistent with this text. As is apparent from the foregoing general description and the specific embodiments, while forms of the present disclosure have been illustrated and described, various modifications can be made without departing from the spirit and scope of the present disclosure. Accordingly, it is not intended that the present

disclosure be limited thereby. Likewise, the term "comprising" is considered synonymous with the term "including" for purposes of United States law. Likewise, whenever a composition, an element, or a group of elements is preceded with the transitional phrase "comprising", it is understood that the same composition or group of elements with transitional phrases "consisting essentially of", "consisting of", "selected from the group of consisting of", or "is" preceding the recitation of the composition, element, or elements and vice versa, are contemplated.

[0085] Certain embodiments and features have been described using a set of numerical upper limits and a set of numerical lower limits. It should be appreciated that ranges including the combination of any two values, e.g., the combination of any lower value with any upper value, the combination of any two lower values, and/or the combination of any two upper values are contemplated unless otherwise indicated. Certain lower limits, upper limits and ranges appear in one or more claims below.

What is claimed is:

1. A method for depositing a silicon-containing passivation film on a micro-LED structure, comprising:
 - generating a plasma within a processing chamber by an RF power;
 - exposing the micro-LED structure disposed on a substrate within the processing chamber to a deposition gas comprising a silicon precursor and a reagent gas;
 - maintaining a flow of the deposition gas while pulsing the RF power between an on-position and an off-position; and
 - simultaneously depositing a passivation film on a sidewall surface and a top surface of the micro-LED structure, wherein:
 - a sidewall portion of the passivation film is deposited on the sidewall surface of the micro-LED structure and a top portion of the passivation film is deposited on the top surface of the micro-LED structure;
 - the passivation film has a step coverage of greater than 70%; and
 - the step coverage is a ratio of an average thickness of the sidewall portion of the passivation film to an average thickness of the top portion of the passivation film.
2. The method of claim 1, wherein the passivation film comprises silicon oxide.
3. The method of claim 2, wherein the step coverage of the passivation film is greater than 75%.
4. The method of claim 3, wherein the step coverage of the passivation film is about 78% to about 95%.
5. The method of claim 3, wherein each of the average thickness of the sidewall portion of the passivation film and the average thickness of the top portion of the passivation film is independently about 50 nm to about 700 nm.

6. The method of claim 3, wherein the average thickness of the sidewall portion of the passivation film is about 70 nm to about 130 nm and the average thickness of the top portion of the passivation film is about 100 nm to about 150 nm.
7. The method of claim 2, wherein the reagent gas comprises nitrous oxide.
8. The method of claim 1, wherein the passivation film comprises silicon nitride.
9. The method of claim 8, wherein the step coverage of the passivation film is greater than 75%.
10. The method of claim 9, wherein the step coverage of the passivation film is about 76% to about 95%.
11. The method of claim 9, wherein each of the average thickness of the sidewall portion of the passivation film and the average thickness of the top portion of the passivation film is independently about 50 nm to about 700 nm.
12. The method of claim 9, wherein the average thickness of the sidewall portion of the passivation film is about 50 nm to about 150 nm and the average thickness of the top portion of the passivation film is about 50 nm to about 150 nm.
13. The method of claim 8, wherein the reagent gas comprises ammonia.
14. The method of claim 1, wherein the micro-LED structure comprises a micro-LED film stack and the top surface of the micro-LED structure comprises an indium tin oxide (ITO) layer, and wherein the passivation film is deposited on the ITO layer.
15. The method of claim 14, wherein the micro-LED film stack further comprises an n-doped layer, a multiple quantum well (MQW) layer, and a p-doped layer, wherein the MQW layer is disposed between the n-doped layer and the p-doped layer, and wherein the ITO layer is disposed on the p-doped layer.

16. A method for depositing a silicon-containing passivation film on a micro-LED structure, comprising:

introducing a silicon precursor and a reagent gas into a processing chamber containing a substrate;

generating a plasma within the processing chamber by an RF power;

exposing the micro-LED structure disposed on the substrate to a deposition gas comprising the silicon precursor and the reagent gas;

maintaining a flow of the deposition gas while pulsing the RF power between an on-position and an off-position; and

simultaneously depositing a passivation film on a sidewall surface and a top surface of the micro-LED structure, wherein:

the passivation film comprises silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof;

a sidewall portion of the passivation film is deposited on the sidewall surface of the micro-LED structure and a top portion of the passivation film is deposited on the top surface of the micro-LED structure;

the passivation film has a step coverage of greater than 75%;

the step coverage is a ratio of an average thickness of the sidewall portion of the passivation film to an average thickness of the top portion of the passivation film; and

each of the average thicknesses of the sidewall portion and the top portion is independently about 50 nm to about 700 nm.

17. The method of claim 16, wherein the passivation film comprises silicon oxide, wherein the step coverage is greater than 78%, and wherein the reagent gas comprises nitrous oxide.

18. The method of claim 16, wherein the passivation film comprises silicon nitride, wherein the step coverage is greater than 80%, and wherein the reagent gas comprises ammonia.

19. The method of claim 16, wherein the passivation film comprises silicon oxynitride.

20. A micro-LED structure, comprising:
- a film stack disposed on a substrate, wherein the film stack comprises:
 - a multiple quantum well (MQW) layer disposed between an n-doped layer and a p-doped layer; and
 - an indium tin oxide layer disposed on the p-doped layer; and
 - a passivation film disposed on a sidewall surface and a top surface of the film stack, wherein:
 - the passivation film comprises silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof;
 - a sidewall portion of the passivation film is disposed on the sidewall surface of the micro-LED structure and a top portion of the passivation film is disposed on the top surface of the micro-LED structure;
 - the passivation film has a step coverage of greater than 70%;
 - the step coverage is a ratio of an average thickness of the sidewall portion of the passivation film to an average thickness of the top portion of the passivation film; and
 - each of the average thicknesses of the sidewall portion and the top portion is independently about 50 nm to about 700 nm.

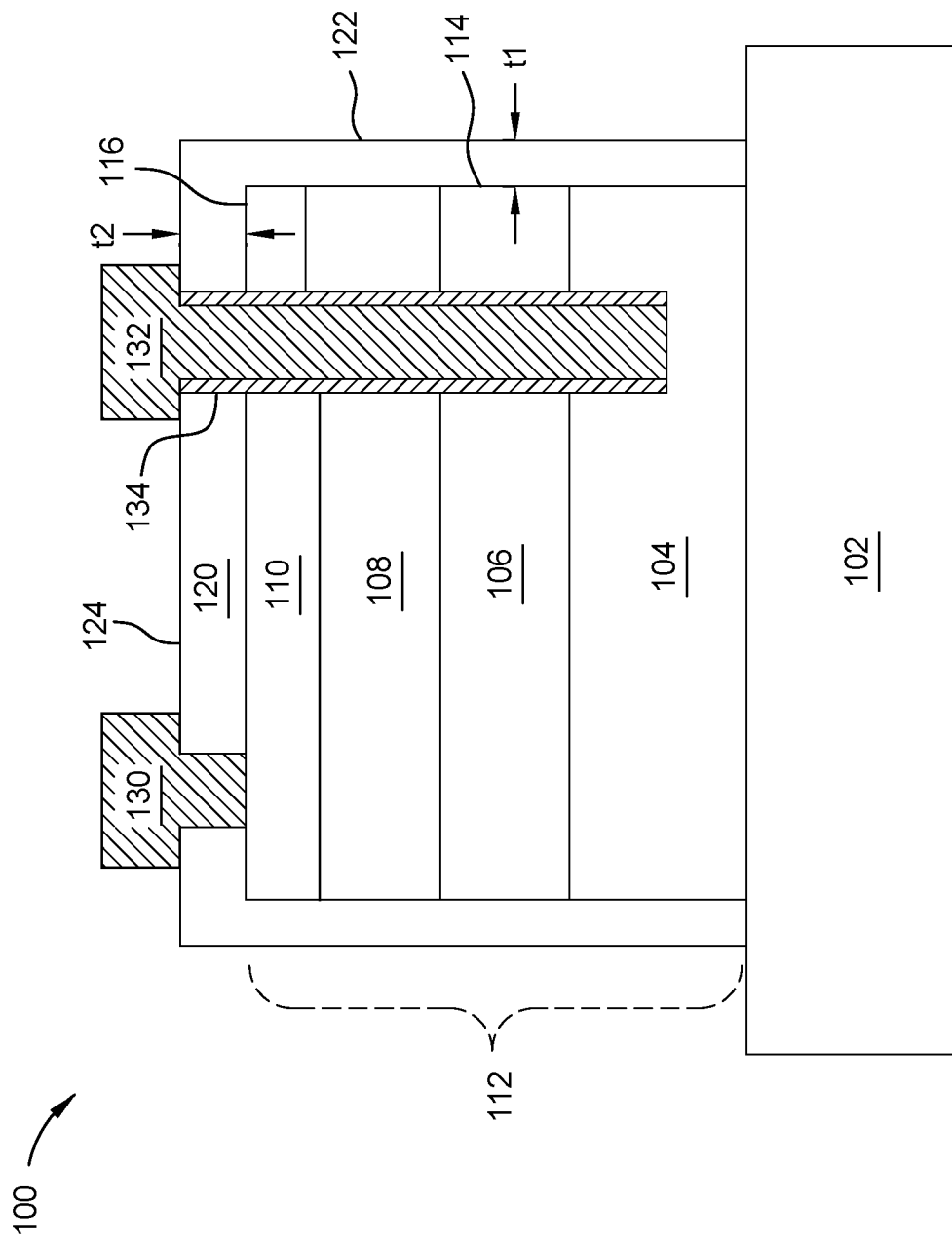


FIG. 1

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2020/119907

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/033(2006.01)i; C23C 16/34(2006.01)i; C23C 16/513(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L; C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, CNTXT, CNKI, SIPOABS, DWPI, WOTXT, USTXT, EPTXT, STN, ISI Web of Science, Elsevier Science Direct; APPLIED MATERIALS, INC.; FANG Jun, CHI Hyo-In, HO Dustin W.; LED OR light emitting diode?, plasma-enhanced chemical vapor deposition OR PE-CVD OR PECVD, passivat+ film, indium tin oxide OR ITO, step coverage?, side wall?, multiple quantum well OR MQW, silicon OR +silane

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010184302 A1 (ASM. JAPAN K.K.) 22 July 2010 (2010-07-22) Description paragraphs 20-34, 42, 82	1-20
X	US 6449132 B1 (SEAGATE TECHNOLOGY LLC) 10 September 2002 (2002-09-10) Column 2, lines 43 to Column 3, lines 59	1-20
X	US 6809043 B1 (ADVANCED MICRO DEVICES INC.) 26 October 2004 (2004-10-26) Column 3, lines 1-58	1-20
X	CN 103177952 A (INST. MICROELECTRONICS CHINESE ACAD. SCI.) 26 June 2013 (2013-06-26) Description paragraphs 20-32	1-20
A	CN 103117338 A (CHINESE ACAD. SCI. SEMICONDUCTORS INST.) 22 May 2013 (2013-05-22) Claims 1-6	1-20
A	CN 105355763 A (HANGZHOU SILAN AZURE CO., LTD.) 24 February 2016 (2016-02-24) the whole document	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance
 “E” earlier application or patent but published on or after the international filing date
 “L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
 “O” document referring to an oral disclosure, use, exhibition or other means
 “P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
 “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
 “Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
 “&” document member of the same patent family

Date of the actual completion of the international search

22 June 2021

Date of mailing of the international search report

12 July 2021

Name and mailing address of the ISA/CN

National Intellectual Property Administration, PRC
 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
 100088
 China

Authorized officer

YANG, Kun

Facsimile No. (86-10)62019451

Telephone No. (86-10)53962711

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2020/119907**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

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