(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 May 2017 (04.05.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/074385 A1

(51) International Patent Classification:
H04B 10/69 (2013.01) *H04B 10/2507* (2013.01)

(21) International Application Number:
PCT/US2015/058044

(22) International Filing Date:
29 October 2015 (29.10.2015)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **HEWLETT-PACKARD ENTERPRISE** [US/US]; 11445 Compaq Center Drive W., Houston, Texas 77070 (US).

(72) Inventors: **ZHU, Kehan**; 1501 Page Mill Rd., Palo Alto, California 94304-1100 (US). **LI, Cheng**; 1501 Page Mill Rd., Palo Alto, California 94304-1100 (US). **FIORENTINO, Marco**; 1501 Page Mill Rd., Palo Alto, California 94304-1100 (US).

(74) Agents: **LIOU, Lisa** et al.; Hewlett-Packard Company, Intellectual Property Administration, 3404 E. Harmony Road, Mail Stop 35, Fort Collins, Colorado 80528-9599 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: RECEIVERS WITH AUTOMATIC GAIN CONTROL

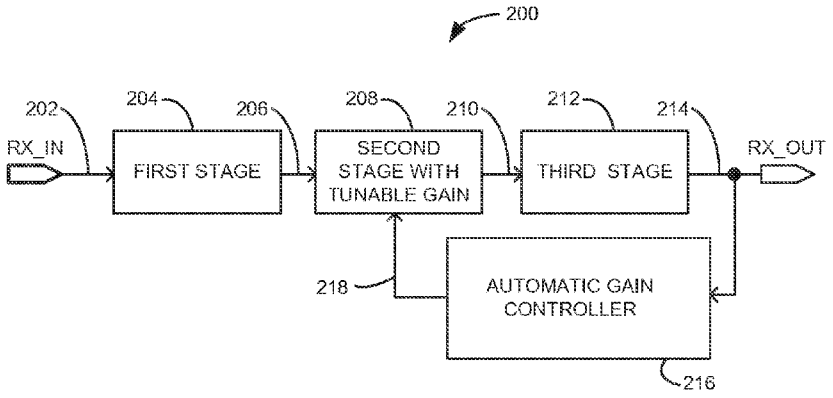


Fig. 2

(57) Abstract: One example of a receiver includes a first stage, a second stage, a third stage, and an automatic gain controller. The first stage amplifies an input signal to provide a first signal. The second stage amplifies or attenuates the first signal to provide a second signal based on a tunable gain of the second stage. The tunable gain is adjusted in response to a differential signal. The third stage amplifies the second signal to provide an output signal. The automatic gain controller provides the differential signal based on a comparison between a peak voltage of the output signal and the sum of a common mode voltage of the output signal and an offset voltage.

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RECEIVERS WITH AUTOMATIC GAIN CONTROL

Statement of United States Government Interest

[0001] This invention was made with United States government support under Contract No. H98230-14-3-0011. The United States government has certain rights in the invention.

Background

[0002] Data center networks may use fiber optics to communicate data between devices, such as servers and switches. An optical transmitter is used to convert an electrical signal to an optical signal for transmission through a fiber optic cable. An optical receiver is used to convert a received optical signal back into an electrical signal.

Brief Description of the Drawings

[0003] Figure 1 is a schematic diagram illustrating one example of a system.
[0004] Figure 2 is a block diagram illustrating one example of an optical receiver.
[0005] Figure 3 is a block diagram illustrating another example of an optical receiver.
[0006] Figure 4 is a schematic diagram illustrating one example of an optical receiver.

[0007] Figure 5 illustrates one example of an eye diagram for an input signal and an eye diagram for an output signal.

[0008] Figure 6 illustrates one example of a PAM-4 eye diagram for an output signal at a 32 GBd rate.

[0009] Figure 7 is a flow diagram illustrating one example of a method for receiving an optical signal.

Detailed Description

[0010] In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific examples in which the disclosure may be practiced. It is to be understood that other examples may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present disclosure is defined by the appended claims. It is to be understood that features of the various examples described herein may be combined, in part or whole, with each other, unless specifically noted otherwise.

[0011] Four-level pulse-amplitude modulation (PAM-4) is one of the enablers for next generation high-speed data center networking. Compared to non-return-to-zero (NRZ) modulation, the signal-to-noise ratio (SNR) of PAM-4 is intrinsically at least 9 dB less than the SNR of NRZ with the same amplitude. When receiving an optical PAM-4 signal, the gain of the transimpedance amplifier (TIA) used to convert the optical PAM-4 signal into an electrical PAM-4 signal should be automatically adjusted to accommodate different optical power levels of the PAM-4 signal. If the different optical power levels of the PAM-4 signal are not accommodated, the output PAM-4 signal will have amplitude distortion as may be observed from an eye diagram of the output PAM-4 signal.

[0012] In addition, a variable gain control method used in an NRZ TIA in which a metal-oxide-semiconductor field-effect transistor (MOSFET) is used as a variable resistor will result in level dependent rise-time and fall-time effect during

level transitions when processing a PAM-4 signal. Therefore, as may be observed from an eye diagram of the output PAM-4 signal, the output PAM-4 signal will have a time skew effect due to the MOSFET nonlinearity at large signal swing. This time skew will result in timing issues for slicer circuits following the TIA at higher speeds (e.g., 32 GBd).

[0013] Accordingly, the following description describes examples of an optical receiver (e.g., a TIA) for receiving a PAM-4 optical signal. The TIA includes an automatic gain control circuit to ensure proper functioning of the TIA for a wide dynamic range of optical intensity, while maintaining a constant amplitude, distortion-free and time skew-free PAM-4 electrical output signal. The TIA includes three amplification stages in which the second stage includes a tunable gain. The gain of the second stage is controlled by the output of a fully differential comparator, which compares a peak voltage of the output signal to a sum of a common mode voltage of the output signal and an offset voltage.

[0014] Figure 1 is a schematic diagram illustrating one example of a system 100. System 100 includes an optical detector 106, a parasitic capacitance as indicated by capacitor 110, and an optical receiver 114. In one example, optical detector 106 is a photodiode or other suitable photodetector. The cathode of optical detector 106 is electrically coupled to a supply voltage (VPD) 102. The anode of optical detector 106 is electrically coupled to the input of optical receiver 114 and one terminal of capacitor 110 through a node 108. The other terminal of capacitor 110 is electrically coupled to a common or ground 112. The output of optical receiver 114 is electrically coupled to a node 116.

[0015] Optical detector 106 receives an optical signal as indicated at 104. In one example, optical signal 104 is a PAM-4 optical signal. Optical detector 106 converts optical signal 104 to a current signal to provide a receiver input signal (RX_IN) on node 108. Optical receiver 114 is a transimpedance amplifier that converts the current signal RX_IN on node 108 to a voltage signal to provide a receiver output signal (RX_OUT) on node 116. Due to the configuration of optical receiver 114, RX_OUT has no amplitude distortion and no time skew for a wide dynamic range of RX_IN.

[0016] Figure 2 is a block diagram illustrating one example of an optical receiver 200. In one example, optical receiver 200 provides optical receiver 114 previously described and illustrated with reference to Figure 1. Optical receiver 200 includes a first stage 204, a second stage 208, a third stage 212, and an automatic gain controller 216. The input of first stage 204 receives the input signal RX_IN through a signal path 202. The output of first stage 204 is electrically coupled to a first input of second stage 208 through a signal path 206. The output of second stage 208 is electrically coupled to the input of third stage 212 through a signal path 210. The output of third stage 212 is electrically coupled to the input of automatic gain controller 216 and provides the output signal RX_OUT through a signal path 214. The output of automatic gain controller 216 is electrically coupled to a second input of second stage 208 through a signal path 218.

[0017] First stage 204 is a transimpedance amplifier stage. First stage 204 receives the input signal RX_IN, which is a current signal, and amplifies RX_IN to provide an amplified voltage signal (i.e., a first signal) on signal path 206. In one example, the gain of first stage 204 is greater than the gain of second stage 208 and the gain of third stage 212 to improve the noise performance of optical receiver 200.

[0018] Second stage 208 is an isolating stage and includes a tunable gain. Second stage 208 receives the first signal on signal path 206 and amplifies or attenuates the first signal to provide a second signal on signal path 210. Third stage 212 receives the second signal on signal path 210 and amplifies the second signal to provide the output signal RX_OUT on signal path 214. Automatic gain controller 216 receives RX_OUT on signal path 214 to provide a differential signal on signal path 218 for adjusting the gain of second stage 208. Automatic gain controller 216 provides the differential signal based on a comparison between a sensed peak voltage of RX_OUT and the sum of a common mode voltage of RX_OUT and an offset voltage. The offset voltage is a predefined voltage that may be selected to set the amplitude of RX_OUT.

[0019] In response to the peak voltage of RX_OUT being greater than the sum of the common mode voltage of RX_OUT and the offset voltage, automatic gain

controller 216 adjusts the gain of second stage 208 such that second stage 208 attenuates of the first signal to provide the second signal. In response to the peak voltage of RX_OUT being less than the sum of the common mode voltage of RX_OUT and the offset voltage, automatic gain controller 216 adjusts the gain of second stage 208 such that second stage 208 amplifies the first signal to provide the second signal.

[0020] Figure 3 is a block diagram illustrating another example of an optical receiver 300. Optical receiver 300 is similar to optical receiver 200 previously described and illustrated with reference to Figure 2, except that automatic gain controller 216 includes a peak detector 302 and a fully differential comparator 306. The input of peak detector 302 receives the output signal RX_OUT through signal path 214. The output of peak detector 302 is electrically coupled to the input of fully differential comparator 306 through a signal path 304. The output of fully differential comparator 306 is electrically coupled to the second input of second stage 208 through signal path 218.

[0021] Peak detector 302 senses the peak voltage of RX_OUT, senses the common mode voltage of RX_OUT, and provides the offset voltage. Peak detector 302 also sums the sensed common mode voltage of RX_OUT and the offset voltage. Fully differential comparator 306 compares the sensed peak voltage of RX_OUT with the sum of the common mode voltage of RX_OUT and the offset voltage to provide the differential signal on signal path 218.

[0022] Figure 4 is a schematic diagram illustrating one example of an optical receiver 400. In one example, optical receiver 400 provides optical receiver 300 previously described and illustrated with reference to Figure 3. Optical receiver 400 includes a first stage, a second stage, a third stage, a peak detector 437, and a fully differential comparator 466.

[0023] The first stage of optical receiver 400 includes transistors 408 and 410 and a resistor 412. In one example, transistor 408 is a p-channel MOSFET and transistor 410 is an n-channel MOSFET. The gates of transistors 408 and 410 and one terminal of resistor 412 are electrically coupled to a node 406. The source of transistor 408 is electrically coupled to a supply voltage (VDD) 402. The drain of transistor 408 is electrically coupled to the other terminal of resistor

412 and the drain of transistor 410 through a node 414. The source of transistor 410 is electrically coupled to a common or ground 404.

[0024] The second stage of optical receiver 400 includes transistors 416, 418, 420a and 420b, 422, 424a and 424b, and 426. In one example, transistors 416, 420a and 420b, and 422 are p-channel MOSFETs and transistors 418, 424a and 424b, and 426 are n-channel MOSFETs. In this example, transistors 420a and 420b are a stacked device providing a two finger transistor generally described herein as transistor 420. Transistors 424a and 424b are a stacked device providing a two finger transistor generally described herein as transistor 424. In other examples, transistors 420 and 424 may have another suitable number of fingers. The number of fingers of each transistor 420 and 424 and/or the length of each transistor 420 and 424 may be selected to set the effective resistance of each transistor 420 and 424 and thus leave a sufficient resistor tuning range for transistors 422 and 426 as well as maintain the bandwidth of the second stage..

[0025] Transistors 416 and 418 are arranged in an inverter configuration. The gates of transistors 416 and 418 are electrically coupled to node 414. The drain of transistor 416 and the drain of transistor 418 are electrically coupled to a node 428. Transistor 422 is electrically coupled in parallel with transistors 420a and 420b. The gates of transistors 420a and 420b are electrically coupled to common or ground 404. The gate of transistor 422 is electrically coupled to a node 468. The source of transistor 420b and the source of transistor 422 are electrically coupled to supply voltage 402. The drain of transistor 420b is electrically coupled to the source of transistor 420a. The drain of transistor 420a is electrically coupled to the source of transistor 416 and the drain of transistor 422.

[0026] Transistor 426 is electrically coupled in parallel with transistors 424a and 424b. The gates of transistors 424a and 424b are electrically coupled to supply voltage 402. The gate of transistor 426 is electrically coupled to a node 470. The source of transistor 424b and the source of transistor 426 are electrically coupled to common or ground 404. The drain of transistor 424b is electrically coupled to the source of transistor 424a. The drain of transistor 424a is

electrically coupled to the source of transistor 418 and the drain of transistor 426.

[0027] The third stage of optical receiver 400 includes transistors 430 and 432 and a resistor 434. In one example, transistor 430 is a p-channel MOSFET and transistor 432 is an n-channel MOSFET. The gates of transistors 430 and 432 and one terminal of resistor 434 are electrically coupled to node 428. The source of transistor 430 is electrically coupled to supply voltage 402. The drain of transistor 430 is electrically coupled to the other terminal of resistor 434 and the drain of transistor 432 through a node 436. The source of transistor 432 is electrically coupled to common or ground 404.

[0028] Peak detector 437 includes transistors 438 and 452, capacitors 442, 450, and 456, current sources 444, 464, and 458, and resistors 446 and 460. In one example, transistors 438 and 452 are n-channel MOSFETs. The current (Iss+Ios) of current source 458 is equal to the sum of the current (Iss) of current source 444 and the current (Ios) of current source 464. The gate of transistor 438 is electrically coupled to node 436. The drain of transistor 438 is electrically coupled to supply voltage 402. The source of transistor 438 is electrically coupled to the non-inverting input of fully differential comparator 466, one terminal of capacitor 442, and one terminal of current source 444 through node 440. The other terminal of current source 444 and the other terminal of capacitor 442 are electrically coupled to common or ground 404.

[0029] One terminal of current source 464 is electrically coupled to supply voltage 402. The other terminal of current source 464 is electrically coupled to the inverting input of fully differential comparator 466 and one terminal of resistor 460 through a node 462. The non-inverting output of fully differential comparator 466 is electrically coupled to node 468. The inverting output of fully differential comparator 466 is electrically coupled to node 470. The other terminal of resistor 460 is electrically coupled to one terminal of current source 458, one terminal of capacitor 456, and the source of transistor 452 through a node 454. The other terminal of capacitor 456 and the other terminal of current source 458 are electrically coupled to common or ground 404. The drain of transistor 452 is electrically coupled to supply voltage 402. The gate of

transistor 452 is electrically coupled to one terminal of capacitor 450 and one terminal of resistor 446 through a node 448. The other terminal of capacitor 450 is electrically coupled to common or ground 404. The other terminal of resistor 446 is electrically coupled to node 436.

[0030] The first stage of optical receiver 400 including transistors 408 and 410 and resistor 412 receives the input signal RX_IN on node 406 to provide a first signal on node 414. The gain of the first stage is set by the resistance (RF1) of resistor 412. The first stage is a transimpedance amplifier stage that converts RX_IN, which is a current signal, to a voltage signal to provide the first signal on node 414.

[0031] The second stage of optical receiver 400 is an isolating stage with a tunable gain. The second stage receives the first signal on node 414 to provide a second signal on node 428. The gain of the second stage is controlled by the differential gain control signal (GCTRL and GCTRLb) on nodes 468 and 470, respectively. Transistors 420 and 424 are always on. With transistors 422 and 426 in the linear region due to GCTRL and GCTRLb, respectively, transistors 422 and 426 act as variable resistors and the second stage amplifies or attenuates the first signal on node 414 to provide the second signal on node 428. As GCTRL increases and GCTRLb decreases, the attenuation of the second stage increases.

[0032] The effective transconductance (G_m) of the second stage is given by:

$$G_m(V_c) = \frac{g_m}{1 + g_m(R_{stack} \| R_c(V_c))}$$

where:

g_m is the transconductance of inverting transistors 416 and 418;

R_{stack} is the effective resistance of stacked transistors 420 and 424; and

$R_c(V_c)$ is the voltage controlled resistor provided by transistors 422 and 426.

[0033] The third stage of optical receiver 400 including transistors 430 and 432 and resistor 434 receives the second signal on node 428 to provide the output

signal RX_OUT on node 436. The gain of the third stage is set by the resistance (RF2) of resistor 434 and the transconductance of transistors 430 and 432.

[0034] Peak detector 437 senses the peak voltage of RX_OUT, senses the common mode voltage of RX_OUT, and sets the offset voltage. The peak voltage of RX_OUT is sensed by the circuit including transistor 438, current source 444 and capacitor 442. The sensed peak voltage of RX_OUT is provided on node 440 at the non-inverting input of fully differential comparator 466. The common mode voltage of RX_OUT is sensed by the circuit including resistor 446 and capacitor 450. Resistor 446 and 450 form a low pass filter such that the common mode voltage (VCM) of RX_OUT is provided on node 448. VCM (minus the threshold voltage of transistor 452) is provided on node 454. The offset voltage is set by the current (Ios) of current source 464 and the resistance (Ros) of resistor 460. The common mode voltage and the offset voltage are summed on node 462 at the inverting input of fully differential comparator 466.

[0035] Fully differential comparator 466 receives the sensed peak voltage at the non-inverting input on node 440 and the sum of the common mode voltage and the offset voltage at the inverting input on node 462. Fully differential comparator 466 compares the sensed peak voltage to the sum of the common mode voltage and the offset voltage to provide the differential signal including GCTRL on node 468 and GCTRLb on node 470. In response to the sensed peak voltage being less than the sum of the common mode voltage and the offset voltage, fully differential comparator 466 outputs GCTRL and GCTRLb such that transistors 422 and 426 are turned on more, respectively, and the second stage amplifies the first signal to provide the second signal. In response to the sensed peak voltage being greater than the sum of the common mode voltage and the offset voltage, fully differential comparator 466 outputs GCTRL and GCTRLb such that transistors 422 and 426 are turned on less, respectively, and the second stage attenuates the first signal to provide the second signal.

[0036] Figure 5 illustrates one example of an eye diagram 500 for RX_IN and an eye diagram 510 for RX_OUT for optical receiver 400 previously described and

illustrated with reference to Figure 4. In this example, RX_IN is a PAM-4 signal and thus eye diagram 500 includes a first eye 502, a second eye 504, and a third eye 506. Second eye 504 is above third eye 506, and first eye 502 is above second eye 504. Eye diagram 510 of RX_OUT includes a first eye 512, a second eye 514, and a third eye 516 corresponding to first eye 502, second eye 504, and third eye 506 of eye diagram 500, respectively. Second eye 514 is above first eye 512, and third eye 516 is above second eye 514. As illustrated by eye diagram 500 and eye diagram 510, RX_IN is inverted by optical receiver 400 to provide RX_OUT. The common mode voltage (VCM) of eye diagram 510 is indicated at 518 and the offset voltage (IosRos) of eye diagram 510 is indicated at 520. Accordingly, the amplitude of RX_OUT may be adjusted by adjusting the offset voltage.

[0037] Figure 6 illustrates one example of a PAM-4 eye diagram 600 for RX_OUT at a 32 GBd rate for optical receiver 400 previously described and illustrated with reference to Figure 4. Eye diagram 600 indicates time in picoseconds on x-axis 602 and RX_OUT in millivolts on y-axis 604. As illustrated by eye diagram 600, RX_OUT has no amplitude distortion and no time skew when RX_IN is large such that the second stage of optical receiver 400 is attenuating.

[0038] Figure 7 is a flow diagram illustrating one example of a method 700 for receiving an optical signal. At 702, method 700 includes detecting an optical signal to provide an input signal. In one example, detecting the optical signal comprises detecting a PAM-4 optical signal. At 704, method 700 includes amplifying the input signal to provide a first signal. At 706, method 700 includes amplifying or attenuating the first signal based on a tunable gain to provide a second signal. At 708, method 700 includes amplifying the second signal to provide an output signal. At 710, method 700 includes sensing a peak voltage of the output signal. At 712, method 700 includes sensing a common mode voltage of the output signal.

[0039] At 714, method 700 includes comparing the peak voltage to a sum of the common mode voltage and an offset voltage to provide a differential signal based on the comparison. At 716, method 700 includes setting the tunable gain

based on the differential signal. In one example, amplifying or attenuating the first signal comprises attenuating the first signal in response to the peak voltage being greater than the sum of the common mode voltage and the offset voltage such that the output signal is free of amplitude distortion and time skew. In one example, setting the tunable gain comprises adjusting a first transistor in the linear region as a variable resistor and a second transistor in the linear region as a variable resistor based on the differential signal, respectively. In another example, amplifying or attenuating the first signal comprises amplifying the first signal in response to the peak voltage being less than the sum of the common mode voltage and the offset voltage.

[0040] Although specific examples have been illustrated and described herein, a variety of alternate and/or equivalent implementations may be substituted for the specific examples shown and described without departing from the scope of the present disclosure. This application is intended to cover any adaptations or variations of the specific examples discussed herein. Therefore, it is intended that this disclosure be limited only by the claims and the equivalents thereof.

CLAIMS

1. A receiver comprising:

a first stage to amplify an input signal to provide a first signal;

a second stage to amplify or attenuate the first signal to provide a second signal based on a tunable gain of the second stage, the tunable gain adjusted in response to a differential signal;

a third stage to amplify the second signal to provide an output signal; and

an automatic gain controller to provide the differential signal based on a comparison between a peak voltage of the output signal and the sum of a common mode voltage of the output signal and an offset voltage.

2. The receiver of claim 1, wherein the automatic gain controller comprises:

a peak detector to sense the peak voltage of the output signal, sense the common mode voltage of the output signal, and provide the offset voltage; and

a fully differential comparator to compare the sensed peak voltage of the output signal with the sum of the common mode voltage of the output signal and the offset voltage to provide the differential signal.

3. The receiver of claim 1, wherein the second stage comprises an always on first transistor in parallel with a second transistor and an always on third transistor in parallel with a fourth transistor, the second transistor and the fourth transistor controlled by the differential signal, respectively, to adjust the gain of the second stage.

4. The receiver of claim 1, further comprising:

an optical detector to detect an optical signal to provide the input signal.

5. The receiver of claim 4, wherein the optical signal comprises a PAM-4 signal.

6. A receiver comprising:

a first stage to amplify an input signal to provide a first signal;

a second stage to amplify or attenuate the first signal to provide a second signal based on a tunable gain of the second stage;

a third stage to amplify the second signal to provide an output signal;

a peak detector to sense a peak voltage of the output signal, to sense a common mode voltage of the output signal, and to provide an offset voltage; and

a fully differential comparator to adjust the gain of the second stage based on a comparison between the sensed peak voltage and the sum of the common mode voltage and the offset voltage.

7. The receiver of claim 6, wherein the second stage comprises:

an isolator comprising a first transistor and a second transistor in an inverter configuration;

an always on third transistor electrically coupled in series with a drain-source path of the first transistor;

an always on fourth transistor electrically coupled in series with a drain-source path of the second transistor;

a fifth transistor electrically coupled in parallel with the third transistor; and

a sixth transistor electrically coupled in parallel with the fourth transistor,

wherein the fifth transistor and the sixth transistor are controlled by outputs of the fully differential comparator, respectively.

8. The receiver of claim 7, wherein the third transistor comprises a stacked device to set an effective resistance of the third transistor, and

wherein the fourth transistor comprises a stacked device to set an effective resistance of the fourth transistor.

9. The receiver of claim 6, wherein the input signal comprises a current signal and the first signal comprises a voltage signal.

10. The receiver of claim 6, wherein the input signal comprises a PAM-4 signal.

11. A method for receiving an optical signal, the method comprising:

detecting an optical signal to provide an input signal;

amplifying the input signal to provide a first signal;

amplifying or attenuating the first signal based on a tunable gain to provide a second signal;

amplifying the second signal to provide an output signal;

sensing a peak voltage of the output signal;

sensing a common mode voltage of the output signal;

comparing the peak voltage to a sum of the common mode voltage and an offset voltage to provide a differential signal based on the comparison; and

setting the tunable gain based on the differential signal.

12. The method of claim 11, wherein detecting the optical signal comprises detecting a PAM-4 optical signal.

13. The method of claim 12, wherein amplifying or attenuating the first signal comprises attenuating the first signal in response to the peak voltage being greater than the sum of the common mode voltage and the offset voltage such that the output signal is free of amplitude distortion and time skew.

14. The method of claim 11, wherein setting the tunable gain comprises adjusting a first transistor in the linear region as a variable resistor and a second transistor in the linear region as a variable resistor based on the differential signal, respectively.

15. The method of claim 11, wherein amplifying or attenuating the first signal comprises amplifying the first signal in response to the peak voltage being less than the sum of the common mode voltage and the offset voltage.

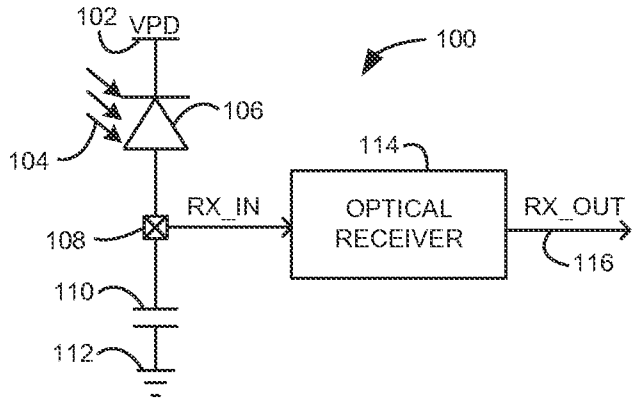

102
VPD
100
106
104
114
RX_IN
OPTICAL
RECEIVER
RX_OUT
108
116
110
112

Fig. 1

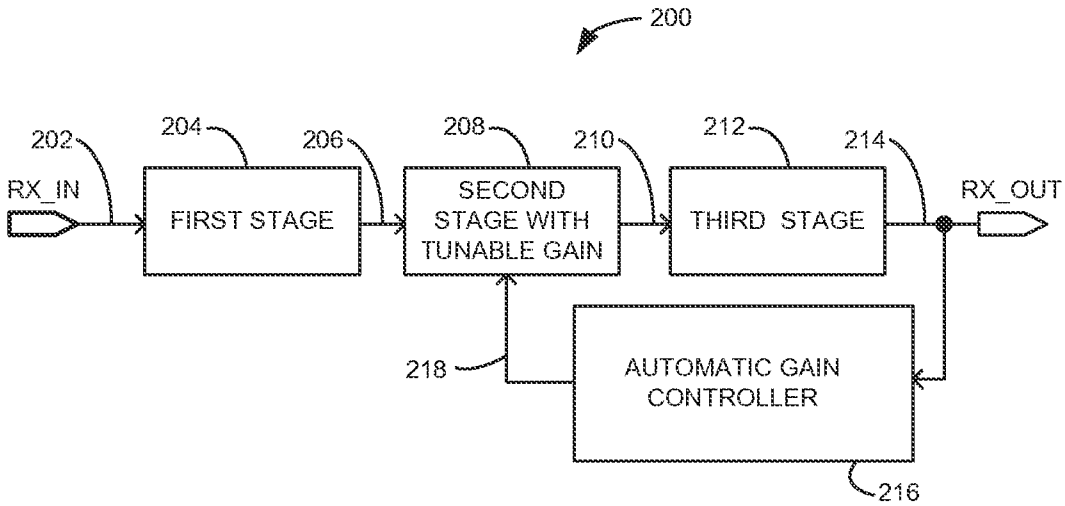

200
202
204
206
208
210
212
214
RX_IN
FIRST STAGE
SECOND
STAGE WITH
TUNABLE GAIN
THIRD STAGE
RX_OUT
218
AUTOMATIC GAIN
CONTROLLER
216

Fig. 2

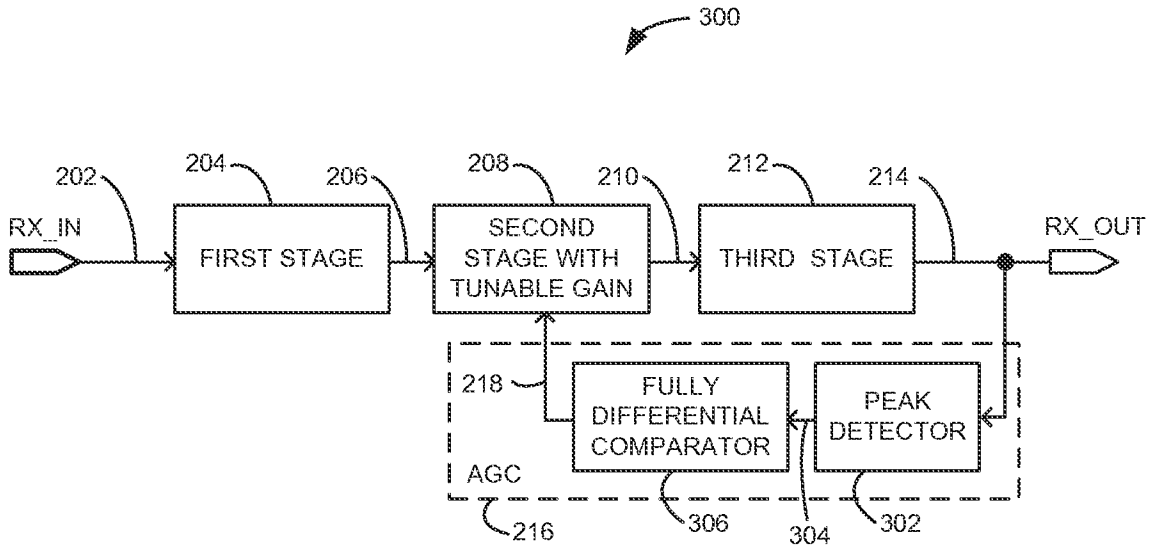

300
202
204
206
208
210
212
214
RX_IN
FIRST STAGE
SECOND STAGE WITH TUNABLE GAIN
THIRD STAGE
RX_OUT
218
FULLY DIFFERENTIAL COMPARATOR
PEAK DETECTOR
AGC
216
306
304
302

Fig. 3

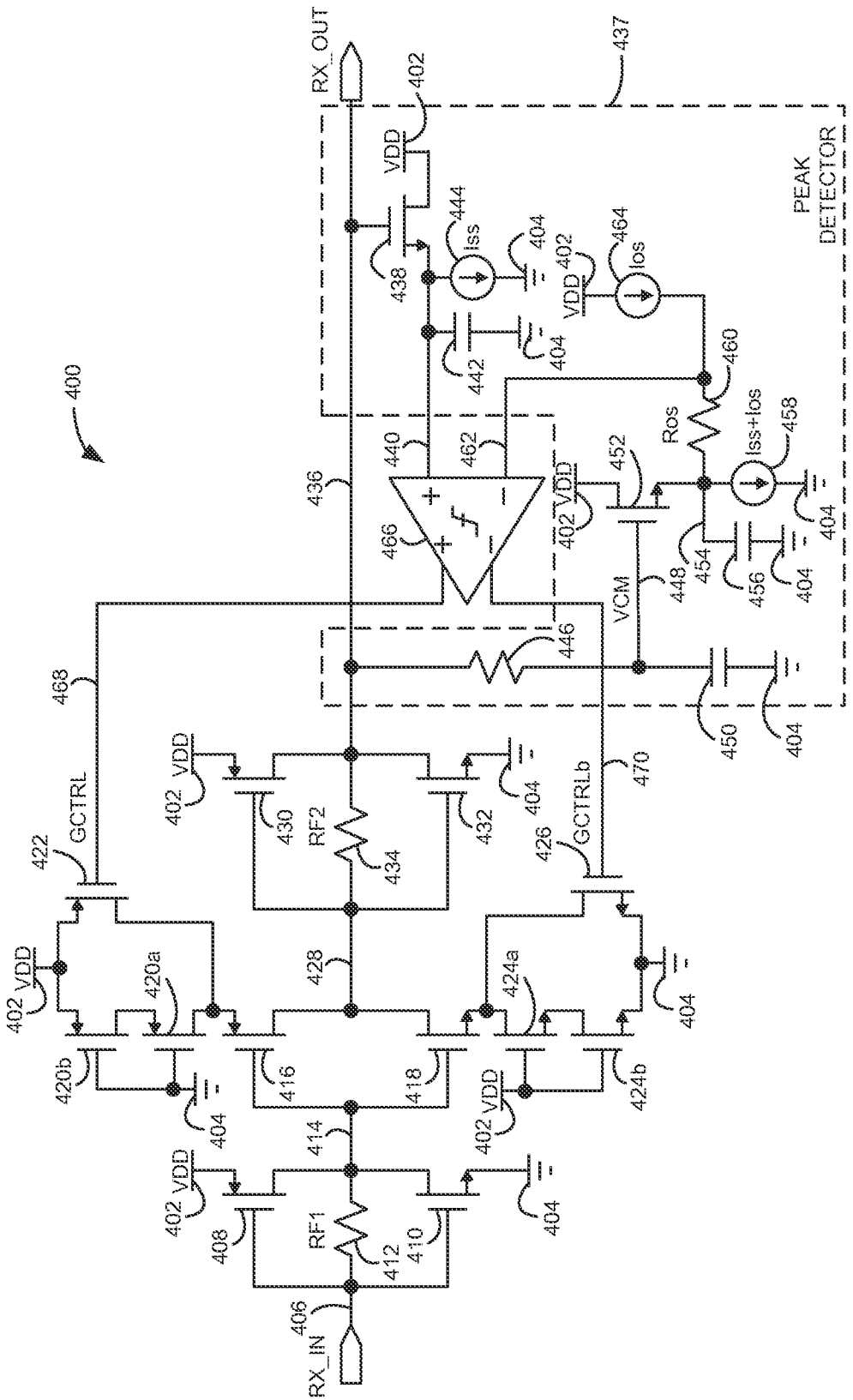

400
RX_OUT
RX_IN
406
437
PEAK DETECTOR
VDD
402
404
GCTRL
GCTRLb
422
426
RF1
RF2
408
410
412
414
428
430
432
434
416
418
420a
420b
424a
424b
436
438
440
442
444
446
448
450
452
454
456
458
460
462
464
466
468
470
Iss
Ios
Iss+Ios
Ros
VCM
f

Fig. 4

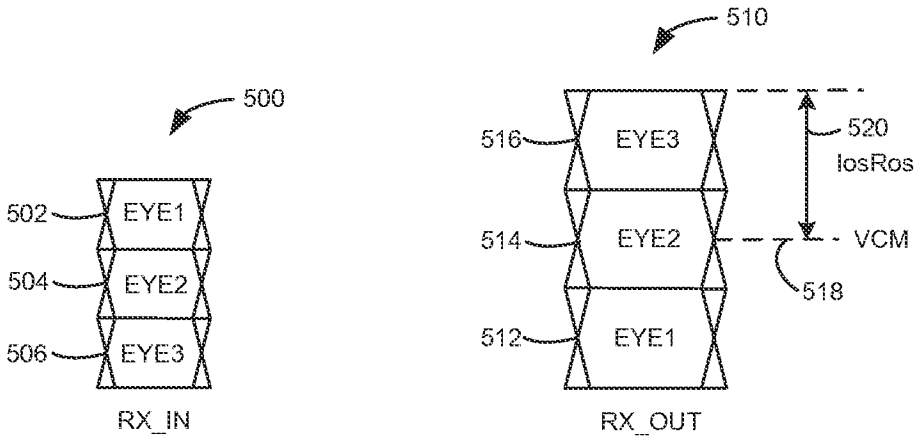

500
502
EYE1
504
EYE2
506
EYE3
RX_IN
510
516
EYE3
514
EYE2
512
EYE1
520
IosRos
VCM
518
RX_OUT

Fig. 5

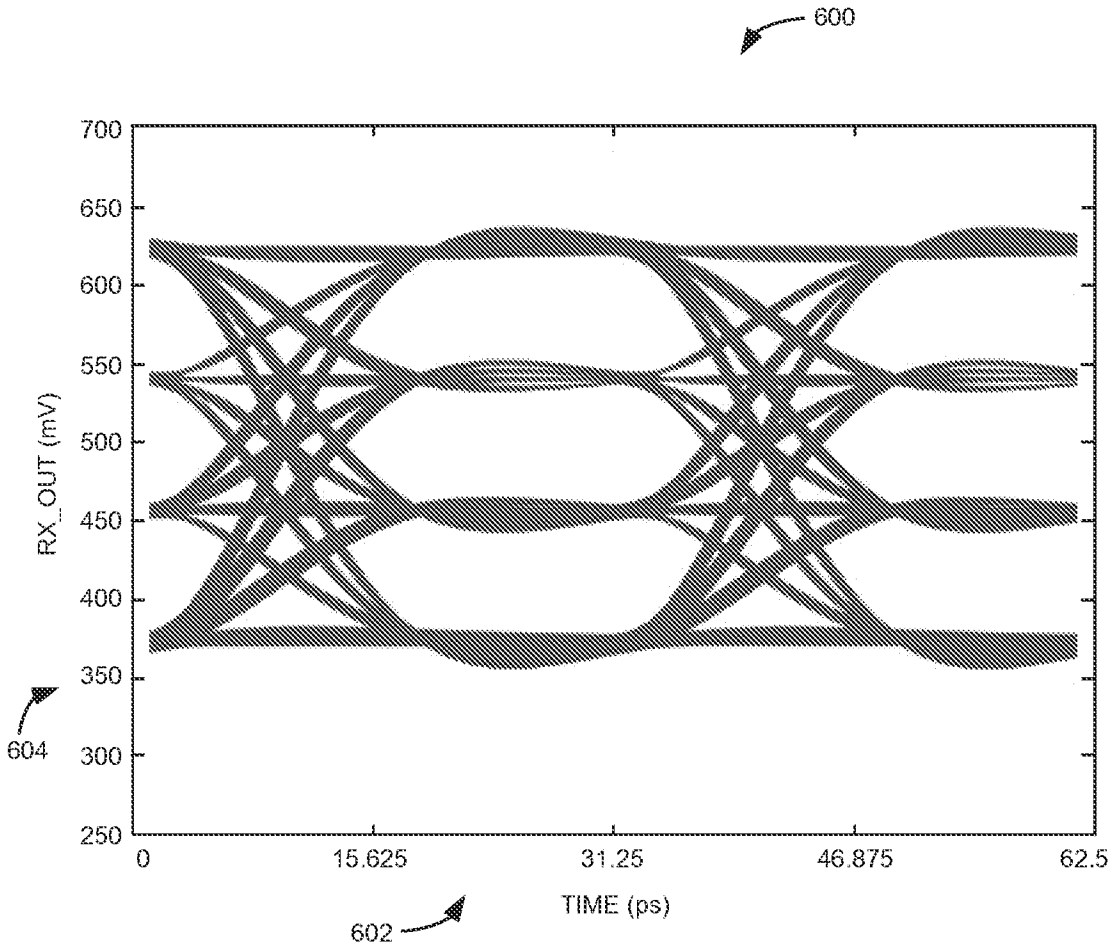

600
700
650
600
550
500
450
400
350
300
250
RX_OUT (mV)
604
0
15.625
31.25
46.875
62.5
TIME (ps)
602

Fig. 6

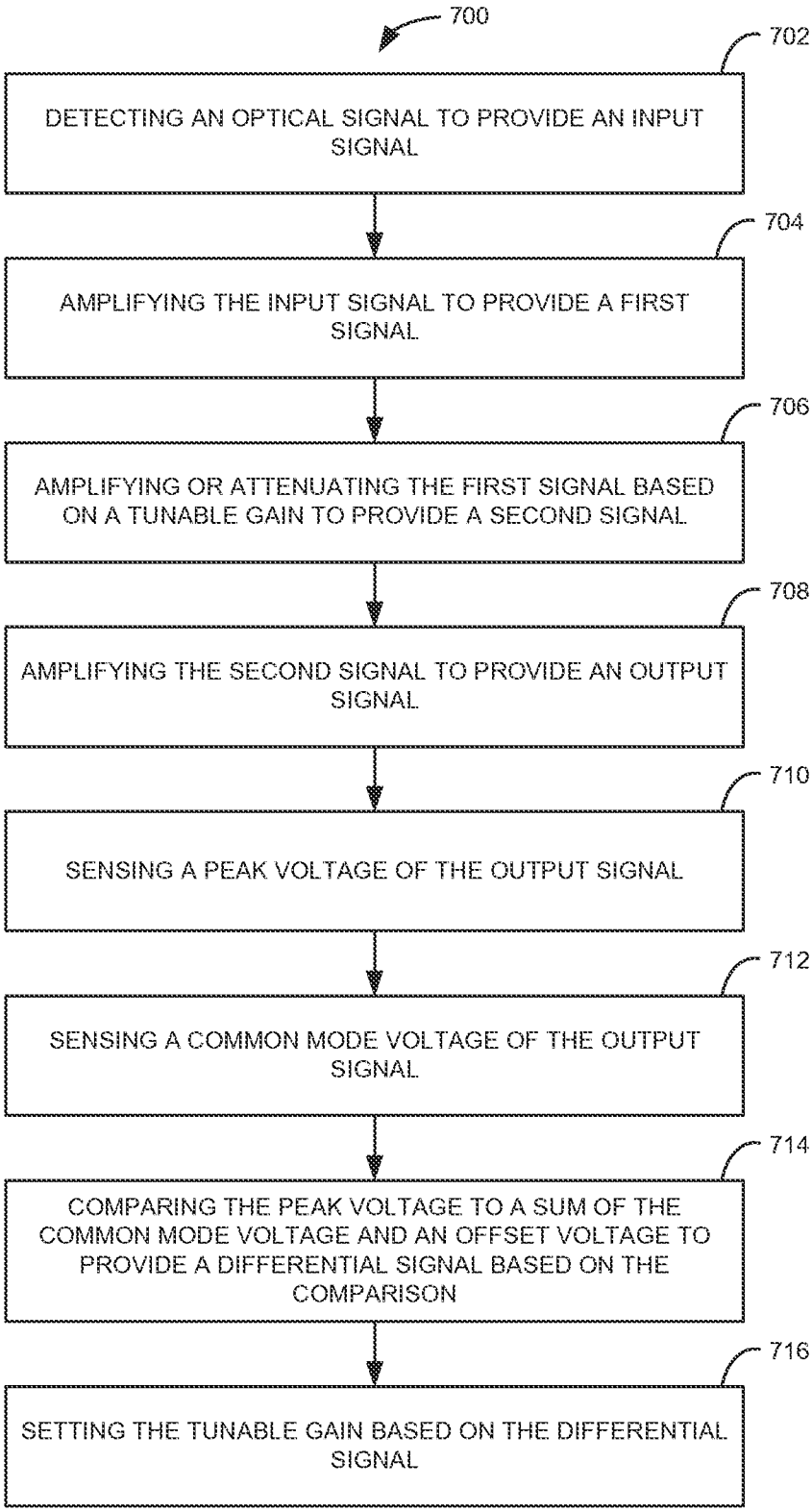

700
702
DETECTING AN OPTICAL SIGNAL TO PROVIDE AN INPUT SIGNAL
704
AMPLIFYING THE INPUT SIGNAL TO PROVIDE A FIRST SIGNAL
706
AMPLIFYING OR ATTENUATING THE FIRST SIGNAL BASED ON A TUNABLE GAIN TO PROVIDE A SECOND SIGNAL
708
AMPLIFYING THE SECOND SIGNAL TO PROVIDE AN OUTPUT SIGNAL
710
SENSING A PEAK VOLTAGE OF THE OUTPUT SIGNAL
712
SENSING A COMMON MODE VOLTAGE OF THE OUTPUT SIGNAL
714
COMPARING THE PEAK VOLTAGE TO A SUM OF THE COMMON MODE VOLTAGE AND AN OFFSET VOLTAGE TO PROVIDE A DIFFERENTIAL SIGNAL BASED ON THE COMPARISON
716
SETTING THE TUNABLE GAIN BASED ON THE DIFFERENTIAL SIGNAL

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/058044

A. CLASSIFICATION OF SUBJECT MATTER

H04B 10/69(2013.01)i, H04B 10/2507(2013.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B 10/69; H03G 3/30; H03F 3/16; H04B 10/516; H04B 10/61; H03F 1/34; H03F 3/45; H04B 10/60; H04B 10/2575; H04B 10/2507

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: tunable gain, differential signal, peak voltage, common mode voltage, offset voltage

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0306760 A1 (TEXAS INSTRUMENTS DEUTSCHLAND GMBH) 16 October 2014 See paragraphs [0015]-[0026]; claims 1, 3; and figure 1.	1-15
A	US 2014-0334832 A1 (LUXTERA, INC.) 13 November 2014 See paragraphs [0040]-[0048]; and figure 3.	1-15
A	US 2010-0283543 A1 (KRISHNA SHIVARAM et al.) 11 November 2010 See paragraphs [0037]-[0060]; and figures 3-4.	1-15
A	US 2010-0073083 A1 (SEHAT SUTARDJA) 25 March 2010 See paragraphs [0106]-[0111]; and figures 7-8.	1-15
A	JP 05239868 B2 (NEC CORP.) 17 July 2013 See paragraphs [0024]-[0026]; and figure 4.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 July 2016 (26.07.2016)	**26 July 2016 (26.07.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
HAN, JOONG SUB
Telephone No. +82-42-481-3578

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/058044

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