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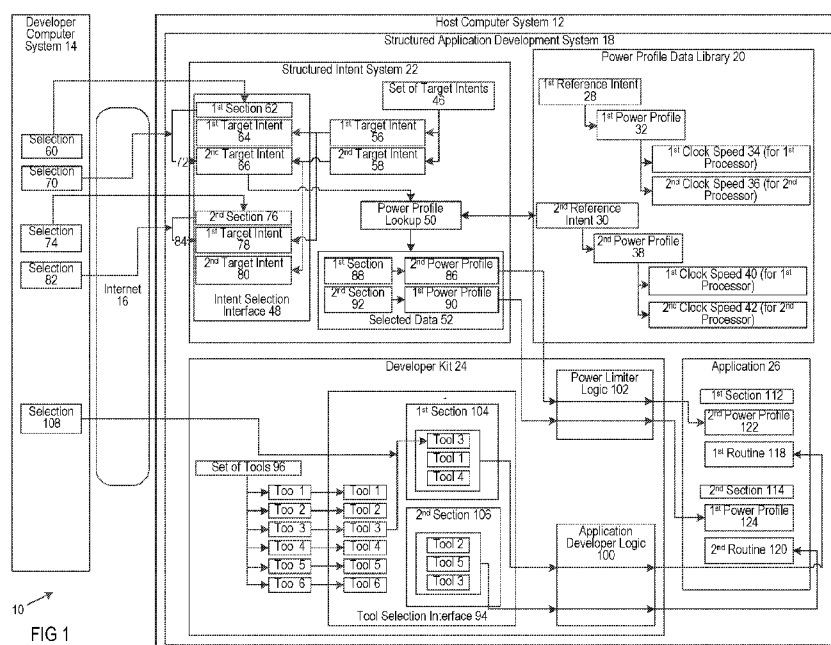


FIG 1

(57) Abstract: A power profile library includes a plurality of power profiles with each power profile having a plurality of maximum clock speeds for respective processors. The maximum clock speeds of each power profile are selected to limit a maximum amount of heat per unit time generated by the processors in combination. A developer computer system selects sections of an eventual application for a consumer device and a target intent for each section. A power profile lookup uses the target intents to determine a power profile for each section.

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TARGET INTENT-BASED CLOCK SPEED DETERMINATION AND ADJUSTMENT TO LIMIT TOTAL HEAT GENERATED BY MULTIPLE PROCESSORS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. Provisional Patent Application No. 62/802,140, filed on February 6, 2019, all of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1). Field of the Invention

[0002] This invention relates to structured application development system.

2). Discussion of Related Art

[0003] Consumer devices such as personal computers, smart phones, stereoscopic viewers, mixed reality viewers, etc. have a storage medium for storing an application and one or more processors that execute routines of the application. Such applications include operating systems and other applications such as games, browsers, etc. that perform a multitude of tasks.

[0004] Multi-core processor chips include more than one processor core. These processor cores may, for example, include a central processing unit (CPU), a graphic processing unit (GPU), vector processing, etc. When an application developer develops an application for running on multiple processors, the developer programs clock speeds for the various

processors.

[0005] Each processor generates an amount of heat per unit time that increases as its clock speed goes up. A multi-processor chip can normally dispense of all the heat of one processor running at 100% of its maximum clock speed. However, when all the processors run at 100% of their maximum clock speed, a multi-core processor chip may not be able to dispense of all the heat that is generated by all the processors, which may cause damage to the circuitry of the processors of the multi-core processor chip. Specifications may exist for clock speeds of a multi-core processor chip that detail how the clock speeds should be limited to limit the maximum amount of heat that is generated by all of the processors per unit time. The danger exists that a developer may ignore the specifications, which will result in damage to the multi-core processor chip.

SUMMARY OF THE INVENTION

[0006] According to one aspect of the invention, a host computer system is provided that includes a host computer processor, a computer-readable medium connected to the host computer processor, and a set of instructions on the computer-readable medium, the set of instructions being readable by the host computer processor and including a structured application development system having a power profile data library on the computer-readable medium that includes a first reference intent a first power profile associated with the first reference intent and having a respective first maximum clock speed for a first processor and a respective second maximum clock speed for a second processor, a second reference intent, and a second power profile associated with the second reference intent and having a respective first maximum clock speed for the first processor and a respective second maximum clock speed for the second processor, the first maximum clock speed of the first power profile being different from the first maximum clock speed for the second power profile.

[0007] The invention also provides a method of operating a host computer system including storing a power profile data library on a computer-readable medium, the power profile data library including a first reference intent, a first power profile associated with the first reference intent and having a respective first maximum clock speed for a first processor and a respective second maximum clock speed for a second processor, a second reference intent, and a second power profile associated with the second reference intent and having a respective first maximum clock speed for the first processor and a respective second maximum clock speed for the second processor, the first maximum clock speed of the first power profile being different from the first maximum clock speed for the second power

profile.

[0008] The invention further provides a consumer device that includes a multi-core processor chip having a body and a plurality of processors on the body, a computer-readable medium connected to the processors, and an application on the computer-readable medium, the application having a first section, the first section having, a first routine that is executable by the processors, and a first power profile having a respective maximum clock speed for each one of the processors, and a second section, the second section having a second routine that is executable by the processors, and a second power profile having a respective maximum clock speed for each one of the processors so that at least one of the processors has a maximum clock speed that changes from the first section to the second section, wherein the processors jointly generate a first amount of heat per unit time during the first section and a second amount of heat during the second section and the second amount of heat is less than 10% different than the first amount of heat.

[0009] The invention further provides a method of operating a consumer device that includes storing an application on the computer-readable medium connected to a plurality of processors on a body of a multi-core processor chip, the application having first and second sections, executing the first section with the processors, the first section having, a first routine that is executable by the processors, and a first power profile having a respective maximum clock speed for each one of the processors, and executing the second section with the processors, the second section having, a second routine that is executable by the processors, and a second power profile having a respective maximum clock speed for each one of the processors so that at least one of the processors has a maximum clock speed that changes from the first section to the second section, wherein the processors jointly generate

a first amount of heat per unit time during the first section and a second amount of heat during the second section and the second amount of heat is less than 10% different than the first amount of heat.

[0010] The invention further provides a consumer device that includes first and second processors a computer-readable medium connected to the processors, and an application on the computer-readable medium, the application having a first section, the first section having a first routine that is executable by the first and second processors, and a first power profile, the first power profile having first and second maximum clock speeds for the first and second processors, and a second section, the second section having, a second routine that is executable by the first and second processors, and a second power profile, the second power profile having first and second maximum clock speeds for the first and second processors, the first maximum clock speed of the first power profile being different from the first maximum clock speed for the second power profile and the second maximum clock speed of the first power profile be different from the second maximum clock speed for the second power profile.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The invention is further described by way of example with reference to the accompanying drawings, wherein:

[0012] Figure 1 is a block diagram showing a network environment, according to an embodiment of the invention having a host computer system and a developer computer system that are connected to one another over a network in the form of the Internet;

[0013] Figure 2 is a block diagram similar to Figure 1 showing a download interface;

[0014] Figure 3 is a block diagram of the developer computer system and a consumer device;

[0015] Figure 4 is block diagram illustrating functioning of an application on the consumer device;

[0016] Figure 5 is a block diagram illustrating further functioning of the application on the consumer device;

[0017] Figures 6A, 6B and 6C are graphs showing power curves of three different processors;

[0018] Figures 7A, 7B and 7C are graphs showing three different power profiles;

[0019] Figures 8A, 8B and 8C are graphs illustrating heat generated by the power profiles in Figures 7A, 7B and 7C respectively; and

[0020] Figure 9 is a block diagram of a machine in the form of a computer system forming part of the network environment.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Figure 1 of the accompanying drawings illustrates a network environment 10 that includes a host computer system 12 and a developer computer system 14 that are connected to one another over a network in the form of the Internet 16, according to an embodiment of the invention. A majority of data and logic resides on the host computer system 12 and the developer computer system 14 is given access to certain components on the host computer system 12 over the Internet 16 with only a browser application residing on the developer computer system 14. In another embodiment, all of the data and functionality may reside on the developer computer system 14, thus eliminating the need for the host computer system 12 – the developer computer system 14 effectively becomes the host computer system. It is, however, preferred that certain controls reside on the host computer system 12 and outside the reach of a developer at the developer computer system 14. A further embodiment may include certain data and functionality on the host computer system 12, in particular such data and functionality that should be under the control of the host computer system 12, while a remainder of the data and functionality may reside on the developer computer system 14.

[0022] The host computer system 12 includes a structured application development system 18. The structured application development system 18 initially resides on a storage medium of the host computer system 12. Components of the structured application development system 18 are loaded into memory of the host computer system 12 as they are needed. Components of the structured application development system 18 include selected data 52 that remain on the memory and various components of logic that are executable by a host computer processor of the host computer system 12 connected to the memory.

[0023] The structured application development system 18 includes a power profile data

library 20, a structured intent system 22, a developer kit 24, and an application 26 that is being developed. The application 26 may not initially form part of the structured application development system 18. However, it is shown as part of the structured application development system 18 because it is constructed by the other components of the structured application development system 18 in conjunction with selections that are made by a developer on the developer computer system 14.

[0024] The power profile data library 20 has a first reference intent 28 and second reference intent 30. By way of example, the first reference intent 28 may be “graphics-intensive” and the second reference intent 30 may be “startup” or any other label designated to characterize demands or loads on equipment included in the system on which the program is running. The first reference intent 28 has a first power profile 32 associated therewith. The first power profile 32 has a first clock speed 34 for a first processor and a second clock speed 36 for a second processor. The first processor may, for example, be a graphic processing unit (GPU) and the second processor may be a central processing unit (CPU). If the first reference intent 28 is a graphics-intensive intent, then the first clock speed 34 for the GPU will be set high and the second clock speed 36 for the CPU will be set low. The clock speeds are selected in a manner that will limit the amount maximum of heat per unit time that the first and second processors jointly generate on a multi-core processor chip, while at the same time having each processor run at a clock speed that is optimal given the first reference intent 28.

[0025] The second reference intent 30 has a second power profile 38 associated therewith. The second power profile 38 has a first clock speed 40 for the first processor and a second clock speed 42 for the second processor. By way of example, the second reference intent 30

is a startup intent. For startup purposes the first clock speed 40 is set relatively low if the first processor is a GPU and the second clock speed 42 is set relatively high if the second processor is a CPU. The first and second clock speeds 40 and 42 are preemptively determined to keep the heat generated by the first and second processors below a maximum amount of heat per unit time if the first and second processors are on the same multi-core processor chip. What should be noted is that the first clock speed 34 of the first power profile 32 may be higher than the first clock speed 40 of the second power profile 38 and that the second clock speed 36 of the first power profile 32 may be lower than the second clock speed 42 of the second power profile 38.

[0026] The power profile data library 20 only has first and second power profiles 32 and 38. It should however be understood that the power profile data library 20 may include more power profiles, for example four power profiles, each power profile being associated with a respective reference intent.

[0027] Furthermore, the first power profile 32 and the second power profile 38 include clock speeds for only first and second processors. Each power profile may also include a clock speed for a third processor, a fourth processor, etc.

[0028] The structured intent system 22 includes a set of target intents 46, an intent selection interface 48, a power profile lookup 50 and selected data 52.

[0029] The set of target intents 46 includes a first target intent 56 and second target intent 58. The first target intent 56 may, for example, be “graphics-intensive” and the second target intent 58 may be “startup” and are therefore similar to the first and second reference intents 28 and 30 in the power profile data library 20.

[0030] The developer at the developer computer system 14 uses a browser that resides on

the developer computer system 14 to access the intent selection interface 48 over the Internet 16. The intent selection interface 48 may, for example, be an interactive web page that is downloadable from the host computer system 12 over the Internet 16 on to the developer computer system 14 by the browser application and is viewable within a browser window on a display of the developer computer system 14. The intent selection interface 48 allows the developer to select sections of an application and select target intents for the respective sections.

[0031] At 60, the developer selects a first section 62 that will eventually form part of an application. The structured intent system 22 displays the first target intent 58 in the intent selection interface 48 as a first target intent 64 and the second target intent 58 as a second target intent 66. The developer is then prompted to select either the first target intent 64 or the second target intent 66 for association with the first section 62. It can be noted that the developer is not permitted to select both the first target intent 64 and the second target intent 66. The first target intent 64 and the second target intent 66 may, for example, be presented within the intent selection interface 48 in a drop down list that allows selection of only one of the first target intent 64 and the second target intent 66 and disallows selection of the other target intent. At 70, the developer makes a selection to associate the second target intent 66 (which is the same as the second target intent 58) with the first section 62. The first section 62 thus has the second target intent 66 associated therewith and the second target intent 66 is a startup-intensive target intent. The arrow 72 indicates the association of the second target intent 66 with the first section 62.

[0032] At 74, the developer makes a selection for a second section 76 of an eventual application. The structured intent system 22 displays the first target intent 56 as a first target

intent 78 and the second target intent 58 as a second target intent 80 so that the developer can make a selection between the first target intent 78 and the second target intent 80. Again, the developer is only permitted to select one of the first target intent 78 and the second target intent 80 at the exclusion of the other target intent. At 82, the developer makes a selection to associate the first target intent 78 (which is the same as the first target intent 56) with the second section 76. The arrow 84 indicates the association of the first target intent 78 with the second section 76.

[0033] The power profile lookup 50 uses the second target intent 66 of the first section 62 to determine a reference intent within the power profile data library 20. In the present example, the second target intent 66 matches the second reference intent 30 because they are both startup-intensive intents. The power profile lookup 50 then extracts the second power profile 38, including the first clock speed 40 and second clock speed 42, from the power profile data library 20. The power profile lookup 50 then stores the second power profile 38 as a second power profile 86 in the selected data 52. The power profile lookup 50 stores the first section 62 as a first section 88. The power profile lookup 50 also associates the second power profile 86 with the first section 88. As will be understood by one skilled in the art of data structures, the first section 88 and the first section 62 may be the exact same piece of data. However, for purposes of illustration and ease of explanation, the first section 62 and the first section 88 are shown as separate pieces of data.

[0034] Similarly, the power profile lookup 50 uses the first target intent 78 associated with the second section 76 to find a reference intent in the power profile data library 20. In the present example, the first target intent 78 matches the first reference intent 28 because they are both graphics-intensive intents. The power profile lookup 50 extracts the first power

profile 32 associated with the first reference intent 28, including the first clock speed 34 and the second clock speed 36. The power profile lookup 50 then stores the first power profile 32 as a first power profile 90 within the selected data 52. The power profile lookup 50 stores the second section 76 as a second section 92 within the selected data 52. The power profile lookup 50 also associates the first power profile 90 with the second section 92 in the selected data 52.

[0035] The developer is not permitted to select clock speeds that are not represented in the respective power profiles 86 and 90. It is thus not possible for the developer to select clock speeds that, in combination, will result in too much heat being generated per unit time on a multi-core processor chip. The developer is, however, permitted to select a target intent for a respective section for purposes of tailoring the clock speeds of the respective processors without resulting in too much heat per unit time being generated by the processors in combination.

[0036] The developer kit 24 includes a set of tools 96, a tool selection interface 94, an application developer logic 100 and a power limiter logic 102.

[0037] The set of tools 96 are a set of basic tools that a developer requires to structure the components of sections of an application that are stored on a storage device of host computer system 12. The set of tools 96 is represented as Tool 1 to Tool 6. The developer at the developer computer system 14 downloads the tool selection interface 94 from the host computer system 12 for display on the developer computer system 14, similar to the way that the intent selection interface 48 was displayed. The tool selection interface 94 includes a first section 104 and a second section 106 that correspond to the first section 88 and the second section 92 in the selected data 52. The tools of the set of tools 96 are also displayed

within the tool selection interface 94. At 108, the developer selects a first tool (Tool 3) for the first section 104. The developer subsequently proceeds to select further tools for the first section 104. The tools for the first section 104 are thus configurable by the developer in terms of their selection and their sequence. The developer also selects tools for the second section 106 in a configurable manner. The first section 104 and its tools and the second section 106 and its tools represent to the developer how the application will function in terms of its sections and the functionality of each section.

[0038] The application developer logic 100 creates first and second sections 112 and 114 in the application 26. The first section 112 corresponds to the first sections 62, 88 and 104. The second section 114 corresponds to the second sections 76, 92 and 106. The application developer logic 100 compiles the tools of the first section 104 as a first routine 118 and enters the first routine 118 within the first section 112 of the application 26. The application developer logic 100 compiles the tools of the second section 106 as a second routine 120 and enters the second routine 120 in the second section 114.

[0039] The power limiter logic 102 retrieves the second power profile 86 corresponding to the first section 88 from the selected data 52 and enters the second power profile 86 as a second power profile 122 as part of the first section 112 of the application 26. The power limiter logic 102 also retrieves the first power profile 90 corresponding to the second section 92 in the selected data 52 and enters the first power profile 90 as a first power profile 124 in the second section 114. The second power profile 122 of the first section 112 includes the first clock speed 40 for the first processor and second clock speed 42 for the second processor. The first power profile 124 of the second section 114 includes the first clock speed 34 for the first processor and the second clock speed 36 for the second processor. The

first section 112 and the second section 114 thus each has a respective routine 118 and 120 and each has respective clock speeds for the first and second processors that are selected to be intent-specific and that are limited by the power limiter logic 102 to limit the generation of more than a predetermined amount of heat per unit time for the processors in combination.

[0040] As shown in Figure 2, the structured application development system 18 further includes a download interface 98. The developer at the developer computer system 14 retrieves the download interface 98 from the host computer system 12 and displays the download interface 98 on the display of the developer computer system 14. The developer, using the developer computer system 14, interacts with the download interface 98 to download the application 26 from the host computer system 12 on to the developer computer system 14. The application 26 then resides as an application 130 on the developer computer system 14.

[0041] Figure 3 shows the developer computer system 14 and a consumer device 132. The consumer device 132 has a storage medium 134 and a multi-core processor chip 136. The multi-core processor chip 136 has a body 140 and first and second processors 142 and 144 manufactured in and on the body 140. The body 140 includes a semiconductor material such as silicon, germanium, gallium arsenide or the like and may include further components and materials that are commonly known in the art of semiconductor packaging. The first and second processors 142 and 144 include transistors and other electrical components that are interconnected to form logic devices. The first and second processors 142 and 144 are connected to external power sources and have clocks that can be set at preselected clock speeds. The developer uses the developer computer system 14 to create a

copy of the application 130 and store the copy of the application as an application 150 on the storage medium 134. The consumer device 132 is then programmed with the application 150. In a bulk manufacturing process, the application 130 may first be transferred to a programmer that is used to program multiple consumer devices for scaled distribution.

[0042] Figures 4 and 5 illustrate how the application 150 executes on the consumer device 132. In Figure 4, the first section 112 of the application 150 executes. The clock speeds of the second power profile 122 are used to set the clock speeds of the first and second processors 142 and 144. By way of example, the second power profile 122 includes a first clock speed of 39 GHz for the first processor 142 and a second clock speed for the second processor 144 of 200 GHz. The first and second processors 142 and 144 execute the first routine 118. Sections of the first routine 118 that are executed by the first processor 142 are represented by a first routine 118A and sections of the first routine 118 that are executed by the second processor 144 are represented by a first routine 118B. The first routine 118A and 118B may be partially executed at the same time or may have portions that interweave so that portions of the first routine 118A and the first routine 118B alternate with one another. The clock speeds at which the first routine 118A and the first routine 118B are executed by the first processor 142 and the second processor 144 originate from the power profile data library 20 in Figure 1 and due to the logic that is provided to the developer and not provided to the developer, the developer is prevented from selecting different clock speeds.

[0043] Figure 5 shows the execution of the second section 114. The first power profile 124 is used to set the clock speeds of the first processor 142 and the second processor 144. By way of example, the first processor 142 has a clock speed of 150 GHz and the second processor 144 has a clock speed of 120 GHz. The second routine 120 is executed by the

first and second processors 142 and 144. Components of the second routine 120 that are executed by the first processor 142 are represented by a second routine 120A and components of the second routine 120 that are executed by the second processor 144 are represented as a second routine 120B.

[0044] Figures 6A, 6B and 6C show that three different processors may have three different heat generation curves. In each figure, heat generated per unit time in Watts is shown on the vertical axis and performance as a percentage of maximum clock speed is shown on the horizontal axis. The heat generation curve for the processor shown in Figure 6A initially increases slowly, followed by an acceleration and then a deceleration. The heat generation curve for the processor in Figure 6B initially increases rapidly followed by a gradual deceleration. The heat generation curve for the processor shown in Figure 6C increases linearly. The heat generation curves shown in Figures 6A, 6B and 6C have to be considered when calculating a total amount of heat generated by the three processors.

[0045] Figures 7A, 7B and 7C show three different power profiles that may be stored. Figure 7A shows a power profile wherein priority is given to a first of the processors. The first processor is permitted to run at 100% of its maximum clock speed. The clock speeds of the second and third processors are reduced to below 100% of their maximum clock speeds. Figure 7B shows a power profile wherein priority is given to a third processor. The third processor is set to run at a clock speed that is equal to 100% of its maximum clock speed while the clock speeds of the first and second processors are reduced to below 100% of their maximum clock speeds. Figure 7C shows a power profile wherein performance is balanced. The clock speeds of all three processors are reduced to below 100% of their maximum clock speeds.

[0046] Figure 8A, 8B and 8C illustrate the heat generated by the power profiles in Figures 7A, 7B and 7C, respectively. Each processor generates heat according to its respective heat generation curve in Figures 6A, 6B and 6C. The total amount of heat generated per unit time for all three processors is the same in Figures 8A, 8B and 8C. Although the total amount of heat generated per unit time is the same, a small variation may be possible without departing from the scope and spirit of the invention. For example, the total amount of heat generated per unit time by a first power profile may be less than 10% higher or less than 10% lower than the total amount of heat generated per unit time following a second power profile. A third power profile may generate heat per unit time that is less than 10% higher or lower than that of the first power profile.

[0047] The consumer device 132 described herein may be a mixed reality system as described in U.S. Patent Application No: 14/331,218 which is incorporated by reference herein.

[0048] Figure 9 shows a diagrammatic representation of a machine in the exemplary form of a computer system 900 within which a set of instructions, for causing the machine to perform any one or more of the methodologies discussed herein, may be executed. In alternative embodiments, the machine operates as a standalone device or may be connected (e.g., networked) to other machines. In a network deployment, the machine may operate in the capacity of a server or a client machine in a server-client network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify

actions to be taken by that machine. Further, while only a single machine is illustrated, the term “machine” shall also be taken to include any collection of machines that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies discussed herein.

[0049] The exemplary computer system 900 includes a processor 930 (e.g., a central processing unit (CPU), a graphics processing unit (GPU), or both), a main memory 932 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), and a static memory 934 (e.g., flash memory, static random access memory (SRAM, etc.), which communicate with each other via a bus 936.

[0050] The computer system 900 may further include a video display 938 (e.g., a liquid crystal displays (LCD) or a cathode ray tube (CRT)). The computer system 900 also includes an alpha-numeric input device 940 (e.g., a keyboard), a cursor control device 942 (e.g., a mouse), a disk drive unit 944, a signal generation device 946 (e.g., a speaker), and a network interface device 948.

[0051] The disk drive unit 944 includes a machine-readable medium 950 on which is stored one or more sets of instructions 952 (e.g., software) embodying any one or more of the methodologies or functions described herein. The software may also reside, completely or at least partially, within the main memory 932 and/or within the processor 930 during execution thereof by the computer system 900, the memory 932 and the processor 930 also constituting machine readable media. The software may further be transmitted or received over a network 954 via the network interface device 948.

[0052] While certain exemplary embodiments have been described and shown in the

accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described since modifications may occur to those ordinarily skilled in the art.

CLAIMS

What is claimed:

1. A host computer system comprising:
 - a host computer processor;
 - a computer-readable medium connected to the host computer processor; and
 - a set of instructions on the computer-readable medium, the set of instructions being readable by the host computer processor and including:
 - a structured application development system having:
 - a power profile data library on the computer-readable medium that includes:
 - a first reference intent;
 - a first power profile associated with the first reference intent
 - and having a respective first maximum clock speed for a first processor and a respective second maximum clock speed for a second processor;
 - a second reference intent; and
 - a second power profile associated with the second reference intent and having a respective first maximum clock speed for the first processor and a respective second maximum clock speed for the second processor, the first maximum clock speed of the first power profile being different from the first maximum clock speed for the second power profile.
2. The host computer system of claim 1 wherein,

the structured application development system has:

a structured intent system includes:

a set of target intents including first and second target intents;

an intent selection interface to select first and second sections

and select a target intent from the set of target intents for association with the first and second section respectively; and

a power profile lookup that determines a power profile for each of the first and second sections from the power profile data by matching the target intent selected for the respective section and a reference intent to associate a power profile.

3. The host computer system of claim 2, wherein

the structured application development system has:

a developer kit that includes:

a set of tools;

a tool selector interface to select tools from the set of tools and arrange the tools in a customizable order for the first and second sections;

an application developer logic configured to generate an application based on the order that the tools are arranged for the first and second sections, the application being executable by a processor of a consumer device; and

a power limiter logic that, due to associating each of the first and second section with a respective power profile, is configured to limit the first and second processors to the maximum clock speeds of the respective power profile for the

respective section when the respective section is executed on a consumer device having the first and second processors.

4. The host computer system of claim 3, wherein the intent selection interface is accessible over a network from a developer computer system to select the first and second sections and select the target intent from the set of target intents for association with the first and second section respectively.

5. The host computer system of claim 3, wherein the intent selection interface is accessible over a network from a developer computer system to select the tools from the set of tools and arrange the tools in the customizable order for the first and second sections.

6. The host computer system of claim 3, wherein the power limiter logic inserts the maximum clock speeds of the respective power profile for the respective section into the application.

7. The host computer system of claim 6, wherein the structured application development system further has:

a download interface that is accessible over a network from a developer computer system to download the application with the maximum clock speeds of the respective power profile for the respective section in the application from the host computer system onto the developer computer system.

8. The host computer system of claim 1, wherein the second maximum clock speed of the first power profile is different from the second maximum clock speed for the second power profile.
9. The host computer system of claim 1, wherein the second maximum clock speed for the first power profile is the same as the second maximum clock speed for the second power profile.
10. A method of operating a host computer system comprising:
storing a power profile data library on a computer-readable medium, the power profile data library including:
a first reference intent;
a first power profile associated with the first reference intent and having a respective first maximum clock speed for a first processor and a respective second maximum clock speed for a second processor;
a second reference intent; and
a second power profile associated with the second reference intent and having a respective first maximum clock speed for the first processor and a respective second maximum clock speed for the second processor, the first maximum clock speed of the first power profile being different from the first maximum clock speed for the second power profile.

11. The method of claim 10, further comprising:

storing a set of target intents including first and second target intents on the computer-readable medium;

displaying, with a host computer processor, an intent selection interface to select first and second sections and select a target intent from the set of target intents for association with the first and second section respectively; and

executing, with the host computer processor, a power profile lookup that determines a power profile for each of the first and second sections from the power profile data by matching the target intent selected for the respective section and a reference intent to associate a power profile.

12. The method of claim 11, further comprising:

storing a set of tools on the computer-readable medium;

displaying, with the host computer processor, a tool selector interface to select tools from the set of tools and arrange the tools in a customizable order for the first and second sections;

executing, with the host computer processor, an application developer logic that generates an application based on the order that the tools are arranged for the first and second sections, the application being executable by a processor of a consumer device; and

executing, with the host computer processor, a power limiter logic that, due to associating each of the first and second section with a respective power profile, limits the first and second processors to the maximum clock speeds of the respective power profile for

the respective section when the respective section is executed on a consumer device having the first and second processors.

13. A consumer device that includes:

a multi-core processor chip having a body and a plurality of processors on the body;

a computer-readable medium connected to the processors; and

an application on the computer-readable medium, the application having:

a first section, the first section having:

a first routine that is executable by the processors; and

a first power profile having a respective maximum clock speed for

each one of the processors; and

a second section, the second section having:

a second routine that is executable by the processors; and

a second power profile having a respective maximum clock speed for

each one of the processors so that at least one of the processors has a maximum clock speed that changes from the first section to the second section, wherein the processors jointly generate a first amount of heat per unit time during the first section and a second amount of heat during the second section and the second amount of heat is less than 10% different than the first amount of heat.

14. The consumer device of claim 13, wherein the second amount of heat is the same as the first amount of heat.

15. The consumer device of claim 13, wherein the first and second processors have different heat generation curves.

16. The consumer device of claim 13, wherein the processors include at least a first processor and a second processor, the second processor generating less heat per unit time than the first processor during the first section and more heat than the first processor during the second section. wherein the processors include at least a third processor, the third processor generating less heat per unit time than the first processor during the first section and more heat than the first processor during the second section.

17. The consumer device of claim 13, further comprising:

a third section, the third section having:

a third routine that is executable by the processors; and

a third power profile having a respective maximum clock speed for each one of the processors so that at least one of the processors has a maximum clock speed that changes from the first section to the third section, wherein the processors jointly generate a third amount of heat per unit time during the third section and the third amount of heat is less than 10% different than the first amount of heat.

18. A method of operating a consumer device that includes:

storing an application on the computer-readable medium connected to a plurality of processors on a body of a multi-core processor chip, the application having first and second sections;

executing the first section with the processors, the first section having:

a first routine that is executable by the processors; and

a first power profile having a respective maximum clock speed for each one of the processors; and

executing the second section with the processors, the second section having:

a second routine that is executable by the processors; and

a second power profile having a respective maximum clock speed for each one of the processors so that at least one of the processors has a maximum clock speed that changes from the first section to the second section, wherein the processors jointly generate a first amount of heat per unit time during the first section and a second amount of heat during the second section and the second amount of heat is less than 10% different than the first amount of heat.

19. A consumer device that includes:

first and second processors;

a computer-readable medium connected to the processors; and

an application on the computer-readable medium, the application having:

a first section, the first section having:

a first routine that is executable by the first and second processors;

and

a first power profile, the first power profile having first and second maximum clock speeds for the first and second processors; and

a second section, the second section having:

a second routine that is executable by the first and second processors;
and

a second power profile, the second power profile having first and second maximum clock speeds for the first and second processors, the first maximum clock speed of the first power profile being different from the first maximum clock speed for the second power profile and the second maximum clock speed of the first power profile be different from the second maximum clock speed for the second power profile.

20. The consumer device of claim 19, further comprising:

a multi-core processor chip holding the first and second processors.

21. The consumer device of claim 19, wherein the first and second processors have different heat generation curves.

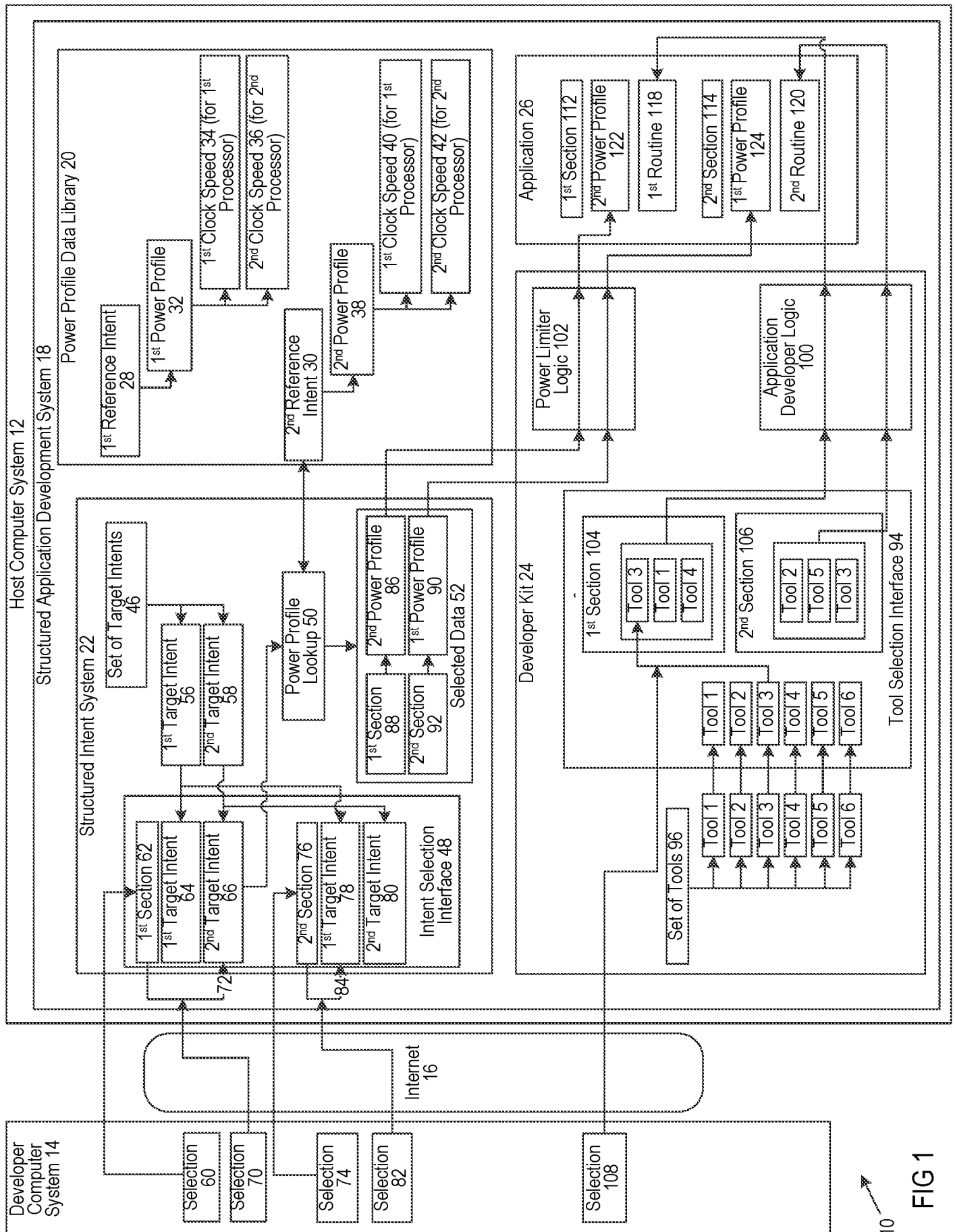
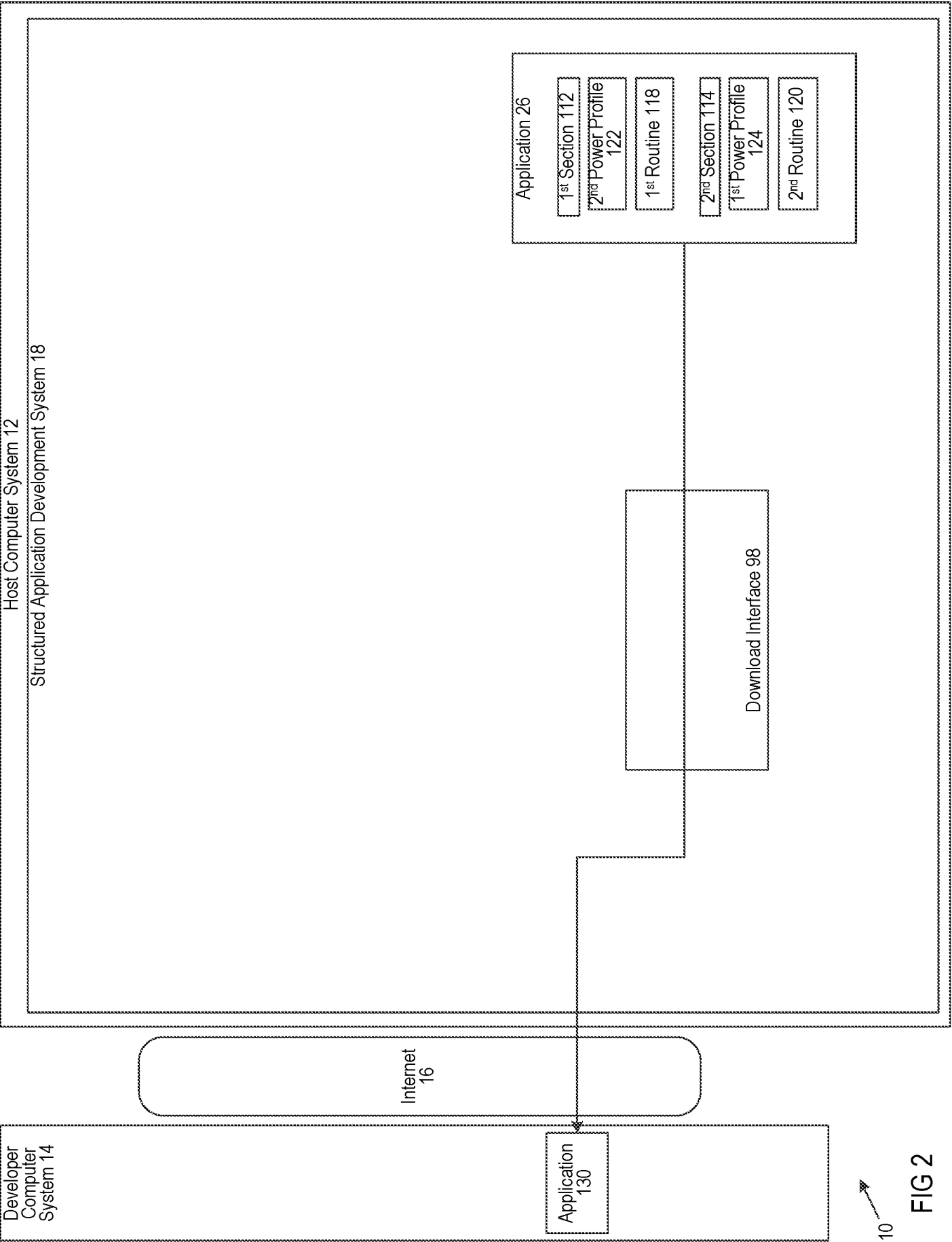
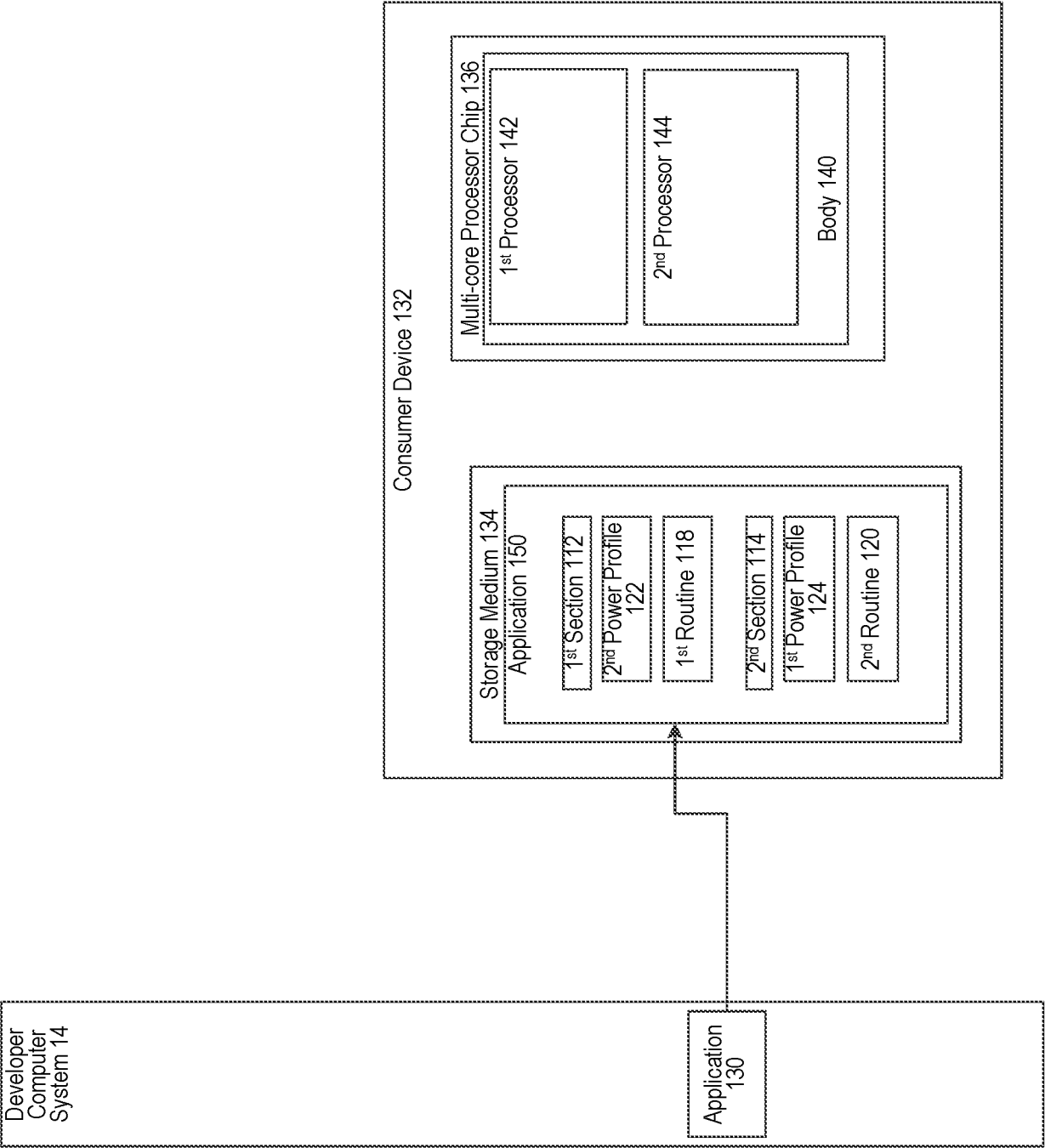


FIG 1



10

FIG 2



10

FIG 3

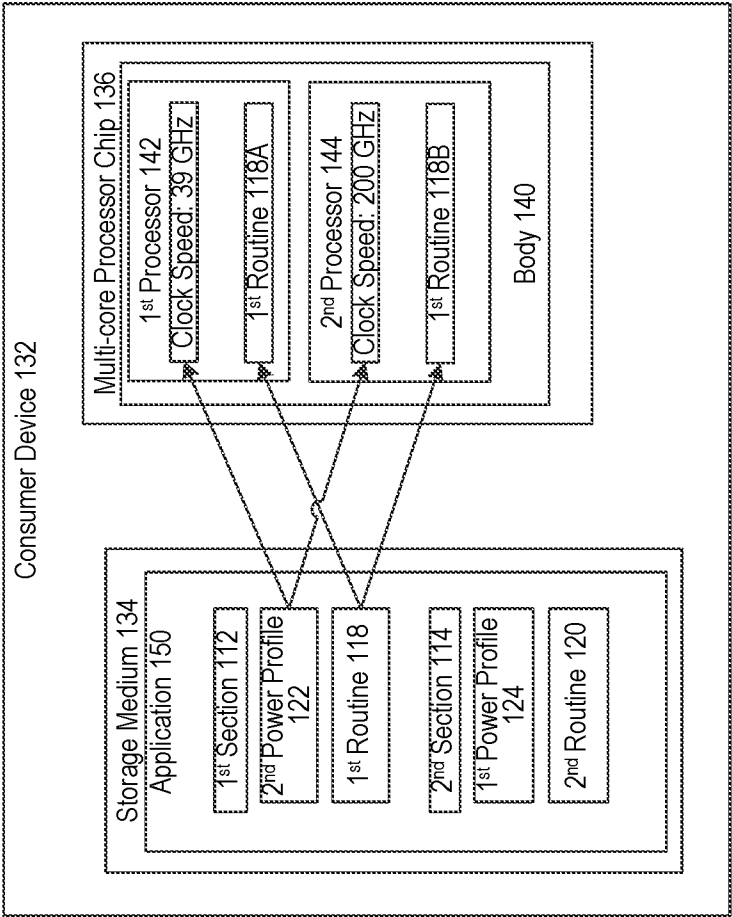


FIG 4

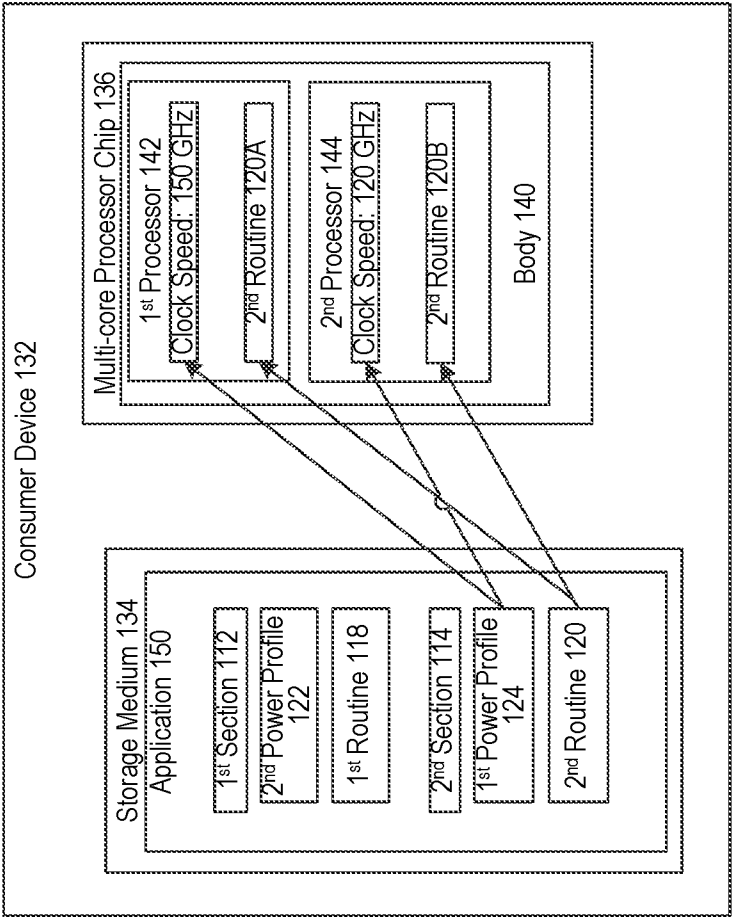
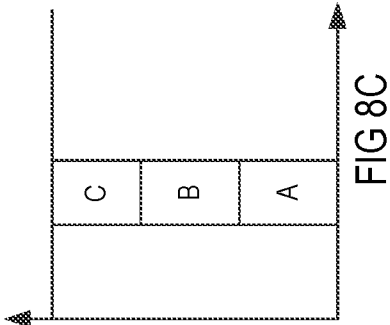
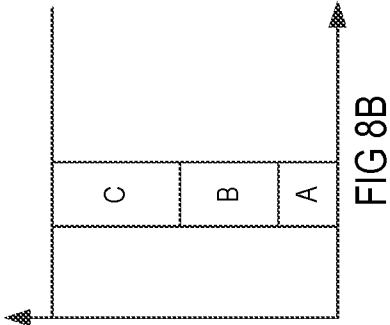
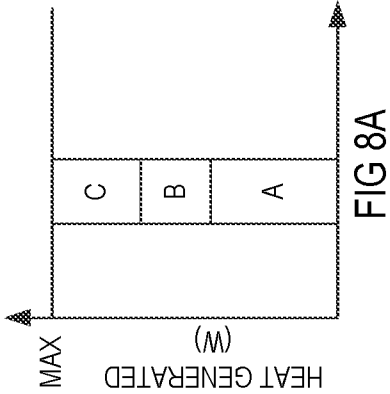
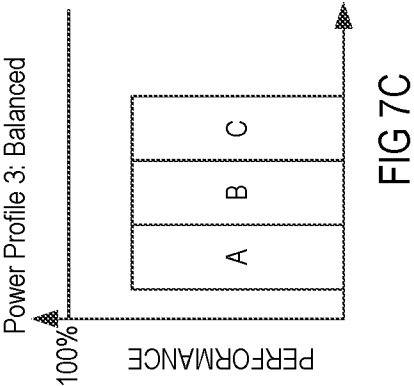
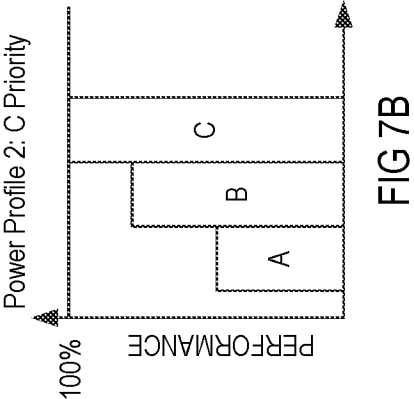
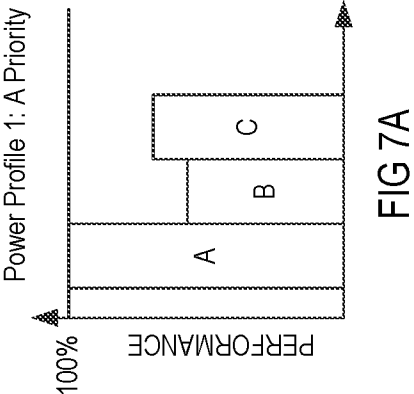
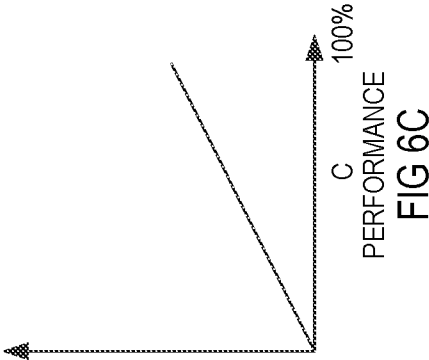
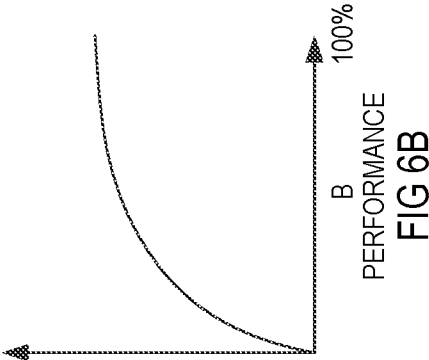
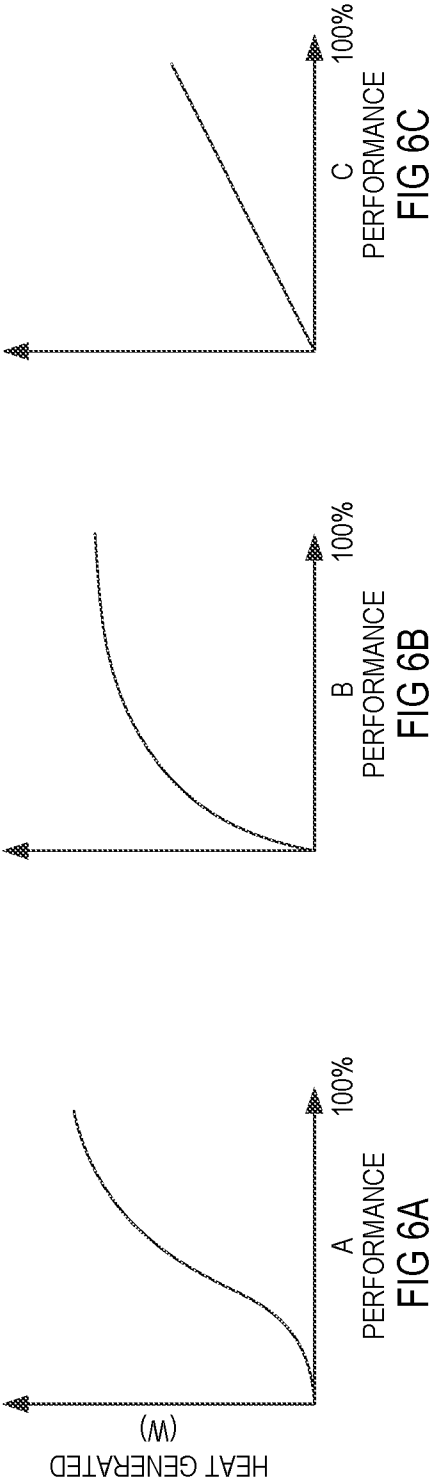


FIG 5



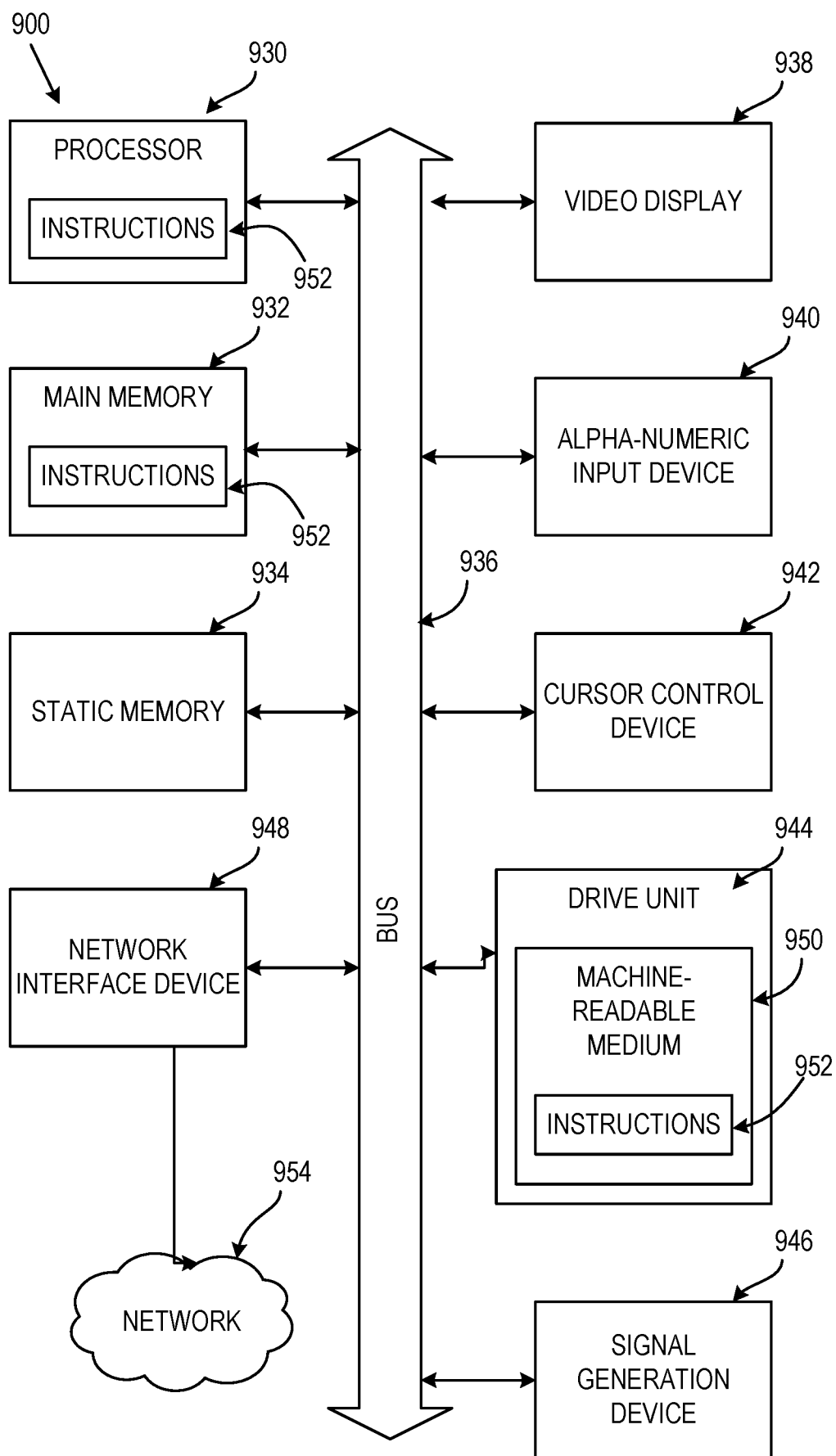


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2020/017023

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See extra sheet(s).

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-12, 19-21

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2020/017023

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G06F 1/28; G06F 1/32; H04B 1/707 (2020.01)

CPC - G06F 1/3206; G06F 1/3287; G06F 1/10; G06F 1/189; G06F 1/206 (2020.05)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

see Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

see Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

see Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2018/0102981 A1 (MICROSOFT TECHNOLOGY LICENSING, LLC) 12 April 2018 (12.04.2018) entire document	1-12, 19-21
A	US 2011/0145617 A1 (THOMSON et al) 16 June 2011 (16.06.2011) entire document	1-12, 19-21
A	US 2015/0134995 A1 (SAMSUNG ELECTRONICS CO., LTD) 14 May 2015 (14.05.2015) entire document	1-12, 19-21
A	US 2012/0246506 A1 (KNIGHT) 27 September 2012 (27.09.2012) entire document	1-12, 19-21
A	US 2004/0001533 A1 (TRAN et al) 01 January 2004 (01.01.2004) entire document	1-12, 19-21
A	WEISSEL et al. "Process cruise control: event-driven clock scaling for dynamic power management." In: Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems. 11 October 2002 (11.10.2002) Retrieved on 16 May 2020 (16.05.2020) from <URL: https://dl.acm.org/doi/pdf/10.1145/581630.581668 > entire document	1-12, 19-21

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

25 May 2020

Date of mailing of the international search report

15 JUN 2020

Name and mailing address of the ISA/US

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Facsimile No. 571-273-8300

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Telephone No. PCT Helpdesk: 571-272-4300

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2020/017023

Continued from Box No. III Observations where unity of invention is lacking

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claims 1-12, 19-21, drawn to a host computer system comprising: a host computer processor; a computer-readable medium connected to the host computer processor

Group II, claims 13-18, 19-21, drawn to a consumer device that includes: a multi-core processor chip having a body and a plurality of processors on the body.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention: a host computer system comprising: a host computer processor; a computer-readable medium connected to the host computer processor; a power profile data library on the computer-readable medium that includes: a first reference intent; a first power profile associated with the first reference intent and having a respective first maximum clock speed for a first processor and a respective second maximum clock speed for a second processor; a second reference intent; and a second power profile associated with the second reference intent and having a respective first maximum clock speed for the first processor and a respective second maximum clock speed for the second processor, the first maximum clock speed of the first power profile being different from the first maximum clock speed for the second power profile as claimed therein is not present in the invention of Group II. The special technical feature of the Group II invention: a consumer device that includes: a multi-core processor chip having a body and a plurality of processors on the body; a computer-readable medium connected to the processors; and an application on the computer-readable medium, the application having: a first section, the first section having: a first routine that is executable by the processors; and a first power profile having a respective maximum clock speed for each one of the processors; and a second section, the second section having: a second routine that is executable by the processors; and a second power profile having a respective maximum clock speed for each one of the processors so that at least one of the processors has a maximum clock speed that changes from the first section to the second section, wherein the processors jointly generate a first amount of heat per unit time during the first section and a second amount of heat during the second section and the second amount of heat is less than 10% different than the first amount of heat as claimed therein is not present in the invention of Group I.

Unity exists between claims 1-12 and 19-21 (Group I) or between claims 13-18 and 19-21 (Group II). However unity does not exist between claims 1-12 and 13-18 since there exists no common special technical feature between independent claims 1 and 13 (see PCT Examination Guidelines Chapter 10 at 10.30, Example 10).

Groups I and II lack unity of invention because even though the inventions of these groups require the technical feature of a computer readable medium connected to the processor; a first power profile having a respective maximum clock speed for a processor and a second power profile having a respective maximum clock speed for a processor, this technical feature is not a special technical feature as it does not make a contribution over the prior art.

Specifically, US 2004/0001533 to Tran et al. teaches a computer readable medium connected to the processor; a first power profile having a respective maximum clock speed for a processor and a second power profile having a respective maximum clock speed for a processor (para. [0005], [0041], [0080-0083], [0085]).

Since none of the special technical features of the Group I or II inventions are found in more than one of the inventions, unity of invention is lacking.