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(54) **Display panel driving method**

(57) A display panel includes a number of display lines. These display lines are divided into a plurality of adjacent display line groups. Pixel cells arranged on the respective display lines in each display line group are made to emit light continuously over different light emission periods based on weighting values allocated to the display lines for each field display period. The light emis-

sion operation spanning these light emission periods is divided into a first-half period and second-half period of the field display period. A favorable image display in which flicker and dither patterns are suppressed is feasible.

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a driving method for a display panel that has a multiple grayscale processing circuit that subjects a video input signal to multiple grayscale processing.

2. Description of the Related Art

[0002] Recently, where two-dimensional image display panels are concerned, plasma display panels (hereinafter called 'PDP'), in which a plurality of discharge cells are arranged in the form of a matrix, have been attracting attention. The subfield method is known as a driving method for displaying an image corresponding with a video input signal on the PDP. The subfield method divides a single-field display period into a plurality of subfields and causes each of the discharge cells to selectively discharge light in each subfield in accordance with the luminance level represented by the video input signal. Accordingly, an intermediate luminance corresponding with the total light emission period within the single-field period is then visible.

[0003] Fig. 1 of the attached drawings shows an example of a light emission drive sequence based on this subfield method. This emission drive sequence is disclosed in, for example, Japanese Patent Application Kokai (Laid-Open Publication) No. 2000-227778.

[0004] The light emission drive sequence shown in Fig. 1 divides a single field period into 14 subfields, which are the subfields SF1 to SF14. All the discharge cells of the PDP are initialized in lit mode only in the leading subfield SF1 of these subfields SF1 to SF14 (Rc). Each of the subfields SF1 to SF14 sets some of the discharge cells to unlit mode in accordance with the video input signal (Wc) and causes only the discharge cells of lit mode to discharge light over the period allocated to the subfield concerned (Ic).

[0005] Fig. 2 of the attached drawings shows an example of a light emission drive pattern in a single field period of each discharge cell that is driven on the basis of this light emission drive sequence (see Japanese Patent Application Kokai No. 2000-2277785).

[0006] According to the light emission pattern shown in Fig. 2, the discharge cells initialized in lit mode in the leading subfield SF1 are then set to unlit mode in a particular one subfield of the subfields SF1 to SF14, as indicated by the black circles. Once the discharge cell is set to unlit mode, the discharge cell does not re-enter lit mode until the one field period ends. Accordingly, during the period until the discharge cells are set to unlit mode, as indicated by the white circles, the discharge cells discharge light continuously in these subfields. Here, each of the fifteen different light emission patterns shown in

Fig. 2 has a different total light emission period within a single field period, and hence fifteen different intermediate luminances are rendered. That is, an intermediate luminance display for (N+1) grayscales (N being the number of subfields) is feasible.

[0007] However, with this driving method, because there are restrictions on the number of subfields, there is a shortage in the number of grayscales. In order to compensate for the shortage in the number of grayscales, multiple grayscale processing such as error diffusion and dither processing is performed on the video input signal.

[0008] Error diffusion processing converts the video input signal into 8-bit pixel data, for example, for each pixel. The upper 6 bits of the pixel data is treated as display data and the remaining lower two bits of the pixel data is treated as error data. Then, the error data of the pixel data are weighted and added based on the respective peripheral pixels and the resultant is reflected in the display data. As a result of this operation, a pseudo-representation of the luminance of the lower two bits of the original pixel is provided by the peripheral pixels, and, consequently, a luminance grayscale representation of the 8 bits of pixel data is possible by means of the six bits of display data. Further, dither processing is performed on the six-bit error-diffusion-processed pixel data obtained by the error diffusion processing. In dither processing, a single pixel unit is rendered from a plurality of adjoining pixels, and dither coefficients consisting of different coefficient values are allocated and added to the error-diffusion-processed pixel data corresponding with the respective pixels in the single pixel unit. As a result of the addition of the dither coefficients, when viewed in the single pixel unit, the luminance of the 8-bit original data can be represented by only the upper four bits of the dither-added pixel data. Therefore, the upper four bits of the dither-added pixel data are extracted and allocated to each of the 15 different light emission patterns shown in Fig. 2 as multiple grayscale pixel data PDs.

[0009] However, when a dither coefficient addition is performed regularly on the pixel data by means of dither processing and so forth, a pseudo pattern which is completely independent of the video input signal, i.e. a so-called dither pattern, is sometimes observed, which compromises the quality of the displayed image.

[0010] In addition, if the light emission drive pattern shown in Fig. 2 is employed, switching from the continuous light emission state to the unlit state occurs once or less within a single field period. This means that the switching frequency is the same as the vertical synchronization frequency for a single field display period. Accordingly, when a PAL television signal whose vertical synchronization frequency is only 50Hz is supplied as the video input signal, flicker is prominent.

SUMMARY OF THE INVENTION

[0011] An object of the present invention is to provide a display panel driving method that can produce an improved image display in which flicker and dither patterns are suppressed.

[0012] According to one embodiment of the present invention, there is provided an improved driving method to performs grayscale driving of a display panel in accordance with pixel data derived from on a video input signal. The display panel includes pixel cells arranged on each of display lines of the display panel. The display lines are divided into a plurality of display line groups, and each display line group consists of a plurality of adjacent display lines. The driving method includes a light emission driving step in which, in accordance with the pixel data, the pixel cells arranged on the display lines in the display line group concerned are made to emit light continuously over different light emission periods based on weighting values allocated to the display lines in the display line group concerned, for each field display period of the video signal. Each of the light emission periods is divided into two parts such that one part takes place in a first-half period of the field display period concerned and another part takes place in a second-half period of the field display period concerned. Each part starts from a reset step.

[0013] These and other objects, aspects and advantages of the present invention will become apparent to those skilled in the art when the following detailed description and appended claims are read and understood in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]

Fig. 1 shows an example of a light emission drive sequence based on the subfield method;

Fig. 2 shows an example of light emission drive patterns within a single field period for each discharge cell that is driven on the basis of the light emission drive sequence shown in Fig. 1;

Fig. 3 shows the constitution of a plasma display device that is driven by the driving method according to the present invention;

Fig. 4 shows an example of line dither offset values; Fig. 5 shows a data conversion table used by a drive data conversion circuit shown in Fig. 3;

Figs. 6A to 6H show examples of light emission drive sequences in the first to eighth fields, respectively;

Fig. 7 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 6A; Fig. 8 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 6B; Fig. 9 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 6C;

Fig. 10 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 6D;

Fig. 11 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 6E;

Fig. 12 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 6F;

Fig. 13 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 6G;

Fig. 14 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 6H;

Fig. 15 shows the luminance level of each of the first to fifth grayscale drive fields for each display line;

Fig. 16 serves to illustrate the line dither processing operation when pixel data of [010100] is supplied;

Fig. 17 represents the transition of the line dither weighting for each display line;

Fig. 18 shows an example of a light emission drive sequence when the weighting of the luminance is varied for each subfield;

Fig. 19 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 18;

Fig. 20 shows the luminance level for each display line of each of the first to fifth grayscale driving when the optical drive sequence shown in Fig. 18 is employed;

Fig. 21 shows an example of the light emission drive sequence according to the present invention;

Fig. 22 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 21;

Fig. 23 shows another example of the light emission drive sequence according to the present invention; and

Fig. 24 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 23.

DETAILED DESCRIPTION OF THE INVENTION

[0015] A description of a drive device for driving a plasma display panel (PDP) based on a driving method of the present invention will now be provided with reference to Fig. 3.

[0016] The PDP 100 includes a front-side substrate (not shown) that functions as a display surface, and a rear-side substrate (not shown) that is disposed in a position opposite the front-side substrate. A discharge space filled with discharge gas is defined between the front-side substrate and rear-side substrate. Belt-shaped row electrodes X_1 to X_n and row electrodes Y_1 to Y_n are alternately arranged in parallel to each other

and provided on the front-side substrate. Belt-shaped column electrodes D_1 to D_m arranged to cross over the row electrodes are provided on the rear-side substrate. The row electrodes X_1 to X_n and Y_1 to Y_n are arranged such that the first to n th display lines of the PDP 100 are defined by n pairs of row electrodes X_i and Y_i . Discharge cells G serving as pixels are formed at the intersection points (including the discharge space) between the row electrode pairs and column electrodes. That is, $(n \times m)$ discharge cells $G_{(1,1)}$ to $G_{(n,m)}$ are formed in a matrix shape on the PDP 100.

[0017] A pixel data conversion circuit 1 converts a video input signal into 6-bit pixel data PD, for example, for each pixel, and then supplies this pixel data PD to a multiple grayscale processing circuit 2. The multiple grayscale processing circuit 2 includes a line dither offset value generation circuit 21, an adder 22, and a lower bit discard circuit 23.

[0018] The line dither offset value generation circuit 21 first generates eight line dither offset values LD with the values '0' to '7' respectively to match eight display line groups of the PDP 100. The first to n th display lines of the PDP 100 are separated by eight lines and grouped as shown below:

the $(8N-7)$ th display line group consisting of the 1st, 9th, 17th, ..., $(n-7)$ th display lines;
 the $(8N-6)$ th display line group consisting of the 2nd, 10th, 18th, ..., and $(n-6)$ th display lines;
 the $(8N-5)$ th display line group consisting of the 3rd, 11th, 19th, ..., and $(n-5)$ th display lines;
 the $(8N-4)$ th display line group consisting of the 4th, 12th, 20th, ..., and $(n-4)$ th display lines;
 the $(8N-3)$ th display line group consisting of the 5th, 13th, 21st, ..., and $(n-3)$ th display lines;
 the $(8N-2)$ th display line group consisting of the 6th, 14th, 22nd, ..., and $(n-2)$ th display lines;
 the $(8N-1)$ th display line group consisting of the 7th, 15th, 23rd, ..., and $(n-1)$ th display lines; and
 the $(8N)$ th display line group consisting of the 8th, 16th, 24th, ..., and n th display lines.

[0019] Here, N is a natural number equal to or less than $(1/8) \cdot n$. The line dither offset value generation circuit 21 repeatedly executes, for each field and with 8 fields forming one cycle, the alteration of allocation of the line dither offset values LD to the display line groups, as shown in Figs. 4A to 4H.

[0020] Specifically, as shown in Fig. 4A, the line dither offset value generation circuit 21 allocates, in the very first field, the following line dither offset values LD to the eight display line groups:

'0' for the $(8N-7)$ th display line group,
 '3' for the $(8N-6)$ th display line group,
 '6' for the $(8N-5)$ th display line group,
 '1' for the $(8N-4)$ th display line group,
 '4' for the $(8N-3)$ th display line group,

'7' for the $(8N-2)$ th display line group,
 '2' for the $(8N-1)$ th display line group, and
 '5' for the $(8N)$ th display line group.

5 **[0021]** As shown in Fig. 4B, the line dither offset values LD with the following values are allocated in the second field:

10 '4' for the $(8N-7)$ th display line group;
 '7' for the $(8N-6)$ th display line group;
 '2' for the $(8N-5)$ th display line group;
 '5' for the $(8N-4)$ th display line group;
 '0' for the $(8N-3)$ th display line group;
 '3' for the $(8N-2)$ th display line group;
 15 '6' for the $(8N-1)$ th display line group; and
 '1' for the $(8N)$ th display line group.

[0022] As shown in Fig. 4C, the line dither offset values LD with the following values are allocated in the third field:

20 '2' for the $(8N-7)$ th display line group;
 '5' for the $(8N-6)$ th display line group;
 '0' for the $(8N-5)$ th display line group;
 '3' for the $(8N-4)$ th display line group;
 25 '6' for the $(8N-3)$ th display line group;
 '1' for the $(8N-2)$ th display line group;
 '4' for the $(8N-1)$ th display line group; and
 '7' for the $(8N)$ th display line group.

[0023] As shown in Fig. 4D, the line dither offset values LD with the following values are allocated in the fourth field:

30 '6' for the $(8N-7)$ th display line group;
 '1' for the $(8N-6)$ th display line group;
 '4' for the $(8N-5)$ th display line group;
 '7' for the $(8N-4)$ th display line group;
 '2' for the $(8N-3)$ th display line group;
 35 '5' for the $(8N-2)$ th display line group;
 '0' for the $(8N-1)$ th display line group; and
 '3' for the $(8N)$ th display line group.

[0024] As shown in Fig. 4E, the line dither offset values LD with the following values are allocated in the fifth field:

40 '1' for the $(8N-7)$ th display line group;
 '4' for the $(8N-6)$ th display line group;
 '7' for the $(8N-5)$ th display line group;
 '2' for the $(8N-4)$ th display line group;
 '5' for the $(8N-3)$ th display line group;
 '0' for the $(8N-2)$ th display line group;
 '3' for the $(8N-1)$ th display line group; and
 55 '6' for the $(8N)$ th display line group.

[0025] As shown in Fig. 4F, the line dither offset values LD with the following values are allocated in the sixth

field:

'5' for the (8N-7)th display line group;
 '0' for the (8N-6)th display line group;
 '3' for the (8N-5)th display line group;
 '6' for the (8N-4)th display line group;
 '1' for the (8N-3)th display line group;
 '4' for the (8N-2)th display line group;
 '7' for the (8N-1)th display line group; and
 '2' for the (8N)th display line group.

[0026] As shown in Fig. 4G, the line dither offset values LD with the following values are allocated in the seventh field:

'3' for the (8N-7)th display line group;
 '6' for the (8N-6)th display line group;
 '1' for the (8N-5)th display line group;
 '4' for the (8N-4)th display line group;
 '7' for the (8N-3)th display line group;
 '2' for the (8N-2)th display line group;
 '5' for the (8N-1)th display line group; and
 '0' for the (8N)th display line group.

[0027] As shown in Fig. 4H, the line dither offset values LD with the following values are allocated in the eighth field:

'7' for the (8N-7)th display line group;
 '2' for the (8N-6)th display line group;
 '5' for the (8N-5)th display line group;
 '0' for the (8N-4)th display line group;
 '3' for the (8N-3)th display line group;
 '6' for the (8N-2)th display line group;
 '1' for the (8N-1)th display line group; and
 '4' for the (8N)th display line group.

[0028] The line dither offset value generation circuit 21 provides the adder 22 with the line dither offset values LD allocated to the display lines belonging to discharge cells corresponding with pixel data PD supplied by the pixel data conversion circuit 1.

[0029] The adder 22 provides the lower bit discard circuit 23 with line-offset-added pixel data LF, which is prepared by adding the line dither offset values LD to pixel data PD supplied by the pixel data conversion circuit 1. The lower bit discard circuit 23 discards the lower three bits of the line-offset-added pixel data LF and then supplies the remaining three upper bits of this data LF to the drive data conversion circuit 3 as multiple grayscale pixel data MD.

[0030] A drive data conversion circuit 3 converts multiple grayscale pixel data MD into 4-bit pixel drive data GD in accordance with a data conversion table shown in Fig. 5 and supplies the four-bit pixel drive data GD to a memory 4.

[0031] The memory 4 sequentially captures and stores the 4-bit pixel drive data GD. Each time the mem-

ory 4 finishes the writing of one image-frame (n rows $\times$ m columns) of pixel drive data $GD_{1,1}$ to $GD_{n,m}$, the memory 4 divides the pixel drive data $GD_{1,1}$ to $GD_{n,m}$ into bit digits (0th to 3rd bits) and reads one display line's worth of this data at a time in correspondence with the subfields SF0 to SF3 respectively. The memory 4 supplies m pixel drive data bits corresponding to one display line to a column electrode driver circuit 5 as the pixel drive data bits DB1 to DBm.

[0032] That is, in the subfield SF0, the memory 4 reads only the 0th bit of each of the pixel drive data $GD_{1,1}$ to $GD_{n,m}$ one display line at a time, and supplies the respective 0th bits to the column electrode driver circuit 5 as the pixel drive data bits DB1 to DBm. In the next subfield (i.e., subfield SF1), the memory 4 reads, one display line at a time, only the respective first bits of pixel drive data $GD_{1,1}$ to $GD_{n,m}$ and supplies these first bits to the column electrode driver circuit 5 as the pixel drive data bits DB1 to DBm. Next, in the subfield SF2, the memory 4 reads only the respective second bits of the pixel drive data $GD_{1,1}$ to $GD_{n,m}$ one display line at a time and supplies these second bits to the column electrode driver circuit 5 as pixel drive data bits DB1 to DBm. Subsequently, in the subfield SF3, the memory 4 reads only the respective third bits of the pixel drive data $GD_{1,1}$ to $GD_{n,m}$ one display line at a time and supplies these third bits to the column electrode driver circuit 5 as pixel drive data bits DB1 to DBm.

[0033] A drive control circuit 6 generates various timing signals for grayscale-driving the PDP 100 in accordance with the light emission drive sequences shown in the following drawings:

the first subfield: Fig. 6A;
 the second subfield: Fig. 6B;
 the third subfield: Fig. 6C;
 the fourth subfield: Fig. 6D;
 the fifth subfield: Fig. 6E;
 the sixth subfield: Fig. 6F;
 the seventh subfield: Fig. 6G; and
 the eighth subfield: Fig. 6H.

[0034] The drive control circuit 6 supplies these timing signals to the column electrode driver circuit 5, the row electrode Y driver circuit 7 and the row electrode X driver circuit 8 respectively. A series of driving shown in Figs. 6A to 6H is executed repeatedly.

[0035] The column electrode driver circuit 5, the row electrode Y driver circuit 7, and the row electrode X driver circuit 8 generate various drive pulses (not shown) to drive the PDP 100 as described below in accordance with the timing signals supplied by the drive control circuit 6, and apply these drive pulses to the column electrodes D_1 to D_m , row electrodes X_1 to X_n , and row electrodes Y_1 to Y_n of the PDP 100, respectively.

[0036] It should be noted that in the light emission drive sequence shown in Figs. 6A to 6H, each of the fields of the video input signal is constituted by the five

subfields SF0 to SF4.

[0037] The leading subfield SF0 sequentially executes a reset step R and an address step W0. The reset step R causes all the discharge cells $G_{(1,1)}$ to $G_{(n,m)}$ of the PDP 100 to perform a reset discharge all together and initializes the discharge cells $G_{(1,1)}$ to $G_{(n,m)}$ in a lit mode (state in which a wall charge of a predetermined amount is formed). In the address step W0, the discharge cells G arranged on the first to nth display lines of the PDP 100 are selectively made to perform an erase discharge in accordance with the pixel drive data GD as shown in Fig. 5, in sequence one display line at a time, so that the selected discharge cells are brought into an unlit mode (state where the wall charge has been erased or extinguished). The discharge cells in which the erasure discharge is not induced in this address step W0 retain the state up until immediately before this address step W0, that is, the lit mode.

[0038] Each of the subfields SF1 to SF3 are further divided into eight subfields SF1₁ to SF1₈, SF2₁ to SF2₈, and SF3₁ to SF3₈ respectively. Address steps W1 to W8 are executed in the subfields SF1₁ to SF1₈, SF2₁ to SF2₈, and SF3₁ to SF3₈ respectively. It should be noted that the subfield SF1 (SF2, SF3) may be referred to as a primary subfield and the subfield SF1_i (SF2_i, SF3_i) may be referred to as a secondary subfield.

[0039] In the address step W1, only discharge cells that are arranged in the (8N-7)th display lines (i.e., the 1st, 9th, 17th, ..., and (n-7)th display lines) among all the discharge cells $G_{(1,1)}$ to $G_{(n,m)}$ in the PDP 100, are selectively caused to perform an erasure discharge in accordance with the pixel drive data. As a result, discharge cells in which an erasure discharge is induced are set to the unlit mode, and discharge cells in which an erasure discharge is not induced retain the state up until immediately before the address step W1. That is, the address step W1 sets the discharge cells arranged on the (8N-7)th display lines to either the unlit or lit mode in accordance with the pixel drive data.

[0040] In the address step W2, only the discharge cells arranged on the (8N-6)th display lines (i.e., the 2nd, 10th, 18th, ..., and (n-6)th display lines) are selectively made to perform an erasure discharge in accordance with the pixel drive data. As a result, discharge cells in which an erasure discharge is induced are set to the unlit mode, and discharge cells in which an erasure discharge is not induced retain the state up until immediately before the address step W2. That is, the address step W2 sets the discharge cells arranged on the (8N-6)th display lines to either the unlit mode or the lit mode in accordance with the pixel drive data.

[0041] In the address step W3, only discharge cells arranged on the (8N-5)th display lines (i.e., the 3rd, 11th, 19th, ..., and (n-5)th display lines) are selectively made to perform an erasure discharge in accordance with the pixel drive data. As a result, discharge cells in which an erasure discharge is induced are set to the unlit mode, and discharge cells in which an erasure discharge is not

induced retain the state up until directly before the address step W3. That is, the address step W3 sets the discharge cells arranged on the (8N-5)th display lines to either the unlit or lit mode in accordance with the pixel drive data.

[0042] In the address step W4, only discharge cells arranged on the (8N-4)th display lines (i.e., the 4th, 12th, 20th, ..., and (n-4)th display lines) are selectively made to perform an erasure discharge in accordance with the pixel drive data. As a result, discharge cells in which an erasure discharge is induced are set to the unlit mode, and discharge cells in which an erasure discharge is not induced retain the state up until directly before the address step W4. That is, the address step W4 sets the discharge cells arranged on the (8N-4)th display lines to either the unlit or lit mode in accordance with the pixel drive data.

[0043] In the address step W5, only discharge cells arranged on the (8N-3)th display lines (i.e., the 5th, 13th, 21st, ..., and (n-3)th display lines) are selectively made to perform an erasure discharge in accordance with the pixel drive data. As a result, discharge cells in which an erasure discharge is induced are set to the unlit mode, and discharge cells in which an erasure discharge is not induced retain the state up until directly before the address step W5. That is, the address step W5 sets the discharge cells arranged on the (8N-3)th display lines to either the unlit or lit mode in accordance with the pixel drive data.

[0044] In the address step W6, only discharge cells arranged on the (8N-2)th display lines (i.e., the 6th, 14th, 22nd, ..., and (n-2)th display lines) are selectively made to perform an erasure discharge in accordance with the pixel drive data. As result, discharge cells in which an erasure discharge is induced are set to the unlit mode, and discharge cells in which an erasure discharge is not induced retain the state up until directly before the address step W6. That is, the address step W6 sets the discharge cells arranged on the (8N-2)th display lines to either the unlit or lit mode in accordance with the pixel drive data.

[0045] In the address step W7, only discharge cells arranged on the (8N-1)th display lines (i.e., the 7th, 15th, 23rd, ..., and (n-1)th display lines) are selectively made to perform an erasure discharge in accordance with the pixel drive data. Discharge cells in which an erasure discharge is induced are set to the unlit mode, and discharge cells in which an erasure discharge is not induced retain the state up until directly before the address step W7. That is, the address step W7 sets the discharge cells arranged on the (8N-1)th display lines to either the unlit or lit mode in accordance with the pixel drive data.

[0046] In the address step W8, only discharge cells arranged on the (8N)th display lines (i.e., the 8th, 16th, 24th, ..., and nth display lines) are selectively made to perform an erasure discharge in accordance with the pixel drive data. Discharge cells in which an erasure dis-

charge is induced are set to the unlit mode, and discharge cells in which an erasure discharge is not induced retain the state up until directly before the address step W8. That is, the address step W8 sets the discharge cells arranged on the (8N)th display lines to either the unlit or lit mode in accordance with the pixel drive data.

[0047] In the light emission drive sequence shown in Fig. 6A, the following address steps are executed in the subfields:

the address step W6 in the subfields SF1₁, SF2₁, SF3₁ respectively;
the address step W3 in the subfields SF1₂, SF2₂, SF3₂ respectively;
the address step W8 in the subfields SF1₃, SF2₃, SF3₃ respectively;
the address step W5 in the subfields SF1₄, SF2₄, SF3₄ respectively;
the address step W2 in the subfields SF1₅, SF2₅, SF3₅ respectively;
the address step W7 in the subfields SF1₆, SF2₆, SF3₆ respectively;
the address step W4 in the subfields SF1₇, SF2₇, SF3₇ respectively; and
the address step W1 in the subfields SF1₈, SF2₈, SF3₈ respectively.

[0048] In the light emission drive sequence shown in Fig. 6B, the following address steps are executed in the subfields:

the address step W2 in the subfields SF1₁, SF2₁, SF3₁ respectively;
the address step W7 in the subfields SF1₂, SF2₂, SF3₂ respectively;
the address step W4 in the subfields SF1₃, SF2₃, SF3₃ respectively;
the address step W1 in the subfields SF1₄, SF2₄, SF3₄ respectively;
the address step W6 in the subfields SF1₅, SF2₅, SF3₅ respectively;
the address step W3 in the subfields SF1₆, SF2₆, SF3₆ respectively;
the address step W8 in the subfields SF1₇, SF2₇, SF3₇ respectively; and
the address step W5 in the subfields SF1₈, SF2₈, SF3₈ respectively.

[0049] In the light emission drive sequence shown in Fig. 6C, the following address steps are executed in the subfields:

the address step W8 in the subfields SF1₁, SF2₁, SF3₁ respectively;
the address step W5 in the subfields SF1₂, SF2₂, SF3₂ respectively;
the address step W2 in the subfields SF1₃, SF2₃,

SF3₃ respectively;
the address step W7 in the subfields SF1₄, SF2₄, SF3₄ respectively;
the address step W4 in the subfields SF1₅, SF2₅, SF3₅ respectively;
the address step W1 in the subfields SF1₆, SF2₆, SF3₆ respectively;
the address step W6 in the subfields SF1₇, SF2₇, SF3₇ respectively; and
the address step W3 in the subfields SF1₈, SF2₈, SF3₈ respectively.

[0050] In the light emission drive sequence shown in Fig. 6D, the following address steps are executed in the subfields:

the address step W4 in the subfields SF1₁, SF2₁, SF3₁ respectively;
the address step W1 in the subfields SF1₂, SF2₂, SF3₂ respectively;
the address step W6 in the subfields SF1₃, SF2₃, SF3₃ respectively;
the address step W3 in the subfields SF1₄, SF2₄, SF3₄ respectively;
the address step W8 in the subfields SF1₅, SF2₅, SF3₅ respectively;
the address step W5 in the subfields SF1₆, SF2₆, SF3₆ respectively;
the address step W2 in the subfields SF1₇, SF2₇, SF3₇ respectively; and
the address step W7 in the subfields SF1₈, SF2₈, SF3₈ respectively.

[0051] In the light emission drive sequence shown in Fig. 6E, the following address steps are executed in the subfields:

the address step W3 in the subfields SF1₁, SF2₁, SF3₁ respectively;
the address step W8 in the subfields SF1₂, SF2₂, SF3₂ respectively;
the address step W5 in the subfields SF1₃, SF2₃, SF3₃ respectively;
the address step W2 in the subfields SF1₄, SF2₄, SF3₄ respectively;
the address step W7 in the subfields SF1₅, SF2₅, SF3₅ respectively;
the address step W4 in the subfields SF1₆, SF2₆, SF3₆ respectively;
the address step W1 in the subfields SF1₇, SF2₇, SF3₇ respectively; and
the address step W6 in the subfields SF1₈, SF2₈, SF3₈ respectively.

[0052] In the light emission drive sequence shown in Fig. 6F, the following address steps are executed in the subfields:

the address step W7 in the subfields SF1₁, SF2₁, SF3₁ respectively;
 the address step W4 in the subfields SF1₂, SF2₂, SF3₂ respectively;
 the address step W1 in the subfields SF1₃, SF2₃, SF3₃ respectively;
 the address step W6 in the subfields SF1₄, SF2₄, SF3₄ respectively;
 the address step W3 in the subfields SF1₅, SF2₅, SF3₅ respectively;
 the address step W8 in the subfields SF1₆, SF2₆, SF3₆ respectively;
 the address step W5 in the subfields SF1₇, SF2₇, SF3₇ respectively; and
 the address step W2 in the subfields SF1₈, SF2₈, SF3₈ respectively.

[0053] In the light emission drive sequence shown in Fig. 6G, the following address steps are executed in the subfields:

the address step W5 in the subfields SF1₁, SF2₁, SF3₁ respectively;
 the address step W2 in the subfields SF1₂, SF2₂, SF3₂ respectively;
 the address step W7 in the subfields SF1₃, SF2₃, SF3₃ respectively;
 the address step W4 in the subfields SF1₄, SF2₄, SF3₄ respectively;
 the address step W1 in the subfields SF1₅, SF2₅, SF3₅ respectively;
 the address step W6 in the subfields SF1₆, SF2₆, SF3₆ respectively;
 the address step W3 in the subfields SF1₇, SF2₇, SF3₇ respectively; and
 the address step W8 in the subfields SF1₈, SF2₈, SF3₈ respectively.

[0054] Further, in the light emission drive sequence shown in Fig. 6H, the following address steps are executed in the subfields:

the address step W1 in the subfields SF1₁, SF2₁, SF3₁ respectively;
 the address step W6 in the subfields SF1₂, SF2₂, SF3₂ respectively;
 the address step W3 in the subfields SF1₃, SF2₃, SF3₃ respectively;
 the address step W8 in the subfields SF1₄, SF2₄, SF3₄ respectively;
 the address step W5 in the subfields SF1₅, SF2₅, SF3₅ respectively;
 the address step W2 in the subfields SF1₆, SF2₆, SF3₆ respectively;
 the address step W7 in the subfields SF1₇, SF2₇, SF3₇ respectively; and
 the address step W4 in the subfields SF1₈, SF2₈, SF3₈ respectively.

[0055] In each of the subfields SF1₁ to SF1₈, SF2₁ to SF2₈, and SF3₁ to SF3₈, directly before the respective address steps W1 to W8, a sustain step I, which causes only the discharge cells set to the lit mode to discharge light continuously over the period '1', is executed.

[0056] In the final subfield SF4, only the sustain step I, which causes the discharge cells set to the lit mode to discharge light continuously over the period '1', is executed.

[0057] The drive control circuit 6 performs light emission driving as shown in Figs. 7 to 14 in accordance with the light emission drive sequences shown in Figs. 6A to 6H.

Fig. 7 shows light emission drive patterns based on the light emission drive sequence in Fig. 6A;

Fig. 8 shows light emission drive patterns based on the light emission drive sequence in Fig. 6B;

Fig. 9 shows light emission drive patterns based on the light emission drive sequence in Fig. 6C;

Fig. 10 shows light emission drive patterns based on the light emission drive sequence in Fig. 6D;

Fig. 11 shows light emission drive patterns based on the light emission drive sequence in Fig. 6E;

Fig. 12 shows light emission drive patterns based on the light emission drive sequence in Fig. 6F;

Fig. 13 shows light emission drive patterns based on the light emission drive sequence in Fig. 6G; and

Fig. 14 shows light emission drive patterns based on the light emission drive sequence in Fig. 6H.

[0058] When '1000' pixel drive data GD, which represents the lowest luminance, is supplied, a light emission display based on first grayscale driving is executed. Because the 0th bit of the pixel drive data GD is logic level 1, an erasure discharge (indicated by the black circles) is induced in the discharge cells in the address step W0 of the subfield SF0, and the discharge cells become the unlit mode. According to the driving scheme shown in Figs. 6A to 6H, the opportunity, in a single field display period, for discharge cells to shift from the unlit mode to the lit mode arises only in the reset step R of the leading subfield SF0. Accordingly, discharge cells that have become the unlit mode retain the unlit state in the course of the single field display period.

[0059] In other words, in the first grayscale driving in accordance with the '1000' pixel drive data GD, each discharge cell retains an unlit state in the course of a single field display period, thereby achieving the luminance level (brightness level) 0 as shown in Fig. 15.

[0060] When '0100' pixel drive data GD representing a luminance one level higher than that of the '1000' pixel drive data is supplied, a light emission display based on second grayscale driving is implemented. Because the first bit of the pixel drive data GD is logic level 1, an erasure discharge (indicated by overlapping circles) is induced in the discharge cells in the address steps W1 to W8 of the subfield SF1. Thereupon, because discharge

cells are initialized in the lit mode in the reset step R of the leading subfield SF₀, sustained discharge light emission is implemented continuously in the sustain steps I that exist in the interval up until the erasure discharge is induced. For example, in the light emission drive sequence shown in Fig. 6A, the address steps are executed as follows:

Address step W₆, which performs erasure discharge on the (8N-7)th display line group, is executed in the subfield SF_{1₁};
 Address step W₃, which performs erasure discharge on the (8N-6)th display line group, is executed in the subfield SF_{1₂};
 Address step W₈, which performs erasure discharge on the (8N-5)th display line group, is executed in the subfield SF_{1₃};
 Address step W₅, which performs erasure discharge on the (8N-4)th display line group, is executed in the subfield SF_{1₄};
 Address step W₂, which performs erasure discharge on the (8N-3)th display line group, is executed in the subfield SF_{1₅};
 Address step W₇, which performs erasure discharge on the (8N-2)th display line group, is executed in the subfield SF_{1₆};
 Address step W₄, which performs erasure discharge on the (8N-1)th display line group, is executed in the subfield SF_{1₇}; and
 Address step W₁, which performs erasure discharge on the (8N)th display line group, is executed in the subfield SF_{1₈}.

[0061] Accordingly, as indicated by the white and overlapping circles in Fig. 7, the discharge cells perform a sustained discharge continuously in the sustain steps I of the following subfields:

Subfields SF_{1₁} to SF_{1₈} for the (8N-7)th display line;
 Subfields SF_{1₁} to SF_{1₅} for the (8N-6)th display line;
 Subfields SF_{1₁} to SF_{1₂} for the (8N-5)th display line;
 Subfields SF_{1₁} to SF_{1₇} for the (8N-4)th display line;
 Subfields SF_{1₁} to SF_{1₄} for the (8N-3)th display line;
 Subfield SF_{1₁} for the (8N-2)th display line;
 Subfields SF_{1₁} to SF_{1₆} for the (8N-1)th display line;
 and
 Subfields SF_{1₁} to SF_{1₃} for the (8N)th display line.

[0062] That is, in the second grayscale driving in accordance with the '0100' pixel drive data GD, the discharge cells arranged on each display line are each driven at a luminance level corresponding with the period of the light emission produced by the sustained discharge induced in the course of a single field display period, as shown in Fig. 15. Specifically,

the discharge cells arranged on the (8N-7)th display line are at the luminance level '8';
 the discharge cells arranged on the (8N-6)th display

lines are at the luminance level '5';

the discharge cells arranged on the (8N-5)th display lines are at the luminance level '2';

the discharge cells arranged on the (8N-4)th display lines are at the luminance level '7';

the discharge cells arranged on the (8N-3)th display lines are at the luminance level '4';

the discharge cells arranged on the (8N-2)th display lines are at the luminance level '1';

the discharge cells arranged on the (8N-1)th display lines are at the luminance level '6'; and

the discharge cells arranged on the (8N)th display lines are at the luminance level '3'.

[0063] When '0010' pixel drive data GD representing a luminance one level higher than that of the '0100' pixel drive data is supplied, a light emission display based on third grayscale driving is performed. Because the second bit of the pixel drive data GD is logic level 1, an erasure discharge (indicated by overlapping circles) is induced in each discharge cell in the address steps W₁ to W₈ of the subfield SF₂. The discharge cells are initialized in the lit mode in the reset step R of the leading subfield SF₀, so that sustained discharge light emission is executed continuously in the sustain steps I that exist during the interval up until the erasure discharge is induced. For example, in the light emission drive sequence shown in Fig. 6A, the address steps are executed as follows:

address step W₆, which performs erasure discharge on the (8N-7)th display line group, is executed in the subfield SF_{2₁};

address step W₃, which performs erasure discharge on the (8N-6)th display line group, is executed in the subfield SF_{2₂};

address step W₈, which performs erasure discharge on the (8N-5)th display line group, is executed in the subfield SF_{2₃};

address step W₅, which performs erasure discharge on the (8N-4)th display line group, is executed in the subfield SF_{2₄};

address step W₂, which performs erasure discharge on the (8N-3)th display line group, is executed in the subfield SF_{2₅};

address step W₇, which performs erasure discharge on the (8N-2)th display line group, is executed in the subfield SF_{2₆};

address step W₄, which performs erasure discharge on the (8N-1)th display line group, is executed in the subfield SF_{2₇}; and

address step W₁, which performs erasure discharge on the (8N)th display line group, is executed in the subfield SF_{2₈}.

[0064] Accordingly, as indicated by the white and overlapping circles in Fig. 7, the discharge cells perform a sustained discharge continuously in the sustain steps I of the following subfields:

the (8N-7)th display line in the subfields SF1₁ to SF1₈ and the subfields SF2₁ to SF2₈;
 the (8N-6)th display line in the subfields SF1₁ to SF1₈ and the subfields SF2₁ to SF2₈;
 the (8N-5)th display line in the subfields SF1₁ to SF1₈ and the subfields SF2₁ to SF2₈;
 the (8N-4)th display line in the subfields SF1₁ to SF1₈ and the subfields SF2₁ to SF2₈;
 the (8N-3)th display line in the subfields SF1₁ to SF1₈ and the subfields SF2₁ to SF2₈;
 the (8N-2)th display line in the subfields SF1₁ to SF1₈ and the subfield SF2₁;
 the (8N-1)th display line in the subfields SF1₁ to SF1₈, and the subfields SF2₁ to SF2₈;
 the (8N)th display line in the subfields SF1₁ to SF1₈, and the subfields SF2₁ to SF2₈.

[0065] That is, in the third grayscale driving in accordance with the '0010' pixel drive data GD, the discharge cells arranged on each display line are each driven at a luminance level corresponding with the period of the light emission produced by the sustained discharge induced in the course of a single field display period, as shown in Fig. 15. Specifically,

the discharge cells arranged on the (8N-7)th display lines are at the luminance level '16';
 the discharge cells arranged on the (8N-6)th display lines are at the luminance level '13';
 the discharge cells arranged on the (8N-5)th display lines are at the luminance level '10';
 the discharge cells arranged on the (8N-4)th display lines are at the luminance level '15';
 the discharge cells arranged on the (8N-3)th display lines are at the luminance level '12';
 the discharge cells arranged on the (8N-2)th display lines are at the luminance level '9';
 the discharge cells arranged on the (8N-1)th display lines are at the luminance level '14'; and
 the discharge cells arranged on the (8N)th display lines are at the luminance level '11'.

[0066] When '0001' pixel drive data GD representing a luminance one level higher than that of the '0010' pixel drive data is supplied, a light emission display based on fourth grayscale driving is performed as detailed below. Because the third bit of the pixel drive data GD is logic level 1, an erasure discharge (indicated by overlapping circles) is induced in each discharge cell in the address steps W1 to W8 of the subfield SF3. The discharge cells are initialized in the lit mode in the reset step R of the leading subfield SF0, so that sustained discharge light emission is executed continuously in the sustain steps I that exist during the interval up until the erasure discharge is induced. For example, in the light emission drive sequence shown in Fig. 6A, the address steps are executed as follows:

Address step W6, which performs erasure discharge on the (8N-7)th display line group, is executed in the subfield SF3₁;

Address step W3, which performs erasure discharge on the (8N-6)th display line group, is executed in the subfield SF3₂;

Address step W8, which performs erasure discharge on the (8N-5)th display line group, is executed in the subfield SF3₃;

Address step W5, which performs erasure discharge on the (8N-4)th display line group, is executed in the subfield SF3₄;

Address step W2, which performs erasure discharge on the (8N-3)th display line group, is executed in the subfield SF3₅;

Address step W7, which performs erasure discharge on the (8N-2)th display line group, is executed in the subfield SF3₆;

Address step W4, which performs erasure discharge on the (8N-1)th display line group, is executed in the subfield SF3₇; and

Address step W1, which performs erasure discharge on the (8N)th display line group, is executed in the subfield SF3₈.

[0067] Accordingly, as indicated by the white and overlapping circles in Fig. 7, the discharge cells perform a sustained discharge continuously in the sustain steps I of the following subfields. Specifically,

Subfields SF1₁ to SF2₈ and the subfields SF3₁ to SF3₈ for the (8N-7)th display line;

Subfields SF1₁ to SF2₈ and the subfields SF3₁ to SF3₅ for the (8N-6)th display line;

Subfields SF1₁ to SF2₈ and the subfields SF3₁ to SF3₂ for the (8N-5)th display line;

Subfields SF1₁ to SF2₈ and the subfields SF3₁ to SF3₇ for the (8N-4)th display line;

Subfields SF1₁ to SF2₈ and the subfields SF3₁ to SF3₄ for the (8N-3)th display line;

Subfields SF1₁ to SF2₈ and the subfield SF3₁ for the (8N-2)th display line;

Subfields SF1₁ to SF2₈, and the subfields SF3₁ to SF3₆ for the (8N-1)th display line;

[0068] Subfields SF1₁ to SF2₈, and the subfields SF3₁ to SF3₃ for the (8N)th display line.

[0069] That is, in the fourth grayscale driving in accordance with the '0001' pixel drive data GD, the discharge cells each emit light at a luminance level corresponding with the period of the light emission produced by the sustained discharge induced in the course of a single field display period, as shown in Fig. 15. Specifically,

the discharge cells arranged on the (8N-7)th display lines are at the luminance level '24';

the discharge cells arranged on the (8N-6)th display lines are at the luminance level '21';

the discharge cells arranged on the (8N-5)th display lines are at the luminance level '18';

the discharge cells arranged on the (8N-4)th display lines are at the luminance level '23';

the discharge cells arranged on the (8N-3)th display lines are at the luminance level '20';

the discharge cells arranged on the (8N-2)th display lines are at the luminance level '17';

the discharge cells arranged on the (8N-1)th display lines are at the luminance level '22'; and

the discharge cells arranged on the (8N)th display lines are at the luminance level '19'.

[0070] When '0000' pixel drive data GD representing the highest luminance is supplied, a light emission display based on the fifth grayscale driving is implemented. Because all the bits of the pixel drive data GD are logic level 0, erasure discharge is not induced at all during the single field display period. Accordingly, the discharge cells discharge light continuously in the sustain steps I of the subfields SF1₁ to SF1₈, SF2₁ to SF2₈, SF3₁ to SF3₈, and SF4.

[0071] That is, in the fifth grayscale driving in accordance with the '0000' pixel drive data GD, the discharge cells each emit light at a luminance level corresponding with the period of the light emission produced by the sustained discharge induced in the course of a single field display period as shown in Fig. 15. Specifically,

the discharge cells arranged on the (8N-7)th display lines are at the luminance level '25';

the discharge cells arranged on the (8N-6)th display lines are at the luminance level '25';

the discharge cells arranged on the (8N-5)th display lines are at the luminance level '25';

the discharge cells arranged on the (8N-4)th display lines are at the luminance level '25';

the discharge cells arranged on the (8N-3)th display lines are at the luminance level '25';

the discharge cells arranged on the (8N-2)th display lines are at the luminance level '25';

the discharge cells arranged on the (8N-1)th display lines are at the luminance level '25'; and

the discharge cells arranged on the (8N)th display lines are at the luminance level '25'.

[0072] Therefore, in the above described driving, the first to fifth grayscale driving that is capable of representing luminance corresponding to five levels is executed in accordance with five different pixel drive data GD, namely, '1000', '0100', '0010', '0001', and '0000'. Here, different luminance weightings are applied to eight adjacent display lines, and the eight adjacent display lines are driven at different luminance levels determined by the respective luminance weightings, in each of the first to fifth grayscale driving.

[0073] For example, the following luminance weightings ('1' to '8') are allocated to the eight adjacent display lines in the driving according to the light emission drive sequence for the first field shown in Fig. 6A:

(8N-7)th display line: '8';
(8N-6)th display line: '5';
(8N-5)th display line: '2';
(8N-4)th display line: '7';

(8N-3)th display line: '4';

(8N-2)th display line: '1';

(8N-1)th display line: '6'; and

(8N)th display line: '3'.

[0074] The following luminance weightings are allocated to the eight adjacent display lines in the driving according to the light emission drive sequence for the second field shown in Fig. 6B:

(8N-7)th display line: '4';

(8N-6)th display line: '1';

(8N-5)th display line: '6';

(8N-4)th display line: '3';

(8N-3)th display line: '8';

(8N-2)th display line: '5';

(8N-1)th display line: '2'; and

(8N)th display line: '7'.

[0075] The following luminance weightings are allocated to the eight adjacent display lines in the driving according to the light emission drive sequence for the third field shown in Fig. 6C:

(8N-7)th display line: '6';

(8N-6)th display line: '3';

(8N-5)th display line: '8';

(8N-4)th display line: '5';

(8N-3)th display line: '2';

(8N-2)th display line: '7';

(8N-1)th display line: '4'; and

(8N)th display line: '1'.

[0076] The following luminance weightings are allocated to the eight adjacent display lines in the driving according to the light emission drive sequence for the fourth field shown in Fig. 6D:

(8N-7)th display line: '2';

(8N-6)th display line: '7';

(8N-5)th display line: '4';

(8N-4)th display line: '1';

(8N-3)th display line: '6';

(8N-2)th display line: '3';

(8N-1)th display line: '8'; and

(8N)th display line: '5'.

[0077] The following luminance weightings are allocated to the eight adjacent display lines in the driving according to the light emission drive sequence for the fifth field shown in Fig. 6E:

(8N-7)th display line: '7';

(8N-6)th display line: '4';

(8N-5)th display line: '1';

(8N-4)th display line: '6';

(8N-3)th display line: '3';

(8N-2)th display line: '8';

(8N-1)th display line: '5'; and
(8N)th display line: '2'.

[0078] The following luminance weightings are allocated to the eight adjacent display lines in the driving according to the light emission drive sequence for the sixth field shown in Fig. 6F:

(8N-7)th display line: '3';
(8N-6)th display line: '8';
(8N-5)th display line: '5';
(8N-4)th display line: '2';
(8N-3)th display line: '7';
(8N-2)th display line: '4';
(8N-1)th display line: '1'; and
(8N)th display line: '6'.

[0079] The following luminance weightings are allocated to the eight adjacent display lines in the driving according to the light emission drive sequence for the seventh field shown in Fig. 6G:

(8N-7)th display line: '5';
(8N-6)th display line: '2';
(8N-5)th display line: '7';
(8N-4)th display line: '4';
(8N-3)th display line: '1';
(8N-2)th display line: '6';
(8N-1)th display line: '3'; and
(8N)th display line: '8'.

[0080] The following luminance weightings are allocated to the eight adjacent display lines in the driving according to the light emission drive sequence for the eighth field shown in Fig. 6H:

(8N-7)th display line: '1';
(8N-6)th display line: '6';
(8N-5)th display line: '3';
(8N-4)th display line: '8';
(8N-3)th display line: '5';
(8N-2)th display line: '2';
(8N-1)th display line: '7'; and
(8N)th display line: '4'.

[0081] As indicated by the light emission drive patterns shown in:

Fig. 7 for driving that corresponds with the light emission drive sequence of Fig. 6A;
Fig. 8 for driving that corresponds with the light emission drive sequence of Fig. 6B;
Fig. 9 for driving that corresponds with the light emission drive sequence of Fig. 6C;
Fig. 10 for driving that corresponds with the light emission drive sequence of Fig. 6D;
Fig. 11 for driving that corresponds with the light emission drive sequence of Fig. 6E;

Fig. 12 for driving that corresponds with the light emission drive sequence of Fig. 6F;

Fig. 13 for driving that corresponds with the light emission drive sequence of Fig. 6G; and

Fig. 14 for driving that corresponds with the light emission drive sequence of Fig. 6H,

the discharge cells belonging to the eight adjacent display lines are made to emit light at respective different luminance levels based on the above weighting.

[0082] The actual drive operation executed in accordance with the video input signal will be described by taking the driving in the first field shown in Fig. 6A as an example.

[0083] When the 6-bit pixel data PD corresponding with each column of discharge cells belonging to the eight adjacent display lines are all 010100', the line dither offset value generation circuit 21 adds the line dither offset values LD shown in Fig. 4A to the pixel data PD of the display lines, respectively, as shown in Fig. 16. As a result of this addition of the line dither offset values LD, the following line-offset-added pixel data LF are obtained for each of the display lines, as shown in Fig. 16. Specifically,

(8N-7)th display line: the value LF is '010100';
(8N-6)th display line: the value LF is '010111';
(8N-5)th display line: the value LF is '011010';
(8N-4)th display line: the value LF is '010101';
(8N-3)th display line: the value LF is '011000';
(8N-2)th display line: the value LF is '011011';
(8N-1)th display line: the value LF is '010110'; and
(8N)th display line: the value LF is '011001'.

[0084] The lower bit discard circuit 23 discards the lower 3 bits of each of these line-offset-added pixel data LF, thereby obtaining the remaining upper 3 bits of data as the multiple grayscale pixel data MD. That is, as shown in Fig. 16, the following multiple grayscale pixel data MD are obtained for the eight adjacent display lines:

(8N-7)th display line: the data MD is '010';
(8N-6)th display line: the data MD is '010';
(8N-5)th display line: the data MD is '011';
(8N-4)th display line: the data MD is '010';
(8N-3)th display line: the data MD is '011';
(8N-2)th display line: the data MD is '011';
(8N-1)th display line: the data MD is '010'; and
(8N)th display line: the data MD is '011'.

[0085] These multiple grayscale pixel data MD are converted into 4-bit pixel drive data GD by the drive data conversion circuit 3. Specifically,

(8N-7)th display line: the data GD is '0010';
(8N-6)th display line: the data GD is '0010';
(8N-5)th display line: the data GD is '0001';
(8N-4)th display line: the data GD is '0010';
(8N-3)th display line: the data GD is '0001';
(8N-2)th display line: the data GD is '0001';

(8N-1)th display line: the data GD is '0010'; and
(8N)th display line: the data GD is '0001'.

[0086] Therefore, as a result of the light emission drive patterns shown in Fig. 7, the discharge cells belonging to these eight adjacent display lines are driven to emit light at the following luminance levels:

discharge cells arranged on the (8N-7)th display line: the luminance level '16';
discharge cells arranged on the (8N-6)th display line: the luminance level '13';
discharge cells arranged on the (8N-5)th display line: the luminance level '18';
discharge cells arranged on the (8N-4)th display line: the luminance level '15';
discharge cells arranged on the (8N-3)th display line: the luminance level '20';
discharge cells arranged on the (8N-2)th display line: the luminance level '17';
discharge cells arranged on the (8N-1)th display line: the luminance level '14'; and
discharge cells arranged on the (8N)th display line: the luminance level '19'.

[0087] Consequently, the luminance level produced by averaging the luminance levels of the eight display lines is observed.

[0088] As described above, the plasma display device shown in Fig. 3 drives each of the eight adjacent display lines to emit light such that the different line dither offset values LD are added to pixel data PD of the display lines and the different luminance weightings are applied to the display lines. As a result of this driving, so-called line dither processing, which allows the luminance difference between adjacent display lines to be generated, is implemented.

[0089] In the line dither processing, the bias of the luminance difference between adjacent display lines of the PDP 100 should be substantially uniform. To this end, the bias is limited to lie within a predetermined value in this embodiment. For example, when '010100' pixel data PD is supplied, the bias of the luminance difference is '2', as shown in Fig. 16. Specifically,

the luminance difference between the (8N-7)th and (8N-6)th display lines is '3';
the luminance difference between the (8N-6)th and (8N-5)th display lines is '5';
the luminance difference between the (8N-5)th and (8N-4)th display lines is '3';
the luminance difference between the (8N-4)th and (8N-3)th display lines is '5';
the luminance difference between the (8N-3)th and (8N-2)th display lines is '3';
the luminance difference between the (8N-2)th and (8N-1)th display lines is '3'; and
the luminance difference between the (8N-1)th and (8N)th display lines is '5'.

[0090] It should be noted that when other pixel data

PD are supplied, the bias of the luminance difference between the adjacent display lines is equal to or less than '2' in this embodiment.

[0091] For example, according to the light emission drive patterns shown in Fig. 7, discharge cells belonging to the eight adjacent display lines emit light at luminance levels corresponding to the five grayscales as shown in Fig. 15. In the line dither processing used in this embodiment, the line dither offset values LD are added to the pixel data PD so that when a certain display line is driven with kth grayscale driving ($k=1, 2, 3, 4, 5$), the adjacent display lines are driven at kth grayscale driving or ($k+1$)th grayscale driving. Accordingly, for example, when the discharge cells arranged on the (8N-7)th display line are driven to emit light at the luminance level '16' by means of the third grayscale driving, the discharge cells arranged on the (8N-6)th display line are driven to emit light at the luminance level '13' by means of the third grayscale driving, or are driven to emit light at the luminance level '21' by means of the fourth grayscale driving. Thus, when the discharge cells arranged on the (8N-6)th display line are driven with the third grayscale driving, the difference in luminance between the (8N-6)th display line and (8N-7) display line is '3', whereas when the discharge cells on the (8N-6)th display line are driven with the fourth grayscale driving, the luminance difference between the (8N-6)th display line and (8N-7) display line is '5'. The bias of these two luminance differences is therefore '2'.

[0092] In this manner, when the line dither processing is executed, the bias of the luminance differences between adjacent display lines is restricted in a predetermined range, so that a high quality dither-processed image with a smaller luminance bias is expressed.

[0093] Further, in the line dither processing according to this embodiment, the first to eighth fields of the video input signal constitute one cycle, and the weighting of the line dither processing for each of the eight adjacent display lines is changed for each field as shown in Fig. 17.

[0094] That is, the allocation of the following line dither processes to the respective display lines is changed for each field:

First line dither processing, which adds a '0' line dither offset value LD to the pixel data PD and performs light emission driving corresponding with an '8' luminance weighting;

Second line dither processing, which adds a '1' line dither offset value LD to the pixel data PD and performs light emission driving corresponding with a '7' luminance weighting;

Third line dither processing, which adds a '2' line dither offset value LD to the pixel data PD and performs light emission driving corresponding with a '6' luminance weighting;

Fourth line dither processing, which adds a '3' line dither offset value LD to the pixel data PD and per-

forms light emission driving corresponding with a '5' luminance weighting;

Fifth line dither processing, which adds a '4' line dither offset value LD to the pixel data PD and performs light emission driving corresponding with a '4' luminance weighting;

Sixth line dither processing, which adds a '5' line dither offset value LD to the pixel data PD and performs light emission driving corresponding with a '3' luminance weighting;

Seventh line dither processing, which adds a '6' line dither offset value LD to the pixel data PD and performs light emission driving corresponding with a '2' luminance weighting; and

Eighth line dither processing, which adds a '7' line dither offset value LD to the pixel data PD and performs light emission driving corresponding with a '1' luminance weighting.

[0095] As shown in Fig. 17, in the first field, the first to eighth line dither processes are allocated to the display lines as follows:

(8N-7)th display line: first line dither processing;
(8N-6)th display line: fourth line dither processing;
(8N-5)th display line: seventh line dither processing;

(8N-4)th display line: second line dither processing;
(8N-3)th display line: fifth line dither processing;
(8N-2)th display line: eighth line dither processing;
(8N-1)th display line: third line dither processing;
and
(8N)th display line: sixth line dither processing.

[0096] In the second field, the first to eighth line dither processes are allocated to the display lines as follows:

(8N-7)th display line: fifth line dither processing;
(8N-6)th display line: eighth line dither processing;
(8N-5)th display line: third line dither processing;
(8N-4)th display line: sixth line dither processing;
(8N-3)th display line: first line dither processing;
(8N-2)th display line: fourth line dither processing;
(8N-1)th display line: seventh line dither processing; and
(8N)th display line: second line dither processing.

[0097] In the third field, the first to eighth line dither processes are allocated to the display lines as follows:

(8N-7)th display line: third line dither processing;
(8N-6)th display line: sixth line dither processing;
(8N-5)th display line: first line dither processing;
(8N-4)th display line: fourth line dither processing;
(8N-3)th display line: seventh line dither processing;
(8N-2)th display line: second line dither processing;
(8N-1)th display line: fifth line dither processing; and

(8N)th display line: eighth line dither processing.

[0098] In the fourth field, the first to eighth line dither processes are allocated to the display lines as follows:

(8N-7)th display line: seventh line dither processing;
(8N-6)th display line: second line dither processing;
(8N-5)th display line: fifth line dither processing;
(8N-4)th display line: eighth line dither processing;
(8N-3)th display line: third line dither processing;
(8N-2)th display line: sixth line dither processing;
(8N-1)th display line: first line dither processing; and
(8N)th display line: fourth line dither processing.

[0099] In the fifth field, the first to eighth line dither processes are allocated to the display lines as follows:

(8N-7)th display line: second line dither processing;
(8N-6)th display line: fifth line dither processing;
(8N-5)th display line: eighth line dither processing;
(8N-4)th display line: third line dither processing;
(8N-3)th display line: sixth line dither processing;
(8N-2)th display line: first line dither processing;
(8N-1)th display line: fourth line dither processing;
and
(8N)th display line: seventh line dither processing.

[0100] In the sixth field, the first to eighth line dither processes are allocated to the display lines as follows:

(8N-7)th display line: sixth line dither processing;
(8N-6)th display line: first line dither processing;
(8N-5)th display line: fourth line dither processing;
(8N-4)th display line: seventh line dither processing;
(8N-3)th display line: second line dither processing;
(8N-2)th display line: fifth line dither processing;
(8N-1)th display line: eighth line dither processing;
and
(8N)th display line: third line dither processing.

[0101] In the seventh field, the first to eighth line dither processes are allocated to the display lines as follows:

(8N-7)th display line: fourth line dither processing;
(8N-6)th display line: seventh line dither processing;
(8N-5)th display line: second line dither processing;
(8N-4)th display line: fifth line dither processing;
(8N-3)th display line: eighth line dither processing;
(8N-2)th display line: third line dither processing;
(8N-1)th display line: sixth line dither processing;
and
(8N)th display line: first line dither processing.

[0102] In the eighth field, the first to eighth line dither processes are allocated to the display lines as follows:

(8N-7)th display line: eighth line dither processing;
 (8N-6)th display line: third line dither processing;
 (8N-5)th display line: sixth line dither processing;
 (8N-4)th display line: first line dither processing;
 (8N-3)th display line: fourth line dither processing;
 (8N-2)th display line: seventh line dither processing;
 and
 (8N-1)th display line: second line dither processing;
 and
 (8N)th display line: fifth line dither processing.

[0103] In this embodiment, the respective line dither processing is applied alternately to upper and lower display in the screen for each field.

[0104] For example, in Fig. 17, the fifth line dither processing, which adds a '4' line dither offset value LD to the pixel data PD and performs light emission driving corresponding with a '4' luminance weighting, is allocated to the (8N-3)th display line in the first field. However, in the second field, the fifth line dither processing is performed on the (8N-7)th display line located below the (8N-3)th display line in the screen as indicated by the arrow. In the third field, the fifth line dither processing is performed on the (8N-1)th display line located above the (8N-7)th display line as shown by the arrow. In the fourth field, the fifth line dither processing is performed on the (8N-5)th display line located below the (8N-1)th display line as indicated by the arrow. In the fifth field, the fifth line dither processing is performed on the (8N-6)th display line located above the (8N-5)th display line as indicated by the arrow. In the sixth field, the fifth line dither processing is performed on the (8N-2)th display line located below the (8N-6)th display line as indicated by the arrow. In the seventh field, the fifth line dither processing is performed on the (8N-4)th display line located above the (8N-2)th display line as indicated by the arrow. In the eighth field, the fifth line dither processing is performed on the (8N)th display line located below the (8N-4)th display line as indicated by the arrow.

[0105] Accordingly, there is a lower probability for the viewer of the picture displayed on the screen of the PDP 100 to continuously see the pixels emitting light with the same luminance while moving his or her eyes over the screen. Thus, a favorable dither display in which pseudo contours are not readily observed is obtained.

[0106] It should be noted that although, in the embodiment shown in Figs. 6A to 6H, the luminance weighting is the same in each of the subfields SF1 to SF4, that is, the whole light emission period in each sustain step I of each of the subfields SF1₁ to SF1₈, SF2₁ to SF2₈, SF3₁ to SF3₈, and SF4 is '1', the weighting for each subfield may be different.

[0107] For example, in place of the light emission drive sequence shown in Fig. 6A, a light emission drive sequence as shown in Fig. 18 may be adopted, in which the weighting of the subfields SF1 to SF4 are as follows:

Subfield SF1:1

Subfield SF2:2
 Subfield SF3:3
 Subfield SF4:4.

[0108] In this light emission drive sequence, the light emission period in the sustain step I of each of the subfields SF1₁ to SF1₈ is '1', the light emission period in the sustain step I of each of the subfields SF2₁ to SF2₈ is '2', the light emission period in the sustain step I of each of the subfields SF3₁ to SF3₈ is '3', and the light emission period in the sustain step I of the subfield SF4 is '4'. Fig. 19 shows light emission drive patterns based on the light emission drive sequence shown in Fig. 18.

[0109] Here, in the first grayscale driving corresponding with the '1000' pixel drive data GD, the discharge cells retain the unlit state in the course of the single field display period and driving at the luminance level 0 is performed.

[0110] In the second grayscale driving corresponding with the '0100' pixel drive data GD, as shown in Fig. 20, the discharge cells are driven at the following luminance levels:

the discharge cells arranged on the (8N-7)th display line at the luminance level '8';
 the discharge cells arranged on the (8N-6)th display line at the luminance level '5';
 the discharge cells arranged on the (8N-5)th display line at the luminance level '2';
 the discharge cells arranged on the (8N-4)th display line at the luminance level '7';
 the discharge cells arranged on the (8N-3)th display line at the luminance level '4';
 the discharge cells arranged on the (8N-2)th display line at the luminance level '1';
 the discharge cells arranged on the (8N-1)th display line at the luminance level '6'; and
 the discharge cells arranged on the (8N)th display line at the luminance level '3'.

[0111] In the third grayscale driving corresponding with the '0010' pixel drive data GD, as shown in Fig. 20, the discharge cells are driven at the following luminance levels:

the discharge cells arranged on the (8N-7)th display line at the luminance level '24';
 the discharge cells arranged on the (8N-6)th display line at the luminance level '18';
 the discharge cells arranged on the (8N-5)th display line at the luminance level '12';
 the discharge cells arranged on the (8N-4)th display line at the luminance level '22';
 the discharge cells arranged on the (8N-3)th display line at the luminance level '16';
 the discharge cells arranged on the (8N-2)th display line at the luminance level '10';
 the discharge cells arranged on the (8N-1)th display line at the luminance level '4'; and
 the discharge cells arranged on the (8N)th display line at the luminance level '1'.

play line at the luminance level '20'; and
the discharge cells arranged on the (8N)th display
line at the luminance level '14'.

[0112] In the fourth grayscale driving according to the
'0001' pixel drive data GD, as shown in Fig. 20, the dis-
charge cells are driven at the following luminance levels:

the discharge cells arranged on the (8N-7)th display
line at the luminance level '48';
the discharge cells arranged on the (8N-6)th display
line at the luminance level '39';
the discharge cells arranged on the (8N-5)th display
line at the luminance level '30';
the discharge cells arranged on the (8N-4)th display
line at the luminance level '45';
the discharge cells arranged on the (8N-3)th display
line at the luminance level '36';
the discharge cells arranged on the (8N-2)th display
line at the luminance level '27';
the discharge cells arranged on the (8N-1)th display
line at the luminance level '42'; and
the discharge cells arranged on the (8N)th display
line at the luminance level '33'.

[0113] With the fifth grayscale driving corresponding
with '0000' pixel drive data GD, which represents the
highest luminance, as shown in Fig. 20, all the discharge
cells belonging to the display lines of the PDP are driven
at the luminance level '52'.

[0114] In the driving shown in Figs. 18 and 19, be-
cause there is one or fewer opportunities for the dis-
charge cells to make the transition from the lit state to
the unlit state within a single field display period, the
flicker cycle is the same as the vertical synchronization
frequency of the video input signal. Therefore, when a
PAL-system television signal with a low vertical synchro-
nization frequency, or similar, is supplied as the video
input signal, flicker is more prominent.

[0115] In this embodiment, therefore, in order to re-
solve this problem, the light emission drive sequence
shown in Fig. 21 is adopted in place of the light emission
drive sequence shown in Fig. 18.

[0116] Similar to the driving shown in Fig. 18, the light
emission drive sequence shown in Fig. 21 uses the fol-
lowing luminance weightings for the subfields SF1, SF2,
SF3, and SF4:

Subfield SF1: luminance level 1 is allocated;
Subfield SF2: luminance level 2 is allocated;
Subfield SF3: luminance level 3 is allocated; and
Subfield SF4: luminance level 4 is allocated.

[0117] In addition, the subfields SF1 to SF3 are each
divided into eight subfields SF1₁ to SF1₈, SF2₁ to SF2₈,
and SF3₁ to SF3₈.

[0118] In Fig. 21, similar to the subfield SF0 shown in
Fig. 18, a reset step R, which initializes all the discharge

cells in the lit mode, and an address step W0, which
causes the selected discharge cells to make the transi-
tion to the unlit mode by causing these cells to selec-
tively perform an erasure discharge in accordance with
pixel drive data GD, in sequence one display line at a
time, are executed in the leading subfield SF01.

[0119] After the execution of the subfield SF01, the
subfields SF1₁ to SF1₈ are executed as detailed below.

[0120] First, the sustain step I, in which the discharge
cells set to the lit mode are made to repeatedly perform
a sustained discharge over period '1', and the address
step W6, in which only the discharge cells arranged on
the (8N-2)th display line are made to selectively perform
an erasure discharge in accordance with pixel drive data
GD, are executed in the leading subfield SF1₁ of the
subfield SF1. In the next subfield (i.e., subfield SF1₂),
the sustain step I, in which the discharge cells set to the
lit mode are made to repeatedly perform a sustained dis-
charge over period '1', and the address step W3, in
which only the discharge cells arranged on the (8N-5)th
display line are made to selectively perform an erasure
discharge in accordance with pixel drive data GD, are
executed. In the next subfield (i.e., subfield SF1₃), the
sustain step I, in which the discharge cells set to the lit
mode are made to repeatedly perform a sustained dis-
charge over period '1', and the address step W8, in
which only the discharge cells arranged on the (8N)th
display line are made to selectively perform an erasure
discharge in accordance with pixel drive data GD, are
executed. In the subfield SF1₄, the sustain step I, in
which the discharge cells set to the lit mode are made
to repeatedly perform a sustained discharge over period
'1', and the address step W5, in which only the discharge
cells arranged on the (8N-3)th display line are made to
selectively perform an erasure discharge in accordance
with pixel drive data GD, are executed. In the subfield
SF1₅, the sustain step I, in which the discharge cells set
to the lit mode are made to repeatedly perform a sus-
tained discharge over period '1', and the address step
W2, in which only the discharge cells arranged on the
(8N-6)th display line are made to selectively perform an
erasure discharge in accordance with pixel drive data
GD, are executed. In the subfield SF1₆, the sustain step
I, in which the discharge cells set to the lit mode are
made to repeatedly perform a sustained discharge over
period '1', and the address step W7, in which only the
discharge cells arranged on the (8N-1)th display line are
made to selectively perform an erasure discharge in ac-
cordance with pixel drive data GD, are executed. In the
subfield SF1₇, the sustain step I, in which the discharge
cells set to the lit mode are made to repeatedly perform
a sustained discharge over period '1', and the address
step W4, in which only the discharge cells arranged on
the (8N-4)th display line are made to selectively perform
an erasure discharge in accordance with pixel drive data
GD, are executed. In the subfield SF1₈, the sustain step
I, in which the discharge cells set to the lit mode are
made to repeatedly perform a sustained discharge over

period '1', and the address step W1, in which only the discharge cells arranged on the (8N-7)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed.

[0121] After the execution of the subfields SF1₁ to SF1₈, the subfield SF3 is executed as described below.

[0122] First, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '10', and the address step W6, in which only the discharge cells arranged on the (8N-2)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed in the leading subfield SF3₁ of the subfield SF3. In the next subfield (i.e., subfield SF3₂), the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', and the address step W3, in which only the discharge cells arranged on the (8N-5)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF3₃, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', and the address step W8, in which only the discharge cells arranged on the (8N)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF3₄, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', and the address step W5, in which only the discharge cells arranged on the (8N-3)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF3₅, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', and the address step W2, in which only the discharge cells arranged on the (8N-6)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF3₆, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', and the address step W7, in which only the discharge cells arranged on the (8N-1)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF3₇, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', and the address step W4, in which only the discharge cells arranged on the (8N-4)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF3₈, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', and the address step W1, in which only the discharge cells arranged on the (8N-7)th display line are made to selectively perform

an erasure discharge in accordance with pixel drive data GD, are executed.

[0123] After the execution of the subfields SF3₁ to SF3₈, the subfield SF02 is executed.

[0124] The reset step R, which initializes all the discharge cells in the lit mode, and an address step W0, which causes selected discharge cells to make the transition to the unlit mode by causing these cells to selectively perform an erasure discharge in accordance with pixel drive data GD, in sequence one display line at a time, are executed in the subfield SF02.

[0125] After the execution of the subfield SF02, the subfield SF2 is executed as detailed below.

[0126] First, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '9', and the address step W6, in which only the discharge cells arranged on the (8N-2)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed in the leading subfield SF2₁ of the subfield SF2. In the subfield SF2₂, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', and the address step W3, in which only the discharge cells arranged on the (8N-5)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF2₃, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', and the address step W8, in which only the discharge cells arranged on the (8N)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF2₄, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', and the address step W5, in which only the discharge cells arranged on the (8N-3)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF2₅, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', and the address step W2, in which only the discharge cells arranged on the (8N-6)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF2₆, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', and the address step W7, in which only the discharge cells arranged on the (8N-1)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF2₇, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', and the address step W4, in which only the discharge cells arranged on the (8N-4)th display line are made to selectively perform

an erasure discharge in accordance with pixel drive data GD, are executed. In the subfield SF_{2g}, the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', and the address step W₁, in which only the discharge cells arranged on the (8N-7)th display line are made to selectively perform an erasure discharge in accordance with pixel drive data GD, are executed.

[0127] After the execution of the subfields SF_{2₁} to SF_{2_g}, the subfield SF₄ is executed. In the subfield SF₄, only the sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '4', is implemented.

[0128] As described above, in the light emission drive sequence shown in Fig. 21, the reset step R, which initializes all the discharge cells in the lit mode is executed twice, namely, at the start of the first half of the single field display period and at the start of the second half of this period. In addition, the driving operations equivalent to the subfields SF₁ and SF₃ shown in Fig. 18 are executed in the first half of the single field display period, while the driving operations equivalent to the subfields SF₂ and SF₄ are executed in the second half.

[0129] Fig. 22 shows the pixel drive data GD and light emission drive pattern based on the light emission drive sequence shown in Fig. 21.

[0130] First, when '1000' pixel drive data GD, which represents the lowest luminance, is supplied, a light emission display based on the first grayscale driving is performed as detailed below. That is, as shown in Fig. 22, an erasure discharge (indicated by a black circle) is induced in each of the discharge cells in the address step W₀ of each of the subfields SF₀₁ and SF₀₂. In the driving shown in Fig. 21, the opportunity to set the discharge cells to the lit mode arises only twice in the course of the single field display period, namely, in the reset step R of the subfield SF₀₁ and in the reset step R of the subfield SF₀₂. Therefore, in the first grayscale driving according to the '1000' pixel drive data GD, a light emission display at the luminance level 0 is executed as a result of the discharge cells retaining the unlit mode in the course of the single field display period.

[0131] When pixel drive data GD '0100', which represents luminance that is one level higher than that of the pixel drive data '1000', is supplied, a light emission display based on second grayscale driving is performed as detailed below. That is, as shown in Fig. 22, an erasure discharge (indicated by overlapping circles) is induced in each of the discharge cells in the address steps W₁ to W₈ of the subfield SF₁, and an erasure discharge (indicated by a black circle) is induced in each of the discharge cells in the address step W₀ of the subfield SF₀₂. Because the discharge cells are initialized in the lit mode in the reset step R of the leading subfield SF₀₁, sustained discharge light emission (indicated by a white circle) is performed continuously in sustain steps I that exist during the interval up until the erasure discharge is induced. In the second grayscale driving according to

the '0100' pixel drive data GD, therefore, the discharge cells arranged on each display line are each driven to emit light at a luminance level that corresponds with the period of the light emission generated by the sustained discharge induced during the single field display period, that is,

the discharge cells arranged on the (8N-7)th display line are at the luminance level '8';

the discharge cells arranged on the (8N-6)th display line are at the luminance level '5';

the discharge cells arranged on the (8N-5)th display line are at the luminance level '2';

the discharge cells arranged on the (8N-4)th display line are at the luminance level '7';

the discharge cells arranged on the (8N-3)th display line are at the luminance level '4';

the discharge cells arranged on the (8N-2)th display line are at the luminance level '1';

the discharge cells arranged on the (8N-1)th display line are at the luminance level '6'; and

the discharge cells arranged on the (8N)th display line are at the luminance level '3'.

[0132] When '0010' pixel drive data GD that represents luminance that is one level higher than that of the '0100' pixel drive data, is supplied, a light emission display based on third grayscale driving is performed as detailed below. That is, as shown in Fig. 22, an erasure discharge (indicated by overlapping circles) is first induced in each of the discharge cells in the address steps W₁ to W₈ of the subfield SF₁. Because the discharge cells are initialized in the lit mode in the reset step R of the leading subfield SF₀₁, sustained discharge light emission (indicated by a white circle) is performed continuously in sustain steps I that exist during the interval up until the erasure discharge is induced. Further, in the reset step R of the subfield SF₀₂, all the discharge cells are once again initialized in the lit mode, so that sustained discharge light emission (indicated by a white circle) is continuously performed in sustain steps I that exist in the interval up until the erasure discharge (indicated by overlapping circles) is induced in each of the address steps W₁ to W₈ of the subfield SF₂. As shown in Fig. 21, in the sustain step I of each of the subfields SF_{1₁} to SF_{1_g}, and SF_{2₁} to SF_{2_g}, sustained discharge light emission is performed over period '1' and, in the sustain step I of the subfield SF_{2₁}, the sustained discharge light emission is performed over period '9'. Accordingly, in the third grayscale driving corresponding with the '0010' pixel drive data GD, the discharge cells arranged on each display line are driven to emit light at a luminance level that corresponds with the total period of the light emission generated by the sustained discharge induced in the sustain step I of each of the subfields SF₁ and SF₂ during the single field display period, that is,

the discharge cells arranged on the (8N-7)th display line are at the luminance level '24';

the discharge cells arranged on the (8N-6)th display line are at the luminance level '18';

the discharge cells arranged on the (8N-5)th display line are at the luminance level '12';

the discharge cells arranged on the (8N-4)th display line are at the luminance level '22';

the discharge cells arranged on the (8N-3)th display line are at the luminance level '16';

the discharge cells arranged on the (8N-2)th display line are at the luminance level '10';

the discharge cells arranged on the (8N-1)th display line are at the luminance level '20'; and

the discharge cells arranged on the (8N)th display line are at the luminance level '14'.

[0133] When '0001' pixel drive data GD, which represents a luminance that is one level higher than the 0010' pixel drive data, is supplied, a light emission display based on fourth grayscale driving is performed as detailed below. That is, as shown in Fig. 22, an erasure discharge (indicated by overlapping circles) is first induced in each of the discharge cells in the address steps W1 to W8 of the subfield SF3. Because the discharge cells are initialized in the lit mode in the reset step R of the leading subfield SF01, sustained discharge light emission (indicated by a white circle) is performed continuously in sustain steps I that exist during the interval up until the erasure discharge is induced. Then, in the reset step R of the subfield SF02, all the discharge cells are once again initialized in the lit mode, and sustained discharge light emission (indicated by a white circle) is performed continuously in sustain steps I that exist in the interval up until the erasure discharge (indicated by overlapping circles) is induced in the address steps W1 to W8 of the subfield SF2. As shown in Fig. 21, sustained discharge light emission is performed over period '1' in the sustain step I of each of the subfields SF1₁ to SF1₈, and SF2₂ to SF2₈, over period '9' in the sustain step I of the subfield SF2₁, over period '10' in the sustain step I of the subfield SF3₁, and over period '2' in the sustain step I of each of the subfields SF3₂ to SF3₈. Accordingly, in the fourth grayscale driving corresponding with the '0001' pixel drive data GD, the discharge cells arranged on each display line are each driven to emit light at a luminance level that corresponds with the total period of the light emission generated by the sustained discharge induced in the sustain steps I of each of the subfields SF1, SF3, and SF2 during the single field display period, that is,

the discharge cells arranged on the (8N-7)th display line are at the luminance level '48';

the discharge cells arranged on the (8N-6)th display line are at the luminance level '39';

the discharge cells arranged on the (8N-5)th display line are at the luminance level '30';

the discharge cells arranged on the (8N-4)th display line are at the luminance level '45';

the discharge cells arranged on the (8N-3)th display line are at the luminance level '36';

the discharge cells arranged on the (8N-2)th display line are at the luminance level '27';

the discharge cells arranged on the (8N-1)th display line are at the luminance level '42'; and

the discharge cells arranged on the (8N)th display line are at the luminance level '33'.

[0134] When '0000' pixel drive data GD, which represents the highest luminance, is supplied, a light emission display based on the fifth grayscale driving is performed as detailed below. In the fifth grayscale driving, erasure discharge is not induced at all during the single field display period as shown in Fig. 22, so that the discharge cells discharge light continuously in the sustain steps I of each of the subfields SF1₁ to SF1₈, SF2₁ to SF2₈, SF3₁ to SF3₈, and SF4. Therefore, the discharge cells arranged on each display line are driven to emit light at the luminance level '52'.

[0135] Similar to the driving shown in Figs. 18 and 19, therefore, the driving shown in Figs. 21 and 22 performs the light emission driving on the discharge cells arranged on eight adjacent display lines at five luminance levels as shown in Fig. 20.

[0136] In addition, in the driving shown in Figs. 21 and 22, when the discharge cells are caused to emit light (sustained discharge) continuously over a period determined by the pixel drive data in a single field display period, the driving is executed with dispersion by means of a first-half subfield group (SF1₁ to SF1₈ and SF3₁ to SF3₈) and a second-half subfield group (SF2₁ to SF2₈ and SF4). Accordingly, as shown in Fig. 22, there are two opportunities for the discharge cells to make the transition from the lit state to the unlit state within the single field display period in each of the third and fourth grayscale driving. Therefore, the frequency with which the discharge cells switch from the lit state to the unlit state is two times the vertical synchronization frequency, so that a favorable display is provided in which flicker is suppressed even when a PAL-system television signal with a low vertical synchronization frequency, or similar, is supplied as the video input signal.

[0137] In the driving shown in Figs. 21 and 22, the light emission period is allocated to the sustain step I of each subfield such that the luminance levels of the eight adjacent display lines are the same as those shown in Fig. 20 even when the discharge cells are driven to emit light by means of dispersion into two, namely with a first-half subfield group and a second-half subfield group. Specifically, the light emission periods are set as follows:

Subfields SF1₁ to SF1₈: period '1';

Leading subfield SF2₁ of the subfield SF2: period '9';

Subfields SF2₂ to SF2₈: period '1';

Leading subfield SF3₁ of the subfield SF3: period '10';

Subfields SF3₂ to SF3₈: period '2'.

[0138] That is, the light emission period in the leading subfield SF2₁ (SF3₁) of the lower subfields SF2₁ to SF2₈ (SF3₁ to SF3₈) in the subfield SF2 (SF3) is set larger

than the light emission period in subsequent subfields SF₂₂ to SF₂₈ (SF₃₂ to SF₃₈).

[0139] Here, the light emission period $T_{1ST}(i)$ of the sustain step I in the leading subfield SF of the subfield SF(i) satisfies the relation:

$$T_{1ST}(i) = \{[n-1] \cdot C(i-1) + C(i)\} / n - C(i-2) + T_{1ST}(i-2),$$

where n is a division number of the subfield SF;

C(i) is the light emission period corresponding with the weighting of the subfield SF(i);

C(i-1) is the light emission period corresponding with the weighting of the subfield SF(i-1);

C(i-2) is the light emission period corresponding with the weighting of the subfield SF(i-2);

$T_{1ST}(i)$ is light emission period of the leading subfield of the subfield SF(i); and

$T_{1ST}(i-2)$ is the light emission period of the leading subfield of the subfield SF(i-2).

[0140] Further, the light emission period T(i) of the sustain step I in each of the second and subsequent subfields of the subfield SF(i) is determined by the equation:

$$T(i) = \{C(i) - T_{1ST}(i)\} / (n-1).$$

[0141] In the above described embodiment, so-called selective erasure addressing is adopted in order to set each of the discharge cells to either the lit mode or unlit mode in accordance with the pixel data. Specifically, all the discharge cells are preset to the lit mode and the selected discharge cells are made to make the transition to the unlit mode in accordance with pixel data.

[0142] However, the present invention can be similarly applied when so-called selective write addressing is adopted. In the selective write addressing, all the discharge cells are preset to the unlit mode and a write discharge is induced in the selected discharge cells in accordance with pixel data so that these discharge cells make the transition to the lit mode.

[0143] Fig. 23 shows a light emission drive sequence for a case where a light emission drive sequence as shown in Fig. 21 is implemented with the selective write addressing. Fig. 24 shows light emission drive patterns that are executed based on the light emission drive sequence shown in Fig. 23.

[0144] When the selective write addressing is adopted, the drive data conversion circuit 3 shown in Fig. 3 converts multiple grayscale pixel data MD into 5-bit pixel drive data GD consisting of 0th to 4th bits in accordance with the data conversion table shown in Fig. 30. The drive control circuit 6 implements light emission drive control on the basis of the light emission drive sequence as shown in Fig. 23 in accordance with this pixel drive

data GD.

[0145] In the light emission drive sequence shown in Fig. 23, the subfields SF₀, SF₃₁ to SF₃₈, SF₂₁ to SF₂₈, SF₁₁ to SF₁₈, SF₄, and SF₂₁ to SF₂₈ are executed in sequence.

[0146] The reset step R, which initializes each of the discharge cells in the unlit mode by inducing a reset discharge in all the discharge cells to form a wall charge in each discharge cell, and the address step W₀, which sets the selected discharge cells in the lit mode by causing the write discharge in the selected discharge cells in accordance with the 0th bit of the pixel drive data GD, are executed in the subfield SF₀.

[0147] After the execution of the subfield SF₀, the subfield SF₃ is executed as follows.

[0148] In the subfield SF₃₁, the address step W₁, in which only the discharge cells arranged on the (8N-7)th display line are made to selectively perform a write discharge in accordance with the third bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', are executed. In the next subfield (i.e., subfield SF₃₂), the address step W₄, in which only the discharge cells arranged on the (8N-4)th display line are made to selectively perform a write discharge in accordance with the third bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', are executed. In the subfield SF₃₃, the address step W₇, in which only the discharge cells arranged on the (8N-1)th display line are made to selectively perform a write discharge in accordance with the third bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', are executed. In the subfield SF₃₄, the address step W₂, in which only the discharge cells arranged on the (8N-6)th display line are made to selectively perform a write discharge in accordance with the third bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', are executed. In the subfield SF₃₅, the address step W₅, in which only the discharge cells arranged on the (8N-3)th display line are made to selectively perform a write discharge in accordance with the third bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '2', are executed. In the subfield SF₃₆, the address step W₈, in which only the discharge cells arranged on the (8N)th display line are made to selectively perform a write discharge in accordance with the third bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are

discharge in accordance with the second bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', are executed. In the subfield SF2₅, the address step W5, in which only the discharge cells arranged on the (8N-3)th display line are made to selectively perform a write discharge in accordance with the second bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', are executed. In the subfield SF2₆, the address step W8, in which only the discharge cells arranged on the (8N)th display line are made to selectively perform a write discharge in accordance with the second bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', are executed. In the subfield SF2₇, the address step W3, in which only the discharge cells arranged on the (8N-5)th display line are made to selectively perform a write discharge in accordance with the second bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '1', are executed. In the subfield SF2₈, the address step W3, in which only the discharge cells arranged on the (8N-2)th display line are made to selectively perform a write discharge in accordance with the second bit of the pixel drive data GD and then set to the lit mode, and a sustain step I, in which the discharge cells set to the lit mode are made to repeatedly perform a sustained discharge over period '9', are executed.

[0155] Whether the write discharge is induced or not in the address steps W0 to W8 of the subfield SF0 is determined by the 0th bit of the pixel drive data GD shown in Fig. 24. Whether the write discharge is induced or not in the address steps W0 to W8 of the subfield SF1 is determined by the first bit of the pixel drive data GD. Whether the write discharge is induced or not in the address steps W0 to W8 of the subfield SF2 is determined by the second bit of the pixel drive data GD. Whether the write discharge is induced or not in the address steps W0 to W8 of the subfield SF3 is determined by the third bit of the pixel drive data GD. That is, only when the bit in question of the pixel drive data GD is logic level 1, the write discharge is induced in the discharge cells in the address step W of the subfield corresponding with this bit and such discharge cells are set to the lit mode. In the light emission driving sequence shown in Fig. 23, the opportunity to shift the discharge cells from the lit mode to the unlit mode in the course of a single field display period arises only in the reset steps R of the subfields SF0 and SF4.

[0156] Therefore, when '00000' pixel drive data GD representing the lowest luminance as shown in Fig. 24 is supplied, for example, a light emission display based

on the first grayscale driving is performed as detailed below. That is, as shown in Fig. 24, no write discharge (indicated by overlapping circles) is performed during the single field display period, so that a light emission display at the luminance level 0 is executed as a result of the respective discharge cells retaining the unlit mode during the single field display period.

[0157] When '01000' pixel drive data GD, which represents luminance one level higher than the '00000' pixel drive data, is supplied, a light emission display based on the second grayscale driving is performed as detailed below. That is, as shown in Fig. 24, a write discharge (indicated by overlapping circles) is induced in each of the address steps W1 to W8 in only the subfield SF1, so that sustained discharge light emission (indicated by a white circle) is performed continuously in sustain steps I that exist during the interval until the reset step R of the subfield SF4 is implemented after the write discharge is induced. According to the second grayscale driving for the '01000' pixel drive data GD, therefore, the discharge cells arranged on the display lines are each driven to emit light at a luminance level that corresponds with the period of the light emission generated by the sustained discharge that is induced during the single field display period. Specifically,

the discharge cells arranged on the (8N-7)th display line are at the luminance level '8';

the discharge cells arranged on the (8N-6)th display line are at the luminance level '5';

the discharge cells arranged on the (8N-5)th display line are at the luminance level '2';

the discharge cells arranged on the (8N-4)th display line are at the luminance level '7';

the discharge cells arranged on the (8N-3)th display line are at the luminance level '4';

the discharge cells arranged on the (8N-2)th display line are at the luminance level '1';

the discharge cells arranged on the (8N-1)th display line are at the luminance level '6'; and

the discharge cells arranged on the (8N)th display line are at the luminance level '3'.

[0158] When '01100' pixel drive data GD, which represents luminance one level higher than that of the '01000' pixel drive data, is supplied, a light emission display based on third grayscale driving is performed as detailed below. That is, as shown in Fig. 24, a write discharge (indicated by overlapping circles) is induced in respective discharge cells in the address steps W1 to W8 of the subfields SF1 and SF2. Accordingly, sustained discharge light emission (indicated by a white circle) is performed continuously in sustain steps I that exist during the interval until the reset step R of the subfield SF4 is implemented after the write discharge is induced in the subfield SF1. Then, after all the discharge cells are initialized in the unlit mode in the reset step R of the subfield SF4, a write discharge (indicated by overlapping circles) is induced again in the subfield SF2, and sustained discharge light emission (indicated by a white

circle) is executed continuously in subsequent sustain steps I. Therefore, in the third grayscale driving, the respective discharge cells are each driven to emit light at a luminance level that corresponds with the total number of light emission discharge, which is the total of the sustained discharge light emissions performed in the first half of the single field display period and the discharge light emissions performed in the second half of this period. Specifically,

the discharge cells arranged on the (8N-7)th display line are at the luminance level '24';

the discharge cells arranged on the (8N-6)th display line are at the luminance level '18';

the discharge cells arranged on the (8N-5)th display line are at the luminance level '12';

the discharge cells arranged on the (8N-4)th display line are at the luminance level '22';

the discharge cells arranged on the (8N-3)th display line are at the luminance level '16';

the discharge cells arranged on the (8N-2)th display line are at the luminance level '10';

the discharge cells arranged on the (8N-1)th display line are at the luminance level '20'; and

the discharge cells arranged on the (8N)th display line are at the luminance level '14'.

[0159] When '00110' pixel drive data GD, which represents luminance one level higher than that of the '01100' pixel drive data, is supplied, a light emission display based on the fourth grayscale driving is performed as detailed below. That is, as shown in Fig. 24, a write discharge (indicated by overlapping circles), is induced in respective discharge cells in the address steps W1 to W8 of each of the subfields SF3 and SF2. Accordingly, sustained discharge light emission (indicated by a white circle) is performed continuously in sustain steps I that exist during the interval until the reset step R of the subfield SF4 is implemented after the write discharge is induced in the subfield SF3. Then, after all the discharge cells are initialized in the unlit mode in the reset step R of the subfield SF4, a write discharge (indicated by overlapping circles) is induced once again in the subfield SF2, and sustained discharge light emission (indicated by a white circle) is executed continuously in subsequent sustain steps I. Therefore, in the fourth grayscale driving, the respective discharge cells are each driven to emit light at a luminance level that corresponds with the total number of light emission discharge, which is the total of the number of sustained discharge light emissions performed in the first half of the single field display period and the number of discharge light emissions performed in the second half of this period, that is,

the discharge cells arranged on the (8N-7)th display line are at the luminance level '48';

the discharge cells arranged on the (8N-6)th display line are at the luminance level '39';

the discharge cells arranged on the (8N-5)th display line are at the luminance level '30';

the discharge cells arranged on the (8N-4)th display

line are at the luminance level '45';

the discharge cells arranged on the (8N-3)th display line are at the luminance level '36';

the discharge cells arranged on the (8N-2)th display line are at the luminance level '27';

the discharge cells arranged on the (8N-1)th display line are at the luminance level '42'; and

the discharge cells arranged on the (8N)th display line are at the luminance level '33'.

[0160] When '10001' pixel drive data GD, which represents the highest luminance, is supplied, a light emission display based on fifth grayscale driving is performed as detailed below. That is, as shown in Fig. 24, a write discharge (indicated by overlapping circles) is induced in respective discharge cells in the address step W0 of each of the subfields SF0 and SF4. Accordingly, as shown in Fig. 24, all the discharge cells are kept in the lit mode during the single field display period and are driven to emit light at the luminance level '52', which corresponds with the total number of light emissions in all the sustain steps I within the single field display period.

Claims

1. A display panel driving method that performs grayscale driving of a display panel in accordance with pixel data derived from on a video signal, the display panel including pixel cells arranged on each of display lines of the display panel, the display lines being divided into a plurality of display line groups, each said display line group consisting of a plurality of adjacent display lines, the driving method comprising:

a light emission driving step in which, in accordance with the pixel data, the pixel cells arranged on the display lines in the display line group concerned are made to emit light continuously over different light emission periods based on weighting values allocated to the display lines in the display line group concerned, for each field display period of the video signal,

wherein each of the light emission periods is divided into two parts such that one part takes place in a first-half period of the field display period concerned and another part takes place in a second-half period of the field display period concerned, with each said part starting from a reset step.

2. The display panel driving method according to claim 1, wherein each said field display period comprises a plurality of subfields, and the light emission driving step comprises:

a first-half light emission driving step, which

comprises first to Mth address steps (M is an integer greater than one), in which in each of M consecutive lower subfields that constitute the subfield in the first-half period, the display lines are selected every M lines while the pixel cells

belonging to the selected display lines are set to a driving mode corresponding with the pixel data; and a first light emission step in which only those pixel cells whose drive mode is a lit mode immediately before or after each of the first to Mth address steps is made to emit light a number of times corresponding with the weighting of the subfield in the first-half period; and

a second-half light emission driving step, which comprises first to Nth address steps (N is an integer greater than one), in which in each of N consecutive lower subfields that constitute the subfield in the second-half period, the display lines are selected every N lines while the pixel cells belonging to the selected display lines are set to a driving mode corresponding with the pixel data; and a second light emission step in which only those pixel cells whose drive mode is a lit mode immediately before or after each of the first to Nth address steps is made to emit light a number of times corresponding with the weighting of the subfield in the second-half period.

3. The display panel driving method according to claim 2, wherein the number of light emissions allocated to the leading subfield among the M consecutive lower subfields in the first light emission step is larger than the number of light emissions allocated to each of the remaining lower subfields among the M consecutive lower subfields, and the number of light emissions allocated to the leading subfield among the N consecutive lower subfields in the second light emission step is larger than the number of light emissions allocated to each of the remaining lower subfields among the N consecutive lower subfields.

4. The display panel driving method according to claim 2 or 3, wherein the reset step initializes the driving mode of all the discharge cells in the lit mode, and is executed prior to the first to Mth address steps in the first-half period and is also executed prior to the first to Nth address steps in the second-half period.

5. A method of grayscale-driving a display panel based on pixel data derived from an input image signal, the display panel including a plurality of display lines, with a plurality of pixel cells serving as pixels being arranged on each of the plurality of display lines, the plurality of display lines being divided into a plurality of groups, each group consisting of a predetermined number of neighboring display lines,

each single field display period of the input image signal being divided into a plurality of primary subfields, the method comprising:

dividing the plurality of primary subfields of the field display period into a first subfield group, belonging to a first half of the field display period, and a second subfield group, belonging to a second half of the field display period; dividing at least one of the primary subfields in the first subfield group into a plurality of secondary subfields, and dividing at least one of the primary subfields in the second subfield group into a plurality of secondary subfields; performing a first reset step in only a leading primary subfield in the first subfield group to set all the pixel cells into a lit mode and a second reset step in only a leading primary subfield in the second subfield group to set all the pixel cells into the lit mode again; performing an addressing step, in each of the secondary subfields, to selectively set the pixel cells arranged on only a particular display line of each display line group, into an unlit mode based on the pixel data; and performing a sustain step, in each of the secondary subfields, to cause those pixel cells which are in the lit mode immediately prior to the addressing step, to emit light a number of times determined by weightings.

6. The driving method according to claim 5, wherein the pixel cells are brought into the lit mode from the leading secondary subfield in the first and second subfield groups alternately, as a light emission driving level increases.

7. The driving method according to claim 5 or 6, wherein the number of light emission performed by the leading secondary subfield in the sustain step is greater than the number of light emission performed by other secondary subfields in the respective sustain steps.

8. A method of grayscale-driving a display panel based on pixel data derived from an input image signal, the display panel including a plurality of display lines, with a plurality of pixel cells serving as pixels being arranged on each of the plurality of display lines, the plurality of display lines being divided into a plurality of groups, each group consisting of a predetermined number of neighboring display lines, each single field display period of the input image signal being divided into a plurality of primary subfields, the method comprising:

dividing the plurality of primary subfields of the field display period into a first subfield group,

belonging to a first half of the field display period, and a second subfield group, belonging to a second half of the field display period;
dividing at least one of the primary subfields in the first subfield group into a plurality of secondary subfields, and dividing at least one of the primary subfields in the second subfield group into a plurality of secondary subfields;
performing a first reset step in only a leading primary subfield in the first subfield group to set all the pixel cells into an unlit mode and a second reset step in only a leading primary subfield in the second subfield group to set all the pixel cells into the unlit mode again;
performing an addressing step, in each of the secondary subfields, to selectively set the pixel cells arranged on only a particular display line of each display line group, into a lit mode based on the pixel data; and
performing a sustain step, in each of the secondary subfields, to cause those pixel cells which are in the lit mode immediately after the addressing step, to emit light a number of times determined by weightings.

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9. The driving method according to claim 8, wherein the pixel cells are brought into the lit mode from a last secondary subfield in the first and second subfield groups alternately, as a light emission driving level increases.
10. The driving method according to claim 9, wherein the number of light emission performed by the last secondary subfield in the sustain step is greater than the number of light emission performed by other secondary subfields in the respective sustain steps.

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FIG. 1

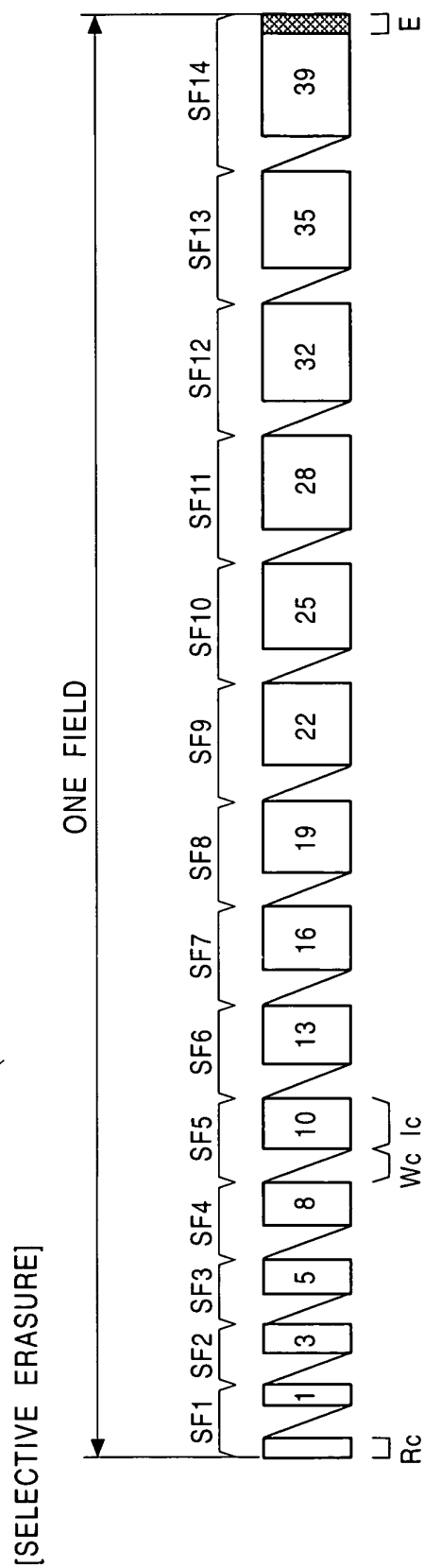


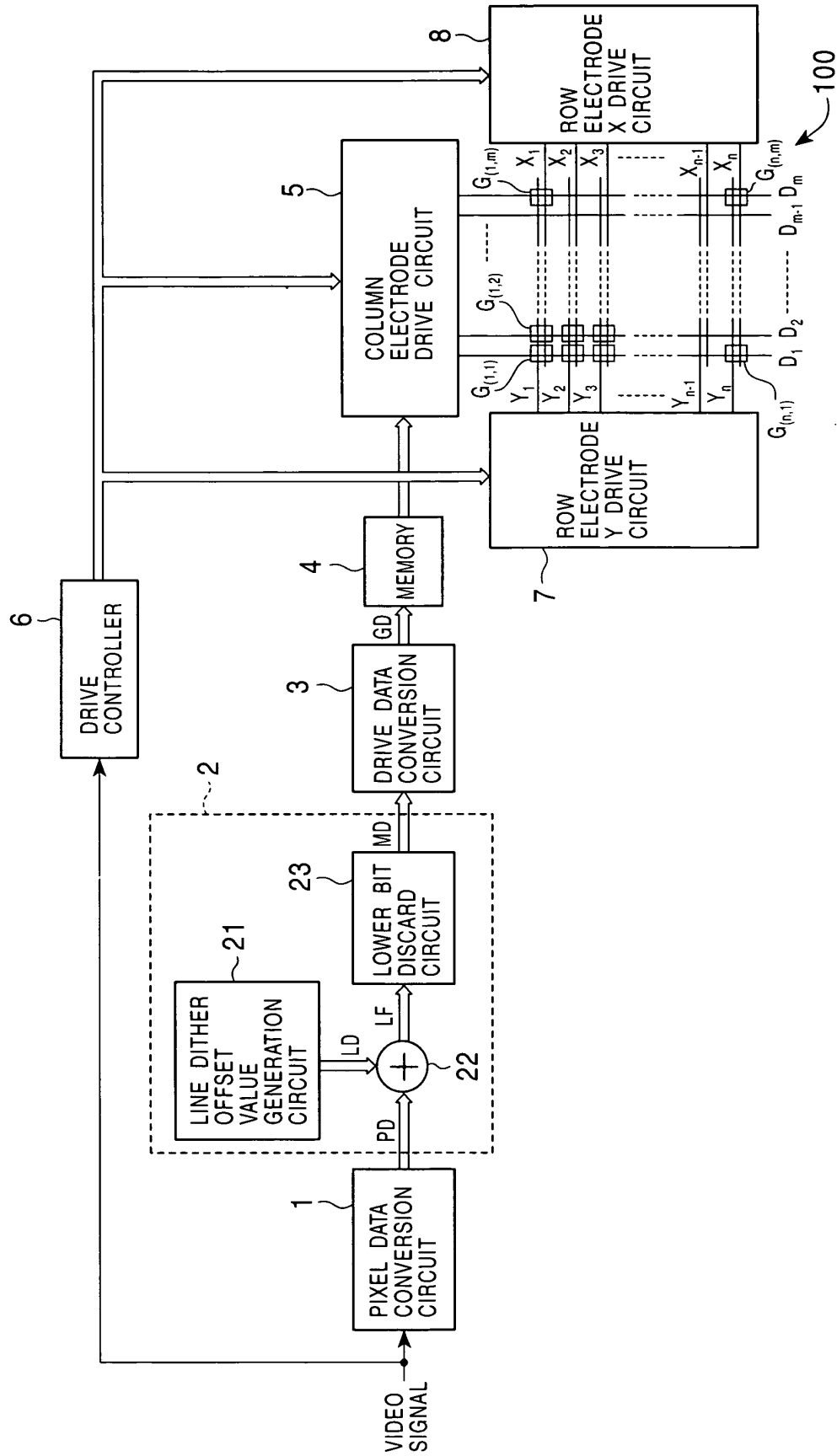
FIG. 2

[SELECTIVE ERASURE]

Ds	HD														LIGHT EMISSION DRIVE PATTERN IN ONE FIELD														LIGHT EMISSION LUMINANCE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	
0000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	●														0
0001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	○	●													1
0010	0	0	1	0	0	0	0	0	0	0	0	0	0	0	○	○	●												4
0011	0	0	0	1	0	0	0	0	0	0	0	0	0	0	○	○	○	●											9
0100	0	0	0	0	1	0	0	0	0	0	0	0	0	0	○	○	○	○	●										17
0101	0	0	0	0	0	1	0	0	0	0	0	0	0	0	○	○	○	○	○	●									27
0110	0	0	0	0	0	0	1	0	0	0	0	0	0	0	○	○	○	○	○	○	●								40
0111	0	0	0	0	0	0	0	1	0	0	0	0	0	0	○	○	○	○	○	○	○	●							56
1000	0	0	0	0	0	0	0	0	1	0	0	0	0	0	○	○	○	○	○	○	○	○	●						75
1001	0	0	0	0	0	0	0	0	0	1	0	0	0	0	○	○	○	○	○	○	○	○	○	○	●				97
1010	0	0	0	0	0	0	0	0	0	0	1	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	●		122
1011	0	0	0	0	0	0	0	0	0	0	0	1	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	150
1100	0	0	0	0	0	0	0	0	0	0	0	0	1	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	182
1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	○	217
1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

BLACK CIRCLE: SELECTIVE ERASURE DISCHARGE
 WHITE CIRCLE: LIGHT EMISSION

FIG. 3



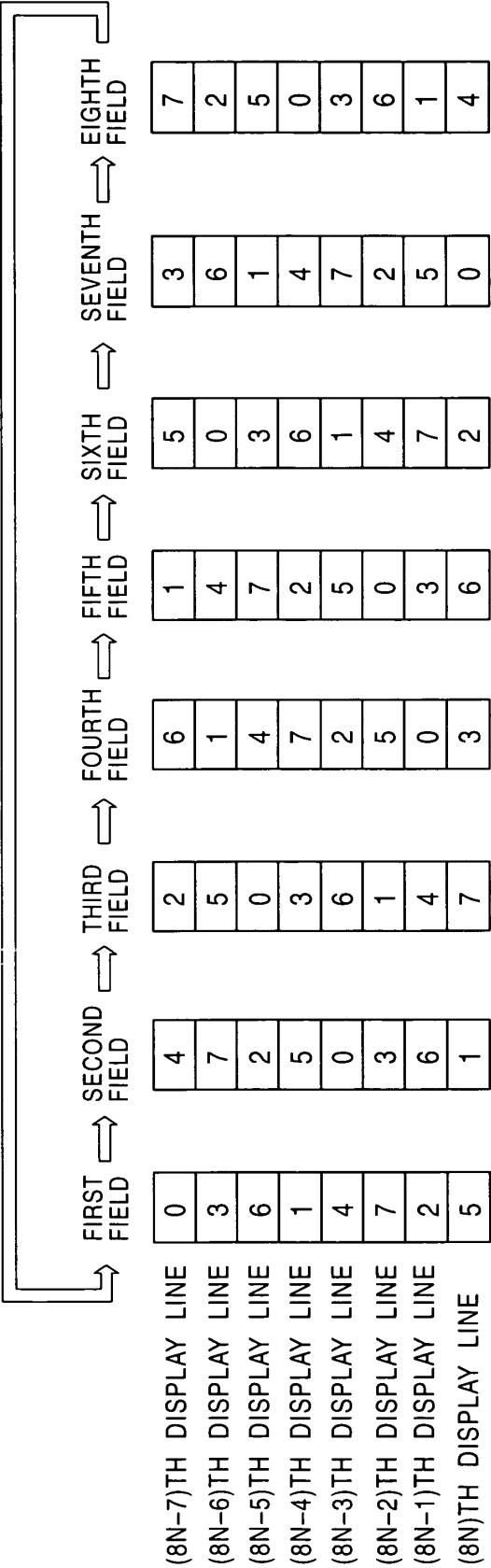


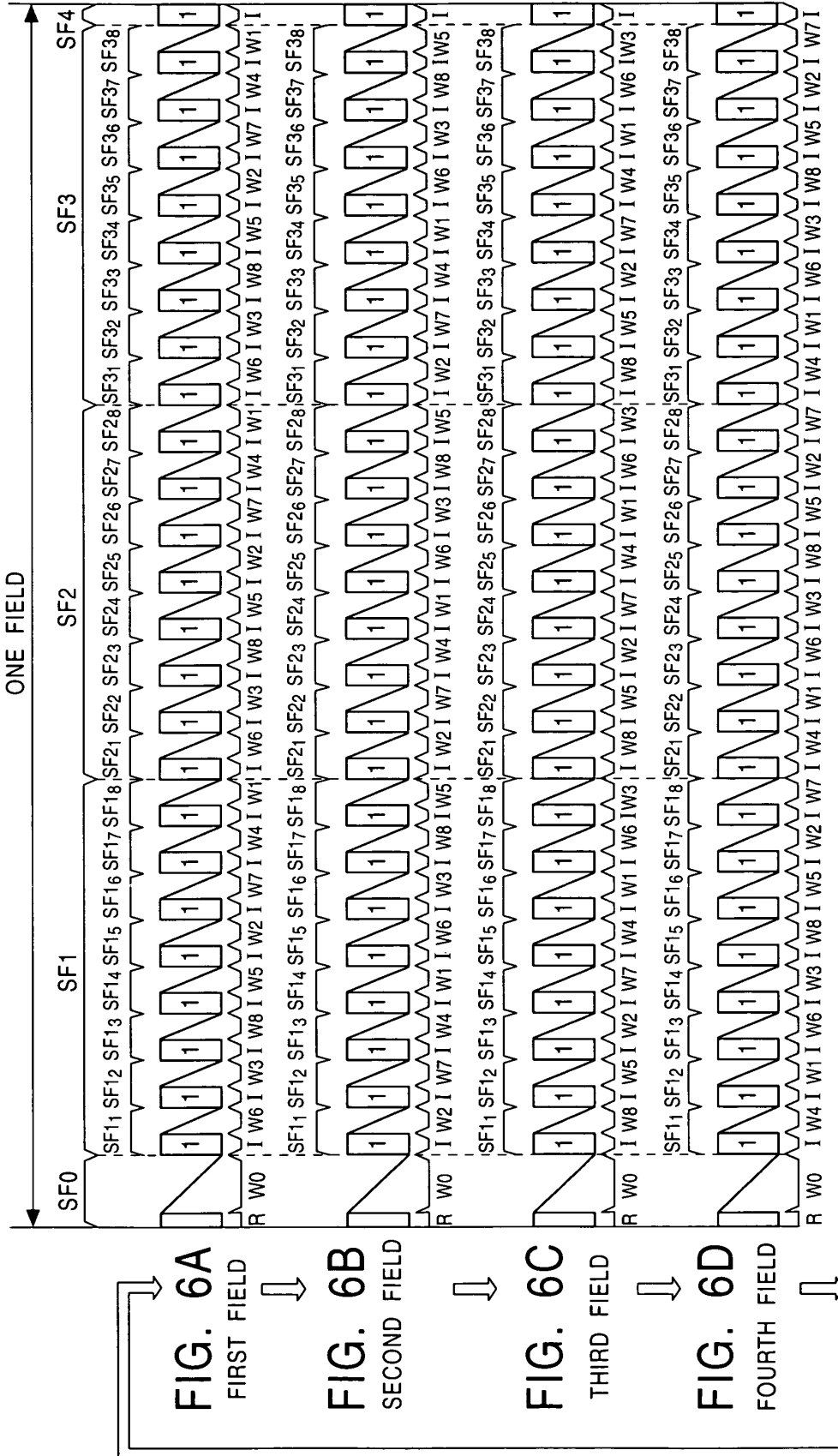
FIG. 4A FIG. 4C FIG. 4E FIG. 4G

FIG. 4B FIG. 4D FIG. 4F

FIG. 4H

FIG. 5

CONVERSION TABLE				
MD	GD			
	0	1	2	3
000	1	0	0	0
001	0	1	0	0
010	0	0	1	0
011	0	0	0	1
100	0	0	0	0



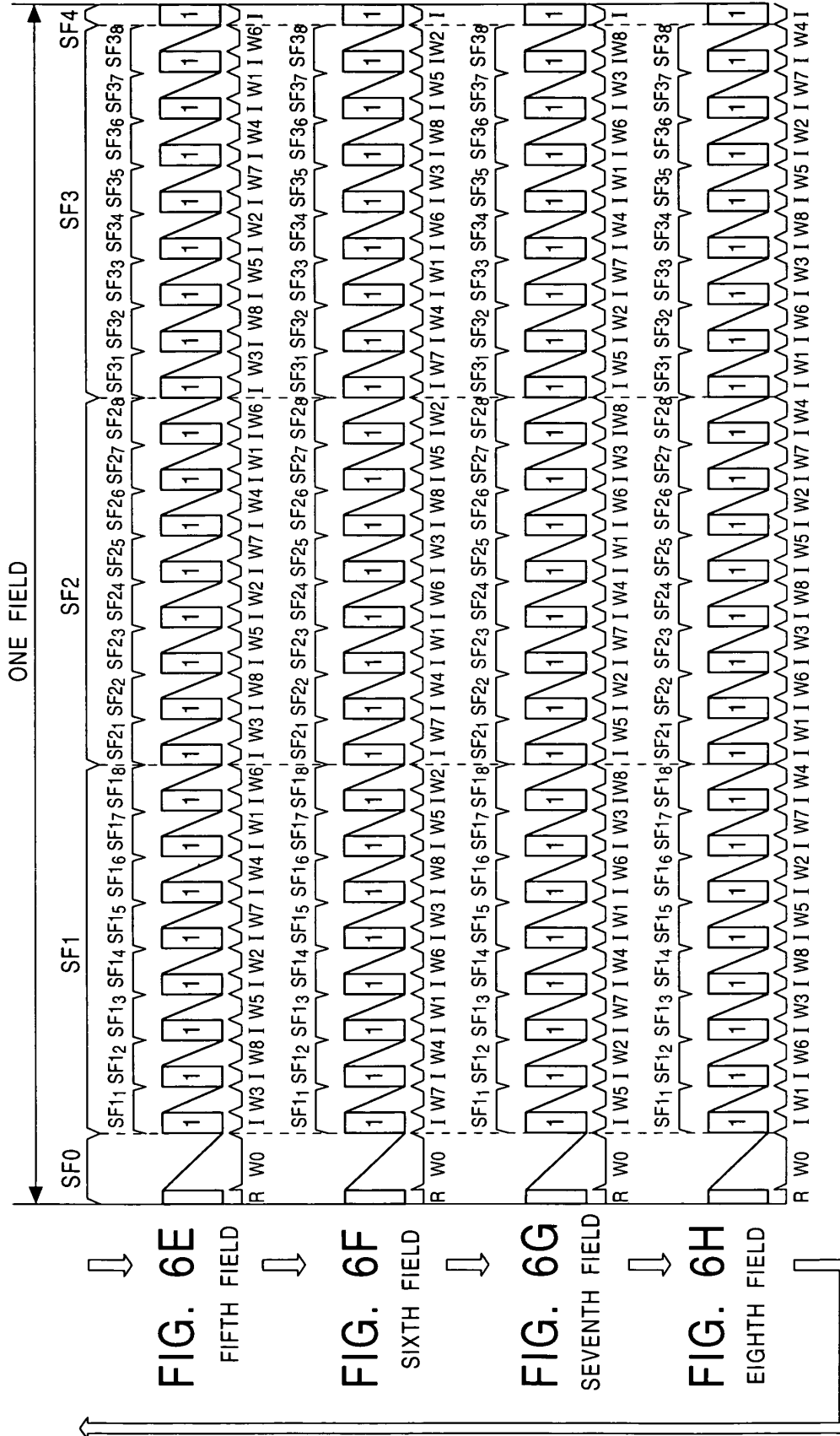


Fig. 8

[illegible]

FIG. 9

[illegible]

FIG. 10

[illegible]

FIG. 11

[illegible]

FIG. 12

[illegible]

FIG. 13

[illegible]

FIG. 15

	FIRST GRAYSCALE DRIVING	SECOND GRAYSCALE DRIVING	THIRD GRAYSCALE DRIVING	FOURTH GRAYSCALE DRIVING	FIFTH GRAYSCALE DRIVING
(8N-7)TH DISPLAY LINE		8	16	24	25
(8N-6)TH DISPLAY LINE	5	13	21	25	
(8N-5)TH DISPLAY LINE	2	10	18	25	
(8N-4)TH DISPLAY LINE		7	15	23	25
(8N-3)TH DISPLAY LINE	4	12	20	25	
(8N-2)TH DISPLAY LINE	1	9	17	25	
(8N-1)TH DISPLAY LINE		6	14	22	25
(8N)TH DISPLAY LINE	3	11	19	25	
(8N-7)TH DISPLAY LINE		8	16	24	25
⋮					
0					

FIG. 16

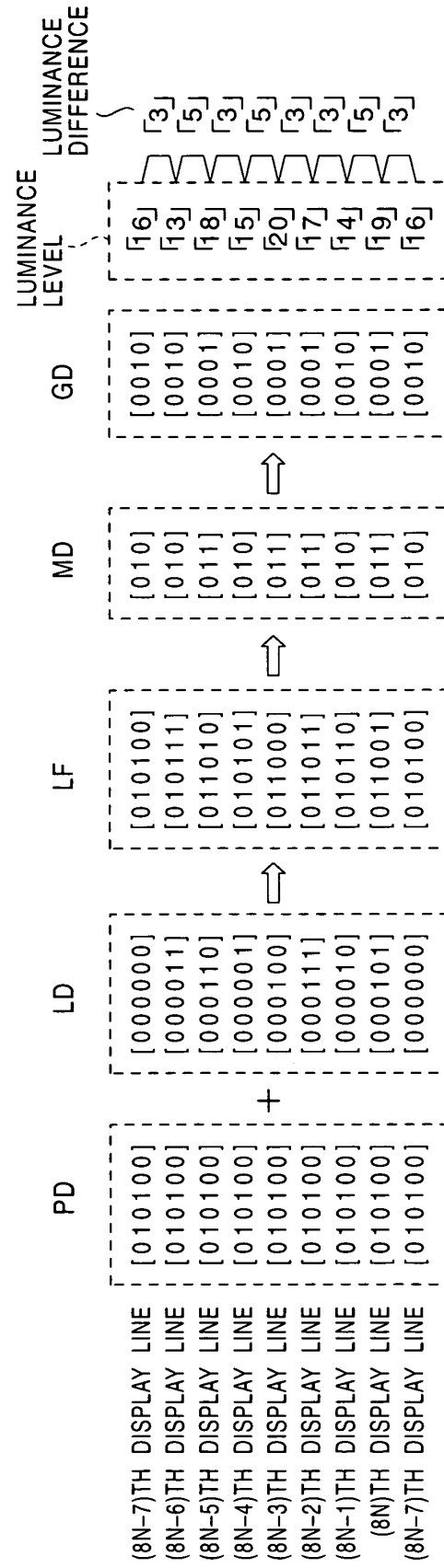


FIG. 17

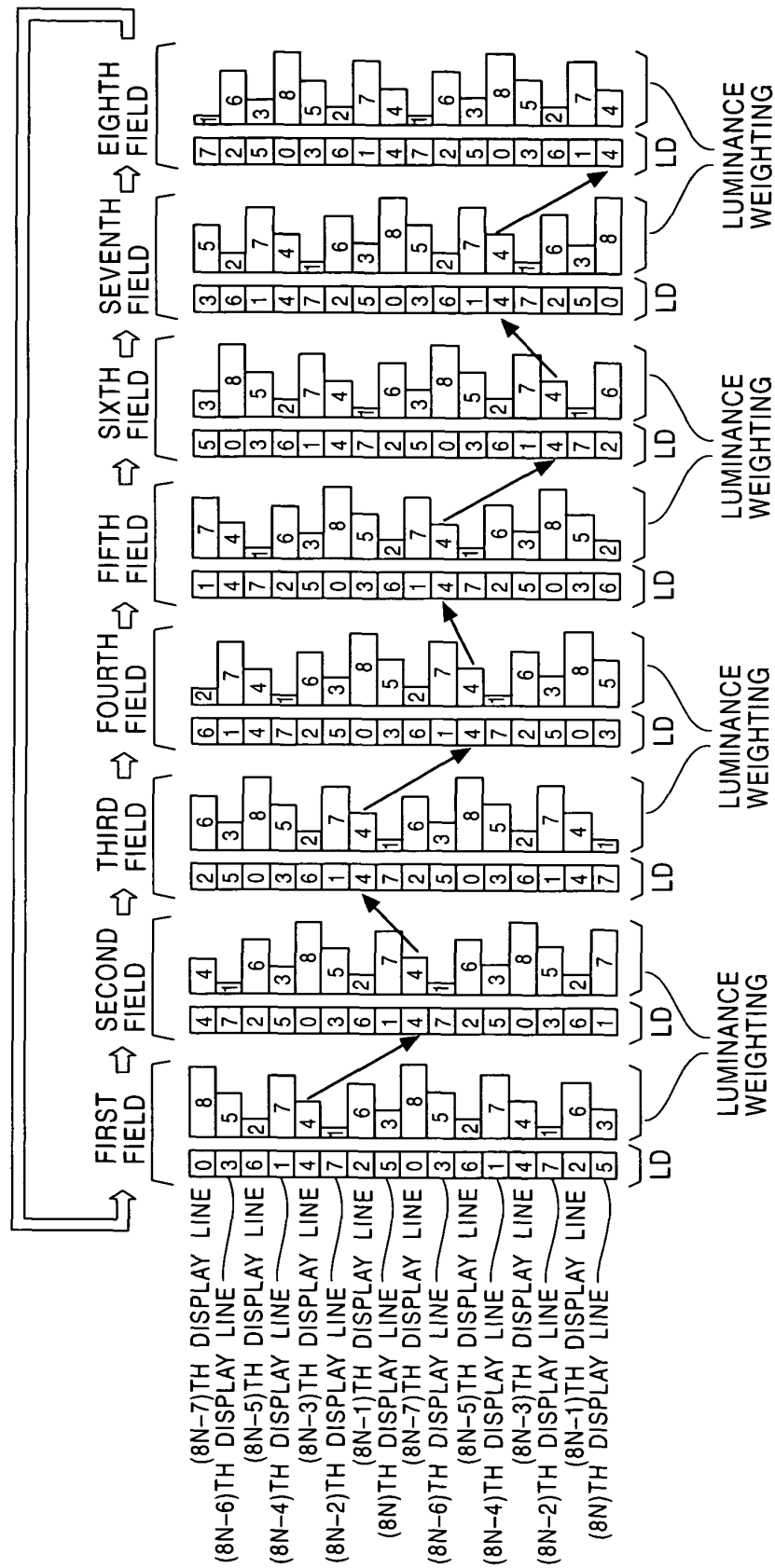


FIG. 18

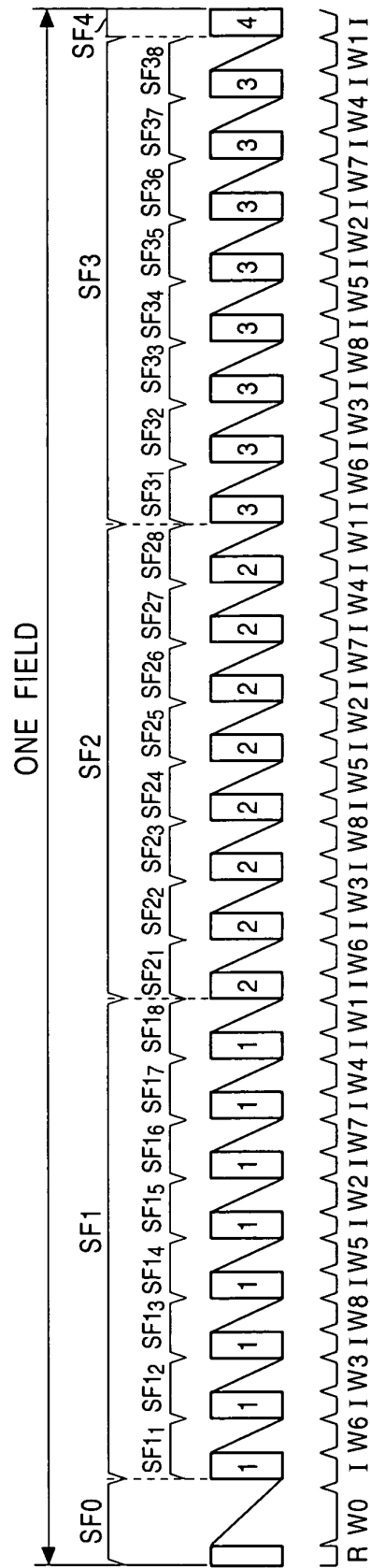


FIG. 20

	FIRST GRAYSCALE DRIVING	SECOND GRAYSCALE DRIVING	THIRD GRAYSCALE DRIVING	FOURTH GRAYSCALE DRIVING	FIFTH GRAYSCALE DRIVING
(8N-7)TH DISPLAY LINE		8	24	48	52
(8N-6)TH DISPLAY LINE	5		18	39	52
(8N-5)TH DISPLAY LINE	2	12	30		52
(8N-4)TH DISPLAY LINE		7	22	45	52
(8N-3)TH DISPLAY LINE	4	16	36		52
(8N-2)TH DISPLAY LINE	1	10	27		52
(8N-1)TH DISPLAY LINE		6	20	42	52
(8N)TH DISPLAY LINE	3	14	33		52
(8N-7)TH DISPLAY LINE		8	24	48	52
:					
:					
:					
0					

FIG. 21

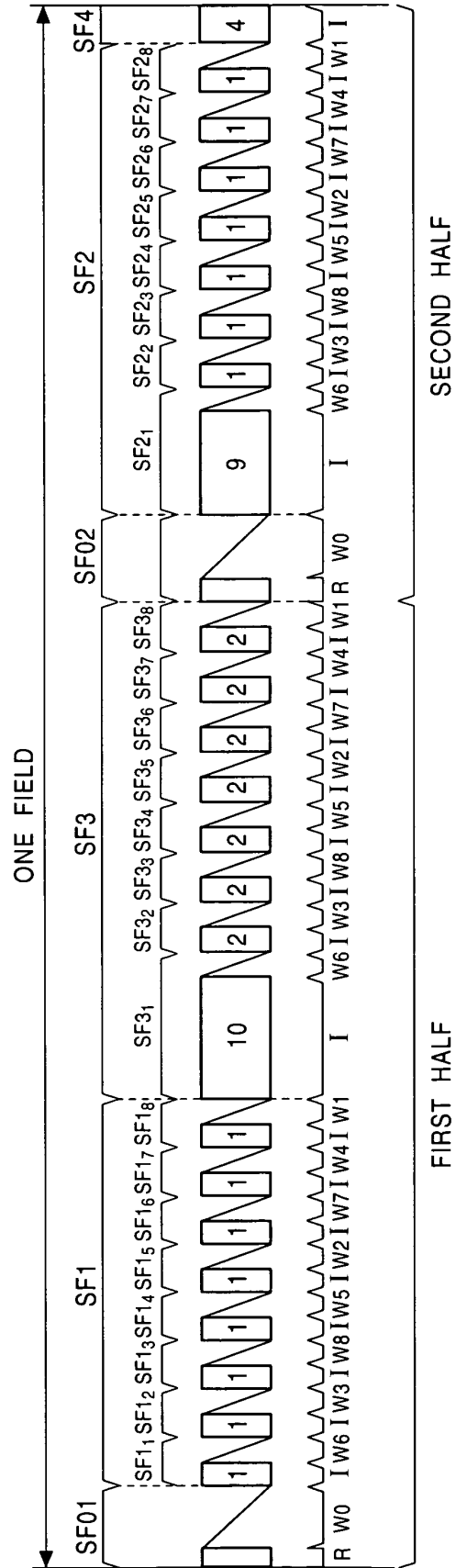


FIG. 22

G. 22	PIXEL DRIVE DATA GD 0 1 2 3	DISPLAY LINE	LIGHT EMISSION PATTERN																																LUMINANCE																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
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			SF 0	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	SF 15	SF 16	SF 17	SF 18	SF 19	SF 20	SF 21	SF 22	SF 23	SF 24	SF 25	SF 26	SF 27	SF 28	SF 29	SF 30	SF 31		SF 32	SF 33	SF 34	SF 35	SF 36	SF 37	SF 38	SF 39	SF 40	SF 41	SF 42	SF 43	SF 44	SF 45	SF 46	SF 47	SF 48	SF 49	SF 50	SF 51	SF 52																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
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FIG. 23

